DESIGN AND MODELING OF MILLIMETER-WAVE CMOS FOR WIRELESS TRANSCEIVERS

(無線トランシーバ用ミリ波 CMOS の設計とモデリングに関する研究)

Thesis by

LAI Chee Hong Ivan

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Abstract

The history of millimeter-wave is introduced from the time of Maxwell's predictions with his famous equations. History of the silicon integrated circuit developed separately from the 1960's. These two fields merged in the 1990's when the operating frequency of silicon circuits reached high gigahertz to make possible CMOS millimeter-wave circuits today. This research focuses on the use of CMOS 90nm process technology to implement millimeter-wave circuit building blocks for the wireless transceiver.

The high frequency analog portion of the wireless transceiver consists of the amplifiers, mixers and oscillators, each performing a specific function according to their roles in the transmitter or receiver. The design of each block is requires careful considerations, including frequency and power requirements for CMOS implementation. In addition, the interconnections will severely affect the performance of the devices. Therefore, simply interconnecting working devices are not trivial. In order to carry out the research work, designs are made using various software including high frequency circuit simulators. Chip layout for mask design is then made with the layout editor and checked with verification tools. Measurement results are finally obtained with the carefully-calibrated use of various chip measurement equipments, including a 110-GHz vector network analyzer.

The structure of the receiver or transmitter will almost always be realized as a string of operations where each operation is either one of these three frequency domain operations:

- *a filter*, for the suppression of signals outside the wanted channel;

- *an amplifier*, to adjust the signal level;
- *a mixer*, to change the center frequency.

To realize these circuit building blocks, fundamental passive device structures are first studied, designed and modeled. The substrate-coupled inductor model is a model that can accurately predict the performance of the on-chip inductor. The on-chip inductor is a common device used in many circuits. Techniques to implement this model for circuit simulators in a scalable manner using monomial equations are explained. Another basic passive device is the transmission line, which is used for interconnecting different building blocks as well as having other uses, is studied for its slow-wave phenomenon. Consequently, new transmission line structures with high performance are developed and modeled. With these passive devices and high performance transistors from a CMOS 90nm process technology, millimeter-wave circuits are developed. This includes a 20-26 GHz frequency up-conversion mixer for wide-band vehicular radar use, a 60-GHz frequency down-conversion mixer for the 59-66 GHz license-free band and a 50-GHz variable-gain amplifier. These circuits are designed, fabricated, measured and reported.

This thesis concludes with a summary of the circuits and devices have been explained in detail. A brief discussion of the future prospects for silicon millimeter-wave design is then made. For future works, improved CMOS process technology will be used and it will inevitably have with more stringent design requirements. However, it will provide devices with higher performances at higher millimeter-wave frequency. Circuits employing these devices can be explored and utilized.

List of Publications

Journals

[1] Ivan C. H. Lai and Minoru Fujishima, "A New On-Chip Substrate-Coupled Inductor Model Implemented With Scalable Expressions," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2491-2499, Nov. 2006.

[2] Ivan C. H. Lai, Hideyuki Tanimoto and Minoru Fujishima, "Characterization of High Q Transmission Line Structure for Advanced CMOS Processes," *IEICE Special Section on Emerging Microwave Techniques*, vol. E89-C, no. 12, pp. 1872-1879, Dec. 2006.

[3] Ivan C. H. Lai, Chiaki Inui and Minoru Fujishima, "CMOS on-chip stacked Marchand balun for millimeter-wave applications," IEICE Electron. Express, vol. 4, no. 2, pp. 48-53, Jan. 2007.

[4] Ivan C. H. Lai and Minoru Fujishima, "On-chip asymmetric coaxial waveguide structure for chip area reduction," *Japanese Journal of Applied Physics Special Issue Part 1*, vol. 46, no. 4B, Apr. 2007. (To be published)

[5] Ivan C. H. Lai and Minoru Fujishima, "An Integrated Low-Power 20-26 GHz CMOS Up-Conversion Mixer Using New Stacked Marchand Baluns," *IEICE Special Section on Low-Power, High Speed LSIs and Related Technologies*, vol. E90-C, no. 4, Apr. 2007. (To be published)

International Conferences

[1] Ivan C. H. Lai and Minoru Fujishima, "Simple modeling expressions for substrate network of on-chip inductors," *Int. Conf. on Microwave Test Structures*, vol. 18, pp. 113-118, Apr. 2005.

[2] M. Fujishima, K. Yamamoto, and I.C.H. Lai, "High-performance RFCMOS designs for high-speed and secure communications," *International Symposium on Advanced Electronics for Future Generations*, pp. 141-146, Oct. 2005.

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[4] Ivan C. H. Lai and Minoru Fujishima, "An Integrated 20-26 GHz CMOS Up-Conversion Mixer with Low Power Consumption," *European Solid-State Circuits Conf. Proc.*, pp. 400-403, Sep. 2006.

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[6] Ivan C. H. Lai and Minoru Fujishima, "Pseudo-Millimeter-Wave Up-Conversion Mixer with On-Chip Balun for Vehicular Radar Systems," Proc. 12th Asia and South Pacific Design Automation Conf., pp. 106-107, Jan. 2007.

[7] Ivan C. H. Lai and Minoru Fujishima, "High-Q Slow-Wave Transmission Line for Chip Area Reduction on Advanced CMOS Processes," *Int. Conf. on Microwave Test Structures*, Mar. 2007. (To be published)

[8] Ivan C. H. Lai, Yuki Kambayashi and Minoru Fujishima, "50-GHz Double-Balanced Up-Conversion Mixer Using CMOS 90nm Process," *Int. Symposium On Circuits and Systems*, May 2007. (To be published)

Local Conferences

[1] C. H. Lai, Ningyi Wang and Minoru Fujishima, "A gain-boosted amplifier based on inductive gate cascode circuit," *IEICE Silicon Analog RF Conf.*, Aug. 2005.

[2] Hideyuki Tanimoto, Ivan C. H. Lai and Minoru Fujishima, "Slow-Wave Coplanar Waveguide for Area-Reduction," *IEICE Electronic Society Conf.*, Sep. 2005.

[3] Ivan C. H. Lai and Minoru Fujishima, "Substrate-coupled inductor model for circuit design simulations," *IEICE Integrated Circuits and Devices 2005-199*, pp. 43-48, Dec. 2005.

[4] C-H. I. Lai and Minoru Fujishima, "High Q Transmission Line Structure for Advanced CMOS Processes," *IEICE Silicon Analog RF Conf.*, Aug. 2006.

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[7] Minoru Fujishima, Ivan C.-H. Lai and Ahmet Oncu, "Millimeter-Wave CMOS Systems for Secure-Life Electronics," *COE Symp. on Adv. Electronics for Future Generations – Secure-Life Electronics for Quality Life and Society*, pp. 147-152, Jan. 2007.

[8] Ivan Chee-Hong Lai and Minoru Fujishima, "CMOS Variable Gain Amplifier using Gain-Boosting Resonator," *IEICE General Conf.*, Mar. 2007. (To be published)

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Chapter 1

Introduction

This introduction will provide a brief history and motivation of this research on millimeter waves. Technical and economic challenges will be introduced before detailing the specific goals of this research. Technical challenges include the considerations in the design of the millimeter-wave transceiver, the use of the design tools required to realize the transceiver and the careful use of the measurement equipments to verify the performance of the circuits.

1.1 History and Motivations

Millimeter-wave is understood as the wavelength of a propagating electromagnetic signal that is less than 10mm. This wavelength corresponds to the frequency band above 30 GHz in free-space. It is noted that the first millimeter wave activity occurred in the 1890's, at which Hertz had performed experiments confirming Maxwell's theory predicting the possibility of radio waves. The early methods used in generating waves at this high frequency involve the use of spark gap generator. Further works by J. C. Bose of Presidency College, Calcutta, India, investigated a source using spark gap having platinum electrodes specially shaped to emphasize the radiation at millimeter waves and made the first quantitative measurements at wavelengths down to 5mm in that period [1]. Figure 1.1 shows the simplified description of the spark gap generator used. Figure 1.1 (a) shows the radiator used to generated 5-mm radiation, while Fig. 1.1 (b) shows the arrangement with a lens L at the exit of the waveguide [2].

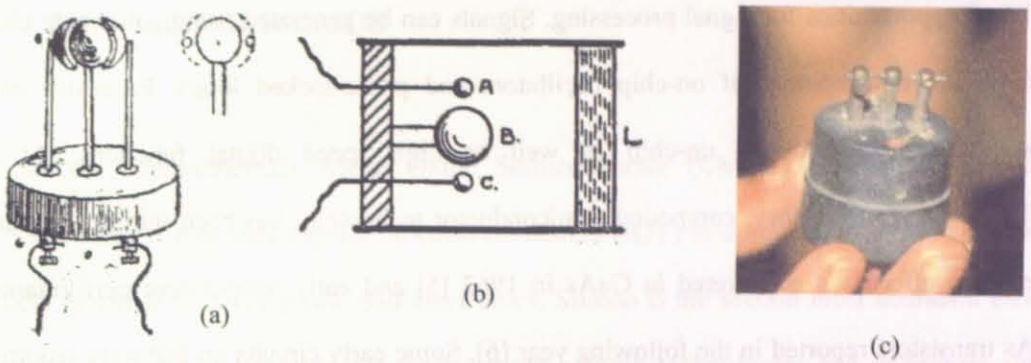


Fig. 1.1 An early spark gap generator for producing millimeter-waves [2].

The most widely known developments occurred on and around the Second World War when the Massachusetts Institute of Technology (MIT) Radiation Laboratory developed the radar technology. In fact, Bell Telephone Laboratories had developed an interest in millimeter waves even before World War II and there was interest in millimeter waves for conventional radio communication. However, atmospheric attenuation due to oxygen water vapor and rainfall was a serious disadvantage, but was not well understood at first. In 1949, R. Beringer made early measurements on oxygen absorption near 5mm (60GHz) [3] for furthering until what we know today about electromagnetic attenuation in air. Figure 1.2 shows the plot of attenuation at different frequency and their respective origins.

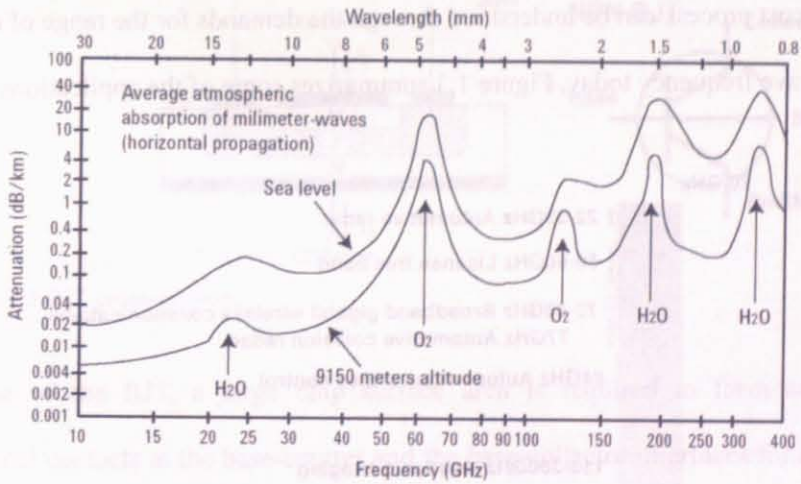


Fig. 1.2 Attenuation of electromagnetic signal in air [4].

The development of the transistor using semiconductor technology in the 1960's opens a new

realm of opportunities for signal processing. Signals can be generated using solid-state circuits through the development of on-chip oscillators and phase-locked loops. Extensive analog functions can be realized on-chip as well as high speed digital functions. At high millimeter-wave frequency, compound semiconductor technology has been initially employed. The Gunn effect was discovered in GaAs in 1962 [5] and early temperature performance of GaAs transistors reported in the following year [6]. Some early circuits on InP were reported in the late 1980's [7]. Applications of the millimeter-wave and sub-millimeter wave frequency with these technologies developed tremendously through the use of vehicular radars and optoelectronics in recent years.

In meantime, silicon technology has been developing since the invention of the silicon transistor in 1954, shortly after the invention of the germanium transistor in 1947 at the Bell Labs. Due to the lower cost of silicon material and properties of its native oxide, silicon CMOS has become popular and dominated the low-frequency consumer applications with large investments on the technology's infrastructure. In recent years, the use of silicon technology at high frequency has been improved with process innovations such as the silicon germanium (SiGe) process. The need for a low cost process can be understood through the demands for the range of applications in millimeter-wave frequency today. Figure 1.3 summarizes some of the applications.

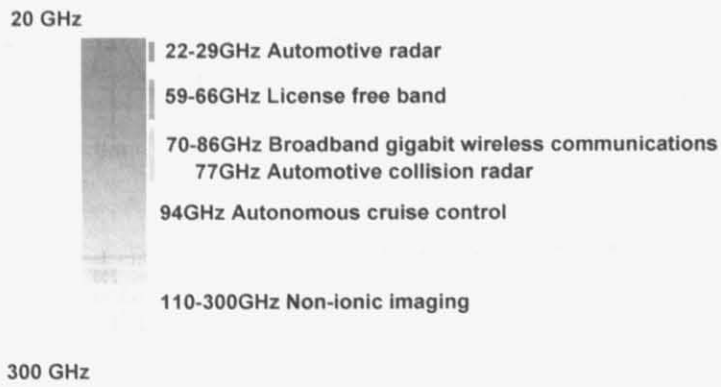


Fig. 1.3 List of frequency allocation in the millimeter and sub-millimeter bands.

1.2 CMOS and SiGe BiCMOS

The silicon Complementary Metal Oxide Semiconductor (CMOS) process and the SiGe BiCMOS process that uses bipolar junction transistors (BJT) in conjunction to CMOS provide the best potential to develop low cost electronics. Silicon is the second most abundant element in the earth's crust and is used for the substrate of both technologies and undergoes similar processing steps. The primary difference is in the use of an additional germanium implantation step to form the heterojunctions to produce BJTs in the SiGe BiCMOS technology. Figures 1.4 and 1.5 illustrate the cross sections of the MOSFET and the SiGe BJT respectively.

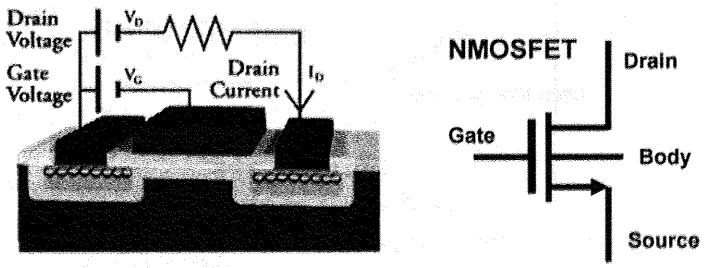


Fig. 1.4 MOSFET cross-section.

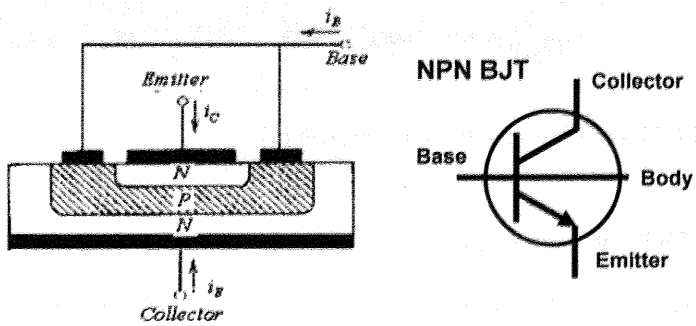


Fig. 1.5 BJT cross-section.

In the case of the BJT, a large chip surface area is required to form sufficiently large 2-dimensional contacts at the base-emitter and the base-collector interfaces for carrier injection. This results in a less compact layout on the chip.

In contrast, the MOSFET occupies an area determined primarily by the width of the gate while keeping the channel length to a minimum. The minimum channel length is determined by the process technology node. In a given SiGe process, the technology node of the MOS transistor is in a less advanced stage than its CMOS counterpart. In 2006, the mainstream SiGe process uses a 0.13μm half-pitch of its MOS transistors, while CMOS is already in the realm of 60nm. Historically, the minimum channel length is limited by the process lithographic capabilities and follows a scaling development according to Moore's law. Moore's law is an observation and a guide to the phenomenon that device integration doubles in every given period due to the reduction in size of the devices. Figure 1.6 shows the scaling developments since 1968.

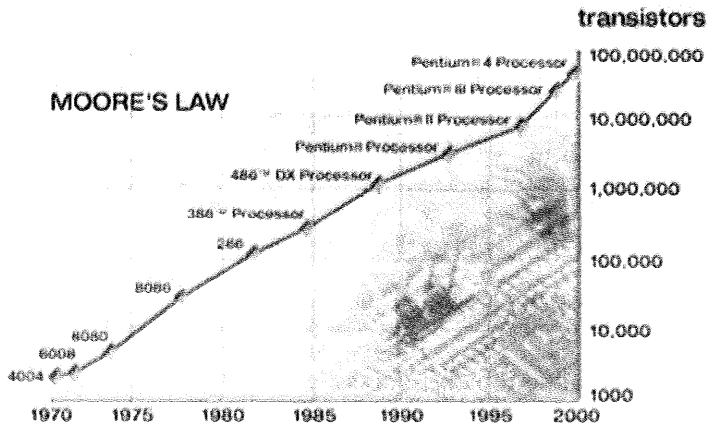


Fig. 1.6 Moore's law and the actual growth [8].

Advanced CMOS process is extremely desirable to highly integrate the MOSFETs for digital functions, since digital functions occupy the large part of a modern device. In 2004, the Intel Montecito dual-core chip contains 1.72 billion transistors using a 90nm CMOS process. It would therefore be desirable if analog circuits for wireless functions can share this same technology and be implemented on-chip.

The challenge in using CMOS is that CMOS technology has not been used for millimeter-wave

process until recently. The first commercial MOS transistors were built with a minimum feature size of approximately 25μm with low current unity-gain transition frequency f_T. To realize amplification with such transistors at gigahertz frequency range was impossible as the operation frequency can only be a fraction of f_T. Recent developments in CMOS technology have improved the technology node to 45nm. Sub-100nm technology allows f_T with a value of 150 GHz and beyond. This makes it possible to design CMOS circuit to operate at millimeter-wave frequencies now. Fig 1.7 shows the increasing CMOS f_T will overtake that of InP and SiGe in the near future. This expectation is derived from the continuing commitment of advancing the CMOS processes.

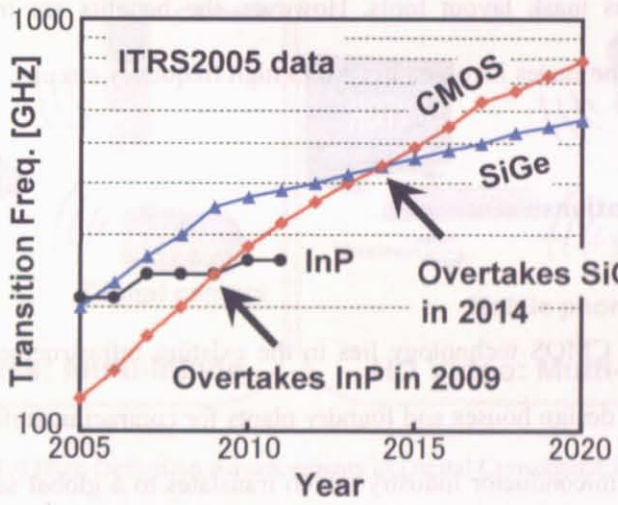


Fig. 1.7 Progress in CMOS RF Characteristics.

1.3 Challenges in Using CMOS

Using advanced CMOS process technology however brings with it some difficulties. The scaling requirements demand a lower supply voltage V_{dd}, which now limits the use of conventional circuit topologies that requires voltage stacking. New circuit techniques to overcome this problem are required [9]. Other important problems include the variations due to

the finer resolution of the devices, which will degrade the matching requirements of conventional differential circuit topologies and the problem of increasing switching speed difference between NMOS and PMOS.

For the circuit designer, using CMOS to design millimeter-wave circuits are extremely challenging. It requires knowledge on traditional separate fields of expertise, including semiconductor physics, radio wave propagations, circuit theory, and layout design. In additional, each of these areas has also reached a level of sophistication that requires the designer to understand software of various 3-D field solvers, transient and frequency-domain circuit simulations as well as mask layout tools. However, the benefits are tremendous once the designer can adapt to the issues involved in CMOS high frequency circuits.

1.4 Market Motivations

The benefits of using CMOS technology lies in the existing infrastructure, including process equipment makers, IC design houses and foundry plants for contract manufacturing has evolved into the core of the semiconductor industry which translates to a global sales of over US$220 billion in 2005 [10] as depicted in Fig. 1.8.

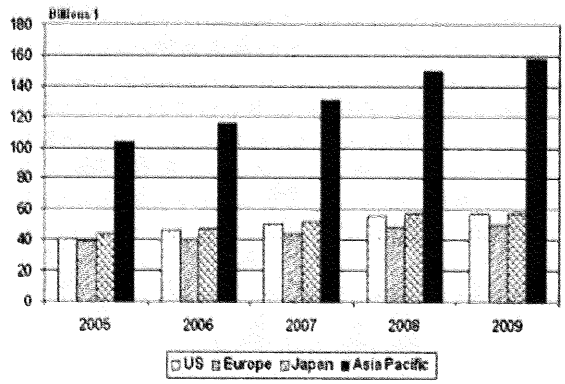


Fig. 1.8 Current and predicted microchip sales growth in the semiconductor industry [10].

These benefits translate to a lower cost for volume manufacturing circuit components. Volume manufacturing is possible with a large demand. It is expected future demand will driven by high frequency communications and its related applications.

At high frequency transmission, a larger bandwidth is available for higher data rates. Fig. 1.9 illustrates high-definition video applications for future home electronic devices that requires high data rates. They can possibly share the existing use of the mobile phone and video recorders.

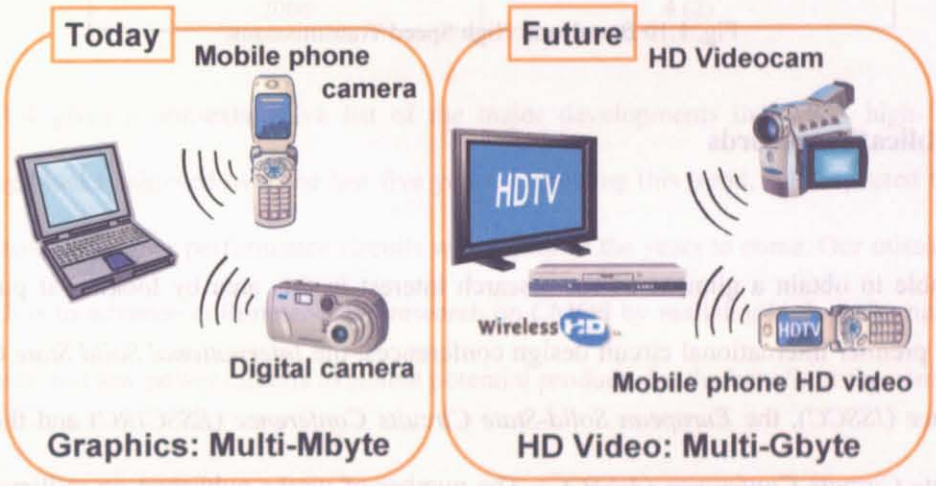


Fig. 1.9 High Definition Advancements in Digital Consumer Electronics.

Applications often drive demands in technological products. Existing data speeds do not exceed 10 Mbps for W-CDMA of the mobile phone and 54 Mbps for the 802.11 wireless LAN standards, as shown in Fig. 1.10. Therefore, applications utilizing these standards cannot deliver high definition videos which require high data rates. However, with the use of the 7 GHz broadband link at 60 GHz, high data rates in excess of 1 Gbps can be achieved. More applications requiring high data rates can be developed. Consequently, with more interesting applications in existing and new products, there will be higher demand.

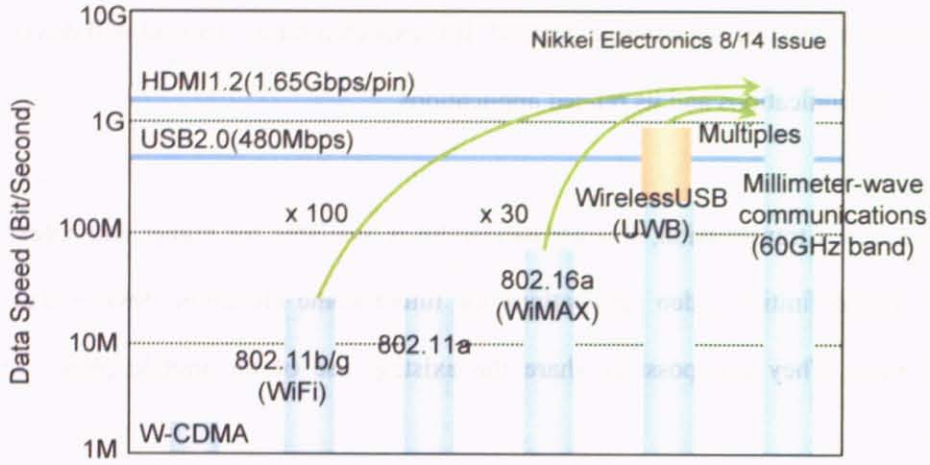


Fig. 1.10 Broadband High Speed Transmissions.

1.5 Publication records

We are able to obtain a glimpse of the research interest in this area by looking at published works to premier international circuit design conferences, the *International Solid State Circuits Conference* (*ISSCC*), the *European Solid-State Circuits Conference* (*ESSCIRC*) and the *Asian Solid-State Circuits Conference (A-SSCC)*. The number of works published on millimeter and sub-millimeter waves (>20 GHz) are given in Table 1.1, 1.2 and 1.3 respectively (works using standard CMOS processes are given in brackets). It can be seen that there is a general trend of increasing numbers over the years in using silicon at high frequency circuit designs.

Table 1.1 Number of Papers reported in ISSCC on millimeter wave circuits.

Year	*Number of Papers*
2002	3 (2)
2003	1 (0)
2004	8 (4)
2005	10 (5)
2006	7 (3)
2007	9 (8)

Table 1.2 Number of Papers reported in ESSCIRC on millimeter wave circuits.

Year	*Number of Papers*
2002	3 (1)
2003	5 (3)
2004	4 (1)
2005	5 (3)
2006	6 (5)

Table 1.3 Number of Papers reported in A-SSCC on millimeter wave circuits.

Year	*Number of Papers*
2005	2 (2)
2006	4 (2)

Table 1.4 gives a non-exhaustive list of the major developments in CMOS high-frequency building blocks achieved over the last five years. Following this trend, it is expected that more innovative and higher performance circuits will appear in the years to come. Our mission in this research is to advance millimeter-wave research on CMOS by realizing high performance, high frequency and low power circuits to enable potential products for the benefit of the consumers.

Table 1.4 Highest operation frequency reported in recent years using CMOS.

Year	*Development at high frequency*
2002	5GHz Transceiver [11]
2003	24GHz LNA [12]
2004	55GHz Frequency divider [13]
2005	60GHz Mixer [14]
2006	70GHz Frequency divider [15]

With an understanding of the motivation behind the exploitation of the millimeter-wave frequency band using CMOS technology, access to the band using a transceiver is needed. This chapter describes the general design of the transceiver for the millimeter-wave project, including the project's specific objectives. Design tools and measurement tools are then introduced. This provides a better description of the circuit realization process.

1.6 Analog IC Design for the RF Transceiver

In order to enable control and the exchange of information, it is necessary to establish communication links between users. The link can be established through transmission in wireless channels of the atmosphere. Wireless communication has the advantage of reduced physical cablings and therefore, improves the ease of connectivity. It is therefore a key requirement in the development of the ubiquitous technology. However, in order for the digital data and information to access the wireless channel for transmission, it is necessary to employ transceivers. A transceiver is a radio front end that performs high frequency analog signal processing to provide a two-way interface between the information source at low base-band frequency and the channel. Figure 1.11 illustrates this basic link for any communication systems. The information at the base-band can perform various control and data functions. The transceiver is designed and implemented on an integrated circuit (IC).

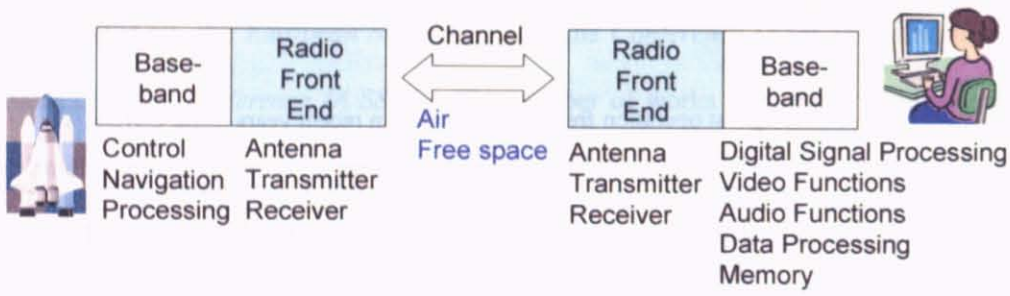


Fig. 1.11 The basic link in the communication system includes the radio front ends and the base-bands at the ends of the channel.

The transceiver comprises the transmitter and the receiver. The transmitter and the receiver further consist of other circuit building blocks, some of which can be shared such as the antenna and the phase-locked loop. However, due to the different power requirements and interference tolerances of the transmitter and receiver circuit, the design of most building blocks are conceptually different from each other.

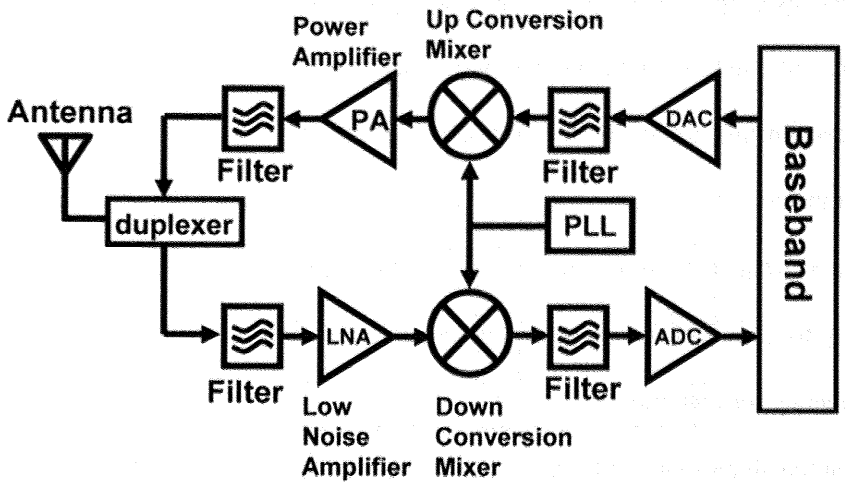


Fig. 1.12 The RF transceiver design for the millimeter-wave band is composed of different circuit building blocks.

Figure 1.12 shows the general block diagram of the transceiver. The transmitter, as shown in the upper path, receives the input modulated signal from the base-band processor through the digital-to-analog converter (DAC) and up-converts the carrier frequency to the desired value through one or more mixing, filtering and amplification operations. A power amplifier boosts the output power to the desired level and passes through a filter to reduce out-of-band power before transmitting through the antenna. The receiver may share the same antenna with the transmitter through a duplexer that minimizes the interaction between the two signals. The received signal is then filtered before amplification by the low-noise amplifier (LNA) to remove the image signal so that the down-conversion mixer can perform the frequency conversion correctly. The filtering requirements of the image signal, however, depend on the receiver architecture. The down-converted signal is converted to its digitalized form by the analog-to-digital converter (ADC) and de-modulated. Recent developments in software defined radio [16] have suggested all-digital solutions to replace the front-end. However, there still exist various difficulties including the digitization of signals at high frequencies.

At millimeter-wave frequencies, the conventional analog architecture is the only applicable solution at present due to the unattainable high clock speeds required for sampling signals of 30 GHz and above. In this architecture, a transceiver front-end has to perform three tasks in both receive and transmit path:

- The center frequency of the modulated wanted signal has to be changed from a low frequency to a very high frequency for transmission or from the very high frequency to a low frequency for reception.
- All unwanted signals situated outside the desired signal channel must be suppressed so that they do not interfere with the correct operation of the wireless communication link and other devices.
- The signal levels have to be adjusted in order to obtain the highest possible performance.

The transceiver front-end does not make any change to the shape or form of the modulated signal. This is done in the base-band at low frequencies by means of the modulation and demodulation process. A receiver or transmitter will therefore almost always be realized as a string of operations where each operation is either one of these three frequency domain operations:

- *a filter*, for the suppression of signals outside the wanted channel;
- *an amplifier*, to adjust the signal level;
- *a mixer*, to change the center frequency.

Filters are required to block signals and spectral components outside the pass band. In mixer circuits, the undesired local oscillator and input signal at the output can be suppressed. Conventional passive filters can be implemented using discrete inductors and capacitors, by exploiting mechanical resonance in quartz crystals or by using acoustic waves in ceramic materials. The passive L-C ladder filter that enjoys widespread use today was invented in 1915

nearly simultaneously by Wagner in Germany Campbell in the U.S. [17], [18]. The basic filter topology invented by Wagner is shown in Fig. 1.13.

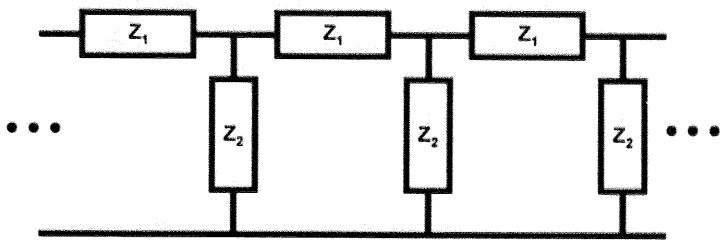


Fig. 1.13 Generic structure of the electric wave-filter or ladder filter by K. W. Wagner in 1919.

In integrated transceivers, one can also employ passive spiral inductors and capacitors, but the low quality factor and small inductance of integrated inductors severely limits their utility. Active filters are viable but consume power, produce distortion and noise. Recently, there have been some developments in micromechanical filters on silicon that deserves further exploration. Currently, to implement filters at millimeter-wave frequency, interconnects operating as transmission lines can be used. The transmission line replaces the discrete inductors and capacitors by the appropriate lengths to produce the required impedances. This implementation is feasible because the short wavelength of the millimeter-wave signal in the dielectric consumes small area. However, transmission lines have high losses on silicon substrate. As a result, transmission lines with high quality factors are needed. Chapter 2 will present details of the work on the on-chip spiral inductor and Chapter 3 introduces new transmission line structures for high quality factor. These transmission line structures also have properties to reduce required lengths for smaller chip area usage.

Amplifiers in a transceiver circuit perform various amplification functions. In the transmitter, there is a power amplifier immediately before the antenna. Similarly, a low noise amplifier is the first active stage in the receiver, immediately after the antenna. There are other

intermediate-stage amplifiers to boost the signal power levels in the transmit- and receive-path as when needed. Therefore, intermediate-stage amplifiers are often implemented as variable gain amplifiers whose gain can be controlled externally. The design of the amplifier requires careful considerations. The specification of the amplifier for gain, linearity, output power and noise figures varies according to the role of the amplifier in the transceiver as well as the application of the transceiver in which the amplifier is used. In addition, there are general design trade-offs between linearity and efficiency, gain and noise figures, gain and bandwidth as well as between power consumption and gain bandwidth product. Another trade-off between operating frequency and gain is a also an important consideration in the design of millimeter-wave amplifiers. Therefore, two approaches are required:

- Select and optimize an amplifier topology to satisfy the minimum requirements and in addition, achieve high performance in important parameters for the required application.
- Develop new circuit topologies to push both sides of the trade-off parameters to a higher performance level.

The need to develop new circuits becomes more critical when advanced CMOS process technology is used. Advanced CMOS process with low supply voltages prevents many conventional circuits with high voltage overheads to be used. These conventional circuits have performed well but become unsuitable for next-generation circuits in the millimeter-wave frequency. Furthermore, designing RF amplifiers using CMOS is challenging because the performance demand on the MOSFET for high gain and high frequency is stretched. For millimeter-wave amplifiers, impedance matching lines as well as routing interconnects all play an important role in success of the design. In chapter 7, the design and implementation of a 50 GHz variable gain amplifier will be described.

The mixer is a device for performing frequency conversion. For the usage of the mixer in the

receiver, there are two inputs, the RF (radio frequency) and the LO (local oscillator). The desired output is the IF (intermediate frequency). For use in the transmitter, the two inputs are the IF and the LO instead, and the output is the RF. The LO is generated by a phase-locked loop (PLL) that includes a voltage-controlled oscillator (VCO). In the design of the mixer, the number of required stages depends on the topology. In the heterodyne transceiver, more than one level of frequency conversion is required. Therefore, mixers will be cascaded with filters in between. Additional amplifiers may be needed too if the mixers and filters result in too much losses. The specific mixer implementation also depends on the design specifications according to the transceiver's application, as in the case of the amplifier. Finally, the mixer design for high millimeter-wave frequency requires an effective layout that is complemented by useful circuit techniques:

- When high LO rejection is required, as in most cases with transmitters, Gilbert cell mixer topology can be deployed. In addition to optimizing the performance of the Gilbert topology, non-conventional designs should be explored. New circuit designs should take into consideration of new filtering technology such as MEMS that may relax this requirement in the future.
- Low power demands on the transceiver will persist and designs minimizing power dissipation at the expense of other excessive performance parameters will be needed.
- In the zero-IF or low-IF architecture of a receiver, the image problem is resolved through complex operations of the signal with quadrature devices. Otherwise, filters will be required. In implementing these passive devices, the geometry of the layout should be efficient to reduce chip area consumption.
- Chip area consumption can be reduced with proper design of the transmission line, which is the fundamental building block of all passive devices used by the mixer.

The fundamental purpose of the mixer is to reduce the carrier frequency so that signal

processing can be performed. Gain is also easier to obtain using IF amplifiers at lower frequencies than at high frequencies with reduced risk of instability and oscillations. Chapters 6 and 7 will discuss the detailed implementation of the up-conversion mixer and the down-conversion mixer respectively. Chapter 8 will present the details of a gain-boosting amplifier.

The amplifier, mixer and other active circuits depends on the MOSFETs for operations. Therefore, it is useful to briefly describe the MOSFET modeling at high gigahertz frequencies. Modeling the MOSFET requires consideration of the parasitic associated with the external layout of the MOS transistor in addition to the characteristics of the transistor per se. These parasitic causes the characteristics of the MOSFET to deviate significantly from those predicted using the low frequency models. Low frequency MOS model [19] includes the popular BSIM models. They may be suitable for use up to low gigahertz frequencies. Figure 1.14 shows a high frequency RF model of the MOSFET that has been augmented with parasitic lumped elements on the standard BSIM3 model for use at higher gigahertz frequencies.

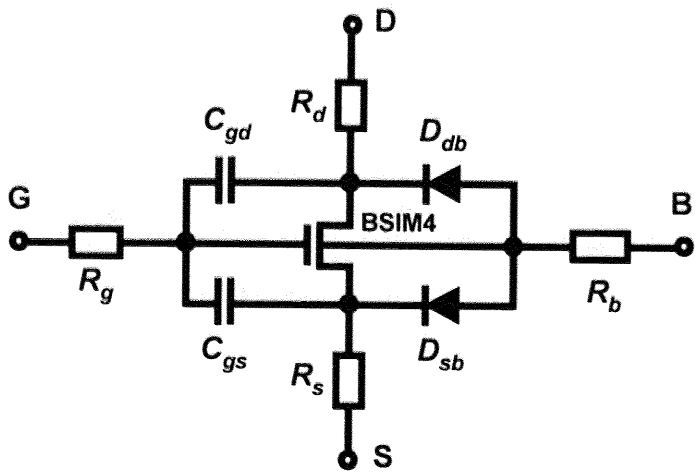
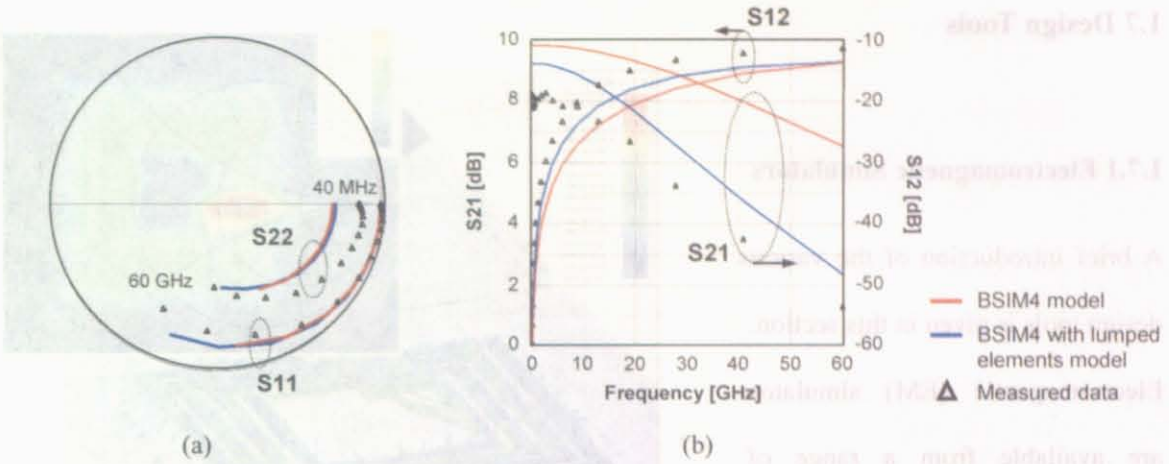


Fig. 1.14 RF small-signal model of NMOSFET.



(a) (b)

Fig. 1.15 Comparison of the MOSFET fast model, slow model and the measurement data (a) S11 and S22 (b) S21 and S12.

The core BSIM4 model parameters can be extracted from its D.C. characteristics. The lumped components of the RF model contain numerical parameters that can be determined by optimal fitting of the measured scattering parameter data from fabricated MOSFET test structures. Figure 1.15 shows the comparison of the model correspondence to the fabricated MOSFET test structures.

After presenting the history, motivations, application of the transceiver and its building blocks as well as the specific transistor modeling, a brief introduction of the design and measurement tools will be made to better understand what the development work involves.

1.7 Design Tools

1.7.1 Electromagnetic Simulators

A brief introduction of the various design tools is given in this section. Electromagnetic (EM) simulators are available from a range of vendors to perform evaluations on devices. The basic trade-off of the simulators is the required simulation time and the accuracy of the obtained results.

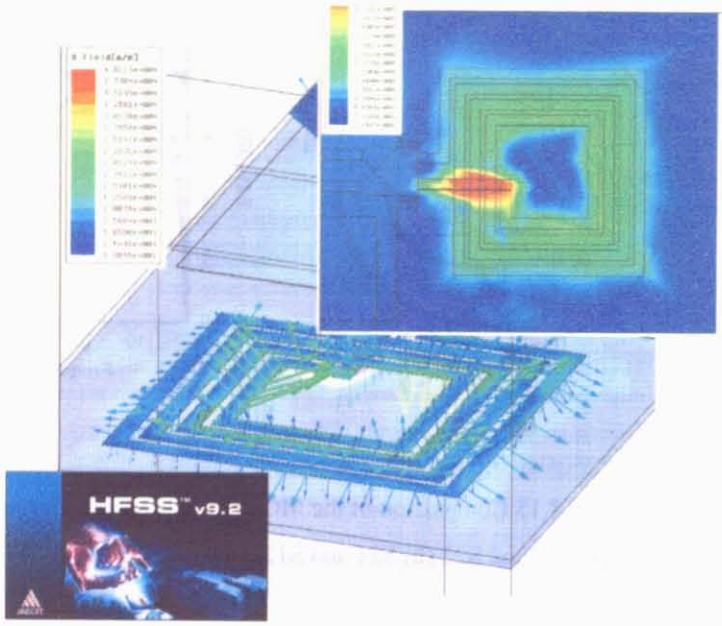


Fig. 1.16 Ansoft HFSS 3-D EM simulation software for designing passive structures.

It is therefore important that the designer can make a reasonable judgment of which simulator to use; by understanding what the minimum level of accuracy that will be significant to the circuit's need. Figure 1.16 illustrates the inductor simulations performed on Ansoft HFSS. Ansoft's 2-D Extract is also frequently employed for the evaluation of transmission lines. Figure 1.17 introduces Agilent's Momentum that is a part of the company's circuit simulation software Advanced Design System.

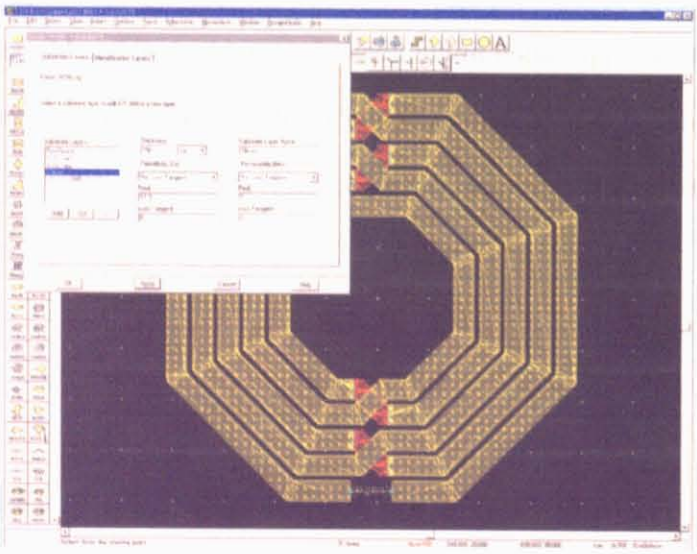


Fig. 1.17 Agilent Momentum 2.5-D simulation software for evaluating layouts.

1.7.2 Circuit Simulators

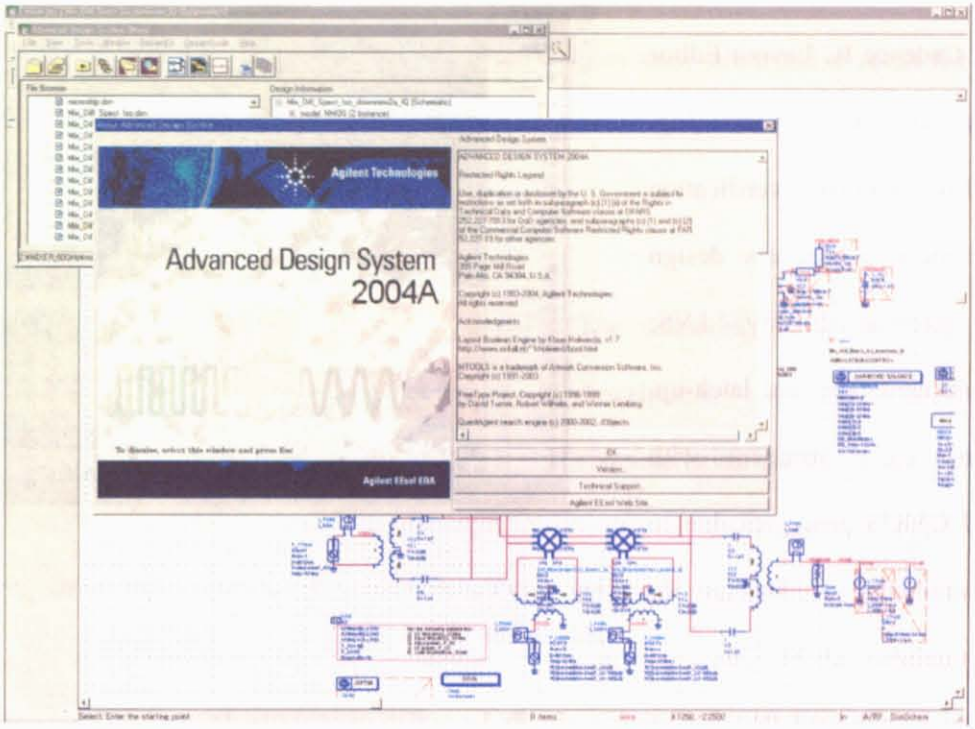


Fig. 1.18 Agilent's Advanced Design System (ADS) uses the harmonic balance simulator.

Today, numerous EDA tools and flows for accurate and efficient RFIC design are commercially available. However, only three algorithms for circuit simulation dominate the industry: transient, PSS (periodic steady state), and harmonic balance. The PSS algorithm is effectively an RF-simulation extension to a transient-simulation engine, assuming that a periodic signal exists in the system. Cadence Design System's SpectreRF simulation implements the PSS algorithm. The harmonic-balance engine is a pure frequency-domain approach. If the input signal is small enough that nonlinear elements in the circuit do not significantly distort the signal output, then the small-signal simulation gives valid results. However, as the input signal becomes increasingly large, new frequencies appear at the output. Harmonic balance solves for each of these new frequencies. This work uses Agilent's Advanced Design System (ADS) that employs the harmonic-balance engine.

1.7.3 Layout Editor

The industry's de-facto layout software Cadence IC Layout Editor has been used for the works (Fig. 1.19). The required verification tools include rule checkers: design (DRC); antenna; density; LVS; option; electrostatics; and latch-up. Rules are more stringent with advanced CMOS processes due to the requirements of Design for Manufacturability (DFM) [20].

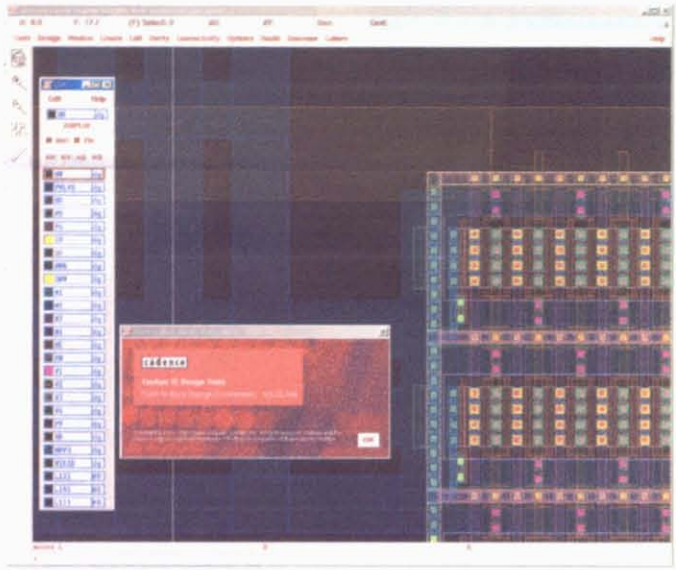


Fig. 1.19 Cadence layout design tool is used for the physical chip layout.

It is to be emphasized that performing circuit layout require understanding of the possible sources of high-frequency parasitic and to take steps in avoiding them. In addition, variations of the layout from the circuit schematics should be carefully evaluated to determine the impact on performance. To effectively understand the possible sources of high-frequency parasitic, the designer may have to take a "3-D" view through a visualization of the physical structures of the devices that is drawn on the layout. Figure 1.20 illustrates the example of the physical structures of the MOSFET and interconnects whose dimensions and positions are determined by the layout designer.

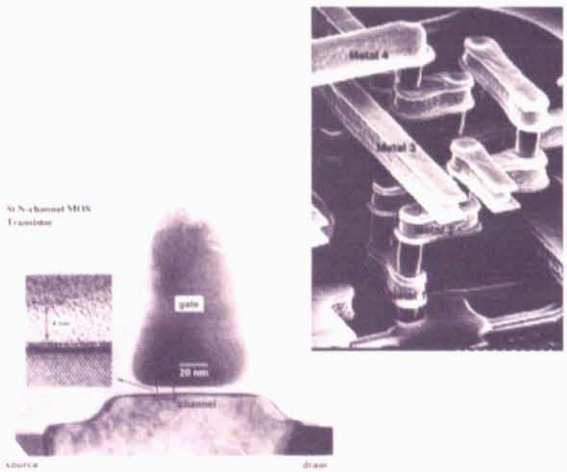


Fig. 1.20 Visualizing the physical structure of the IC is the key to successful analog RF layout design.

1.8 Measurement Equipment

After the design phase, the chip is fabricated and measurements are made to verify the design to obtain the true physical characteristics.

1.8.1 Vector Network Analyzer

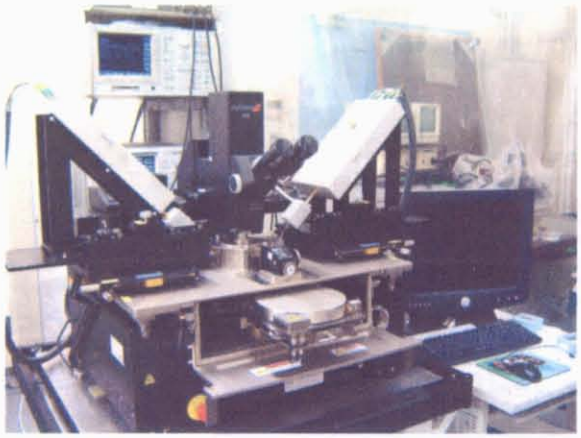


Fig. 1.21 On-wafer probe station for S-parameter measurements with frequency extension up to 110 GHz.

The scattering parameters are powerful descriptions of the circuit's port characteristics. For measurements of the scattering parameters, a vector network analyzer (VNA) has to be employed. This setup makes low-power, linear measurements to characterize the device under test (DUT). It is used in conjunction with the on-wafer probe station shown in Fig. 1.21. This delicate equipment lowers the contact probes onto pads designed on the chip with areas less than 100μm×100μm. A close-up view of the probes is shown in Fig. 1.22. For measurements of multi-port devices such as baluns, a four-port VNA can be used and operates in a similar way. The operation involves a primary calibration step using one of the established standards:

- *Short-Open-Load-Through* (SOLT)
- *Through-Reflection-Load* (TRL)
- *Load-Reflection-Match* (LRM)

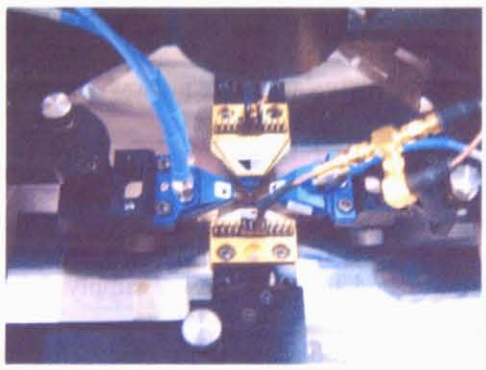


Fig. 1.22 Close-up view of a four-probe setup.

The objective of the calibration step is to define exactly where the measurement system ends and the DUT begins. This location is called "reference plane". All error contributions, inside the VNA and in the cables up to the probe tips have to be calibrated out.

1.8.2 Power Measurements

(a) (b)

Fig. 1.23 (a) signal generators; (b) setup for power measurements with signal generators, spectrum analyzer and source modules connected.

Measurements of power characteristics are performed on high powered devices that cannot be accurately measured by the VNA. Measurements are difficult because any "frequency sweep" in the power measurements must carefully take into account of the corresponding equipment, cable and probe losses at the frequency. Therefore, power measurements can be time-consuming. The setup depends on the type of circuit to be measured, but will primarily consist of signal generators, shown in Fig. 1.23(a), the spectrum analyzer, harmonic mixers, millimeter-source modules and the D.C. power supply. Measurements are conducted using the on-wafer probe station using calibrated cable lengths for connections in the setup, demonstrated in Fig. 1.23(b).

1.8.3 Noise Measurements

Noise measurements are important in the receiver measurements because noise contributed from the circuits affects the quality of the received signals. The most significant noise-contributing devices are found in the first stages of the receiver, the low-noise amplifier and the first-stage down-conversion mixer. When these circuits operate at high-millimeter wave frequencies, the noise figures are generally higher than when operated at low frequencies. Accurate measurements are required to characterize the noise for overall receiver designs.

The noise figure meter, such as Agilent N8975A Noise Figure Analyzer of Fig. 1.24, generates a 28VDC pulse signal to drive a noise source, which generates noise to drive the DUT. The output of the DUT is then measured by the noise figure analyzer. Since the input noise and Signal-to-Noise ratio of the noise source is known to the analyzer, the noise figure of the DUT can be calculated internally and displayed. For high frequency measurements, a harmonic mixer to down-convert the measurement frequency is required.

Fig. 1.24 Front panel of a noise figure analyzer.

1.9 Chapter Summary

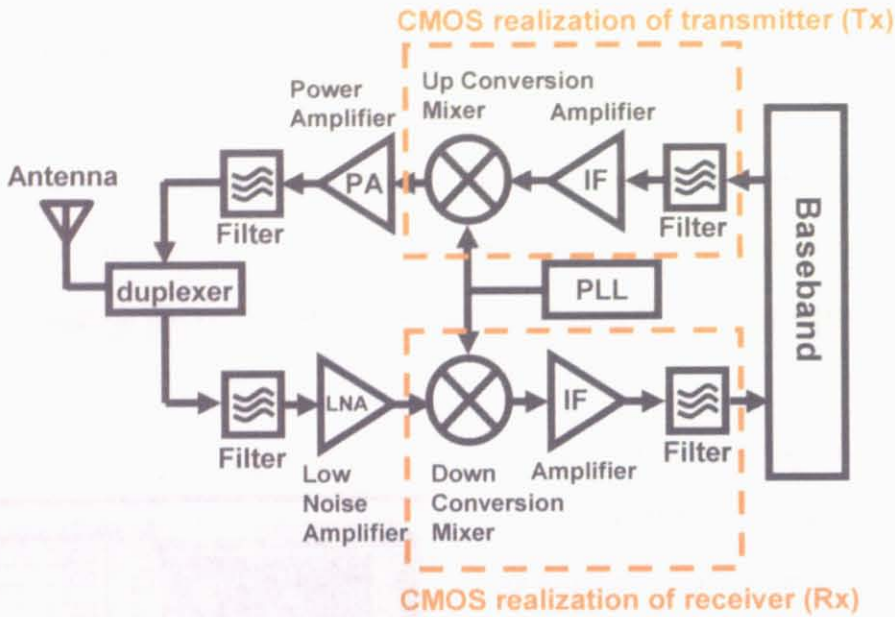


Fig. 1.25 The objectives of this research are to realize the main building blocks in the millimeter-wave RF transceiver design on silicon.

The important building blocks of the transceiver at millimeter-wave frequency are described. The goals of this research is to develop the frequency conversion mixer circuits, amplifier and components for realizing the on-chip filter. The primary component for realizing the on-chip filter at millimeter-wave frequency is the transmission line. Inductors will also be studied. These components will be the silicon realization of the transmitter and receiver, as shown in Fig. 1.25. Specifically, the following challenges will be taken into account when realizing the circuits, which are identified as follows:

- Reliability and efficiency of models for design simulation.
- The on-chip inductor requires accurate modeling.
- Transmission lines with high quality factors are needed.
- Designs should minimize chip area usage to achieve similar functionality.

- Low power consumption in circuits
- Refined layout techniques to achieve design success at high frequency.
- The design, realization and testing of new types of building blocks needed for and newly developed receiver and transmitter topologies
- The design, realization and testing of high performance CMOS circuits for high frequency transceivers

The final discussions in this chapter are the introduction of the design software and measurement equipments. The careful use of these tools on each of the building blocks to obtain design and measurement results will described and discussed in the following chapters. Chapters 3 to 6 presents the on-chip passive devices, including the inductor, transmission lines and the balun. Chapters 7 and 8 presents the frequency conversion mixers. Chapter 9 presents the 50 GHz amplifier using a new resonance techqniue. Chapter 10 concludes with a summary and expected future developments.

Chapter 2

CMOS On-Chip Inductor

The first passive component to be carefully studied in this work is the CMOS on-chip inductor. This component is employed in the low gigahertz parts of the transceiver and is commonly used in analog RFICs. In the design of the transceiver, accurate active and passive models are necessary to predict the real performance of the circuits. The on-chip inductor suffers from substrate losses due to the high conductivity of the silicon. This loss must be accurately modeled through detailed analysis using simulations and qualitative expressions. In particular, it is useful to clarify the factor determining the performance of inductors through an analysis based on the electrical equivalent-circuit model [21]-[23].

2.1 Physical Phenomena In The On-Chip Inductor

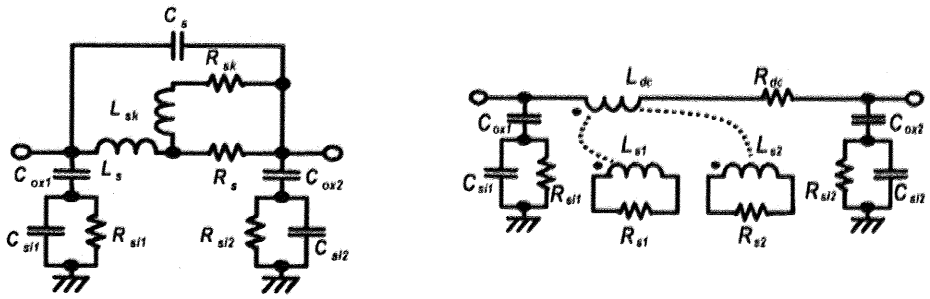
To assess the performance of inductors, simple and accurate modeling of an inductor to account for physical phenomena is imperative. Here, the major physical phenomena to be considered for on-chip inductors are as follows.

1. According to skin and proximity effects, current will not flow uniformly in wiring and resistance increases with increasing frequency [24].
2. When the current flowing in wiring becomes less uniform with increasing frequency, inductance decreases [25].
3. In the case of a low-resistivity substrate, a large current flows in a substrate due to capacitive

coupling between the wirings and the substrate with increasing frequency. Moreover, an eddy current also flows in the substrate by magnetic coupling. In particular, it is known that the influence of the eddy current cannot be disregarded when the resistivity of the substrate is below 1 Ω·cm. [26]

2.2 Existing Inductor Models

A brief review of existing equivalent-circuit inductor models is presented here. Fig. 2.1(a) shows the single-pi model [25], [27] that considers the skin and proximity effects. In this model, the additional inductor L_{sk} and resistor R_{sk} connected in parallel to the resistor R_s model the skin and proximity effects. Fig. 2.1(b) considers the eddy currents [28]. Here, the substrate network separated from the wiring network models the eddy current.

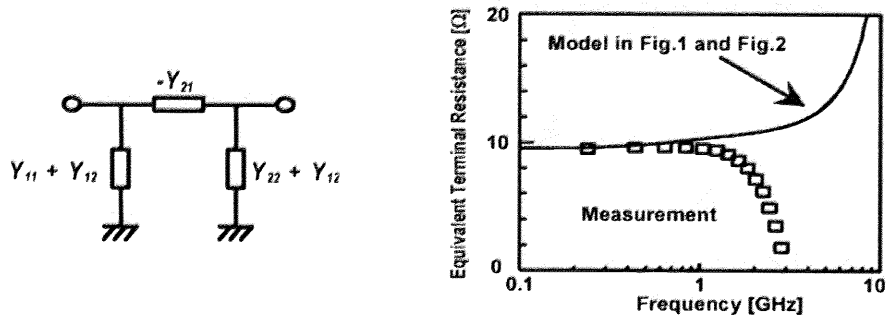


(a) (b)

Fig. 2.1 General types of existing models to represent the on-chip inductor; (a) pi-model for skin and proximity effects (b) pi-model for the eddy currents with separate networks.

Both equivalent circuits are based on pi-type models as shown in Fig. 2.2(a), where $-Y_{21}$ between terminals is determined by parameters such as L_s, R_s, R_{sk}, L_{sk}, and C_s for the case in Fig. 2.1(a) [29]. In the pi-type model, wiring resistance, increasing with frequency according to the skin and proximity effects, is considered as $\mathrm{Re}(-1/Y_{21})$, which is named equivalent terminal resistance (ETR), hereafter. However, as shown in Fig. 2.2(b), the ETR, calculated from the

measurement of an inductor, begins to decrease with increasing frequency.



(a) (b)

Fig. 2.2 Single pi-model characteristics; (a) schematic block diagram of the pi-type models; (b) Comparison of Re(1/Y21) obtained by measurement and simulation of pi-model.

One attempt to explain the phenomenon of the ETR decreasing with increasing frequency is a two-pi model of Fig. 2.3. It assumes distributed characteristics [26]. However, the two-pi model has a singular point above the resonance frequency. This is a point where the prediction of the impedance is too low and its effect is explained through a circuit example in Section 2.6. Hence, it cannot fully explain the physical phenomenon, particularly in the case of a low-resistivity substrate.

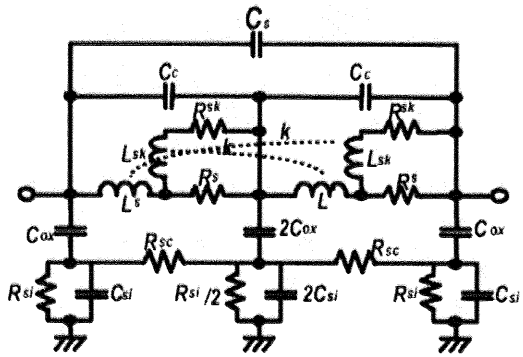
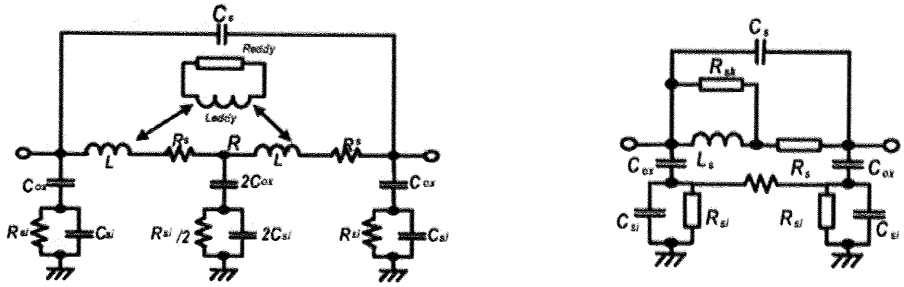


Fig. 2.3 An extended two pi inductor model.

Similar variations of the above models such as those in Fig. 2.4(a) and (b) have been reported in [30], [31] respectively.



(a) (b)

Fig. 2.4 Alternative on-chip inductor models.

The model of Fig. 2.4(a) uses a R_{eddy} and L_{eddy} loop to estimate the current crowding effects of the metal coil. This model is based on the two-pi topology. The model of Fig. 2.4(b) models the substrate resistance but it does not consider the reduction of the inductance due to the coupling of the eddy current. Effectively, it is based on the single-pi model.

We have proposed the substrate-coupled model [32] that includes a substrate network to model the eddy current as shown in Fig. 2.5. This model can account for losses generated in both the vertical and horizontal directions as the current flows through the low-resistivity substrate. This is an improved model over single-pi model because of the accurate ETR prediction at high frequency and over the more advanced two-pi model because of its simplicity in parameter extraction and the absence of the singular point. Figure 2.6 illustrates how the substrate-coupled model compares with the others.

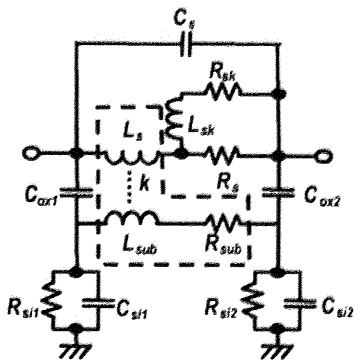


Fig. 2.5 Equivalent circuit model of an inductor based on substrate phenomena reported in [32].

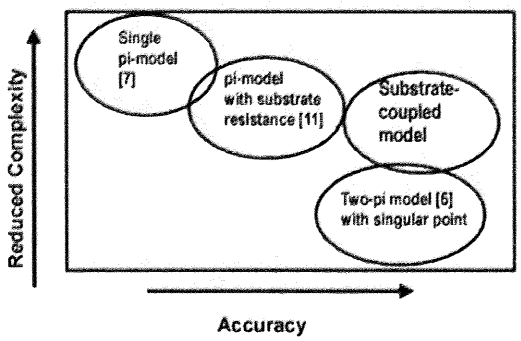


Fig. 2.6 The substrate-coupled inductor model with a substrate network has distinct advantages over the other existing models.

In the following sections, the substrate-coupled model will be described in more detail by explaining the physical phenomenon of the on-chip inductor. Simulation and measurement results are then compared to verify this model. The effects of the substrate eddy current under an on-chip inductor coil have often been studied and numerically modeled. However, no closed-form expressions for a precise model are available for the resistance and inductance of this eddy current because it is a complex function of both the process parameter and geometry. Subsequent sections will describe the method to implement the model with data-fitted equations that are scalable with geometry. Finally, the impact of the model accuracy upon performance evaluation will be studied through examples of the VCO and LNA.

2.3 Substrate-Coupled Inductor Model

In the substrate-coupled model shown in Fig. 2.5, the circuit elements enclosed with the dotted line have improved the conventional pi-model. In this circuit, C_{ox1} and C_{ox2} are the capacitances between the wiring and the substrate, and C_{si1} and C_{si2} are the substrate capacitances. R_{si1} and R_{si2} are the substrate resistances in the z-axis direction; L_s and L_{sk} are the wiring inductances; R_s and R_{sk} are the wiring resistances describing the skin and proximity effects. However, R_{sk} and L_{sk} can be absorbed into R_s and L_s for practical implementation reasons; and C_s is the capacitance

between terminals. Here, R_{sub} and L_{sub} denote the substrate resistance and inductance in the θ-axis direction, and k is the coupling coefficient of L_s and L_{sub}. Since the eddy current and the current in the z-axis direction flow in the same substrate, their networks merge differently. The current that flows in the substrate network composing of R_{sub} and L_{sub} is in the opposite direction to the current that flows in the wiring network composing of R_s, R_{sk}, L_s and L_{sk} as a result of mutual inductance. Consequently, this current decreases the ETR of the inductor. Hence, this additional substrate network is required as previous single-pi models show a discrepancy of exceedingly high values for ETR at high frequency. At low frequency, however, since the substrate network has little linkage with the wiring network through C_{ox1} and C_{ox2}, the eddy current has no discernible impact on the ETR. At high frequency, on the other hand, the linkage through C_{ox1} and C_{ox2} is strong and the reduction in ETR appears notably in spite of the skin and proximity effects.

The cross-section of an on-chip inductor is shown in Fig. 2.7. In the following discussions, cylindrical coordinates are used, where the r- and θ-axes correspond to the radial and angular directions of the inductor, respectively, and the z-axis corresponds to the vertical direction of the substrate.

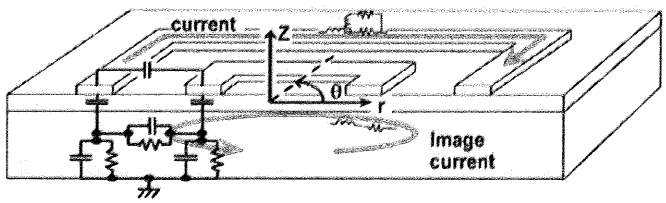


Fig. 2.7 Cross-section of an on-chip inductor.

The substrate network between each turn exists in the r-axis direction, and that between substrate surface and ground exists in the z-axis direction. Moreover, the substrate network of the eddy current flowing in the substrate exists in the θ-axis direction. When substrate resistivity is low, a large eddy current flows. Since the electric field of the negative direction of the θ-axis

is larger than that of the r-axis direction, the current flow in the r-axis direction is neglected and only that in the θ-axis direction is considered for simplicity. This new inductor model of Fig. 2.5 considers the eddy current by mutual coupling between the inductances of the wiring and the substrate.

2.4 Equations for Scalable Models

For simplified implementation of the substrate-coupled model, the following model is used:

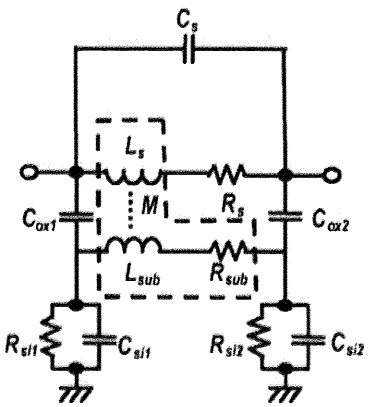


Fig. 2.8 Simplified substrate-coupled inductor model suitable for use in circuit simulations.

R_{sk} and L_{sk}, partially representing the skin and proximity effects are absorbed into R_s and L_s without any loss in accuracy. This can be seen from the results of the fitting in the following discussion. The series inductance L_s, using monomial expression is given by [33]

$$L_s = \beta_1 d_{out}{}^{a_1} w^{b_1} s^{c_1} n^{d_1} d_{avg}{}^{e_1} . \tag{2.1}$$

where d_{out} is the outer diameter of the coil, w is the width of the conductor, s is the space between the conductors, n is the number of turns and β_1, a_1, b_1, c_1, d_1 and e_1 are the constants depending on a fabrication process. For the 0.35μm process used in this work, the coefficients are obtained as in Table 2.2(a). For the 0.15μm SOI process, the coefficients are obtained as in Table 2.3(a) These coefficients are extracted using a least square fit technique of Eq. (2.2) for

the logarithm of Eq. (2.1) from simulated results.

$$\sum_{k=1}^{N}\left[\begin{array}{l}\log\left(L_{measured,k}\right)-\log\beta_1-a_1\log\left(d_{out,k}\right)\\-b_1\log\left(w_k\right)-c_1\log\left(s_k\right)-d_1\log\left(n_k\right)-e_1\log\left(d_{avg,k}\right)\end{array}\right]\rightarrow 0 \tag{2.2}$$

where N represents the number of data sets over the design range.

L_{sub} represents the eddy current flowing in the substrate. It is noted that the induced eddy current in the substrate is effectively circulating as a coil with a certain dimension. This effective coil, however, appears as a single coil consisting of indistinguishable number of turns. Fig. 2.9 shows the finite element simulations of an inductor using Ansoft HFSS showing the eddy current in the substrate.

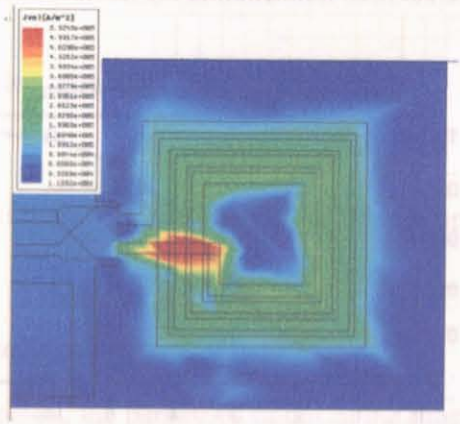


Fig. 2.9 Eddy current induced by the metal coil of inductance L_s, circulating in the low-resistivity substrate. This current loop can conceptually be viewed as an effective coil.

Generally, we have to consider the effective dimensions of outer diameter, conductor width, conductor space and number of turns of the eddy current coil. Although it is difficult to determine these parameters directly, the variation of the eddy current dimensions is considered to scale with the dimensions of the conductor as shown in Fig. 2.9. Using this assumption, L_{sub} is approximate as

$$L_{sub}=\beta_2 {d_{out}}^{a_2} w^{b_2} s^{c_2} n^{d_2} {L_s}^{e_2}. \tag{2.3}$$

where the extracted coefficients are shown also in Tables 2.2(a) and 2.3(a).

An expression for the substrate resistance was reported in [26] that describes R_{sc}, the resistance of the electric coupling of the lines in the substrate in Fig. 2.3:

$$R_{sc} = \frac{1.5 \times \rho \cdot n \cdot (w+s)}{l \cdot t} \tag{2.4}$$

In the equation, ρ is the substrate resistivity, l is the conductor length and t is the substrate thickness. In general, a monomial form of the equation,

$$R_{sub} = \beta_3 n^{a_3} (w+s)^{b_3} l^{c_3} \tag{2.5}$$

provides a good approximation where the coefficients are shown in Tables 3.2 and 3.3. The coupling coefficient, k, is also difficult to be extracted directly in a closed-form function. Figure 2.10 shows the values of the k curve as a function of the number of turns.

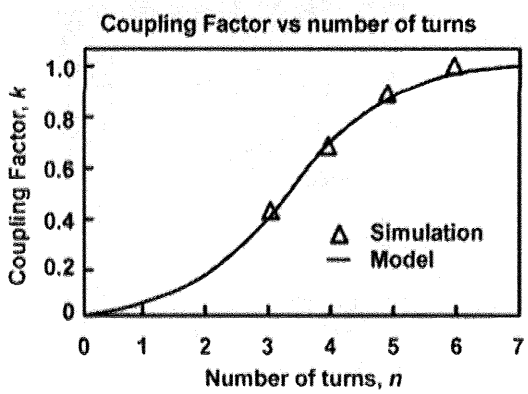


Fig. 2.10 Sample variation of k with the number of turns for d_{out}=250μm, w=15μm and s=1μm.

Here, k is approaching to 0 when the various dimensions fall to zero; and approaching to 1 when n increases to infinity. For practical purposes, the range of validity is limited to the span of the inductor dimensions tested. The equation approximating this relationship is thus given by:

$$k = 1 - e^{\beta_4 n^{a_4} d_{out}{}^{b_4} w^{c_4} s^{d_4}} \tag{2.6}$$

The other circuit elements are given by equations provided by [34]. A summary of the required equations for the model is shown in Table 2.1, where K_a, K_b, K_c, K_d and K_e represent the process

and material constants. These values can be determined by curve fitting when no material parameters of a process are known.

Table 2.1 Summary Model Parameters.

C_s	$K_a n \cdot w^2$
R_s	$K_b l / w$
C_{ox1}, C_{ox2}	$K_c l \cdot w$
R_{si1}, R_{si2}	$K_d /(lw)$
C_{si1}, C_{si2}	$K_e l \cdot w$
L_s	$\beta_1 {d_{out}}^{a_1} w^{b_1} s^{c_1} n^{d_1} {d_{avg}}^{e_1}$
L_{sub}	$\beta_2 {d_{out}}^{a_2} w^{b_2} s^{c_2} n^{d_2} {L_s}^{e_2}$
R_{sub}	$\beta_3 n^{a_3} (w+s)^{b_3} l^{c_3}$
k	$1 - e^{\beta_4 n^{a_4} {d_{out}}^{b_4} w^{c_4} s^{d_4}}$

The sequence of the coefficient extraction steps are as follows:

1. Simulation programs such as ASITIC [22] is first set up with the correct technology parameters and verified.
2. Simulations are made over a range of inductors.
3. Using the S-parameters, the parameter values of the substrate-coupled model are each numerically extracted. This includes the values of L_s, L_{sub}, R_{sub} and k.
4. Using the values of L_s, L_{sub}, R_{sub} and k, together with their geometry, the coefficients of the expressions are extracted using linear optimizations on the least-square fitting method. Other parameters are initially pre-determined by existing equations for the single-pi model. They can then subsequently be more accurately characterized by expressions involving the geometry parameters.

In order to obtain the coefficients of the above expressions, a range of 72 inductors with various geometries have been simulated using ASITIC that evaluates the Green's function [35]. The

model parameters are then optimally extracted from the generated S-parameters. This array of geometry and the model parameters, L_s, L_{sub}, R_{sub} and k, is applied to the above equations to obtain the coefficients by numerical fitting. For example, to evaluate the expression for L_s, we first extract the circuit parameters from the S-parameters. The circuit parameters are extracted according to the following procedures. The equivalent circuit shown in Fig. 2.5 is divided into six groups as shown in Fig. 2.11.

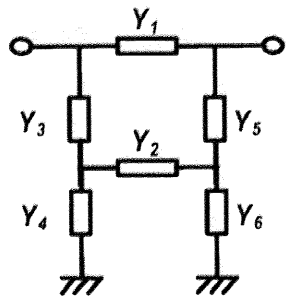


Fig. 2.11 Schematic block diagram of the substrate-coupled model.

Assume that $Y_4 \cong Y_6$ and $Y_3 \cong Y_5$ in Fig. 2.11, we obtain

$$Y_{11} + Y_{21} = (Y_3^{-1} + Y_4^{-1}) \tag{2.7}$$

Equation (2.7) shows that $Y_{11} + Y_{21}$ correspond to a series combination of Y_3 and Y_4 comprising C_{ox1}, C_{si1}, and R_{si1}, as in the case of the pi-type models in Fig. 2.1(a) and Fig. 2.1(b). Similarly, $Y_{22} + Y_{12}$ is equal to the series combination of Y_5 and Y_6 comprising C_{ox2}, C_{si2}, and R_{si2}. Using parameters from Y_3 to Y_6, C_{ox1}, C_{ox2}, C_{si1}, C_{si2}, R_{si1} and R_{si2} are extracted. After these parameters are extracted and the constraint on L_s, R_s, L_{sk} and R_{sk} is derived from the lowest-frequency data, the remaining parameters are extracted using a circuit optimizer. Then, consider the expression of L_s:

$$\begin{gathered} L_s = \beta_1 d_{out}^{\,a_1} w^{b_1} s^{c_1} n^{d_1} d_{avg}^{\,e_1} \\ \log(L_s) = \log(\beta_1) + a_1 \log(d_{out}) + b_1 \log(w) + c_1 \log(s) + d_1 \log(n) + e_1 \log(d_{avg}) \\ \text{Minimize} \Rightarrow \quad \log(L_S) - \log(\beta_1) - \ldots - e_1 \log(d_{avg}) \end{gathered} \tag{2.8}$$

Through linear optimization using solvers such as Microsoft Excel or Matlab, β_1, a_1, b_1, c_1, d_1, e_1 can be obtained using N=72 different values of $\log(L_s)$ and corresponding values of $\log(d_{out})$, $\log(w)$, $\log(s)$, $\log(n)$ and $\log(d_{avg})$. Consider also the simplified case if d_{out}, w, s and d_{avg} are held constant.

$$\begin{aligned} L_s &= \beta_1' n^{d_1} \\ \log(L_s) &= \log(\beta_1') + d_1 \log(n) \end{aligned} \tag{2.9}$$

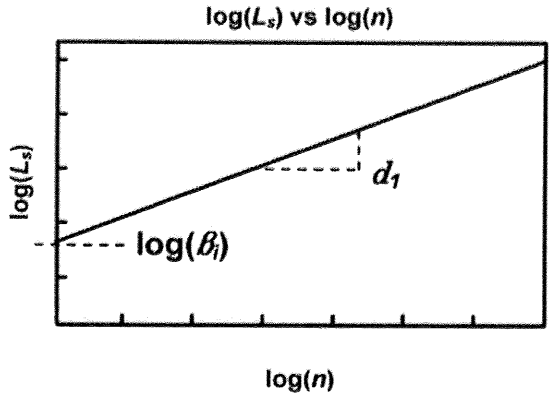


Fig. 2.12 Optimal linear fitting can be used to obtain the coefficients of the multi-variable function.

Thus $\log(\beta_1)$ and d_1 can be obtained through a linear fit through $\log(L_s)$ against $\log(n)$ as in Fig. 2.12. The summary of the coefficients from fitting is given in Table 2.2 for CMOS 0.35μm and Table 2.3 for SOI 0.15μm processes.

Table 2.2(a) Coefficients for Data-Fitted Monomial Expressions for CMOS 0.35μm Process.

Model Parameter	β_i	a_i	b_i	c_i	d_i	e_i
L_s	2.50×10^{-4}	1.84	-0.76	-0.14	1.10	-
L_{sub}	6.18×10^{-7}	0.94	4.13	-1.06	-1.90	1.35
R_{sub}	156	1.36	0.93	-1.40	-	-
k	-4.85×10^{4}	0.91	-1.96	-0.83	0.56	-

Table 2.2 (b) Coefficients for Other Circuit Elements for CMOS 0.35μm Process.

K_a [fF(μm)$^{-2}$]	K_b [Ω]	K_c [fF(μm)$^{-2}$]	K_d [Ω(μm)^2]	K_e [fF(μm)$^{-2}$]
0.0415	0.0302	4.28×10^{3}	8.04×10^{6}	2.10×10^{-4}

Table 2.3 (a) Coefficients for Data-Fitted Monomial Expressions for SOI 0.15μm Process.

Model Parameter	β_i	a_i	b_i	c_i	d_i	e_i
L_s	10^{-4}	2.31	-1.47	-0.08	1.24	-
L_{sub}	10^{-6}	0.98	4.39	-0.99	-1.84	0.68
R_{sub}	39	1.30	0.93	-1.40	-	-
k	-4.90×10^{4}	2.6	-2.12	-0.98	1.60	-

Table 2.3 (b) Coefficients for Other Circuit Elements for SOI 0.15μm Process.

K_a [fF(μm)$^{-2}$]	K_b [Ω]	K_c [fF(μm)$^{-2}$]	K_d [Ω(μm)^2]	K_e [fF(μm)$^{-2}$]
0.0895	0.0466	2.93×10^{-3}	3.03×10^{7}	2.10×10^{-4}

2.5 Experimental Results

For measuring the inductors, the Anritsu 37397 vector network analyzer is used together with the on-wafer probe station. Cascade Microtech ground-signal-ground (GSG) probes are used. Short-Open-Load-Through (SOLT) calibration method is used. To verify the proposed model, several inductors with symmetric octagonal designs have been fabricated on the basis of 0.35μm CMOS process, where the inductors are formed with the top-layer metal. The dimensions of the inductors are summarized in Table 2.4 for the CMOS 0.35μm process.

Table 2.4 Dimensions of Fabricated Inductors on CMOS 0.35μm process.

	d_{out} [μm]	w [μm]	s [μm]	n
#1	200	10	5	4
#2	300	15	5	5
#3	250	10	5	5
#4	200	10	1	4
#5	350	10	3	4

After measuring inductors using a vector network analyzer, the parasitic capacitances and resistances of pads and leads are de-embedded using the open- and short-dummy patterns to extract the S-parameters of the inductor core. The comparison results between the simulation and the measurement on ETR are shown in Fig. 2.13 for diagnosis. Here, the proposed model describes well the reduction in ETR which cannot be explained with the conventional model since the conventional model does not consider the eddy current adequately. The comparison results of S11 and S21 using the measurement and the simulation are shown in Fig. 2.14. The solid line indicates the simulation with the proposed model and the dashed line indicates the simulation with the conventional model. While the proposed model indicates good agreement with the measurement up to 10 GHz, the conventional model shows discrepancy above 3 GHz.

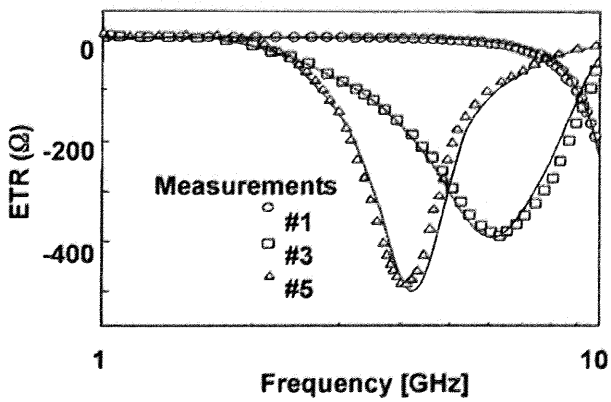


Fig. 2.13 Comparison of the ETRs between the measurements and simulations using samples #1, #3 and #5. Dimensions correspond to Table 3.4 for the CMOS 0.35μm process.

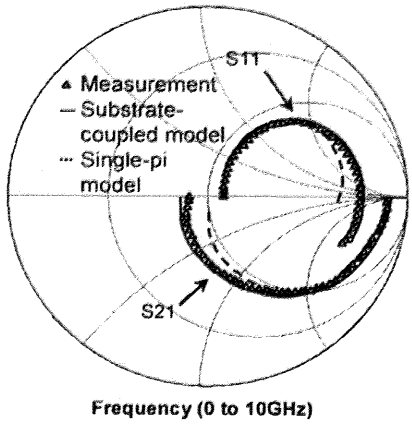


Fig. 2.14 Comparison of S11 and S21 between measurements and simulations of sample inductor #3.

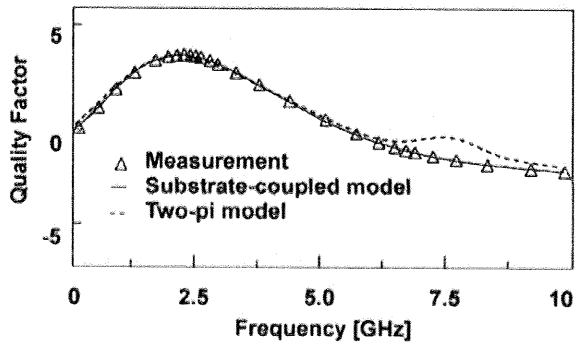


Fig. 2.15 Q-factor predicted by the measured, substrate-coupled model and the two-pi model of sample inductor #3.

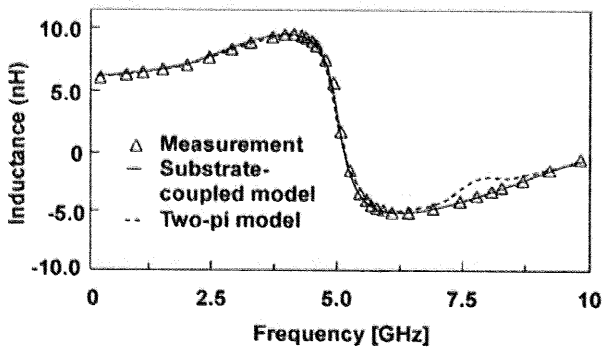


Fig. 2.16 Comparison of inductances predicted by the measured, substrate-coupled model and the two-pi model of sample inductor #3.

Figure 2.15 and 2.16 compare the models with the measured Q-factor and inductance respectively. As shown in Fig. 3.15, the Q-factor of the substrate-coupled model corresponds closely to the measurement results. The sample data shown is taken from the 0.35μm-process inductor #3. The two-pi model, on the other hand, deviates from the measured result at the singular point near 7.2 GHz. In Fig. 2.16, the inductances obtained by the substrate-coupled model and the measurement as well. With the two-pi model, however, the singular point causes a slight overestimate. Figure 2.17 shows the micrograph of the symmetric inductors that are successfully characterized with the substrate-pi model of Fig. 2.8.

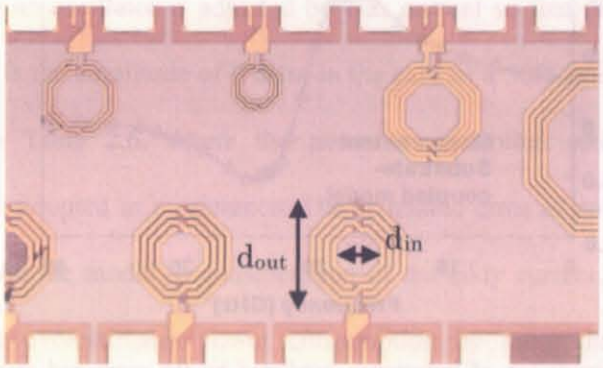


Fig. 2.17 Micrograph of the inductors.

Characterization is also made on inductors fabricated on Silicon-On-Insulator (SOI) 0.15μm process. Table 2.5 shows the dimensions of the inductors.

Table 2.5 Dimensions of Fabricated Inductors on SOI 0.15μm Process.

	d_{out} [μm]	w [μm]	s [μm]	n
#1	96	10	3	2
#2	122	10	3	3
#3	148	10	3	4

Figure 2.18 and Fig. 2.19 shows the results of the SOI 0.15μm process inductors.

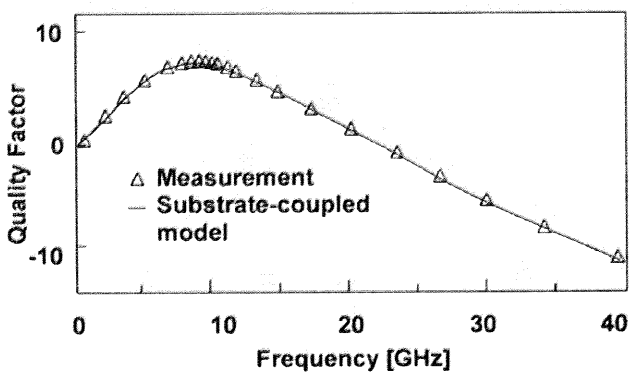


Fig. 2.18 Comparison of Q-factor predicted by the measured results and the substrate-coupled model of sample inductor #3 from the SOI process.

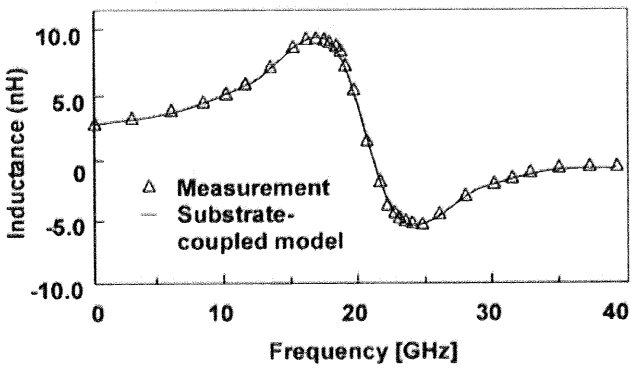


Fig. 2.19 Comparison of inductance predicted by the measured results and the substrate-coupled model of sample inductor #3 from the SOI process.

2.6 Circuit Performance

The substrate-coupled inductor model is analyzed in a LC oscillator circuit. Since the tank impedance can also be accurately predicted by the conventional single-pi model, a measure of the power consumption can demonstrate the advantage of predicting the ETR correctly. The oscillator used for comparison is shown in Fig. 2.20.

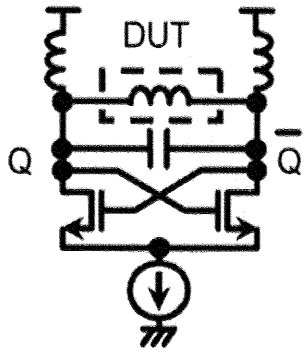


Fig. 2.20 Schematic of an LC oscillator.

Here, oscillation frequency to which the Q-factor serves as the maximum from measurement is used. The output of an oscillator is adjusted by bias current so that the output amplitude may give 0.316V, which is the amplitude of 0 dBm in the case of a 50Ω load. The simulation results are summarized in Table 2.6, where the power consumption estimated from numerical measurement data is adopted as a reference. The estimated error of power consumption is less than 20% when using the model in consideration of the eddy current. On the other hand, the conventional model overestimates power consumption by more than 100% of the result obtained by the measurement.

Table 2.6 Power Consumption as a Measure of Oscillator Performance.

	Oscillation frequency [GHz]	Power consumption [mW] % error		
		reference	Substrate-coupled model	Pi-model
#1	7.6	0.69	0.80/+15.9%	2.03 /+196%
#2	4.4	0.63	0.75/+19%	2.03 /+225%
#3	5.8	0.50	0.55 /+10%	2.05 /+312%
#4	5.9	0.82	0.80 /-2.4%	1.62 /+99%
#5	3.7	0.59	0.69 /+16.9%	1.88 /+221%

In order to further evaluate the performance of the inductor model, the harmonic components generated in the circuit is estimated. An amplifier is designed to operate at 2.4 GHz in the

schematic diagram of Fig. 2.21.

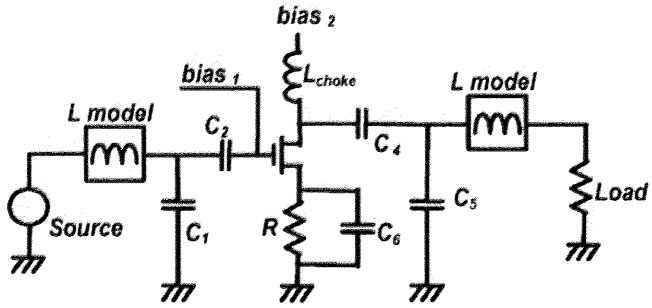


Fig. 2.21 Amplifier schematics employing the use of two 6.3nH inductor models at the input and output matching networks.

The matching inductors are chosen as 6.3nH. The output performance of the circuit is compared by using the different inductor models and the measured inductor.

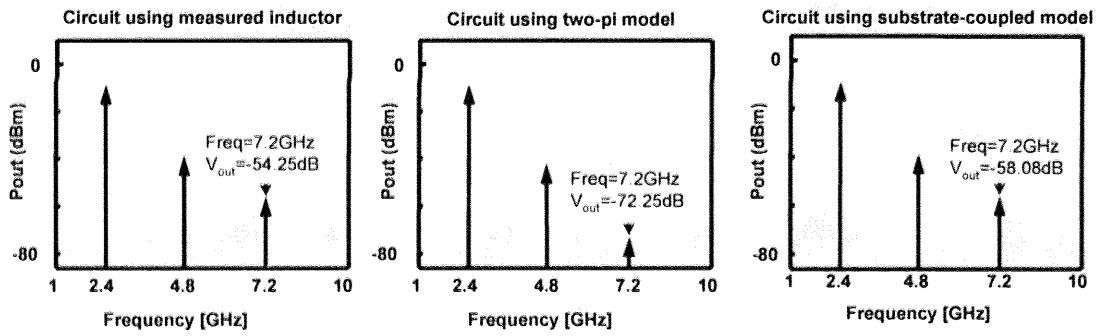


Fig. 2.22 Spectrum outputs of the circuit employing different inductor models in the matching networks; it can be seen that the two-pi model gives significantly lower results for the third harmonics.

Using the proposed extraction method allows us to obtain the equivalent substrate-coupled inductor model used in the circuit. The model parameters of the two-pi model, on the other hand, are first extracted using methods of [26]. The resulting output spectrum of the circuit is shown in Fig. 2.22 for both models, compared with the measured inductor. As shown in Fig. 2.22, the substrate-coupled model does not underestimate the spectral power of the third harmonics as much as the two-pi model does. For nonlinear circuits that utilize the third harmonics, this

particular case demonstrates the advantage of this substrate-coupled model.

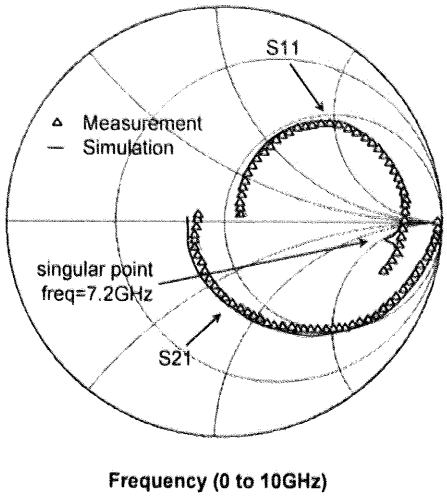


Fig. 2.23 The singular point can be observed at 7.2 GHz with the two-pi model.

This discrepancy of the two-pi model is a result of the singular point that is observed in Fig. 2.23 when S11 is plotted on the smith chart. This singular point falls on f=7.2 GHz in this case as a result of the mid-branch of the two-pi model. Since the substrate-coupled model does not contain this branch, it does not suffer from this problem. As a result, although the fundamental frequency of the amplifier is way below this singular point at 2.4 GHz, the third harmonics is adversely affected. This example shows that the singular point from the two-pi model does affect the prediction of the circuit performance. Specifically, it demonstrates the importance of predicting performance beyond the self-resonant frequency. The proposed model can predict the harmonics of the LNA accurately because the ETR, in addition to the inductance can be accurately predicted.

2.7 Chapter Summary

A substrate-couple inductor model is proposed. The model takes into account the effects of the eddy current flowing in the substrate under the metal coils. This effect is described by the reduction of the ETR with increasing frequency which cannot be explained by the conventional pi-model. The accuracy of the model has been proven with good fitting of the quality factor and inductance over a wide bandwidth. The accuracy of the inductor model affects the prediction of the power consumption of an LC oscillator and the harmonics of the LNA. Measured results show an overestimation of more than 100% in the case of an LC oscillator when the conventional model is used. Simulation results of the LNA show an unrealistic 15dB reduction of the third harmonics when the conventional model is used instead of the substrate-coupled model. To make practical use of this model, scalable expressions in terms of geometric parameters are required. These expressions are derived with least-square fitting methods on the coefficients of monomial expressions. The coefficients of the expressions are verified using field-solver simulations and fabricated inductors. The Q-factor and inductance of the extracted model corresponds well with measured results. Successful characterization of fabricated inductors with the substrate-coupled inductor model has been made on the CMOS 0.35μm and SOI 0.15μm process technology.