博士論文

Highly-Functional Gate-Driver ICs for Advanced Power Devices

(先端パワーデバイス向け 高機能ゲート駆動 IC)

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Abstract

Power devices are key devices of power electronics, which is a major technology in power conversion systems. A power device is a switching device that controls ON / OFF of a large current, and there are types such as a thyristor, a gate turn-off (GTO), a bipolar junction transistor (BJT), a metal-oxide-semiconductor field effect transistor (MOSFET) and an insulated gate bipolar transistor (IGBT). Among them, MOSFET and IGBT are widely used because of ease of handling. The MOSFET and the IGBT control the switching by the voltage of the gate terminal. The electrical control of the gate terminal is performed by a circuit called a gate driver. The gate driver has the function of controlling the switching characteristics by adjusting the gate waveform and quickly turning off when the device is short-circuited.

The performance of power devices such as IGBT and MOSFET used in power electronics has been improving year by year, and current density and operation speed are increasing. As a result, increase in noise during switching of the power device and reduction in short-circuit withstand capability are advanced, so improvement in reliability is required. In order to solve these problems, improvement of the switching characteristics of the power device

by the gate driver and improvement of short-circuit detection speed are required.

In this research, a gate driver and short-circuit detector that can be applied to various power devices are proposed, demonstrating improvement of switching characteristics and improvement of short circuit detection speed.

Chapter 1 introduces the background of this thesis. After describing the switching operation of the IGBT in detail, the adverse effects caused by the performance improvement will also be described. Based on this, the purpose of this research is described.

Chapter 2 proposed clocked gate driver IC design. In order to be compatible with various power devices, the gate driver can adjust the drivability and the timing programmably, and generates a gate driving waveform for improving the switching characteristics for each device. The effectiveness of the gate driver is demonstrated by driving the gates of Si-IGBT and SiC-MOSFET.

Chapter 3 proposes automatic optimization of IGBT gate driving waveform using the gate driver. Automatic optimization using simulated annealing is done because it is difficult to set parameters with great freedom of the gate driver by human hand. The effectiveness of the automatic optimization is demonstrated by experiments on two kinds of IGBTs.

Chapter 4 proposes fast short-circuit detector design with robustness to a change of operating conditions. By using the analog delay multiplier, it corresponds to the change of the operating condition. In addition, the detection speed is improved by implementing the detector circuit on the IC. The effectiveness of the short-circuit detector is demonstrated by experiments.

In Chapter 5, this thesis concludes and gives future prospects.

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Chapter 1

Introduction

1.1. Background

Power electronics is one of core technologies that supports today's society heavily dependent on electricity. A role of power electronics is to convert electronic power to mechanical power such as motor rotation or to convert a type of electric power to different types of electric power found in an AC to DC and a DC to DC conversion. Main applications of power electronics are hybrid cars, air conditioners, welding equipment, photovoltaics, wind electricity, UPS, and so on (Fig. 1.1). Since these applications deal with high power, efficiency and safety are required to reduce power loss and to prevent serious accidents. In order to improve the efficiency and safety, researches and developments of the power electronics have been conducted and contribute to the spread of electric technology which is indispensable to our life today.

Power devices are a core of power electronics that handle high-power electricity safely and efficiently. The power devices are considered as active switches with high-voltage and

large-current capability, and power device types include thyristors, Gate Turn-Off thyristors (GTOs), Insulated-Gate-Bipolar-Transistors (IGBTs), Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) and Bipolar Junction Transistors (BJTs). Materials used for power devices are widely-used inexpensive Si or high-performance yet expensive SiC and GaN. By appropriately selecting a device type and a material, it is possible to cover diverse applications. Because of these application diversity and electrical power demand, a power-electronics market is increasing with the spread of electric technology, and it is expected to grow at the rate of 8% per year (Fig. 1.2).

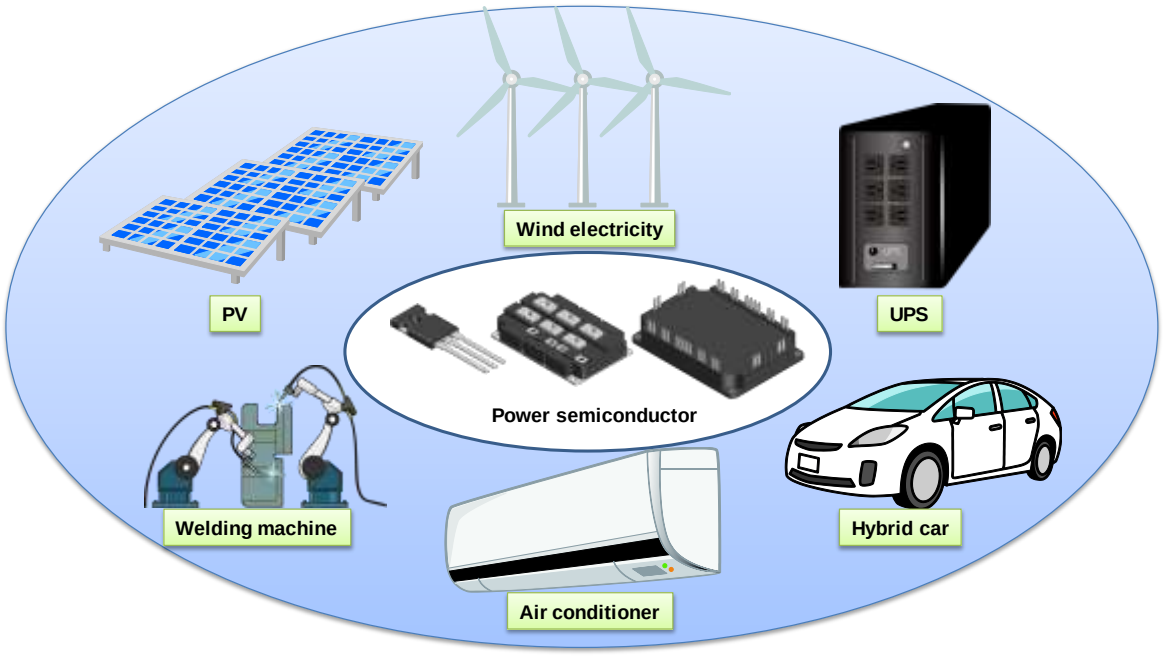


Fig. 1.1 Applications of power electronics.

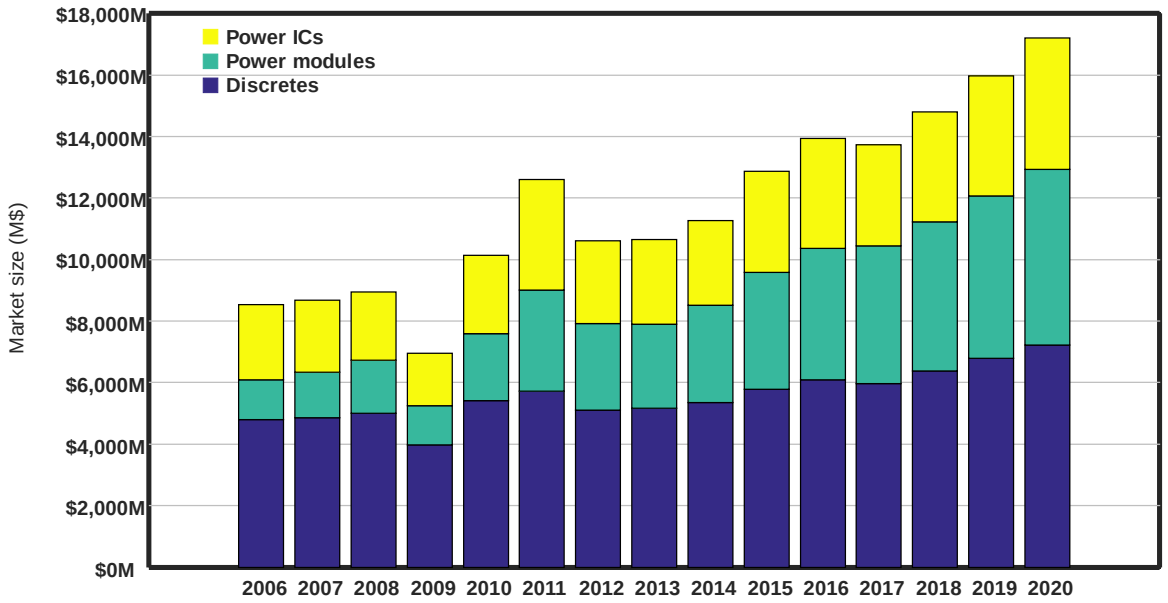


Fig. 1.2 Market growth of power semiconductors [1.1].

Fig. 1.3 shows applications of power devices in terms of an operating frequency and operating power. Although the GTO and the thyristor are slow in switching operation, they have high conductivity and are used in high-power applications such as national grids. The Bipolar, the MOSFET and the IGBT are used for driving motors, power supplies, railways, electric cars, and industrial machineries. A power IC is a power conversion element and is used as a power supply part for a PC or a smartphone. Compound semiconductors such as SiC and GaN boast low-loss and high-speed switching, and researches and developments are actively carried out. Although the devices made by the compound semiconductors have high performance, they are expensive and not so visible in the market, and thus it is indispensable for these devices to lower the cost by a forthcoming research. Among the above-mentioned devices, the IGBT and the MOSFET are easy to use because they control the switching operation through the insulated gate. So, they are attracting attention and widely used as the technology that can be widely applied for an industrial and an in-vehicle use. Since the IGBT has a structure suitable for high-power applications, it is expected to replace the GTO and the thyristor by applying to the higher voltage applications with the

help of further researches and developments.

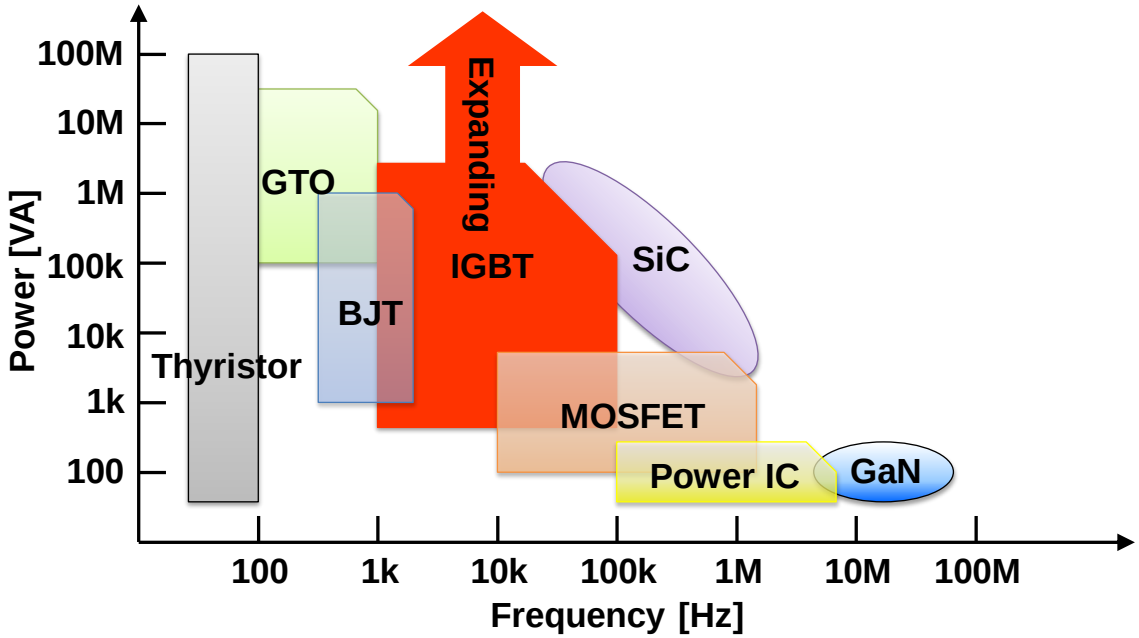


Fig. 1.3 Application ranges of power devices for operating frequency and conversion power rating.

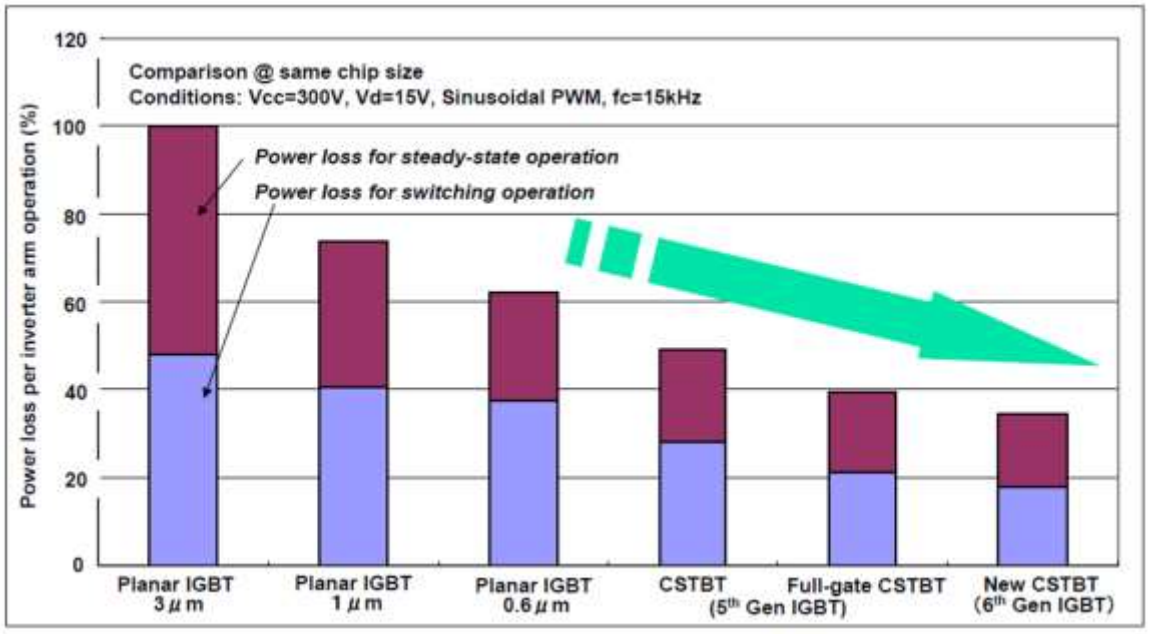


Fig. 1.4 Performance improvement of Mitsubishi IGBT [1.2].

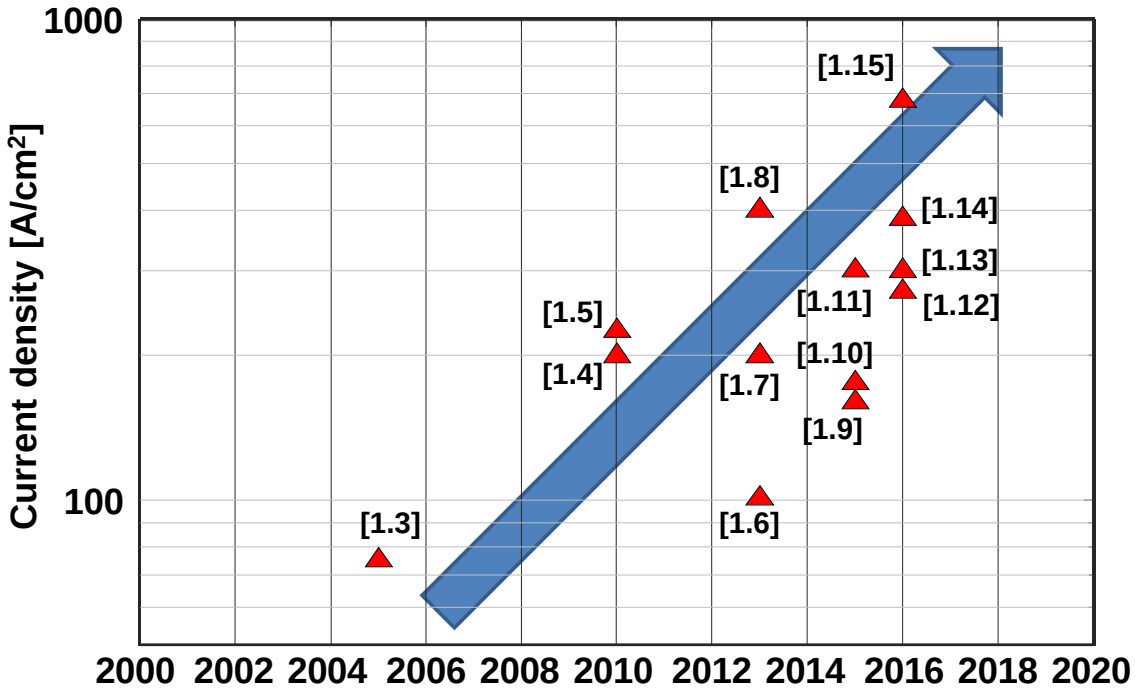


Fig. 1.5 Current density per unit area of 600V-rating IGBTs in recent research.

A performance improvement of the IGBT has been realized in recent years [1.2]. Fig. 1.4 shows, as an example, that the power loss in the same chip area and the same operating condition of Mitsubishi IGBT is decreasing. The power loss is improved compared with the earliest ones. These performance improvements are realized by improving the device structure of the IGBT's. Similarly, Fig. 1.5 shows the improvement in the current density at the same on-voltage of the 600-V IGBT in recent years. The high current-density device will show the lower loss at the same current output because of the lower on-voltage in coming years. In the future, the power loss of the IGBT will be improved by the extensive research and development.

In this chapter, introductions are given on the characteristics and the requirements for IGBT devices for a preferable switching. After that, an overview of this thesis is described as to the improvements of the IGBT performance.

1.2. Power electronics circuits

Fig. 1.6 shows a basic architecture of a power conversion system using power devices. The power conversion circuit is composed of a main circuit, a controller and a gate driver. The main circuit is using power devices as switches. It is called an arm in which a free-wheeling diode is connected in parallel to an IGBT (or MOSFET). Two arms connected in series are called a leg, and a high voltage (from several hundred volts to several thousand volts) is applied between the top and the bottom of the leg. A main circuit is in most cases composed of parallelly-connected legs and an inductive load. The main circuit controls the power output by appropriately switching each arm. The controller which is operated under a low voltage (1V ~ 5V) determines the timing of switching. The switch timing is determined by monitoring the state of the output with sensors. The controller also has a role of stopping the system operation properly when a short circuit of the main circuit is detected and of preventing accidents and failures. The gate driver receives about 1-V switching signal from the controller through an isolator and drives the gates of IGBT's at the higher voltage around 15V. Connecting the low-voltage signal of the controller directly to the high-voltage main circuit results in destruction of the controller due to overvoltage. Therefore, it is necessary to isolate the low-voltage side from the high-voltage side by the isolators. One more characteristics that the gate driver should have is that the gate driver must drive the gate of an IGBT with appropriate drivability. Safety is an important concern because the power conversion circuit deals with high power and if any accident happens the resultant damage is considerable. When the drivability of the gate driver for the gate of the IGBT is too strong, an abrupt voltage and/or current change of the main circuit occurs. This abrupt

change in turn give rise to a large noise, which tends to cause malfunctions of the main circuit. If a malfunction occurs in the main circuit handling high power, it may result in an explosion or a fire. On the other hand, if the drivability is too weak, the switching of the main circuit will be slow and the loss may increase. Thus, drivability of the gate driver is properly controlled for the better performance of the main circuit. Also, a gate driver has a role of protecting the power conversion circuit by detecting a short-circuit condition of an IGBT. In summary, a gate driver has to drive a gate of an IGBT while satisfying the safety condition, providing high efficiency of the main circuit and as well as eliminating short-circuit conditions of the main circuits.

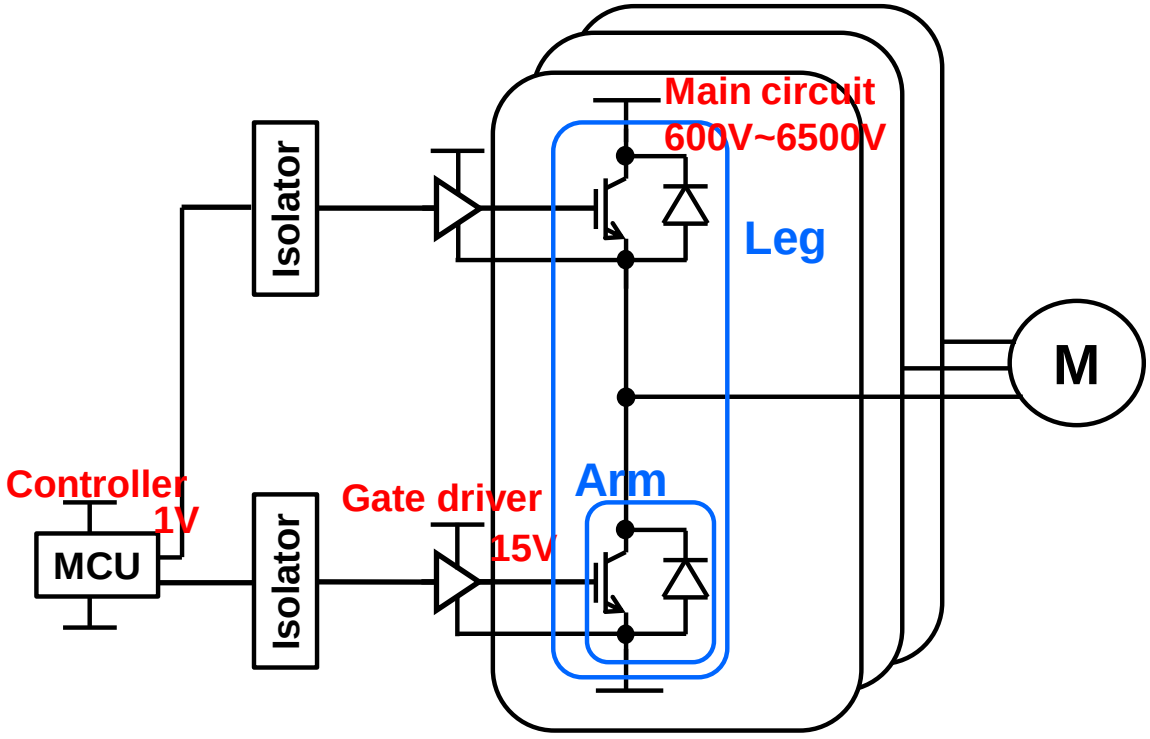


Fig. 1.6 Basic architecture of power conversion circuit.

1.3. Power device structures

The power device has a high breakdown voltage in an off-state, and high conductivity in an on-state. In this section, the device structure of the IGBT which covers a wide application range is described. The special switching characteristics is also described that is resulted from the device structure of an IGBT.

1.3.1. IGBT

An IGBT has a vertical structure in which a MOSFET and a BJT are combined. Fig. 1.7 shows the IGBT device structure and the equivalent circuit and a circuit symbol. The IGBT has three terminals, a collector, an emitter and a gate. The IGBT chip surface has the emitter terminal and the gate terminal, and the collector terminal is on the back side of the chip. A high voltage is applied between the collector terminal and the emitter terminal. In an off-state, the high voltage of several hundred volts to several thousand volts is applied between these terminals to turn off a collector current, and in an on-state, a large current flows with a low on-state voltage between the collector and the emitter. A switching control signal of about 15V is applied between the gate terminal and the emitter terminal. A gate-emitter voltage controls a collector-emitter on / off state. The gate-emitter voltage of 15V turns on the IGBT and that of 0V turns off the device.

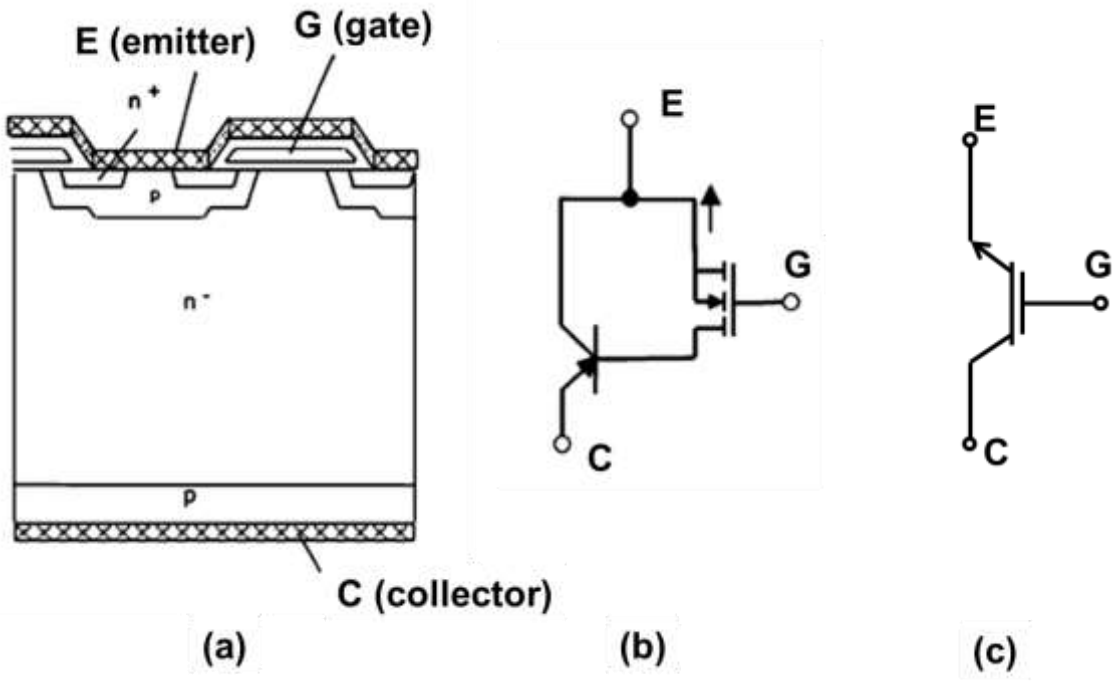


Fig. 1.7 (a) IGBT device structure and (b) equivalent circuit (c) symbol.

The device structure of an IGBT is a combination of an N-type MOSFET in the lateral direction and a PNP BJT in the vertical direction. This structure provides high conductivity in the on-state and high breakdown voltage in the off-state. The on / off state of the MOSFET is controlled by the gate terminal voltage. The MOSFET turns on when the gate voltage is high, and the electron current flows from the emitter terminal through the N^- layer to the collector terminal. The BJT is turned on by flowing the electron current of the MOSFET to the N^- layer. In this state, the accumulation of electrons and holes in the N^- layer causes electric conductivity modulation to achieve the lower voltage drop across the IGBT device. On the other hand, the MOSFET turns off when the gate voltage is low. Since the MOSFET current is off, the base current of the BJT disappears and the BJT turns off. In the off-state, a wide depletion layer appears in the N^- layer. This depletion layer realizes high breakdown voltage. Thus, the IGBT has the property of being the bipolar device that can be controlled by the insulated gate.

Since the IGBT has the structure and the function combining MOSFET and BJT, the equivalent circuit is also provided in the same form. This equivalent circuit is a bit complicated to use as a circuit symbol. Therefore, the symbol is usually represented in the form of the BJT with the insulated gate for simplicity. For the convenience of describing the device structure in Fig. 1.7, a collector terminal which is applied a high voltage is placed on the bottom. In the circuit description, however, the high voltage terminal is located on the upper side. Thus, it should be noted that the up side and the down side of a device structure figure and those of a circuit schematics are reversed. Therefore, when writing a circuit schematic, the symbol in Fig. 1.7 (c) is handled upside down.

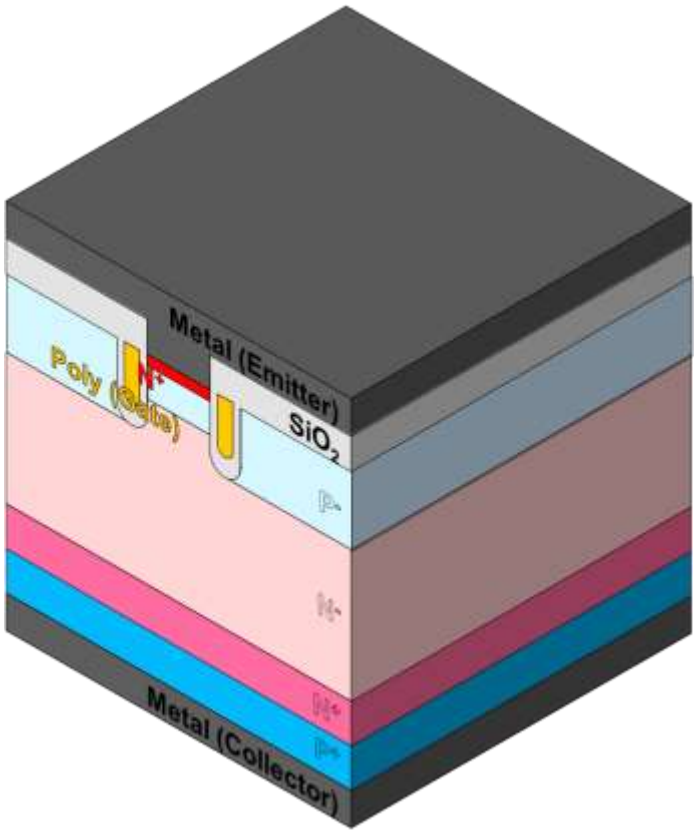
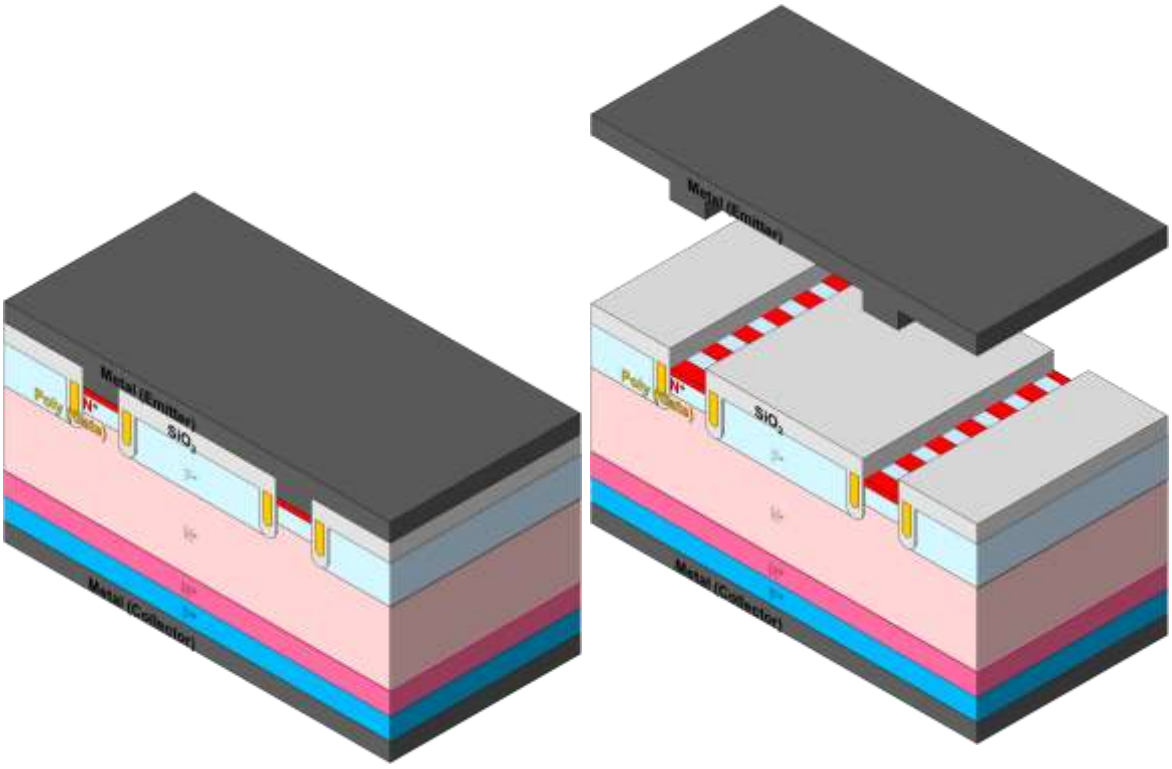


Fig. 1.8 A 3D device structure of PT trench gate IGBT.



(a) (b)

Fig. 1.9 3D device structures of two IGBT cells (a) with emitter metal and (b) without emitter metal.

Fig. 1.8 shows a 3D device structure of a punch-through (PT) trench gate IGBT. The IGBT has high current density. By creating a MOS structure on the side of the trench gate, the density of the cell is increased and the conduction loss of the channel is reduced. Also, by adopting the PT structure, the thickness of the N - layer is made thin and the conduction loss is reduced. This structure is widely adopted for the current IGBT.

In a IGBT chip, this cell structure is repeatedly formed over the entire chip area. Fig. 1.9 (a) shows a 3D device structure of two IGBT cells. Cell structures are formed at regular intervals in the lateral direction. Also, Fig. 1.9 (b) shows the 3D device structure without emitter metal. In the depth direction of the trench gate structure, P^- layer and N^+ layer are formed in a stripe shape. As described above, in the IGBT chip, the cell structure is formed in the lateral direction and the depth direction.

1.4. IGBT switching behaviors

The IGBT exhibits a special behavior during switching. This is due to the special device structure of the IGBT for achieving high breakdown voltage. Since the width of the depletion layer existing in the N^- layer changes during on / off switching of the IGBT, the capacity of the depletion layer changes along with the change of V_{CE}. By changing the capacitance of the depletion layer, the capacitance between the gate and the collector of the IGBT changes. This capacitance change causes the behavior in which the gate voltage trajectory becomes horizontal during switching. This horizontal gate voltage trajectory is called a Miller plateau. In this section, I describe the IGBT switching behaviors of turn-on and turn-off, and the importance of the IGBT gate control.

1.4.1. Explanation and analysis of turn-on behavior of IGBT

The IGBT turn-on behavior is divided into four phases. Fig. 1.10 shows an IGBT turn-on waveform of a collector current (I_C), a collector-emitter voltage (V_{CE}) and a gate-emitter voltage (V_G). The IGBT gate has two parasitic capacitances, a gate-emitter capacitance (C_{GE}) and a gate-collector capacitance (C_{GC}). These two capacitances are the basis of a unique gate voltage waveform of an IGBT.

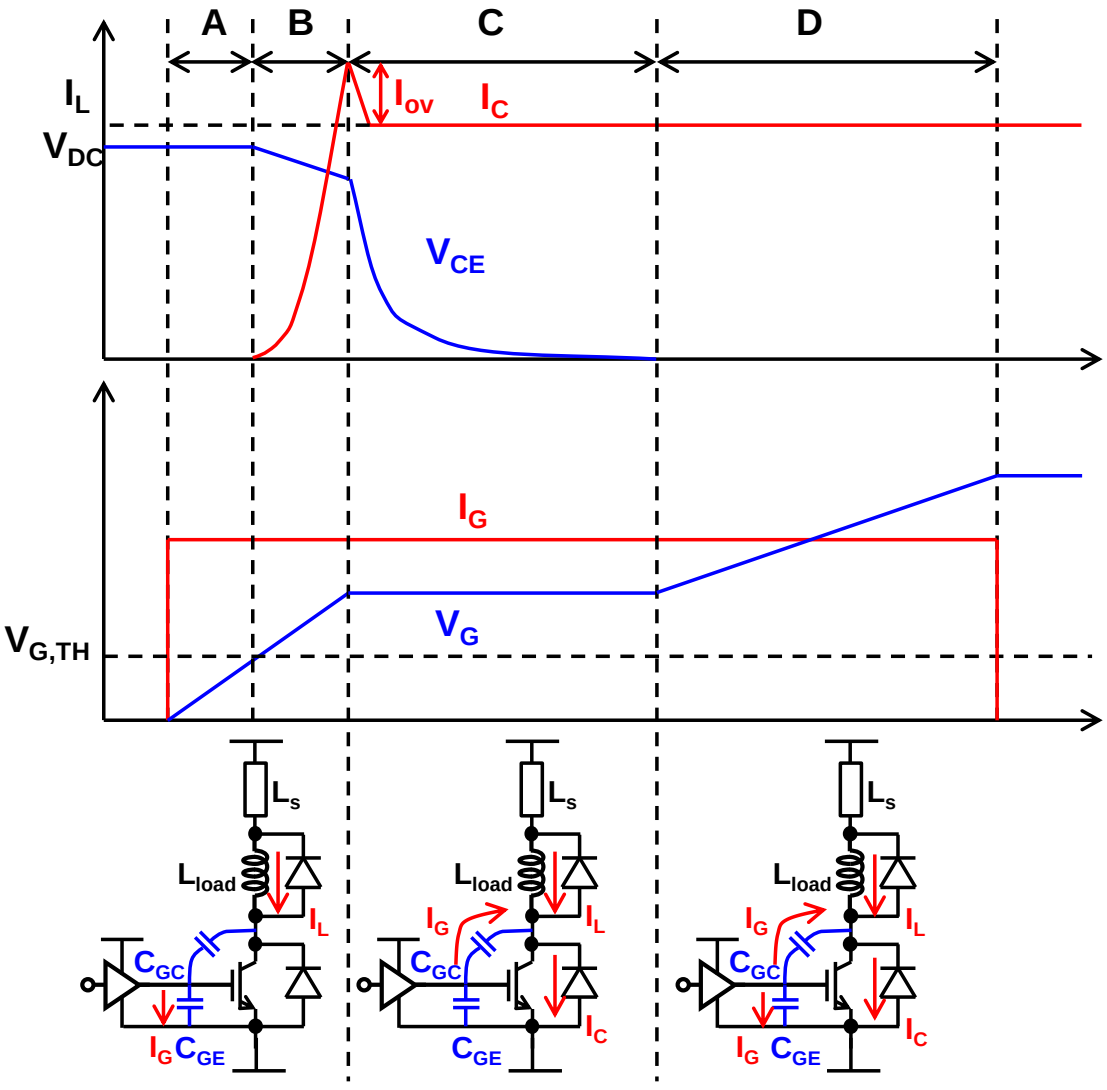


Fig. 1.10 The IGBT turn-on waveform diagram divided into four phases. (Phase A) before the turn-on. (Phase B) a start of turn-on (Phase C) a Miller plateau (Phase D) after the Miller plateau.

Phase A in Fig. 1.10 shows the gate voltage operation before the IGBT turn-on operation. In this state, the gate current I_G flows mainly into C_{GE} and continues until the voltage V_G exceeds the threshold voltage $V_{G,\,th}$. During this timeframe, at the capacitance value of the C_{GC} is very small and can be almost ignored. Therefore, the gate voltage is expressed by a following equation.

$$\frac{dV_G}{dt} = \frac{I_G}{C_{GE}} \tag{1.1}$$

Phase B in Fig. 1.10 shows a start of the IGBT turn-on switching and V_G changes in the same way as Phase A according to Eq. (1.1). When V_G exceeds $V_{G,\,th}$, the turn-on operation starts. During this timeframe, V_{CE} decreases and I_C increases. The current I_C rapidly increases until it reaches the load current I_L flowing in the inductive load. On the other hand, V_{CE} drops very slowly until I_G reaches I_L. The I_C change at this moment is expressed by a following equation,

$$\frac{dI_C}{dt} = g_m \frac{I_G}{C_{GE}} . \tag{1.2}$$

Here, C_{GC} is a very small value and ignored, g_m the transconductance of the IGBT described later. In the subsequent calculations, g_m is treated as a constant for simplicity. On the other hand, V_{CE} drops very slowly until I_G reaches I_L according to stray inductance of a busbar L_s and I_C change. The V_{CE} change is expressed by a following equation,

$$\frac{dV_{CE}}{dt} = L_s \frac{dI_C}{dt} = g_m L_s \frac{I_G}{C_{GE}} . \tag{1.3}$$

At an end of phase B, I_C reaches I_L with an overshoot current. The overshoot current caused by a reverse recovery current and a junction capacitance of high-side diode in Fig. 1.10. Fig. 1.11 shows a schematic current waveform of Si-diode turn-off during IGBT turn-on. Q_{rr} equals to diode's stored charge. The reverse current I_{rr} is expressed by a following equation,

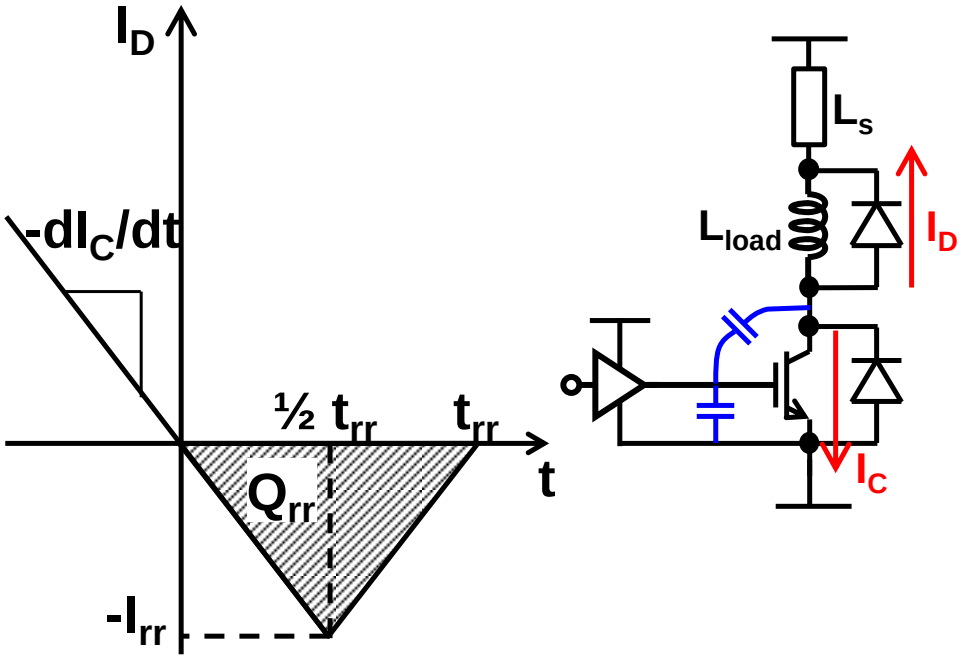


Fig. 1.11 Schematic current waveform of Si-diode turn-off during IGBT turn-on.

$$I_{rr} = I_{ov} = \sqrt{Q_{rr}\frac{dI_C}{dt}} = \sqrt{g_m Q_{rr}\frac{I_G}{C_{GE}}}\,. \tag{1.4}$$

The overshoot current during the turn-on switching is expressed by I_L+I_{rr}. And power loss in phase B is expressed by a following equation,

$$P_B = V_{DC}\int_{phaseB} I_C dt = \frac{1}{2}V_{DC}I_L^2\frac{C_{GE}}{g_m I_G}\,. \tag{1.5}$$

Here, the change of V_{CE} and the overshoot current I_{rr} are ignored for simplicity. From Eqs. (1.4)(1.5), switching characteristics in phase B is controlled by I_G.

Phase C in Fig. 1.10 shows a waveform of the IGBT Miller plateau. After I_G reaches I_L, V_{CE} drops rapidly. As the voltage of V_{CE} changes, the capacitance value of C_{CG} also increases. Fig. 1.12 shows collector-emitter voltage dependency of IGBT parasitic capacitances [1.16]. In this figure, C_{res} corresponds to C_{GC}. C_{GC} increases sharply with voltage drop of V_{CE}. During this timeframe, as shown in Fig. 1.10 (b), the current I_G flows into C_{GC}. This is because C_{GC} increases even if it is attempted to raise V_G by I_G, so that the

current is consumed to charge the increased capacity. From the contact equation at the gate contact, the above behavior is shown by a following equation,

$$I_G - C_{GE}\frac{dV_G}{dt} - C_{GC}\frac{d(V_G - V_{CE})}{dt} = 0\,. \tag{1.6}$$

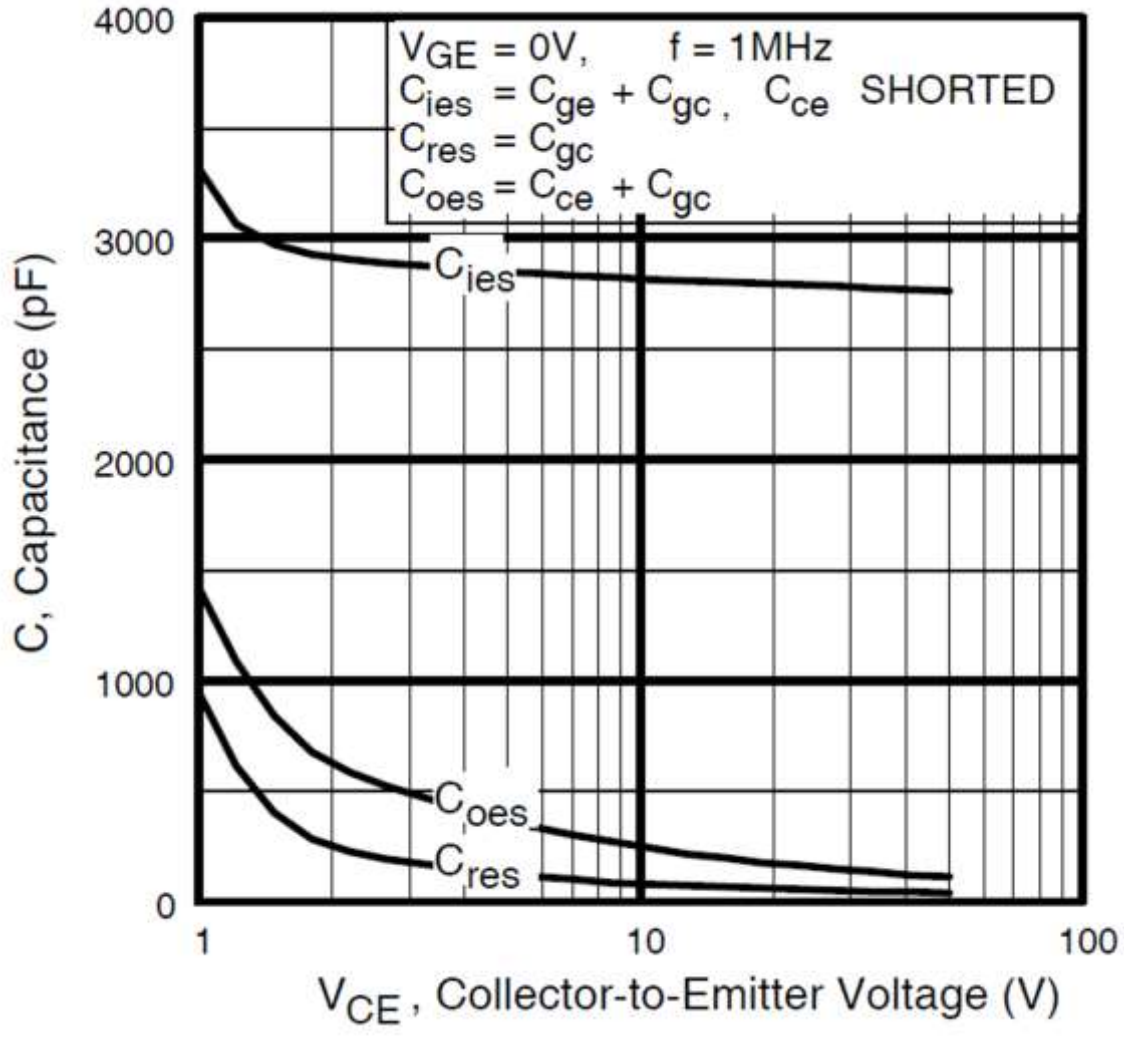


Fig. 1.12 Collector-emitter voltage dependency of parasitic capacitance of IGBT [1.16].

Similarly, from the equation at the collector contact, the behavior is shown by a following equation,

$$I_L - I_C(V_G) - C_{GC}\frac{d(V_{CE}-V_G)}{dt} - C_{CE}\frac{dV_{CE}}{dt} = 0. \quad (1.7)$$

Here, I_C (V_G) represents that I_C is a function of V_G and I_C. V_G during the Miller plateau are described by following equations,

$$I_C = \beta(V_G - V_{G,TH})^2, \quad (1.8)$$

$$V_{G,Miller} = V_{G,TH} + \frac{I_L}{g_m} \quad (1.9)$$

Here, the coefficient β is determined by the MOSFET and the BJT in the IGBT. The simultaneous equations of Eqs. (1.6) (1.7) give a following equation,

$$C_{GE}\frac{dV_G}{dt} = I_L - I_C(V_G) \equiv I. \quad (1.10)$$

Here we approximated as $C_{GC} \gg C_{CE}$ and $I_L \gg I_G$. Consider the point where I = 0, that is, when the I_C reaches I_L. Let us consider the case where V_G deviates from the Miller voltage. As V_G increase, I_C increase and I<0. Conversely, As V_G decrease, I_C decrease and I>0. This means that d V_G / d t takes a value in the opposite direction to the change of V_G and negative feedback is applied. Therefore, I = 0, that is, dV_G / dt = 0 and the Miller plateau appears. This continues while I_G decreases the gate-collector voltage. In other words, while V_{CE}>V_G, this relational expression holds. The V_{CE} voltage change in this timeframe is expressed by a following equation,

$$\frac{dV_{CE}}{dt} = -\frac{I_G}{C_{GC}}. \quad (1.11)$$

Here, C_{GC} is a function of V_{CE} as shown in Fig. 1.12. And switching loss during phase C is expressed by a following equation,

$$P_C = I_L \int_{phaseC} V_{CE}dt = I_L \int_{phaseC} (V_{DC} - \frac{I_G}{C_{GC}}t)dt = \frac{1}{2}\frac{C_{GC}}{I_G} I_L V_{DC}^2. \quad (1.12)$$

Here, C_{GC} is treated as a constant for simplicity.

After the Miller plateau end in Phase D, C_{GC} become a fixed value. Therefore, the behavior of V_G is to charge up the fixed value capacity by I_G. And V_G expresses the following equation,

$$\frac{dV_G}{dt} = \frac{I_G}{C_{GE} + C_{GC}} . \tag{1.13}$$

In the IGBT turn-on operation, the Miller plateau appears due to the C_{GC} change that depend on V_C. And the span of Miller plateau is controlled by I_G according to Eqs. (1.2) (1.10) (1.11). Also, from the equations (1.4)(1.5)(1.12), the current overshoot and the switching loss depend on I_G. This means that the IGBT switching characteristics can be controlled with I_G. In addition, as described above, the period during which the voltage changes and the current changes appear in different periods, so that it is possible to adjust them separately.

1.4.2. Explanation and analysis of turn-off behavior of IGBT

The IGBT turn-off is divided in four phases as well as turn-off. Fig. 1.13 shows an IGBT turn-off waveform of I_C, V_{CE} and V_G. The IGBT gate has two parasitic capacitances, C_{GE} and C_{GC}. These two capacitances are the basis of the special gate voltage trajectory of the IGBT same as the turn-on case.

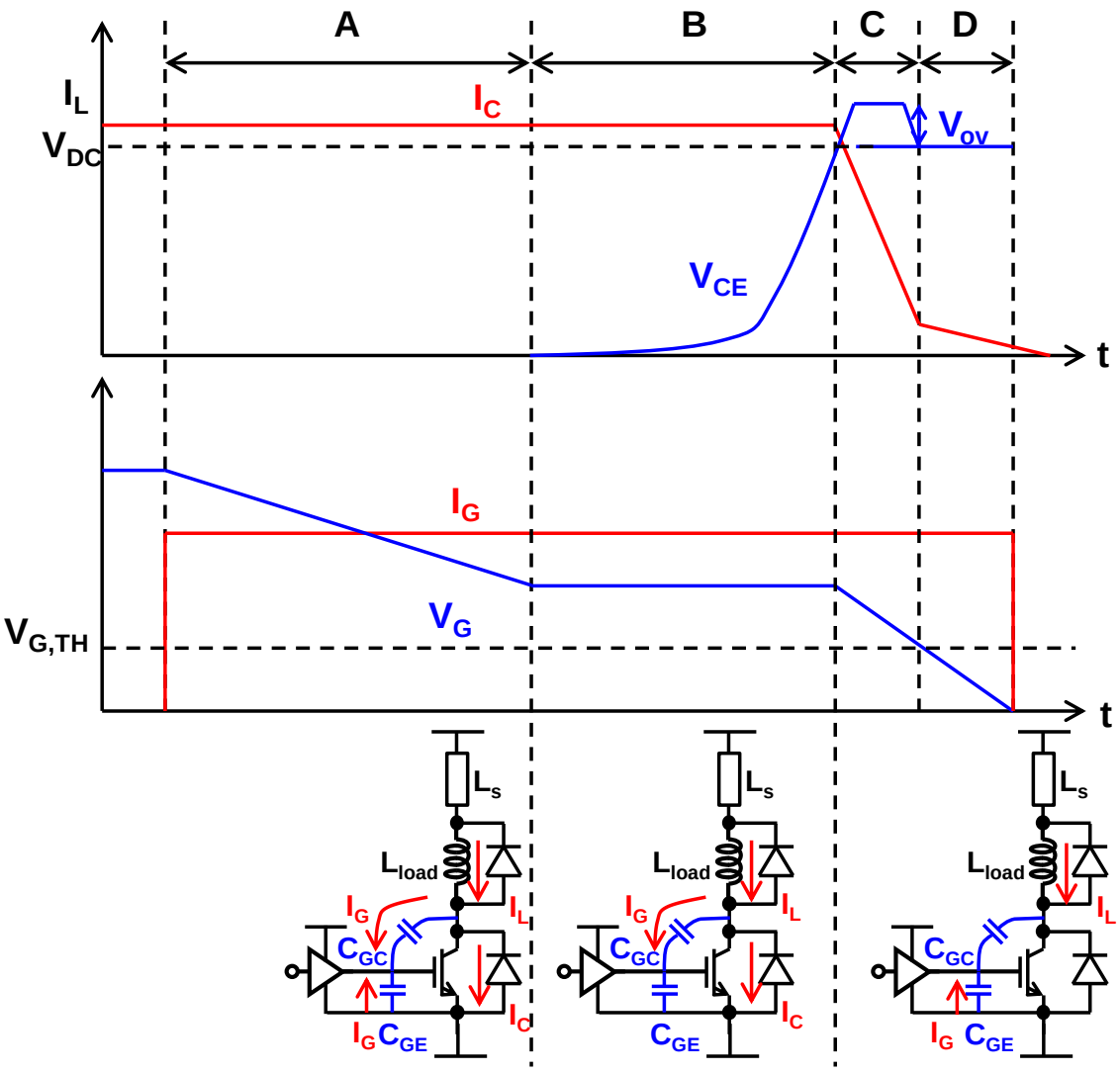


Fig. 1.13 The IGBT turn-off waveform diagram divided into four phases. (Phase A) before the turn-off. (Phase B) a start of turn-off (Phase C) the Miller plateau (Phase D) after the Miller plateau.

Phase A in Fig. 1.13 shows the gate voltage operation before the IGBT turn-off operation. In this state, the gate current I_G flows out mainly from C_{GE} and C_{GC} continues until the voltage V_G reaches the Miller voltage. The Miller voltage is expressed by Eq. (1.9). During this time, the turn-off of the IGBT has not started yet. Therefore, the gate voltage is expressed by Eq. (1.13). Here, I_G takes negative value in the turn-off case.

Phase B in Fig. 1.13 shows a waveform of the IGBT Miller plateau. When V_G reaches the Miller voltage, the turn-off operation starts. In this timeframe, V_{CE} increase and I_C decrease start. V_{CE} increases according to the C_{GC} change and I_G. On the other hand, I_C drops very slowly until the Miller plateau comes to a second half. The collector voltage change during this timeframe is expressed by Eq. (1.11). In the phase B, the current I_G flows out from C_{GC}. This is because C_{GC} decreases even if it is attempted to drop V_G by I_G, so that the current is consumed to discharge the decreased capacity. The above behavior is shown by Eq. (1.11) as in the turn-on case. As can be seen from the fact that the same equation as at the turn-on is obtained, it can be seen that the Miller plateau also appears at the turn-off. And switching loss in this phase B is expressed like Eq. (1.12) at turn-on case.

Phase C in Fig. 1.13 shows waveform diagram after the Miller plateau end, C_{GC} become a fixed value. Therefore, the behavior of V_G is to discharge the fixed value capacity by I_G. And V_G is expressed by Eq. (1.1). And the I_C change during this timeframe is expressed by Eq. (1.2). The voltage overshoot is caused by the I_C change and L_S, so it is expressed by following equation,

$$V_{ov} = -L_s \frac{dI_C}{dt} = -g_m L_s \frac{I_G}{C_{GE}}. \tag{1.14}$$

The switching loss in phase C expressed like Eq. (1.5) at turn-on case.

In the IGBT turn-off operation, the Miller plateau appears due to C_{GC} change that depend on V_C. From the Eqs. (1.2) (1.10) (1.11), a slew rate of V_{CE}, I_C and a span of Miller plateau

depend on I_G. Also, from the Eqs. (1.4)(1.5)(1.12), the voltage overshoot and the switching loss depend on I_G. This means that the IGBT switching characteristics can be controlled with I_G This means that the IGBT switching characteristics can be controlled with I_G same as the turn-on case. In addition, as described above, the period during which the voltage changes and the current changes appear in different periods, so that it is possible to adjust them separately.

As can be seen from above the description, the IGBT the switching characteristics of the turn-on and the turn-off case is controlled with the gate current I_G. The slew rate of V_{CE} and I_C is related to the noise generation during the switching. And the switching span which the Miller plateau occupies a large proportion relates to the switching loss. Therefore, to obtain appropriate switching characteristics, it is necessary to set the I_G appropriately. In the previous study, it is said that it is better to decrease I_G during the period when I_C and V_C change significantly, and increase I_G during other periods. I_G is the output of the gate driver. So, I_G is controlled by the gate driver. The design of the gate driver is the important technology to set the properly set I_G, to fully bring out the IGBT performance and to improve the switching noise and loss.

1.5. Problems in high-performance IGBT

The current density improvement of the IGBT is important for improving the efficiency of the power conversion circuit, but at the same time the safety problem becomes larger. There are two problems in improving current density of the IGBT. There are noise generation and short-circuit tolerance. In order to put the high-performance IGBT into practical use, it is necessary to solve these two problems. In this section, the safety problem of high-performance IGBT and the importance of the IGBT gate control is described.

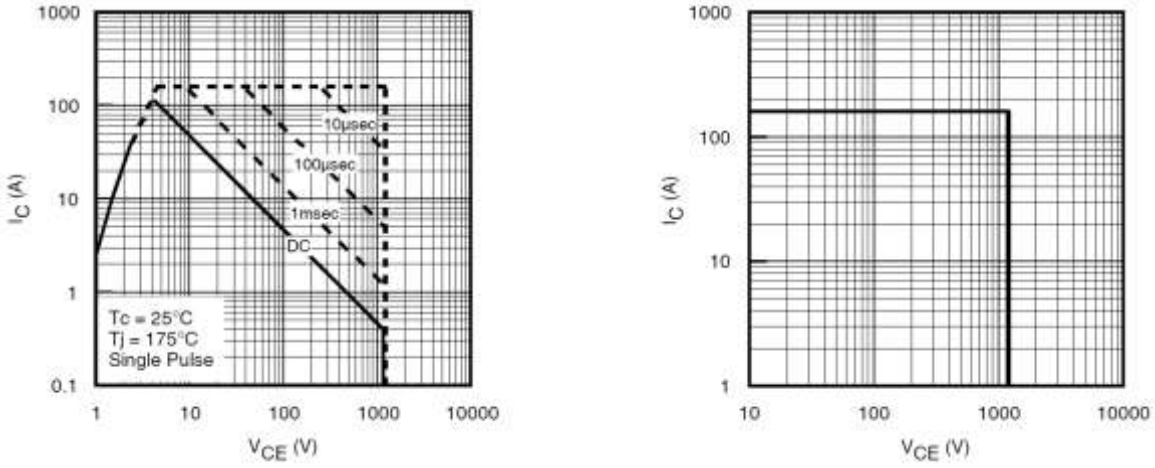


Fig. 1.14 (a) Forward SOA. (b) Reverse bias SOA [1.16].

Fig. 1.14 shows safe operating areas (SOAs) of an IGBT [1.16]. SOAs indicate the area where the device operates safely. A SOA at turn-on switching and on-state is indicated by Forward SOA shown in Fig. 1.14 (a). T_c and T_j indicate the case temperature of the device and the junction temperature, respectively. The dashed line means that it must not stay beyond that line for more than the attached time. A SOA at turn-off switching is indicated by reverse bias SOA shown in Fig. 1.14 (b). The switching of the IGBT should be within

the range of SOAs.

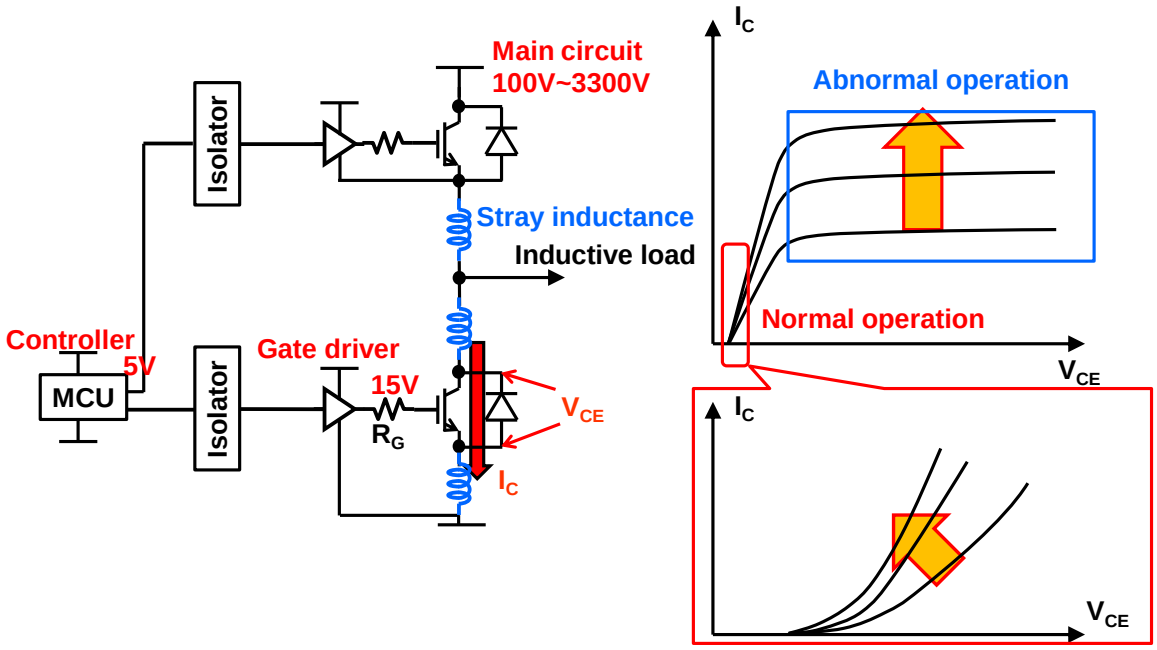


Fig. 1.15 Effect of increasing current density of IGBTs.

Fig. 1.15 shows effect of increasing current density of IGBTs. The IGBT noise generated by the current slew and the stray inductance of a power conversion circuit board. Because of these two factors, voltage noise is generated at the switching operation. The voltage noise becomes radiation noise and voltage stress to the IGBT in the other legs via the inductive load. Therefore, this noise causes the malfunction of the IGBT or surrounding machines. In the case of the high-performance IGBT, having the high current density, the current slew is increases during the switching operation that results in larger voltage noise. In order to solve this voltage noise problem, it is necessary to reduce the stray inductance of the power conversion circuit board or to reduce the current slew by applying the lower gate driving current. But the lower gate driving current results in the lower switching efficiency. Therefore, in order to applying this method, it is necessary to improve the trade-off between the switching loss and the V_C / I_C slew.

A short-circuit leads to device destruction due to excessive heat. In the normal operation

shown in Fig. 1.15, the IGBT on-voltage is low at the IGBT is on-state. On the other hand, in the short circuit condition, the IGBT on-state voltage is high as in the abnormal operation shown in Fig. 1.15. For example, consider the case where two IGBTs in the same leg simultaneously turn-on. In this case, A high voltage and a large current are simultaneously applied between the collector-emitter terminal of these IGBTs. At this moment, excessive heat is generated in these IGBTs. The excessive heat results in the device destruction. In order to prevent from the destruction, it is necessary to detect the short-circuit condition quickly and turn-off the IGBT gate appropriately before being destroyed by the heat. In the high-performance IGBT case, the overcurrent in the abnormal condition increases. The current increase in the abnormal operation accelerate the device destruction due to greater heat. There are three ways to prevent from this short-circuit destruction. One way is to increase the stray inductance intentionally. Increasing the stray inductance slows down the current increase speed of the IGBT during the short circuit. However, this method conflicts with the voltage noise solution that the stray inductance is reduced as mentioned above. Second way is to reduce the gate driving current. The lower gate driving current reduces the IGBT current slew in the switching operations. As mentioned in the previous paragraph, however, the lower gate driving current results in the lower switching efficiency. Third way is to detect the short-circuit condition more quickly. This requires a high speed short circuit detection function by the gate driver.

For these problems of the noise and the short-circuit, passive components are required conflicting characteristics. Therefore, it is necessary to solve these problems by applying the gate driver technology that controls the IGBT gate actively.

1.6. Research objectives

The objective of this research is to study a gate driver suitable for high-performance IGBTs. The high-performance IGBTs mean high current density switches with low on-voltage. As mentioned in the previous section, the high-performance IGBTs have safety problems in terms of the noise and the short-circuit. However, conflicting problems will be appeared when attempting to solve these problems using passive elements. One of the problems is that the characteristics of the stray inductance required for noise and the short circuit are opposite to each other. Another is that the trade-off with power efficiency when solving by adjusting gate drivability. Therefore, a gate driver with an active function is the key technology for the high-performance IGBT switching.

In addition, adjusting the IGBT switching characteristics becomes a serious task as the performance of the IGBT improves. The IGBT switching characteristics change depending on the parasitic components of the power conversion circuit board, variations in device characteristics, and operating conditions. In order to solve these problems, not only examination at the simulation level but also adjustment at the actual machine level may be necessary. An optimization method of the IGBT switching characteristics is important task.

Corresponding to these motivations, this research has the following concrete objectives:

1. Investigate circuit design techniques to drive the high-performance IGBT.
2. Investigate optimization techniques to search optimal gate driving waveforms of IGBT.
3. Investigate circuit design techniques to improve the speed and the robustness of short-circuit detector.

In the conventional design, gate drivers are composed of just passive components. It is

impossible to flexibly coping with the changes in operating conditions. This must be designed according to the worst operating conditions, and it is necessary to set the IGBT switching characteristics poor. In addition, switching characteristics are different depending on device variations. Therefore, the engineer needs to adjust the switching characteristics at the actual machine level. It is costly. On the other hand, conventional short-circuit detectors need a current sensor or a voltage sensor for high voltage applications. These sensors are slow in response speed, so they are not suitable for high-speed short-circuit detection.

Therefore, the significance of this research in terms of engineering resides in the following points.

1. The circuit scheme for programmably generating gate drive waveform was proposed to improve the trade-off between switching loss and noise of IGBTs whereas conventional gate drivers have low or no programmability.
2. The automatic optimization method using simulated annealing algorithm is proposed to search optimum gate driving waveforms of IGBTs whereas they were searched by hand.
3. High speed short-circuit detector with a tolerance to operating condition is proposed whereas the conventional short-circuit detector was relatively slow or low in robustness.

1.7. Chapter organization and overview

This paper is organized as follows.

Chapter 2 proposes the programmable gate driver techniques. The gate driver has This gate driver is of a clock synchronous type, and by using output transistors connected in

parallel, the output driving force and the output timing are programmably controlled.

Chapter 3 proposes the automatic optimization method of IGBT gate driving waveform. This method automatically searches for the optimum gate driving waveform by applying the simulated annealing to the search algorithm using the gate driver introduced in Chapter 2.

Chapter 4 proposes novel short-circuit detectors. It has an analog delay multiplier circuit to improve robustness to change of operating conditions.

Conclusions based on this research are presented in Chapter 5.

Fig. 1.16 summarizes the organization overview of this thesis.

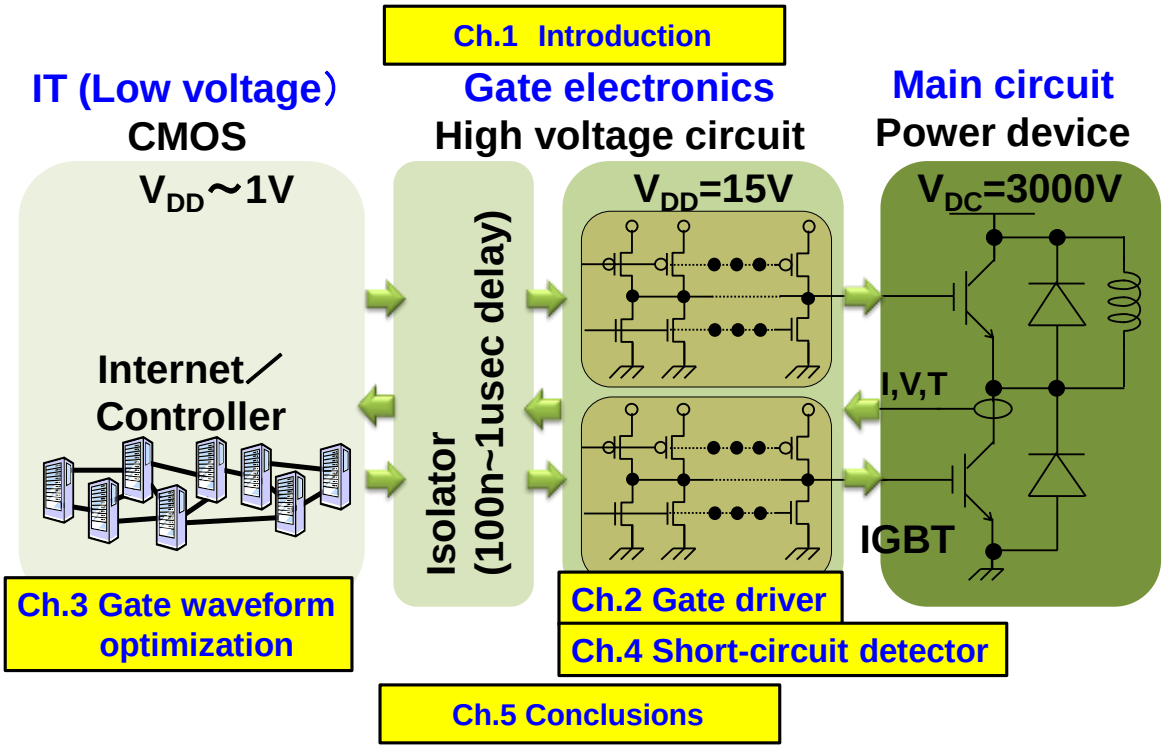


Fig. 1.16 Paper organization.

1.8. References

[1.1] P. Gueguen, “How Power Electronics will reshape to meet the 21st century challenges?” IEEE Int. Symp. on Power Electronics Conf. and Expo., pp. 17-20, May 2015.

[1.2] G. Majumdar, “Power Module Technology for Home Power Electronics,” Proc. Int. Power Electronics Conf. pp. 773-777, 2010.

[1.3] S. E. Bererich, A. J. Bauer, L. Frey and H. Ryssel, “Triple trench gate IGBTs,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 251-254, May 2005.

[1.4] M. Takei, S. Fujikake, H. Nakazawa, T. Naito, T. Kawashima, K. Shimoyama and H. Kuribayashi, “DB (Dielectric Barrier) IGBT with extreme injection enhancement,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 383-386, May 2010.

[1.5] M. Momose, K. Kumada, H. Wakimoto, Y. Onozawa, A. Nakamori, K. Sekigawa, M. Watanabe, T. Yamazaki and N. Fujishima, “A 600V Super Low Loss IGBT with Advanced Micro-P Structure for the next Generation IPM,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 379-382 May 2010.

[1.6] L. Zhu and X. Chen, “A Novel Snapback-Free Reverse Conducting IGBT with Anti-parallel Shockley Diode,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 261-264, May 2013.

[1.7] J. Hu, M. Bobde, H. Yilmaz and A. Bhalla, “Trench Shielded Planar gate IGBT (TSPG-IGBT) for Low Loss and Robust Short-Circuit Capalibity,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 25-28, May 2013.

[1.8] L. M. Selgi and L. Fragapane, “Experimental evaluation of a 600 V super-junction planar PT IGBT prototype – Comparison with planar PT and trench gate PT technologies,” IEEE European Conf. Power Electronics and Applications, pp. 1-7, Sept. 2007.

[1.9] J. Kim, S. Kim, K.-H. Oh and C. Yun, “A 600V FS-IGBT using locally isolated P-well structures for improved short circuit ruggedness,” IEEE Int. Conf. Power Electronics and ECCE-Asia, pp. 823-828, Jun. 2015.

[1.10] R. Kimibaba, K. Konishi, Y. Fukada, A. Narazaki and M. Tarutani, “Next Generation 650V CSTBTTM with improved SOA fabricated by an Advanced Thin Wafer Technology,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 149-152, May 2015.

[1.11] A. Theisen, T. Heinzel, J. Kawabata, Y. Kusunoki, Y. Nishimura, Y. Onozawa, Y. Kobayashi and O. Ikawa, “The Compact and High Power Density 7th Generation IGBT Module,” IEEE European Conf. Power Electronics and Applications, pp. 1-10, Sept. 2015.

[1.12] K.-H. Oh. J. Kim, H. Seo, J. Jung, E. Kim, S.-S. Kim and C. Yun, “Experimental Investigation of 650V Superjunction IGBTs,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 299-302, Jun. 2016.

[1.13] H. Feng, W. Yang, Y. Onozawa, T. Yoshimura, A. Tamenori and J. K. O. Sin, “A 1200 V-class Fin P-body IGBT with Ultra-narrow-mesas for Low Conduction Loss,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 203-206, Jun. 2016.

[1.14] Z. Yang, J. Zhu, W. Sun, J. Zhou, Y. Zhu, P. Ye and Z. Li, “A Low Loss IGBT with Shallow p-well to Adjust the Carrier Profiles at the Emitter Side,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 327-330, Jun. 2016.

[1.15] M. Rahimo, M. Andenna, L. Storasta, C. Corvasce and A. Kopta, “Demonstration of an Enhanced Trench Bimode Insulated Gate Transistor ET-BIGT,” IEEE Proc. Int. Symp. Power Semiconductor Devices and ICs, pp. 151-154, Jun. 2016.3

[1.16] International Rectifier, “INSULATED GATE BIPOLAR TRANSISTOR,” IRG7PH46UPbF datasheet, Jul. 2012.

Chapter 2

Clocked Gate Driver (CGD) IC Design

2.1. Introduction

A gate driver is the key technology for the switching of power devices. The gate driver is required to reduce noise and loss during the switching operation of the power devices. During the switching operation of the power devices, current / voltage noise is generated in the power conversion circuits as shown in Fig. 2.1. This noise generated by the switching power device causes malfunction and device stress of the switching device itself and other devices. These events caused by the noise are a serious problem leading to device destruction. Furthermore, there is a trade-off relationship between noise and loss, and it is necessary to properly set the gate driver depending on the application. For the future power devices with increased power density as described in Chapter 1, this problem becomes more serious. Important functions of the gate driver are suppression of the noise generation at the

switching operation, and of malfunction due to the influence of the noise while suppressing increase in switching loss.

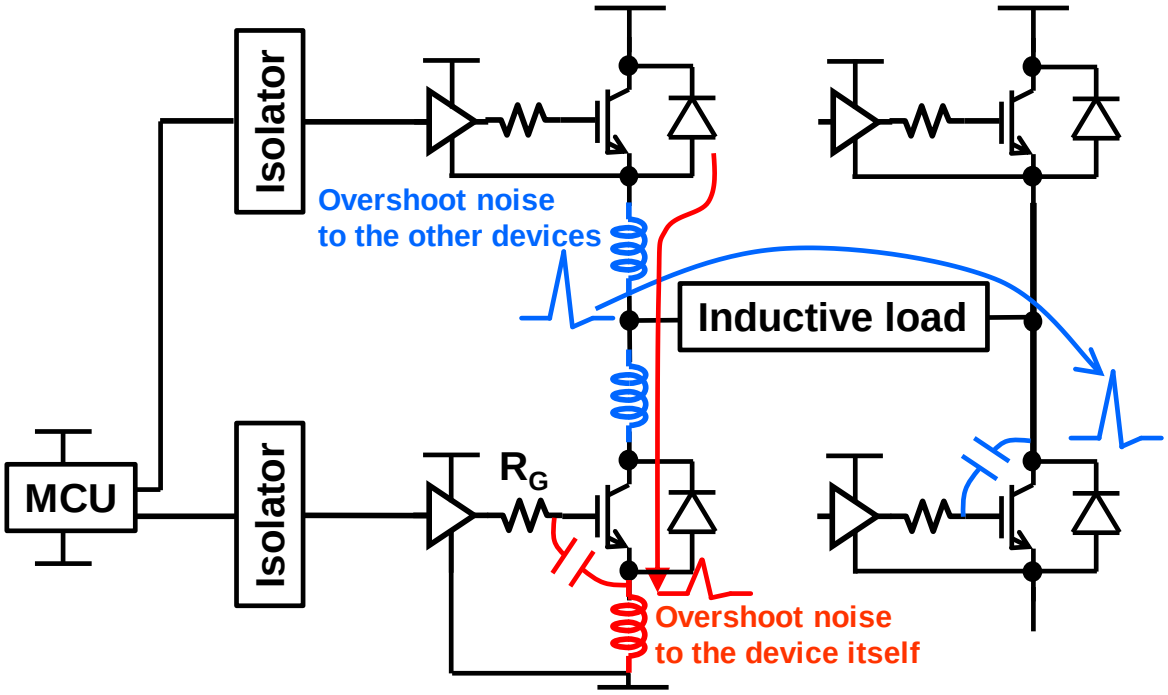


Fig. 2.1 The Overshoot noise generated in the power conversion circuit at the switching operations.

The noise to the other devices is generated by the stray inductance and the current change. This is because a large self-induced electromotive force (EMF) is generated by abrupt change in the current flowing through the stray inductance. These factors appear in the form of voltage overshoot at the output of the leg. This voltage overshoot is conducted to the other leg via the inductive load. The voltage overshoot has two effect on the other leg. One is excessive voltage stress on a power device in the other leg. When the excessive voltage stress by the voltage overshoot is repeatedly applied to the power device, it leads to degradation or destruction of the device. Another is malfunction of a gate driver of the other leg. A sharp voltage slew that occurs with the voltage overshoot causes a voltage change in

the gate driver of the other leg output through the gate-collector capacitance (so called Miller capacitance). The voltage change leads to malfunction of the power device of the other leg. The voltage overshoot is the main problem of the noise to other devices.

There are two methods to solve the voltage overshoot problem. Ones is to reduce the stray inductance. It is necessary to design the circuit board so that the floating inductance is sufficiently small with respect to the current flowing on the board. The other is to adjust the drivability of the gate driver. In the example of Fig. 2.1, the drivability is adjusted by the gate resistance R_G. However, there is a trade-off between suppression of the voltage overshoot and tolerance by R_G adjustment. Consider the case where R_G is increased. The voltage overshoot is suppressed because R_G slows switching. On the other hand, as R_G increases, the influence of the voltage overshoot on the gate driver output increases. This is because the increase in R_G is susceptible to the influence of the voltage change due to the capacitive coupling via the Miller capacitance. There is also a trade-off between switching speed determined by R_G and the switching loss. In the case of R_G increased, slow switching operation increases the switching loss and degrades power conversion efficiency. It is necessary to properly set R_G while taking into consideration this voltage overshoot suppression and tolerance tradeoff. As described above, in order to suppress the influence of the voltage overshoot and the switching loss, it is necessary to appropriately set the stray inductance and the gate resistance.

The noise to the switching device itself is generated by fast on / off switching operation and a reverse recovery current from a freewheeling diode of the other arm in the same leg as shown in Fig. 2.1. These factors appear as current overshoots flowing in the device during switching operation. This is because the fast switching operation causes the accumulated charge of the diode to be drawn instantaneously and a large reverse recovery current is generated. The current overshoot has two effect on the device in the switching operation.

One is overcurrent stress on the power device in the switching operation. When the overcurrent stress by the current overshoot is repeatedly applied to the power device, it leads to degradation and destruction of the device. Another is malfunction of the gate driver of the device in the switching operation. A sharp current slew that occurs with the current overshoot causes a voltage change in the gate driver output through the stray inductance of the emitter terminal (the emitter inductance). The emitter inductance generates self-induced EMF so as to hinder the switching voltage of the gate driver output. The current overshoot become self-poisoning noise of the switching device.

There are two methods to solve the current overshoot problem. One is to reduce the emitter inductance. It is necessary to design the circuit board so that the floating inductance is sufficiently small with respect to the current flowing on the board. The other is to increase the gate resistance R_G. This is because the large R_G slows the switching operation, the current overshoot and the current slew are suppressed. However, the slow switching operation increases switching loss and degrades power conversion efficiency. As described above, in order to suppress the influence of the current overshoot and the switching loss, it is necessary to appropriately set the emitter inductance and R_G.

The influence of the switching noise is suppressed by adjustment of R_G and the stray inductance reduction. However, these methods require more severe adjustment as the current density of the power device increases. This is because there is a trade-off between the noise suppression and tolerance by R_G, and restriction on board wiring to reduce the stray inductance. The gate driver must solve the above problem while suppressing the switching loss. Therefore, new noise countermeasures are required instead of conventional solutions. In this chapter, the programmable gate driver IC as the method to solve the noise problem is proposed. And it is demonstrated that the gate driver IC is effective for improving the trade-off between the overshoot noise and the switching loss during the turn-on

operation.

In this chapter, the gate driving waveform is optimized by hand using the programmable gate driver IC for the combination of the SiC-MOSFET and the SiC-diode, and the combination of the Si-IGBT and the SiC-diode. In the next chapter, automatic gate waveform optimization is performed using the same driver IC for the combination of Si-IGBT and Si-diode and Si-IGBT and SiC-diode. Table 2-1 shows a summary of device combinations and operating conditions experimented in this research.

Table 2-1 Summary of device combinations and operating conditions.

Power device / Diode	Si-IGBT		SiC-MOSFET	
	Operation	Subsection & operation condition	Operation	Subsection & Operation condition
SiC	Turn-on	2.4.1 (by hand) @500V 15.7A 3.5.1 (automatic) @500V 52A	Turn-on	2.4.2 (by hand) @500V 15.7A
	Turn-off	3.5.2 (automatic) @500V 52A		
Si	Turn-on	3.5.3 (automatic) @300V 52A	N/A	
	Turn-off	3.5.4 (automatic) @300V 52A		

2.1.1. Conventional gate drivers

Fig. 2.2 shows a conventional single resistor gate driver and its trade-off between overshoot and switching loss. This gate driver consists of an output buffer and the single resistor (R_G). As shown in the example in Section 2.1, the gate driver controls the switching characteristics with R_G. An advantage of the gate driver is simple architecture. However, as described in Section 2.1, to cope with a severe noise immunity requirement, it is necessary to respond only by changing the resistance parameter. Furthermore, it is possible to drive the gate optimally by dynamically changing the gate drivability from the Eqs. (1.4)(1.5)(1.12)(1.14) in Section 1.4. Therefore, with this gate driver, it is possible to satisfy the noise requirement and to reduce the switching loss when the current density of the power device is improved.

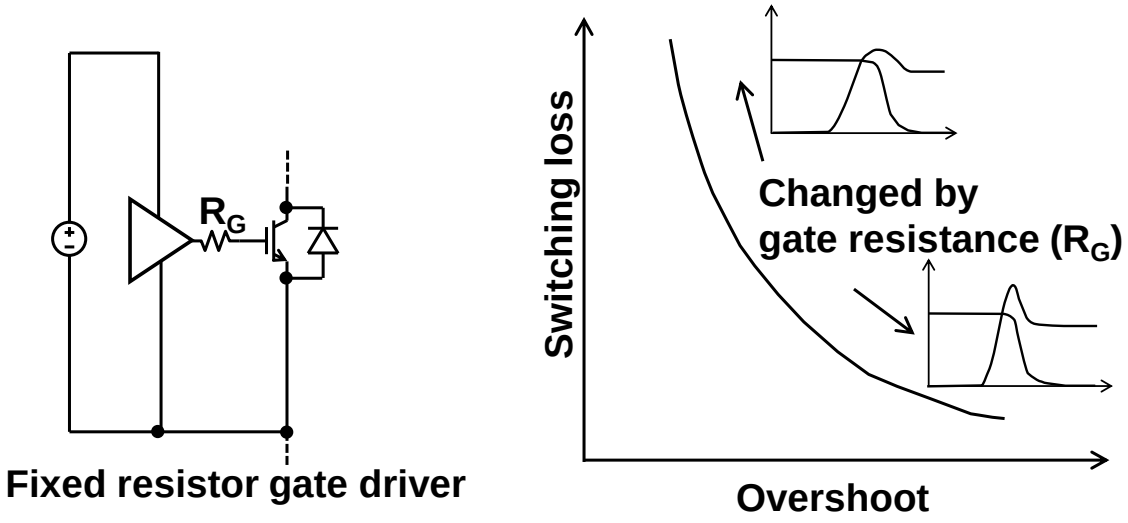


Fig. 2.2 Schematic of conventional single resistor gate driver and its trade-off between overshoot and switching loss.

2.1.2. Active gate drivers

Active gate drivers have been proposed to solve the problem of the conventional gate driver. Fig. 2.3 shows an active gate driver. The active gate driver has an output switch connected in parallel, and can output an arbitrary current (or set an arbitrary gate resistor) at an arbitrary timing [2.1] [2.2] [2.6] [2.10]. Therefore, as described in Chapter 2, it is possible to set the gate resistance to a low gate resistance in order to obtain noise immunity in the off-state while switching with an appropriate gate drivability. Also, since the gate drivability can be dynamically controlled, it is possible to dynamically control switching characteristics from the Eqs. (1.2)(1.11) in Section 1.4. Therefore, the active gate driver technology is an important technology to support the development of the future power devices.

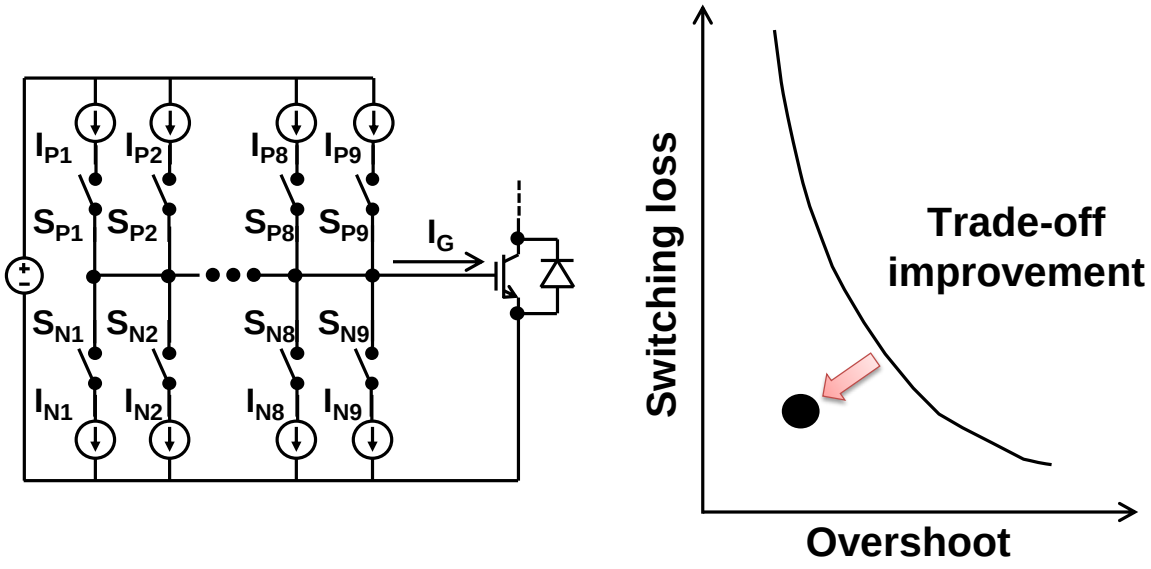


Fig. 2.3 Schematic of active gate driver and its trade-off improvement.

2.1.3. Active gate waveform

An active gate driving waveform is generated by dynamically controlling the gate drivability using the active gate driver. The main purpose of the active gate driving waveform is to improve the trade-off between turn-on / turn-off loss and current / voltage overshoot. Fig. 2.4 shows optimum gate driving waveforms described in previous research [2.10]. In the previous research, the trade-off is improved by lowering the gate drivability (I_G) only during the period when the I_C / V_C slew is large. As described in Section 2.1, a target of this gate driving waveform is to improving the switching performance by lowering I_C / V_C slew that causes the overshoot noise. Therefore, from the Eqs.(1.5)(1.12)(1.14) in Section 1.4, trade-off of the switching characteristics is improved by dynamically controlling I_G that can control I_C / V_C slew. By reducing the drivability only at the required moment, the increase in switching time is suppressed. As a result, the increase in switching loss is suppressed. For the above reasons, the trade-off improvement in the switching characteristics is realized by the active gate driving waveform as shown in Fig. 2.4.

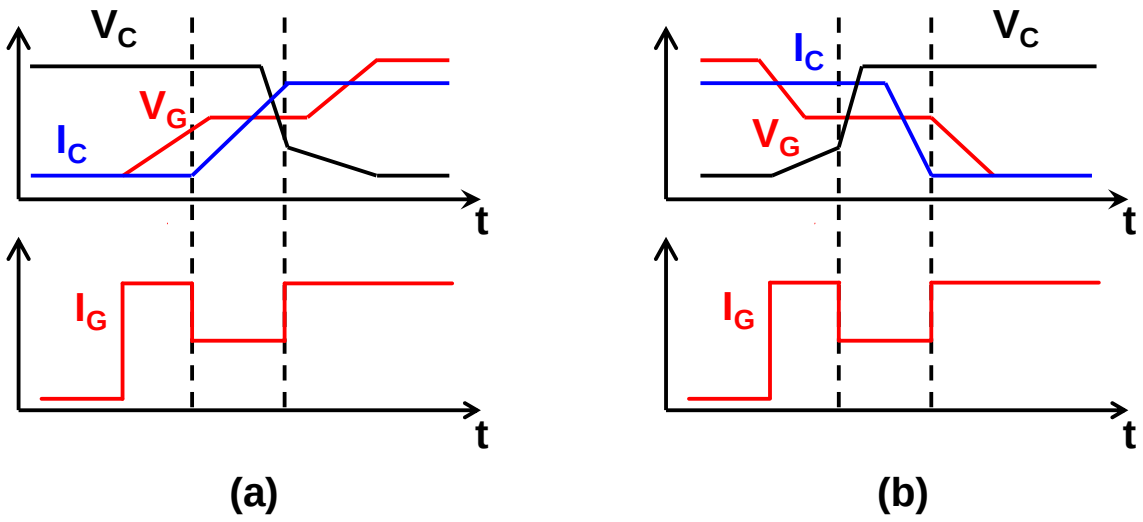


Fig. 2.4 The optimum gate driving waveforms described in the previous research [2.10]. (a) turn-on waveform (b) turn-off waveform.

2.1.4. Active gate driver specification

The function of the active gate driver is set an appropriate drivability at an arbitrary timing to improve switching characteristics of various power devices. For this reason, the active gate driver requires sufficient drivability and timing accuracy to control the gate of the target power device. From the Eqs. (1.1)(1.2)(1.11) in Section 1.4, the drivability and timing accuracy required to the active gate driver increase in proportion to g_m which is the transconductance of IGBT. g_m is also a numerical value representing the current density of the IGBT, so the higher the current density, the higher g_m per chip area. From Fig. 1.5, the current density of the power device has increased exponentially, and it is assumed that the increase will continue in the future. Therefore, the active gate driver with the high drivability accuracy and the timing accuracy is required for the future power devices.

Conventional active gate drivers have low drivability accuracy and no timing compensation function [2.10]. Therefore, in this research an active gate driver with high

drivability and timing accuracy is proposed and demonstrated that improve the switching characteristics of different type of power devices. Table 2-2 shows target specification of this thesis.

Table 2-2 Target specification of proposed active gate driver.

	Single resistor gate driver	Conventional active gate driver	Proposed active gate driver
Trade-off	**Bad**	**Good**	**Good**
Programmability	**No**	**Yes**	**Yes**
Accuracy in timing and drivability	×	×	◎

2.2. Proposed gate driver

The schematic diagram of the implemented general-purpose clocked gate driver (CGD) IC is shown in Fig. 2.5. CGD IC is developed for the switching of power devices at V_{DC} = 500V. In order to realize programmable 63-level drivability and timing control for the gate voltage of the power device of 15V, CGD IC is applied a clock circuit technique and high-voltage IC technology. CGD IC consists of 63-parallel drivers for 63-level drivability change, predrivers for the adjustment of output drivability of a single driver in the 63-parallel drivers, D-flipflops (DFFs) for the clock-based function. The parameters of NMOS in digital block are L=600nm and W=2μm, and the PMOS are L=600nm and W=2μm. Binary-to thermometer-code decoders prevents output noise due to timing skew in the IC. The Level shifters and buffer blocks shift up signals in low-voltage side to high-voltage side. Output of the driver IC is connected to the gate of the power device and input connected to a 6-bit binary control signal, B_{PMOS} (B_{NMOS}) and clock (CK). The control signal specifies

number of activated PMOS (NMOS) driver transistors. The power supply voltage (V_{DRIVE}) applicable to CGD IC is 5V–18V, and V_{DRIVE} of 15V is used in the following measurements. The voltage swing of input digital signals (B_{PMOS}, B_{NMOS}, and CK) is 5V, and the swing is increased to V_{DRIVE} by level-shifters.

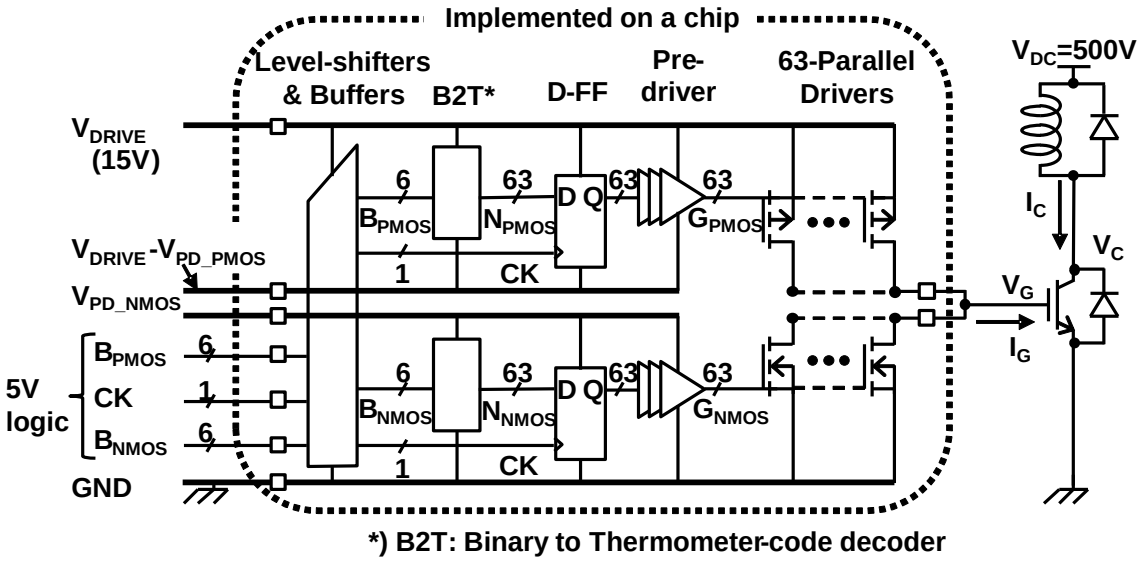


Fig. 2.5 Schematic diagram of general-purpose clocked gate driver IC.

Fig. 2.6 shows schematic of level-shifter and SR-latch buffer. Level shifter shifts up 0-5V input digital signals to 10-15V signals. This is because that a gate-source breakdown voltage of the PMOSs in 63-parallel drivers is only 5V compared to a drain-source breakdown voltage of 20V. Therefore, voltage swings of the digital signal for the PMOS must be 10-15V. The level shifter operates with pulse signals and consists of common-source circuit with Zener diode for protection of 5-V gate of the buffers from overvoltage. MOSFET of the common-source circuit is the same high-voltage n-MOSFET as 63-parallel drivers. In order to generate the pulse signal for the level shifters, pulse generator (Fig. 2.7) convert the digital input signal B_{PMOS} into the pulse signal. After the shifting up, the SR-

latch regenerate B_{PMOS} from the 10-15V pulse signal from the level shifter.

The binary to thermometer-code decoder converts the binary input signal B_{PMOS} (B_{NMOS}) to thermometer-code signal N_{PMOS} (N_{NMOS}). The binary-coded input is indispensable since 63 x 2 input pins are too many to handle. The binary signals, however, may cause spike problems in the gate current (I_G). When the spike occurs, a large voltage spike or voltage ringing may appear in the gate voltage (V_G). These abnormal behaviors in the gate voltage break down the power device by overvoltage in the gate or malfunction of power device. For example, when the binary input changes from 011111 (31) to 100000 (32), there is a possibility that the state goes from 011111 (31) to 111111 (63) to 100000 (32) causing a few nano-seconds glitch at the pre-driver, if there are variability of devices and interconnection designs which make the most significant bit change faster than the other bits. This is the cause of the spike problems. To prevent this problem, a small-sized binary to thermometer-code decoder in Fig. 2.8 is employed.

A pair of thermometer-code signals (B_{PMOS} and B_{NMOS}) are latched by the CK and activate the final 63 PMOS (NMOS) transistors via predrivers. In the following measurements, CK frequency is 25MHz and 40-ns time step control of the drivability is applied. This value was determined by the specification of measuring equipment.

Predrivers control output drivability of the 63 parallel drivers. Predrivers are consists of inverter chains as shown in Fig. 2.9. By adjusting the predriver voltage swing, V_{PD_PMOS} and V_{PD_NMOS}, from 1.2V to 5V, the output drivability of a single driver MOS transistor can be tuned from 3mA to 80mA. The peak drivability is 63 times of the single driver, which corresponds to the maximum peak current of the gate current (I_G) from 0.19A (= 3mA x 63) to 5A (= 80mA x 63). V_{PD_PMOS} and V_{PD_NMOS} of 1.8V is used in the following measurements.

The 63-parallel drivers pull up (pull down) the gate of the power device according to G_{PMOS} (G_{NMOS}) from the predrivers. The 63 parallel drivers are composed of laterally

diffused MOSs (LDMOSs) with drain-source breakdown voltage 20V and gate-source breakdown voltage 5V.

Fig. 2.10 shows operation waveforms for 63 PMOS transistors to pull up V_G in CGD IC. The operation for 63 NMOS transistors to pull down V_G is similar. An arbitrary I_G waveform is generated by applying a control bit pattern (B_{PMOS} (B_{NMOS})) in each clock cycle with 40-ns step and digitally specifying time and current pairs of t_i and I_{Gi} (i=1,2,3…n).

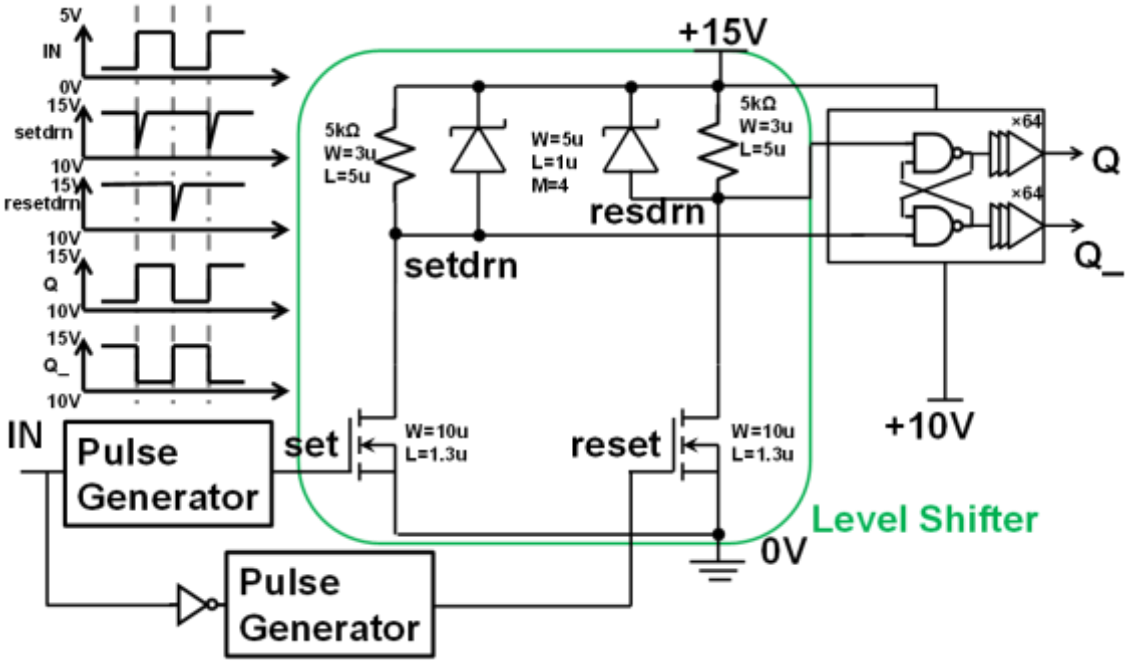


Fig. 2.6 Schematic diagram of level shifter and SR-latch buffer.

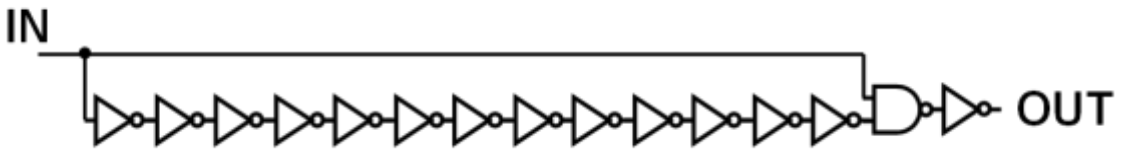


Fig. 2.7 Schematic of pulse generator.

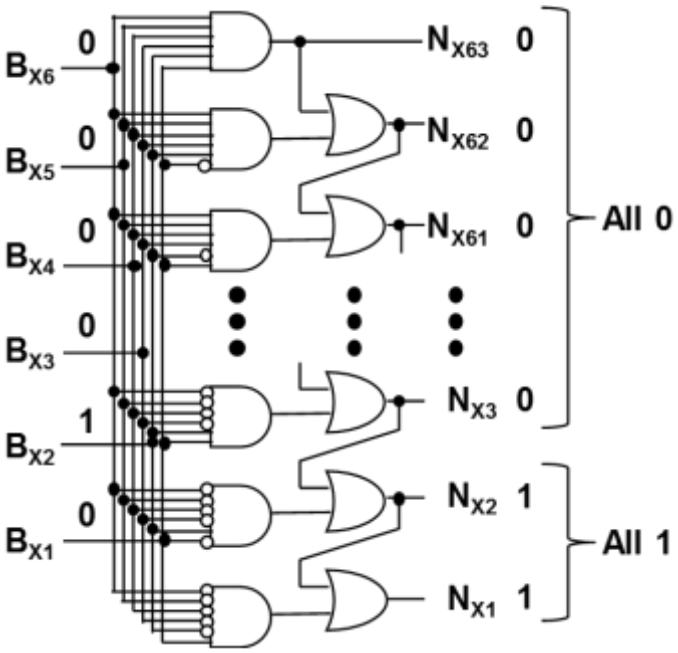


Fig. 2.8 Schematic of binary-to-thermometer code decoder.

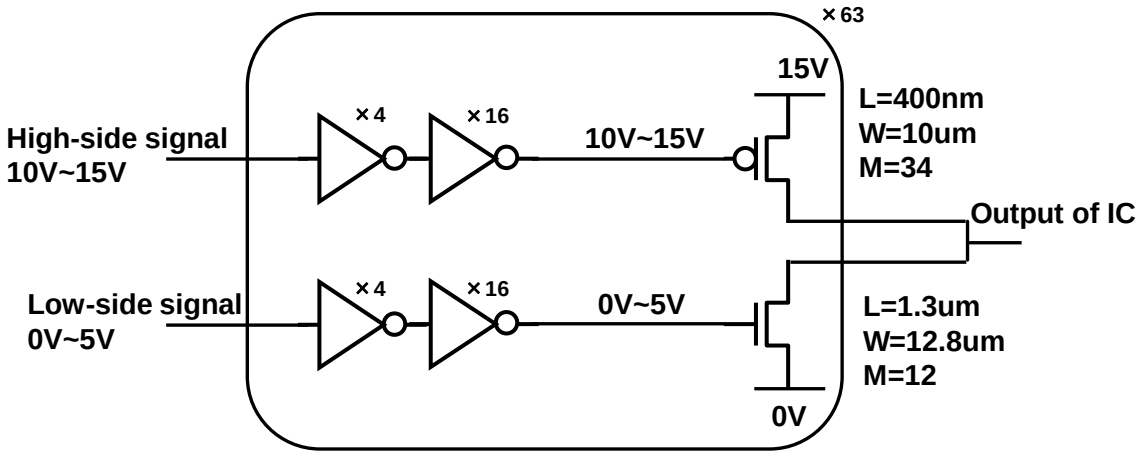


Fig. 2.9 schematics of predriver and output driver of CGD IC.

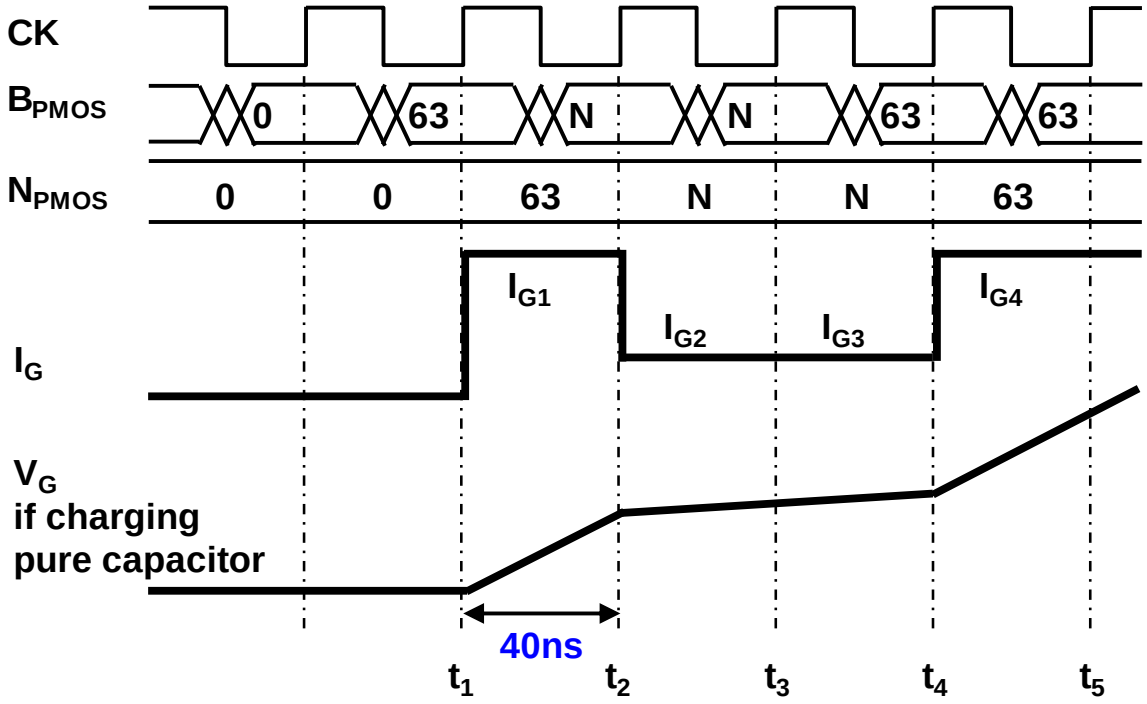


Fig. 2.10 Operation waveforms for 63 PMOS transistor pull up V_G in CGD.

2.3. Modeling of gate driver

In this chapter, the modeling of the 63 parallel drivers in Fig. 2.5 is discussed. In the previous the segmented gate drivers [2.10], the transistors in the segmented gate drivers (Fig. 2.11(a)) were modeled as a resistor (Fig. 2.11 (b)). In this paper, it is proposed that the transistors in the segmented gate drivers should be modeled as current-source (Fig. 2.11 (c)) instead of the resistor (Fig. 2.11 (b)). Fig. 2.12 shows the SPICE simulated pull-up and pulldown waveforms of V_G with two models in Fig. 2.11. The capacitance in Fig. 2.11 is 22nF emulating the gate capacitance of the power devices. V_{PD_PMOS} and V_{PD_NMOS} are 5V and 1.8V in Fig. 2.12 (a) and (b), respectively. Compared with the resistor model, the current-source model is in good agreement with the driver with transistors. Therefore, the gate driver behaves like the constant-current driver (Fig. 2.11 (c)) rather than the resistor (Fig. 2.11 (b)) because of the high output resistance of MOS transistors in a saturation region.

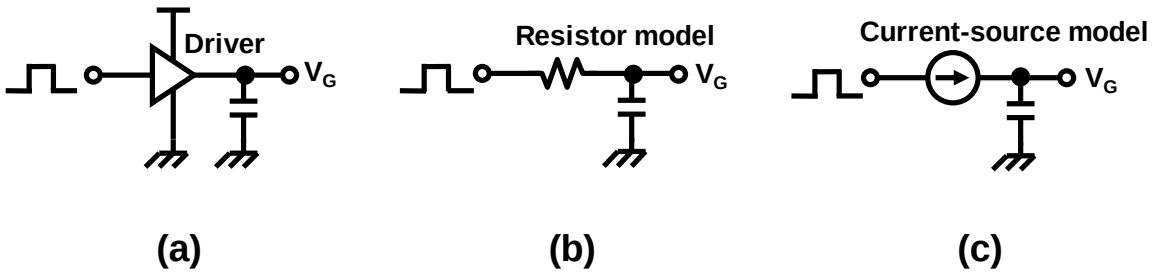


Fig. 2.11 Modeling of gate drivers (a) Original gate driver. (b) Conventional resistor model. (c) Proposed current-source model.

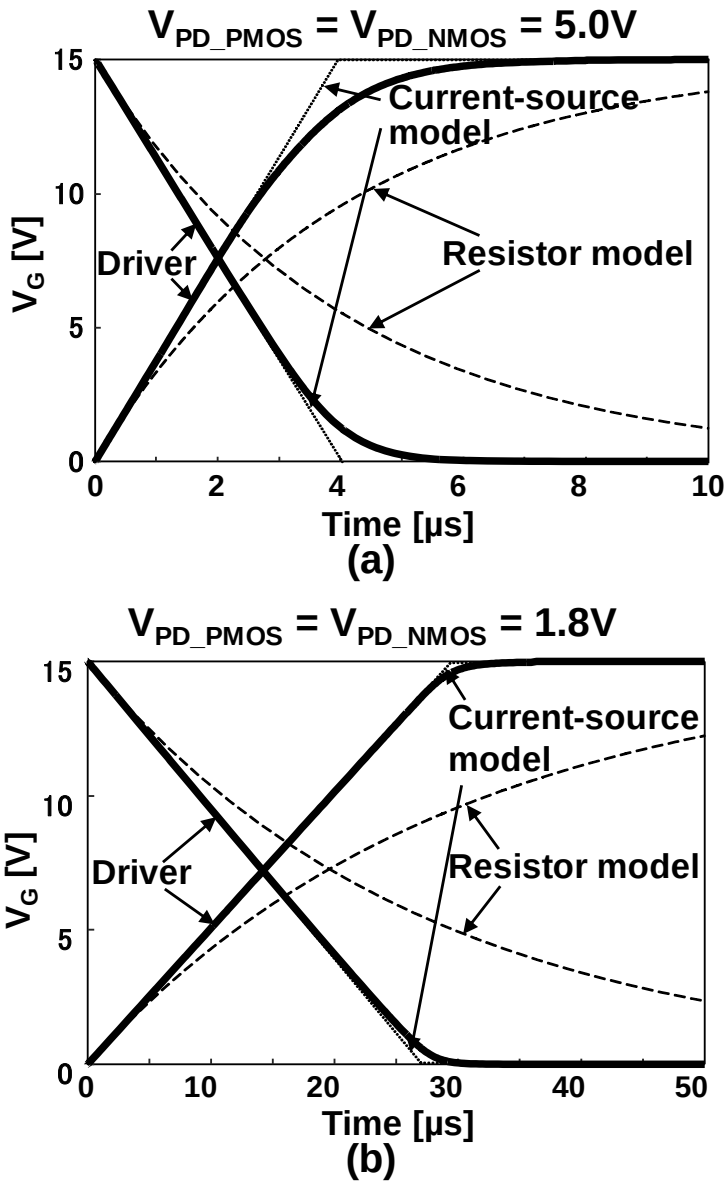


Fig. 2.12 SPICE simulated pull-up and pull down waveforms of V_G with two models in Fig. 2.11 (c). V_{PD_PMOS} and V_{PD_NMOS} are 5V and 1.8V in (a) and (b), respectively.

2.4. Measurement results

The proposed general-purpose CGD IC is fabricated with 0.18μm Bipolar-CMOS-DMOS (BCD) process. Fig. 2.13 shows a die photo of CGD IC. The core size is 2300μm by 730μm. The IC composed by NMOS drivers, PMOS drivers and driver output control blocks that consists of level shifters, DFFs array, binary-to-thermometer code decoders and predrivers. The number of pads is 16 at the output terminal, 6 at the VDD and VSS terminals. A balance between the area size of the NMOS drivers and PMOS drivers. It is because guard ring rules of the NMOS drivers. Fig. 2.14 shows photos of PCB. The 2.5-mm square CGD IC is placed on the top side of PCB. Si-IGBTs and SiC-diodes are placed on the reverse side of PCB.

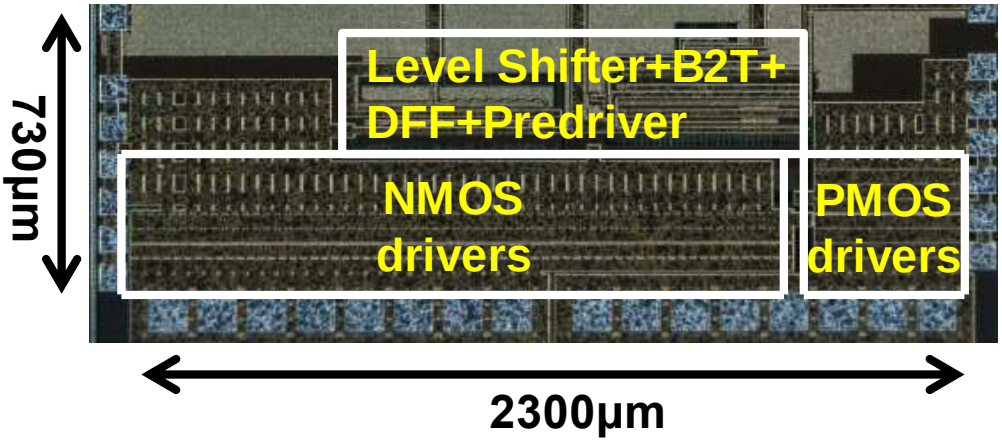


Fig. 2.13 Die photo of clocked gate driver IC.

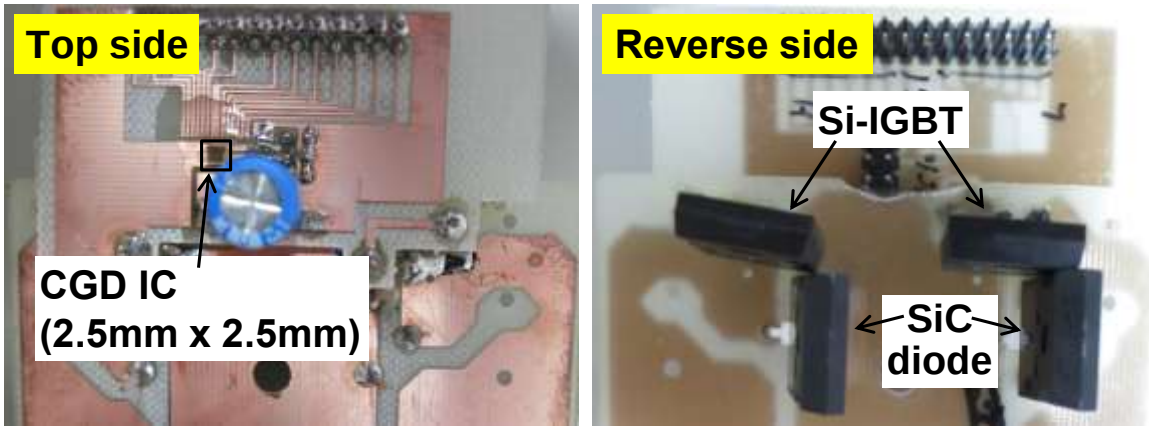


Fig. 2.14 Photo of PCB.

Turn-on characteristics are measured with a double-pulse setup shown in Fig. 2.5 with SiC-diodes (C4D10120D, 1200V, 18A) at V_{DC} = 500V. To demonstrate the versatility of the proposed general-purpose CGD IC, both Si-IGBT (IRG7PH46UPbF, 1200V, 75A) and SiC-MOSFET (SCH2080KE, 1200V, 40A) are driven by CGD IC. Although in Fig. 2.5, an IGBT symbol is used for a power device, the Si-IGBT is replaced by the SiC-MOSFET when the SiC-MOSFET is under test. Notations such as I_C and V_C are used even for the SiC-MOSFET device just for simplicity.

The double pulse test is measurement method to obtain turn-on / turn-off switching characteristics of power devices. Fig. 2.15 shows waveform diagram of the double pulse test in a chopper circuit composed of a power device, two freewheeling diodes and a load inductor. The double pulse test is performed by inputting two kind of switching pulse signals successively to the gate of the power device. The double pulse consists of a fist wide pulse signal and a second narrow pulse signal. During the first pulse, collector current I_C increases according to the load inductor of the chopper circuit. The duration of the first pulse determines the load current condition. At the end of the first pulse, the turn-off switching characteristics of the power device at I_C at this moment is obtained. In the interval between the first pulse and the second pulse, the increased current of I_C is stored in the load inductor.

At the start of the second pulse, the turn-on switching characteristics of the power device at the current stored in the load inductance is obtained. The double pulse test measures the turn-on / turn-off switching characteristics of power devices under the load current condition determined by the width of the first pulse.

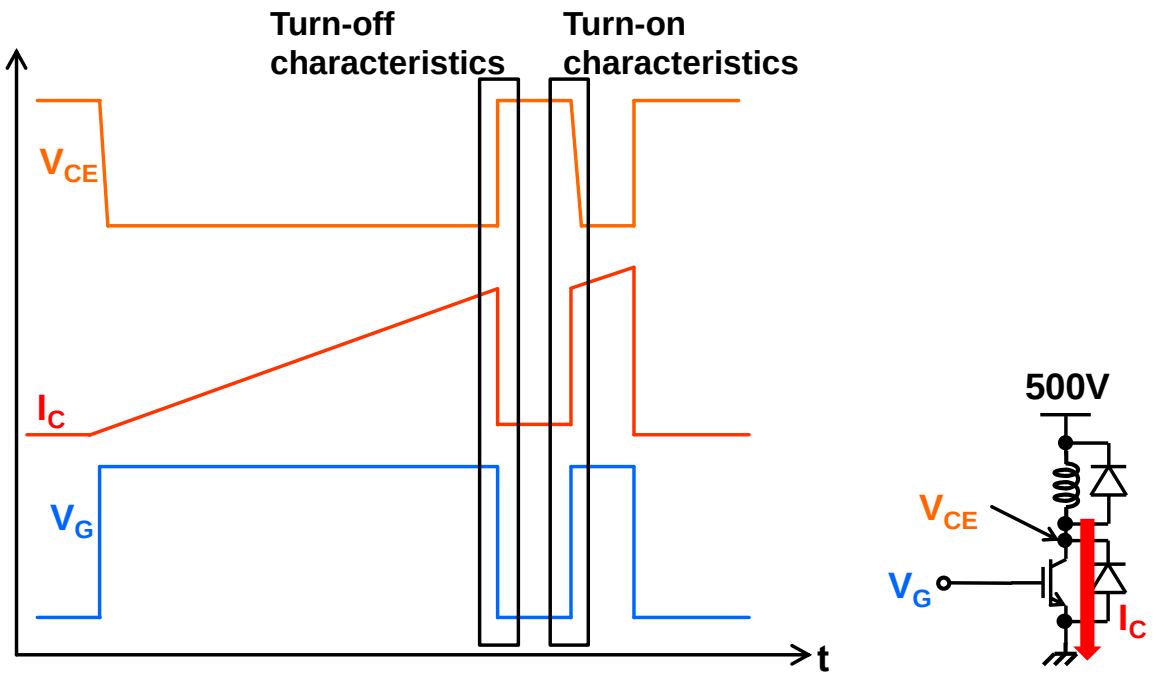


Fig. 2.15 Waveform diagram of the double pulse test in a chopper circuit.

To show the advantage of the proposed CGD IC with programmable 63-level drivability, three types of gate waveforms shown in Fig. 2.16 are compared. Fig. 2.16 (a) shows a conventional "non-active gate drive" [2.11]. To show the trade-off between the turn-on energy loss and the I_C overshoot, I_G to pull-up V_G is varied by N_{PMOS} in the measurement. Fig. 2.16 (b) shows a conventional "9-level active gate drive" emulating the 9-level segmented gate driver [2.10]. This waveform is based on [2.5, 2.7, 2.9-10, 2.12]. At the turn-on, N_{PMOS} changes from 0 to m and keeps m for t1. Then, N_{PMOS} changes from m to 9 level of i (i = 2 to 58 with 7 increments in between) and keeps i for t2. Finally, N_{PMOS}

changes from i to m. Fig. 2.16 (c) shows the proposed “63-level active gate drive”. Fig. 2.16 (c) is the same as Fig. 2.16 (b) except for i. In Fig. 2.16 (c), i is from 0 to 63 with 1 increment in between. Table 2-3 shows m, t_1, and t_2 in the measurements for the Si-IGBT and the SiC-MOSFET, respectively.

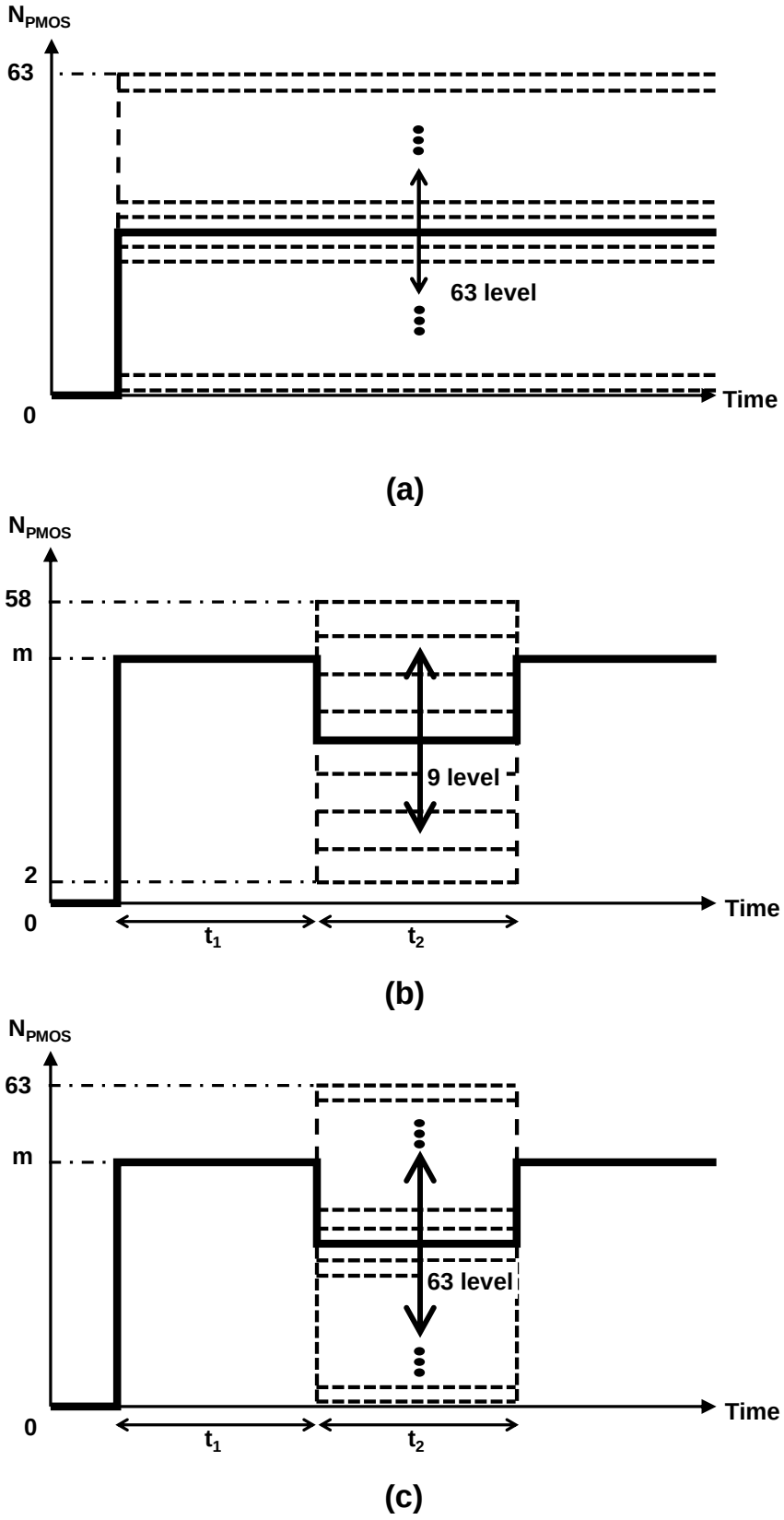


Fig. 2.16 Three types of turn-on gate waveforms. (a) No active gate drive. (b) 9-level active gate drive. (c) Proposed 63-level active gate drive.

Table 2-3 Parameters used in measurements for Si-IGBT and SiC-MOSFET.

	Si-IGBT	SiC-MOSFET
m	31	63
t_1	160ns	40ns
t_2	160ns	80ns

2.4.1. Si-IGBT

Fig. 2.17 shows measured energy loss versus I_C overshoot in turn-on characteristics at 500-V switching with the three gate waveforms shown in Fig. 2.16 for the Si-IGBT. In the non-active gate drive, the trade-off between the turn-on energy loss and the I_C overshoot is observed. By using 63-level active gate drive, however, the loss-overshoot trade-off can be optimized more compared with cases of 9-level active gate drive [2.10] and non-active gate drive. The proposed 63-level active gate drive reduces the measured energy loss at the same IC overshoot by 38% (Fig. 2.17) for the Si-IGBT. Similarly, the proposed 63-level active gate drive reduces the measured IC overshoot at the same energy loss by 25% (Fig. 2.17) for the Si-IGBT. The corresponding measured waveforms of N_{PMOS}, V_G, V_C, and I_C for the Si-IGBT is shown in Fig. 2.18. The 25% reduction of the I_C overshoot is clearly shown in Fig. 2.18.

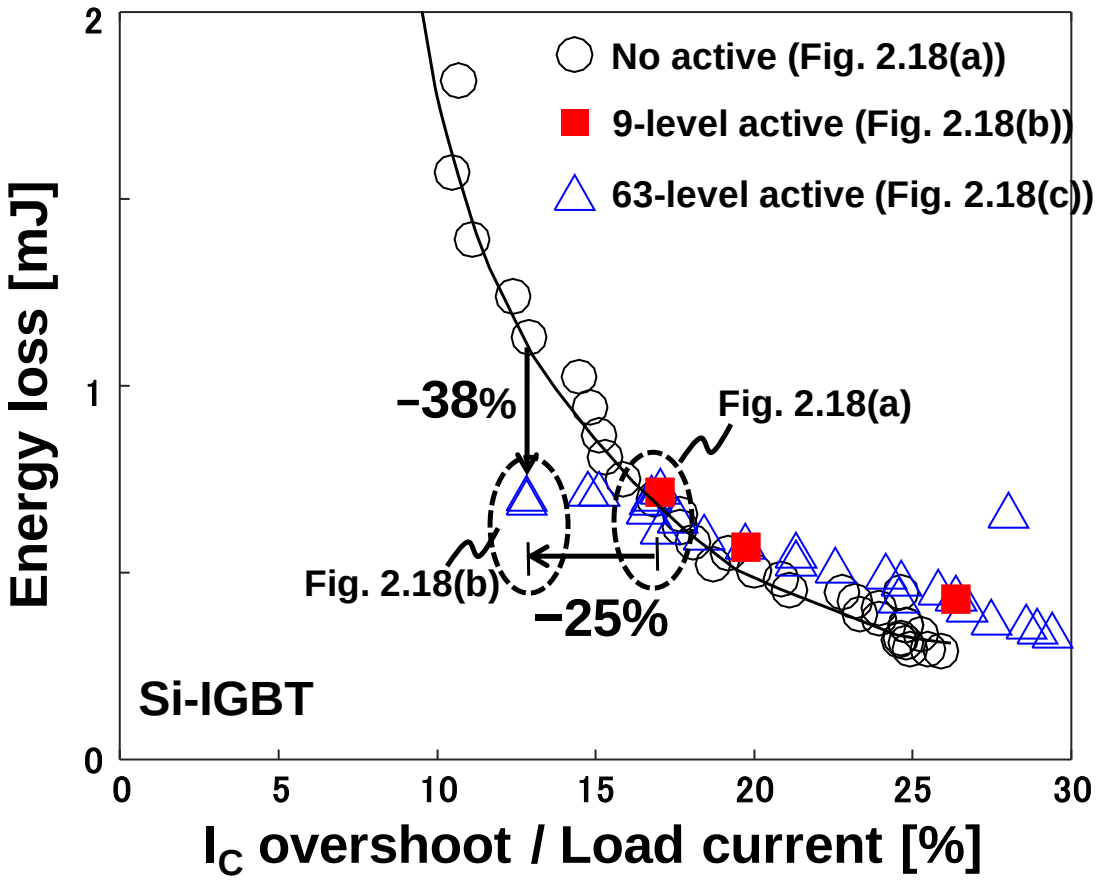


Fig. 2.17 Measured energy loss vs. IC overshoot in turn-on characteristics at 500-V switching for Si-IGBT.

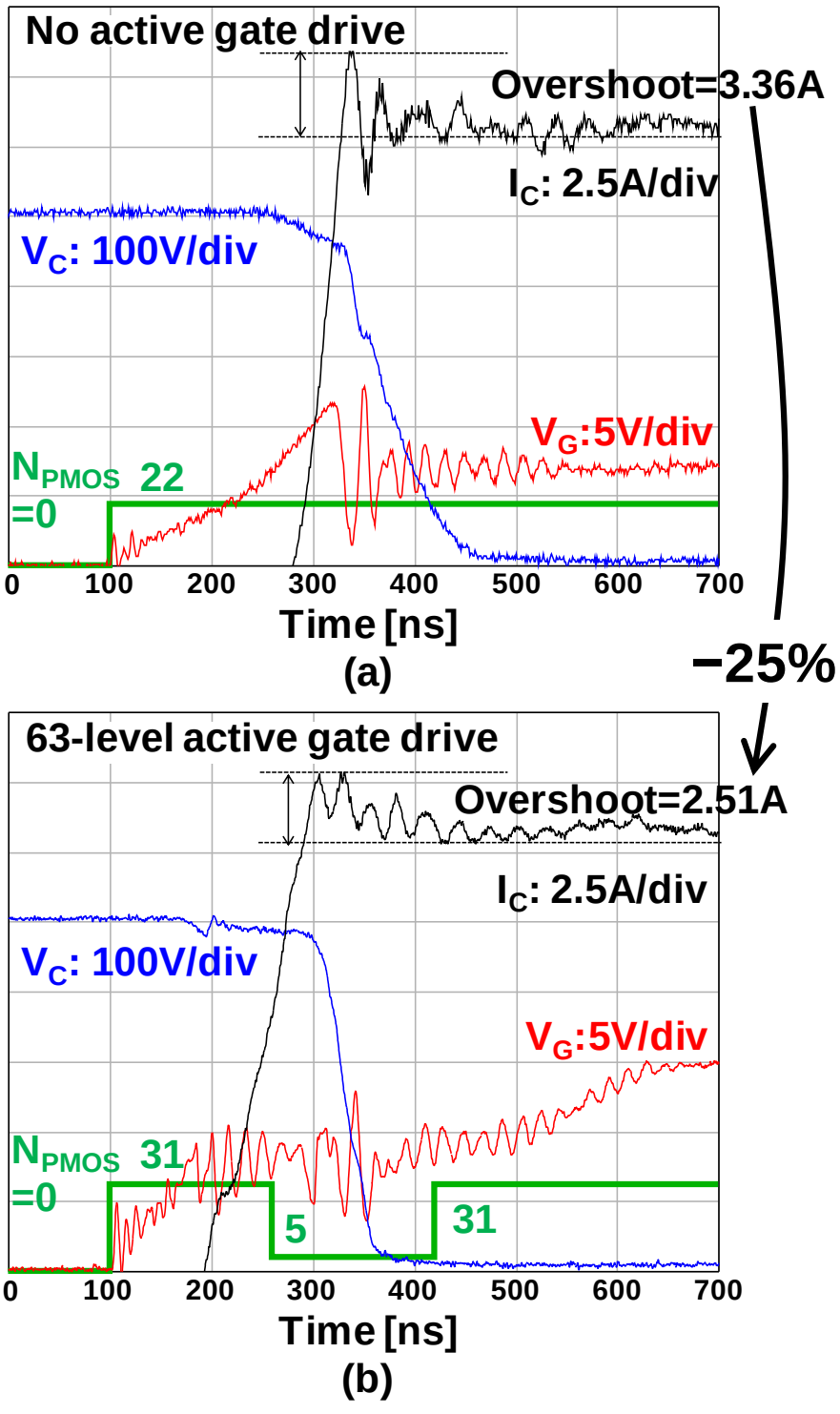


Fig. 2.18 Measured waveforms for Si-IGBT corresponding to Fig. 2.17. (a) No active gate drive. (b) Proposed 63-level active gate drive.

2.4.2. SiC-MOSFET

Fig. 2.19 shows measured energy loss versus I_C overshoot in turn-on characteristics at 500-V switching with the three gate waveforms shown in Fig. 2.16 the SiC-MOSFET. In the non-active gate drive, the tradeoff between the turn-on energy loss and the I_C overshoot is observed. By using the 63-level active gate drive, however, the loss-overshoot trade-off can be optimized more compared with cases of 9-level active gate drive [2.10] and non-active gate drive. The proposed 63-level active gate drive reduces the measured energy loss at the same I_C overshoot by 55% (Fig. 2.19) for the SiC-MOSFET. Similarly, the proposed 63-level active gate drive reduces the measured I_C overshoot at the same energy loss by 41% (Fig. 2.19) for the SiC-MOSFET. The corresponding measured waveforms of N_{PMOS}, V_G, V_C, and I_C for the SiC-MOSFET are shown in Fig. 2.20. The 41% reduction of the I_C overshoot are clearly shown in Fig. 2.20.

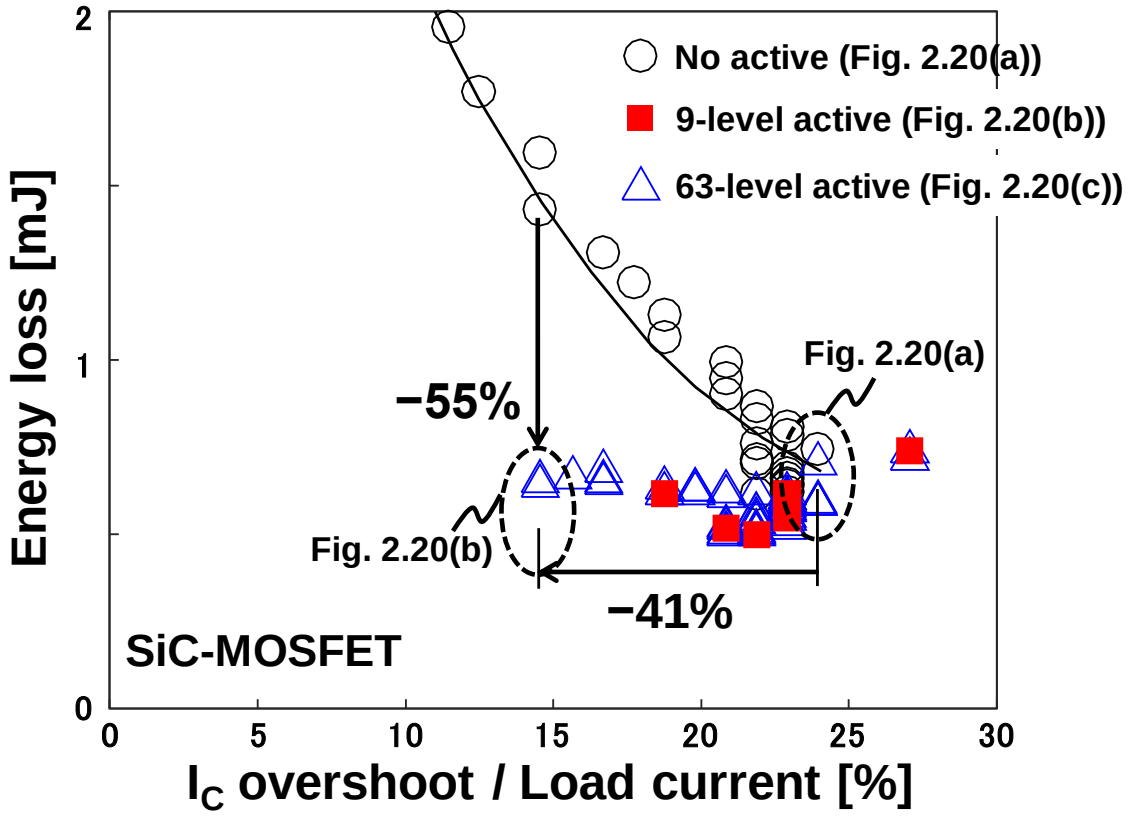


Fig. 2.19 Measured energy loss vs. IC overshoot in turn-on characteristics at 500-V switching for SiC-MOSFET.

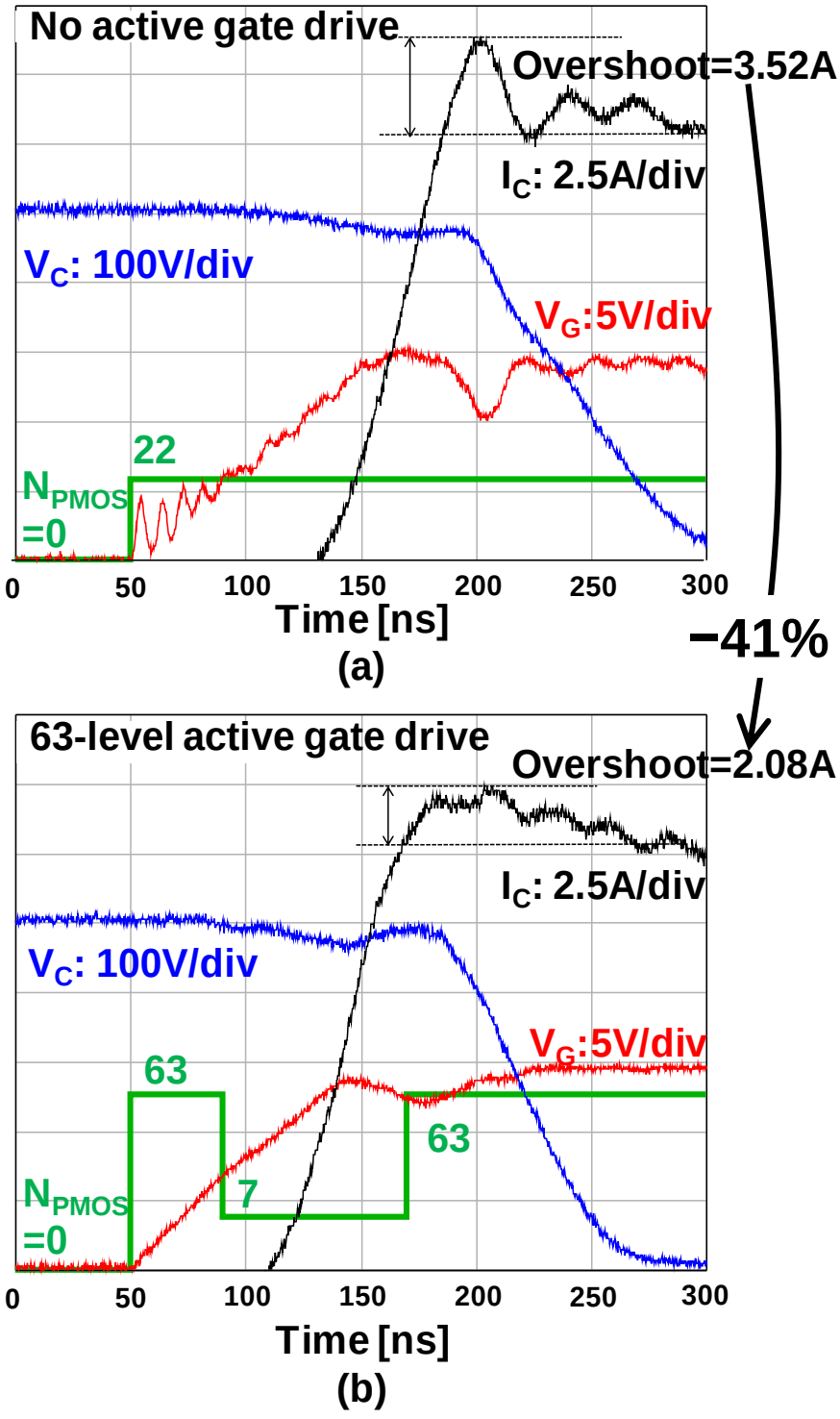


Fig. 2.20 Measured waveforms for SiC-MOSFET corresponding to Fig. 2.19. (a) No active gate drive. (b) Proposed 63-level active gate drive.

Table 2-4 Comparison with previous gate drivers.

	[2.1]	[2.2]	[2.6]	[2.10]	This work
Implementation	PCB	PCB	PCB	IC	IC
Target power device	Si-IGBT	Si-IGBT	SiC-MOSFET	Si-IGBT	Si-IGBT & SiC-MOSFET
Time programmability	NA	NA	NA	NA	40-ns step
Number of drivability levels	2	2	4	9	63
How to change drivability	R_G	R_G	Drive voltage	Driver size	B_{PMOS}, B_{NMOS} V_{PD_PMOS}, V_{PD_NMOS}
Gate current	NA	NA	NA	NA	3mA~5A

Table 2-4 shows a comparison of the proposed CGD IC with previous gate drivers. This work achieved the 40-ns step timing control and 63-level drivability, thereby enabling the gate waveform optimization for both the Si-IGBT and the SiC-MOSFET. The time programmability is achieved for the first time and the 63-level drivability is the largest number of the drivability levels.

2.5. Conclusion

The general-purpose CGD IC to generate an arbitrary gate waveform is the universal platform for fine-grained gate waveform optimization handling various power transistors. The 40-ns step timing programmability is achieved for the first time and the 63-level drivability is the largest number of the drivability levels in the previously published gate drivers. In the 500-V switching measurements, the proposed CGD reduces the IC overshoot by 25% and 41% and the energy loss by 38% and 55% for the Si-IGBT and the SiC-MOSFET, respectively.

2.6. References

[2.1] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," IEEE Trans. on Power Electronics, Vol. 29, No. 7, pp 3720-3732, Jul. 2014.

[2.2] M. Sasaki, H. Nishio, and W. T. Ng, "Dynamic gate resistance control for current balancing in parallel connected IGBTs," IEEE Applied Power Electronics Conf. and Expo., pp. 244-249, Mar. 2013.

[2.3] N. Teerawanich and M. Johnson, "Design optimization of quasi-active gate control for series-connected power devices," IEEE Trans. on Power Electronics, Vol. 29, No. 6, pp. 2705-2714, Jun. 2014.

[2.4] Y. Miki, M. Mukunori, T. Matsuyoshi, M. Tsukuda, and I. Omura, "High speed turn-on gate driving for 4.5kV IEGT without increase in PIN diode recovery current," IEEE Int. Symp. on Power Semiconductor Devices and ICs, pp. 347-350, May. 2013.

[2.5] V. John, B. S. Suh, and T. A. Lipo, "High-performance active gate drive for high-power IGBT's," IEEE Trans. on Industry Application, Vol. 35, No. 5, Sep. 1999.

[2.6] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration," IEEE Applied Power Electronics Conf and Expo., pp.774-781, Mar. 2015.

[2.7] Y. Lobsiger and J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT gate driver," IEEE Trans. on Power Electronics, Vol. 30, No. 6, pp. 3402-3417, Jun. 2015.

[2.8] Z. Dong, Z. Zhang, X. Ren, X. Ruan, and Y. F. Liu, "A gate drive circuit with mid-

level voltage for GaN transistor in 7-MHz isolated resonant converter," IEEE Applied Power Electronics Conf. and Expo., pp. 731-736, Mar. 2015.

[2.9] N. Idir, R. Bausière, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," IEEE Trans. on Power Electronics, Vol. 21, No. 4, Jul. 2006.

[2.10] A. Shorten, W. T. Ng, M. Sasaki, T. Kawashima, and H. Nishio, "A segmented gate driver IC for the reduction of IGBT collector current over-shoot at turn-on," IEEE Int. Symp. on Power Semiconductor Devices and ICs, pp. 73-76, Mar. 2013.

[2.11] S. Azzopardi, A. Kawamura, and H. Iwamoto, "Switching performances of 1200V conventional planar and trench punch-through IGBTs for clamped inductive load under extensve measurements," Int. Power Electronics and Motion Control Conf., Vol. 1, pp. 64-69, Aug. 2000.

[2.12] I. Baraia, J. A. Barrena, G. Abad, J. M. Canales, and U. Iraola, "An experimentally verified active gate control method for the series connection of IGBT/diodes," IEEE Trans. on Power Electronics, Vol. 27. No. 2, pp. 1025-1038, Feb. 2012.

Chapter 3

Automatic Optimization of IGBT Gate Driving Waveform

3.1. Introduction

Gate driving waveform optimization of power devices for improving the trade-off between switching loss and current or voltage overshoot has been attracting attention [3.1-9]. Recently for this purpose, a programmable gate driver IC has been developed [3.4], which enables to generate almost arbitrary waveforms for the gate voltage by changing the number of driving n-MOSFETs and p-MOSFETs at a certain time step. It can drive various power devices such as power MOSFETs, Si-IGBTs and SiC-MOSFETs. The optimization of the gate waveform, however, has to be conducted manually by human because of mismatch with IGBT simulation model due to variations and the parasitic components. Thus, finding satisfactory waveforms takes days of time and the search space is very limited.

Although the optimization strategies were presented in previous publications, the exact optimization depends on the board design, the systems design and the component parts, and thus quantitatively identifying the optimized waveform for a specific case still needs much effort. Moreover, as the freedom of the gate waveform control goes up, the optimization process is getting increasingly difficult. This chapter reports an automatic optimization of the gate waveform by dynamically combining real measurements and software optimization loop to cope with the inherently time-consuming and costly optimization process.

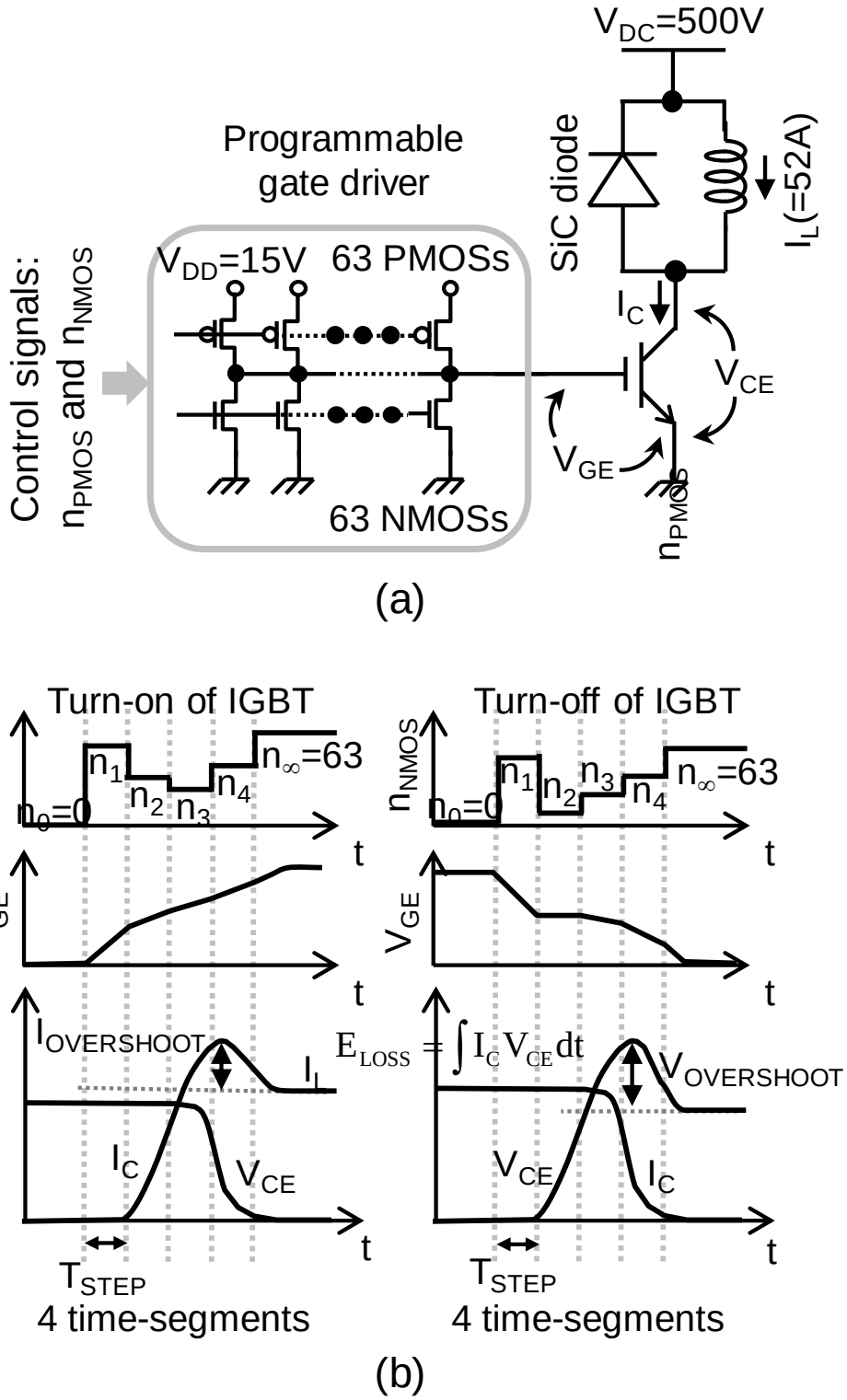


Fig. 3.1 (a) Circuit diagram and (b) waveform sketches used for IGBT gate driving waveform optimization.

3.2. Optimization method

This paper proposes the automation of the gate waveform optimization by using the simulated annealing (SA) algorithm [3.11] and a programmable gate driver IC [3.10]. The system setup used in this paper is shown in Fig. 3.1. Double pulse test circuits are built using Si-IGBT (IRG7PH46UPbF) and SiC-diode (C4D10120D) for 500-V and Si-IGBT module (2MBI100TA-060) including Si-diode for 300-V. Double pulse tests are performed with the load current of 52-A, which is driven +15V / 0V gate voltage levels by a programmable driver IC with 64-level current resolution of V_{PD_PMOS} / V_{PD_NMOS} 1.8 V (Fig. 2.12) and 40-ns minimum time step [3.10]. The actual time step, T_{STEP}, used for the IGBT turn-on case is 80-ns for both Si-IGBT and SiC diode and set and Si-IGBT and Si diode set. T_{STEP}, used for the IGBT turn-off case is 400-ns for the Si-IGBT and the SiC-diode set, and 160ns for the Si-IGBT and the Si-diode set. For both cases, the number of the time-segments is set to 4 in this paper as shown in Fig. 3.1. After these segments, all PMOS or NMOS are on-state in order to avoid malfunction by reducing the gate impedance.

The programmable gate driver IC accepts a sequence of n_{PMOS} (the number of on-state PMOSs) and a sequence of n_{NMOS} (the number of on-state NMOSs) as the control inputs and changes the output drivability accordingly. Any strength of drivability from 0 to 63 (x 12-mA for both of PMOS and NMOS) can be chosen for each of the 4 time-segments, that is, n_1, n_2, n_3, and n_4 in Fig. 3.1 can be any of integers from 0 to 63. Here, a set of the 4 integers [n_1, n_2, n_3, n_4] is called a waveform vector. Since the driver NMOS and PMOS are operated in a saturation region, an almost constant-current driving condition holds in driving the IGBT. Details of the gate driver IC are disclosed in Chapter 2.

In this waveform optimization process, 64^4 (~1.7×10^7) different waveforms need to be

tried for an exhaustive search, which is impractical. The machine-based optimization using the simulated annealing (SA) is proposed to make the optimization practical. The SA is a probabilistic method to find a global minimum of evaluation value from the object function avoiding being trapped at a local minimum. As an example, consider a case where there are local minima. Normally, a search point goes down to the lower potential greedy. However, the search point reaches the local minimum once, the search ends there in the greedy search. In order to avoid being trapped in the local minimum, in the SA, the search point go up the potential at a certain probability. In the gate driving waveform search, the SA is applied to avoid to being trapped local minima.

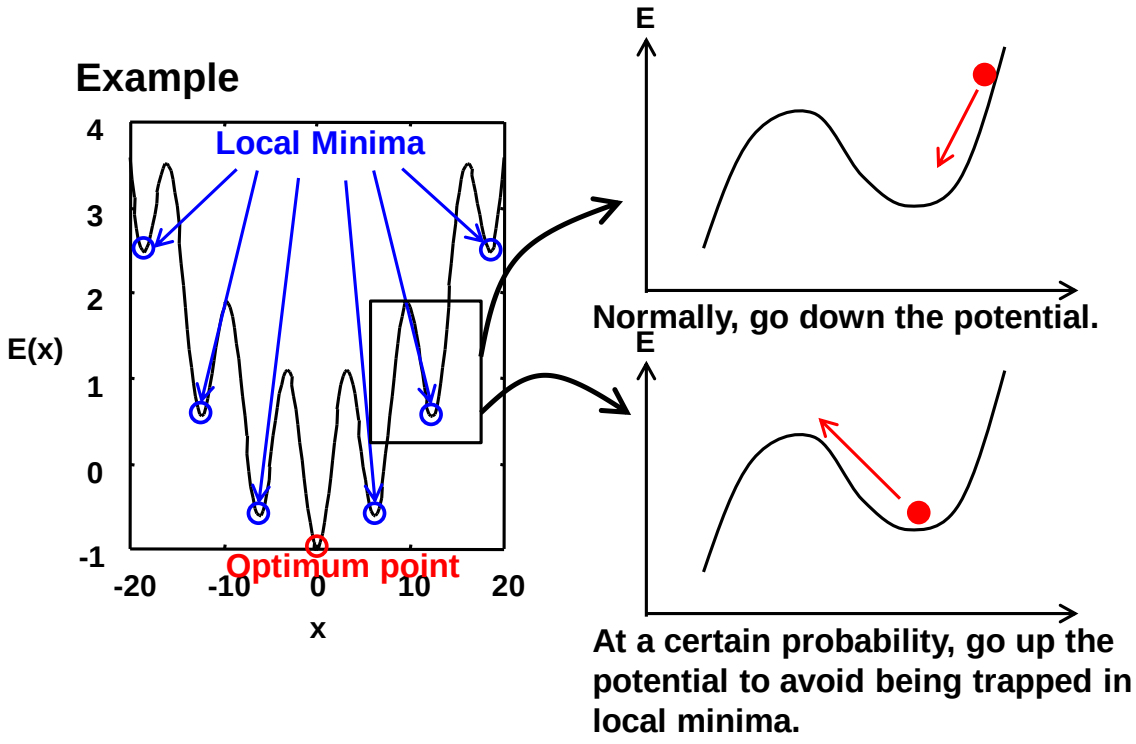


Fig. 3.2 Example of search space with local minima.

The objective of the gate driving waveform search is to improve the trade-off between the energy loss, E_{LOSS} (=), and the overshoot of I_C, $I_{OVERSHOOT}$, for the turn-on case (the

overshoot of V_{CE}, $V_{OVERSHOOT}$, for the turn-off case), whose definitions are shown graphically in Fig. 3.1. In order to achieve this goal, first, the energy loss and the overshoot values are normalized as below. The normalization helps to balance the energy loss optimization and the overshoot optimization.

$$E'_{LOSS} = \frac{E_{LOSS} - E_{LOSS,MIN}}{E_{LOSS,MAX} - E_{LOSS,MIN}}, \tag{3.1}$$

$$I'_{OVERSHOOT} = \frac{I_{OVERSHOOT} - I_{OVERSHOOT,MIN}}{I_{OVERSHOOT,MAX} - I_{OVERSHOOT,MIN}}, \tag{3.2}$$

$$V'_{OVERSHOOT} = \frac{V_{OVERSHOOT} - V_{OVERSHOOT,MIN}}{V_{OVERSHOOT,MAX} - V_{OVERSHOOT,MIN}}, \tag{3.3}$$

where ' signifies the normalized quantity and the subscript MIN (MAX) signifies the minimum (maximum) of the corresponding quantity. For example, $E_{LOSS,MIN}$ is the measured E_{LOSS} when the gate driving waveform is the fastest, that is, all of n1, n2, n3, n4, and n∞ are 63. On the other hand, $E_{LOSS,MIN}$ is the measured E_{LOSS} when the gate drive waveform is the slowest, that is, all of n1, n2, n3, n4, and n∞ are 1. Likewise, the other minimum (maximum) overshoot values are obtained either by the slowest or the fastest gate driving waveform. After the normalization, all of the normalized quantities vary between 0 and 1. The object function, f_{OBJECT} (Fig. 3.3), to be minimized is set as the Euclidean norm as below.

$$f_{OBJECT} = \sqrt{E'^{2}_{LOSS} + I'^{2}_{OVERSHOOT}} \tag{3.4}$$

for the IGBT turn-on case.

$$f_{OBJECT} = \sqrt{E'^{2}_{LOSS} + V'^{2}_{OVERSHOOT}} \tag{3.5}$$

for the IGBT turn-off case.

The reason for setting the object function in this manner is to ensure that the results do not fluctuate for each search trial attempt. Fig. 3.3 shows contour line of f_{OBJECT} and trade-off curve of single drivability. The trade-off curve is a downwardly convex graph. For the

trade-off curve that is a downwardly convex graph, by setting f_{OBJECT} that draws a contour line convex upward, the search point converges to one place. Depending on the application, setting various object functions such as overshoot priority or loss priority may be considered.

The total system setup is shown in Fig. 3.4. A pseudo-code of the SA algorithm is shown in the figure. The algorithm is implemented on a PC using MATLAB and generates a new trial waveform vector, $X_{TRIAL}=[n_1, n_2, n_3, n_4]$. Using this X_{TRIAL} vector as an input, LabVIEW generates control signals to the programmable gate driver. Then the device under test feeds back the measured voltage and current waveform data to the PC through an oscilloscope. Using the measured waveform data, PC calculates the object function, f_{OBJECT} based on the above-mentioned expressions. Depending on f_{OBJECT}, the PC generates the next trial waveform, X_{TRIAL}, according to the SA algorithm. The optimization itereation loop continues until no decrease in f_{OBJECT} is observed for a certain period. Other greedy algorithms were tried but stuck at sub-optimal points while the SA always finds much better optimal points.

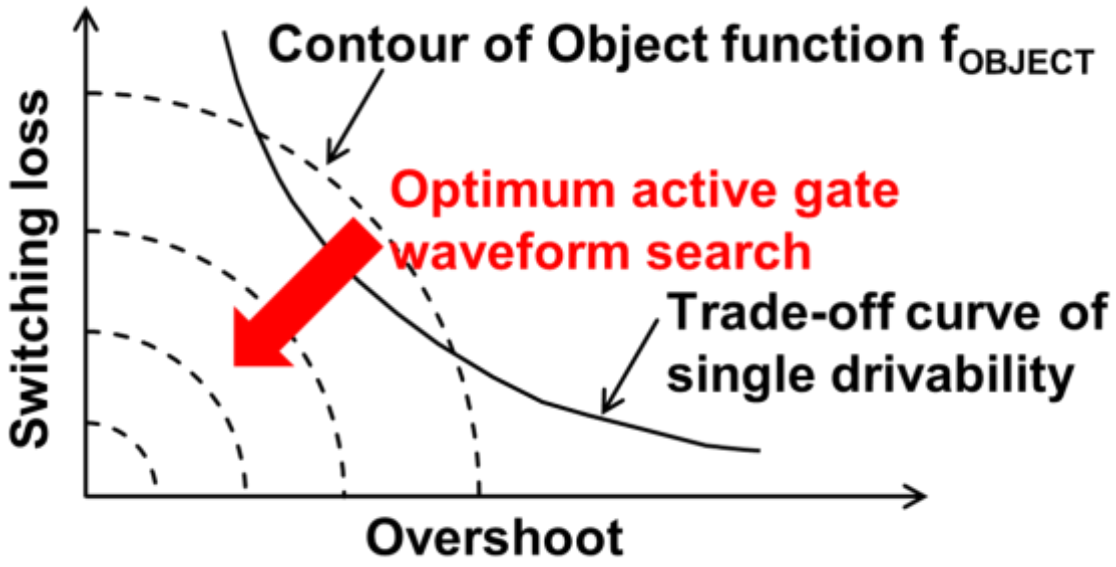


Fig. 3.3 Contour line of f_{OBJCT} and trade-off curve of single drivability.

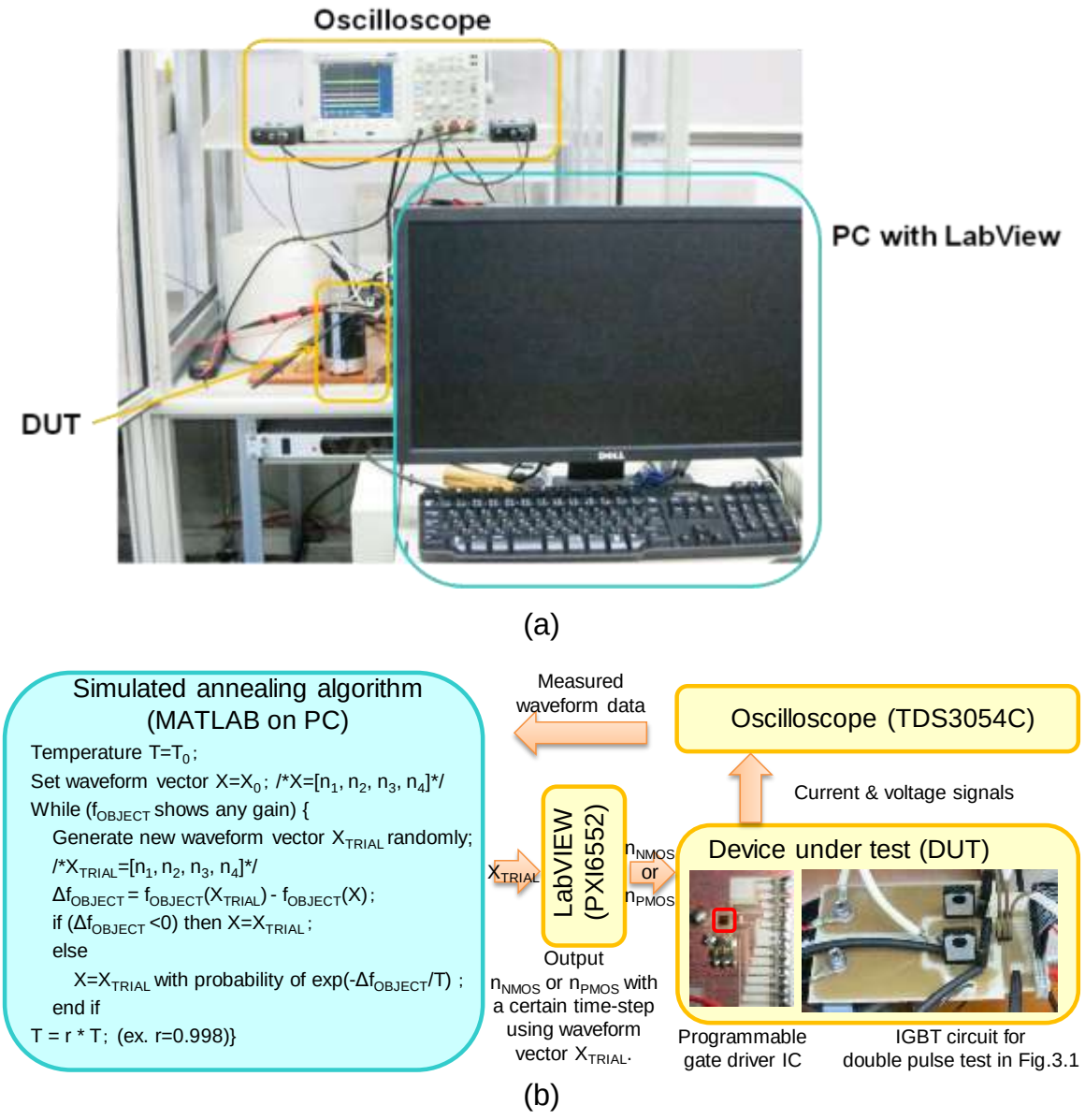


Fig. 3.4 (a) Photo of system setup. (b) System setup for automatic optimization with Si-IGBT and SiC-diode (yellow part is hardware and blue part is software).

3.3. Embodiments

An optimum gate driving waveform searched by the SA is only for the specific operating condition. The operating condition, such as temperature T of power devices and current I_C handled by power devices, of the power conversion circuit change under actual use environment. To cope with the change of the operating conditions, it is necessary to select an optimum gate driving waveform from a look-up table for current operating condition. Fig. 3.5 shows example of the look-up table of optimum gate driving waveforms for each operating condition of a power device having a threshold voltage $V_{G,TH}$. From I_C and T acquired by sensors in the power conversion circuit, the optimum gate driving waveform in the look-up table is selected and drives the power device so as to improve the switching characteristics.

The optimum gate driving waveform also changes with the threshold voltage V_T. a variation of $V_{G,TH}$ is a main factor of device characteristic variation. So, the look-up table for operating conditions is required for each V_T. Fig. 3.6 shows a set of look-up tables for threshold voltage variation. Selecting the look-up table according to V_T of power device from the set, it is possible to keep the optimum driving waveform for different operating conditions and different $V_{G,TH}$.

The automatic optimization of a gate driving waveform for making data table is done before factory shipment. Because of automatic optimization tries randomly generated waveform, sometimes switching operation with poor characteristics is performed. The poor characteristics may result in accident due to malfunction or device stress in an actual use environment. In considering of safety, the configuration of the look-up table is done before the factory shipment.

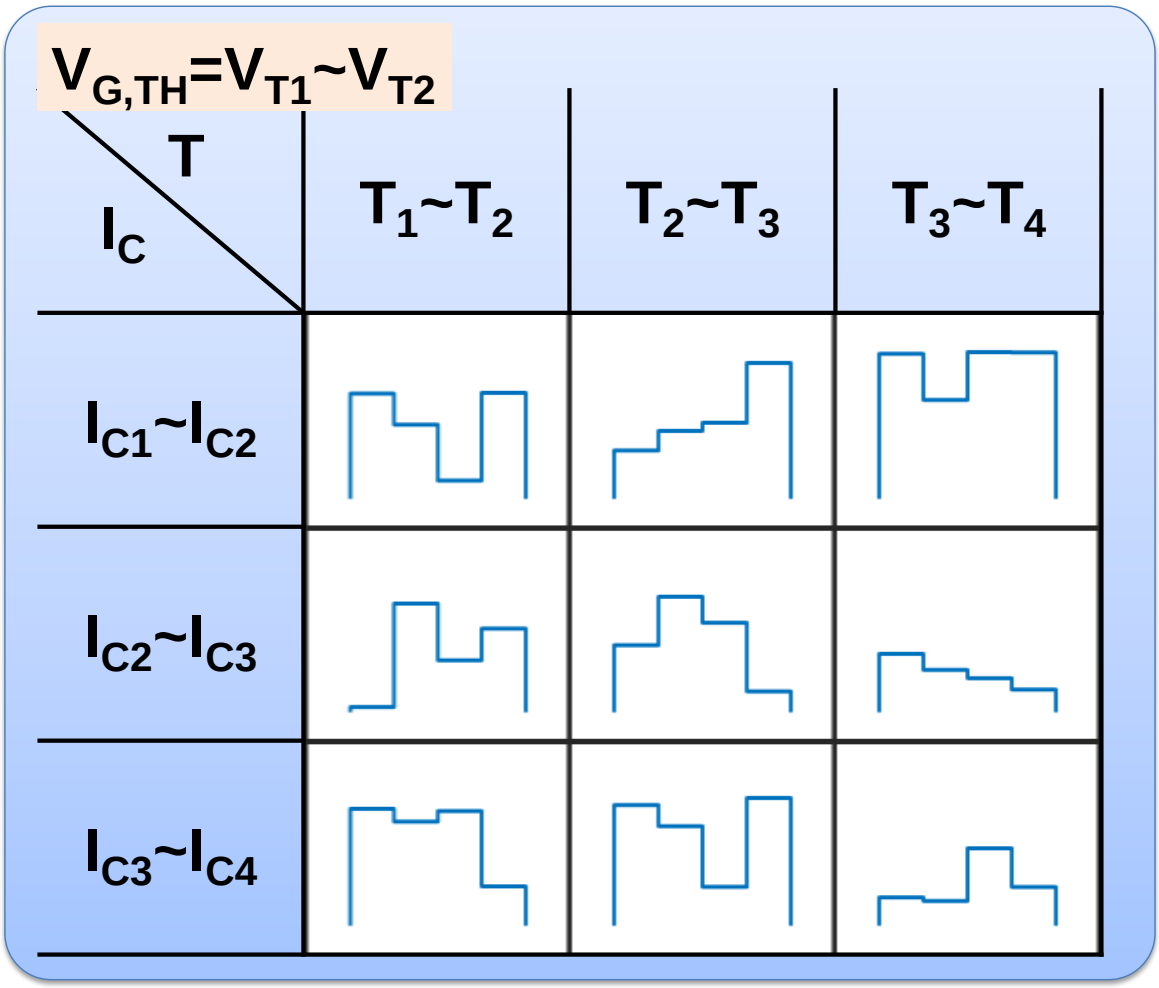


Fig. 3.5 Example of a look-up table of optimum gate driving waveform for each operating condition in a certain V_T.

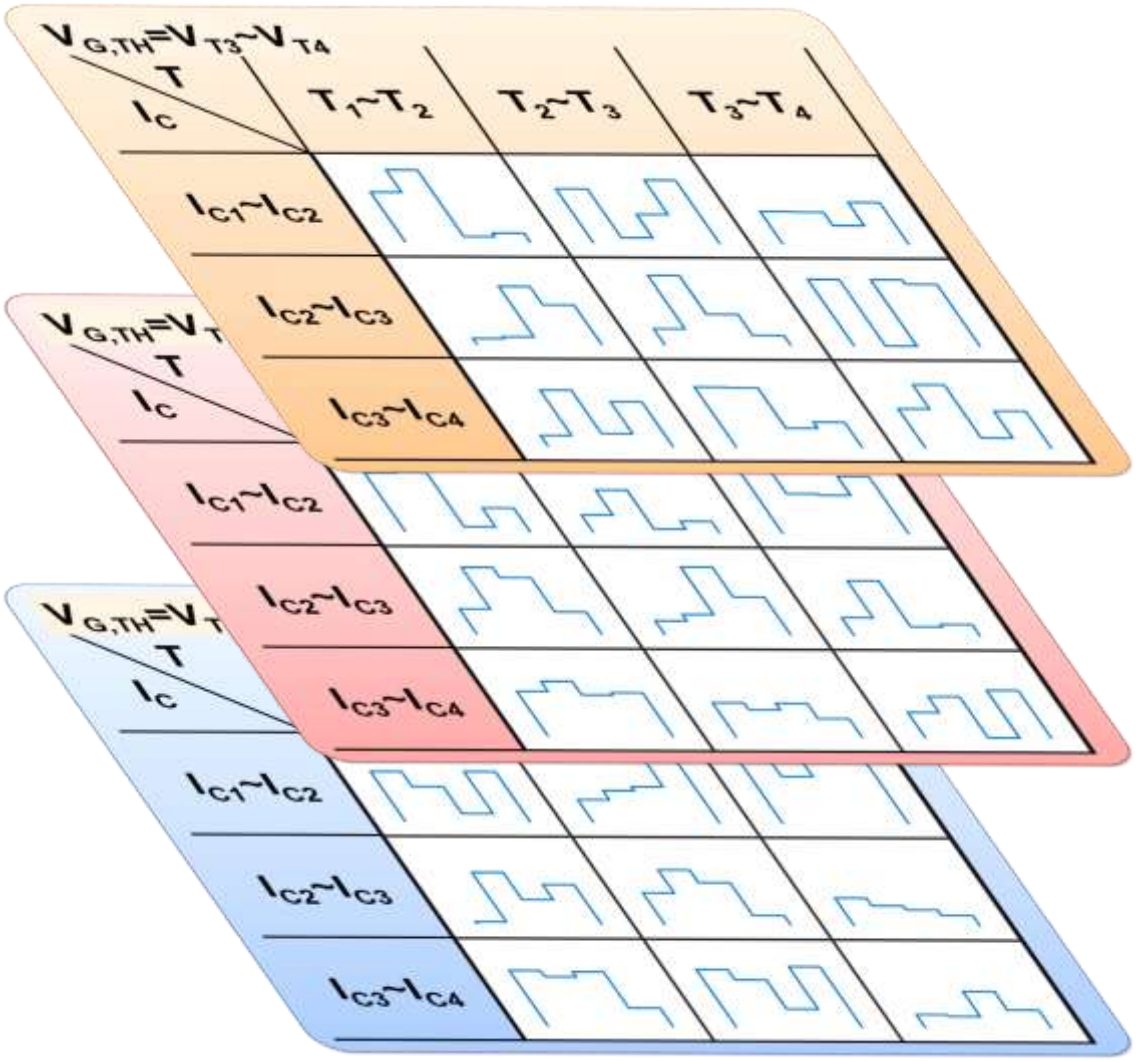


Fig. 3.6 A set of look-up tables.

3.4. Robust optimization

Automatic optimization needs to perform an optimum gate driving waveform with robustness. As described in Section 3.3, the proposed optimization method is assumed to be applied using the lookup table. Therefore, within a range of a selected one square in the table, an optimum gate driving waveform should be robust. The optimum gate driving waveforms searched by the method described Section 3.2 are peaking points and the characteristics deteriorate greatly due to the influence of the variation. So, it is necessary to search the robust optimum point.

To search for the robust optimum gate driving waveform, emulate change in operating condition and $V_{G,TH}$. The operating condition is determined by temperature and a load current. In the case of driving the gate of a power device with an optimum gate driving waveform of a rough shape shown in Fig. 2.4, it is the problem that the timing of decreasing the drivability changes due to the change in the operating condition. In the turn-on case, by reducing the drivability at the timing when I_C reaches I_L, the current overshoot is reduced while suppressing the increase in the switching loss. The time t_p from the start of the gate drive to the time when I_C reaches I_L is expressed by a following equation from Eqs. (1.1) (1.9),

$$t_p = (V_{G,TH} + \frac{I_L}{g_m})\frac{C_{GE}}{I_G}. \tag{3.6}$$

Here, g_m is a coefficient depending on power device temperature. $V_{G,TH}$ varies depending on power device variations. I_L and temperature vary with operating conditions of the power device. When t_p deviates due to the variations in these three parameters, the gate of the power device is strongly driven at the timing when the overshoot occurs, and overshoot

increases. According to Eq. (3.6), the variations in these three parameters is emulated by I_G.

3.5. Measurement results

3.5.1. Results for turn-on of IGBT and SiC-diode

The automatic optimization setup is applied to the turn-on case of the IGBT and the SiC-diode. In this case, a waveform vector [n_1, n_2, n_3, n_4] signifies the number of on-state driver PMOSs, n_{PMOS}, at a given time-segment. The initial waveform vector is set as [63, 63, 63, 63], that is, the fastest single-step turn-on case. Fig. 3.7 shows the history plots of $I_{OVERSHOOT}$, E_{LOSS} and f_{OBJECT} during the optimization process. The optimization process stops after 2420 iterations in this case. One iteration takes 2.2 seconds including the measurement time and the data transfer time to and from the PC. Thus, the total optimization takes 5324-s which is about one and a half hour. Multiple of the optimization processes were tried and all the trials finished within two hours.

The object function, f_{OBJECT}, is successfully minimized from 0.56 to 0.12 in this case. Just for information, a simple greedy optimization method where each of n_1, n_2, n_3, and n_4 is changed by either -1, 0 or 1 and the waveform vector which lowers f_{OBJECT} is searched, the optimization process is stuck at the initial point and never gives any better point. Thus, the optimization methods that can have the ability to get out from the local minima such as the SA is needed. No destructive breakdown of power devices was observed in the optimization process. The proposed method is demonstrated to be effective for an IGBT gate waveform optimization.

Fig. 3.8 shows the measured waveforms at the initial point and the end point of the

optimization iterations shown in Fig. 3.7. At the start, the waveform vector is a simple single-step function and shows the higher I_C overshoot. The improved gate driving waveform turns out to drive relatively strongly at first and then, reduce the drivability just before V_{GE} reaches the threshold voltage of the IGBT, and gradually increase the drivability afterwards. This qualitative description of the optimized waveform is consistent with the previous publications [3.1-3] but the advantage of the proposed method is to provide the quantitative values of parameters.

More than ten optimization trials using SA are carried out and all the trials successfully found the optimized waveform vector, that is, the optimized gate driving waveform. Three examples of optimized waveform vectors are shown in Fig. 3.9. E_{LOSS} and $I_{OVERSHOOT}$ are in a trade-off situation. When E_{LOSS} is low with a fast gate drive, the current overshoot is large but when the current overshoot is decreased by the slower gate drive, the energy loss increases. Thus, in Fig. 3.9, the trade-off is also shown. With a simple single-step gate drive, the trade-off is confined on the blue line even the drivability step height is changed. With the more sophisticated gate drive using the programmable gate driver IC, the achievable trade-off space is enlarged and 40% energy loss reduction and 36% current overshoot reduction are attained compared with the single-step gate drive.

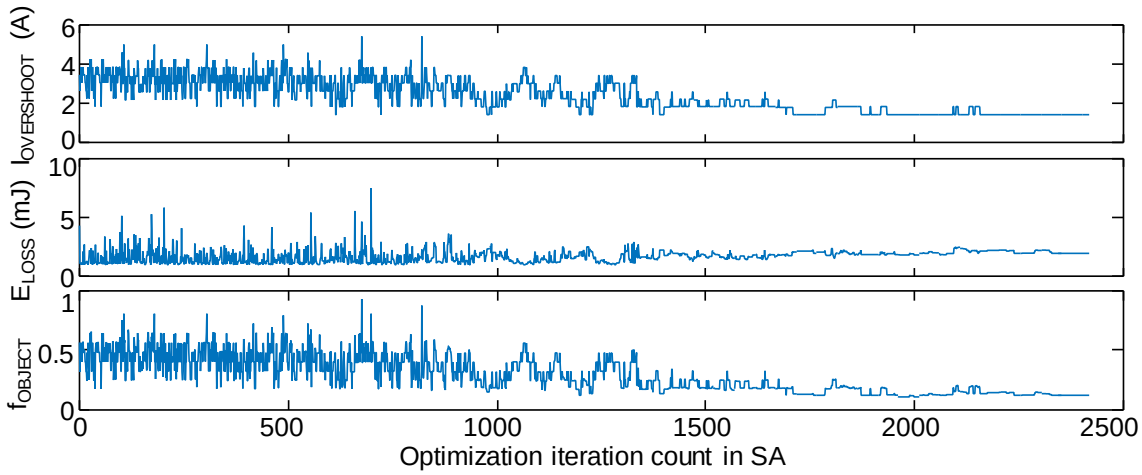
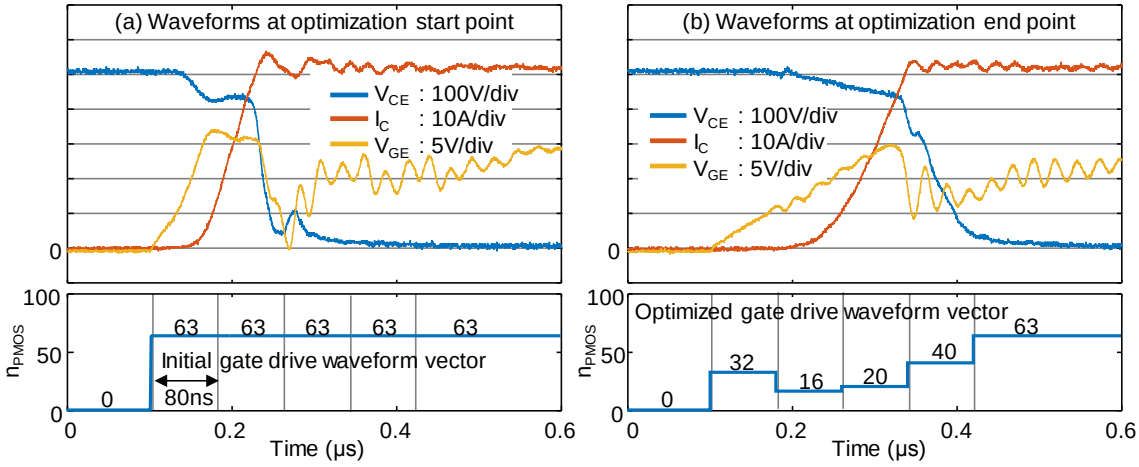


Fig. 3.7 History plots of $I_{OVERSHOOT}$, E_{LOSS} and f_{OBJECT} during optimization process for

turn-on.



(a) (b)

Fig. 3.8 Measured waveforms at (a) start point and (b) end point of SA optimization for Si-IGBT and SiC-diode turn-on case.

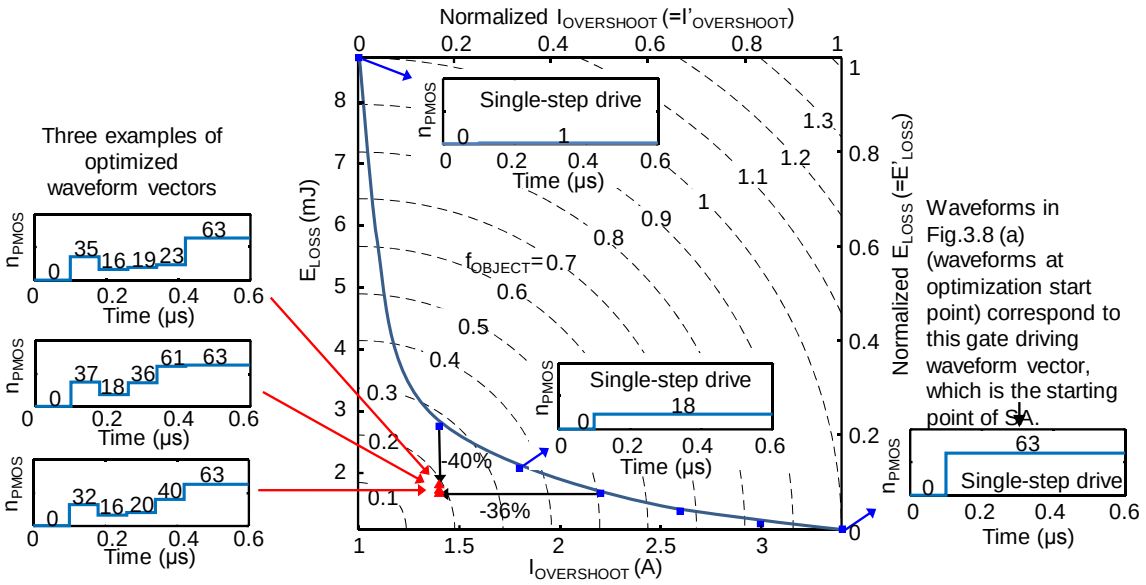


Fig. 3.9 E_{LOSS} - $I_{OVERSHOOT}$ trade-off Si-IGBT and SiC-diode. Broken lines are equi-f_{OBJECT} contour. Red triangles are optimized point.

3.5.2. Results for turn-off of IGBT and SiC-diode

As for the IGBT turn-off case, the optimization procedure is basically the same as the turn-on case. In this case, though, a waveform vector [n_1, n_2, n_3, n_4] signifies the number of on-state driver NMOSs, n_{NMOS}, at a given time-segment. Fig. 3.10 shows the history plots of $I_{OVERSHOOT}$, E_{LOSS} and f_{OBJECT} during the optimization process. The optimization process stops after 3272 iterations in this case. Fig. 3.11 shows the measured waveforms at the initial point and the end point of the optimization process. The optimized gate driving waveform turns out to drive relatively strongly at first and then, reduce the drivability just before V_{GE} reaches the threshold voltage of the IGBT, and gradually increase the drivability afterwards. This reduces the sharp voltage overshoot. The qualitative strategy for the optimized waveform is consistent with the previous publications [3.1, 3.3] but the advantage of the proposed method is to be able to find the quantitative values of parameters in a practical time.

Three examples of optimized waveform vectors are shown in Fig. 3.12. It is seen that the three points are not exactly the same in the waveform vectors because of the stochastic nature of the SA optimization process. Still, all the optimized waveform shows considerable reduction in the object function and all have the characteristics that the drivability is lowered in the middle of the driving process. In Fig. 3.12, the trade-off between the energy loss, E_{LOSS}, and the voltage overshoot, $V_{OVERSHOOT}$, is also shown. With a simple single-step gate drive, the trade-off is confined on the blue line even the drivability step height is changed. With the more sophisticated gate drive using the programmable gate driver IC and four time-segmented drive, the achievable trade-off space is enlarged and 59% energy loss decrease and 57% voltage overshoot reduction are achieved compared with the single-step gate drive.

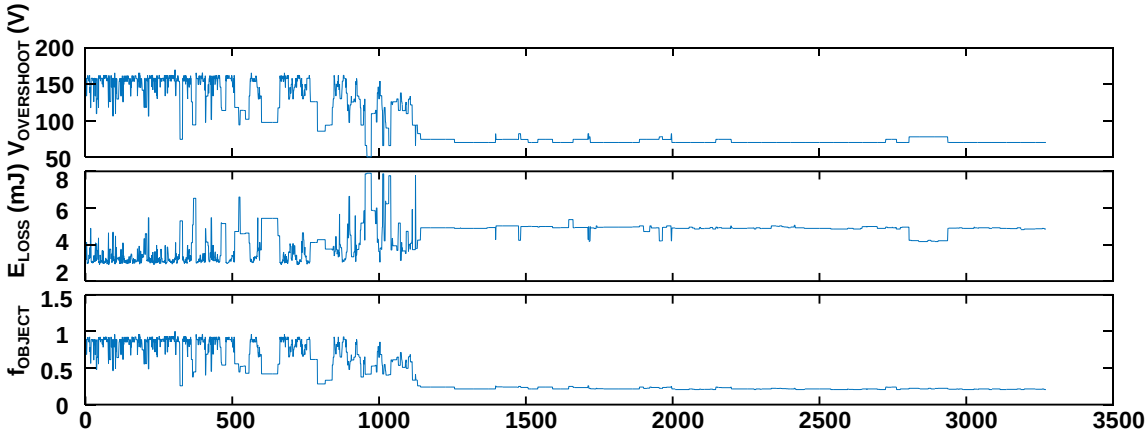
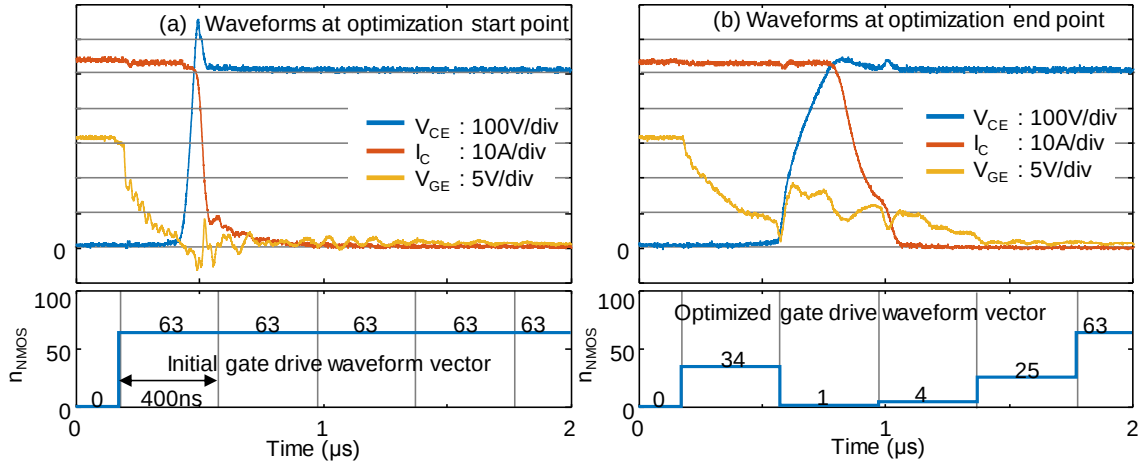


Fig. 3.10 History plots of $V_{OVERSHOOT}$, E_{LOSS} and f_{OBJECT} during optimization process for turn-off.



(a) (b)

Fig. 3.11 Measured waveforms at (a) start point and (b) end point of SA optimization for Si-IGBT and SiC-diode turn-off case.

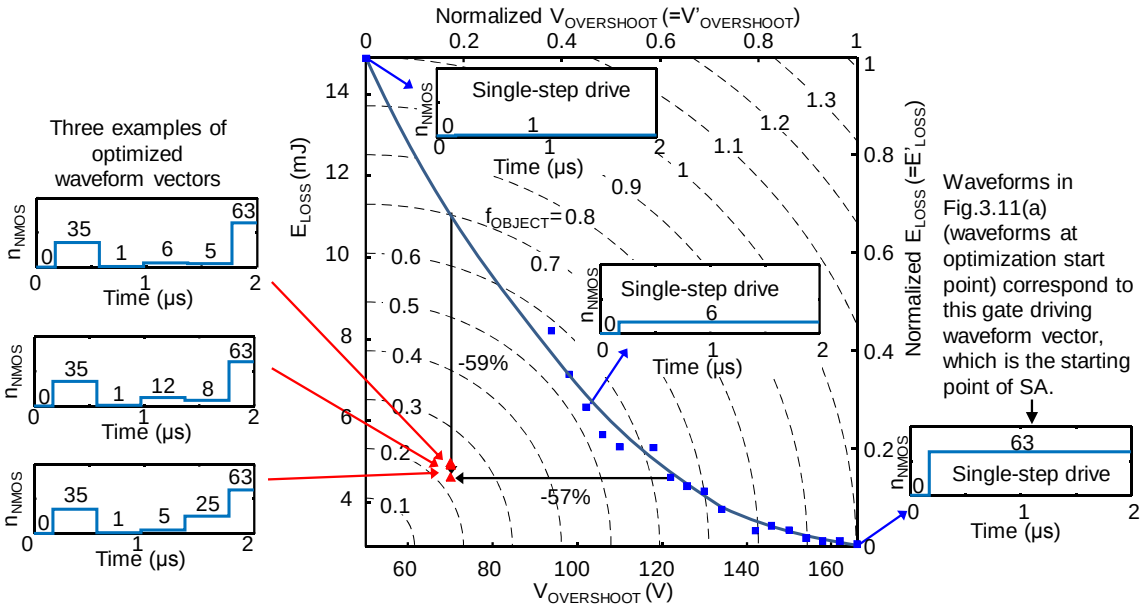


Fig. 3.12 E_{LOSS} - $V_{OVERSHOOT}$ trade-off Si-IGBT and SiC-diode. Broken lines are equi-f_{OBJECT} contour. Red triangles are optimized point.

3.5.3. Results for turn-on of IGBT and Si-diode

The automatic optimization setup is applied to the turn-on case of the Si-IGBT and the Si-diode. As for the Si-IGBT and Si-diode case, the optimization procedure is basically the same as the Si-IGBT and Si-diode case with 300V, 52A as show in Fig. 3.13. Fig. 3.14 shows the measured waveforms at the end point of the optimization process and single-step drive point at the same loss. The optimized gate driving waveform turns out to drive relatively strongly at first and then, reduce the drivability just before V_{GE} reaches the threshold voltage of the IGBT, and gradually increase the drivability afterwards. This reduces the sharp current overshoot.

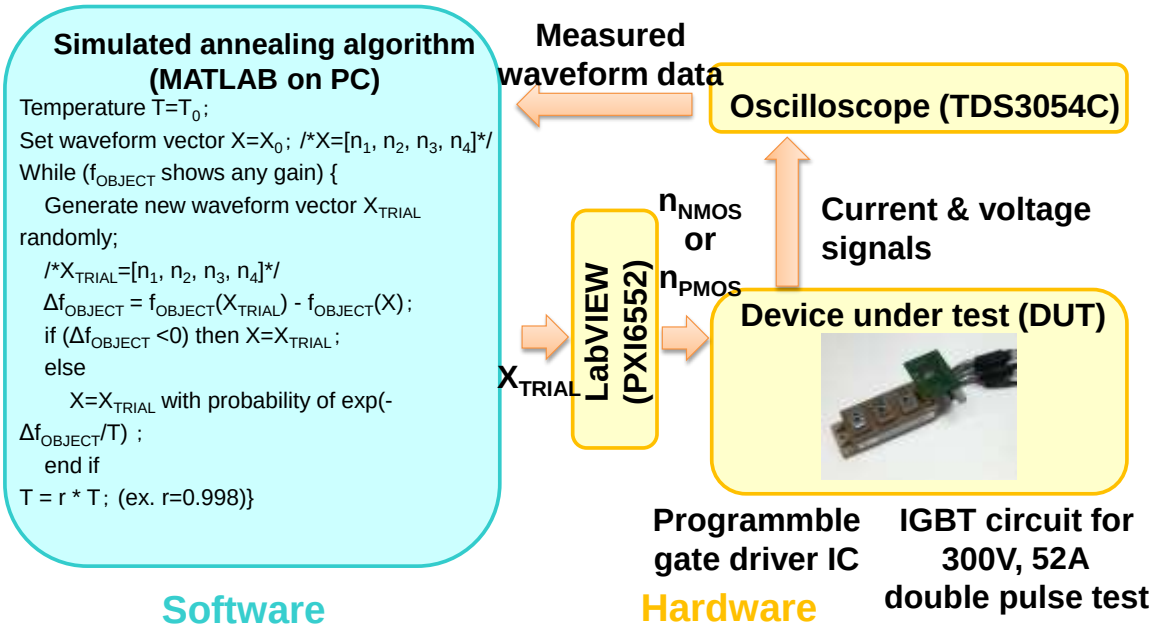
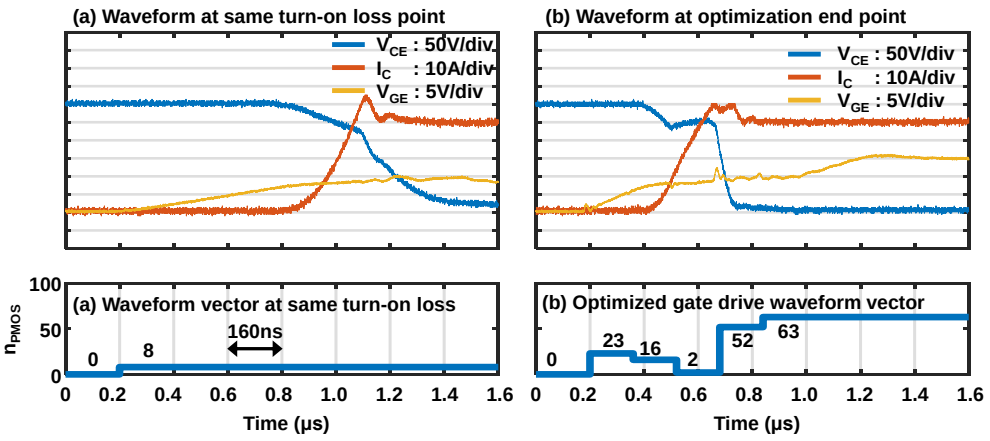


Fig. 3.13 System setup for automatic optimization with Si-IGBT and Si-diode.



(a) (b)

Fig. 3.14 Measured waveforms at (a) Single-step drive at same turn-n loss and (b) optimum point of SA optimization for Si-IGBT and Si-diode turn-on case.

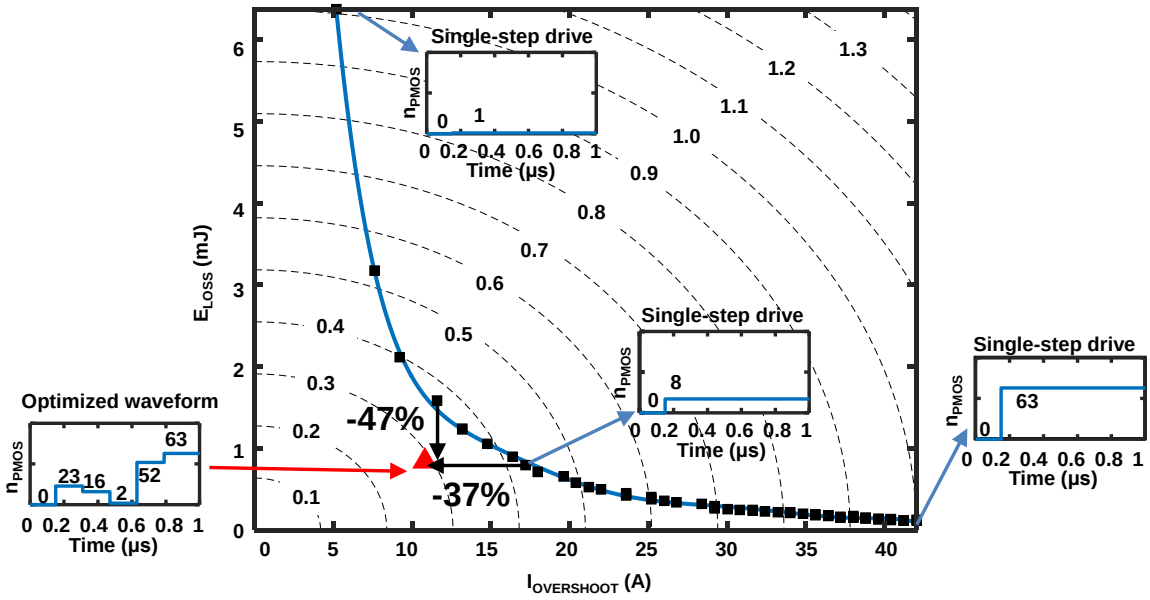
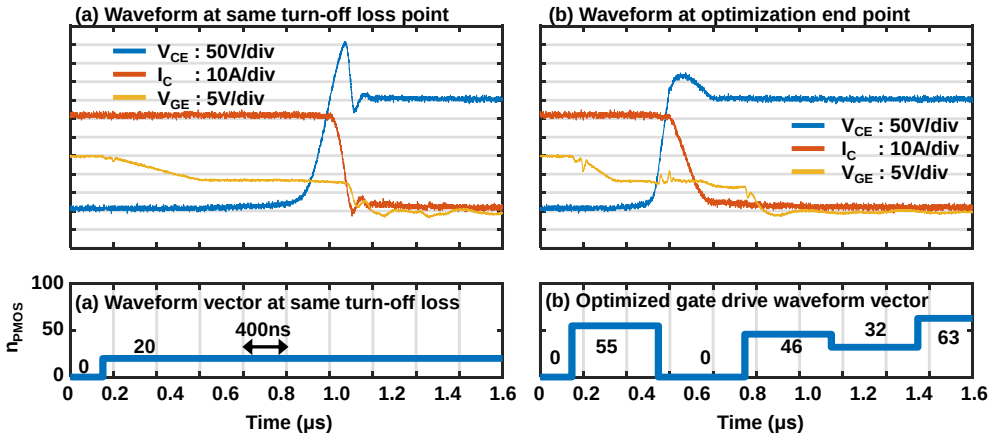


Fig. 3.15 E_{LOSS} - $I_{OVERSHOOT}$ trade-off of Si-IGBT and Si-diode. Broken lines are equi-f_{OBJECT} contour. Red triangles are optimized point.

Fig. 3.15 shows measured energy loss versus I_C overshoot in turn-on characteristics. It is seen that the three points are not exactly the same in the waveform vectors because of the stochastic nature of the SA optimization process. Still, all the optimized waveform shows considerable reduction in the object function and all have the characteristics that the drivability is lowered in the middle of the driving process. In Fig. 3.15, the trade-off between the energy loss, E_{LOSS}, and the current overshoot, $I_{OVERSHOOT}$, is also shown. With a simple single-step gate drive, the trade-off is confined on the blue line even the drivability step height is changed. With the more sophisticated gate drive using the programmable gate driver IC and four time-segmented drive, the achievable trade-off space is enlarged and 47% energy loss decrease and 37% current overshoot reduction are achieved compared with the single-step gate drive.

3.5.4. Results for turn-off of IGBT and Si-diode

The automatic optimization setup is applied to the turn-off case of the Si-IGBT and thSi-diode. As for the Si-IGBT and Si-diode case, the optimization procedure is basically the same as the Si-IGBT and Si-diode case with 300V, 52A as show in Fig. 3.16. Fig. 3.17 shows the measured waveforms at the end point of the optimization process and single-step drive point at the same loss. The optimized gate driving waveform turns out to drive relatively strongly at first and then, reduce the drivability just before V_{GE} reaches the threshold voltage of the IGBT, and gradually increase the drivability afterwards. This reduces the sharp voltage overshoot.



(a) (b)

Fig. 3.16 Measured waveforms at (a) Single-step drive at same turn-n loss and (b) optimum point of SA optimization for Si-IGBT and Si-diode turn-off case.

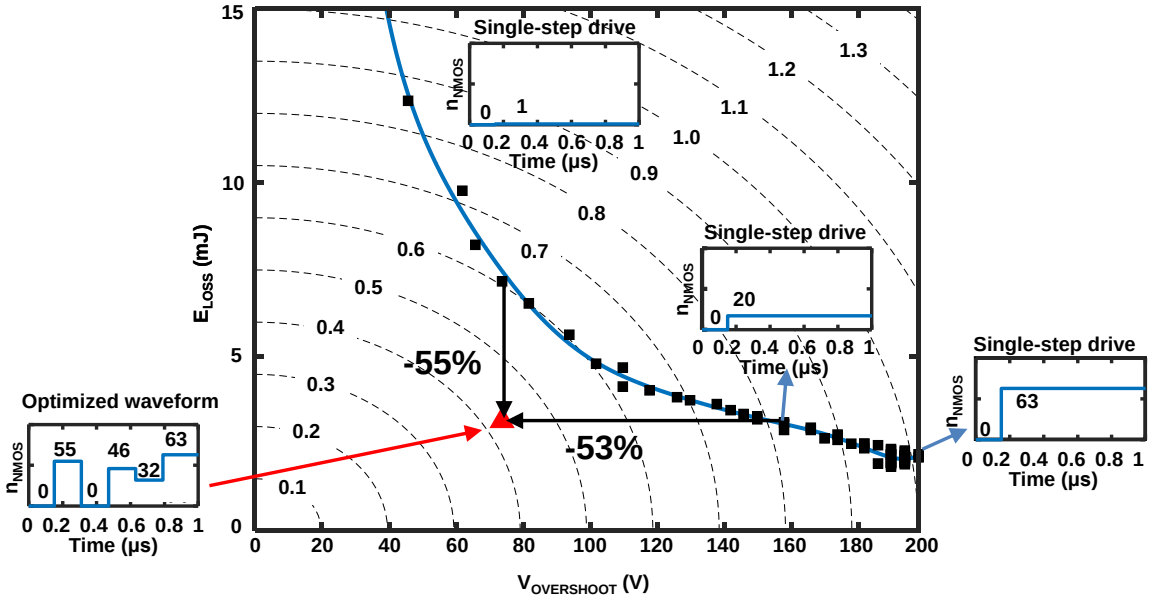


Fig. 3.17 E_{LOSS} - $V_{OVERSHOOT}$ trade-off of Si-IGBT and Si-diode. Broken lines are equi-f_{OBJECT} contour. Red triangles are optimized point.

Fig. 3.15 shows measured energy loss versus V_C overshoot in turn-on characteristics. It is seen that the three points are not exactly the same in the waveform vectors because of the stochastic nature of the SA optimization process. Still, all the optimized waveform shows considerable reduction in the object function and all have the characteristics that the drivability is lowered in the middle of the driving process. In Fig. 3.15, the trade-off between the energy loss, E_{LOSS}, and the current overshoot, $I_{OVERSHOOT}$, is also shown. With a simple single-step gate drive, the trade-off is confined on the blue line even the drivability step height is changed. With the more sophisticated gate drive using the programmable gate driver IC and four time-segmented drive, the achievable trade-off space is enlarged and 55% energy loss decrease and 53% voltage overshoot reduction are achieved compared with the single-step gate drive.

3.5.5. Result for time slot difference

Fig. 3.18 shows difference of f_{OBJECT} for different number of time slots in Si-IGBT and SiC-diode turn-off case. In above measurement, the number of time slots is 4. In order to show the validity of this number of time slots, this subsection shows the difference in f_{OBJECT} depending on the number of time slots. In this measurement, the case where the number of time slots is 1, 4, 8, 16 is measured. When the number of time slots is 1, it becomes the same as fixed resistance drive. For simplicity, $E_{LOSS,MIN}$ in Eq. (3.1) and $V_{OVERSHOOT,MIN}$ in Eq. (3.3) is set to 0. Although f_{OBJECT} improves by increasing the number of time slots, the difference is insignificant. Even if the number of time slots is exponentially increased, the improvement value of f_{OBJECT} is slight. In this case, for time slot number 16 with respect to time slot number 4, the improvement of f_{OBJECT} is about 20%. Increasing the number of time slots leads to an increase in the amount of hardware. That is, the improvement of F by increasing the number of time slots is not cost effective. Therefore, the number of time slots of the active gate driving waveform is sufficiently four.

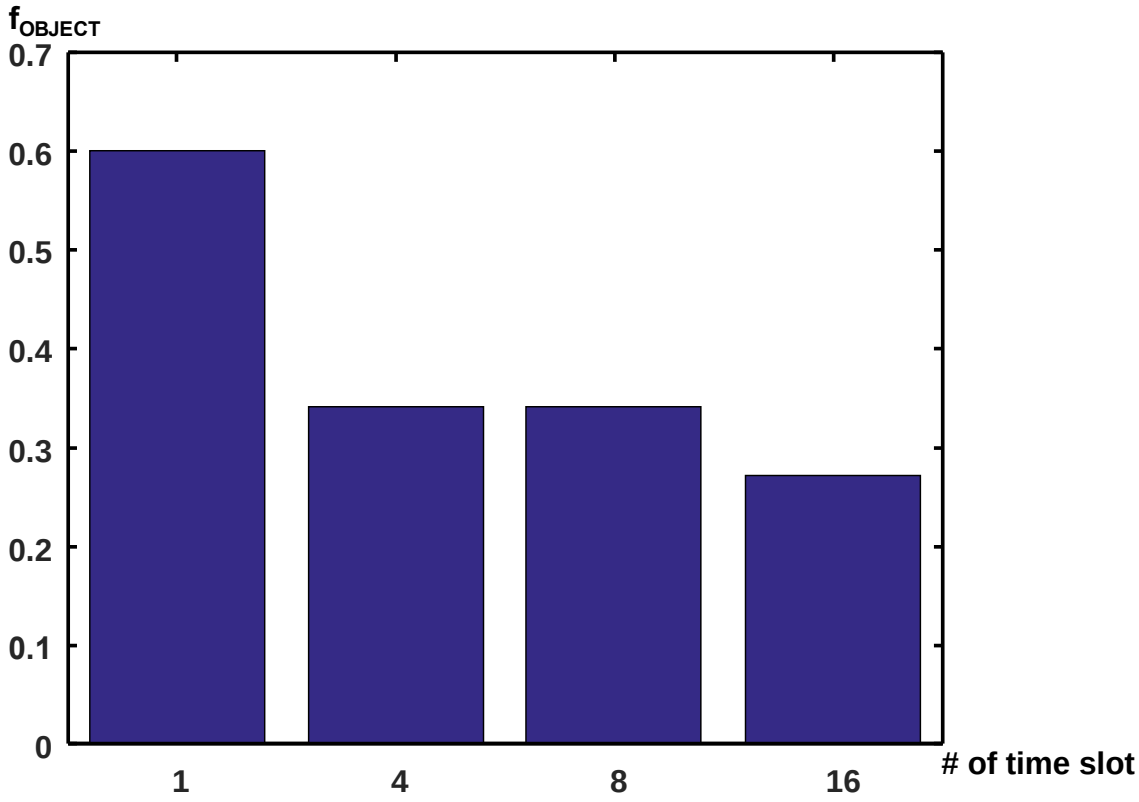


Fig. 3.18 Difference of f_{OBJECT} for different number of time slots.

3.5.6. Robust search

This subsection shows robust SA and its result with the Si-IGBT and the Si-diode turn-off case with V_{PD_NMOS} of 2.0V. In this measurement, a variation of operating condition is emulated by varying I_G. From the Eqs. (1.2) (1.11), switching behavior depends on I_G. Therefore, the variation of operating conditions is emulated by I_G. I_G variation is controlled by V_{PD_NMOS}, and V_{PD_NMOS} is varied by ± 0.1V with respect to the typical value 2.0V. This corresponds to the I_G variation of 20% or more. For the search method, the SA is performed with the worst value among the three points of V_{PD_NMOS} = 1.9, 2.0, 2.1 at the same waveform vector [n_1, n_2, n_3, n_4] set as the evaluation value.

Fig. 3.19 shows SA results without robustness (blue triangle) and with robustness (red

triangle). In the case of the SA without robustness, the searched gate driving waveform shows improved characteristics in V_{PD_PMOS} as a typical value. But, when V_{PD_PMOS} varies, the characteristics deteriorates greatly. On the other hand, the gate driving waveform searched by the SA with robustness shows improved characteristics without degradation even when I_G varies 20%.

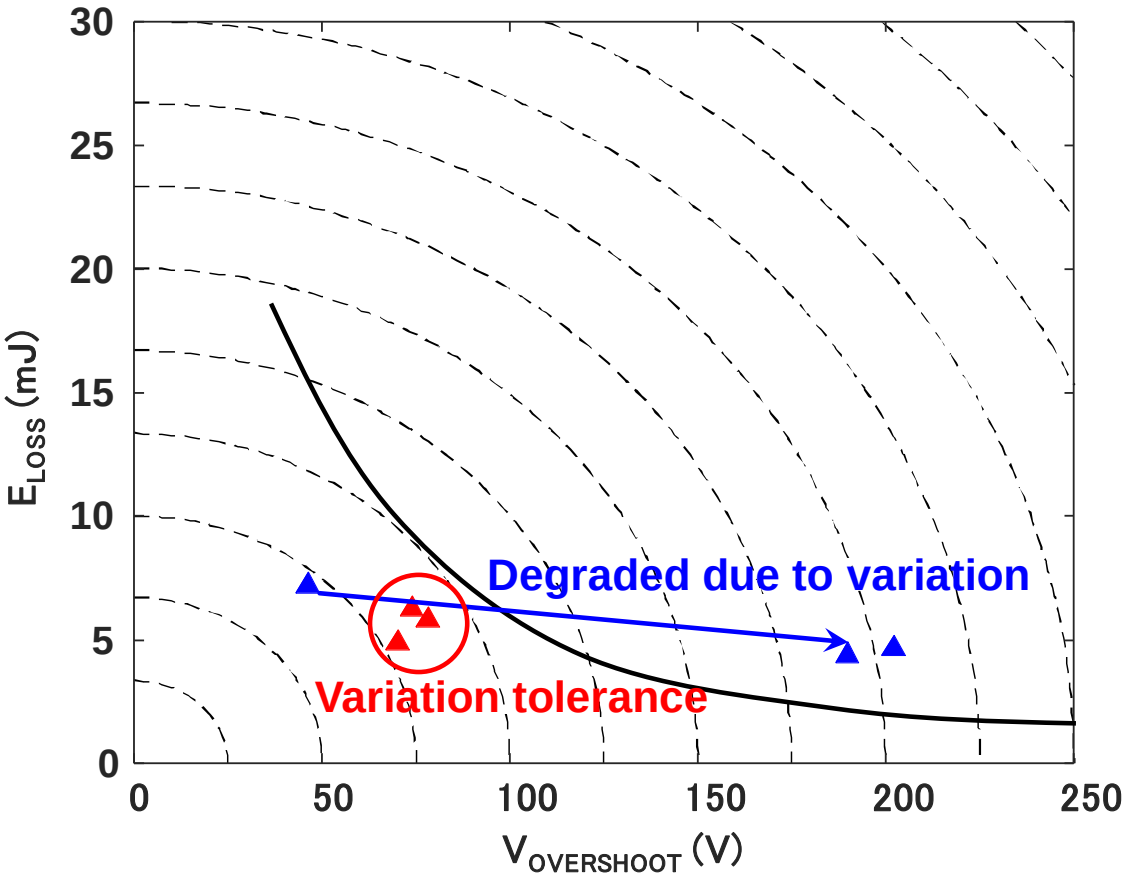


Fig. 3.19 SA results without robustness (blue triangle) and with robustness (red triangle).

3.6. Conclusion

A novel search method based on simulated annealing algorithm is described to find the better gate driving waveforms for power devices. The method is shown to be effective in optimizing the trade-off between the energy loss and the waveform overshoot by using a double pulse test configuration as an example. In this paper, the number of the time-segments is set to four but it may be increased to 16 or more for further better driving waveforms. Then, the search space increases exponentially and the proposed automatic optimization approach becomes more indispensable. Although an optimization example is depicted in this paper, the presented SA-based optimization for the gate driving waveforms can be applicable to the wider range of problems toward the better circuit performance.

3.7. References

[3.1] N. Idir, R. Bausière and J. J. Franchaudm, "Active Gate Voltage Control of Turn-on di/dt and Turn-off dv/dt in Insulated Gate Transistors," IEEE Trans. on Power Electron., vol. 21, no. 4, pp. 849-855, Jul. 2006.

[3.2] A. Shorten, W. T. Ng, M. Sasaki, T. Kawashima and H. Nishio, "A Segmented Gate Driver IC for the Reduction of IGBT Collector Current Over-Shoot at Turn-on," IEEE ISPSD, pp. 73-76, May 2013.

[3.3] F. Zhang, Y. Ren; M. Tian and X. Yang, "A Novel Active Gate Drive for HV-IGBTs using Feed-Forward Gate Charge Control Strategy," IEEE ECCE, pp.7009-7014, 2015.

[3.4] V. John, B. S. Suh, and T. A. Lipo, "High performance active drive for high power IGBTs," in Proc. IEEE IAS'98, 1998, pp. 1519–1529.

[3.5] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," IEEE Trans. on Power Electronics, Vol. 29, No. 7, pp 3720-3732, Jul. 2014.

[3.6] Y. Lobsiger and J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT gate driver," IEEE Trans. on Power Electronics, Vol. 30, No. 6, pp. 3402-3417, Jun. 2015.

[3.7] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration," IEEE Applied Power Electronics Conf. and Expo., pp.774-781, Mar. 2015.

[3.8] D. J. Rogers and B. Murmann, "Digital Active Gate Drives Using Sequential Optimization," IEEE Applied Power Electronics Conf. and Expo., pp. 1650-1656,

Mar. 2016.

[3.9] Y. Miki, M. Mukunori, T. Matsuyoshi, M. Tsukuda, and I. Omura, “High speed turn-on gate driving for 4.5kV IEGT without increase in PIN diode recovery current,” IEEE Int. Symp. on Power Semiconductor Devices and ICs, pp. 347-350, May 2013.

[3.10] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya and T. Sakurai, "General-Purpose Clocked Gate Driver (CGD) IC with Programmable 63-Level Drivability to Reduce Ic Overshoot and Switching Loss of Various Power Transistors," IEEE Applied Power Electronics Conf. and Expo., pp. 1640-1645, Mar. 2016.

[3.11] T. Sakurai, B. Lin and A. R. Newton. "Fast Simulated Diffusion: An Optimization Algorithm for Multi-Minimum Problems and Its Application to MOSFET Model Parameter Extraction," IEEE Trans. on CAD, pp.228-234, Feb. 1992.

Chapter 4

Short-Circuit Detector Design

4.1. Background

A short-circuit is a serious problem causing device destruction. Under the short-circuit condition, high voltage and overcurrent is applied between the collector and the emitter of the power device. Excessive heat due to the high voltage and the overcurrent causes device destruction. In order to avoid the destruction, it is necessary to detect the short-circuit condition quickly and protect the power device by turning off the gate. The time until the power device is destroyed by the short-circuit is called the short-circuit tolerance.

There are two types of an arm-short and a load-short shown as in Fig. 4.1 (a) shows the arm-short. The arm-short occurs when the upper and lower arms in the same leg are turned on at the same time. The cause of the arm-short is malfunction of the arm or due to noise or conduction of one side arm due to device destruction. Current rise at the arm-short is fast because there is no inductive element in the current path. Therefore, at the arm-short, Since the temperature rise of the power device is fast, the short-circuit tolerance is low. Fig. 4.1

(b) shows the load-short. The load-short occurs due to a light load inductance. The cause of the load-short is the connection due to physical damage or load slipping. Current rise at load-short is slow because of there is inductive element in the current path. So, at the load-short, the short-circuit tolerance is high. Compared with the load-short, the arm-short requires quick detection of short-circuit condition because of the low short-circuit tolerance due to fast current rise. The current rise of arm-short is determined by the current performance of the power device. For power devices with high current density, current at arm-short increases and the short-circuit tolerance decreases. In the future power device with increased current density, the arm-short problem is more serious. A high-speed short-circuit detector (SCD) is necessary to protect the future power device from arm-short.

In this chapter, conventional short-circuit detectors and their problems are introduced at first. After that, a novel short-circuit detector is proposed to cope with these problems.

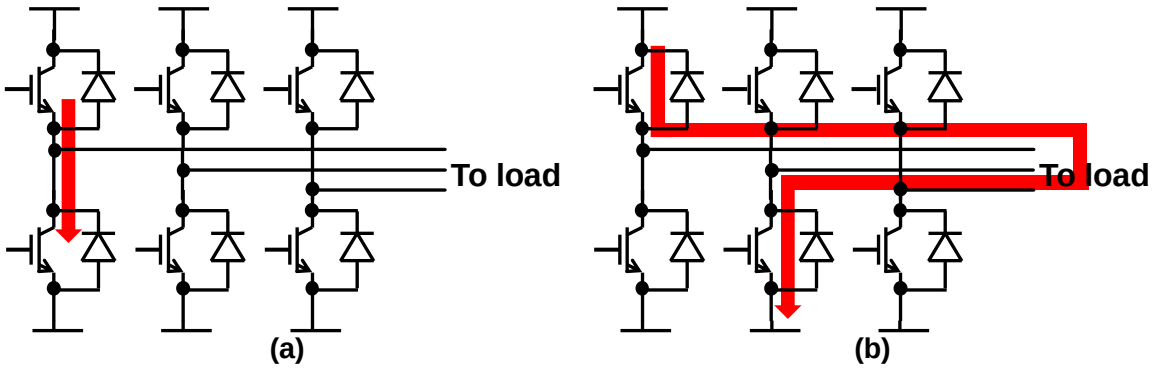


Fig. 4.1 the types of short-circuit. (a) arm-short. (b) load-short.

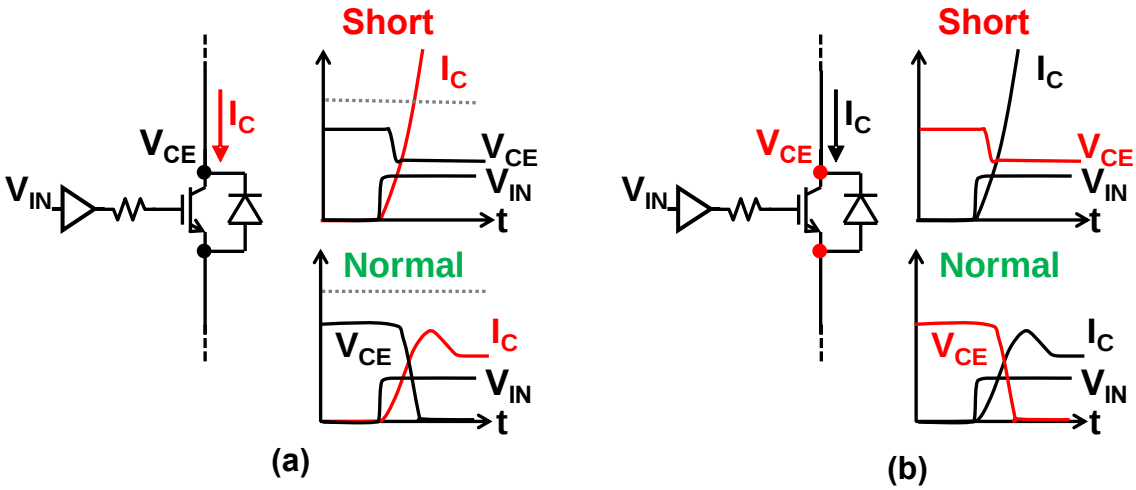


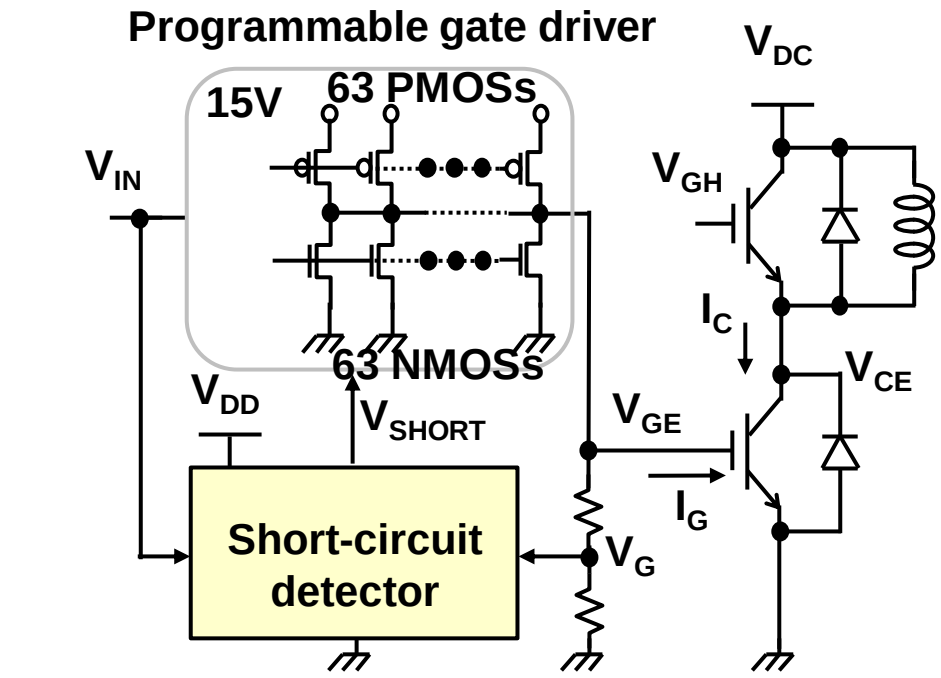
Fig. 4.2 Conventional short-circuit detection method. (a) overcurrent detection. (b) desaturation voltage detection.

Conventional SCDs include a collector current monitoring method and a voltage monitoring method. The current monitoring method detects short-circuit condition by detecting overcurrent of I_C as shown in Fig. 4.2 (a). Normally, I_C does not exceed the rated current of power devices, but in the short-circuit condition, the overcurrent that exceeds the rating flows. This method is realized with a simple architecture, but it takes time to detect a short-circuit condition because the speed of the current sensor is slow. The voltage monitoring method detects the short-circuit condition by detecting excessive voltage of V_{CE} in the on-state as shown in Fig. 4.2 (b). In the normal condition, V_{CE} is low at the on-state, but in the short-circuit condition, V_{CE} is high because of light load. The detection speed of voltage monitoring method is slow because of dead-time to avoid fault detection. At the start of turn-on, V_{CE} is high because the power device is still off. At this moment, if short-circuit detection determination is performed by V_{CE} monitoring, erroneous detection is made as the short-circuit condition despite normal operation. Therefore, it is necessary to set the dead-time in order to wait for completion of the turn-on operation. Since conventional SCDs are slow, it is not suitable for the power device with high current density.

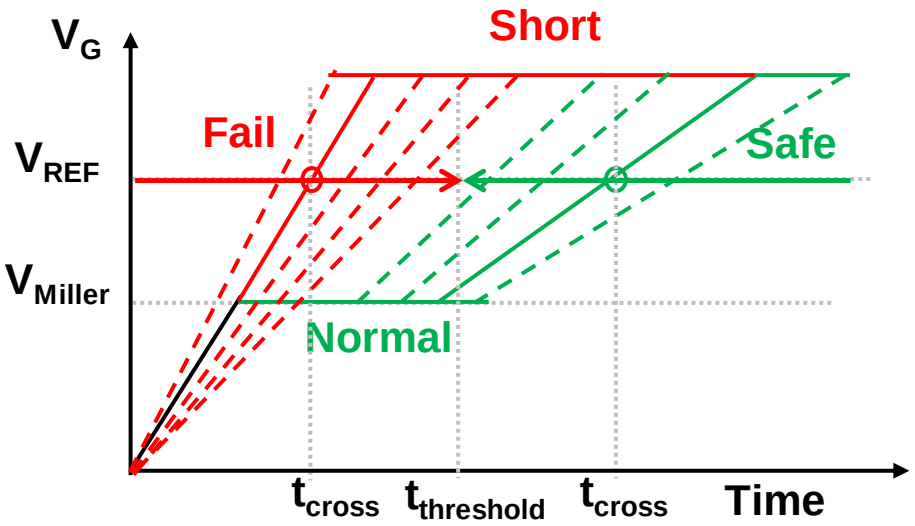
4.2. Gate voltage monitoring method

A SCD by monitoring the gate state of an IGBT is a fast short-circuit detection method. The typical configuration of SCD is shown in Fig. 4.3 (a) has been pursued extensively but most of the proposals were slow and can't meet the need for the future advanced IGBT which demands less than 0.5-μs detection delay. In the figure, V_G is generated by dividing V_{GE} using resistors and monitored by the SCD. A relatively fast SCD was previously reported based on the existence of a Miller plateau in a gate waveform when short-circuit does not occur, which achieved 1-μs detection delay [4.4]. The main cause of the detection delay is the wiring delay on the board. The detection scheme is shown in Fig. 4.3 (b). In this scheme, V_{REF}, above the Miller plateau voltage, V_{Miller}, is preset. The time when V_G crosses V_{REF}, is signified as t_{cross}. If t_{cross} is earlier than a certain preset threshold time, $t_{threshold}$, that is, t_{cross} falls in the red Fail region, the short-circuit condition is met and the short-circuit flag, V_{SHORT}, is asserted. On the other hand, if t_{cross} falls in the green Safe region, V_{SHORT} is negated. This scheme works fine as far as there is no variability in the V_G slope.

In the Chapter 3, the method of performing switching with an optimum gate driving waveform suitable for an operating condition has been proposed for the future power device. The optimum gate driving waveform selection for each operating condition causes variability in the V_G slope. Therefore, if the conventional gate voltage monitoring method is combined with this optimization method, short-circuit detection can not to be normally performed. A SCD is proposed which has high detection speed due to integration and is tolerant to V_G slope change due to circuit technique.



(a)

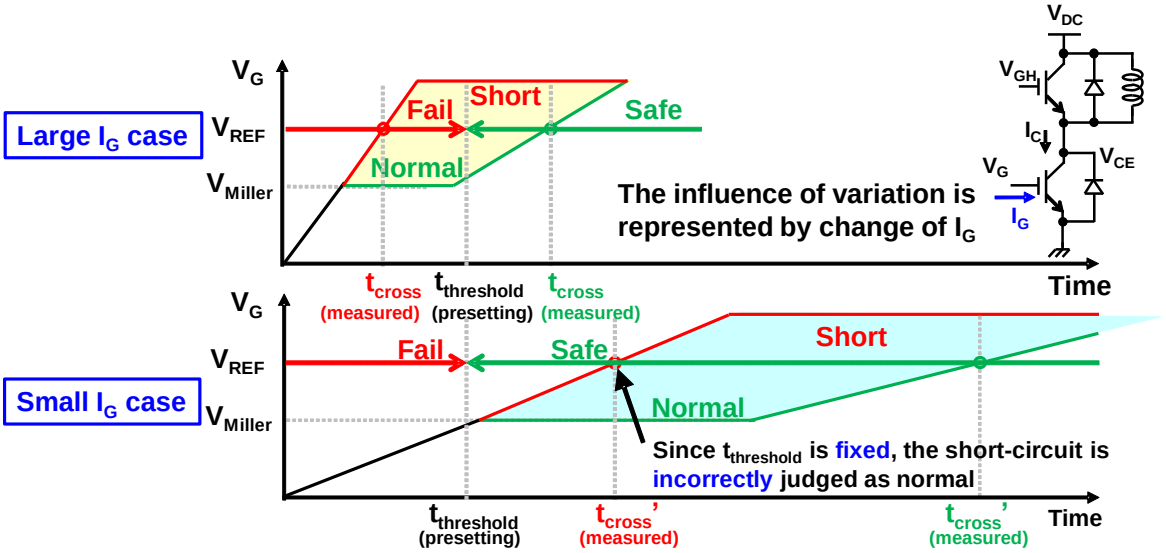


(b)

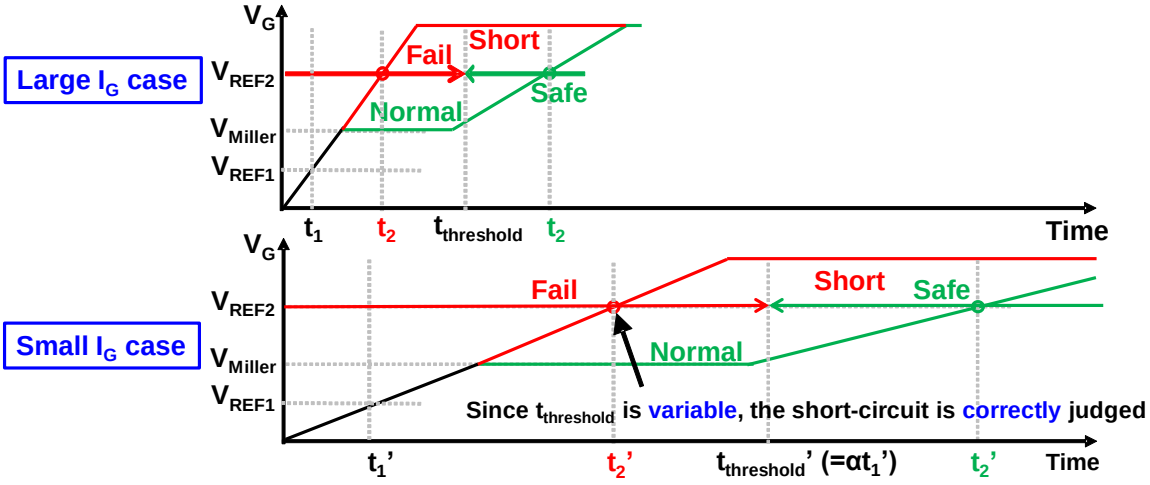
Fig. 4.3 (a) Example of short-circuit detector setup and (b) conventional short-circuit detection scheme.

4.3. Proposed variation-tolerant scheme

Suppose that there is a V_G slope variation as shown in Fig. 4.4 (a) due to the IGBT gate capacitance variation and/or the gate turn-on current variation. If $t_{threshold}$ is preset as shown in the figure, V_{SHORT} is always negated for the slow case since t_{cross}' always falls into the green Safe region. If $t_{threshold}$ is preset at much later time, it is proper for the slow case while it is unacceptable for the fast case. Since there is no overlap between the yellow region and the sky blue region, it is impossible to choose a proper $t_{threshold}$ in this conventional scheme. Even if the V_G slope variation is not that large, the conventional scheme suffers from small margins. In order to cope with this problem, $t_{threshold}$ is adaptively determined in the proposed scheme as is conceptually shown in Fig. 4.4 (b). A certain voltage, V_{REF1}, is preset below V_{Miller}. The time when V_G crosses V_{REF1} is signified as t_1. $t_{threshold}$ is set as αt_1 where the multiplier α is digitally tunable from 1 to 16 using 4-bit control signals. When V_G is slow, t_1 is large and $t_{threshold}$ ($=\alpha t_1$) is also large. On the other hand, when V_G is fast, t_1 is small and $t_{threshold}$ ($=\alpha t_1$) is also small adaptively. In this way, $t_{threshold}$ is properly determined in a self-aligned manner even if the V_G slope has variability as shown in Fig. 4.4 (b).



(a)



(b)

Fig. 4.4 (a) Conventional and (b) proposed SCD operation concept with V_G slope variation.

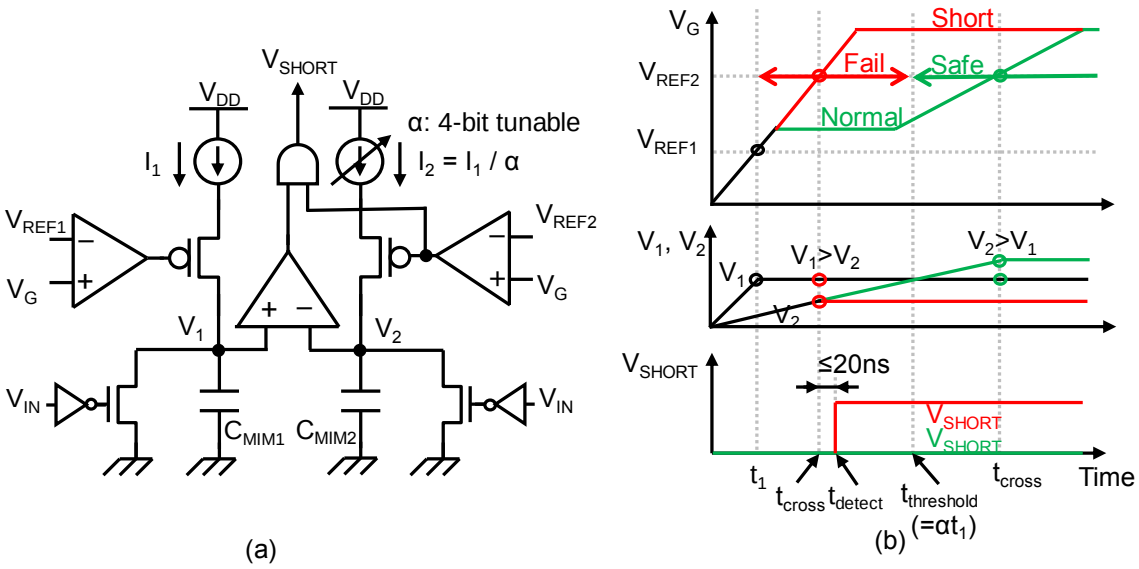


Fig. 4.5 (a) Circuit diagram of proposed scheme and (b) operation waveforms.

The circuit to realize the above-mentioned concept is shown in Fig. 4.5 (a) together with the operation waveforms in Fig. 4.5 (b). When V_{IN} turns on, the MIM capacitors, C_{MIM1} and C_{MIM2}, start to be charged by I_1 and I_1/α, respectively. C_{MIM1} stops to be charged when V_G crosses V_{REF1}, that is, at t_1. C_{MIM2} stops to be charged when V_G crosses V_{REF2}, that is, at t_{cross}. At t_{cross}, V_1 and V_2 are compared. If $V_1 > V_2$, V_{SHORT} is asserted. On the contrary, if $V_1 < V_2$, V_{SHORT} is negated. The threshold time corresponds to the condition that $V_1 = V_2$, and thus $t_{threshold}$ is calculated to be αt_1. In this way, the required adaptivity of $t_{threshold}$ is implemented. This novel analog delay multiplier circuit using two capacitors multiplies t_1 by α to generate $t_{threshold}$.

4.4. Measurement results

The test board photo, the IC photo and the IC layout are shown in Fig. 4. A double pulse test circuit is built with Si-IGBT (IRG7PH46UPbF) and SiC-diode (C4D10120D) as depicted in Fig. 4.3, which is driven by a programmable driver IC with 64-level current resolution and 40-ns minimum time step [4.6]. A single pulse test is employed for the short-circuit condition. Although only low side was measured here, the SCD is easily applied for the high side with proper high-voltage isolators. V_{DC} is set to 50V in order for the short-circuit current to be not so high. The fabricated chip is covered with dummy metal patterns and as a result, the circuit pattern is not clearly visible. Thus, layout of the circuit is also shown in Fig. 4.6 (d).

Fig. 4.7 shows the measured waveforms without and with the short circuit. If there is no short circuit, the Miller plateau is present and V_{SHORT} is negated, while when a short circuit exists, V_{GE} and V_G are rising sharply without the Miller plateau and V_{SHORT} is asserted. The circuit successfully functions over wide range of I_G variation from 72mA through 756mA, which corresponds to more than 10 times the V_G slope variation. The maximum measured short-circuit detection delay is 20ns.

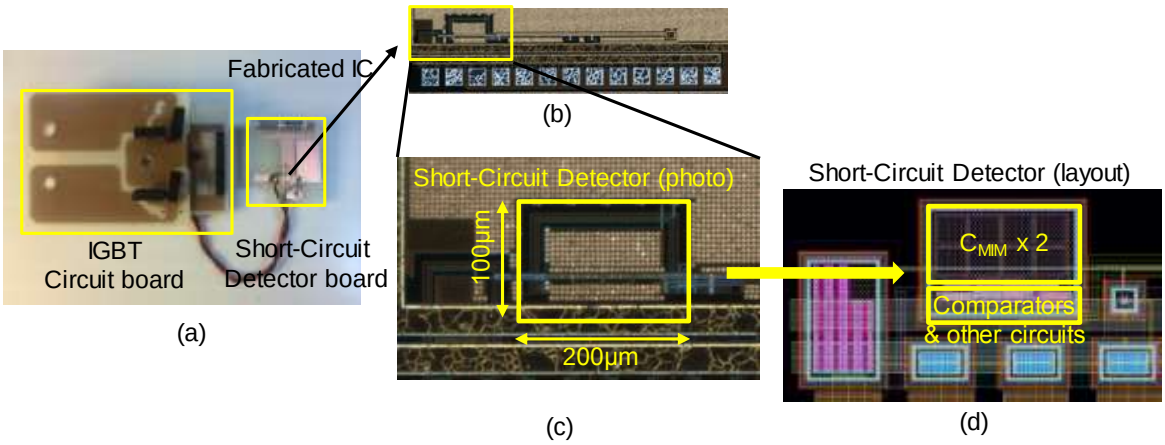


Fig. 4.6 (a) Test board, (b) chip with pad photo, (c) photo of chip main part and (d) layout of chip main part.

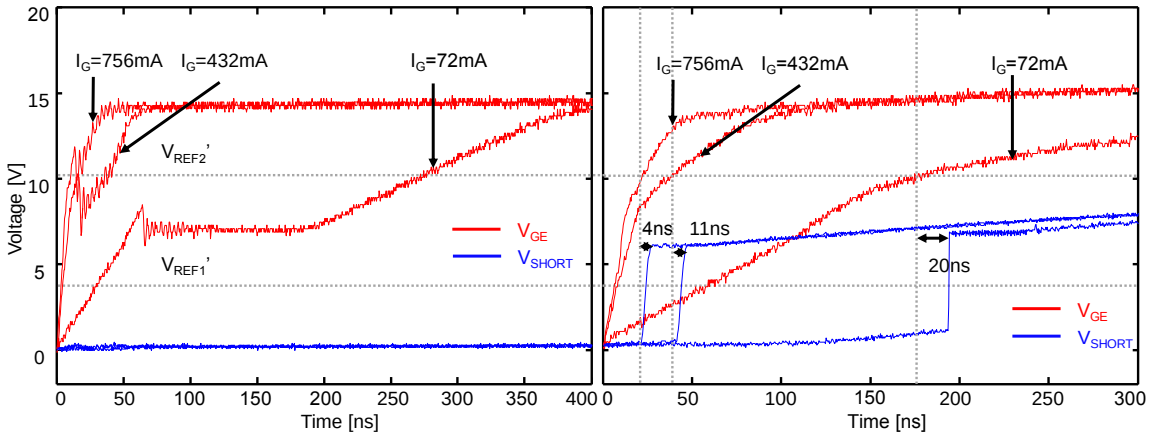


Fig. 4.7 Measured V_G and V_{SHORT} waveforms for (a) normal case and (b) short-circuit case.

Table 4-1 Comparison among Short-Circuit Detection Schemes.

	[4.1]	[4.2]	[4.3]	[4.4]	[4.5]	This work
Detection speed	2μs	1.5μs	3μs	1μs	50ns	20ns
Additional components	V_{CE} sensor	No	Kelvin emitter	No	Kelvin emitter	No
Variation tolerance	NA	NA	NA	NA	NA	>10x V_G slope I_G:72mA~756mA

4.5. Conclusion

A novel short-circuit detection scheme is proposed. The circuit is designed and fabricated using widely used high-voltage CMOS technology. The measurement shows 20-ns detection delay and 10 times V_G slope tolerance.

Table 4-1 shows the comparison of this work with other short-circuit detection schemes. It is seen from the table that the proposed circuit is demonstrated to provide the fastest and the most robust short-circuit detection scheme without additional off-chip components. Consequently, the scheme can be widely applicable to the power circuits with IGBTs for the future.

4.6. References

[4.1] R. S. Chokhawala, J. Catt and L. Kiraly, “A Discussion on IGBT Short-Circuit Behavior and Fault Protection Schemes,” IEEE Trans. Ind. Appl., vol. 31, no. 2, pp.256-263, Mar./Apr. 1995.

[4.2] T. Tanimura, K. Yuasa, and I. Omura, “Full digital short circuit protection for advanced IGBTs,” in Conf. Rec. IEEE ISPSD, pp. 60–63, 2011.

[4.3] Z. Wang, X. Shi, L. M. Tolbert, F. Wang and B. J. Blalock, “A di/dt Feedback-Based Active Gate Driver for Smart Switching and Fast Overcurrent Protection of IGBT Modules,” IEEE Trans. Power. Electron., vol. 29, no. 7, pp. 3720-3732, Jul. 2014.

[4.4] T. Horiguchi, S. Kinouchi, Y. Nakayama, T. Oi, H. Urushibara, S. Okamoto, S. Tominaga and H. Akagi, “A High-Speed Protection Circuit for IGBTs Subjected to Hard-Switching Faults,” IEEE Trans. Ind. Appl., vol. 51, no. 2, pp. 1774-1781, Mar. 2015.

[4.5] S. Hain and M. M. Bakran, “New Ultra-Fast Short Circuit Detection Method Without Using the Desaturation Process of the Power Semiconductor,” Proc of PCIM Europe, pp. 720-727, 2016.

[4.6] K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, T. Sakurai, "General-Purpose Clocked Gate Driver (CGD) IC with Programmable 63-Level Drivability to Reduce Ic Overshoot and Switching Loss of Various Power Transistors," IEEE APEC, pp.1640-1645, 2016.

Chapter 5

Conclusions and Future Prospects

5.1. Conclusions

Improvement of reliability against the noise and the short circuit is realized by the gate drive circuit method for power devices in this research. Chapter 2 shows the programmable gate drive circuit compatible with various power devices and shows that active gate waveform control is possible. In Chapter 3, by using optimum waveform searching method with the programmable gate drive circuit and simulated annealing algorithm, reduction of noise during the switching of power devices is realized. In Chapter 4, by using an analog delay multiplier as a method capable of detecting a short circuit without an off-chip component, we realized a method that can adjust the detection condition arbitrarily at high speed. We introduced the LSI circuit method to the gate drive circuit and showed it to the extent that could not be handled by the conventional passive element method.

The achievement of this research described in each chapter is summarized in Table 5-1.

Table 5-1 The achievement of this research described in each chapter.

Chapter	Methodology	Achievement	Verification
2	Programmable gate driver technology	Improved switching for various devices	Measurement
		Noise tolerance	Simulation
3	Simulated annealing base automatic optimization	Improved switching for various devices	Measurement
		Robust optimization	
4	High-speed and variation-tolerance short-circuit detection technology	20ns detection	Measurement
		10 times variation tolerance	

5.2. Future prospects

In this subsection, future perspectives of power electronics are described as discussions. The power device switching has various other problems to solve with gate drivers. In this thesis, only the problem of single power device switching is discussed. However, power conversion circuits consist of multiple power devices. Interactions between these individual power devices are great concern. Besides, challenges still remain to detect the abnormal state of power devices. In order to solve these problems, it is conceivable that the power electronics will develop.

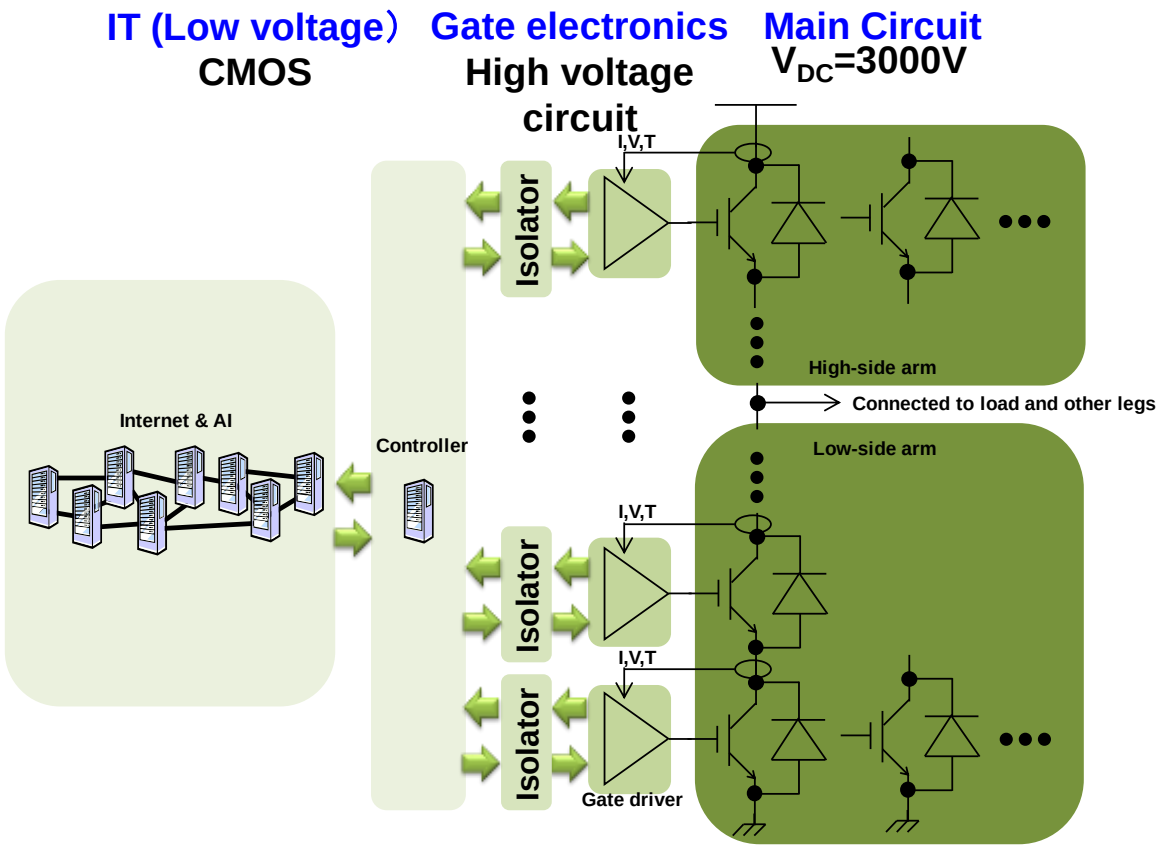


Fig. 5.1 A forecast of future power electronics.

Fig. 5.1 shows a forecast of future power electronics. In order to increase the capacity of the power conversion circuit and increase the withstand voltage, the serialization and parallelization of the IGBT progresses. Since the number of IGBTs increases, in order to optimally control each IGBT, a gate driver is added to each one. Therefore, not only the active drive control described in this thesis but also the current voltage temperature sensor is necessary for the function required for the gate driver. Also, it is conceivable that AI is utilized to compile the data of the IGBT sent from the gate driver to the controller. By utilizing myriad IGBTs data using AI, it is possible to detect a sign of failure and respond to changes in operating conditions. In this section, functions of the gate driver required for future power electronics is discussed.

5.2.1. Integrated sensors for SOA based switching

In order to keep a SOA of power devices, real time monitoring is required. In order to operate the power device more safely, it is necessary to perform the operation strictly observing the SOA. In order to monitor the operation of each power device, current and voltage sensors are all required. However, there are problems in terms of cost, installation space, and sensor performance to attach a sensor to each power device. Therefore, in order to solve these problems, a method of integrating a current / voltage sensor in the IC is conceivable.

Three types of current sensors are considered: Hall sensor, rogowsky coil, transformer. Hall sensor is compatible with integration, sensitivity can be adjusted by sizing. The output voltage V_H of the Hall sensor is expressed by the following equation,

$$V_H = \mu \frac{W}{L} B V_{IN} . \tag{5.1}$$

Here, μ represents mobility of the device. V_{IN} is bias voltage. W represents the length of the Hall element, and it is also the length between the terminals to which V_{IN} is applied. L represents width of Hall device.

A Si-Hall sensor is designed and implemented, and measurement was carried out. Fig. 5.2 shows a layout of designed silicon Hall sensor. Since the silicon Hall sensor has low mobility of silicon, however, magnetism of the magnet can be detected, but magnetism emitted by the current can not be detected. Therefore, it is necessary to use a compound semiconductor for the current detection by the Hall sensor.

In addition to the Hall sensor, a method of implementing a Rogowski coil or a transformer is conceivable.

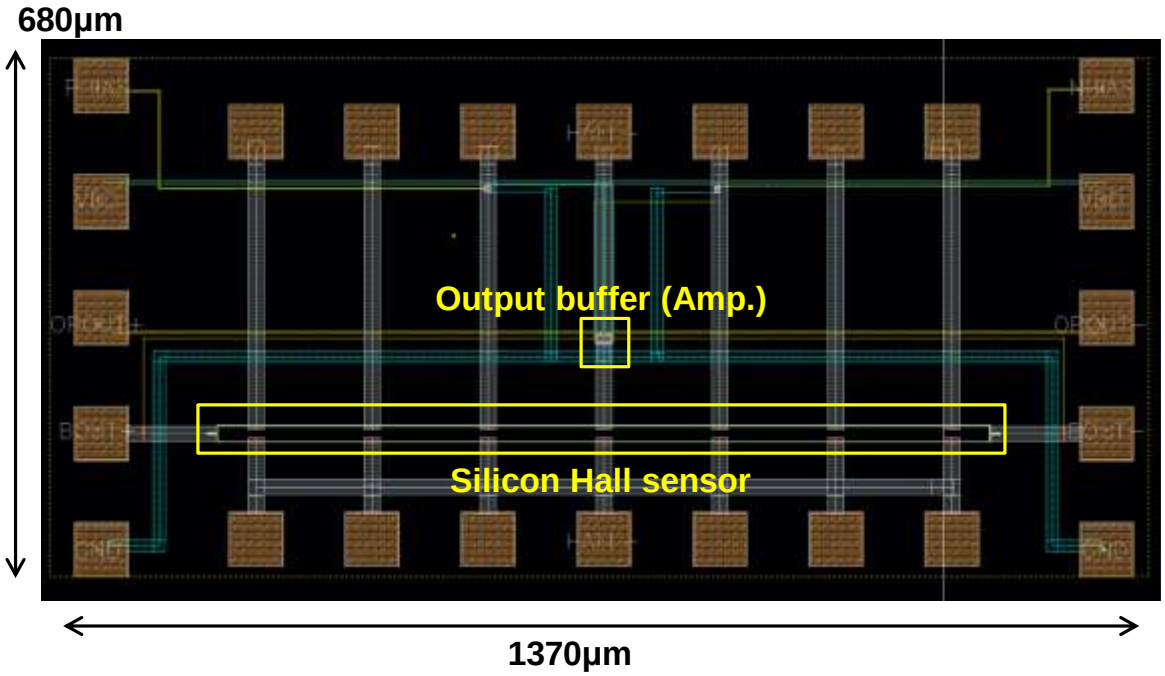


Fig. 5.2 Layout of designed silicon Hall sensor.

5.2.2. Timing control for parallel connected power devices

Device variation of parallel connected power device chips result in thermal concentration. In power modules, power device chips are often connected in parallel in order to increase the current capacity. In such power device chips connected in parallel, heat concentration due to variations among devices becomes a problem. If there are variations among the chips connected in parallel, the switching timing of each is different. When the switching timing is different, at the turn-on time, the current concentrates on the chip which is turned on for the first time, and at the turn-off time, the current concentrates on the chip which was turned off at the last. The temperature of the chip where the current concentrates is high. Then, in the operation in the bipolar saturation region, as the temperature rises, more current flows. Since the IGBT is a device operating in the bipolar saturation region, the current flowing

through the device in which the current is concentrated is further increased due to the temperature rise. This positive cycle causes a problem because the heat concentration occurs.

Conventionally, a method has been adopted to mitigate the problem by selecting devices of close characteristics and connecting them in parallel. This method is costly and can not cope with characteristic changes due to aged deterioration of the device. Therefore, it is conceivable to solve the heat concentration problem by connecting one gate driver chip to one power device chip and adjusting the switch timing of each power device chip.

In a serial connected IGBTs case, overvoltage is main problem. When using IGBTs for high voltage applications, it is sometimes used in serial connection to obtain the higher block voltage. Also in this case, as with the case of parallel connection, variations among devices become a problem. Since the switching timing varies, overvoltage is applied to a specific device. This device is the device with the slowest switching at turn-on, and the fastest switching at turn-off. The variation problem in the serial connection can be similarly solved by the method described in the parallel connection.

5.2.3. Data communication circuit of gate driver for IoT

Each power devices need to be IoT for optimization of whole power conversion system. In the power conversion system, it is important to balance the switch timing and switch characteristics of each power device. It is a very difficult task to optimally adjust the switching of each device, and it is conceivable that optimization by automatic search will be performed in the future. In order to perform automatic optimization, switching characteristics are acquired by each gate driver connected to the power device, and optimum search is performed by the controller. Therefore, in order to acquire the switching characteristics of each power device and send them to the controller, it is necessary to place the data communication circuit on the gate driver.

Between the current gate driver and the controller there is only a communication path for sending switching on / off signals. This is a problem of the cost and communication speed of the signal transmission isolator between the gate driver and the controller. Therefore, it is conceivable to solve the problem by generating a signal bus by integration of the isolator, or by multiplexing signals by increasing communication speed.

Gate drivers in the future requires integrated sensors and high-speed communication path to solve the above-mentioned problems.

Appendix

A.1. Simulated annealing search program

Fig. A.1 shows a block diagram of LabView program for optimum gate driving waveform search with simulated annealing. The program flow starts from the left and flows to the right. First, set the initial condition of the program. The setting items are the number of time slots, an address of a data storage folder, an initial waveform vector and establishment of connection with measurement equipment. After the initial setting, execute the search loop. Operation conditions are set at the beginning of loop processing. They are the setting of the double pulse test, the generation of the waveform vector and the setting of the measurement equipment. After completing the above setting, output the waveform vector via LabView Digital I/O. The result of the double pulse test is taken into a PC via an oscilloscope and evaluated. This evaluation is performed based on the simulated annealing method. When this is completed, it returns to the beginning of the loop.

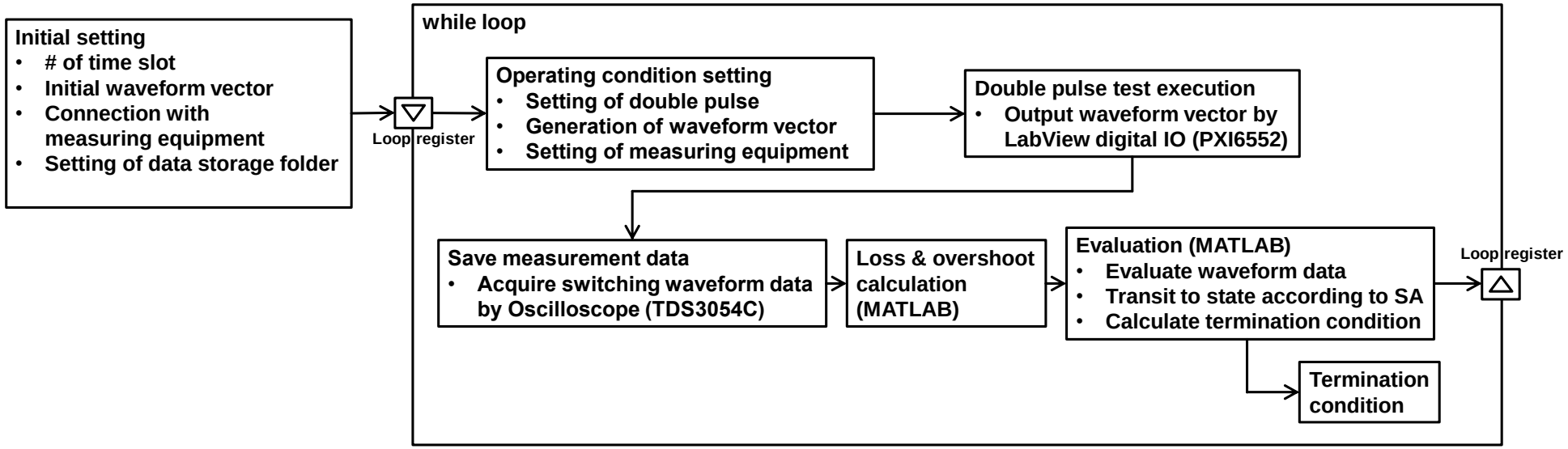


Fig. A.1 Block diagram of LabView program of SA for gate driving waveform optimization.

A.1.1. MATLAB script for loss & overshoot calculation

```
CURRENT=dlmread(file_current, ' ', 1, 0);
cur_tim=CURRENT(:,1);n=max(size(cur_tim));
cur_vol=CURRENT(:,2);
cur_cur=CURRENT(:,3)*20;
cur_gat=CURRENT(:,4);
cur_pow=cur_cur.*cur_vol;
cur_los=zeros(n,1);
for i=2:1:n-99
    ave_vol=0;
    k=0;
    for j=i:1:i+99
        ave_vol=ave_vol+cur_vol(j);
    end
    ave_vol=ave_vol/100;
    if cur_pow(i)<0 || (ave_vol<30)
        cur_los(i)=cur_los(i-1);
    else
        cur_los(i)=cur_los(i-1)+cur_tim(2)*cur_pow(i);
    end
end
curM=max(cur_cur)-load_current;
losM=max(cur_los);
```

A.1.2. MATLAB script for evaluation

```
    In0=Inmax-Inmin;
    Psum0=Psummax-Psummin;
    qeval=sqrt(((In-Inmin)/In0)^2+((Psum-Psummin)/Psum0)^2);
    Ig_now=Ig;
    if (qeval>worst(1))
        worst(1)=qeval
        worst(2)=In
```

```
            worst(3)=Psum
        end
        delE=worst(1)-qeval_sa;
        if (robust==3)&&(delE<0 || (rand<exp(-delE/t)))
            Ig_sa=Ig;
            In_sa=worst(2);
            Psum_sa=worst(3);
            qeval_sa=worst(1);
        else
            Ig=Ig_sa;
        end
        if (qeval_best > qeval_sa)&&robust==3
            Ig_best=Ig_sa;
            In_best=In_sa;
            Psum_best=Psum_sa;
            qeval_best=qeval_sa;
            t_best=t;
        end
   dlmwrite(filename,horzcat(i,Ig_now,In,Psum,qeval,t,robust,worst,Ig_sa,qeval_sa,Ig_bes
t,In_best,Psum_best,qeval_best),'-append');
        if (robust==3)
            worst=[0 500 500]
        end
        if robust==3
            robust=1;
            t=t*0.99;%j=j+1;
        else
            robust=robust+1;
        end
          if t<=(t0/loopc) && qeval_sa>qeval_best && ~isequal(Ig_sa,Ig_best)
              t_best=t_best;
              t=t_best;
              qeval_sa=qeval_best;
              Ig_sa=Ig_best;
              In_sa=In_best;
              Psum_sa=Psum_best;
          end
```

A.2. Waveform optimization with different object function

In this section, results of SA search using different object function f_{OBJECT} are shown. The optimization setup is shown in Fig. A.2. A double pulse test board is built with the Si-IGBT and the SiC-diode, which is driven by a programmable driver IC with 64-level current resolution and 40-ns time step. Any strength of drivability from 0 to 64 (x 12-mA) can be chosen for each of 8 time segments of 40-ns. Thus, 64^8 (~$2.8x10^{14}$) number of waveforms need to be tried for an exhaustive search, which is impractical. The target is to optimize Ic overshoot, I_N, and energy loss, E_{LOSS}, as are defined in Fig. A.2. In order to balance the optimization of I_N and E_{LOSS}, the object function, f_{OBJECT}, to be minimized is chosen to be $I_N \cdot (E_{LOSS})^a$ (a=0.6). The constant a=0.6 was heuristically set so that the weights of I_N and E_{LOSS} are equal in the search. First, a PC randomly generates a new trial waveform, that is, a new waveform vector (n1…n8) using MATLAB and sends control signals to the gate driver through LabVIEW, and then the digital oscilloscope receives measured voltage and current from the board and sends the digital data to the PC. Depending on the measured value of f_{OBJECT}, the PC generates the next trial waveform according to the SA algorithm. The optimization iterations continue until no gain in observed.

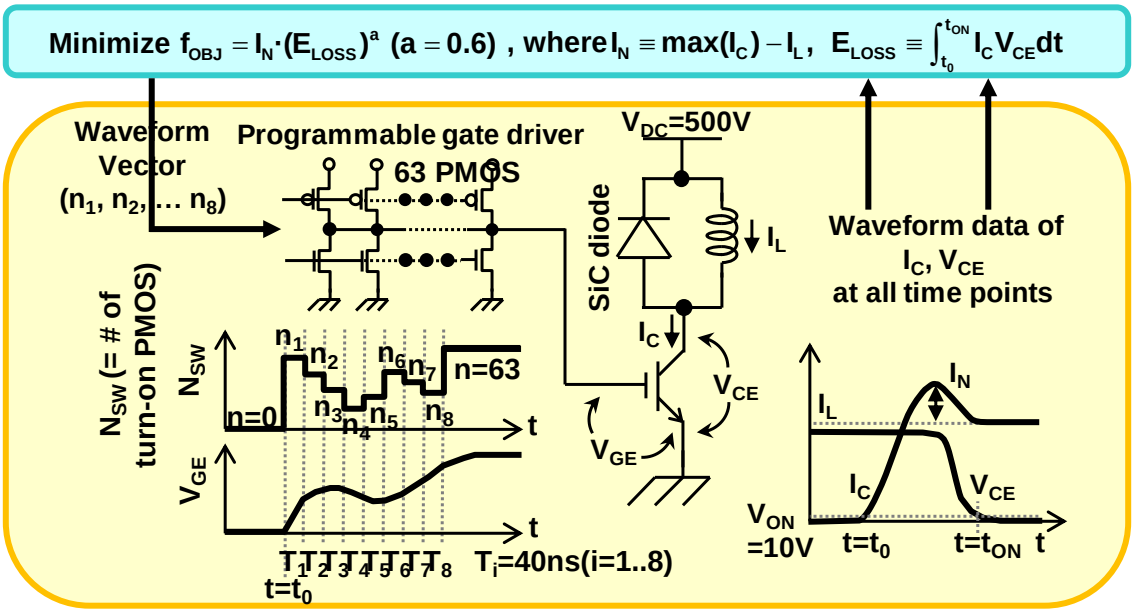


Fig. A.2 System setup for automatic optimization with different f_{OBJECT} used in Chapter 3.

Fig. A.3 shows I_N and E_{LOSS} history during the optimization process. f_{OBJECT} is successfully optimized to about a half from the start point to the end point where the optimization is completed. One physical measurement of about 2 seconds is needed in one SA iteration loop and thus to complete the optimization, it takes about an hour. No destructive breakdown of power devices was observed in the optimization process. In Fig. A.5, a I_N – E_{LOSS} trajectory during the optimization is shown. The optimized point is better than that by human search in terms of both I_N and E_{LOSS}. The measured waveforms of the start point and the end point are shown in Fig. A.5. Fig. A.6 shows three trial results. All the trials successfully found the optimized points. It is also shown that a greedy algorithm fails, which indicates that f_{OBJECT} has multiple local minima.

Optimal search is also possible with this object function. But compared to the result in Chapter 3, the search points vary for each trial. It can be considered that this is because an objective function that depicts a downwardly convex contour line is set for the downward convex trade-off characteristic. In order to avoid variation of the search points for each trial,

it is considered good to set an upwardly convex object function as used in Chapter 3. Depending on applications, it is conceivable that the object function sets a threshold value for the loss or the overshoot that should not be exceeded. It is appropriate to use an object function that is convex, and in some cases a threshold value is provided.

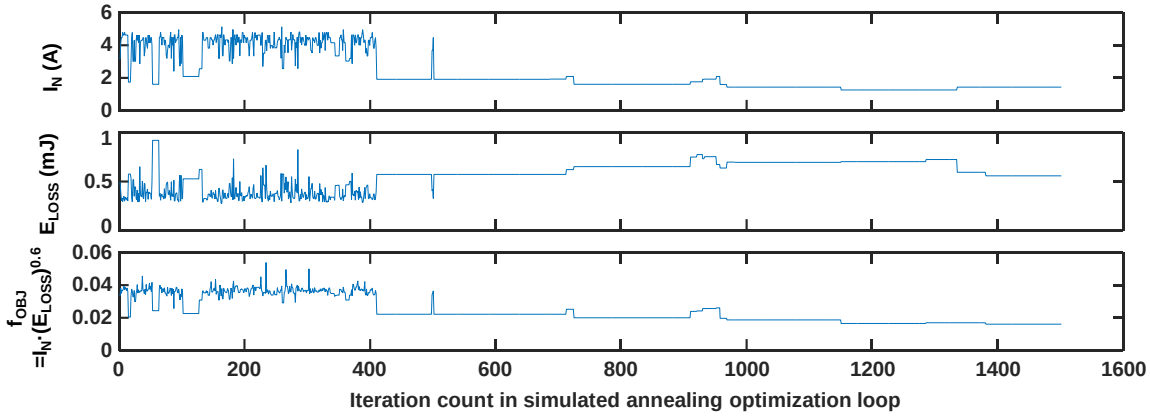


Fig. A.3 History plots of I_N, E_{LOSS} and f_{OBJECT} during optimization process for turn-on.

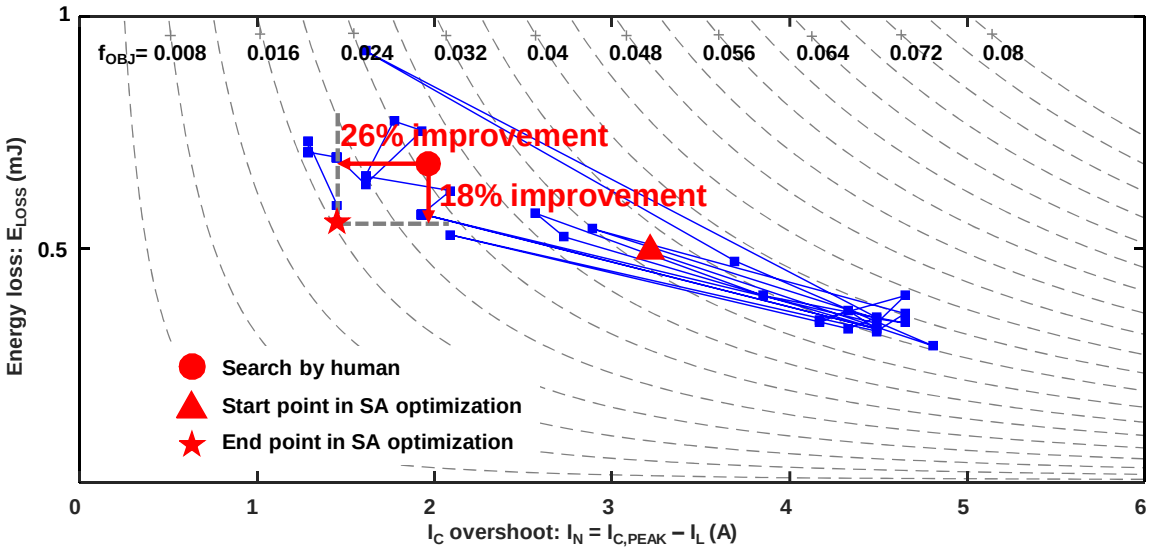


Fig. A.4 I_N – E_{LOSS} trajectory during SA optimization. 26% I_N reduction and 18% ELOSS reduction were achieved using automatic SA optimization over rigorous manual optimization by human.

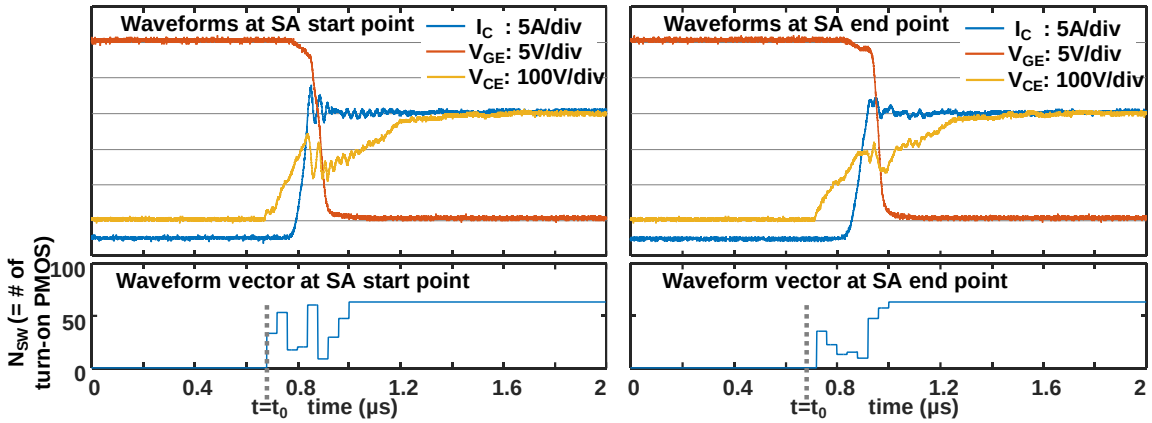


Fig. A.5 Measured waveforms at (a) start point and (b) end point of SA optimization for Si-IGBT and SiC-diode turn-on case.

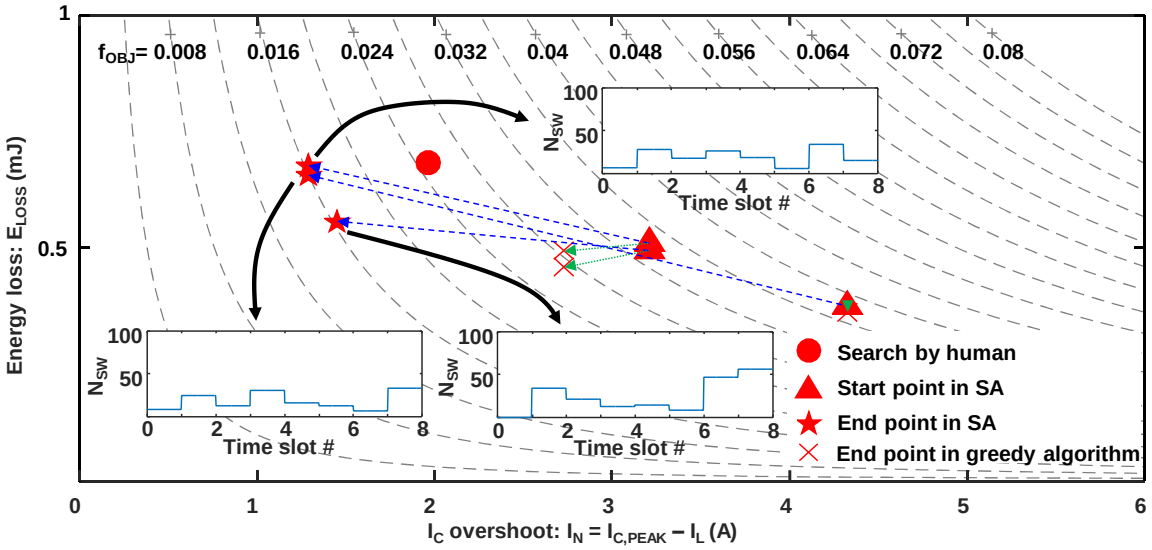


Fig. A.6 I_N – E_{LOSS} trajectory during three optimization runs. Optimized points show about the same f_{OBJECT} but optimized gate waveforms are different. Greedy algorithm fails to optimize.

List of Publications and Presentations

Publications in journals and transactions

1. K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, T. Sakurai, “General-Purpose Clocked Gate Driver IC with Programmable 63-Level Drivability to Optimize Overshoot and EnergyLoss in Switching by Simulated Annealing Algorithm,” IEEE Transactions on Industry Applications, accepted.

Publications in international conferences

1. K. Miyazaki, S. Abe, M. Tsukuda, I. Omura, K. Wada, M. Takamiya, and T. Sakurai, “General-Purpose Clocked Gate Driver (CGD) IC with Programmable 63-Level Drivability to Reduce Ic Overshoot and Switching Loss of Various Power Transistors,” IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, USA, pp. 1640 -1645, March 2016.

2. K. Miyazaki, M. Takamiya, and T. Sakurai, “Automatic Optimization of IGBT Gate Driving Waveform Using Simulated Annealing for Programmable Gate Driver IC,” IEEE Energy Conversion Congress & Exposition (ECCE), Milwaukee, USA, pp. 1 -6, Sep. 2016.
3. K. Miyazaki, Ichiro Omura, M. Takamiya, and T. Sakurai, “20-ns Short-Circuit Detection Scheme with High Variation-Tolerance based on Analog Delay Multiplier Circuit for Advanced IGBTs,” IEEE Southern Power Electronics Conference (SPEC), Auckland, New Zealand, pp. 1 -4, Dec. 2016.
4. H. Obara, K. Miyazaki, M. Takamiya, T. Sakurai, K. Wada, “Active Gate Control in Half-Bridge Inverters Using Programmable Gate Driver ICs to Improve both Surge Voltage and Switching Loss,” IEEE Appl. Power Electron. Conf. and Expo., Mar. 2017, to be presented.

Domestic conferences and workshops

1. 崔　通，宮崎耕太郎，安部征哉，附田正則，大村一郎，小原秀嶺，和田圭二，高宮　真，桜井貴康, “ディジタルゲート駆動 IC を用いた IGBT のスイッチング時における損失とオーバーシュートの自動最適化,” 電気学会，電子デバイス・半導体電力変換合同研究会，電気学会研究会資料，SPC-16-153，pp. 19-24，北九州，2016 年 11 月.
2. 小原秀嶺，和田圭二，宮崎耕太郎，高宮　真，桜井貴康，“プログラマブルゲートドライバ IC を用いた負荷電流フィードバックアクティブゲート制御,” 平成 28 年電気学会産業応用部門大会，1-39，pp. 127-130，群馬，2016 年 8 月.

Patents

1. 宮﨑　耕太郎, 高宮　真, 桜井　貴康, “短絡検出装置および短絡検出方法,” 特願 2016-02808, 2016 年 2 月 12 日出願.
2. 宮﨑　耕太郎, 高宮　真, 桜井　貴康, “ゲート駆動装置,” 特願 2016-014404, 2016 年 1 月 28 日出願.

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