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その他のタイトル	サブ0.3V動作超低消費電力MOSFETのデバイス設計指針に関する研究
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論 文 の 内 容 の 要 旨

論文題目 Study on Device Design Guideline　for Ultra-Low Power MOSFETs in Sub-0.3 V Operation

(サブ0.3V動作超低消費電力MOSFETのデバイス設計指針に関する研究)

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The mobile applications with the internet of things (IoT) features become more widespread in our lives due to people's pursuit of convenience. Such portable electronic devices require ultra low power consumption and even batteryless system. The low power technology can play an important role in addressing the issue of power and energy consumption. The most simplest and effective way to reduce power consumption of very large scale integration (VLSI) systems is supply voltage (V_{dd}) scaling. Meanwhile, the characteristics of VLSI in scaled V_{dd} are very sensitive to device variation. Therefore, it is highly required to carefully design the devices which operate in scaled V_{dd}.

In this study, the device design guideline for ultra-low power metal-oxide semiconductor field-effect-transistors (MOSFETs) in sub-0.3 V operation is proposed. The two main purposes of this study are to realize complementary MOS (CMOS) logic circuits and static random access memory (SRAM) cells for sub-0.3 V operation. The two major parts of this thesis are considered and achieved from all viewpoints of such as measurements, simulation, calculation, and fabrication.

The first half of the thesis deals with the effects of drain-induced barrier lowering (DIBL) on subthreshold devices. Even if there are lots of previous works which have studied to improve subthreshold properties for low power operation, so far, very little attention has been paid to the DIBL effects on CMOS logic circuits, especially in subthreshold region. 1k nMOSFETs are measured and analyzed in terms of DIBL effects on actual devices. From measured results, a device with large DIBL shows severe performance degradation particularly in subthreshold region compared with a device with small DIBL. Moreover, in order to investigate DIBL effects on CMOS logic circuits, CMOS ring oscillators with various DIBL values are assumed by simulation. The large DIBL devices show more current and delay degradation because effective current (I_{eff}) or peak trajectory current is degraded by DIBL despite of the same current (I_{on}). Additionally, the degradation becomes even more serious in subthreshold region. As a result, the energy consumption becomes

increasingly larger with DIBL increase in subthreshold region in spite of reduction in power consumption by V_{dd} scaling. In order to improve energy efficiency, steep S-factor transistors are an excellent candidate because of their superior subthreshold characteristics. In spite of that, steep S-factor transistors show increase of energy consumption by 'threshold voltage (V_{th}) shift by drain voltage (V_{ds}) or η factor' which is similar to DIBL in conventional MOSFETs.

The rest of half of this study suggests a new operation mechanism, V_{th} self-adjustment, for sub-0.3 V operation even enhancing stability of SRAM cells. V_{th} self-adjusting MOSFETs show two kinds of V_{th} states in dynamic characteristics, while they show improved on/off current ratio and S-factor in static characteristics by time-lag of tunneling phenomenon. The V_{th} shift in dynamic characteristics can be used for enhancing stability of SRAM cells. Furthermore, improved on/off current ratio and S-factor are suitable for low voltage operation. However, V_{th} self-adjusting MOSFETs with planar structure show crucial short channel effects due to limitation of vertical scaling. Thus, gate-all-around (GAA) nanowire structure is introduced to V_{th} self-adjusting MOSFETs for strong immunity to short channel effects. In order to enhance V_{th} self-adjusting characteristics, the GAA nanowire structure is modified through enlarged body factor difference between dynamic and static characteristics. Hence, V_{th} shift and S-factor improvement become enhanced. Also, tri-gate nanowire MOSFETs with floating gates are successfully fabricated and they show excellent device performance. Finally, they show V_{th} self-adjusting characteristics even in ultra-low V_{dd} and these results are recomposed to 6 transistors (6T) SRAM cells using simulation. The 6T SRAM cells with V_{th} self-adjustment clearly show stability improvement at V_{dd} = 0.1 V.

This paper has argued the device design for ultra-low voltage operation. The results of this investigation show that it is important to suppress DIBL for CMOS logic circuits and V_{th} self-adjusting MOSFETs are very promising for low power operation, furthermore enhancing stability of SRAM cells.