Study on Ge CMOS Photonics Platform using Ge-on-Insulator Substrate

博士論文（要約）

Study on Ge CMOS Photonics Platform using Ge-on-Insulator Substrate

(Ge-on-Insulator 基板を用いた Ge CMOS フォトニクスに関する研究)

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As a group IV element, Ge is of considerable interest for both electronics and photonics. Due to its high carrier mobility, Ge is perceived as a promising channel material for advanced complimentary metal-oxide-semiconductor (CMOS) technology to further enhance the device performance. On the other hand, Ge is also very useful for photonic applications due to its many attractive properties, especially in the near-infrared and mid-infrared wavelength region. At near-infrared wavelengths, Ge-based photonic devices including Ge lasers and EA modulators as well as Ge photodetectors (PDs) have been intensely investigated for Si photonics. At mid-infrared wavelengths, Ge shows great potential for various applications because of its high transparency, large free-carrier effects and thermo-optic effect, etc.

For these reasons, many efforts have been made to integrate Ge on Si-based platform to enable functionalities, which are mainly based on Ge epitaxial growth technology. However, integration of high-quality Ge layer on Si through epitaxial growth has been found quite challenging because of a large lattice mismatch between Ge and Si, which causes high density of dislocation defects at the Ge/Si interface and in Ge layer, leading to a poor Ge crystal quality.

To realize a high-quality Ge thin film on Si platform, wafer bonding is also a very promising approach. By transferring Ge onto Si from a bulk Ge donor wafer, wafer bonding provides the possibility of achieving high-quality Ge integration with Si. Through wafer bonding with an insulating intermediate layer, crystal defects due to the lattice mismatch between Ge and Si can be avoided, and Ge-on-insulator (GeOI) structure is obtained.

In this dissertation, we propose a Ge CMOS photonics platform using a novel GeOI structure, which can utilize many useful optical properties in Ge for integrated

photonics applications, enable monolithic integration with high performance Ge-based electronics and meanwhile offer strong compatibility to modern Si CMOS technologies.

For the realization of Ge CMOS photonics platform, we have developed the fabrication process of GeOI wafer by combining wafer bonding and ion cut technology. In addition, we have systematically studied the effect of thermal annealing on the GeOI properties in terms of Ge crystal quality, surface morphology, and electrical properties. Under an optimal process condition, high-quality GeOI wafer exhibiting Ge crystal quality comparable with bulk Ge is successfully fabricated. By using a thick buried oxide layer in the GeOI wafer, strong two-dimensional optical confinement is achieved in the GeOI structure, benefiting various photonic device applications.

To achieve a low-dark-current operation in Ge PD, we have explored the effect of surface passivation on the dark current suppression by using a thin GeO_x layer generated from oxygen plasma exposure and have investigated the physics inside surface leakage of Ge metal-semiconductor-metal PD. Reduction of dark current by over one order of magnitude is achieved in fabricated device, mainly attributed to the decrease in the surface leakage current owing to a superior GeO_x/Ge interface. An accumulation condition of the Ge surface which is originated from fixed charges inside the passivation layer is also found helpful to suppress the surface leakage current. We demonstrate that GeO_x passivation is an effective method for dark-current suppression in Ge PDs.

Based on the understanding of surface passivation, we have achieved a high performance Ge rib waveguide PD showing low-dark-current and high-responsivity on the GeOI wafer. We have also investigated transmission properties in amorphous Si (a-Si) and demonstrate Ge PD monolithically integrated with a-Si passive waveguides

on the GeOI substrate as a proof-of-concept of Ge/a-Si hybrid photonic integrated circuit platform.

To apply Ge CMOS photonics platform for mid-infrared (MIR) integrated photonics. We have studied the design methodology of Ge strip waveguide based passive components including single-mode waveguides, grating couplers, MMI couplers, and micro-ring resonators on the GeOI wafer at the 2-μm band. We have discussed the propagation loss reduction of Ge waveguide and have also studied the thermo-optic effect in Ge strip waveguide by using Ge micro-ring resonators.

Based on the study above, we have proposed a Ge MIR integrated photonics platform on the GeOI substrate. In conjunction with the passive building blocks presented before, we demonstrate Ge-based MIR active device, i.e. performing numerical simulation on a carrier injection Ge optical modulator based on free-carrier absorption in Ge and realizing the designed device as a Ge variable optical attenuator on the GeOI substrate. Furthermore, we have also analyzed the issue in fabricated modulator device and discuss the process optimization approaches for further performance enhancement.

Summarizing all the achievements, we conclude that Ge CMOS photonics platform using the high-quality GeOI substrate is very promising for integrated photonics in the near future.