Growth and characterization of Scandate insulator films for oxide field-effect devices
酸化物電界効果デバイスの作製に向けたスカンジウム酸化物絶縁膜の成長と評価

Lippmaa lab. 46111 Takayuki Uozumi

Introduction

Recently, oxides for electronic applications have been widely studied because of the interesting physical properties, e.g. high-temperature superconductivity, colossal magnetoresistance, etc. Many potentially interesting oxide applications are based on heteroepitaxial thin films. However, oxide hetero-interfaces have many unsolved problems, like non-stoichiometry, charge transfer, changes in the electronic states at surfaces and interfaces, etc. A field-effect transistor (FET) is a useful structure for studying the electronic properties of heterointerfaces. Moreover, FETs can be used for carrier doping of transition metal oxides by field effect. Although chemical impurity doping is commonly used to control the carrier concentration, this technique also causes lattice distortions. Therefore, fabrication of a field-effect transistor based on transition metal oxides is very interesting.

FETs have been fabricated using commercial $SrTiO_3$ (STO) single crystal substrates [1]. Atomically flat substrate surface was used as a channel layer. Amorphous $CaHfO_3$ (CHO) thin film was used as the gate insulator layer. The transistor on/off ratio was more than 10^5. It is known that the mobility of carriers in a STO single crystal increases, as the temperature decreases. Therefore, the transistor action can be expected to improve at low temperature. The field effect mobility of the CHO devices, however, was found not to depend on temperature. This behavior can be understood by assuming the presence of interface states that suppress carrier mobility and degrade the properties of the field effect transistor. To avoid this, an epitaxial CHO/STO hetero-interface was used to reduce the density of interface states. Unfortunately, epitaxial CHO thin films form a grain structure due to misfit after an initial growth of ≈10 monolayers, degrading the breakdown properties of the gate insulator because of leak current at grain boundaries. STO based FETs using 4 unit cells of epitaxial and several tens of nanometers of amorphous CHO were fabricated, and showed metallic behavior at low temperature. However, in this structure, trapping states still exist. One solution to reduce interface state density is to use a single thick epitaxial layer.

In this work, wide-gap insulators, $DyScO_3$ and $NdGaO_3$, which have smaller lattice mismatch with STO than CHO (Table.1) were grown on STO substrates and characterized in terms of their insulating properties. $DyScO_3$ (DSO) grew epitaxialy on STO (100) substrate and showed good insulating behavior. It may therefore be possible to use a thicker epitaxial layer as a gate insulator for STO-based FETs.

material	Lattice constant (Å)	mismatch
$SrTiO_3$	3.905 (cubic)	-
$CaHfO_3$	3.993 (psudo-cubic)	2.24 %
$NdGaO_3$	3.860 (psudo-cubic)	-1.17 %
$DyScO_3$	3.944 (psudo-cubic)	0.99 %

Table.1. Lattice constants of insulators

Experimental

DSO film growth was done by Pulsed Laser Deposition (PLD). PLD is widely used for oxide thin film fabrication, and one of the best methods

to obtain high-quality oxide thin films.

DSO films were fabricated on non-doped STO (100) substrates. The growth temperature and oxygen partial pressure were varied from 600 to 1000 °C, and from 10^{-5} to 10^{-1} Torr, respectively. The film thickness was fixed at 80 nm and the laser fluence was 0.8 J/cm^2. DSO films grown on STO substrates were used to measured the surface morphology and crystallinity. The surface morphology was evaluated by Atomic Force Microscopy (AFM), and crystallinity was characterized by X-ray diffraction (XRD) 2θ-θ scans.

Additionally, films with various thicknesses (5, 10, 20, 40, and 80 nm) were grown on conducting Nb:STO substrates to measure breakdown fields and dielectric properties. After film fabrication, annealing treatments were done to compensate for the oxygen vacancies formed during film growth. 50-100 Aluminum pads (Φ ~ 0.2 mm) were evaporated in vacuum on both film and the metallic substrate for breakdown field measurements. Similar samples were fabricated using 0.6 mm square Al pads for capacitance measurements.

FETs were fabricated using epitaxial and amorphous DSO films. The fabrication process is as follows; (i) Amorphous STO (4 u.c.) / LTO (5 u.c.) films were deposited on a STO substrate at room temperature through a metal mask to form the source and drain electrodes. (ii) Films were annealed in a chamber to obtain metallic source and drain electrodes by diffusion of La and Sr. (iii) Epitaxial DSO film was deposited. (iv) Annealed in furnace. (v) Amorphous DSO film deposition. (vi) Annealed in furnace. (vii) Al gate electrode evaporation.

Results and discussion

DSO films on STO (100) substrates grew epitaxialy under all conditions mentioned above. A typical XRD 2θ-θ scan of DSO/STO grown at 700 °C, 1 mTorr is shown in Fig.1.

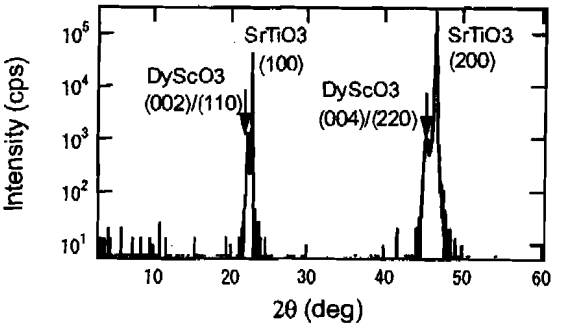

Fig.1. XRD 2θ-θ scan of a DSO film on STO (100) grown at 700 °C, 1 mTorr.

As the growth temperature increased, the out-of-plane axis length relaxed and the FWHM (full width at half maximum) of the rocking curve of the film peak became sharper. Surface roughness increased with the growth temperature. These results indicate that grains in the film grow larger at higher growth temperature, improving crystallinity at the cost of a rougher surface.

The effect of the oxygen partial pressure on film growth was studied similarly. The surface roughness and the FWHM of the film peak rocking curve started to increase above 10 mTorr. From the above mentioned results, 700 °C and 1 mTorr were selected as the optimum growth conditions.

In order to compare the performance of DSO and CHO films, a series of films with various thicknesses were grown on Nb:STO substrates.

RHEED oscillation during DSO film growth continued for about 30 periods, while only 10 oscillations were observed in the CHO case. The average breakdown fields of these films for each film thickness are shown in Fig.2. The low average breakdown field of 50 nm-thick DSO film may be due to tunneling currents.

The insulating properties of DSO are clearly superior to CHO, as shown in Fig.2. It can be concluded that epitaxial DSO films are promising for use as gate insulator layer.

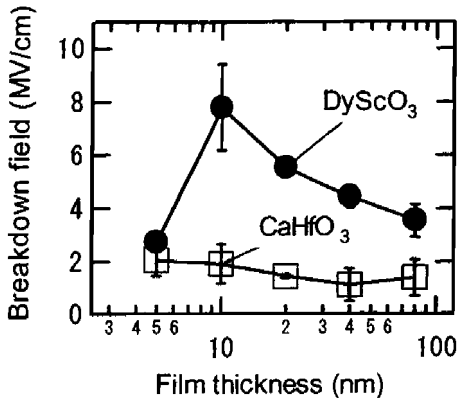

Fig.2. Average breakdown field of DSO and CHO films for various film structure.

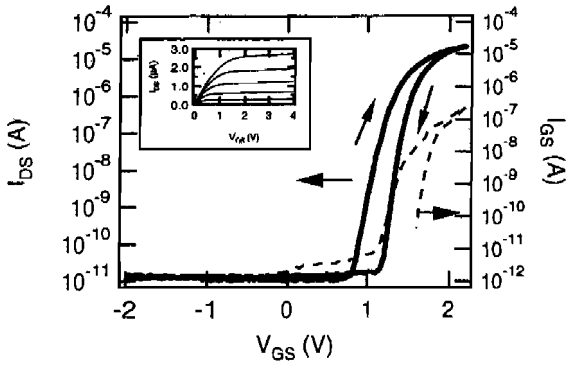

Fig.3. Drain-source current, I_{DS} (solid line), and gate leak current, I_{GS} (dashed line), as a function of gate-source bias (V_{GS}) at 50 K. Inset: I_{DS} vs. V_{DS}, at fixed V_{GS}=0, 0.25, 0.5, 0.75, and 1 V.

STO-based FETs using epitaxial DSO layers were fabricated. 10 unit cells (4 nm) of epitaxial and about 90 nm-thick amorphous DSO were used. The breakdown field of the gate layer in DSO FETs was found to be very low. As mentioned above, a LTO layer was used as source and drain electrodes. It was found that nano-pillar structures form on the surface after annealing treatment. These nano-pillars can be leak sources and as a result, breakdown field was suppressed in the FET structure.

The Drain-source current, I_{DS}, is plotted as a function of Drain-source bias, V_{DS}, at a fixed gate-source bias, V_{GS}, in the inset of Fig.3. I_{DS} is plotted as a function of V_{GS} in Fig.3 with V_{DS} = 0.5 V, which is in the linear region of the I_{DS}-V_{DS} curve. This transistor showed normally on type action at room temperature. At 50 K, the on-off ratio was about 10^6 and the field-effect mobility was 7.4 cm^2/V s. As shown in Fig.3, hysteresis was observed in the I_{DS}-V_{GS} curve. This behavior suggests that the carriers were trapped by interface states.

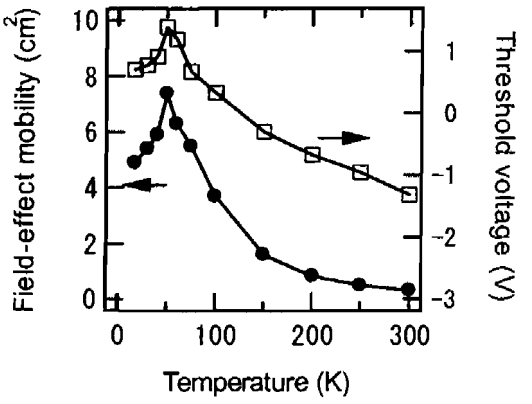

Fig.4. Field-effect mobility (filled circle) and threshold bias (open square) changes were plotted as a function of temperature.

Transistor action was measured at low temperature. The field-effect mobility and threshold bias shift are plotted in Fig.4. This FET showed the metallic behavior, and carrier doping to non-doped STO was observed by electric field-effect. However, the field-effect mobility dropped below 50 K suggesting that interface states still exist at the epitaxial insulator interface or in the insulator layer.

Reference

[1] K. Shibuya et al., Appl. Phys. Lett. **85**, 425 (2004)