4 Wide-gap insulator fabrication

4.1 Introduction

$SrTiO_3$ (STO) based FETs using epitaxial $CaHfO_3$ (CHO) gate insulator have been fabricated and studied the electrical properties of their hetero-interface. Unfortunately, epitaxial CHO thin film forms the grain structure due to the misfit after initial 10 monolayer growth, then the properties as a gate insulator degrades due to breakdown at grain boundaries.

Instead of CHO, wide-gap insulators that have smaller lattice mismatch with STO than CHO, were investigated. It have been already studied that $CaZrO_3$, $LaGaO_3$, $NdGaO_3$[1]. In this study, the candidate materials are $NdGaO_3$ (NGO) and $DyScO_3$ (DSO). The lattice constant table is shown in table.1. It is reported that these two materials grow epitaxialy on STO (100) single crystal substrates, respectively [2],[3]. The band gap width of epitaxial DSO film on $BaTiO_3$ (10 nm)/MgO is also reported as 5.8 eV. Indeed, DSO film is studying for high-k gate material of Si devices [4],[5].

	Lattice constants (Å)					
STO (cubic)	3.905	3.905	3.905			
	a	b	c	psudo-cubic ($\sqrt{a^2+b^2}/2$, c/2)		
CHO [6] (orthorhombic)	5.719	7.892	5.578	3.994 2.28%	3.941 0.922%	average mismatch 1.6%
NGO [7] (orthorhombic)	5.431	5.499	7.710	3.864 -1.05%	3.855 -1.28%	 -1.2%
DSO [8] (orthorhombic)	5.440	5.713	7.887	3.944 0.999%	3.943 0.973%	 0.99%

Table 1: Lattice constant of STO , CHO and wide-gap insulators, NGO and DSO, were listed. The psudo-cubic lattice constant and the lattice mismatch of insulators with STO are also shown.

4.2 Fabrication and characterization of $NdGaO_3$ film

4.2.1 Surface roughness and crystallinity

NGO films were grown on $SrTiO_3$ (100) single crystal substrates. STO is one of the most popular oxide substrate. A perfect TiO_2 termination with molecular step-and-terrace surface can be obtained by NH_4F-HF (BHF) etching a polished substrate [9]. The atomically flat STO substrates were obtained from Shinkosha Co., Ltd. NGO single crystal substrate was used as an ablation target for film growth.

It is reported that NGO film grow epitaxialy on STO (100) substrate in relatively high oxygen partial pressure by RF magnetron sputtering [3]. Then, NGO films were grown in 700-1000 °C at 10 mTorr oxygen partial pressure, and 10^{-5} - 10^{-1} Torr at 700°C. The laser fluence was about 0.6 J/cm^2, and resulting in the growth rate of about 20 pulses per monolayer. It can be thought that the growth rate is relatively high due to the high sintered density of single crystal ablation target. About 80 nm thick samples were fabricated to investigate the crystallinity and surface roughness of temperature and oxygen partial pressure dependence.

A typical RHEED pattern which was grown in 700 °C, 1 mTorr oxygen partial pressure, is shown in Fig.20(a). This spotty pattern indicates the very rough surface structure. The RHEED oscillation is shown in Fig. 20(b). Oscillations continued initial only few monolayer growth. XRD 2θ - θ scan of the same sample is shown in Fig.20(c). This NGO film was polycrystalline. Temperature dependence samples from 700 °C to 1000 °C at 10 mTorr oxygen were fabricated, however, single phase sample could not be obtained. The AFM image of these samples were shown in Fig.21. Grain size became larger with higher growth temperature. This result reflects that grain grow larger at higher growth temperature, as a result, the each large grain make the crystallinity better, on the other hand, the surface become rougher. Multi-domain structure can be observed on the sample surface in Fig.21. Oxygen partial pressure dependence samples from10^{-5} to 10^{-1} at 700 °C did not show single phase NGO film, too. The AFM image of these samples were shown in Fig. 22. The grain structure of the surface dramatically changed above 10 mTorr, because the condition is too far from laser MBE condition.

In summary, in these conditions, epitaxial NGO film on STO substrate could not be obtained. The obtained sample surface is very rough, and nice insulating property can not be expected.

To obtain a film that have more flat surface, thinner NGO films were fabricated. 5 nm thick NGO films were grown at from 700 to 900 °C in 10^{-5}, and 10^{-3} Torr oxygen ambient. The AFM images of 5 nm thick samples were shown in Fig.23. As the temperature and oxygen partial pressure increased, the grains grew larger as described above. From the view point of device application, the grain size should be suppressed to prevent the leak

current flowing the grain boundaries, therefore, lower temperature, 700 °C, is suitable.

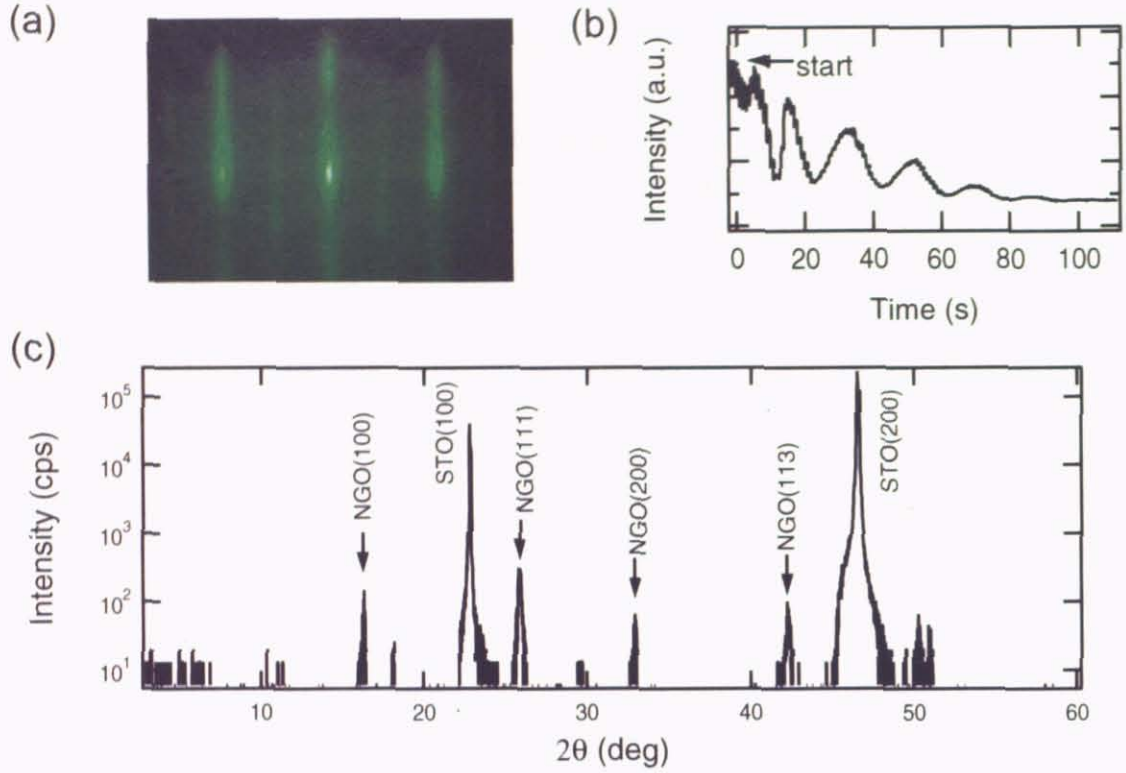

Figure 20: (a) Typical RHEED pattern of NGO film on STO substrate. (b) RHEED oscillation observed during NGO film growth at 700 °C, 1 mTorr. (c) XRD 2θ-θ scan of NGO film grown at 700 °C, 1 mTorr.

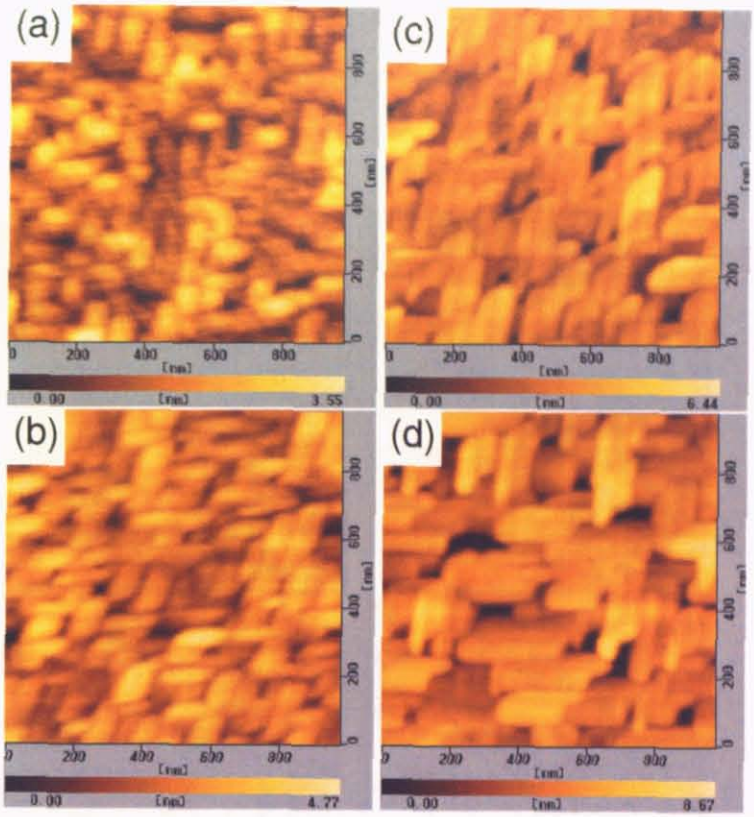

Figure 21: AFM image of NGO film surface grown at (a)700 °C, (b)800 °C, (c)900 °C, (d)1000 °C. These AFM images size are 1 μm × 1 μm.

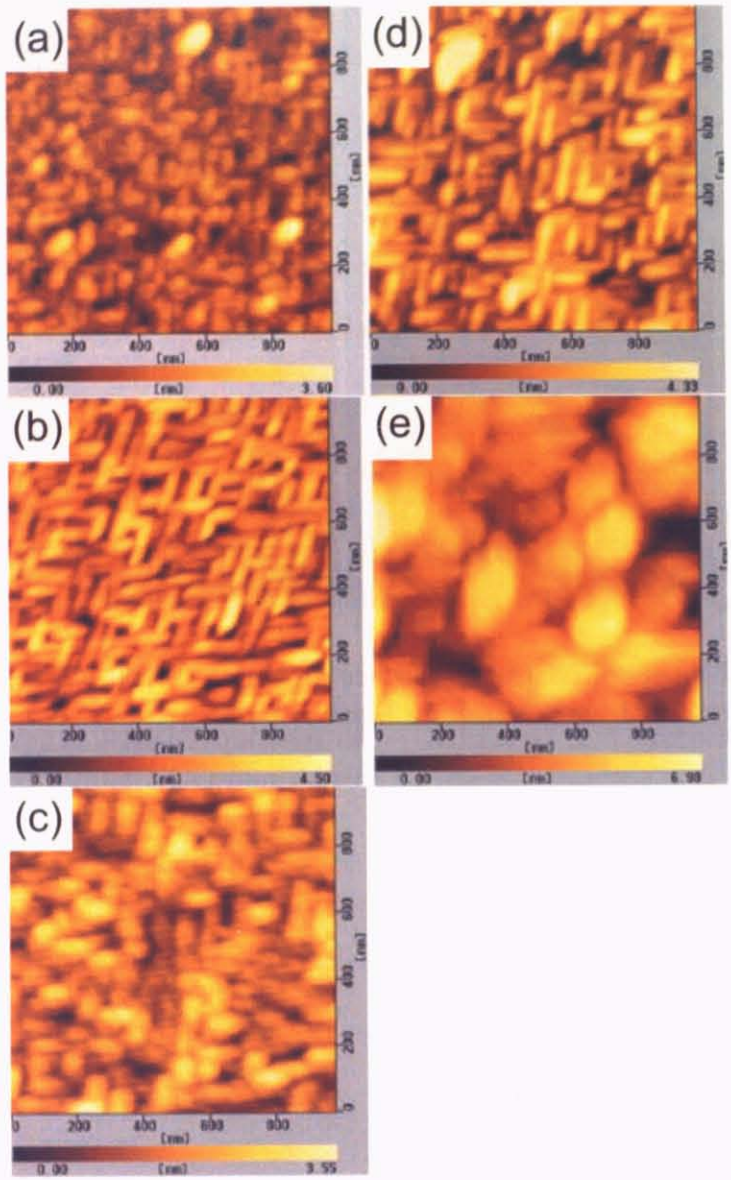

Figure 22: AFM image of NGO film surface grown at (a)10^{-5}, (b)10^{-4}, (c)10^{-3}, (d)10^{-2}, (e)10^{-1} Torr oxygen partial pressure. These AFM images size are 1 μm $\times$ 1 μm.

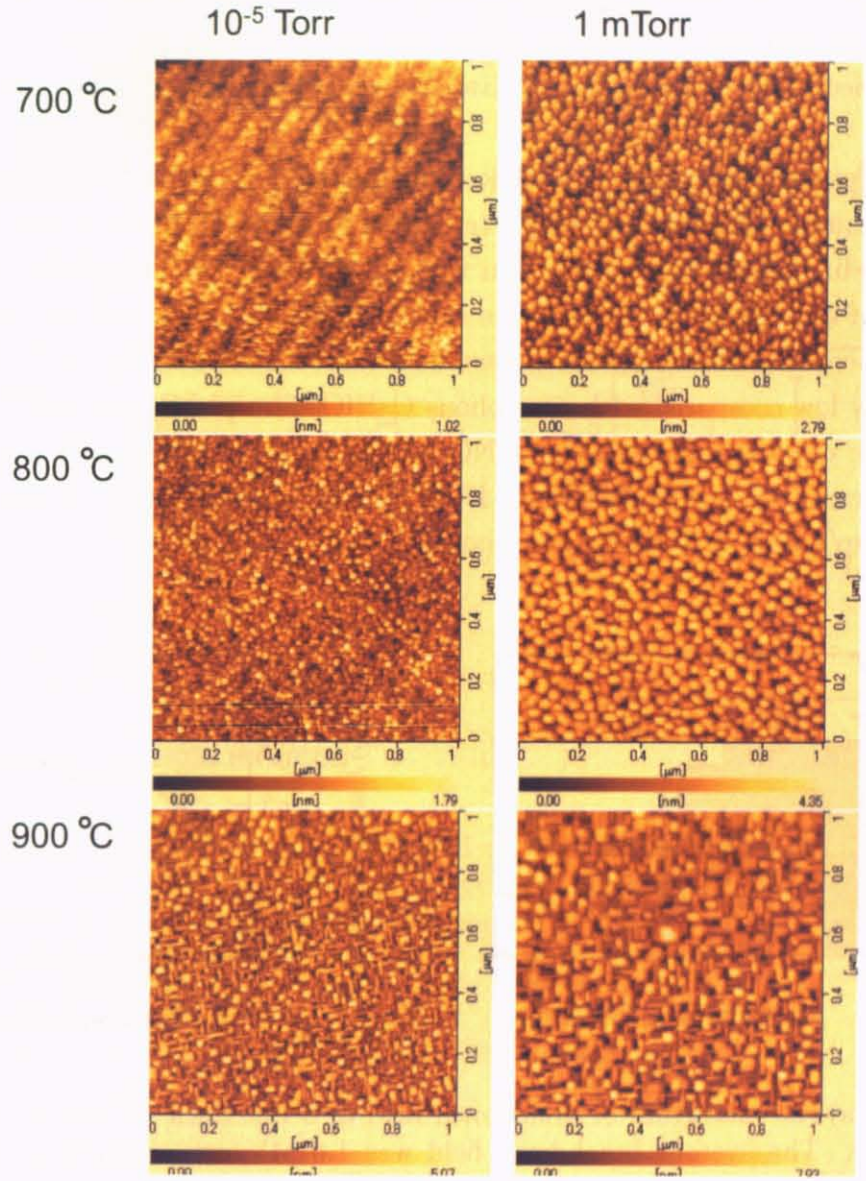

Figure 23: AFM image of 5 nm thick NGO film grown under various conditions. Step and terrace structure can be seen in 700 °C growth film. These AFM images size are 1 μm × 1 μm.

4.2.2 Electrical characterization

Breakdown field of 5nm thick NGO film grown at 700 °C in 1 mTorr oxygen partial pressure and 80 nm thick amorphous films grown in 1, 10, 100 mTorr on conducting Nb doped STO substrate were measured. After the deposition of NGO films on Nb:STO substrates and annealed in farness at 250 °C, 6 hours to compensate the oxygen vacancies in film, Al electrodes (0.2 mmϕ) were evaporated on both film and metallic substrate in vacuum.

The histogram of the value of breakdown field of 5 nm NGO film is shown in Fig.24(a). A typical example of breakdown characteristic of 5 nm NGO film is shown in Fig.24(b). The average breakdown field of this film was 1.3 MV/cm. The histograms of breakdown field value of amorphous NGO films are shown in Fig.25(a)-(c), and the oxygen partial pressure dependence of average breakdown field value is shown in Fig.25(d). These values are relatively low compared with amorphous $CaHfO_3$ film (5 MV/cm [12]).

Dielectric constants of amorphous NGO films were measured, and the values were about 20. Transmittance of amorphous NGO film on Al_2O_3 substrate is shown in Fig.26. The band gap width of NGO is more than 5 eV.

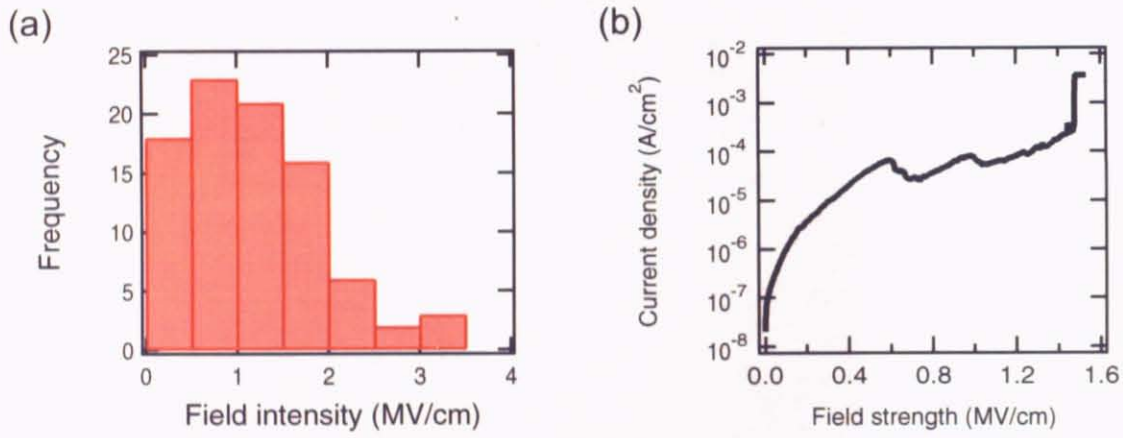

Figure 24: (a)The histogram of breakdown field of 5 nm thick NGO film grown at 700 °C, 1 mTorr. The average breakdown field was 1.6 MV/cm. (b)A typical example of breakdown charcteristic of NGO film.

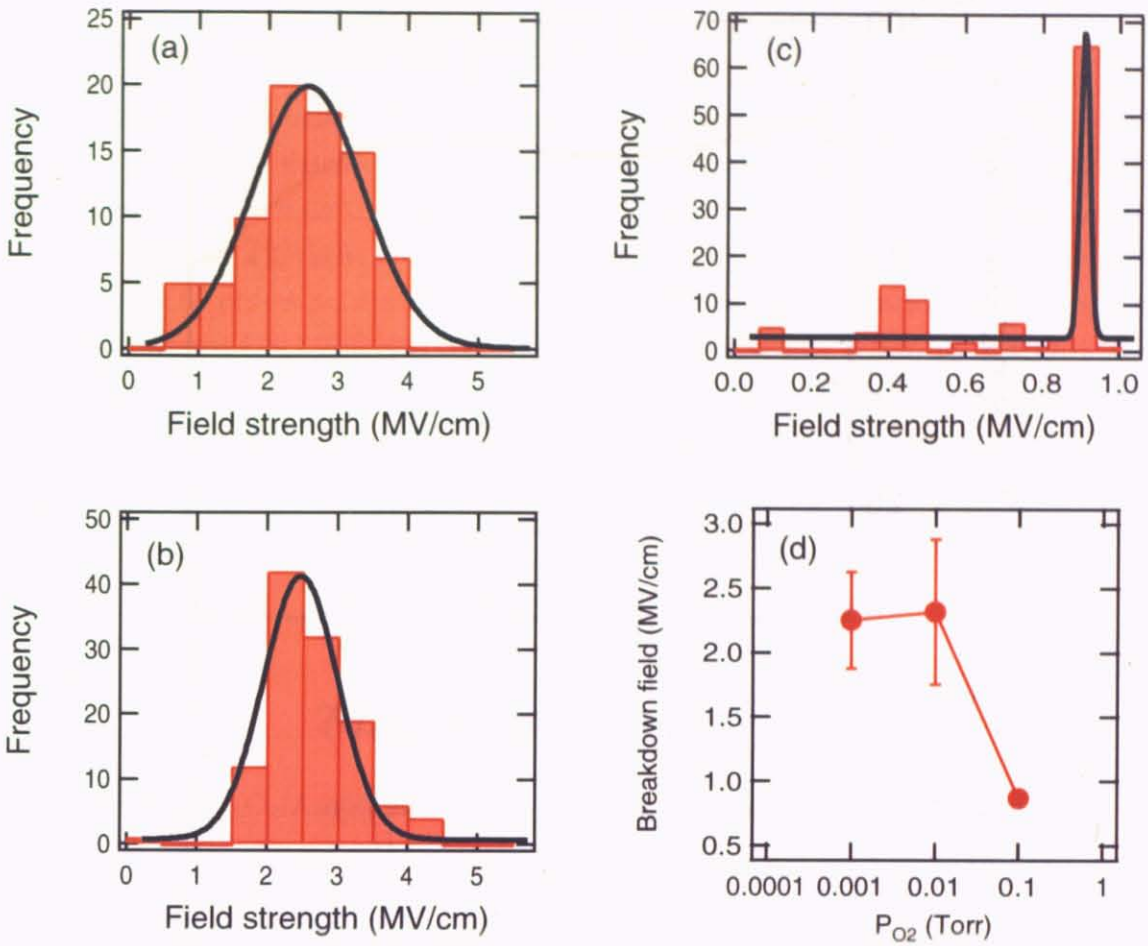

Figure 25: The histogram of breakdown field of amorphous NGO film, (a) grown at 1 mTorr, (b) 10 mTorr, and (c) 100 mTorr oxygen partial pressure. The values of average breakdown field at each oxygen pressure are shown in (d).

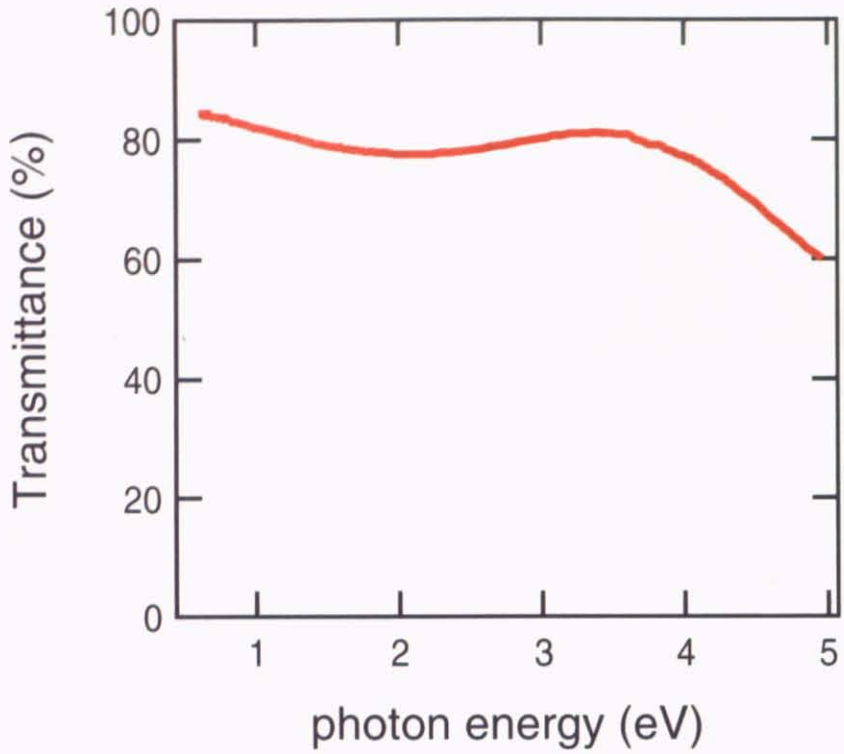

Figure 26: Transmittance of amorphous NGO film on Al_2O_3 substrate.

4.3 Fabrication and characterization of $DyScO_3$ film

4.3.1 Surface roughness and crystallinity

Polycrystalline DSO pellet (TOSHIMA Manufacturing Co., Ltd.) was used for ablation target. The sintered density was 3.68 g/cm^3, and this value is 53 % of the ideal density. DSO films were grown on the STO (100) single crystal substrates. Growth conditions are shown in Fig.27. The laser fluence was about 0.76 J/cm^2, and resulting in the growth rate of about 60 pulses per monolayer. To reduce the oxygen vacancies or other defects at interface between DSO film and STO single crystal substrate, relatively low growth rate was chosen. About 80 nm thick samples were fabricated to investigate the crystallinity and surface roughness of temperature and oxygen partial pressure dependence.

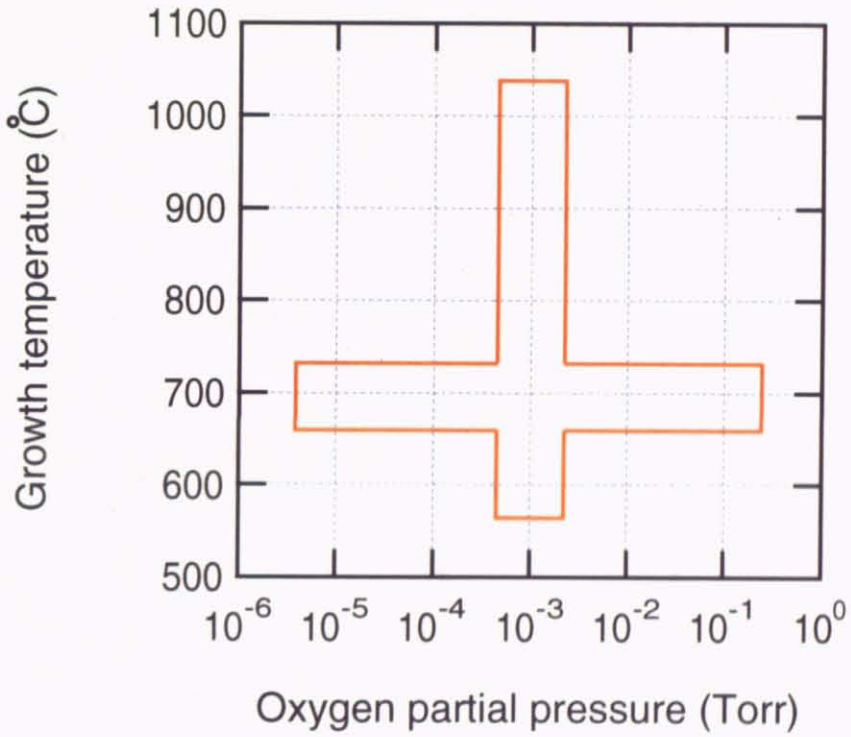

Figure 27: DSO films were fabricated at from 600 to 1000 °C, 1 mTorr, and from $10^{-5}$to 10^{-1} Torr , 700°C.

Firstly, typical examples of RHEED oscillation and pattern are shown in Fig.28. RHEED oscillation continued more than 30 periods shown in Fig.28(a), and the RHEED pattern after deposition (Fig.28(b)) shows the streaky pattern which indicate the relatively rough surface. A typical XRD pattern of 2θ-θ scan is shown in Fig.29. It is obvious that epitaxial DSO film could be obtained from Fig. 29(a). All DSO films fabricated in the conditions shown in Fig.27 grew epitaxialy.

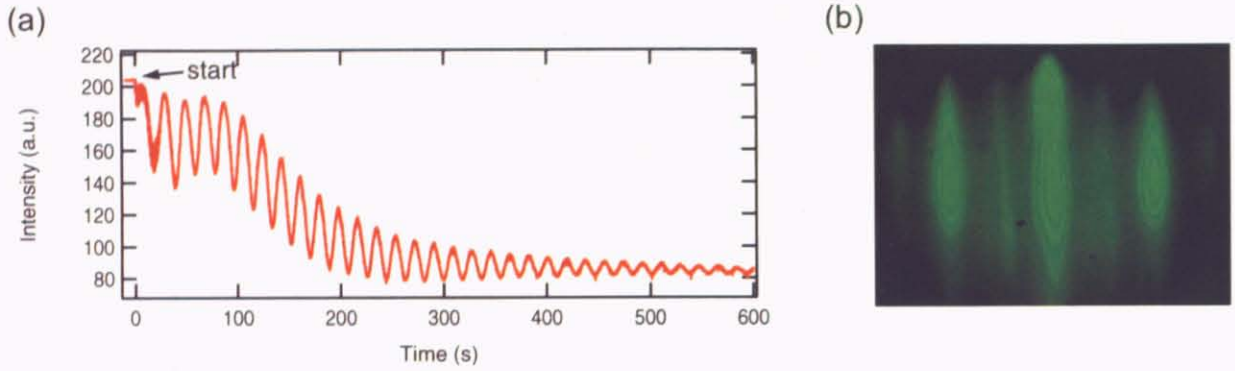

Figure 28: Typical RHEED (a) oscillation , (b) pattern of DSO film grown at 700 °C, 1 mTorr.

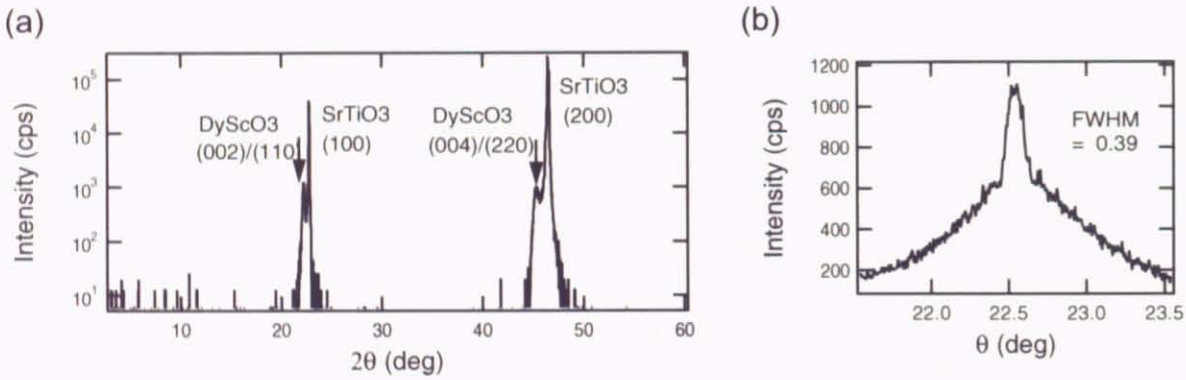

Figure 29: (a) XRD 2θ-θ scan and, (b) rocking curve of DSO film grown at 700 °C, 1 mTorr.

Surface morphology and crystallinity of temperature dependence have investigated. Fig.30 (a) - (d) shows the surface morphology of temperature dependence from 600 to 1000 °C, and the RMS (root mean square) of surface roughness were plotted in Fig.30(e) at each temperature. As shown in Fig.30(d), higher the growth temperature become, rougher the surface of the DSO film.

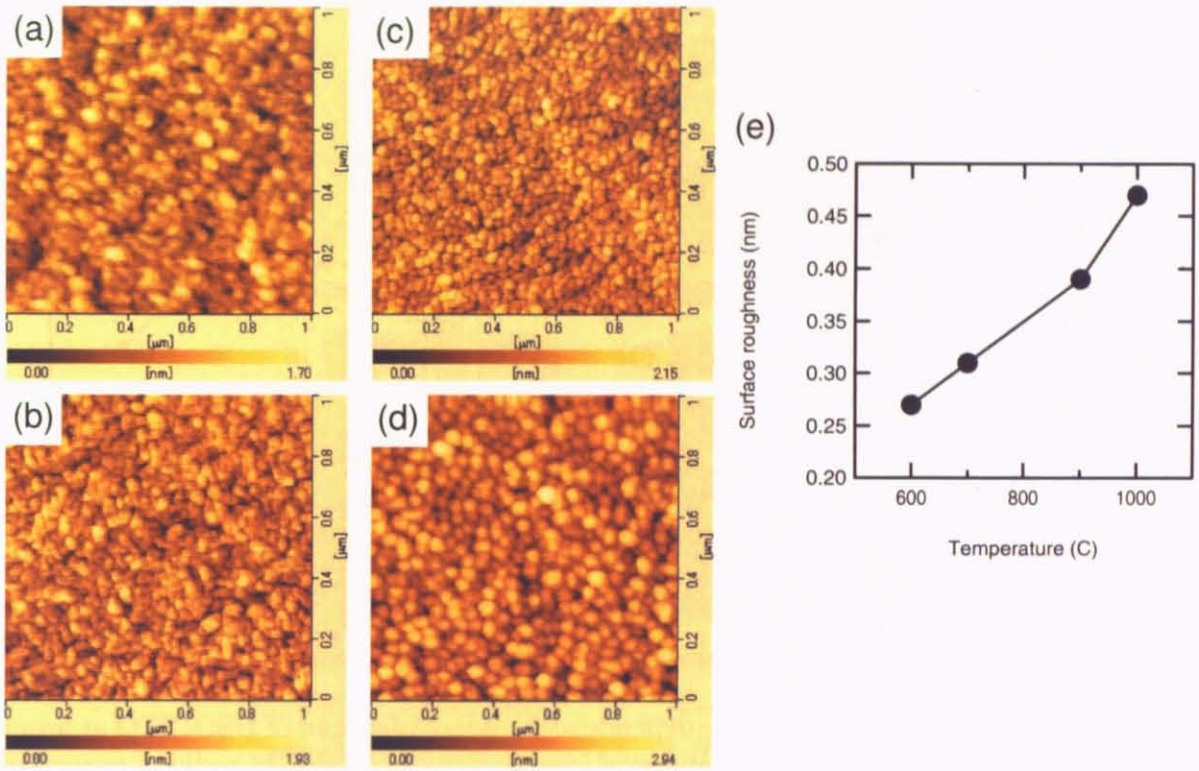

Figure 30: AFM images of surface roughness of DSO film grown at (a) 600, (b) 700, (c) 900, (d) 1000 °C, 1 mTorr. (d) The RMS of surface roughness under these conditions. These AFM images size are 1 μm × 1 μm, and the values of RMS of surface morphology were calculated using 1 μm × 1 μm images.

XRD 2θ-θ scan were also measured. The film peaks around the STO (200) peak are shown in Fig.31(a). The obtained film peak is assigned to DSO (220)/(004) peak, and these two film peaks can not be separated. The out-of-plane axis length change and FWHM (full width at half maximum) of rocking curve of DSO (220)/(004) peak were plotted in Fig.31(b). As the growth temperature increased, the out-of-plane axis length relaxed, and the crystallinity improved. These result indicates that each grains grow relatively freely, and larger at high growth temperature. This is not contradict to the results of surface morphology (Fig.30).

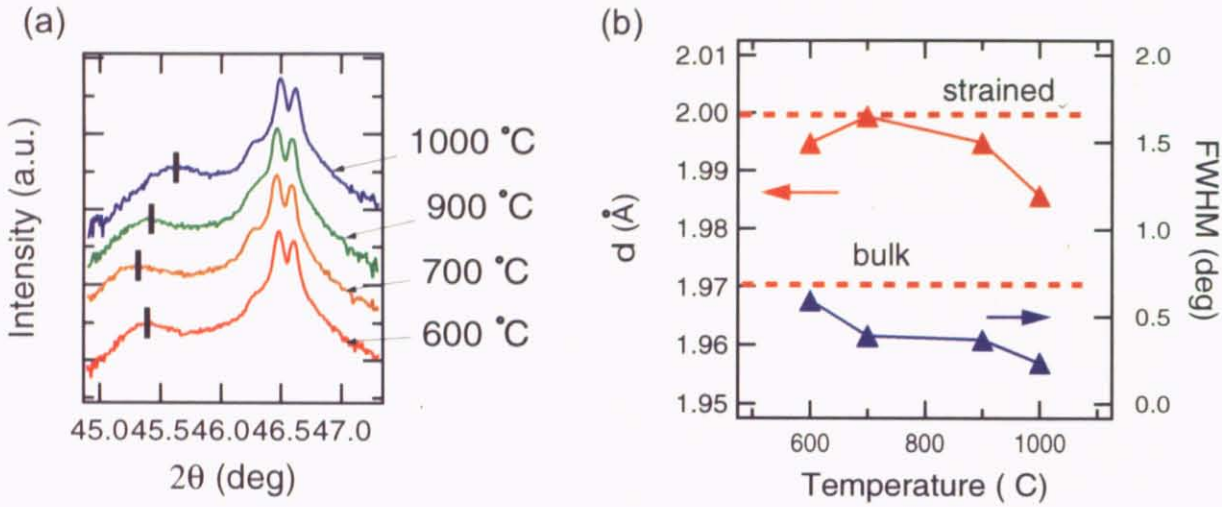

Figure 31: (a) Growth temperature dependence of XRD 2θ-θ scan of DSO/STO at around STO (200) peak and (b) out-of-plane axis length of, and FWHM of rodking curve DSO film (220)/(004) peak of 1 mTorr oxygen partial pressure during film growth.

From the view point of surface flatness, low growth temperature is preferable, on the other hand, to obtain better crystallinity, high growth temperature is needed. Therefore, it can be concluded that the optimum growth temperature is 700 °C.

Oxygen partial pressure dependence during film growth was studied from 10^{-5} to 10^{-1} Torr at 700 °C. Surface morphology of oxygen pressure dependence samples is shown in Fig.32(a) - (e), and the RMS of surface roughness is shown in Fig.32(f). The surface roughness dramatically changed above 10 mTorr.

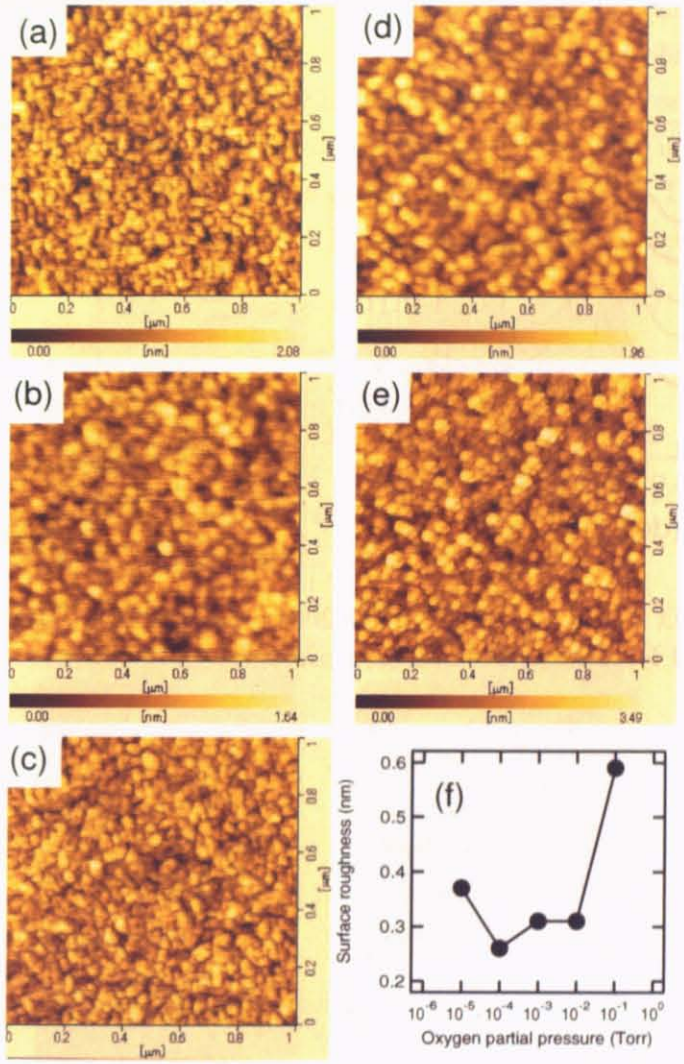

Figure 32: AFM image of growth oxygen pressure, (a) 10^{-5}, (b) 10^{-4}, (c) 10^{-3}, (d) 10^{-2}, and (e) 10^{-1} Torr. (f) RMS of surface roughness at each oxygen pressure. These AFM images size are 1 μm $\times$ 1 μm, and the values of RMS of surface morphology were calculated using 1 μm $\times$ 1 μm images.

XRD 2θ-θ scan, the out-of-plane axis length change, and FWHM of DSO film are shown in Fig.33. The out-of-plane axis length relaxed, and the crystallinity degraded, as the growth pressure became higher. To obtain an insulating interface that have few oxygen vacancies, however, the high growth pressure degrades the surface flatness and crystallinity of the DSO film, there fore 1 mTorr is chosen as growth pressure.

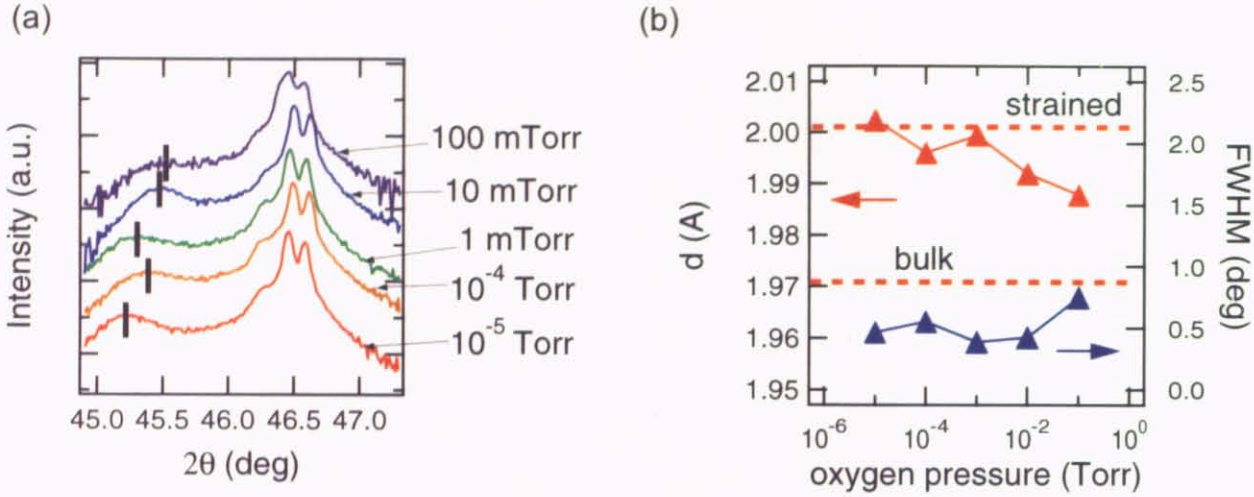

Figure 33: (a)XRD 2θ-θ scan around STO(200) peak is shown. (b) The out-of-plane axis length change and FWHM at each oxygen pressure.

4.3.2 Electrical characterization

A series of various thickness (5, 10, 20, 40, and 80 nm) epitaxial DSO films were fabricated to study the critical thickness that maintains flat surface, breakdown field, and dielectric properties. These DSO films were grown on 0.5 wt% - Nb doped STO substrates at 700 °C, and 1 mTorr oxygen partial pressure. The surface morphology of these films are shown in Fig.34(a)-(e). Step-and-terrace structure could be observed in Fig.34(a)-(c). Typically, about 30 periods of RHEED oscillation could be observed, therefore this result is corresponding to surface morphology change shown in Fig.34. The thickness dependence of RMS of surface roughness is shown in Fig.34(f). The RMS of surface roughness continuously increased with the film thickness, and this result is reasonable.

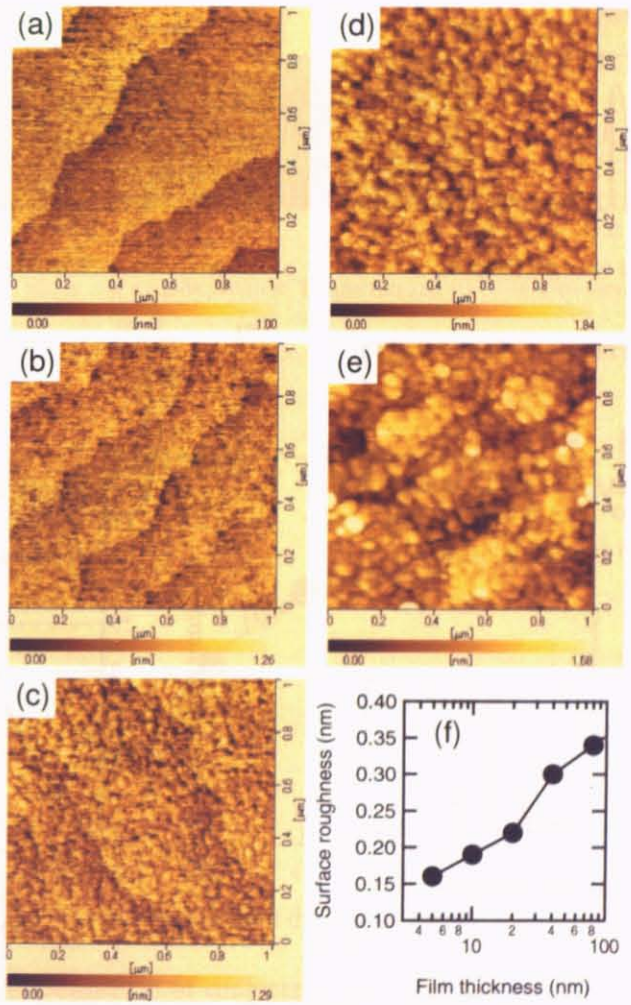

Figure 34: AFM image of DSO film on Nb:STO with various thickness, (a) 5, (b) 10, (c) 20, (d) 40, and (e) 80nm . (f) thickness dependence of RMS of DSO film surface roughness.

Breakdown field of these thickness dependent DSO films were measured. The values of breakdown field were defined as the bias voltage where mechanical breakdown happen. The histograms of distribution of the breakdown field values at each thickness samples are shown in Fig.35(a)-(e). These histograms were fitted by Gaussian. The average breakdown fields of each thickness samples are shown in Fig.35(f), the error bars were attached using σ in Gaussian fitting. The average breakdown field values as a function of film thickness have a peak at 10 nm. This result indicates that the critical thickness of epitaxial DSO film is at around 10 nm. It can be thought that the average breakdown field at 50 nm was low due to the tunneling current. It was found that epitaxial DSO film of 10 nm have quite high breakdown field about 8 MV/ cm. This value is comparable or higher than that of amorphous $CaHfO_3$ film.

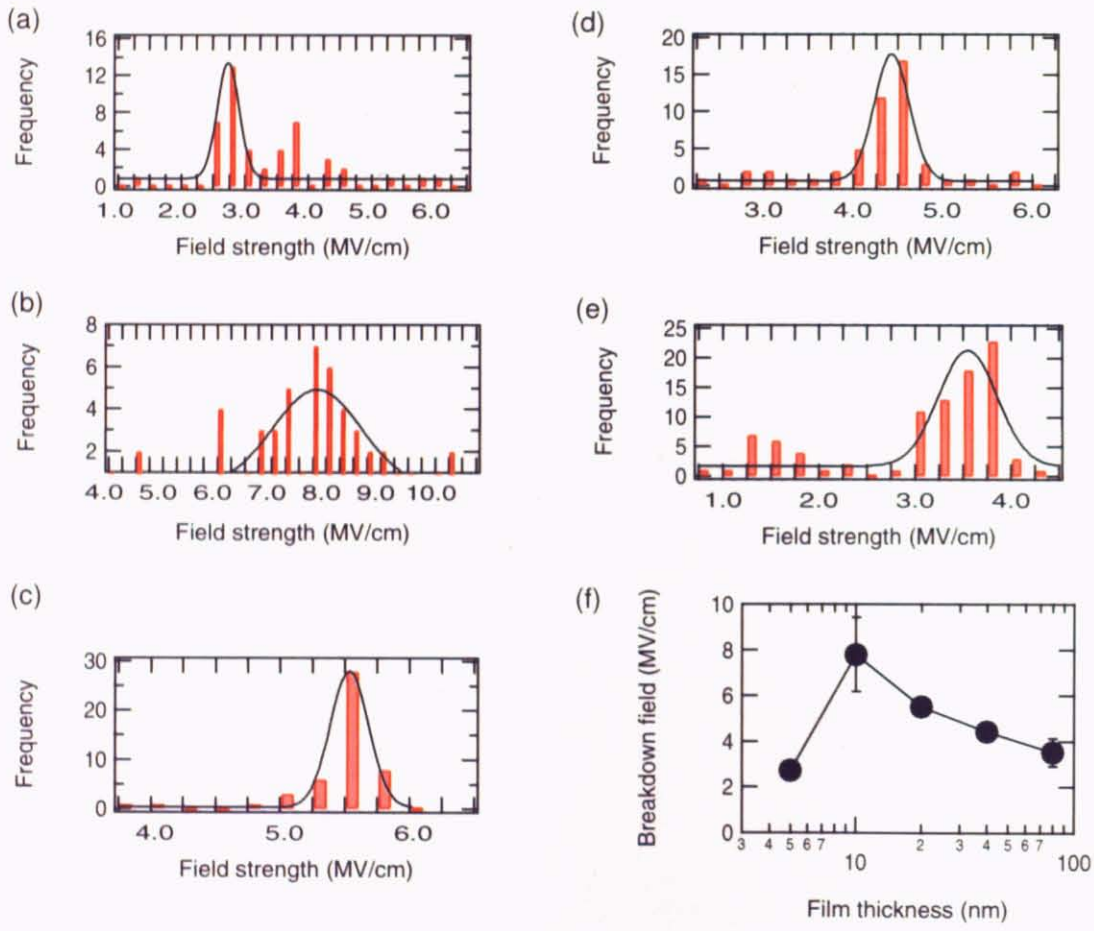

Figure 35: The histogram of breakdown field of epitaxial DSO film with the thickness, (a) 5, (b) 10, (c) 20, (d) 40, and (e) 80 nm. (f) Thickness dependence of average breakdown field at each thickness. These AFM images size are 1 μm $\times$ 1 μm, and the values of RMS of surface morphology were calculated using 1 μm $\times$ 1 μm images.

Dielectric constant of thickness dependent epitaxial DSO films on Nb:STO were measured. The sample configuration is shown in Fig.36. Dielectric constants at each film thickness are shown in Fig.37. Dielectric constant changed much with the film thickness, and such behavior were also reported in (Ba, Sr)TiO_3thin film[10]. The solid line in Fig.37 is fitting line using the assumption as follows:

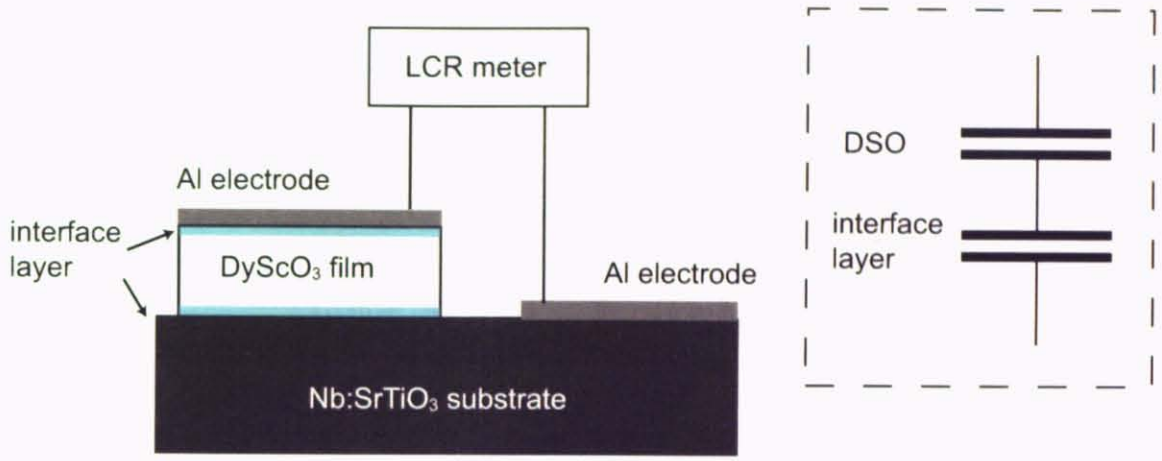

Figure 36: Schematic view of capacitance measurement system,and interfacial layer between film and substrate, Al pad.

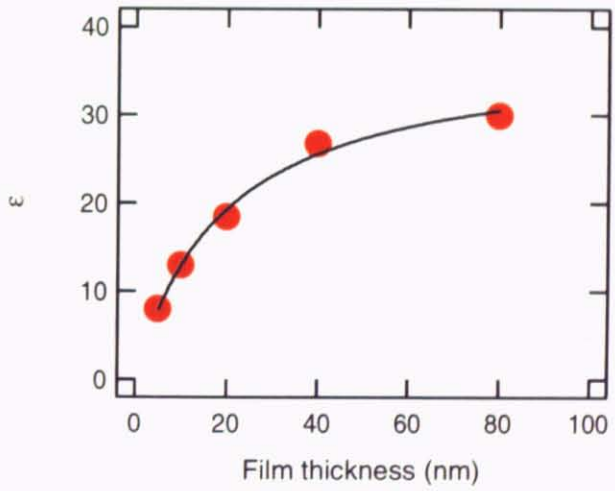

Figure 37: Thickness dependence of dielectric constant of epitaxial DSO film of Nb:STO. Solid line is fitting curve of thickness dependent dielectric constant.

The presence of interfacial layer that have lower dielectric constant than bulky part, and the interfacial layer thickness is independent of the DSO film thickness, were assumed, then the measured samples could be thought as two serial capacitors. The measured capacitance C can be written down as follows;

$$\frac{1}{C} = \frac{1}{C_{DSO}} + \frac{1}{C_{interface}}$$

where, C_{DSO} is capacitance of DSO film bulky part, and $C_{interface}$ is that of interfacial layer assumed above.

$$\frac{d}{\epsilon S} = \frac{d-\delta}{\epsilon_D S} + \frac{\delta}{\epsilon_i S}$$

$$\frac{d}{\epsilon} = \frac{(d-\delta)}{\epsilon_D} + \frac{\delta}{\epsilon_i} = \frac{\{(d-\delta)\epsilon_i + \delta\epsilon_D\}}{\epsilon_i \epsilon_D}$$

$$\epsilon = \frac{d\epsilon_i \epsilon_D}{\{(d-\delta)\epsilon_i + \delta\epsilon_D\}}$$

where, the film thickness, d, interfacial layer thickness, δ, measured dielectric constant, ϵ, dielectric constant of DSO bulky part, ϵ_D, dielectric constant of interfacial layer, ϵ_i, and pad area, S. Thickness dependence of dielectric constant was fitted using the above equation, and parameters were obtained.

- ϵ of interfacial layer = 8.8
- ϵ of DSO = 38
- thickness of interfacial layer = 5.8 nm

The obtained value is far from the reported dielectric constant value 20 that was obtained from DSO/SRO/STO structure [2]. It can be thought that one of the reason of large dielectric constant is due to the epitaxial strain. For example, STO film grown on DSO (110) single crystal substrates shows ferroelectricity at room temperature [11]. TEM images of interface rule out the possibility that a thin layer of low-ϵ materials formed at the interface.

Temperature dependence of dielectric constant of 80 nm thick DSO film is shown in Fig.38. Dielectric constant of DSO film was measured from 4 K to 300 K. Dielectric constant of DSO film dropped rapidly at low temperature.

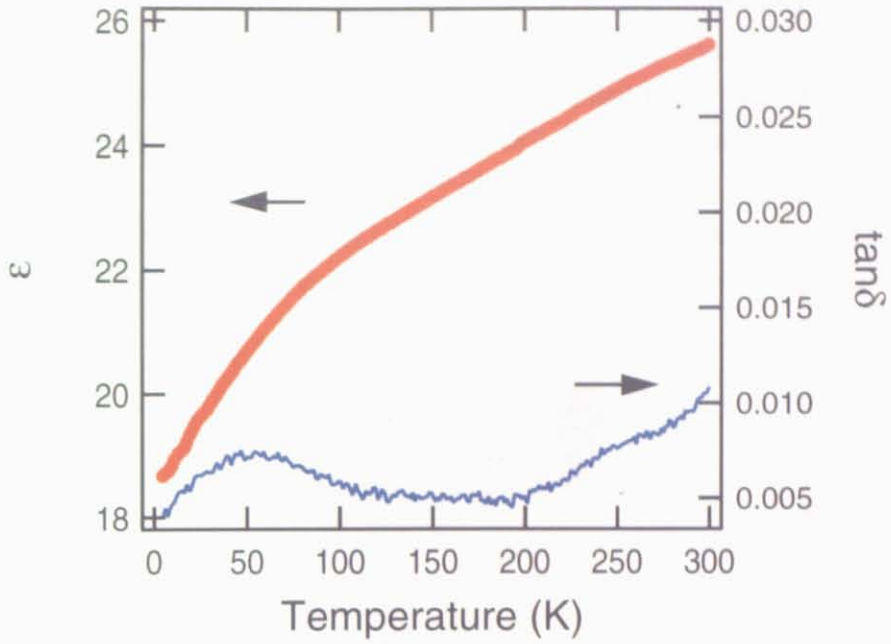

Figure 38: Temperature dependence of dielectric constant of 80 nm DSO film on Nb:STO.

Amorphous DSO films were grown to investigate the breakdown and dielectric properties, because, to fabricate the FETs using epitaxial interface, only epitaxial film structure may be easy to break by application of bias. Generally, the breakdown field become lower in FET structure due to particles on electrodes or other structural problems. Then, thick gate insulator layer will be needed.

Amorphous DSO films were grown on Nb:STO substrates with various thickness, 20, 40, and 80 nm. The surface morphology of these films were shown in Fig.39.

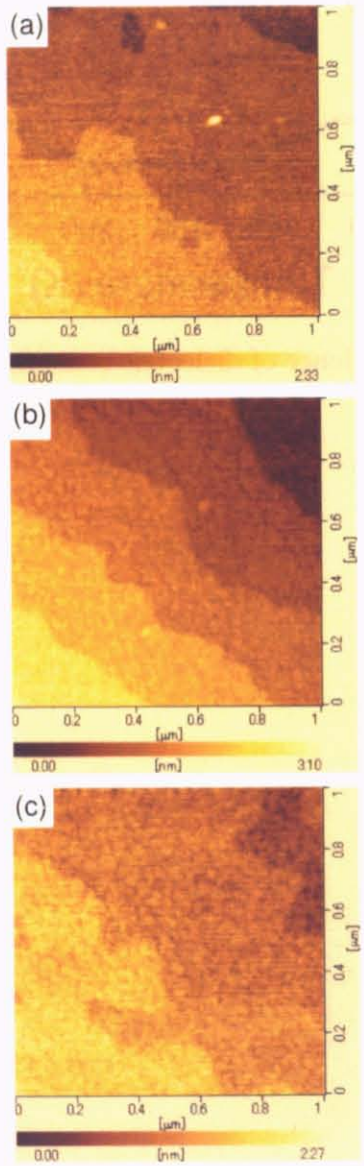

Figure 39: AFM images of amorphous DSO films with thickness,(a) 20, (b) 40, (c) 80 nm. The size of these AFM images were 1μm $\times$ μm.

As shown in Fig.39, surface of amorphous DSO film were atomically flat even 80 nm thick. Breakdown field of these samples were measured as is the case with epitaxial film. The histogram of breakdown fields of amorphous films are shown in Fig.40.(a)-(c). Average breakdown fields at each film thickness are shown in Fig.40.(d).

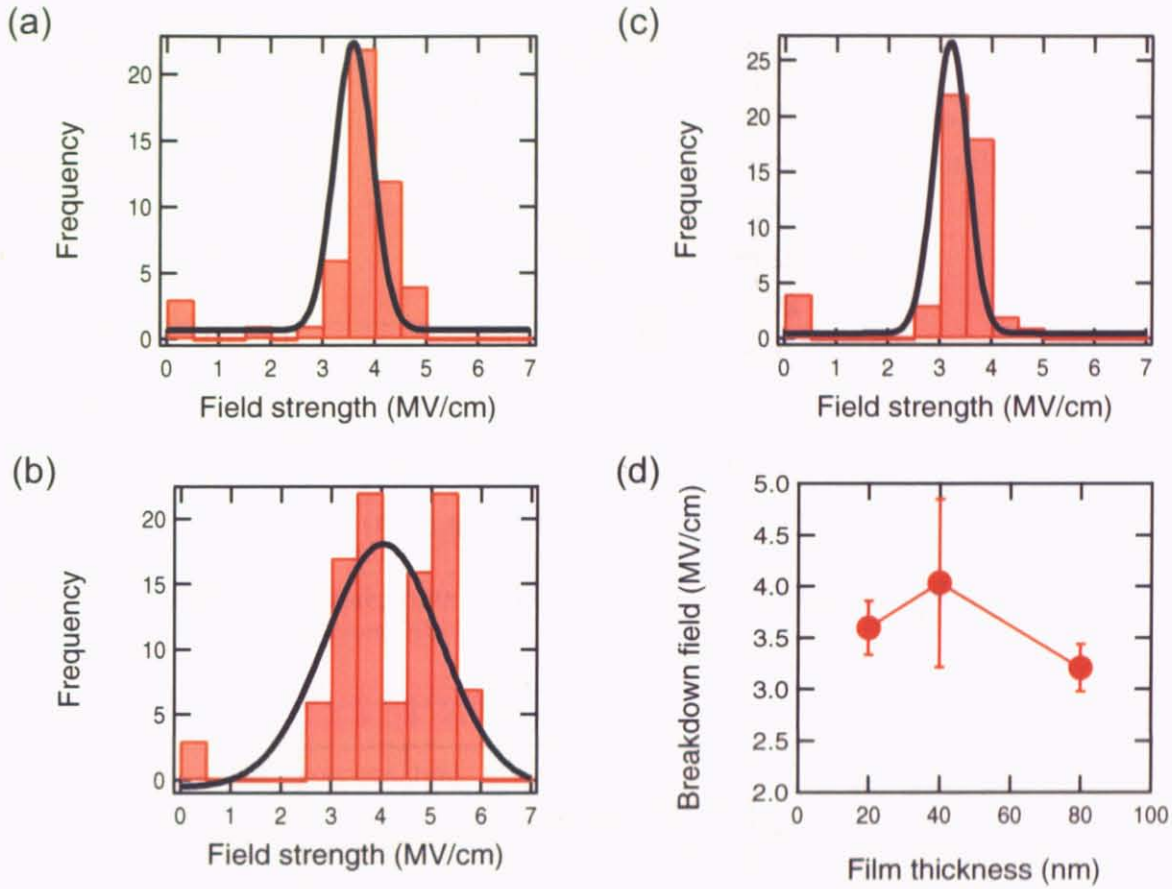

Figure 40: Histograms of breakdown fields of (a) 20, (b) 40, and(c) 80 nm thick amorphous DSO film on Nb:STO.

Dielectric constant of amorphous DSO film at each film thickness is shown in Fig.41.

Transmittance of amorphous DSO film on Al_2O_3 substrate was measured to obtain optical band gap of DSO, and is shown in Fig.42. As shown in Fig.42, it can be concluded that the band gap of DSO is more than 5 eV. The band gap of DSO is reported as 5.7-8 eV [2].

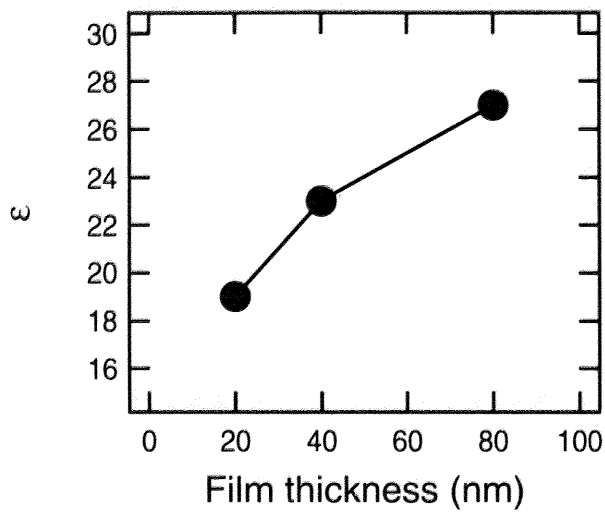

Figure 41: Dielectric constant of various thickness amorphous DSO films on Nb:STO.

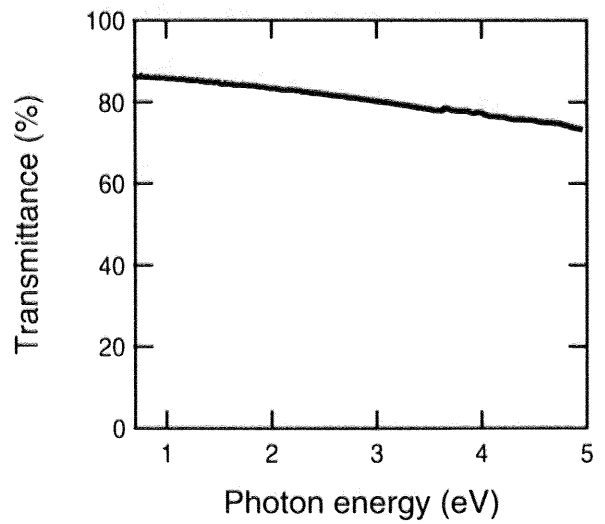

Figure 42: Transmittance of amorphous DSO film on sapphire.

The comparison of epitaxial with amorphous DSO films are shown in Fig.43. The average breakdown field of amorphous DSO film did not depend on the film thickness, on the other hand, epitaxial case, the value keep dropping with film thickness. This result indicates the grain formation and degrade the insulating property with increase of epitaxial film thickness. Considering the thicker gate insulator fabrication, amorphous DSO film is useful.

Dielectric constant of epitaxial and amorphous DSO films on Nb:STO substrates behaved quite similerly. Even in amorphous DSO films, dielectric constant decrease with thinner film thickness. This result suggest that the interfacial layer is not due to epitaxial strian, but the reason is unclear.

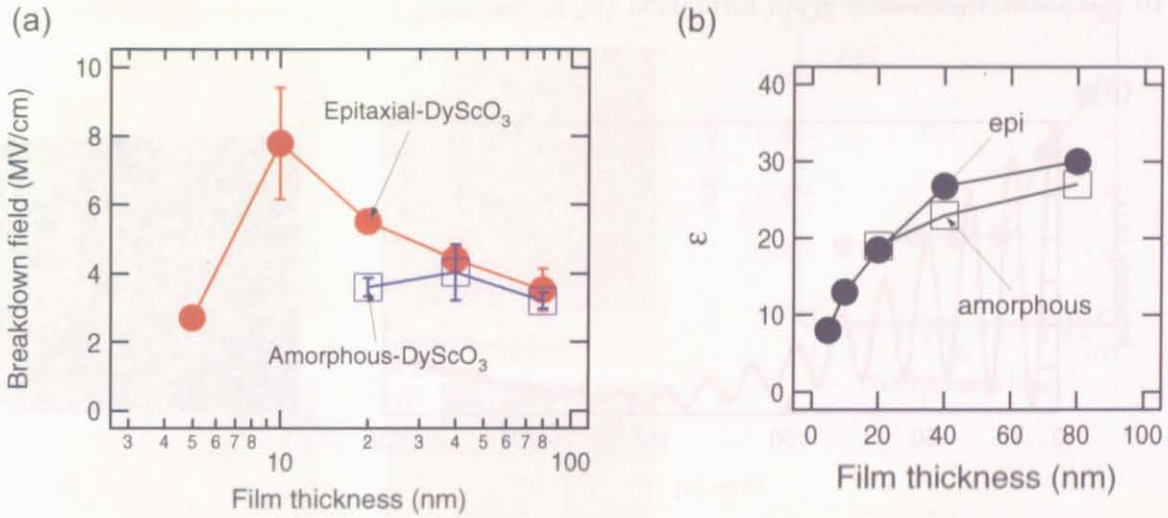

Figure 43: (a) Average breakdown fields of epitaxial and amorphous DSO films. (b) Thickness dependence of dielectric constant of epitaxial and amorphous DSO films.

4.4 Comparison of $DyScO_3$ with $CaHfO_3$ films

It is reported that STO based FETs using amorphous CHO show nice transistor action [12]. Epitaxial CHO films grown on STO (100) and (110) substrate have been studied[6]. Unfortunately, epitaxial CHO film on STO (100) substrate forms grain structure after initial about ten monolayer growth. Therefore, fabricating FETs using epitaxial CHO film, there is a limitation of thickness less than ten unit cell.

Evaluation of surface morphology and breakdown properties of epitaxial CHO films grown on Nb:STO substrates with film thickness was done to compare with epitaxial DSO films. Typical RHEED oscillation and pattern are shown in Fig.44. RHEED oscillation continued about 10 periods during CHO film growth(Fig.44(a)). This result corresponds to the above mentioned grain formation thickness.

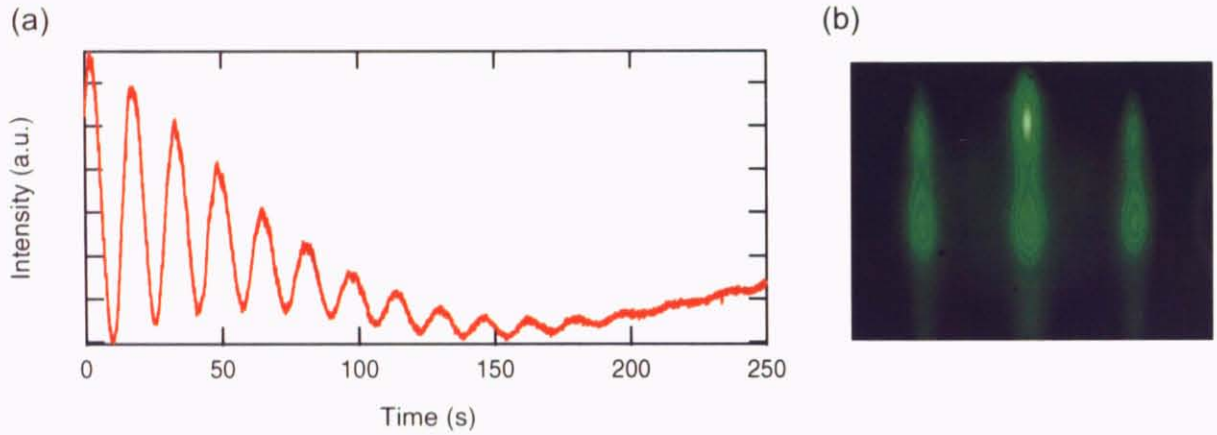

Figure 44: Typical RHEED (a) oscillation, and (b) pattern of epitaxial CHO film grown on Nb:STO substrate at 700 °C, 1 mTorr.

The film thickness dependence of surface morphology and RMS of surface roughness are shown in Fig.45. Film thickness was systematically changed from 1.6 to 40 nm. Step-and-terrace structure survive around 10 nm sample, and above 10 nm, pin-hole defects could be observed.

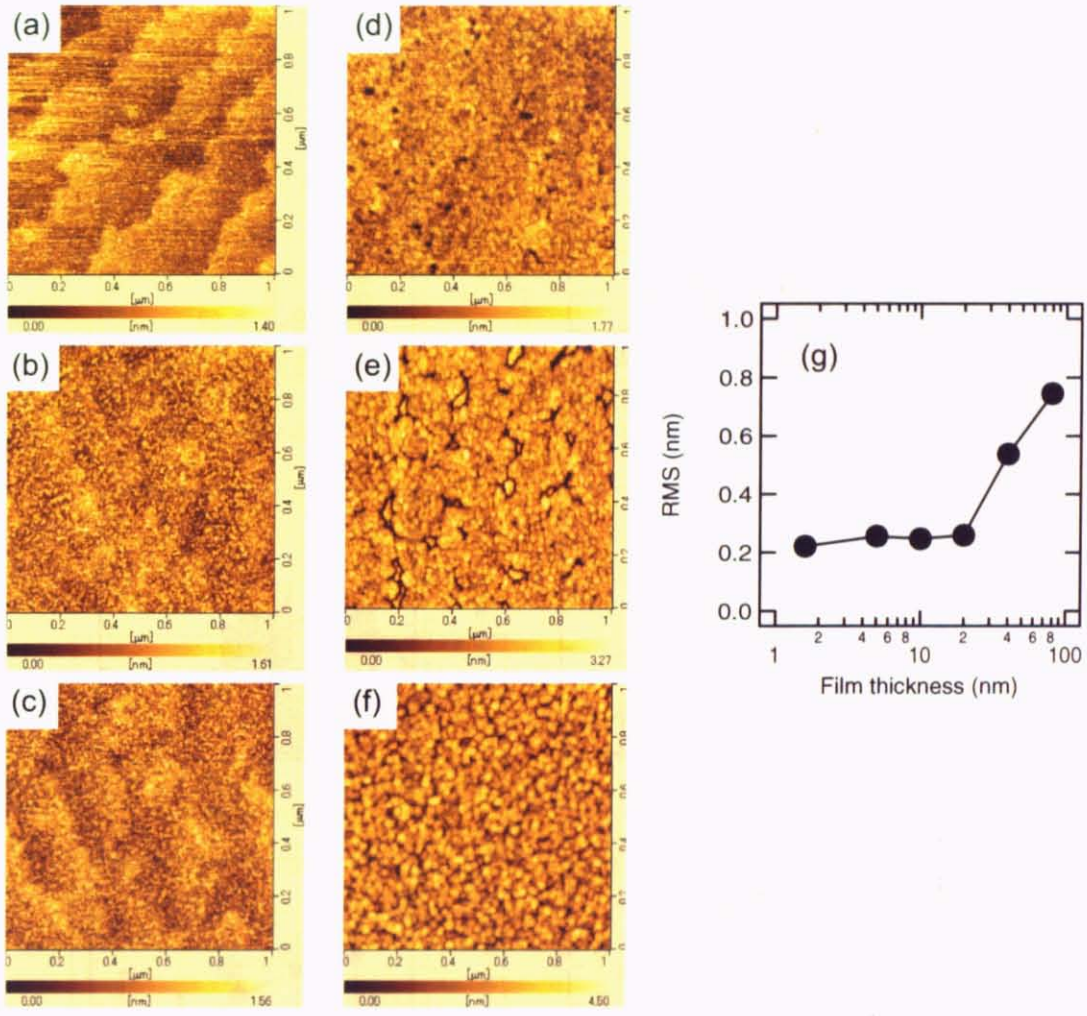

Figure 45: AFM image of epitaxial CHO films with thickness (a) 1.6, (b) 5, (c) 10, (d) 20, (e)40, and (f) 80 nm. These AFM images size are $1\mu m \times 1\mu m$. (g) RMS of surface morphology of epitaxial CHO films at each film thickness. RMS was calcurated using $1\mu m \times 1\mu m$ image.

Breakdown fields were measured about each thickness samples, and the histogram of these breakdown field and average breakdown field with thickness are shown in Fig.46. The breakdown field values of 1.6 nm (4 u.c.)-thick epitaxial CHO film were too low (less than 100 kV/cm), because it can be thought that the tunneling current is dominant in such very thin film.

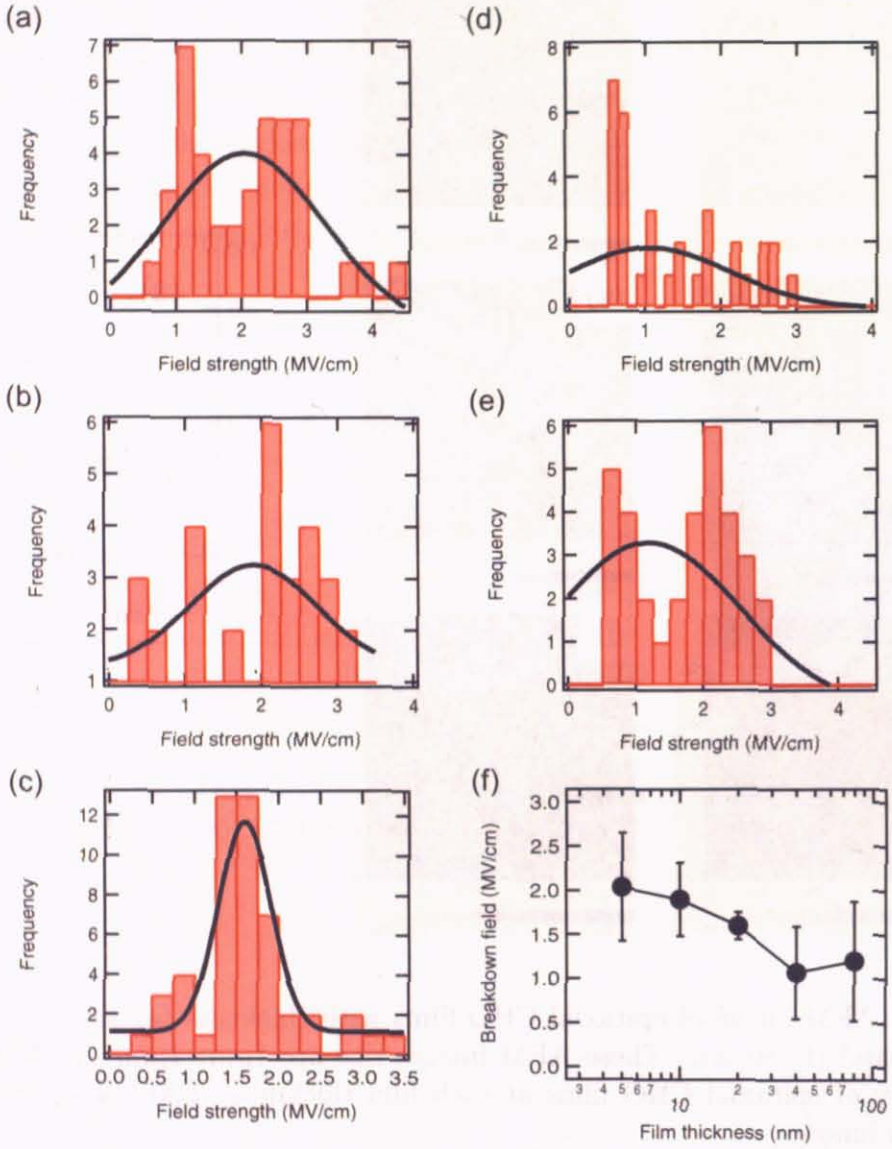

Figure 46: The histogram of breakdown fields of (a) 5, (b) 10, (c) 20, (d)40, and (e) 80 nm thickness epitaxial CHO films on Nb:STO substrates. (f) Average breakdown field of epitaxial CHO films at each film thickness.

Comparison of DSO with CHO film, RHEED oscillation are shown in Fig.47, and RMS of surface roughness and average breakdown field in Fig.48. As shown in Fig.47 and Fig.48, DSO is superior to CHO as insulator layer that have flat surface.

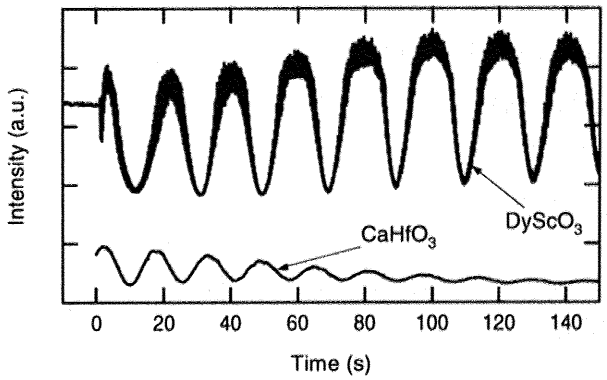

Figure 47: Typical RHEED oscillation of epitaxial DSO and CHO film on Nb:STO substarte.

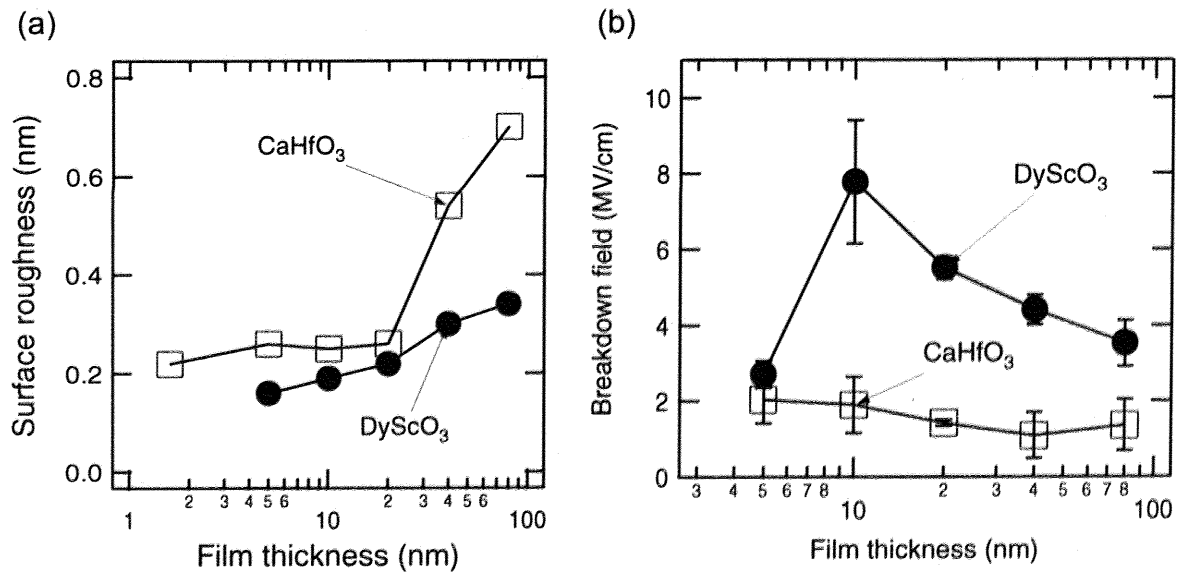

Figure 48: (a) RMS of surface roghness and (b) Average breakdown field of epitaxial DSO and CHO film on Nb:STO.

4.5 Conclusion

Wide-gap insulator films, $NdGaO_3$ and $DyScO_3$, were fabricated on $SrTiO_3$ (100) single crystal substrates. $DyScO_3$ films grew epitaxialy on $SrTiO_3$ (100) substrate. As a result, epitaxial $NdGaO_3$ film could not obtained under conditions that used in this study.

Comparing to $CaHfO_3$ with $DyScO_3$, the surface morphology of $DyScO_3$ film keep flat surface thicker region. Moreover, the insulating properties is much superior to $CaHfO_3$ or $NdGaO_3$. The maximum average breakdown field of epitaxial $DyScO_3$ film recorded about 8 MV/cm at 10 nm-thick film.

The dielectric constant of epitaxial $DyScO_3$ film was about 30 at 80 nm-thick sample. Dielectric constant of epitaxial and amorphous $DyScO_3$ film changed much with film thickness. This result indicates the presence of low-ϵ interfacial layer, however, the origine is unclear

As mentioned above, it can be concluded that $DyScO_3$ is quite good insulating material for not only oxides field-effect devices, but barrier of tunneling junction and so on.

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Appl.Phys.Lett. 85, 425 (2004)

5 Electrical properties of $DyScO_3$ / $SrTiO_3$ hetero-interfaces

5.1 Introduction

A field-effect transistor (FET) is basically composed of two electrodes on a semiconducting substrate, covered by an insulator film (Gate insulator) that can be used to modulate the electronic structure of the surface layer of the semiconductor by field effect. This device controls the current that can flows in the channel between the two electrodes, called source and drain, by the application of voltage to an electrode that is on top of the gate insulator layer. The transistor action is sensitive to the electronic states at the heterointerface.

In this study, $SrTiO_3$ (STO) was used as a semiconducting channel material and a $DyScO_3$ (DSO) film was used as the gate insulator layer. Using a transition metal oxide like STO for the semiconductor layer is very interesting from the view point of carrier doping. Transition metal oxides show wide varieties of interesting physical properties, for instance high-temperature superconductivity, colossal magnetoresistance, ferromagnetism, ferroelectricity and so on. The properties of oxides are generally functions of carrier density and dramatic changes in physical properties can be induced by chemical doping of oxides. In STO, for example, it is possible to observe a series of transitions from an insulating to a semiconductor and further into a metallic state as a function of carrier density. Even superconductivity can be induced at a carrier density of approximately 10^{20} cm^{-3}. In addition to chemical doping, it is also possible to modulate the local density of carriers in thin layers by field effect in a field-effect transistor. Some of the advantages of field-effect doping over chemical doping are the possibility of adjusting the doping level continuously and changing the carrier density without creating disorder, which is inevitable when chemical imputity doping is used.

STO based FETs have been that use $CaHfO_3$ (CHO) as a gate insulator material have already been developed. However, CHO forms a grain structure after an initial growth of $\sim$ 10 monolayers. It is therefore difficult to fabricate fully epitaxial STO/CHO field-effect devices. As mentioned in Section 4.3, DSO films can be grown thicker than CHO films while still maintaining a flat surface. Therefore, it should be possible to fabricate fully epitaxial field-effect devices based on STO and insulating DSO films.

5.2 Amorphous $DyScO_3/SrTiO_3$ FETs

5.2.1 Fabrication process of amorphous $DyScO_3/SrTiO_3$ FETs

Amorphous DSO/STO FETs are technically the easiest structures to fabricate, since the whole process can be done at room temperature. In practice at least one annealing step is needed to handle the formation of oxygen defects during pulsed laser deposition growth of insulator films. The flowchart of the fabrication process of amorphous DSO/STO FETs is shown in Fig. 49.

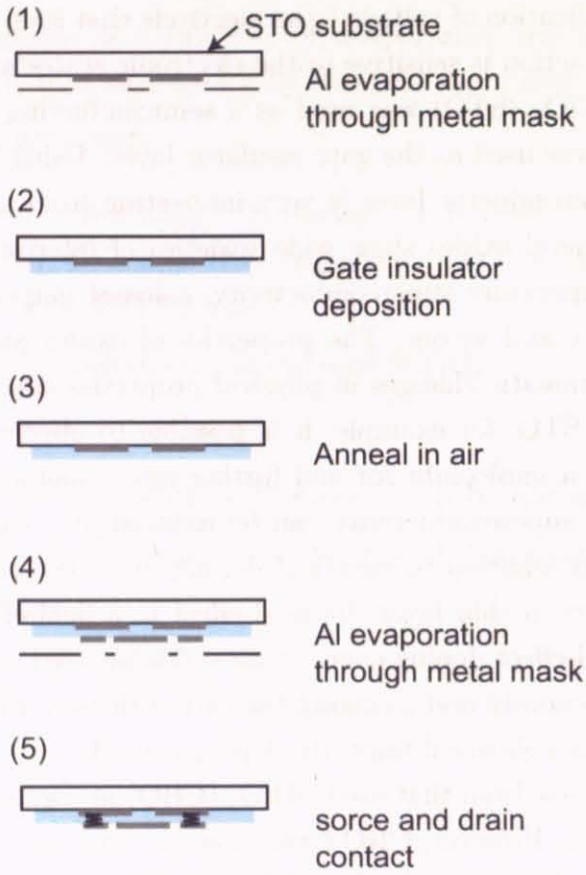

Figure 49: Fabrication process of amorphous DSO/STO FETs

The fabrication steps illustrated in Fig. 49 are the following:

1. Aluminum source and drain electrodes (octagonal shapes in Fig. 51 (a)) were evaporated on STO (100) single crystal substrate in vacuum through a metal contact mask. The schematic view of the sample holder used for fixing the metal mask is shown in Fig. 50.

The thickness of the source and drain electrodes was 100 to 200 nm. The thickness of the source and drain electrodes had to be small in order to prevent the formation of leak sources at the electrode edges in a completed FET structure.

Aluminum was selected as the source and drain electrode material because Al electrodes are known to give Ohmic contacts on STO [1].

2. An amorphous DSO film was deposited on the STO substrate at room temperature, covering the source and drain electrode pads. The oxygen partial pressure during film growth was 1 mTorr. The insulator layer thickness was about 50 nm.

3. The sample was annealed in a furnace in air to fill the oxygen vacancies that formed in the substrate during insulator layer growth. The post-annealing temperature was 250 °C and the annealing time was 6 hours.

4. Aluminum gate electrodes were evaporated on the sample through another metal mask. To avoid breaking the gate insulator layer, the metal mask for gate electrodes was supported by attached tapes. The gate electrodes were keyhole-shaped to minimize overlap between the gate and source-drain electrodes while leaving a large area for attaching wires. The gate electrode layout is shown in Fig. 51 (a).

5. Contact with the source and drain electrode were made by wire-bonding aluminum wires to the film surface, crushing the gate insulator layer and making contact with the aluminum pads at the substrate-insulator interface.

A photograph of an array of FET devices fabricated in this study, and a schematic cross-section drawing of FET are shown in Fig. 51. The 0.5 mm-thick STO (100) substrate was cut into 5 × 10 mm^2 pieces, allowing 19 FETs to be placed on a single substrate. The channel length (L) and width (W) of this device were 100 and 500 μm, respectively. The gate electrode width was 120 μm. There was about 10 μm overlap with both source and drain electrodes.

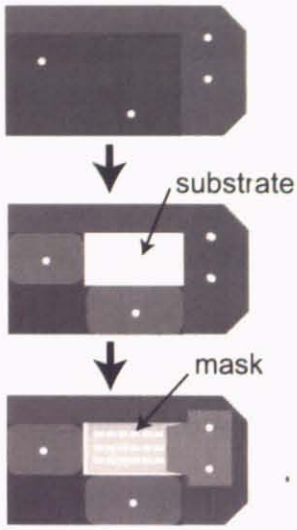

Figure 50: Schematic view of the sample holder that was used to fix the metal mask and STO substrate. First, the STO substrate was fixed in place with two metal brackets. After that, a metal mask was placed on the substrate and fixed with a clamp. The corner of the sample holder was used as a position reference.

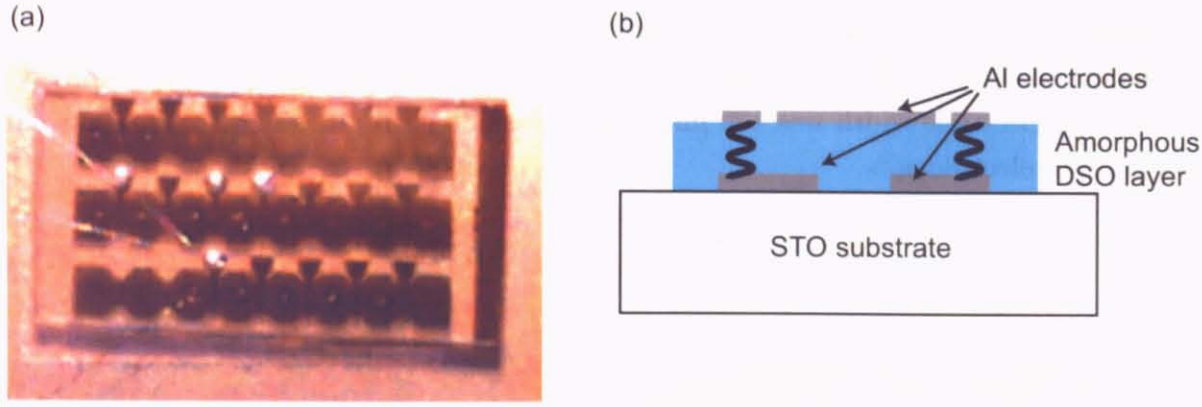

Figure 51: (a) Photograph, (b)Schematic view of an amorphous DSO/STO FET.

5.2.2 Characterization of amorphous DSO/STO FETs

The devices used for characterization contained 50 nm-thick DSO insulator layers. The laser fluence used for insulator deposition was 0.76 J/cm^2, resulting in a growth rate of about 90 pulses per monolayer. Typical AFM images of the insulator layer surface is shown in Fig.52. A step-and-terrace structure was observed on the amorphous film surface. This structure reflects the substrate surface. The flatness of the film is important for FET operation, because a uniform gate field can be applied.

The drain-source current, I_{DS}, measured at room temperature, is plotted as a function of the drain-source bias V_{DS} under various gate bias V_{GS} voltages in Fig. 53 (a).

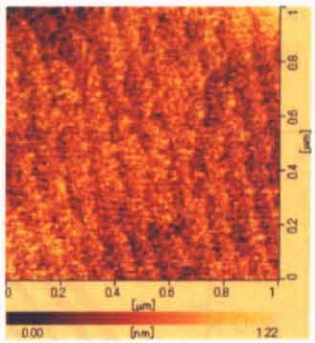

Figure 52: Typical surface morphology of the device surface. The image size is $1 \times 1 \mu m^2$.

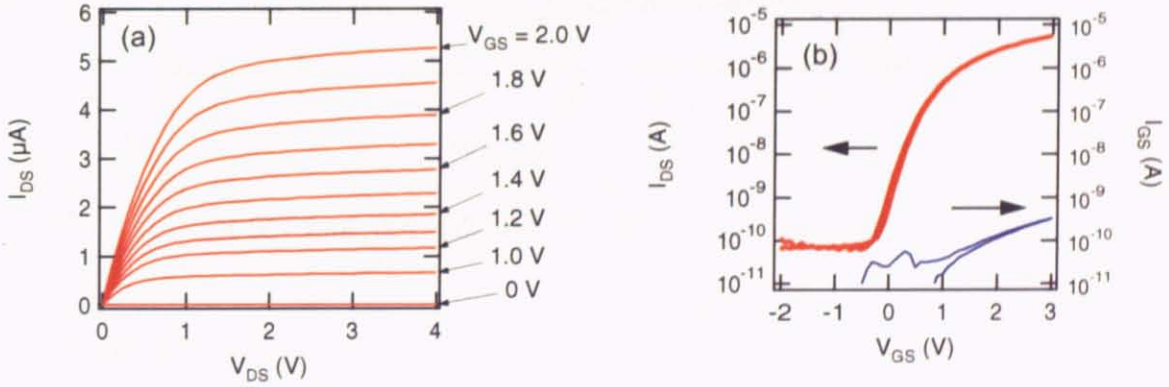

Figure 53: (a) Drain-source current, I_{DS}, plotted as a function of the drain-source bias, V_{DS}. (b) Drain-source current and the gate leak current, I_{GS}, plotted as a function of the gate bias at a fixed drain-source bias V_{DS} of +0.5V. The field-effect mobility was 3.0 cm^2/V s and the on-off ratio was higher than 10^4.

The I_{DS} and gate leak current I_{GS} are shown as a function of V_{GS} in Fig. 53 (b). The measurements were done at room temperature. In these measurements, the V_{DS} was fixed at +0.5 V, which is in the linear region of the I_{DS} vs. V_{DS} curve. The V_{GS} step was 0.1 V and the sweep delay was 0.1 s. The 'off' current was about 100 pA, while the 'on' current reached about 5 μA. The on-off current ratio was more larger than 10^4. The field-effect mobility was 3.0 cm^2/V s at V_{GS} = 3 V, where the field-effect mobility was calculated in the linear region as

$$\mu_{FE} = \frac{L}{W \times V_D \times C_0} \frac{\partial I_D}{\partial V_G}$$

The temperature dependence of the FET properties was measured in order to study the behavior of electronic states at the amorphous DSO/STO interface. The I_{DS} is plotted in Fig. 54 as a function of V_{GS}. Measurements were done at 300, 250, 200, and 150 K.

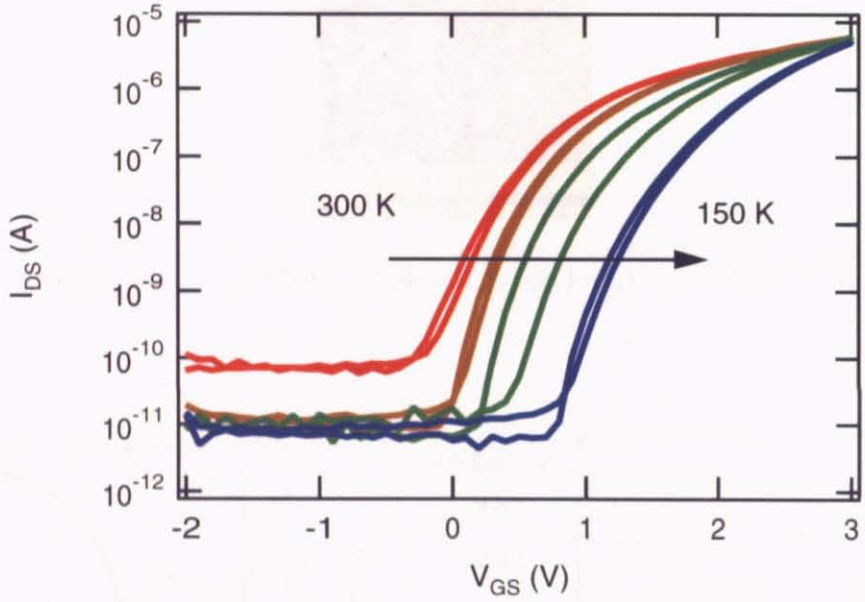

Figure 54: I_{DS} vs. V_{GS} at 300, 250, 200, and 150 K.

As shown in Fig.54, the off current decreases with temperature and the threshold voltage (V_{th}) shifted towards the positive bias side. I_{DS} is re-plotted as a function of the ($V_{DS} - V_{th}$) in Fig. 55(a). The field-effect mobility and the threshold voltage at each temperature are plotted in Fig. 55(b). The threshold voltage shift suggests the presence of interface states. Injection of electrons results in filling the trap states and causes the Fermi energy to shift in the surface layer of the STO substrate. Below the field-effect threshold ($V_{GS} < V_{th}$), the injected charges are trapped at interface states that are located more than a few k_BT below the conduction band bottom (deep traps). When the Fermi level reaches the trap states with energies within a few k_BT from the conduction

band bottom (shallow traps), thermal excitation from trap states to the conduction band becomes possible and interface conductivity increases dramatically, by several orders of magnitude. This threshold shift phenomenon has also been observed in perovskite oxide based amorphous Al_2O_3 / $KTaO_3$ [2], organic [3, 4], CNT [5], and fullerene [6] based FETs.

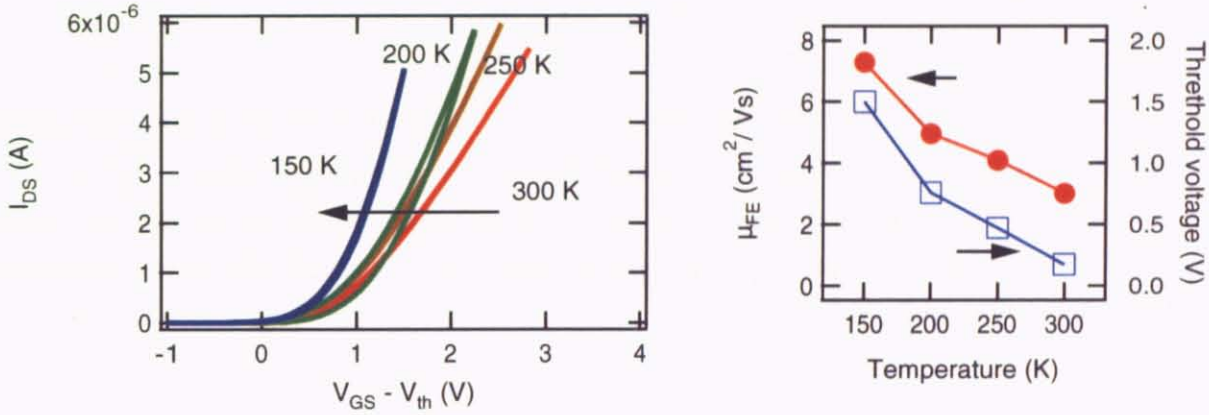

Figure 55: (a) I_{DS} vs. I_{th} at 300, 250, 200, and 150 K. (b) Field-effect mobility (open squares) and threshold voltage (filled circles) shift as a function of temperature.

With cooling, the border between deep and shallow traps shifts towards the conduction band because carriers can no longer be thermally excited from deeper trap states to the conduction band. The concentration of deep traps with energies less than few k_BT below the conduction band, $N_{\text{trap}} = \frac{C_0 V_{\text{th}}}{e}$, can be calculated if the capacitance per unit area, C_0 is known. However, these absolute values are not significant because the Fermi level is not always the same from sample to sample. Variation between samples was large due to difficulty of controlling the fabrication process or variations in the as-received substrate surface properties. The energy distribution of trap states gives more useful information about the nature of the interface trap states. The energy distribution of trap states can be obtained by using the equation

$$\frac{\partial N_{\text{tr}}}{\partial E} = \frac{C_0}{ek_B}\frac{\partial V_{\text{tr}}}{\partial T}$$

As shown in Fig. 56, the threshold shit is a linear function of temperature. The energy distribution of trap states can be calculated from the slope of this line. $\frac{\partial N_{tr}}{\partial E} = 3.2 \times 10^{14} cm^{-2} eV^{-1}$, is almost temperature independent within $\approx$ 0.1 eV of the conduction band. This value is comparable to the energy distribution of trap states at the amorphous CHO/STO interface [7].

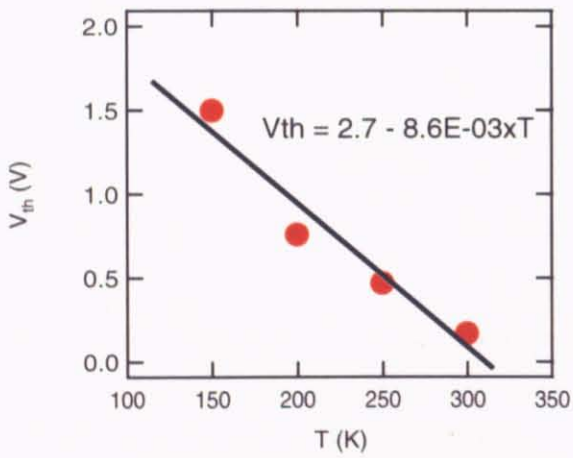

Figure 56: Linear fit of V_{th} vs. temperature.

The I_{DS}-V_{GS} curve measured at 100 K is shown in Fig. 57. In this amorphous DSO/STO FET, carriers could not be induced at 100K. This result indicates that the trap state density is very high at around 9 meV ($\approx 100k_B$) below the conduction band bottom. A schematic drawing of the trap state density at the interface between amorphous DSO and STO is shown in Fig.58. The observed transistor behavior can be understood by assuming that the trap state density close to the band edge is too high to be filled by the induced carriers. Therefore, this device did not work before breakdown of the gate insulator. In summary, amorphous DSO/STO interfaces have very high density of trap states within about 10 meV of the conduction band bottom. The type of defects that are the origin of such state is still unclear.

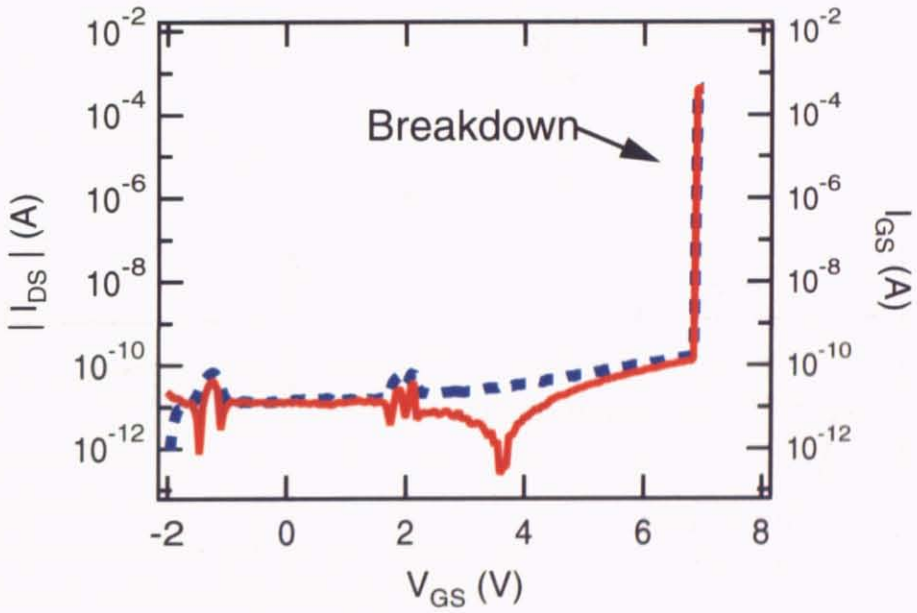

Figure 57: I_{DS} vs. V_{GS} at 100 K. This FET did not show channel current change before gate insulator breakdown at $V_{GS} \approx 7$ V at 100 K.

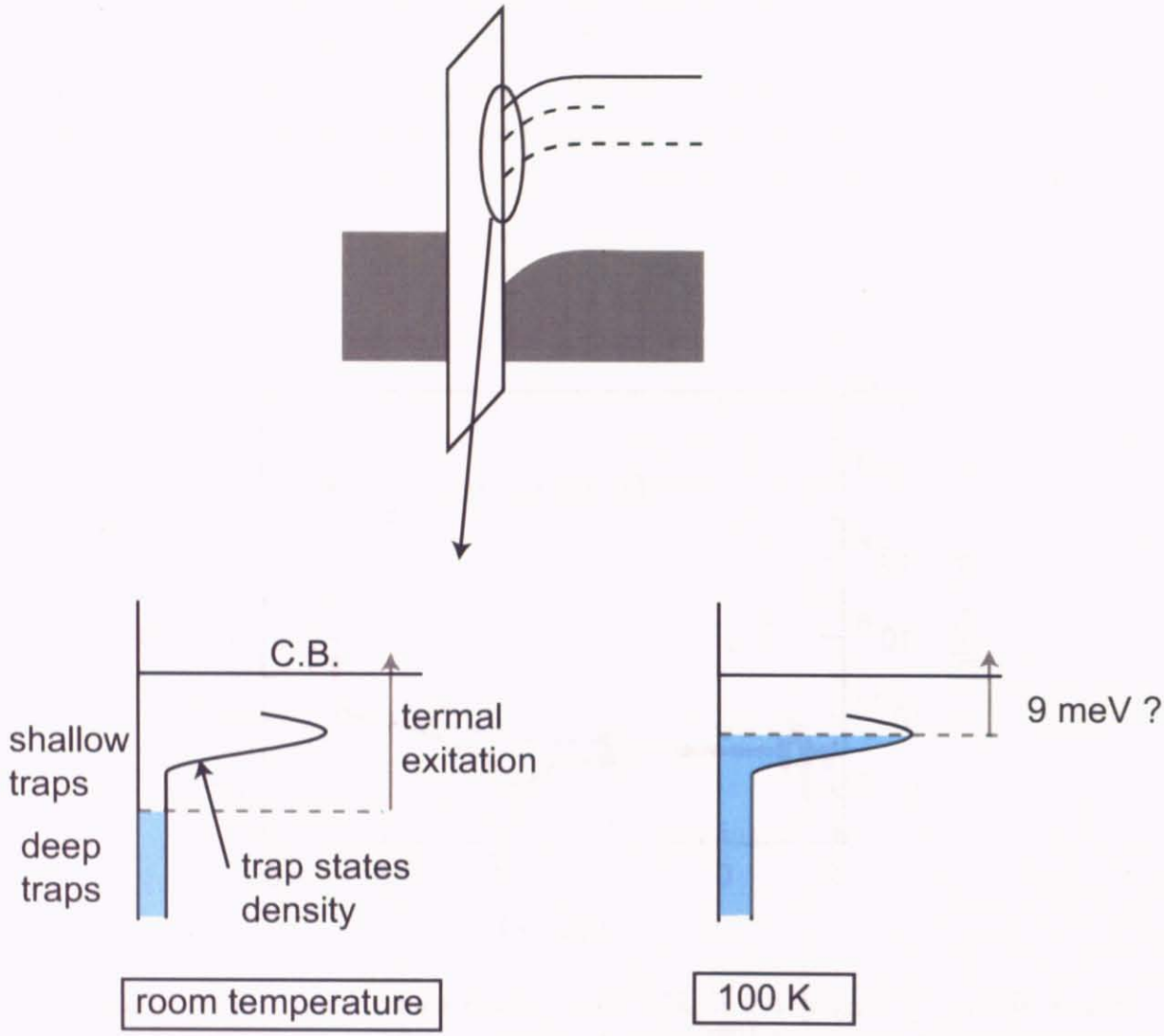

Figure 58: Schematic drawing of electronic states close to the conduction band bottom in the interface region of the amorphous CHO/STO heterostructure.

5.3 Epitaxial $DyScO_3$ / $SrTiO_3$ FETs

5.3.1 Fabrication process of epitaxial $DyScO_3$ / $SrTiO_3$ FETs

The flowchart of STO-based FETs containing epitaxial DSO films is shown in Fig. 59.

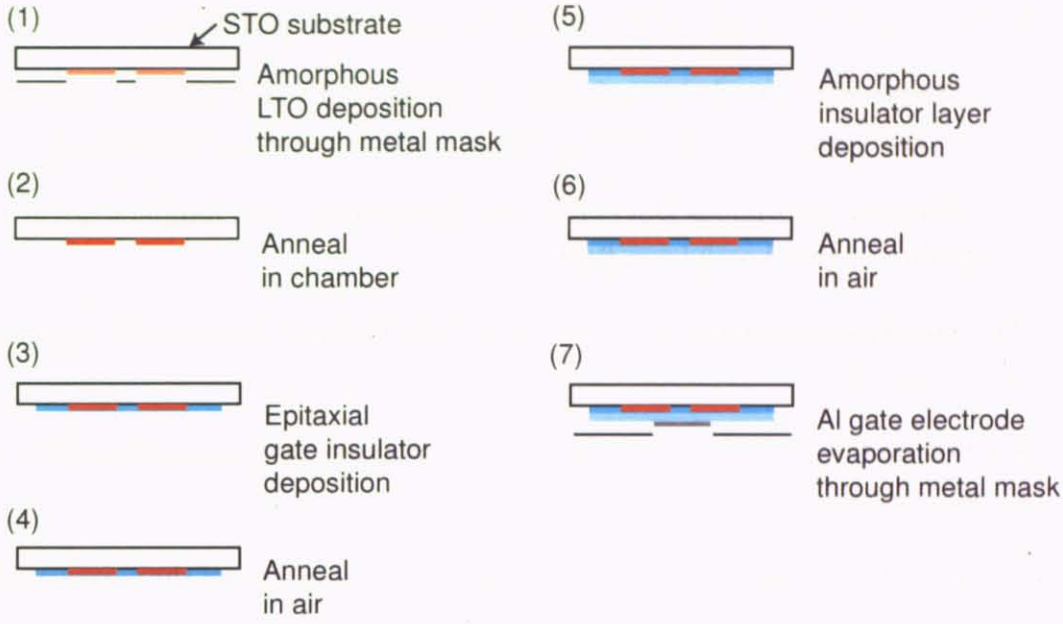

Figure 59: Fabrication flowchart of epitaxial DSO/STO FETs.

The differences between amorphous and epitaxial DSO/STO FET processes is mainly in the structure and material of the source and drain electrodes. In the amorphous FET case, aluminum source and drain electrodes were used. In the epitaxial case, $LaTiO_3$ (LTO) was used as a metallic layer to form the source and drain electrodes. Epitaxial DSO films have to be grown at high temperatures, which means that simple aluminum metal electrodes could no longer be used. Amorphous LTO was first deposited on the STO substrate surface through a contact mask at room temperature and annealed to promote interdiffusion of La and Sr, forming a metallic electrode region. Room temperature growth was done to avoid contamination of the channel region by the stainless steel contact mask. The steps of the epitaxial DSO/STO FET fabrication process are shown in Fig. 59 and outlined below:

1. Amorphous LTO and STO were deposited on a STO substrate through a metal mask at room temperature. The reason for using a STO/LTO multilayer will be explained in Section 5.3.2. The sample holder was the same as in case of the amorphous FET process, shown in Fig. 50.

2. The sample was annealed in the deposition chamber. The annealing was done in two steps. First, the sample was annealed at 800 °C and 10^{-6} Torr of oxygen for 30 minutes to crystallize the LTO, followed by a 1200 °C anneal at 10^{-6} Torr for 3 hours to diffuse La and Sr in the electrode layer.

3. Epitaxial DSO layer was grown at 700 °C and 1 mTorr of oxygen.

4. The sample was annealed in a furnace in air at 500 °C for 12 hours to compensate the oxygen vacancies in the film and in the surface layer of the substrate.

5. An additional amorphous DSO layer was deposited at room temperature at 1 mTorr to obtain a higher breakdown field.

6. The sample was annealed in a furnace at 250 °C for 12 hours to fill any remaining oxygen vacancies.

7. Finally, aluminum gate electrodes were evaporated in vacuum through a contact mask.

A photograph of a FET array and schematic cross-section view of the epitaxial DSO/STO FET is shown in Fig. 60.

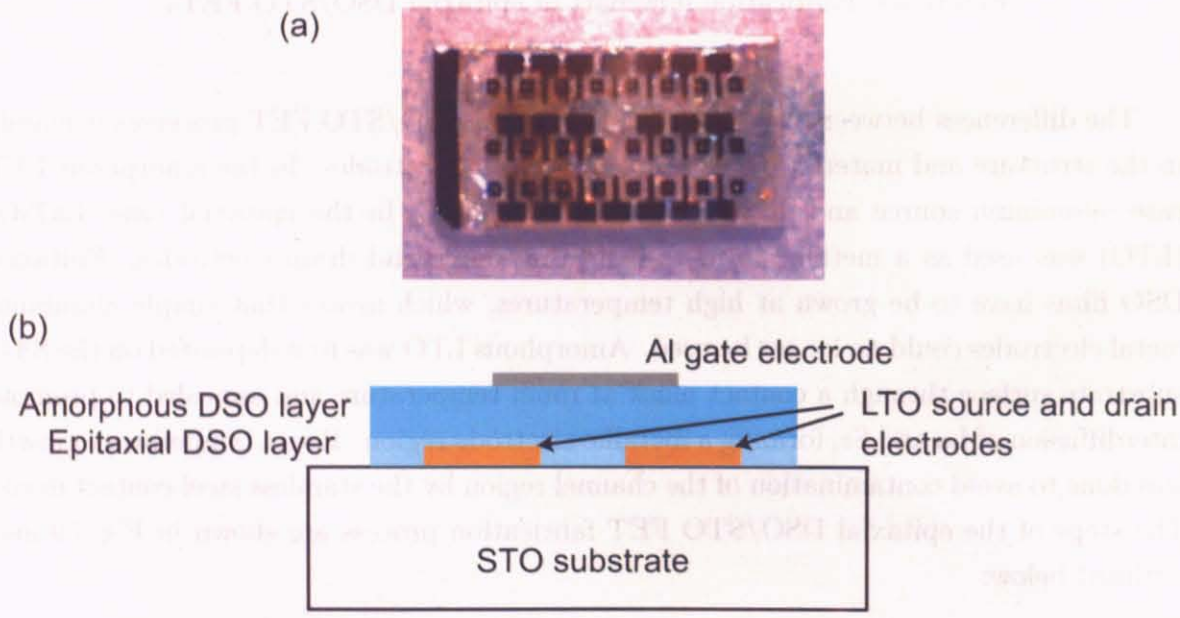

Figure 60: (a) Photograph and (b) schematic view of the epitaxial DSO/STO FET.

5.3.2 $LaTiO_3$ electrode fabrication

LTO films were fabricated for source and drain electrodes of epitaxial DSO/STO FETs. The electrode layers need to be flat and sufficiently conducting to serve as electrodes in a FET device. To achieve these goals, amorphous LTO films were deposited on STO substrates in UHV (back pressure was about 3×10^{-9} Torr) and annealed in two steps in the chamber. The first anneal was done at 800 °C, 10^{-6} Torr oxygen ambient for 30 minutes, followed by a second interdiffusion anneal at 1200 °C, 10^{-6} Torr oxygen ambient for 3 hours. It was found that a 3 unit cell-thick LTO film did not show metallic conductivity while a 4 unit cell film did show metallic conductivity. However, the 4 unit cell-thick LTO film formed nano-pillars on the film surface. These pillars had a height of a few tens of nanometers. Nano-pillar formation could be easily observed in RHEED patterns that showed extra transmission spots appearing during the annealing treatment (Fig. 62(a)). These nano-pillars can be leak sources in the FET structure, because the pillar height is comparable to the gate insulator thickness. In order to avoid such pillar formation, a two-step annealing process was developed. The first annealing step is meant to crystallize the LTO to prevent LTO forming nano-pillars. Though this treatment suppressed the formation of nano-pillar, some 3-dimensional features still existed on the film surface, as shown in Fig.62 (a), (d). As shown in Fig. 62(b), (e), a 3 unit cell LTO film had a very smooth surface when compared to the 4 unit cell LTO film. It can be concluded that 4 unit cells is a critical thickness of LTO nano-pillar formation. To avoid nano-pillar formation, 3 unit cell-thick LTO films were fabricated under various conditions, including higher temperature, lower oxygen pressure, etc. Unfortunately, metallic conductivity could not be obtained.

To enable the growth of thicker LTO layers that remain flat and metallic, a STO cap layer was introduced. It can be expected that strain from both the substrate and the STO cap layer would suppress the formation of nano-pillar without losing metallic conductivity. A 4 unit cell-thick STO / 5 unit cell-thick LTO layer on a STO substrate was processed with the same annealing treatment as discussed before. The RHEED pattern and surface morphology of tis sample are shown in Fig. 62 (c), (f). As shown in the Figure, a flat surface could be obtained when the STO capping layer was used and the layer was metallic. Contact to the electrode layer was made with a wire bonder. As shown in Fig. 61, a sufficiently conducting film could be obtained at low temperature. These LTO/STO electrodes were used in the epitaxial DSO/STO FET devices.

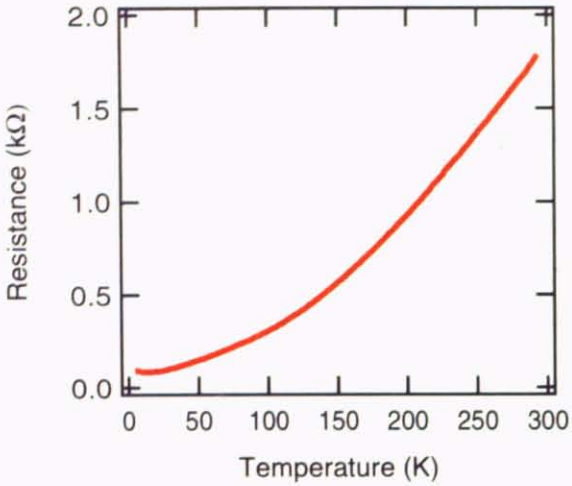

Figure 61: The temperature dependence of resistance of an annealed STO(4 u.c.) / LTO(5 u.c.) / STO heterostructure.

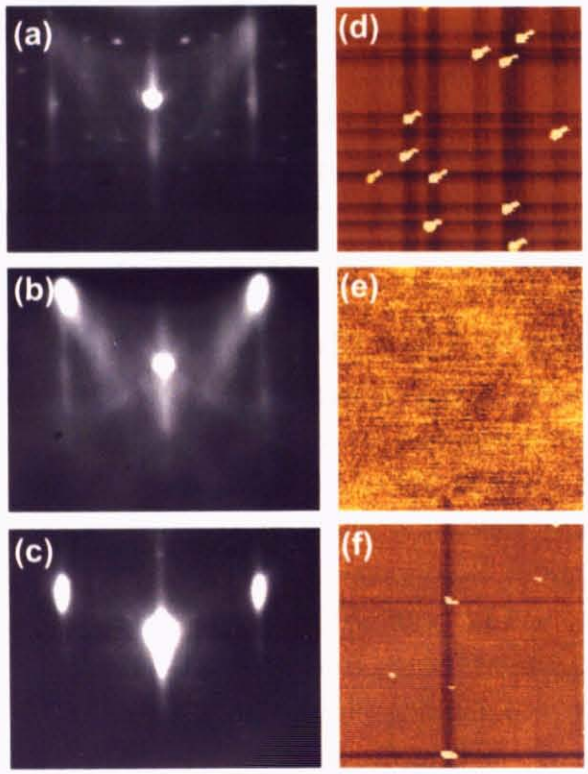

Figure 62: RHEED patterns and AFM images of annealed amorphous LTO film surfaces: (a), (d) 4 unit cells, (b), (e) 3 unit cells, and (c), (f) amorphous STO (4 u.c.) / LTO (5 u.c.) multi-layer surface. The AFM image sizes are 10 μm $\times$ 10 μm.

5.3.3 Characterization of epitaxial $DyScO_3$ / $SrTiO_3$ FETs

FETs with hetero-epitaxial channel interfaces were fabricated. The expectation was that a well-defined interface would be obtained when compared to earlier amorphous gate insulator devices. Moreover, a crystalline gate insulator can reduce the trapping state density inside the insulator layer itself. The growth conditions of the FETs using epitaxial DSO/STO interface, were as follows: first, a 5 monolayer amorphous LTO film was deposited on STO (100) single crystal in UHV, followed by 4 monolayers of amorphous STO deposited at 10^{-6} Torr of oxygen through a metal mask at room temperature. The sample was annealed in the deposition chamber, first at 800 °C for 30 minutes, followed by a second anneal at 1200 °C for 3 hours, as mentioned in Section 5.3.2. A 10 unit cell epitaxial DSO film was grown at 700 °C at 1 mTorr oxygen. The sample was annealed in air to compensate for the oxygen vacancies created during the La/Sr diffusion anneal and insulator film growth.

An AFM image of the epitaxial DSO/STO/LTO/STO surface is shown in Fig. 63. A step-and-terrace structure could be observed, but the presence of some particles reflected the nano-pillar structure that was also observed in 10 μm × 10 μm AFM images. The annealing condition was 500 °C for 12 hours. An additional 90 nm-thick amorphous DSO film was deposited to gain sufficient electrical field breakdown strength. The amorphous layer was deposited at 1 mTorr oxygen ambient at room temperature. After the amorphous layer deposition, the sample was annealed in air again. Annealing was done at 250 °C for 12 hours. Finally, the aluminum gate electrodes were evaporated through a metal mask in vacuum and source and drain contact were finished with a wire-bonding machine.

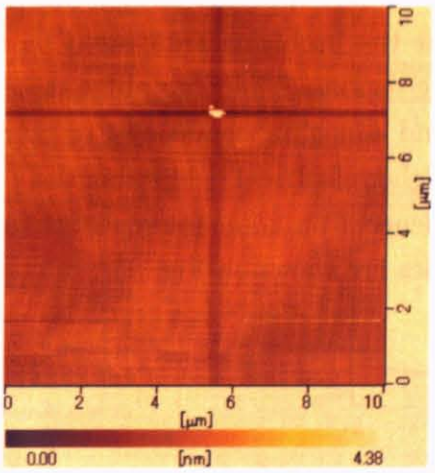

Figure 63: AFM image of the surface of an epitaxial DSO/STO/LTO/STO structure. The size of the image is 10 μm × 10μm.

The I_{DS} vs. V_{DS} room temperature data is shown in Fig. 64(a), and clear transistor action could be observed. The I_{DS} and I_{GS} as a function of V_{GS} at a fixed V_{DS} = 0.5 V, measured at room temperature are shown in Fig. 64 (b).

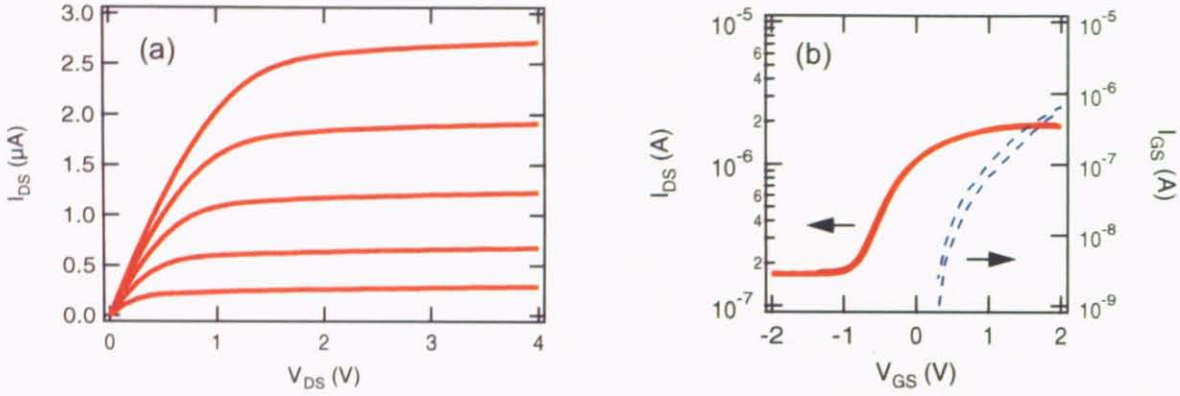

Figure 64: (a) I_{DS} vs. V_{DS} at V_{GS} of 0, 0.25, 0.5, 0.75, and 1 V. (b) I_{DS} and I_{GS} as a function of V_{GS}. V_{DS} = 0.5 V. Both measurements were done at room temperature.

This FET showed a depletion-type behavior at room temperature and this may be due to the oxygen vacancies that still exist at the epitaxial DSO/STO interface. The on-off ratio of this FET was about 10, and the field-effect mobility was 2.9 cm^2/Vs. The gate leak current, I_{GS}, was quite large. The performance of the insulating DSO layer is obviously not adequate in this device. Although amorphous DSO has sufficient field strength (more than 1 MV/cm at 100 K) as shown in Section 5.2.2, the breakdown strength of a 10 unit cell ($\approx$ 4 nm) epitaxial and 90 nm-thick amorphous DSO film was much lower, suggesting that the problems are caused by the presence of 3-dimensional islands in the LTO electrode regions. The nano-pillar structure problem has to be solved by optimizing the growth and annealing conditions, or by removing the tall islands in an etching process to obtain higher electrical field strengths.

The temperature dependence, from room temperature to 17K, of the epitaxial DSO/STO FET switching characteristics are shown in Fig. 65.

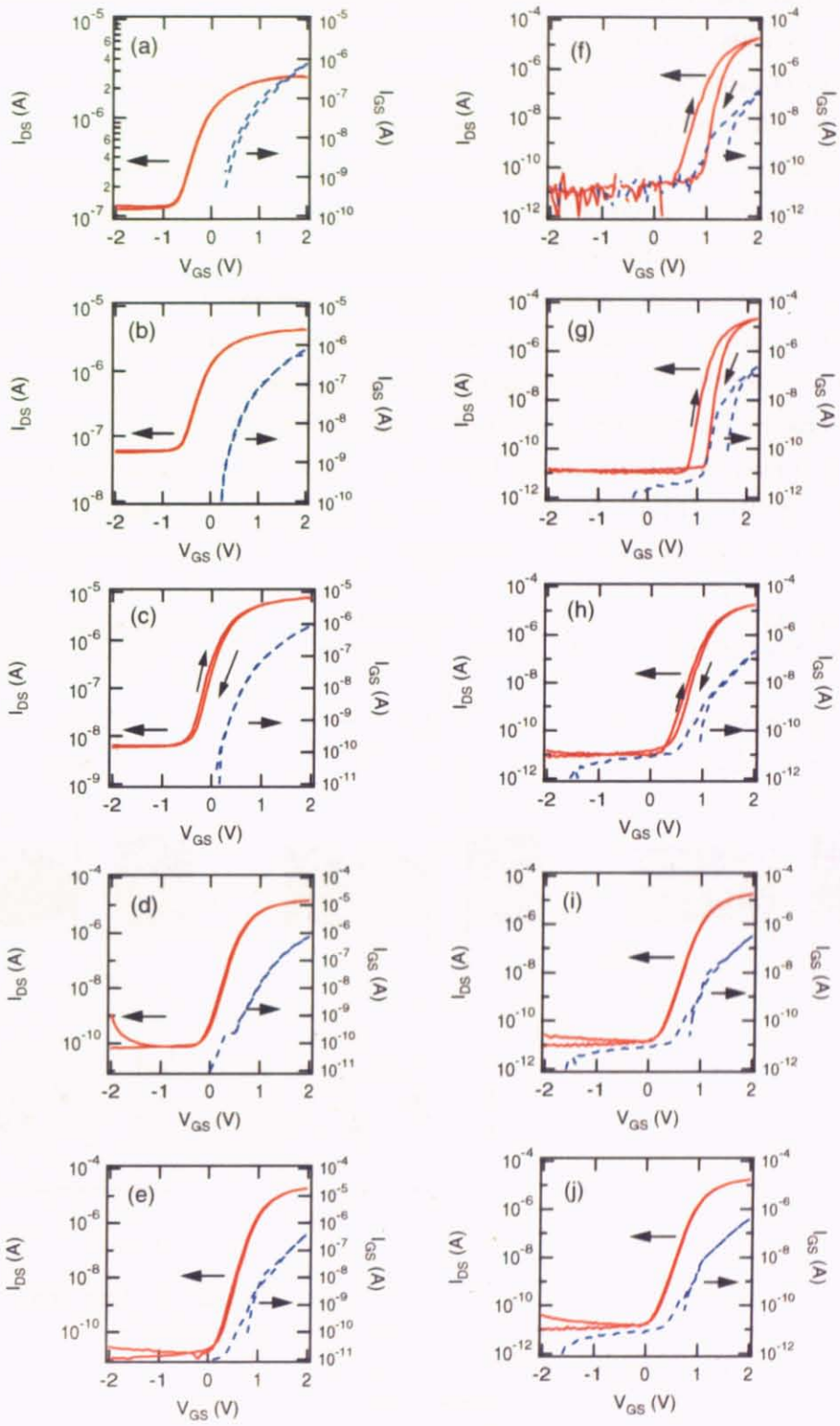

Figure 65: I_{DS} and I_{GS} as a function of V_{GS}, measured at (a) 250, (b) 200, (c) 150, (d) 100, (e) 75, (f) 60, (g) 50, (h) 40, (i) 30, and (j) 17 K.

The off-state currents were strongly suppressed at low temperature due to a decrease of thermal excitation of carriers to the conduction band of STO. At low temperature, especially at 60 and 50 K, a hysteresis behavior was clearly seen. These I_{DS}-V_{GS} curves shown in Fig. 65 also depend on the measurement history. The first measurement showed a larger hysteresis loop, and the positive to negative bias scans followed the same path. This behavior indicates that at any specific temperature, a constant number of field effect-induced carriers were trapped. The schematic drawing of this behavior is shown in Fig. 66. The presence of trap states in the insulator layer is assumed to cause the hysteresis. Close to room temperature, the trapped carriers could be easily thermally excited, but in the low temperature case, the number of carriers decreases due to strong trapping. At relatively high temperature, 50 to 60 K, some of the trapped carriers can be thermally re-excited, resulting in a hysteresis loop. In the low-temperature region, the trapped carriers can not be excited, resulting in a large hysteresis loop only during the first bias scan and after that, hysteresis could not longer be observed.

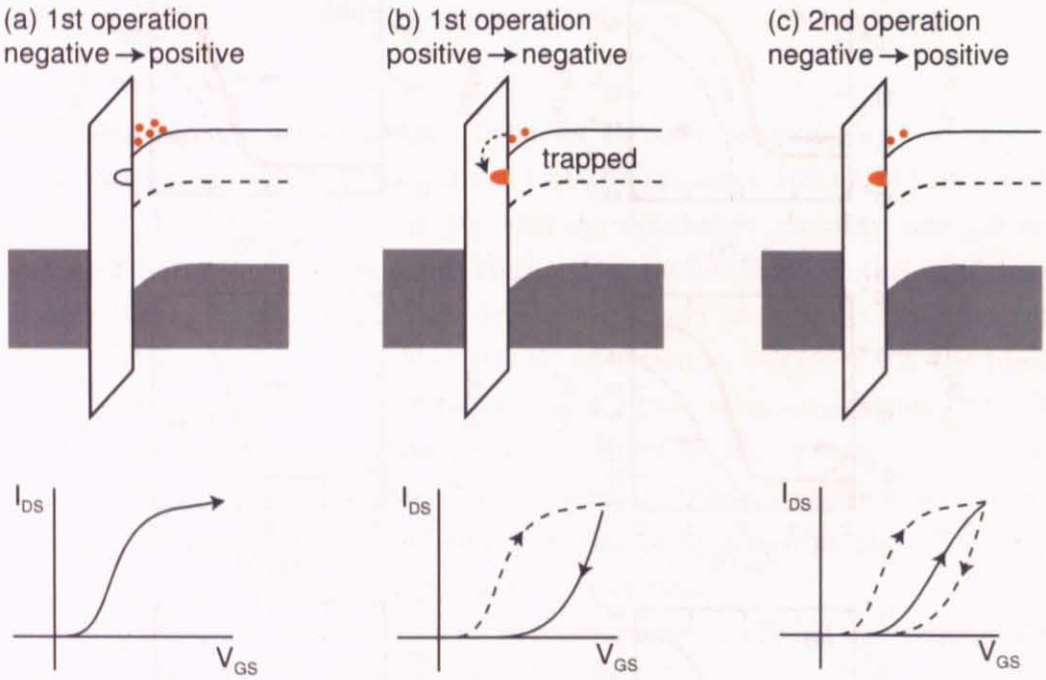

Figure 66: (a) A normal switching behavior is seen during the first scan. (b) At low temperatures, carriers are trapped by trapping sites in the insulator layer, sharply decreasing I_{DS}. (c) At 50~60 K, some of the trapped carriers can be released. In the higher temperature case, all carriers are released from the trap sites while at low temperatures all carriers remain trapped. Therefore, obvious hysteresis loop could only be observed at 50~60 K.

Temperature dependence of I_{DS}-($V_{GS} - V_{th}$) curves are shown in Fig. 67(a). This temperature dependence clearly shows that the interface of epitaxial DSO and STO became metallic. The threshold voltage shift and field-effect mobility are plotted in Fig. 67(b). The field-effect mobility curve was proportional to the T^{-2} above 100 K, and indicates that this behavior can be characterized as electron-doped STO [8]. Both threshold voltage and field-effect mobility increased monotonically until 50 K. However, the temperature dependence of threshold voltage and field-effect mobility had a peak, and below 50 K, both values dropped. The decrease of field-effect mobility is due to trapped carriers. The trapped carriers can also function as scatterers, reducing mobility in the channel. The field-effect mobility suppression at low temperature has also been observed in amorphous CHO/epitaxial CHO/STO FETs [9], amorphous Al_2O_3/STO FETs [10], and organic FETs [3, 11].

The threshold voltage shift can be understood with the help of the same model that was used in the case of amorphous DSO/STO FETs and discussed in Secion 5.2.2. However, this idea can not explain the decrease of the threshold voltage seen below 50 K. As shown in Fig. 68, V_{th} around 50 K deviated from the straight line. This result suggests that the high density states exists around 4 meV ($\approx$ 50 K) below the conduction band bottom. As is the case with amorphous FETs, the energy distribution of deep trap states can be estimated as 2.3×10^{14} cm^2/V s. This value is lower than for amorphous DSO/STO devices.

Metallic channel behavior was obtained by using an epitaxial DSO/STO interface. It was also confirmed that neither the annealing process nor the use of LTO electrodes affected the transport properties of the epitaxial FETs [9].

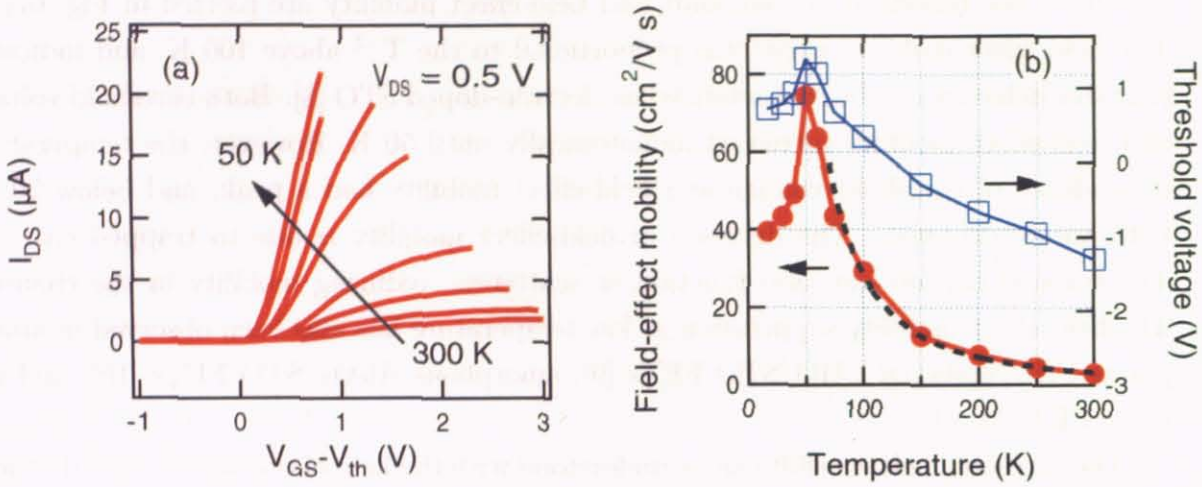

Figure 67: Temperature dependence of (a) I_{DS}-(V_{GS} - V_{th}) curve and (b) field-effect mobility (filled circle) and threshold voltage (open squre) as a function of temperature. The dashed line shows a T^{-2} fit of the field-effect mobility.

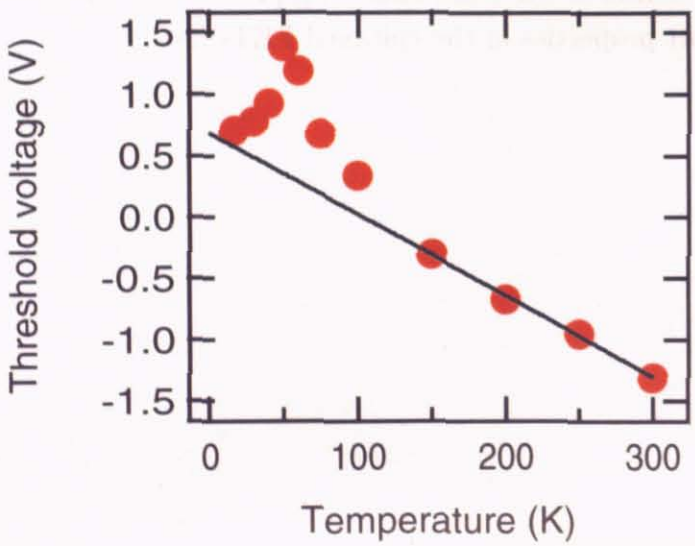

Figure 68: Linear fit (above 150 K) of V_{th} vs. temperature.

5.4 Conclusion

Amorphous and epitaxial DSO films were grown on STO (100) single crystal substrates and the electronic states of the hetero-interfaces were studied using field-effect transistor structures.

Amorphous DSO/STO FETs showed good transistor action at room temperature. The on-off ratio was larger than 10^4 and the field-effect mobility was 3.0 cm^2/Vs. At low temperature (but above 150 K), the threshold voltage sifted toward positive bias voltage side, and below 100 K, the FET no longer worked because the threshold voltage became larger than 7 V, resulting in gate insulator breakdown. The field-effect mobility slightly increased to 7.3 cm^2/Vs at 150 K. The threshold voltage sifts have been observed in many FETs using oxides, organic materials, etc., and indicates the presence of interface states. The transistor properties of amorphous DSO/STO FETs were almost comparable with amorphous CHO/STO FETs. This result indicates that the materials of gate insulator layer which are deposited using PLD are not very significant in the case of amorphous insulator devices.

STO-based FETs were also fabricated using 10 unit cell-thick epitaxial DSO/STO interfaces. To gain sufficient breakdown field strength of the gate insulator layer, additional amorphous DSO was deposited. The amorphous layer thickness was typically about 90 nm. The obtained FETs showed depletion type (normally-on) behavior at room temperature. This behavior indicates the presence of oxygen vacancies at the STO surface. The gate leak current was prominent at room temperature. The main leak source was traced to the presence of nano-pillars on the surface of the LTO-based source and drain electrodes. It is likely that further improvement of the LTO electrodes is possible, resulting in better transistor performance.

The properties of FETs based on epitaxial DSO/STO interfaces were inferior in terms of performance to amorphous devices when measured at room temperature. The on-off ratio was about 10 and the field effect mobility was 2.9 cm^2/Vs. However, unlike amorphous devices, these FETs worked even at 17 K, suggesting that the density of trapping states could be reduced dramatically from the values seen in the amorphous DSO/STO case. The field-effect mobility reached 75 cm^2/Vs at 50 K, but decreases slightly below 50 K. This behavior indicates that some interface states still exist and trapped carriers became scatterers. In this study the epitaxial layer thickness was 10 unit cells, (4 nm) and it is possible for carriers to tunnel. It can be expected that the use of thicker epitaxial layers could improve the low-temperature performance of the FETs.

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6 Conclusion

In Chapter 3, the results of absorption coefficient and photoconductivity measurements were shown. The interface states in amorphous CHO/STO heterostructures were investigated in order to understand the origin of the interface states that are known to degrade the transistor properties of amorphous CHO/STO FETs at low temperature. In photoconductivity measurements, an oxygen vacancies-related peak was obtained at 2.3 eV from the conduction band bottom of STO in amorphous CHO/STO interfaces. This peak was not observed in either clean STO substrates or amorphous CHO films. Thus it can be concluded that this peak is characteristic of an STO interface only. Annealing treatments showed that this 2.3 eV photoconductivity peak is caused by the formation of oxygen vacancies in the STO surface layer. Oxygen vacancies are created by the sputtering effect of the ablation plume during insulator layer deposition by pulsed laser deposition. Applying an annealing treatment at 300 °C for 6 hours, is effective in filling the oxygen vacancy sites and removing the 2.3 eV conductivity peak from the heterostructures. However, this treatment did not significantly improve the low-temperature properties of amorphous CHO/STO FETs. Therefore, the oxygen vacancy-related peak that was found in this study is not the main reason for carrier trapping at STO surfaces.

In order to obtain wide-gap insulator films with smoother surfaces than CHO films, NGO and DSO films were grown on STO (100) single crystal substrates under various conditions. This work is described in Chapter 4. The conditions where DSO films grew epitaxially on STO were identified, while NGO films could not be grown epitaxially on STO in this study. The crystallinity of DSO films became better at higher growth temperatures and low oxygen partial pressures. Good surface flatness was achieved in a low temperature and relatively low oxygen pressure region. Therefore, the DSO film growth conditions for field-effect device applications were selected as 700 °C, 1 mTorr oxygen ambient.

Comparison of DSO films with CHO films was done using a series of films with various thicknesses, grown on Nb:STO. It was found that DSO films are better since thicker layers can be grown while still maintaining flat surfaces. Moreover, the insulating properties of DSO are much better than CHO or NGO. The maximum average breakdown field of epitaxial DSO films reached 8 MV/cm for a thickness of 10 nm-thick. The dielectric constant of an 80 nm-thick DSO film on Nb:STO was $\approx$ 30. This value is very high compared to the reported bulk value of $\approx$ 20. This may be due to the epitaxial strain effect. It can be concluded that DSO is an excellent insulator material not only for oxide field-effect devices, but for use as a barrier in tunnel junctions as well.

In Chapter 5, fabrication and electrical characterization of amorphous DSO/STO FETs and amorphous DSO/epitaxial DSO/STO FET were reported. Although amor-

phous DSO/STO FETs showed good behavior at room temperature, with $\mu_{FE} = 3.0$ cm^2/V s and an on-off ratio of $\approx 10^4$, these transistors did not work below 100 K. As the temperature decreased, the threshold voltage of the FETs shifted towards the positive bias side. This behavior is quite similar to the amorphous CHO/STO FET case, indicating that the trapping states at the interface between the STO substrate and the insulator deposited by PLD always introduced sputtering damage.

STO based-FETs were fabricated using 10 unit cell-thick epitaxial DSO films on STO. To gain sufficient breakdown field strength of the gate insulator layer, an additional amorphous DSO layer was deposited ($\approx$ 90 nm). These FETs showed depletion-type (normally-on) switching and the gate leak current was very high at room temperature. This behavior was explained by the presence of oxygen vacancies at the STO surface. The presence of nano-pillars on the surface of the LTO-based Source and Drain electrodes used in the epitaxial devices were the likely gate leak sources. Further work on improving the LTO electrode fabrication would result in better transistor performance.

The properties of FETs using epitaxial DSO/STO interfaces were inferior in terms of performance to amorphous devices when measured at room temperature, with $\mu_{FE} = 2.9$ cm^2/V s and an on-off ration of $\approx$ 10. However, unlike amorphous devices, these FETs worked even at 17 K. This result indicates that the density of trapping states could be reduced dramatically from the values seen in the amorphous-only case. The μ_{FE} reached 75 cm^2/V s at 50 K, but decreased slightly below 50 K. The threshold shifts were still observed as in the case of amorphous DSO/STO or other FETs. In epitaxial DSO/STO interfaces, the threshold voltage shift dropped below 50 K, just like μ_{FE}. This result suggests that the trapped carriers could not escape from trapping states by thermal activation. Apparently, some interface states still existed and trapped carriers became scatterers.

In this study, the epitaxial layer was only 10 unit cells thick ($\approx$ 4 nm) and it is possible for carriers to tunnel. The probability of tunneling exponentially decreases with the distance. Therefore, it can be expected that the use of a thicker epitaxial layer or down-sizing the devices could improve the low temperature performance of the FETs.

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