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$SrTiO_3$ field effect transistor with $SrTiO_{3-\delta}$ source and drain electrodes

$SrTiO_{3-\delta}$をソース・ドレイン電極に用いた$SrTiO_3$電界効果トランジスタ

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Introduction

Strontium titanate ($SrTiO_3$) is a perovskite that is generating increasing interest as an insulator with a high dielectric constant, as a model system for para- and ferroelectricity, and as one of the best candidates for producing various microelectronic heterostructures when combined with other perovskite materials. High-performance devices based on perovskite-type transition-metal oxides require the fabrication of heterointerfaces with well-controlled electronic properties. Unfortunately, the electronic states that appear at interfaces are not well understood and it is therefore difficult to control device performance. Manipulating the density of carriers in transition-metal oxides without losing crystalline order is very important for the investigation of electronic properties of interfaces. One way to probe the electronic properties is to construct a field-effect transistor (FET) and measure changes in transport properties of thin interface layers as the carrier density is modulated by field effect. In order to probe the electronic structure of epitaxial $SrTiO_3$ heterointerfaces, we have fabricated $SrTiO_3$ (100) single crystal FETs with either amorphous or epitaxial $CaHfO_3$ gate insulator layers [1]. The field-effect performance of FET with amorphous interfaces is limited by trap states that are in the vicinity of the channel interface and also close to the Fermi level of the channel material ($SrTiO_3$).

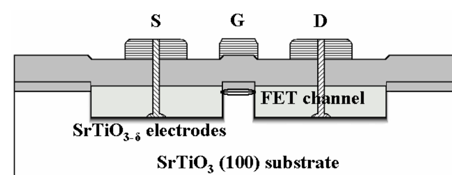

Fig.1. Schematic view of the $SrTiO_3$ FET structure.

To address these issues, a new process was developed for fabricating $SrTiO_3$ FETs. The biggest difficulty of the new process is obtaining an electronically clean heterointerface by conventional oxide thin film growth techniques, such as pulsed laser deposition. Epitaxial layers need to be grown at a high temperature, which brings additional challenges because in addition to the channel layer and the gate insulator, it is also necessary to integrate metallic source and gate electrodes into a transistor device. In order to do this, I have developed a new process for fabricating $SrTiO_3$ FETs based on $CaHfO_3$ gate insulators and source and drain electrodes composed of metallic oxygen-deficient $SrTiO_{3-\delta}$.

After developing new process, careful analysis of the temperature dependence of the transport properties of the $SrTiO_3$ FETs can be used to obtain information on the presence of interface states in an oxide heterostructure.

Experiment

The transistors were fabricated on $5\times10\times0.5\text{mm}^3$ as-supplied $SrTiO_3$(100) single crystal substrates. As a first step, amorphous $CaHfO_3$ gate insulator layers were grown by pulsed laser deposition (PLD) at an oxygen pressure of 3 mTorr. A KrF excimer laser operating at 3 Hz was used for ablation and the laser fluence was 0.7 J/cm^2. After constructing the critical channel interface, the source and drain electrodes of metallic oxygen-deficient $SrTiO_{3-\delta}$ were formed by Ar^+ ion milling at an acceleration voltage of about 500 V. This is an efficient way of introducing oxygen vacancies into a thin surface layer of $SrTiO_3$. These

vacancies function as donors, inducing metallic conductivity in the electrode regions. This technique can be used to obtain clean interfaces, suppress the formation of lattice imperfections, and avoid impurities because the active channel interface is constructed at an early step of the device fabrication process. The pits formed by milling the source and drain electrodes in $SrTiO_3$ were filled by thermal evaporation of SiO_x. For improving the gate breakdown strength of the FETs, a second amorphous $CaHfO_3$ gate insulator layer was grown by PLD, covering the whole device. Electrical contact to the $SrTiO_{3-\delta}$ source and drain electrodes was made by Al wire bonding. A schematic view of a $SrTiO_3$ field effect transistor, fabricated by the new process, is shown in Fig.1.

Several electrode geometries were explored in this work. The most simple devices only contain two contacts, the source and the drain and only 2-point measurements are possible. For 4-point measurements of channel resistivity, FETs with two additional electrodes either crossing the channel region or attaching to the side of the channel area were also fabricated. These additional electrodes were used for 4-point measurements of channel resistivity. The measurement geometry and a photograph of a device are shown in Fig.2.

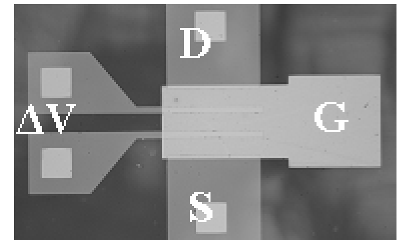

Fig.2. photograph of a $SrTiO_3$ FET with two potential electrodes inside the channel region.

Results and Discussion

An FET with amorphous $CaHfO_3$ gate insulator layers showed a field effect mobility of $2.5 cm^2/Vs$ at room temperature. The off current was very low, about 10 pA, and on-off ratio was higher than 10^6. As shown in Fig.3 (a), the threshold voltage (V_{th}) shifted towards the positive bias side at low temperature. This suggests the presence of interface trap states. This threshold shift phenomenon has also been observed in perovskite oxide based amorphous Al_2O_3 / $KTaO_3$, organic, carbon nanotube, and fullerene based FETs.

I_{DS} as a function of V_{GS} after subtracting the threshold voltage is shown in Fig. 3 (b). It is noteworthy that the field-effect mobility increased at low temperature. This means that the carriers induced by field effect behaved as would be expected for metallic electron-doped $SrTiO_3$. This result confirmed that the FETs fabricated with the new process showed a clear advantage when compared to earlier amorphous $CaHfO_3$ FETs that used aluminum electrodes.

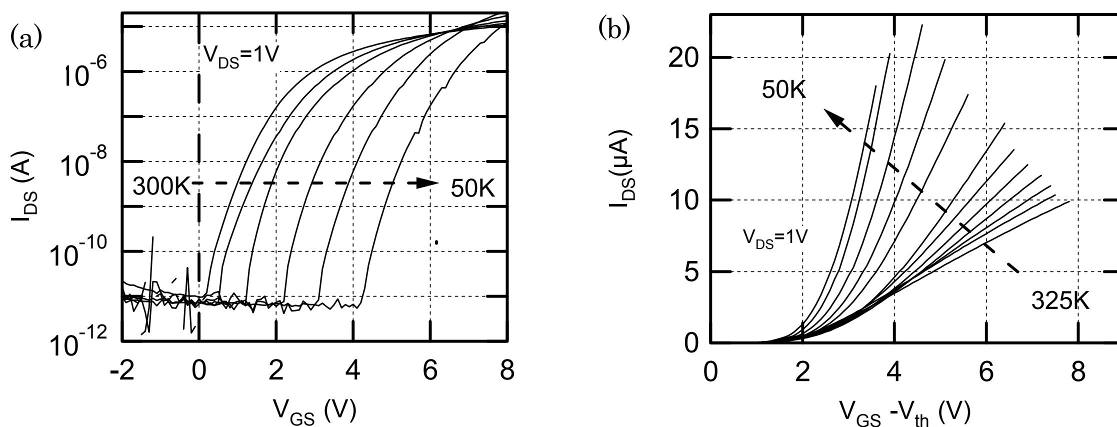

Fig.3. (a)The drain-source current as a function of gate at various temperatures of a FET with an amorphous gate insulator. (b) I_{DS} as a function of V_{GS} at various temperature plotted after subtracting the threshold voltage.

For more accurate channel resistivity measurements, FETs with two potential electrodes inside the channel region were fabricated.

The performance of the FET with amorphous $CaHfO_3$ gate insulator layers is shown in Fig.3. In this FET, a threshold voltage shift towards positive bias was also seen. As shown in Fig.3 (b), the slope of I_{DS} as a function of V_{GS} after subtracting the threshold voltage also rose.

Next, I turn to the details of low temperature characterization of the $SrTiO_3$ FETs. Fig.4 (b) shows the sheet resistance as a function of V_{GS} after subtracting the threshold voltage. Here, the threshold voltages are determined from a linear fit of the square root plots of I_{DS}. The capacitance per unit area of the $CaHfO_3$ gate insulator of this FET was $C_i = 172$ nF/cm^2. the effective sheet carrier density can be estimated by $C_i (V_G - V_{th})$. With increasing gate voltage, sheet resistance fell drastically from GΩ to the order of kΩ. In addition, an decrease of the sheet resistance was observed with reducing temperature. This means that the carriers induced by the field effect behaved same as normal FETs in this study.

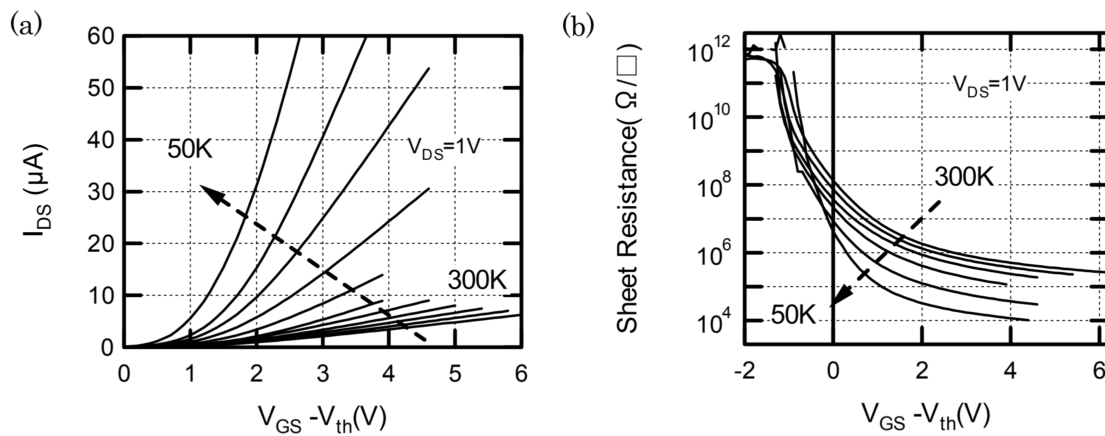

Fig.4. (a)The drain- source current as a function of the gate bias at various temperatures of a FET with two potential electrodes. (b) Sheet resistance as a function of V_{GS}, plotted after subtracting the threshold voltage.

Summary

In summary, a new process has been developed for reducing the density of defects in the channel region of an oxide FET. An insulator-metal transition, induced by field-effect doping, was observed in $SrTiO_3$ single crystal FETs with $SrTiO_{3-\delta}$ source and drain electrodes. $SrTiO_3$ FETs with two potential electrodes inside the channel region were used to measure the channel resistivity. With increasing gate voltage, sheet resistance dropped from several GΩ to the order of kΩ was observed in this FET.

[1] K.Shibuya et al., Appl.Phys.Lett. **88,**212116 (2006).