## Chapter 6

# Fabrication and electronic properties of $SrTiO_3$-based field-effect transistors with amorphous insulator layers

### 6-1 Introduction

The field-effect transistor (FET) is a transistor that relies on an electric field to control the conductivity of a channel in a semiconductor material. The principle behind the field effect transistor is the idea of repelling or attracting charge carriers in a material by applying an external electric field. This remarkably simple principle causes significant changes in the on and off states of a transistor. Many groups have extended this principle to perovskite-type transition metal oxides materials [1, 2, 3, 4, 5, 6, 7].

The operating mechanism of a FET is shown in Figure 6.1. The FET structure is essentially a metal-insulator-semiconductor (MIS) trilayer structure, the MISFET. The energy diagrams in Fig. 6.1 show the case of an n-type semiconductor and the FET is thus of accumulation type. If a positive voltage is applied to the metal gate electrode, the top of the conduction band bends downward and moves closer to the Fermi level. In an ideal MIS diode, no current flows in the structure and the Fermi level remains at a constant energy level in the semiconductor. Since the carrier density depends exponentially on the energy difference ($E_C$ - $E_F$), this band bending causes an accumulation of carriers near the semiconductor surface.

In this work, the same mechanism was studied at an interface between $SrTiO_3$ (n-type Semiconductor) and $CaHfO_3$ (Insulator).

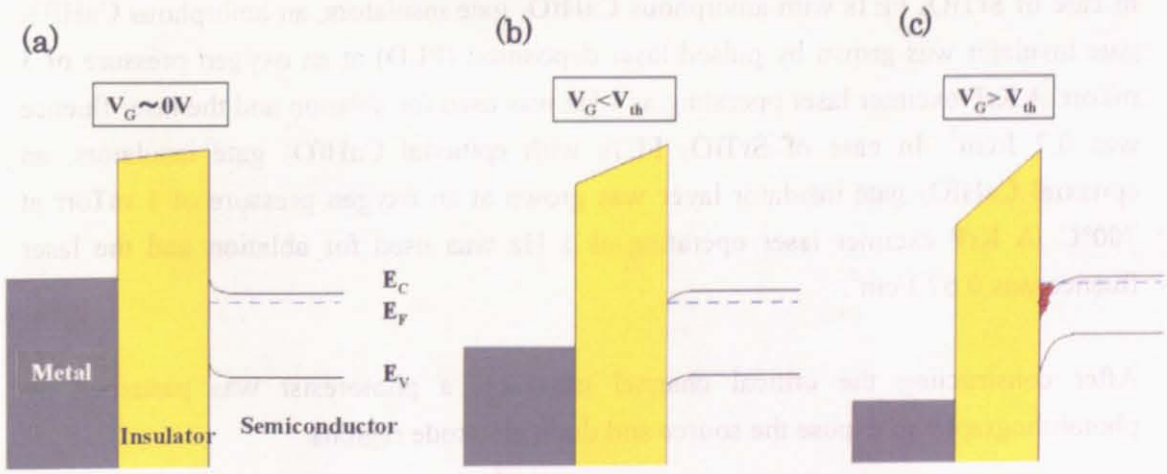



Figure 6.1 The operating mechanism of a FET.

## 6-2 New fabrication process of $SrTiO_3$ FETs

To probe the physical properties of transition metal oxides, field-effect transistors were fabricated and the effect of modulating the carrier density by the field effect on the transport properties of a thin interface layer were measured. In earlier work, $SrTiO_3$ (100) single crystal FETs with either amorphous or epitaxial $CaHfO_3$ gate insulator layers were studied [8, 9]. It was found that the field-effect performance of FETs with amorphous interfaces is limited by trap states that are in the vicinity of the channel interface and also close to the Fermi level of the channel material ($SrTiO_3$).

To address these issues, a new process was developed for fabricating $SrTiO_3$ FETs. The aim of the new process was to obtaining an electronically clean heterointerface by conventional oxide thin film growth techniques, such as pulsed laser deposition. Epitaxial layers need to be grown at a high temperature, which brings additional challenges because in addition to the channel layer and the gate insulator, it is also necessary to integrate metallic source and gate electrodes into a transistor device. In order to do this, a new process was developed for fabricating $SrTiO_3$ FETs based on $CaHfO_3$ gate insulators and source and drain electrodes composed of metallic oxygen-deficient $SrTiO_{3-\delta}$.

After developing the new process, careful analysis of the temperature dependence of the transport properties of the $SrTiO_3$ FETs can be used to obtain information on the presence of interface states in an oxide heterostructure.

The flowchart of the new fabrication process of $SrTiO_3$ FETs is shown in Figure 6.2. the fabrication steps illustrated in Figure 6.2 are the following:

1. The transistors were fabricated on $5\times10\times0.5mm^3$ as-supplied $SrTiO_3$(100) single crystal substrates.

2. In case of $SrTiO_3$ FETs with amorphous $CaHfO_3$ gate insulators, an amorphous $CaHfO_3$ gate insulator was grown by pulsed laser deposition (PLD) at an oxygen pressure of 3 mTorr. A KrF excimer laser operating at 3 Hz was used for ablation and the laser fluence was 0.7 $J/cm^2$. In case of $SrTiO_3$ FETs with epitaxial $CaHfO_3$ gate insulators, an epitaxial $CaHfO_3$ gate insulator layer was grown at an oxygen pressure of 1 mTorr at 700°C. A KrF excimer laser operating at 1 Hz was used for ablation and the laser fluence was 0.67 $J/cm^2$.

3. After constructing the critical channel interface, a photoresist was patterned by photolithography to expose the source and drain electrode regions.

4. The source and drain electrodes of metallic oxygen-deficient $SrTiO_{3-\delta}$ were formed by Ar ion milling the sample surface through the opening is in the photoresist layer at an

acceleration voltage of about 500 V at 10 sccm Ar gas flow for 11 minutes. This is an efficient way of introducing oxygen vacancies into a thin surface layer of $SrTiO_3$. These vacancies function as donors, inducing metallic conductivity in the electrode regions. This technique can be used to obtain clean interfaces, suppress the formation of lattice imperfections, and avoid impurities because the active channel interface is constructed at an early step of the device fabrication process.

5. The pits formed by milling the source and drain electrodes in $SrTiO_3$ were filled by thermal evaporation of $SiO_x$.

6. The $SiO_x$ and photoresist were removed by lift-off.

7. For improving the gate breakdown strength of the FETs, a second amorphous $CaHfO_3$ gate insulator layer was grown by PLD, covering the whole device. A KrF excimer laser operating at 3 Hz was used for ablation and the laser fluence was about 0.7 J/cm$^2$, same as for the first amorphous $CaHfO_3$ layer.

8. Photoresist was patterned through photolithography process to form openings for the gate electrodes.

9. Al gate electrodes were formed on the gate insulator by thermal evaporation.

10. Electrical contact to the buried $SrTiO_{3-\delta}$ source and drain electrodes were made by wire-bonding Al wires to the film surface, crushing the insulating layers above the oxygen-deficient electrodes and making contact with the Al pads on the surface.

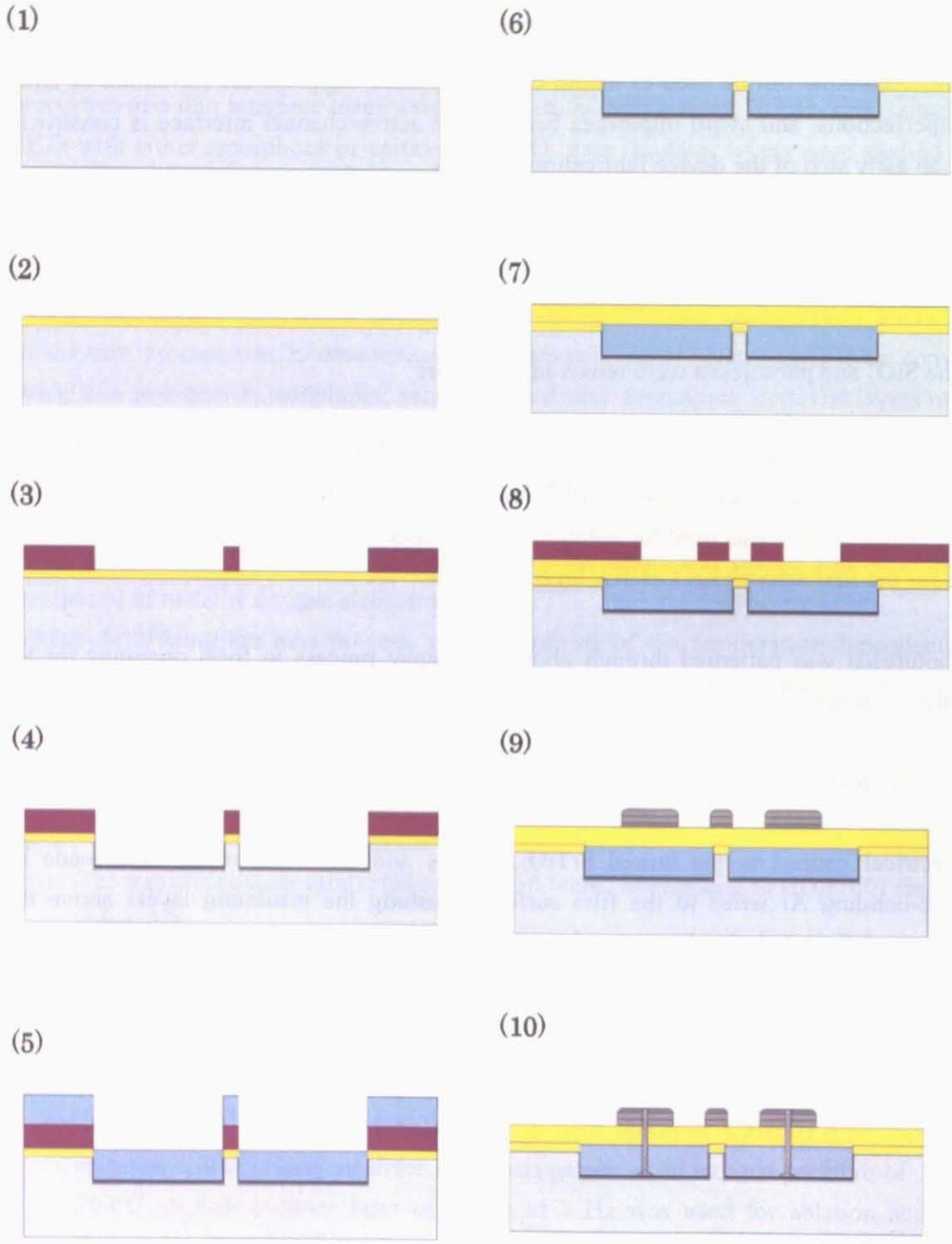
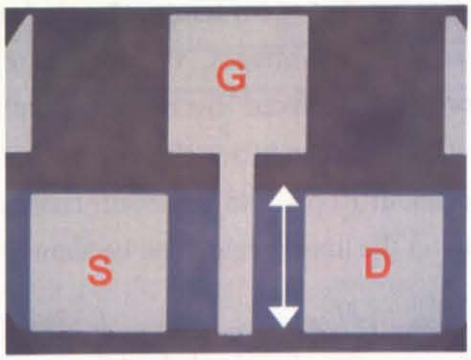



Figure 6.2 The fabrication steps of new process.

A photograph of the $SrTiO_3$ FET fabricated by new process is shown in Figure 6.3. The channel length (L) and width (W) of this device were 100 and 500 μm, respectively. The dimensions were the same as in previous work that used an earlier process [8, 9].

Post-annealing of the devices was done in a furnace at 300 °C for 6 hours after constructing amorphous $CaHfO_3$ or at 400 °C for 12 hours after constructing epitaxial $CaHfO_3$ between steps 2 and 3 to reduce the density of oxygen vacancies in $SrTiO_3$.




**500μm**

Figure 6.3 A photograph of the $SrTiO_3$ FET fabricated by the new process.

## 6-3 Characterization of $SrTiO_3$ FETs with an amorphous $CaHfO_3$ gate insulator

The devices fabricated by the new process included two amorphous $CaHfO_3$ layers. The thickness of the first amorphous $CaHfO_3$ layer which contact with a channel region of $SrTiO_3$ was 18 nm and the thickness of the second amorphous $CaHfO_3$ layer, which covered the first amorphous $CaHfO_3$ layer was 57 nm. Both of these were grown by PLD at an oxygen pressure of 3 mTorr. A KrF excimer laser operating at 3 Hz was used for ablation and the laser fluence was 0.7 J/cm$^2$, resulting in a growth rate of about 0.04 Å/pulse. The depth of Ar ion milled $SrTiO_3$ was 48 nm, and the thickness of $SiO_X$ which filled the pits was 33 nm. The thickness of the Al gate electrode was 30 nm.

The drain-source current, $I_{DS}$, measured at room temperature, is plotted as a function of the drain-source bias, $V_{DS}$, under various gate voltages, $V_{GS}$, in Figure 6.4 (a). The $I_{DS}$ and gate leak current, $I_{GS}$, as a function of $V_{GS}$ for a fixed $V_{DS}$ of +1V are plotted in Figure 6.4 (b). In these measurements, a Keithley 4200 semiconductor characterization system was used.

The off current was very low, at about 10 pA, and the on-off channel current ratio was higher than $10^6$. The field-effect mobility in the linear region can be shown to be

$$\mu_{FE} = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const} \frac{1}{C_i V_{DS}} \frac{L}{W}$$

where $C_i$ is the sheet capacitance of the insulator. The sheet capacitance of the insulator is defined by

$$C_i = \frac{\varepsilon_{CHO} \cdot \varepsilon_0}{t}$$

where $\varepsilon_{CHO}, \varepsilon_0$ are the dielectric constant of the $CaHfO_3$ insulator layer and the permittivity of free space. The dielectric constant of the $CaHfO_3$ insulator layer was assumed to be $\varepsilon_{CHO} = 14$, based on measurements of amorphous $CaHfO_3$ insulator layers [10]. In this device, the sheet capacitance of the insulator was thus $C_i$ = 165 nF/cm$^2$. The field-effect mobility was 2.5 cm$^2$/V s.

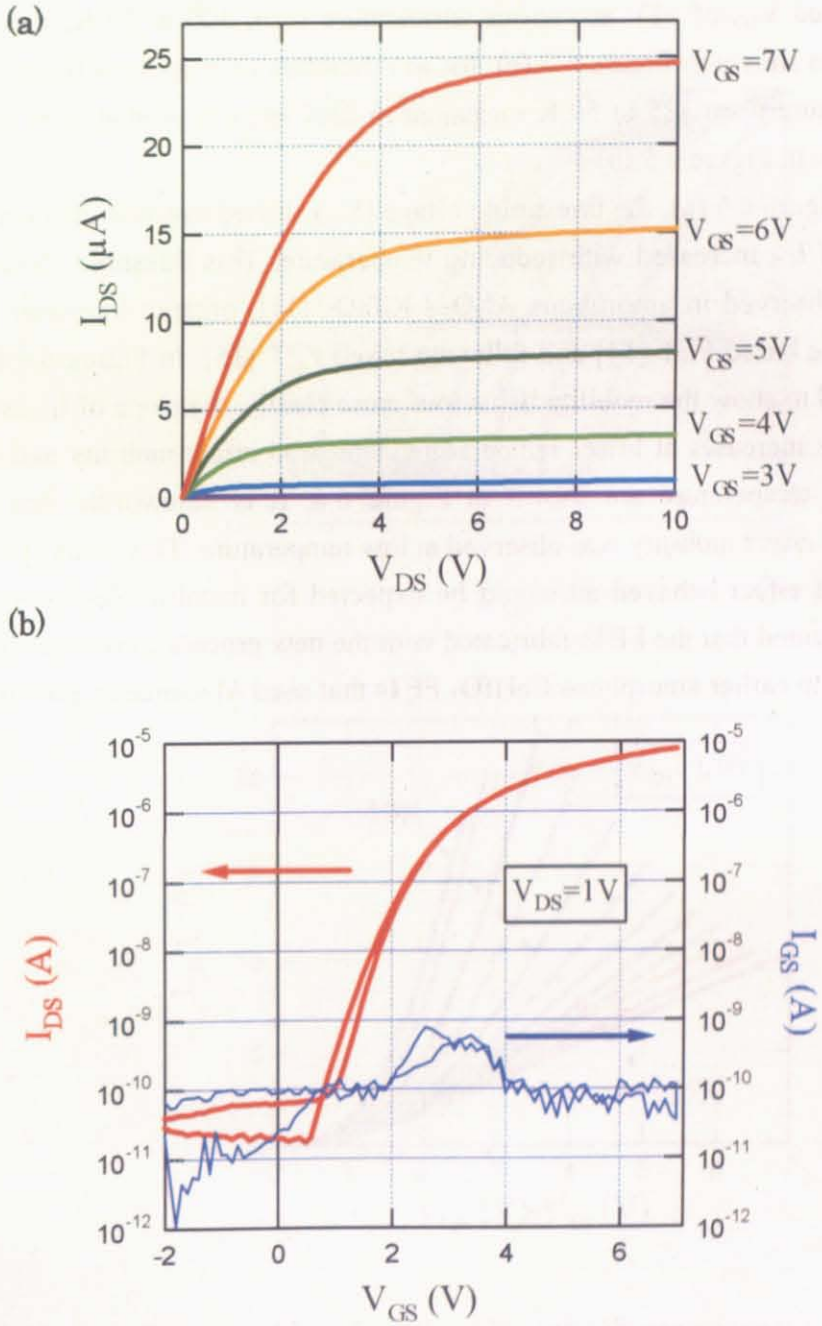
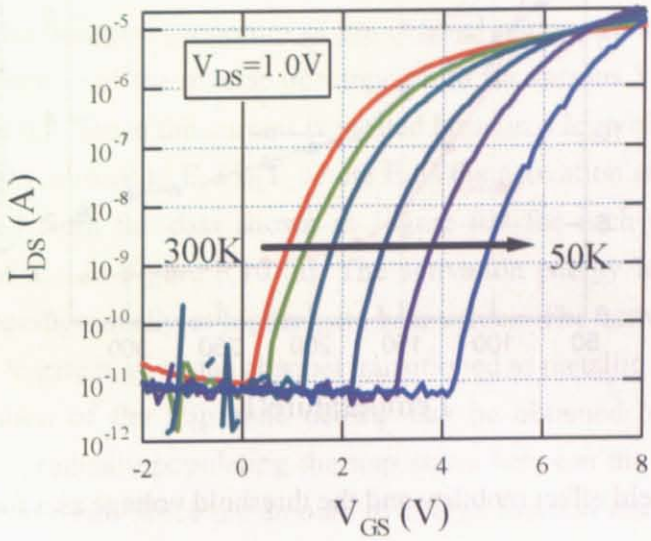



Figure 6.4 (a) $I_{DS}$, measured at room temperature, is plotted as a function of $V_{DS}$, for various gate bias values $V_{GS}$. (b) $I_{DS}$ and $I_{GS}$, as a function of $V_{GS}$ for a fixed $V_{DS}$ of +1V.

The temperature dependence of the FET properties was measured from 325 K to 50 K for studying the physical properties at the amorphous $CaHfO_3/SrTiO_3$ interface. $I_{DS}$ as a function of $V_{GS}$ for a fixed $V_{DS}$ of +1V at various temperature form 300 to 50 K, measured in 50K steps, of a FET is shown in Figure 6.5 (a). $I_{DS}$ as a function of $V_{GS}$, for a fixed $V_{DS}$ of +1V at various temperature from 325 to 50 K measured in 25K steps is plotted after subtracting the threshold voltage in Figure 6.5 (b).

As shown in Figure 6.5 (a), the threshold voltage ($V_{th}$) shifted towards the positive bias side and the slope of $I_{DS}$ increased with reducing temperature. This threshold shift phenomenon has also been observed in amorphous $Al_2O_3$ / $KTaO_3$ [11], organic transistor [12, 13], the carbon nano-tube based FET [14] and fullerene based FET [15]. In Figure 6.5 (b) where the data is re-plotted to show the mobility behaviour more clearly, the slope of $I_{DS}$ as a function of $V_{GS}$ - $V_{th}$ clearly increases at lower temperature. The field effect mobility and the threshold voltage at each temperature are shown in Figure 6.6. It is noteworthy that a significant increase of field-effect mobility was observed at low temperature. This means that the carriers induced by field effect behaved as would be expected for metallic electron-doped $SrTiO_3$. This result confirmed that the FETs fabricated with the new process showed a clear advantage when compared to earlier amorphous $CaHfO_3$ FETs that used Al source and drain electrodes.

(a)




(b)

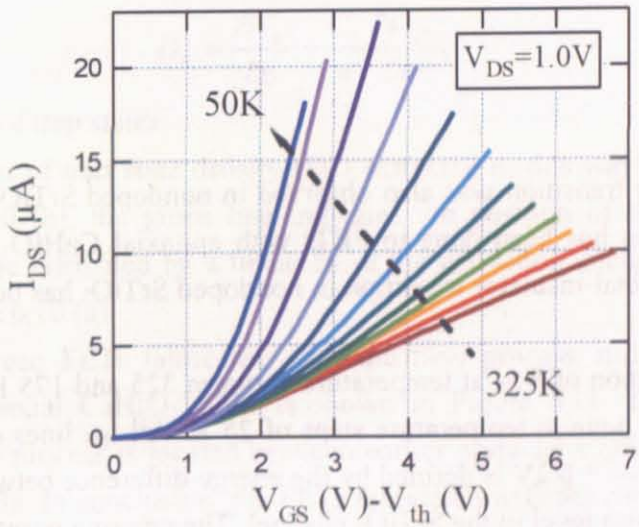



Figure 6.5 (a) $I_{DS}$ as a function of $V_{GS}$ for a fixed $V_{DS}$ of +1V at various temperature form 300 to 50 K measured in 50K steps of the FET. (b) $I_{DS}$ as a function of $V_{GS}$, for a fixed $V_{DS}$ of +1V at various temperatures from 325 to 50 K measured in 25K steps, plotted after subtracting the threshold voltage.

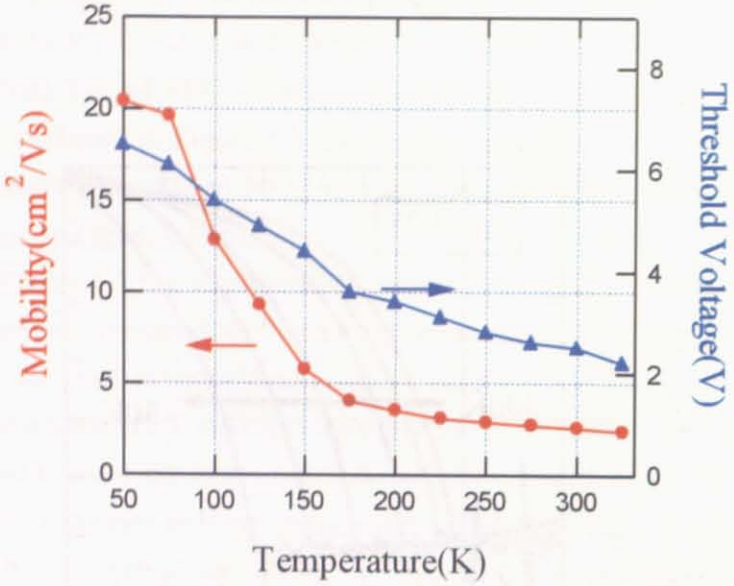



Figure 6.6 The field effect mobility and the threshold voltage as a function of temperature.

A metal-insulator transition was also observed in nondoped $SrTiO_3$ by a field effect in this amorphous FET, as has been done in FETs with epitaxial $CaHfO_3$ gate insulators [9]. The mechanism of a metal-insulator transition in nondoped $SrTiO_3$ has been discussed in detail by Shibuya [10, 16].

The $I_{DS}$ as a function of $V_{GS}$ at temperature between 325 and 175 K is shown in Figure 6.7. Measurement was done in temperature steps of 25 K. All $I_{DS}$ lines cross at a single point of $V_{GS} = 6.2V$. The $V_{GS} = 6.2V$ is defined by the energy difference between the conduction band bottom and the Fermi level in the $SrTiO_3$ channel. The crossing point is therefore independent of temperature.

The sheet resistance of the channel region as a function of temperature at various $V_{GS}$ is shown in Figure 6.8. As shown in Figure 6.8, the sheet resistance decreased at low temperatures when the $V_{GS}$ was above the critical gate bias ($V_{GS} = 6.2V$) and increase when the $V_{GS}$ was below the critical bias. That means that the channel was in a metallic state when the gate bias exceeded the critical value and insulating if the gate bias was smaller than the critical value. This behaviour can be understood if we assume that the Fermi level in $SrTiO_3$ is originally located slightly below the conduction band bottom, within localized states. At low gate bias values, therefore, the conductivity is thermally activated. As the gate bias is increased, the chemical potential shifts higher, until it reaches the conduction band bottom

and the channel layer becomes metallic. The temperature dependence shown in Figure 6.8 could only be analyzed above about 150 K. At lower temperatures, the threshold values of the transistors started to be shifted due to trapping in the insulator, making reliable comparison of $I_{DS}$ plots impossible.

In order to analyze the transport properties of the channel region in the insulating state, the channel current as a function of the inverse of temperature for various $V_{GS}$ below the critical $V_{GS}$ is shown in Figure 6.9. Since the current is plotted here on a logarithmic scale, the slope of channel current is proportional to $E_a / k_B T$, where $E_a$ is the activation energy. The activation energies were extracted from the data shown in Figure 6.9 for each temperature and are shown as a function of $V_{GS}$ in Figure 6.10 (a). The activation energy at zero gate bias was about 0.2 eV and dropped gradually at higher gate bias values. The activation energy finally disappeared at about 6 V gate bias, as the channel transitioned to metallic state.

The energy distribution of the trap state density can be obtained by assuming that an increase of gate bias is gradually populating the trap states between the Fermi level and the bottom of the conduction band. Since the amount of charge injected into the device by field effect is known from the capacitance of the gate stack, the trap state density can also be estimated.

$$D_{tr} = \frac{\partial N_{tr}}{\partial E} = \frac{C_i}{e}\frac{\partial V_{GS}}{\partial E},$$

where $N_{tr}$ is the density of trap states.

The energy distribution of trap state density ($D_{tr}$) extracted in this way is shown in Figure 6.10 (b). In Figure 6.10 (b), the green line indicates the position of the Fermi level, the position of which can be estimated by a linear fit of the activation energy plot for low gate bias, as shown in Figure 6.10 (a).

The comparison between FETs fabricated with the new process and earlier amorphous $CaHfO_3$ FETs and epitaxial $CaHfO_3$ FETs is shown in Figure 6.11. The $D_{tr}$ of the FET fabricated with the new process is located between earlier epitaxial $CaHfO_3$ FET and earlier amorphous $CaHfO_3$ FETs. In conclusion, the FETs fabricated with the new process showed a clear advantage for earlier amorphous $CaHfO_3$ FETs with different process. The main reason for this was that the initial channel interface was deposited in the first step of device fabrication, before starting to define the source and drain electrodes. The contamination of the substrate surface was thus reduced and consequently the observed trap density was dramatically lowered.

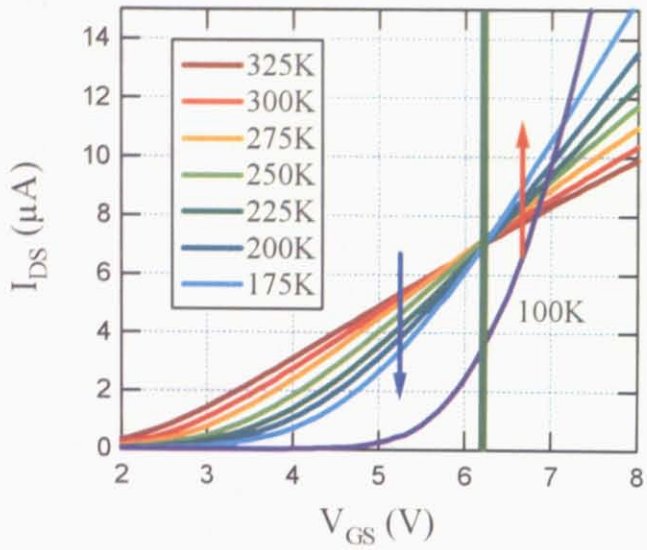



Figure 6.7 The $I_{DS}$ as a function of $V_{GS}$ at temperature varied from 325 at 175 K in 25 K steps.

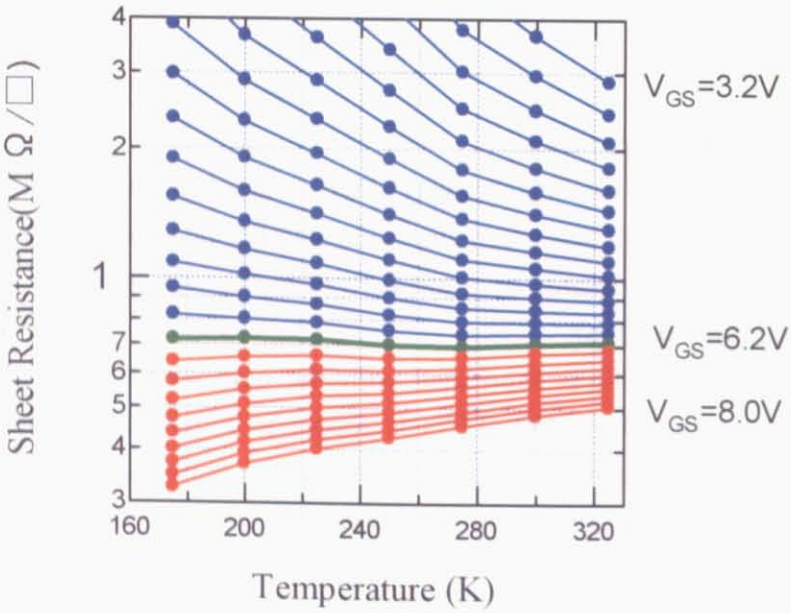



Figure 6.8 The sheet resistance of the channel region as a function of temperature at various $V_{GS}$.

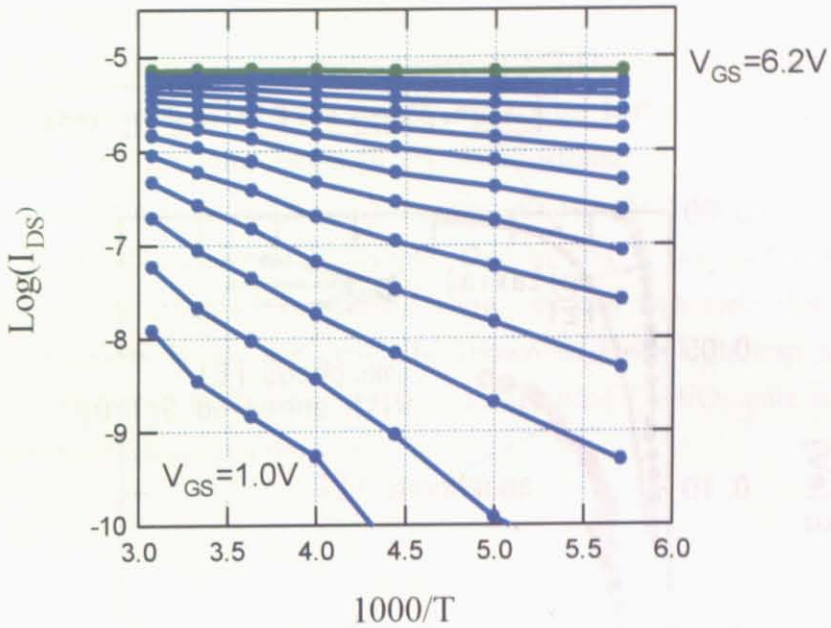



Figure 6.9 The channel current as a function of the inverse temperature for various gate voltages below the critical $V_{GS}$.

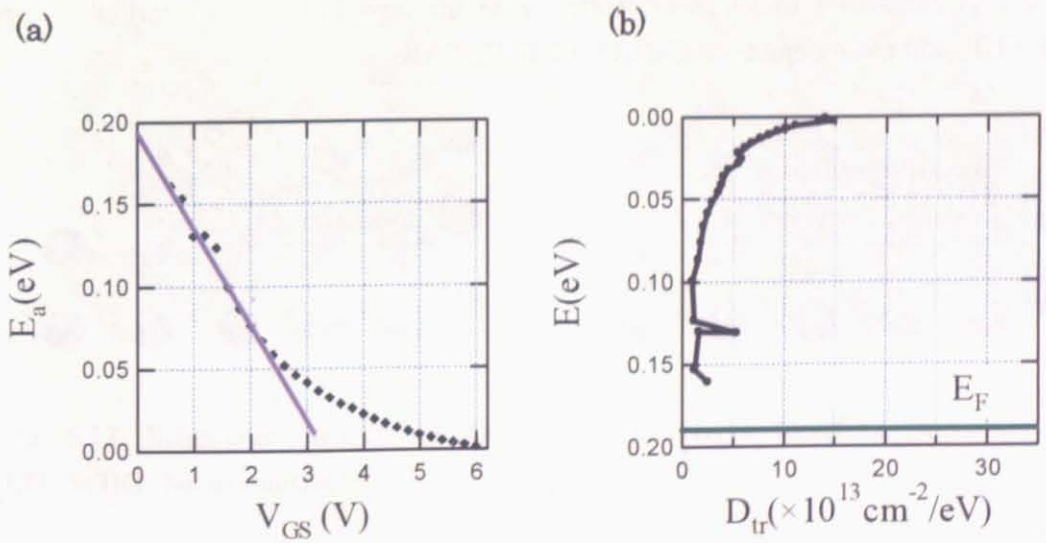



Figure 6.10 (a) The activation energy as a function of $V_{GS}$ (b)The energy distribution of trap state density.

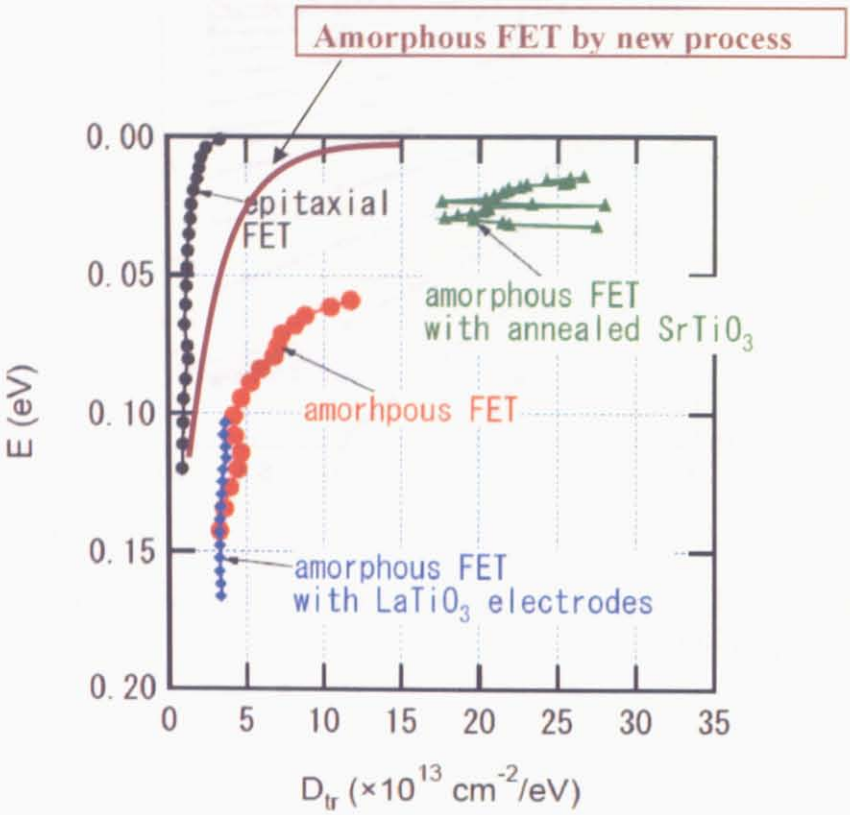



Figure 6.11 Comparison of FETs fabricated with the new process and earlier amorphous $CaHfO_3$ FETs and earlier epitaxial $CaHfO_3$ FETs [Ref. 10].

## 6-4 Fabrication and Characterization of $SrTiO_3$ FETs with an epitaxial $CaHfO_3$ gate insulator

In earlier work, the low-temperature performance of $SrTiO_3$ (100) single crystal FETs with epitaxial $CaHfO_3$ gate insulator layers was found to be better than that of FETs with amorphous $CaHfO_3$ gate insulator layers [8, 9]. As illustrated in Figure 6.12, the interface between the gate insulator layer and the $SrTiO_3$ substrate is very different in a fully epitaxial sample and in an amorphous insulator sample. Due to this, it was contemplated that an epitaxial $CaHfO_3$ gate insulator layer should show reduced trap state densities, because amorphous gate insulator layers are generally known to have high trap state densities. Therefore, I also attempted to fabricate FETs with epitaxial $CaHfO_3$ gate insulator layers using the new electrode fabrication process.

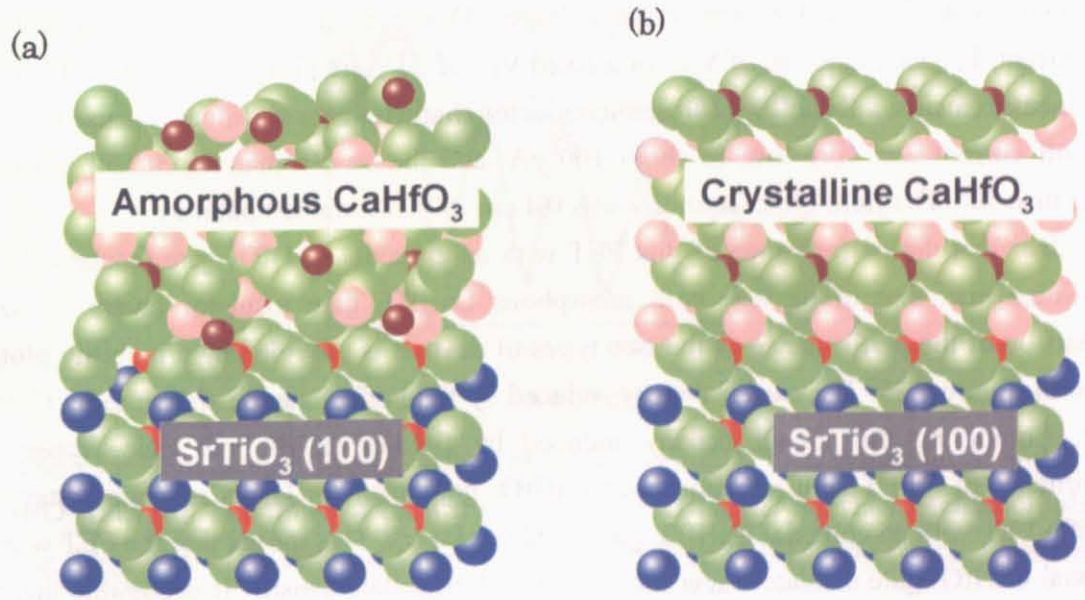



Figure 6.12 Schematic images of an a-$CaHfO_3$/SrTiO3 interface and an epitaxial $CaHfO_3$/$SrTiO_3$ heterointerface.

The fabrication procedure of FETs with epitaxial $CaHfO_3$ gate insulator layers is explained in Section 6.2. The devices fabricated by the new process included an initial epitaxial $CaHfO_3$ layers and a second amorphous $CaHfO_3$ cover layers. The thickness of the epitaxial $CaHfO_3$ layer, which is in contact with the channel region of the $SrTiO_3$ substrate, was 2.4 nm ( 6 unit cells) and the thickness of the amorphous $CaHfO_3$ layer, which covered the epitaxial $CaHfO_3$ layer was 53 nm. The Epitaxial $CaHfO_3$ layers were grown by PLD at an oxygen pressure of 1 mTorr at 700°C. A KrF excimer laser operating at 1 Hz was used for ablation and the laser fluence was 0.67 J/cm$^2$. The amorphous $CaHfO_3$ layers were grown by PLD at an oxygen pressure of 3 mTorr at room temperature. A KrF excimer laser operating at 3 Hz was used for ablation and the laser fluence was 0.68 J/cm$^2$, resulting in a growth rate of about 0.04 Å/pulse. The depth of Ar ion milled $SrTiO_3$ was 48 nm, and the thickness of $SiO_X$ which filled the pits was 26 nm. The thickness of the Al gate electrode was 30 nm.

AFM images showing the surface of a commercial $SrTiO_3$ substrate and an epitaxial $CaHfO_3$ film are shown in Figures 6.13 (a) and (b). RHEED pattern that was measured during growth at 700 °C and 1 mTorr oxygen partial pressure is shown in Figure 6.13 (c).

The drain-source current, $I_{DS}$, measured at room temperature, is plotted as a function of the drain-source bias, $V_{DS}$, under various gate voltages, $V_{GS}$, in Figure 6.14 (a). The $I_{DS}$ and gate leak current, $I_{GS}$, as a function of $V_{GS}$ for a fixed $V_{DS}$ of +1V are plotted in Figure 6.14 (b). In these measurements, a Keithley 4200 semiconductor characterization system was used.

The off current was very low, at about 100 pA, and the on-off channel current ratio was higher than $10^3$. The field-effect mobility was 0.4 cm$^2$/V s at room temperature.

It is clear that the performance of this FET with an epitaxial $CaHfO_3$ gate insulator layers was worse than that of devices with amorphous $CaHfO_3$ gate insulator layers. A better comparison of the performance of the two types of devices is provided by a mobility plot, as shown in Figure 6.15. The carrier density induced by field effect can be shown to be $C_i (V_g - V_{th})/e$. Comparing the carrier density induced by field-effect of both deice types, the performance of a FET with an amorphous $CaHfO_3$ gate insulator layers is much better than that of a FET with an epitaxial $CaHfO_3$ gate insulator layers. This means that the FET with an epitaxial $CaHfO_3$ gate insulator layer included a high trap state density. It is possible that this high trap state density is caused by the non-stoichiometry and high density of crystal defects at the epitaxial $CaHfO_3$ interface.

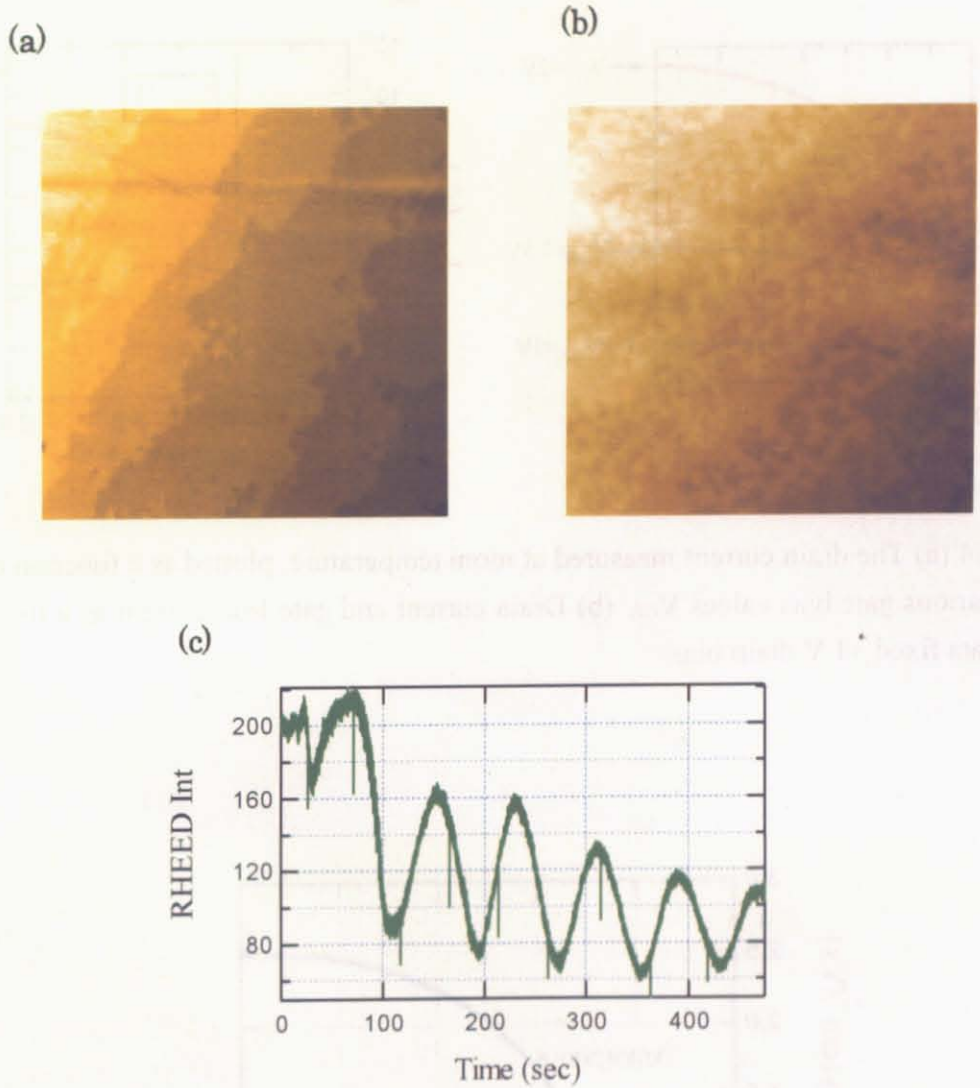



Figure 6.13 AFM images of the surface of a commercial $SrTiO_3$ substrate (a) and epitaxial $CaHfO_3$ film (b). The image sizes are $1 \times 1$ $\mu m^2$. (c) RHEED intensity oscillation observed during the growth of an epitaxial $CaHfO_3$ film on a $SrTiO_3$ (100) single crystal substrate.

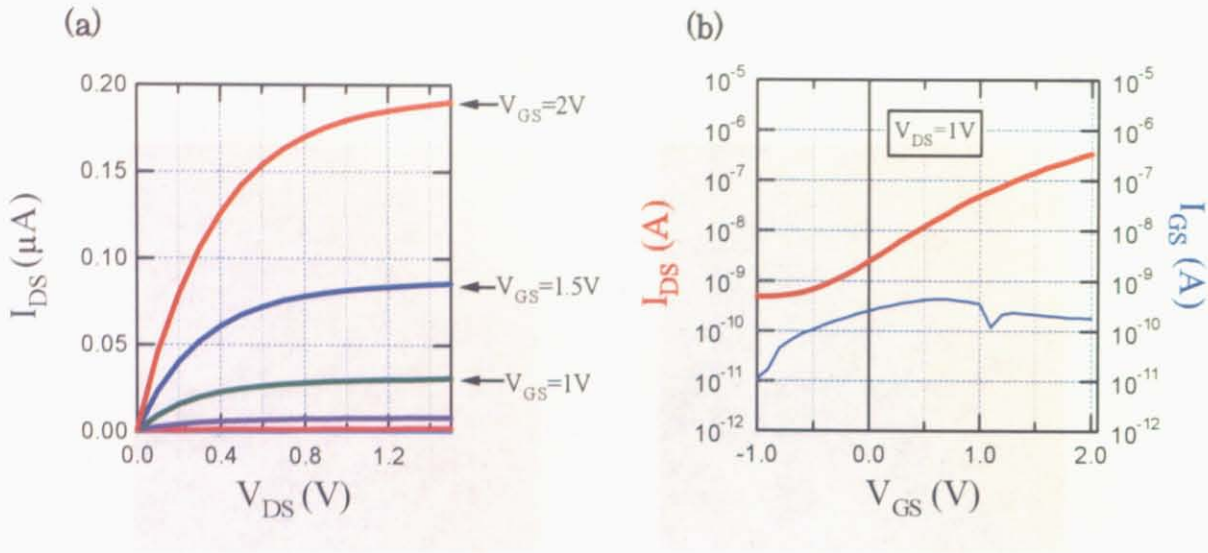



Figure 6.14 (a) The drain current measured at room temperature, plotted as a function of drain bias for various gate bias values $V_{GS}$. (b) Drain current and gate leak current as a function of gate bias ata fixed +1 V drain bias.

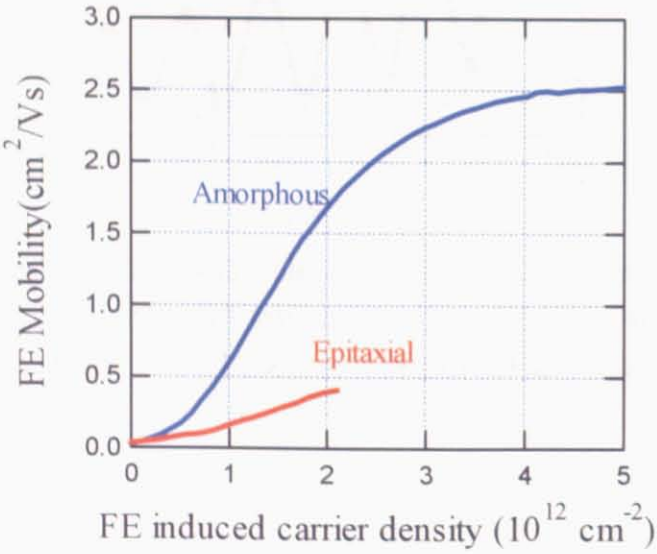



Figure 6.15 Comparison of field-effect mobilities of amorphous and epitaxial devices as a function of induced charge density.

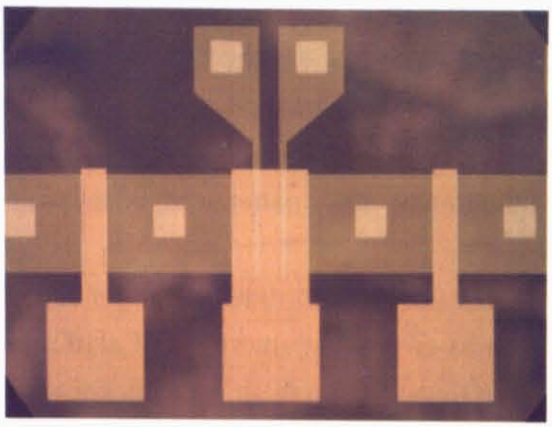
## 6-5 Fabrication and Characterization of $SrTiO_3$ FETs with an amorphous $CaHfO_3$ gate insulator for 4-point measurements of channel resistivity

Several electrode geometries were explored in this work. The simplest devices only contained two contacts to the channel, the source and the drain, and only 2-point measurements were thus possible. For 4-point measurements of channel resistivity, FETs with two additional electrodes either crossing the channel region or attached to the side of the channel area were fabricated. These additional electrodes were used for 4-point measurements of channel resistivity. Photographs of the two electrode configurations are shown in Figures 6.16 (a) and (b). A schematic drawing of the lithography mask patterns together with the electrode dimensions are shown in Figure 6.16 (c).

These devices were fabricated using the new process for electrode definition and also included two amorphous $CaHfO_3$ layers. The thickness of the first amorphous $CaHfO_3$ layer, which was in contact with the channel region of $SrTiO_3$ was 20 nm thick. The thickness of the second amorphous $CaHfO_3$ layer, which covered the first amorphous $CaHfO_3$ layer was 52 nm. Both layers were grown by PLD at an oxygen pressure of 3 mTorr. A KrF excimer laser operating at 3 Hz was used for ablation and the laser fluence was 0.7 J/cm$^2$, resulting in a growth rate of about 0.049 Å/pulse. The depth of Ar ion milled $SrTiO_3$ was 48 nm, and the thickness of $SiO_X$ which filled the pits was 33 nm. The thickness of the Al gate electrode was 30 nm.

In this measurement, a number of current sources, current meters, and voltmeters were used, including a 6485 picoammeter, 6487 picoammeter/voltage source, 6517A electrometer (KEITHLEY) and a 7651 DC source (YOKOGAWA). The 6517A electrometer (KEITHLEY) has very high input impedance, over 200 TΩ, and is thus suitable for measuring the voltage between the two additional side contacts of the device.

(a)



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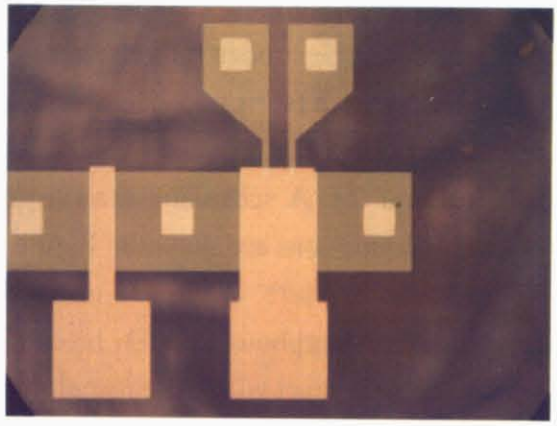

(c)

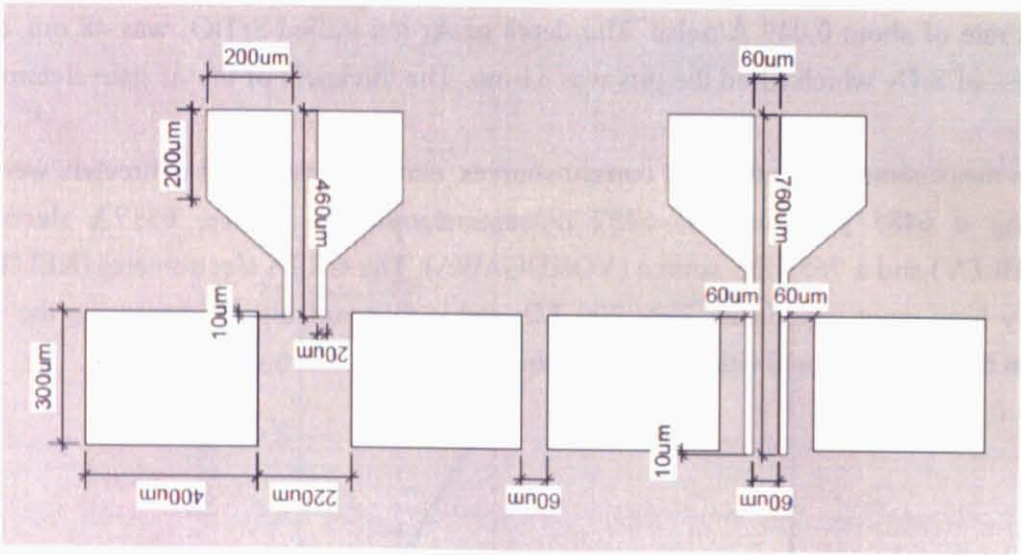


Figure 6.16 Photograph of the FETs with two additional electrodes (a) crossing the channel region (b) attaching to the side of the channel. (b) Schematic drawing of sizes of the FETs.

The temperature dependence of channel resistivity of a FET with two additional electrodes attached to the side of the channel is shown in Figure 6.17. The measurements were made between 300 and 50 K in 25 K steps. The device performed in a similar way to earlier devices that did not have the extra electrodes in the channel.

As shown in Figure 6.17, the threshold voltage of the device clearly shifted with reducing temperature. The threshold voltage values were extracted from linear fits of the square root of $I_{DS}$ vs. $V_{GS}$ plots, shown in Figure 6.18. After replotting in Figure 6.19 the channel current as a function of gate bias that has been corrected for threshold shift, the slope change of the current plot can be clearly seen. The increase of the slope corresponds to the increase of bulk mobility of carriers in $SrTiO_3$ at low temperature.

The sheet resistance of the channel is shown as a function of gate bias in Figure 6.20. Measurements were done for both electrode geometries. The data in Figure 6.20 (a) was taken from a device where the electrodes crossed the channel. Since these electrodes are embedded in the surface of the substrate crystal, the measurement is effectively a 2-point measurement. The results are affected by the contact resistance and due to that a shift of the curves towards higher gate bias is seen at low temperature. More reliable data can be obtained by making contact only to the side of the channel region, as shown in Figure 6.20 (b). In this data set, all sheet resistance curves cross in a narrow range of bias voltages, as expected.

The crossover point presumably corresponds to an induced charge density that is sufficient to raise the chemical potential into the conduction band and thus revert the channel into a metallic state. The threshold shift that is seen in Figure 6.18 is thus reflects the finite density of in-gap impurity states below the conduction band bottom. As the temperature is reduced, the range of energies from which carriers can be excited to the conduction band becomes narrower and a higher gate bias is needed to populate the deeper in-gap impurity states. At lower temperatures there is an additional mechanism that may cause threshold shifts, namely trapped charge in the amorphous insulator. The temperature limit below which such trapping becomes significant can be estimated by looking at the hysteresis behaviour of the sheet resistance. This data is shown in Figure 6.21 for a set of measurements done between 300 and 50 K. The observed hysteresis was insignificant above 100 K. At 50 K, however, a large hysteresis loop appears and the threshold value for that curve can no longer be accurately determined.

The difficulty of analyzing channel conductivity by attempting to re-plot the data as a function of gate bias values that have been corrected for threshold shifts is illustrated in Figure 6.22. In an ideal case this plot should show the channel sheet resistance as a function of effective sheet carrier density. As the plot shows, however, the threshold voltage cannot be determined accurately enough for a meaningful comparison of the plots close to the threshold. The plot does, however, illustrate very well the dramatic drop of sheet resistance from GΩ to the order of tens of kΩ. In addition, an decrease of the sheet resistance was observed with reducing temperature.

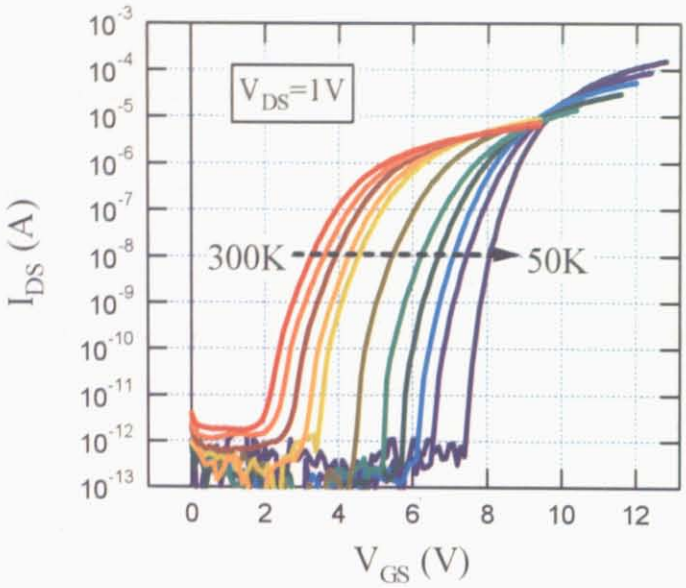


Figure 6.17 Channel current $I_{DS}$ as a function of gate bias $V_{GS}$ for a fixed drain bias of +1V. The channel current was measured between 300 and 50 K in 25K steps. This FET had two additional electrodes attached to the side of the channel.

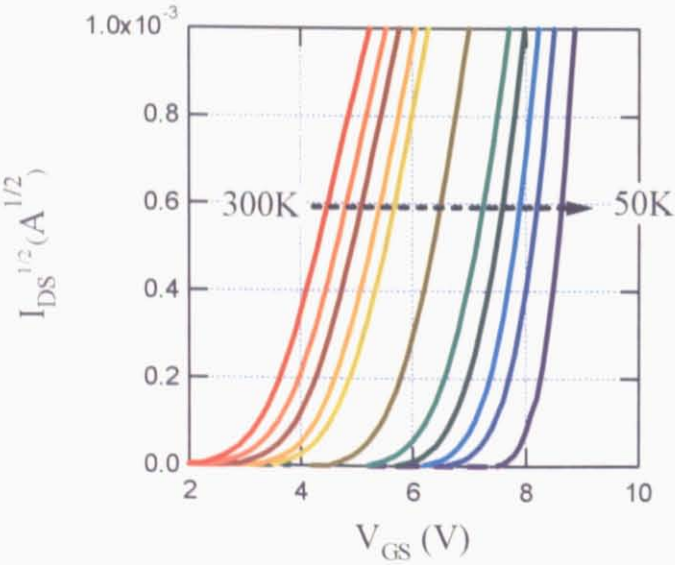


Figure 6.18 The root of channel current plotted as a function of gate bias for a FET with two additional electrodes attaching to the side of the channel.

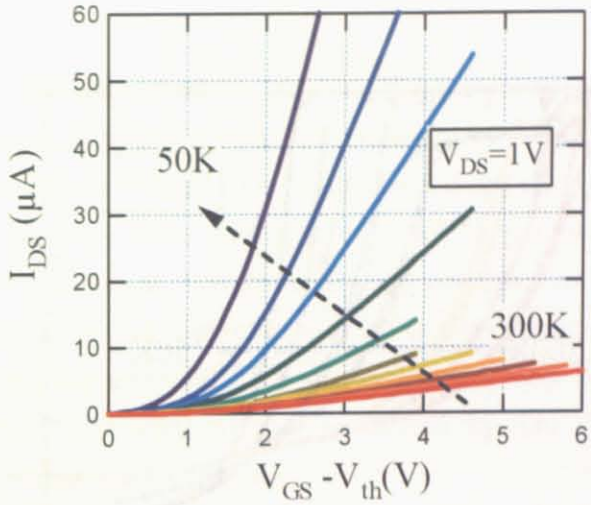


Figure 6.19 $I_{DS}$ as a function of $V_{GS}$, for a fixed $V_{DS}$ of +1V at various temperatures from 300 to 50 K measured in 25K steps, plotted after subtracting the threshold voltage.

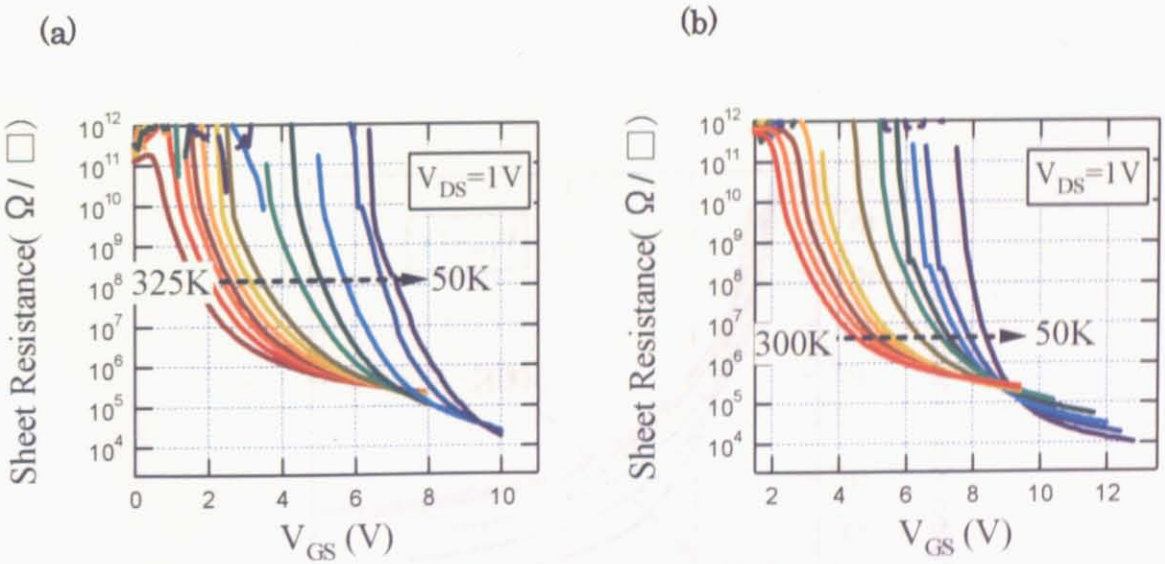


Figure 6.20 The sheet resistance as a function of $V_{GS}$ of the FETs with two additional electrodes (a) crossing the channel region (b) attaching to the side of the channel.

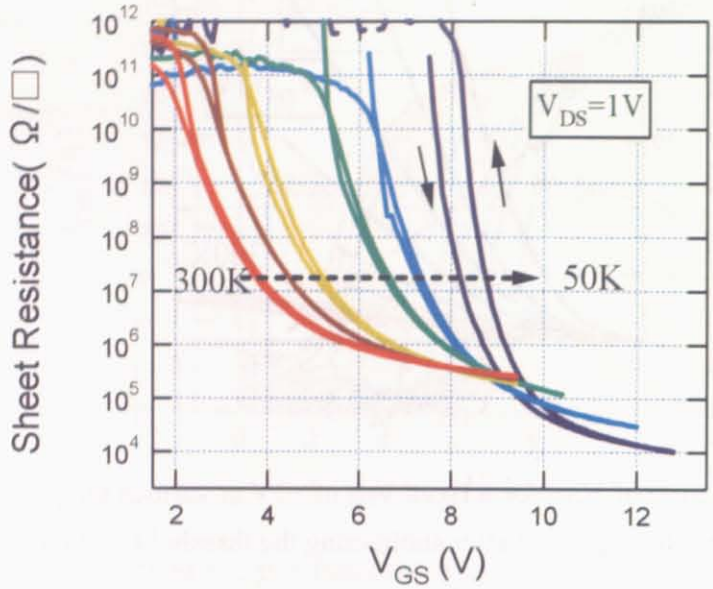


Figure 6.21 The hysteresis behaviour of the sheet resistance as a function of $V_{GS}$ at various temperatures from 300 to 50 K measured in 50K steps.

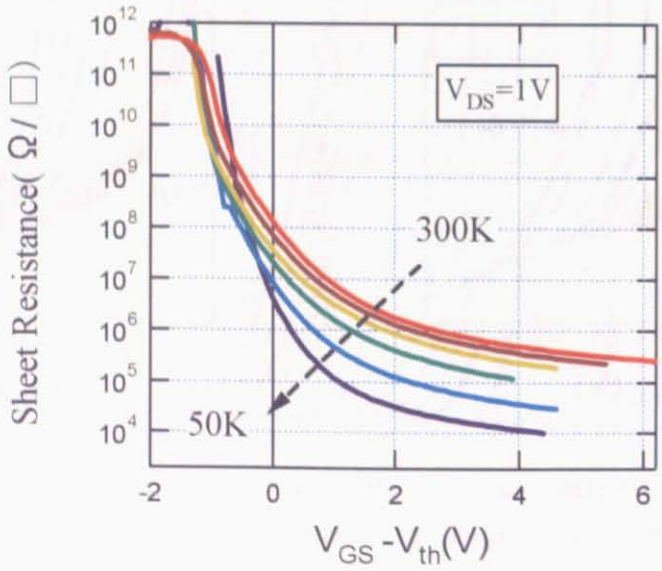


Figure 6.22 The sheet resistance as a function of $V_{GS}$ after subtracting the threshold voltage.

## 6-5 Conclusions

A new process has been developed for reducing the density of defects in the channel region of an oxide FET. An insulator-metal transition, induced by field-effect doping, was observed in $SrTiO_3$ single crystal FETs with $SrTiO_{3-\delta}$ source and drain electrodes.

I also attempted to fabricate FETs with epitaxial $CaHfO_3$ gate insulator layers in this study, to reduce the trap state densities. Unfortunately, the performance of the FETs with epitaxial $CaHfO_3$ gate insulator layers was far inferior to FETs with amorphous $CaHfO_3$ gate insulator layers. This means that the epitaxial FET still included a very high trap state density. It is possible that this high trap state density is caused by the non-stoichiometry and low crystallinity of the epitaxial $CaHfO_3$ film.

I analyzed the sheet resistance of the FET channel layer by fabricating and measuring $SrTiO_3$ FETs with two potential electrodes inside the channel region. With increasing gate voltage, the sheet resistance dropped from several GΩ to the order of kΩ. This showed that the carriers induced by the field effect behaved in the same way as in normal FETs with amorphous $CaHfO_3$ gate insulators.

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# Chapter 7

# Conclusion

In order to probe the electronic structure of oxide heterointerfaces, I developed a new process for fabricating $SrTiO_3$ FETs based on $CaHfO_3$ gate insulators and source and drain electrodes composed of metallic oxygen-deficient $SrTiO_{3-\delta}$.

In Chapter 4, I described the fabrication and characterization of the oxygen-deficient $SrTiO_{3-\delta}$ layers. These oxygen-deficient $SrTiO_{3-\delta}$ layers were formed by Ar ion milling at an acceleration voltage of 500 V. The oxygen-deficient $SrTiO_{3-\delta}$ layers had good thermal stability. The sheet carrier densities of all samples were close to $10^{14}$. The mobilities were higher than 2 $cm^2 V^{-1} s^{-1}$ at room temperature and increased to 1000 $cm^2 V^{-1} s^{-1}$ at low temperature. It can be concluded that these electrical properties are adequate for the use of oxygen-deficient $SrTiO_{3-\delta}$ layers as source and drain electrodes in $SrTiO_3$ field effect transistors.

In Chapter 5, the fabrication and characterization of $CaHfO_3$ insulator films on $SrTiO_3$ (100) single crystal substrates was shown. The optimal growth rate for amorphous $CaHfO_3$ films was found to be 0.067 Å/pulse. The average breakdown field of the films was 3.9 MV/cm.

The influence of substrate annealing on the FET properties was evaluated. The surface morphologies of $SrTiO_3$ (100) single crystal substrates obtained after annealing in the PLD chamber at 1 mTorr partial oxygen pressure for 1 hour were reported. Although higher temperature annealing appeared to be beautiful from the point of view of the step structure, it was also found that if the temperature is too high, there is a high degree of probability that SrO segregation will occur and oxygen vacancies will be formed in the $SrTiO_3$ single crystal substrates. Based on these considerations, epitaxial $CaHfO_3$ films were fabricated at 700 °C and a 1 mTorr oxygen partial pressure.

The fabrication and characterization of $SrTiO_3$-based field-effect transistors was described in Chapter 6. Both amorphous and epitaxial $CaHfO_3$ gate insulator layers were studied. FETs with two additional electrodes either crossing the channel region or attached to the side of the channel for 4-point measurements of channel resistivity were also reported.

The use of a new electrode fabrication process for $SrTiO_3$-based field-effect transistors with amorphous $CaHfO_3$ gate insulator layers resulted in improved device performance and a lower density of trap states in the channel. The field-effect mobility was 2.5 $cm^2/V$ s at room temperature. It is noteworthy that a significant increase of field-effect mobility was observed at low temperature. This means that the carriers induced by field effect behaved as would be expected for metallic electron-doped $SrTiO_3$. This result confirmed that the FETs fabricated with the new process showed a clear advantage when compared to earlier amorphous $CaHfO_3$ FETs that used Al source and drain electrodes. The main reason for this was that the initial channel interface was deposited in the first step of device fabrication, before starting to define

the source and drain electrodes. The contamination of the substrate surface was thus reduced and consequently the observed trap density was dramatically lowered.

$SrTiO_3$-based field-effect transistors with epitaxial $CaHfO_3$ insulator layer showed lower performance than the amorphous devices, despite the electrode process improvements. This means that the FETs with epitaxial gate insulator layers still included a high trap state density in the channel. It is possible that this high trap state density was caused by the non-stoichiometry and high density of crystal defects at the epitaxial $CaHfO_3$ interface.

For 4-point measurements of channel resistivity, FETs with two additional electrodes either crossing the channel region or attached to the side of the channel area were also fabricated. With increasing gate voltage, a dramatic drop of the channel sheet resistance from several GΩ to the order of kΩ was observed. This showed that the carriers induced by the field effect behaved in the same way as in normal FETs with amorphous $CaHfO_3$ gate insulators.

# Achievements Lists

## Poster presentation

- 'Fabrication of $SrTiO_3$ field effect transistor using $SrTiO_{3-\delta}$ as source and drain electrodes'
  The 53th spring meeting of the Japan Society of Applied Physics, 2006, extended abstract vol. 2, p641

## Oral presentation

- 'Single crystal $SrTiO_3$ field effect transitor
  -Device process for the construction of high-quality oxide heterointerfaces-'
  The 67th autumn meeting of the Japan Society of Applied Physics, 2006, extended abstract vol. 2, p575

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**Atsuke Sato**