Process optimization for the Fabrication of Oxide Single Crystal Field Effect Transistors

物質系専攻　66135　西尾　和記
指導教員：Mikk Lippmaa（准教授）

Keywords: Field effect transistor, $SrTiO_3$, device scaling

Introduction

Bulk oxide materials are known for their fascinating physical properties, for instance, high-temperature superconductivity, colossal magnetoresistance, etc. Many of these characteristics depend strongly on carrier concentration. Oxide heterostructures offer interesting ways of probing such material properties. First of all, the properties of interface layers are quite different from the normal bulk properties. This can happen due to structural changes, chemical composition changes or due to charge transfer and orbital hybridization across the interface. Interfaces are also the basic building blocks of oxide-based electronic devices. Therefore, it is very useful to study the possibility of inducing reversible electronic phase transitions in oxide heterostructures by controlling the carrier density by the electrostatic field effect. Oxide field-effect transistors (FETs) can be used to probe the properties of oxides and can also lead to useful applications.

In this study, commercial wet-etched $SrTiO_3$ (001) substrates were used for constructing the semiconducting channel of the transistors. These substrates show a regular step-and-terrace surface structure and can be used to grow very high-quality thin films. The transistor gate insulator layer was grown directly on the as-received substrate surface by pulsed laser deposition (PLD), using $CaHfO_3$ or $DyScO_3$ targets. Much of this thesis work deals with the optimization of the insulator film growth parameters, such as laser fluence, oxygen pressure, and film growth temperature. The work was complicated by the need to avoid damaging the substrate surface by high-energy particles in the ablation plume and still achieve high breakdown fields. These requirements presented conflicting optimization targets. The key to success was to use a device fabrication procedure where either amorphous or epitaxial gate insulators layers could be grown at a very early stage of device processing, avoiding channel contamination and using very low deposition rates. The PLD process is a strongly non-equilibrium high-energy process that always damages a thin interface layer, resulting in oxygen loss and crystal distortion in a thin surface layer of a substrate. In order to load oxygen back into the samples, the devices were annealed in air at 300 to 400°C. Most of the interface damage could be repaired in this way. The source and drain electrodes were patterned by photolithography. The electrodes were formed by fabricating metallic oxygen-deficient regions in the $SrTiO_3$ substrate by Ar ion etching. In order to planarize the device after electrode etching, the devices were covered with a layer of SiOx by thermal evaporation. After lift-off of the photoresist, a second insulator layer was deposited by PLD and aluminum gate, source, and drain electrodes were patterned by photolithography and thermal evaporation.

The main merit of this process is the ability to maintain a contamination-free channel interface. Depositing the first insulator layer as the first step was critical to achieving devices with good switching performance. The process was further optimized for scaled-down devices, reducing the FET channel size to 10 μm length and 50 μm width.

Measurements and results

In this study, the effects of channel scaling on transistors operation, particularly field-effect mobility, was studied. Together with scaling down the lateral dimensions of the device, the insulator thickness could be reduced. FETs based on amorphous $CaHfO_3$ insulators were fabricated with various channel sizes, as shown in Fig. 1. Amorphous gate insulators were used to simplify the device fabrication. The gate insulators thickness was about 60 nm, the laser fluence was about 0.7 J/cm^2 and the growth rate was approximately 60 pulses / monolayer. The oxygen partial pressure was set at 1 mTorr. Each substrate contained an array of transistors with various channel sizes. There were four types of channel on the samples, channel length/width were 10μm /50μm, 20/100, 40/200 and 10/500. FET performance was measured for each device at room temperature. The largest device and smallest device were also measured at lower temperatures, between 50 and 300 K.

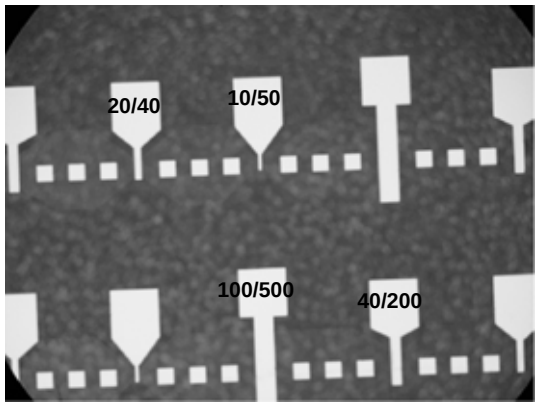

Fig.1 Top view of the array of transistor with different channel sizes

Field effect mobilities at room temperature were extracted from I_{DS}-V_{GS} measurements. Typically the smaller devices showed better performance, as illustrated in Fig. 2 (a). At room temperature, the field effect mobility reached a maximum of about 6 cm^2/Vs.

The temperature dependence of field effect mobility is shown in Fig. 2(b). The bulk Hall mobility of $SrTiO_3$ is also shown in order to compare the field-effect carriers with the Hall mobility of chemically doped carriers. Again, smaller devices showed better performance than larger ones. Mobility of around 230 cm^2/Vs was reached at 50K.

As a result of the new and improved fabrication process, a cleaner interface with a lower carrier trap density could be obtained. By scaling down the channel size, interface contamination could be decreased and field homogeneity could be improved.

In order to reduce structural disorder at the channel interface in the FETs, it was necessary to

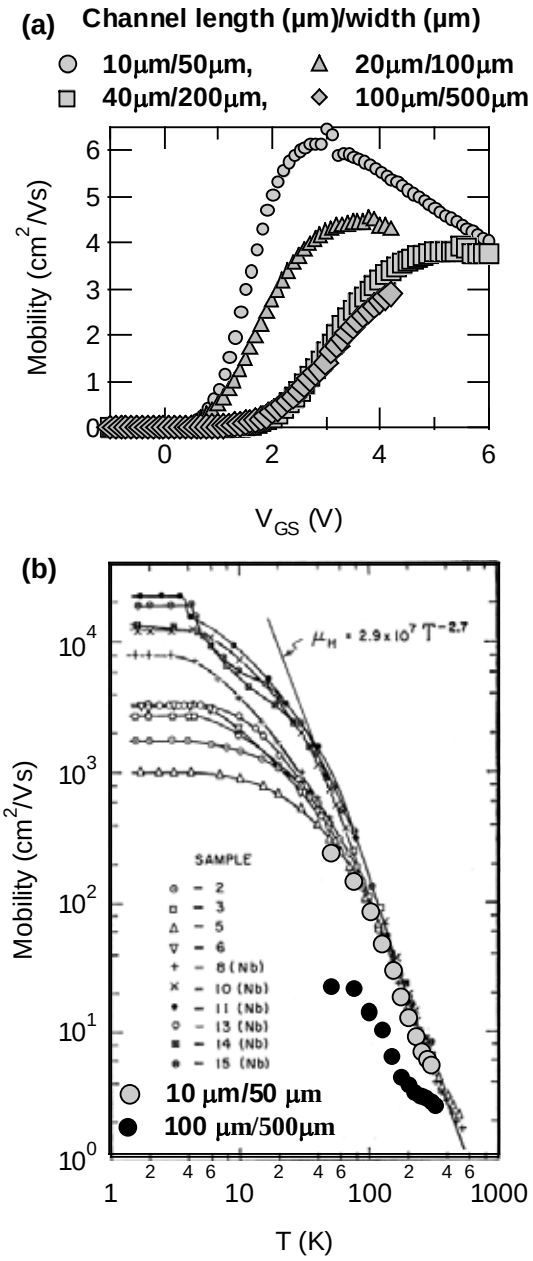

Fig.2 FE mobility **(a)** RT **(b)** low T

replace $CaHfO_3$ with $DyScO_3$, which has a smaller mismatch with $SrTiO_3$. Again, the film growth conditions such as laser fluence and oxygen partial pressure are the most important parameters. Epitaxial $DyScO_3$ films were fabricated by changing the laser fluence and oxygen partial pressure while the film growth temperature was fixed at 700°C.

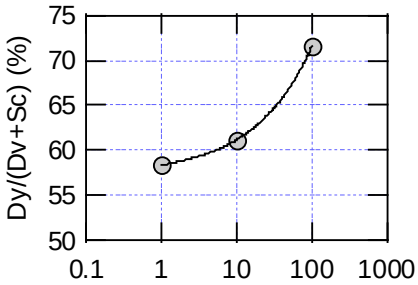

Fig.4 cation ratio vs PO_2

Crystallinity, cation ratio, and breakdown strength were measured for each sample. Crystallinity was estimated by measuring the intensity of the film peak in x-ray diffraction patterns and observing changes in the width of the rocking curve. The cation ratio was measured by SEM-EDS. Breakdown strength was measured with a KEITHLEY-4200 semiconductor analyzer.

It was found that the cation ratio in the films strongly depends on the oxygen partial pressure, as shown in Fig. 4. The laser fluence also affected the cation ratio but not as much as the oxygen pressure. The film crystallinity was found to influence the breakdown strength, as shown in Fig. 5. Growth at lower oxygen pressure gave better film quality, meaning lower divergence of cation ratio and higher breakdown strength. Higher fluence gave better film quality in terms of crystallinity and slightly higher breakdown strength.

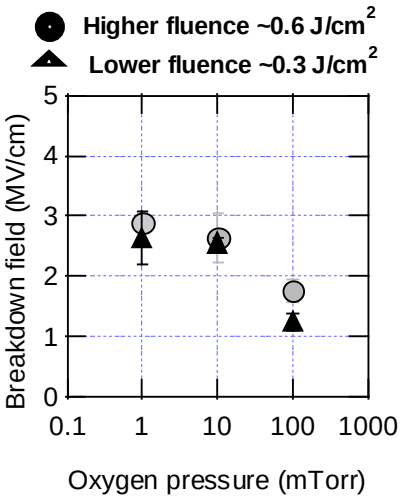

Fig.5 Breakdown field as a function of fuence and PO_2

Experiments also showed that the breakdown strength of insulator films is not a monotonic function of film thickness. Epitaxial $DyScO_3$ still has about 1% lattice mismatch with $SrTiO_3$. Strain relaxation therefore occurs in epitaxial thin films at a thickness of about 20 nm, resulting in a grain structure in the film. Grain formation degrades FET performance due to an inhomogeneous gate field and breakdown along the grain boundaries. In order to avoid grain formation, the film thickness has to be limited below the critical thickness. Samples were fabricated by changing the film thickness between 2.5 and 35 nm. The results of the film thickness optimization are shown in Fig. 6. It was concluded that the optimal thickness is in the 10 to 20 nm range, where breakdown fields of about 4 MV/cm can be achieved with $DyScO_3$.

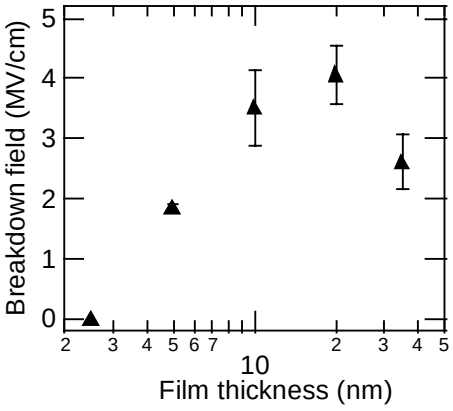

Fig.6 Breakdown strength vs film thickness

【Conference】

- Scaling of Single Crystal $SrTiO_3$ (100) Field-Effect Transistors

14^{th} International Workshop on Oxide Electronics, October 7-10, (2007), Jeju island, Korea