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Process optimization for the Fabrication of Oxide Single Crystal Field Effect Transistors

単結晶電界効果トランジスタの作製に向けたプロセスの最適化

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Process optimization for the Fabrication of Oxide Single Crystal Field Effect Transistors

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Chapter 1. General introduction

1.1 Transition metal oxide

Bulk oxide materials are known for their fascinating physical properties, for instance, superconductivity [1] or high-temperature superconductivity [2], colossal magnetoresistance [3], and ferroelectrics [4]. Many of these characteristics depend strongly on carrier concentration. Oxide heterostructures offer interesting ways of probing such material properties. First of all, the properties of interface layers are quite different from the normal bulk properties. This can happen due to structual changes, chemical composition changes or due to charge transfer and orbital hybridization across the interface.

One of the easiest material properties to measure is resistance. At the same time, measuring the resistivity of a material as a function of temperature, external fields or carrier density, can give a good idea about the mechanisms that control the material properties. An interesting material for transport studies is, for example, $SrTiO_3$, which has a rather simple perovskite lattice structure but very rich physics. The same material can be an insulator, a semiconductor, metal or superconductor. Additionally $SrTiO_3$ has a very high dielectric constant, quantum paraelectric state at low temperature [5], and very high carrier mobility [6]. Oxides like $SrTiO_3$ are therefore interesting materials for developing various device structures. Indeed, $SrTiO_3$ heterostructures have been shown to have very high carrier mobility in a thin two-dimensional interface layer [7]. $SrTiO_3$ also shows the resistive switching effect [8], which can be used to develop a new generation of non-volatile memories. Despite the promises, though, the utilization of these materials in high-quality devices is still very limited in practical applications. The main reason for that is the difficulty of controlling the electrical properties of oxide heterointerfaces and the defect structure of oxide thin films.

A useful tool for probing the transport properties of oxide heterostructures is the field-effect transistor. While transistors have obvious application potential, it is unlikely that $SrTiO_3$-based devices would show properties that would competitive with simple silicon. However, oxide FETs can be used as miniature laboratories for probing the electronic properties of oxides as the carrier density is tuned without affecting any of the other parameters, like lattice distortions or disorder [9].

1.2 Field-effect devices

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important device for very large-scale integrated circuits, such as microprocessors and semiconductor memories.

A FET is a three-terminal semiconductor device. The operating mechanism of FETs can be understood simply by considering a metal-insulator-semiconductor (MIS) diode structure, shown in Fig.1.1(a). Assuming that the semiconductor is n-type, when a positive voltage is applied to the

metal plate, the bands near the semiconductor surface are bent downward, as shown in Fig.1.1 (b). The band bending corresponds to the accumulation of carriers in the interface layer of the semiconductor. If the bending is large enough, the surface becomes inverted, meaning that the Fermi level in the surface layer is above the conduction band bottom. When negative voltage is applied, the bands bend upward and carriers are depleted.

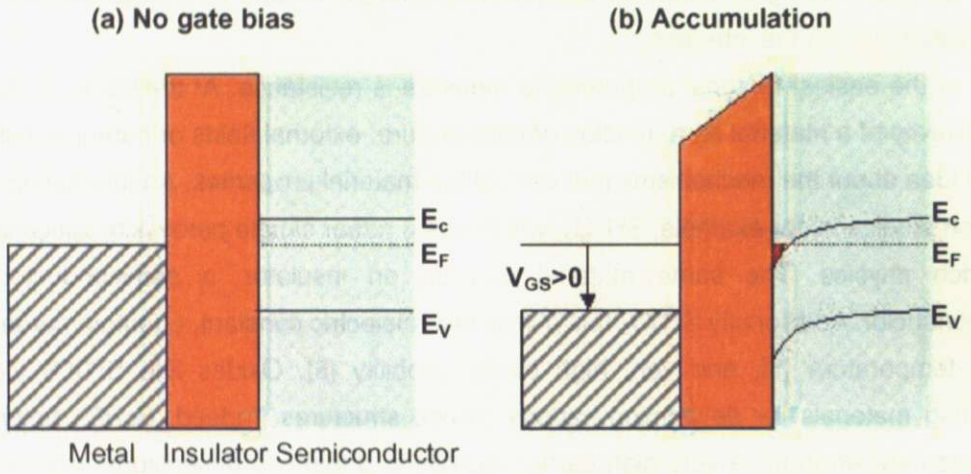

Figure 1.1 schematic energy-band diagram for MIS diodes.
(a) no gate bias, (b) accumulation under positive bias

The simple structure of a MISFET is illustrated in Fig1.2. This is also a three-terminal device. The electrodes attached to the semiconductor are called the source and the drain and the metal contact on the insulator is called a gate. The basic device parameters are channel length, width and the insulator thickness. In an oxide transistor based on an n-type material like intrinsic $SrTiO_3$, there is no current between the source and drain electrodes when no gate bias is applied to the gate because there are no carriers in the channel region. When a positive gate bias is applied to the metal plate, electrons are accumulated in the channel, allowing current to flow between the metallic source and drain electrodes. The channel current I_{DS} can flow by applying a drain bias V_{DS}. The current channel current is proportional to V_{DS} as long as the drain bias remains small compared to the gate bias. This is called the linear region. As V_{DS} increases, the channel current saturates. This happens when the potential difference between the gate and drain electrodes becomes zero. At that point, no carriers are accumulated close to the drain electrode. This is called the saturation region. The channel current in the linear and saturation regions is given by,

$$I_{DS}^{lin} = \frac{W}{L} \mu C_i (V_{GS} - V_{TH}) V_{DS} \qquad (1.1)$$

$$I_{DS}^{sat} = \frac{W}{L} \mu C_i (V_{GS} - V_{TH})^2, \qquad (1.2)$$

where μ is the carrier mobility, C_i is the sheet capacitance of the insulator, and V_{TH} is the threshold voltage. The carrier mobility is one the most important parameters that characterize transistor performance. Field-effect mobility in the linear and saturation regions is given by

$$\mu_{FE}^{lin} = \frac{1}{C_i V_{DS}} \frac{L}{W} \frac{\partial I_{DS}}{\partial V_{GS}} \bigg|_{VDS=const}, \qquad (1.3)$$

$$\mu_{FE}^{sat} = \frac{2}{C_i V_{DS}} \frac{L}{W} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \bigg|_{VDS=const}. \qquad (1.4)$$

There are several merits to using a FET for carrier density tuning instead of chemical doping. The usual way of changing the carrier concentration in a transition-metal oxide crystal is to add valence-mismatched impurities. In case of $SrTiO_3$, for example, n-type conductivity is obtained by substituting La on the Sr site or Nb at the Ti site. However, this process also distorts the lattice and increases disorder. In contrast carrier density tuning by external electric field occurs without structural distortion and the tuning is reversible and continuous. For these reasons, FETs can be very useful in the study of the physical properties of oxides materials.

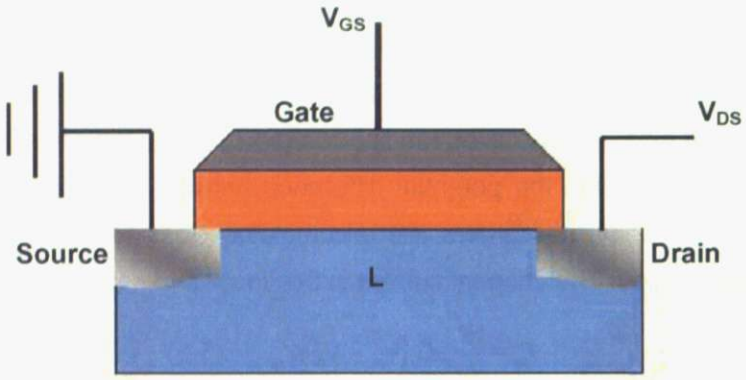

Figure 1.2 Schematic drawing of a MISFET

1.3 Objective of this study

In earlier work in this laboratory, FETs have been fabricated in order to measure the physical properties of oxide heterointerfaces. The first transistors were based on $CaHfO_3$ wide gap insulator in the gate stack and $SrTiO_3$ in the channel. In these devices, the source and drain electrodes were fabricated first, by depositing $LaTiO_3$ through metal stencil masks. The $CaHfO_3$ gate insulator was deposited by pulsed laser deposition (PLD) [10]. However, the performance of the transistors was mediocre. The most likely cause for the limited carrier mobility was extrinsic contamination in the channel region caused by the metal contact masks used for the source and drain area definition and subsequent high-temperature diffusion anneals. In order to solve the contamination problem, a new process was developed, where the first insulator layer was grown before any other processing steps, protecting the critical channel interface. Photolithography and Ar ion etching were used to cut through the initial insulator layer and insert the source and drain electrodes at the channel interface. FETs with amorphous $CaHfO_3$ gate insulators were fabricated by the new process and immediately showed improved performance, such as higher mobility and lower trap density [11]. However, the low-temperature performance was still poor due to residual trap density and low gate insulator breakdown strength.

In this study I focused on scaling effects of the channel region and the thickness of the gate insulator. Because FETs with channel length of 100 μm and width of 500 μm had been fabricated earlier, the target was to scale the devices down by at least a factor of 10. I studied the effects of channel scaling on the number of defects in the channel area, insulator breakdown, and field-effect mobility of the smaller FETs. As a part of this project, I focused on the optimization of epitaxial $DyScO_3$ thin film growth, since $CaHfO_3$ was replaced with $DyScO_3$, which has similar dielectric properties but a better lattice match with the $SrTiO_3$ substrate.

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Chapter 2. Film growth and measurement systems

2.1 System of laser MBE and characterization of oxide thin films

2.1.1 Pulsed laser deposition

Pulsed laser deposition (PLD) is a very versatile thin film growth technique for oxide materials with high melting points. It is very easy to switch between different materials by simply changing ablation targets. Films can be grown in ultrahigh vacuum or in the presence of a background gas at pressures of up to about 1 Torr. Various *in situ* characterization tools can be integrated into a PLD chamber. Most commonly, reflection high-energy electron diffraction (RHEED) is used to characterize the film surface structure. With the help of RHEED, thin film thicknesses can be controlled truly on an atomic scale with fractional monolayer accurately.

The system described here used a pulsed KrF excimer laser operating at a 248 nm wavelength for ablation of oxide targets. The chamber was very compact, with a diameter of 200 mm and a height of 300 mm. The chamber could be kept very clean, with a base pressure in the 10^{-9} Torr range. Samples were loaded into the chamber through a load-lock system to prevent chamber contamination. Reactive gases, typically pure oxygen, could be introduced into the chamber at accurately controlled rates though a piezoelectric gas dozer. The sample stage holding the substrate crystal was mounted about 50 mm above the target, as shown in Fig.2.1.

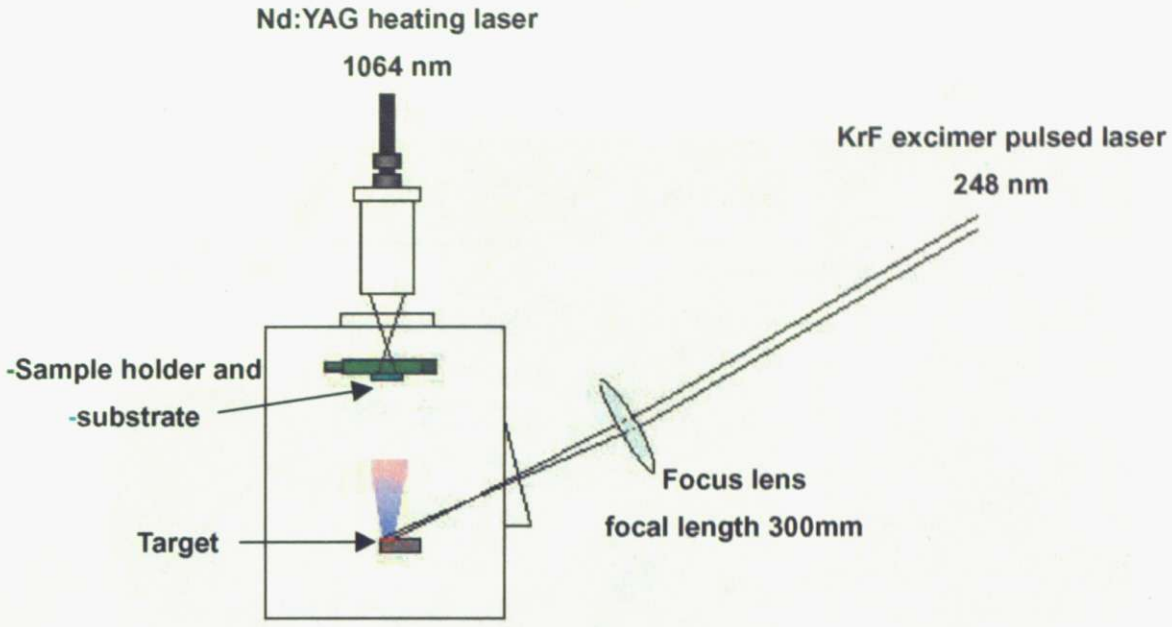
The excimer laser light was introduced into the chamber at a 30 degree incidence angle to the target surface. The energy of laser pulses was adjusted with an optical attenuator. Low-energy edges of the laser beam were cut off with a suitable aperture and the light was focused on the target surface with a single plano-convex lens with a focal length of 300 mm. This lens was mounted on a X-Y-Z stage so that the position on the target and the imaging spot size could be adjusted. Ablation position adjustments are necessary in order to align the center of the ablation plume with the center of the sample. The spot size needed to be adjusted to tune the energy density and plume shape. Since the laser energy density is one of the most important parameters for controlling the ablation process [1], great care was taken to accurately determine the spot size and the total energy delivered to the target surface in each laser pulse.

The spot size was usually measured by placing a piece of thermal printer paper at the target position in the chamber. Typical spot profiles from which the spot area was determined are shown in Fig.2.2 (a). Fig.2.2 (c) shows how the spot size changed when the focusing lens was moved along the z-axis, defined in Fig. 2.2(b). In-plane directions of focus lens, that is x and y-axis, were fixed. Typically spot sizes between 0.05 and 0.1 cm^2 were used. A thermoelectric power meter connected to an oscilloscope was used for monitoring the laser energy in front of the focus lens. The deterioration of transmittance of the laser entrance viewport was also considered when

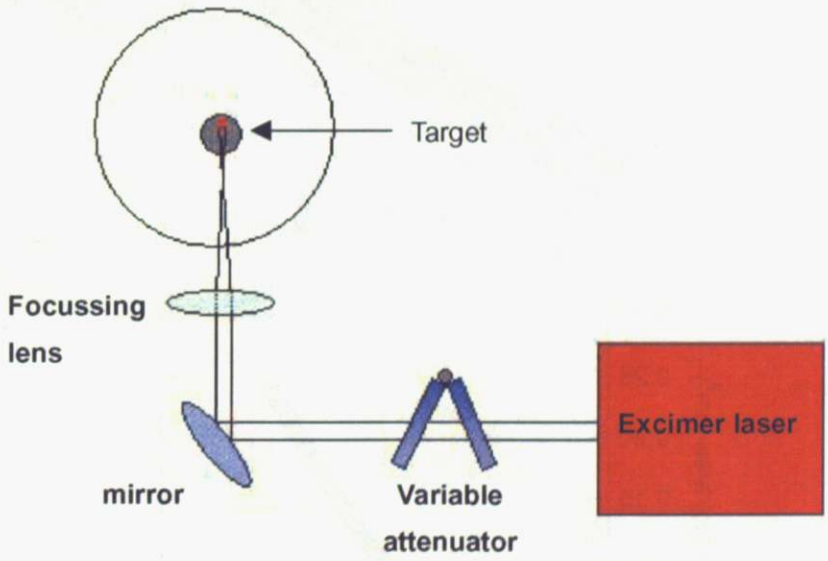
calculating the true energy density on the target [2]. Laser fluence calibration was done by ablation a glass sample and measuring the depth of the pit that was formed. Fig.2.3 shows the ablation pit depth plotted as a function of laser energy as indicated by the power meter outside of the chamber. Measurements were repeated at approximately one month intervals during normal chamber operation. Due to a gradual coating of the laser entrance viewport by the material evaporated from the target, the window transmittance gradually drops, reducing the real laser pulse energy on the target. Since the laser power monitor can only measure the laser energy outside of the vacuum chamber, it is necessary to monitor the additional loss at the viewport and correct the laser pulse energy accordingly. As shown in Fig. 2.3, the ablation rate was initially high, but dropped significantly over a few weeks of chamber use. By measuring the glass plate ablation rates at regular intervals, it was possible to obtain true transmittance correction factors for each experiment.

Another method for calibrating losses in the optics is to use a visual technique. In this case, an Al_2O_3 target was ablated and the laser energy was changed gradually from higher to lower values until the ablation plume vanished. The transmittance of the entrance viewport could be estimated by comparing the threshold laser energy. The advantage of this technique is that chamber contamination is reduced, since only aluminum oxide is ablated, instead of a mixture of possibly volatile oxides that are ejected from a glass plate. An extension of the visual technique is to use a CCD camera, which is more sensitive than the human eye.

This PLD system was equipped with a neodymium doped yttrium aluminum garnet (Nd:YAG) laser heating system for the substrate. The 1064 nm light from the Nd:YAG heating laser was introduced into the chamber through a glass viewport. The light from the laser was transported to the chamber with an optical fiber and focused on the back side of the sample holder with a collimating lens. This system allowed samples to be heated to 1000°C at a laser power of less than 40 W, reducing outgassing in the chamber. The substrates were attached to the holders with mechanical clams and mounted in the sample stage above the ablation target. A schematic drawing of the sample holder is shown in Fig.2.4. An oxidized nickel foil was used to absorb the heating laser light and spread the heat homogeneously over the sample surface. A gold-nickel-gold trilayer was inserted between the oxidized nickel foil and the sample crystal. The sample temperature was measured with an optical pyrometer. Since the pyrometer operated at a wavelength of 2 to 2.5 μm, where the substrate crystals are mostly transparent, it is very important to calibrate the pyrometer for the effective emissivity of the sample. In this study, $SrTiO_3$ (STO) and Nb-doped STO crystals were used. These surface temperature was calibrated by depositing a thin gold film on one half of the sample and determining and heating the sample until the gold film melted. Since the gold melting point is fixed at 1064°C, it was possible to calculate the effective emissivity of the sample. For STO substrates mounted on a gold foil, the typical emissivity value was 0.35. For 0.5wt% Nb-doped STO substrates, emissivity was set at 0.44.



Side view of the chamber



Top view of the chamber

Figure.2.1 Schematic drawings of the PLD system

(a) Schematic of the side view

(b) Schematic of the top view

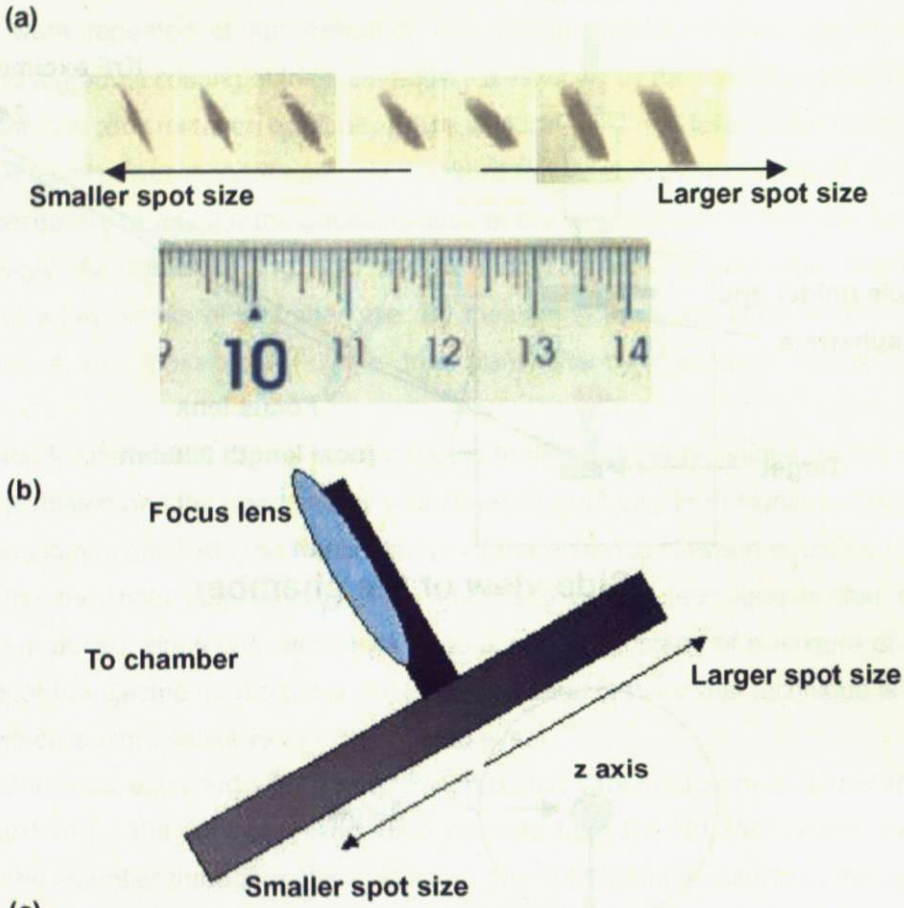
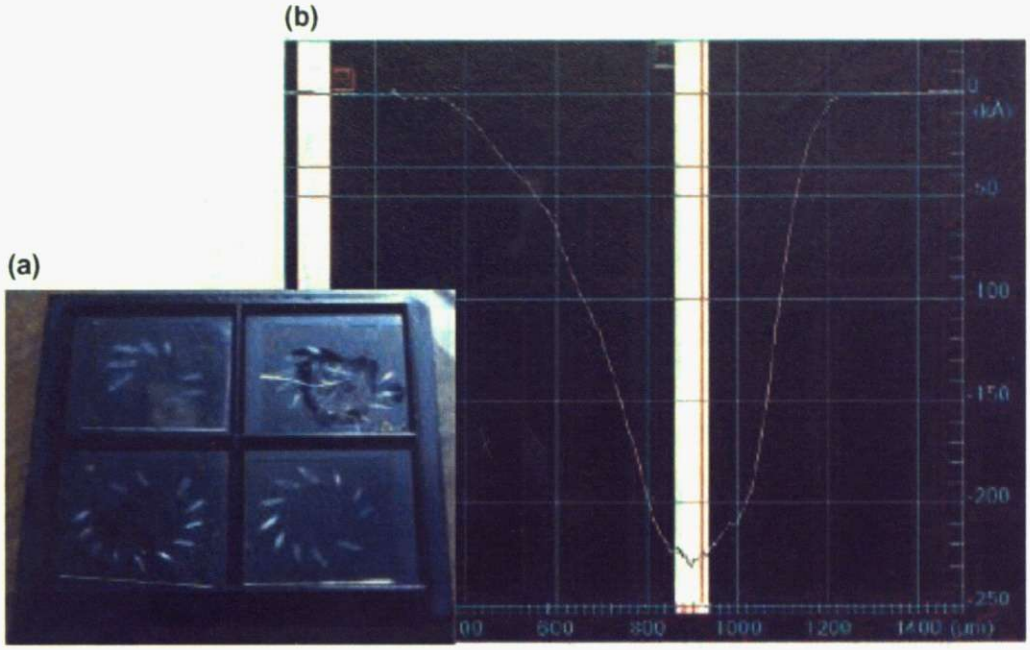


Figure 2.2 (a) ablation spot profiles, (b) Schematic of lens position (c) Laser spot size plotted as a function of focus lens position



Glass 15x15 mm^2 Line profile of ablated position

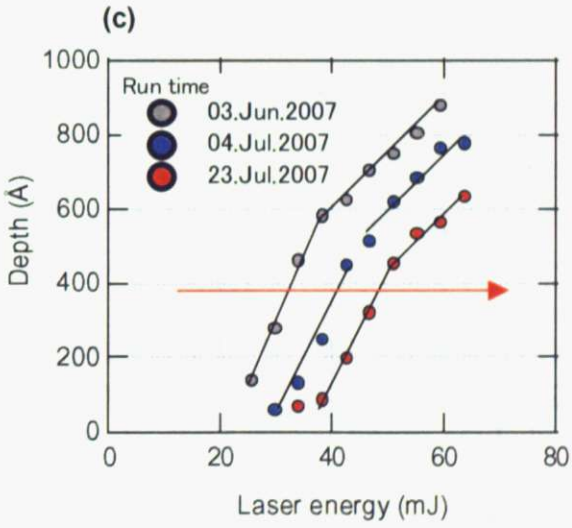


Figure 2.3 (a) glass sample ablated by the excimer laser at various energy densities (b) Line profile of an ablation pit. The maximum depth was measured. (c) Ablated depth plotted as a function of laser energy. In all cases, 500 pulses were fired at the samples.

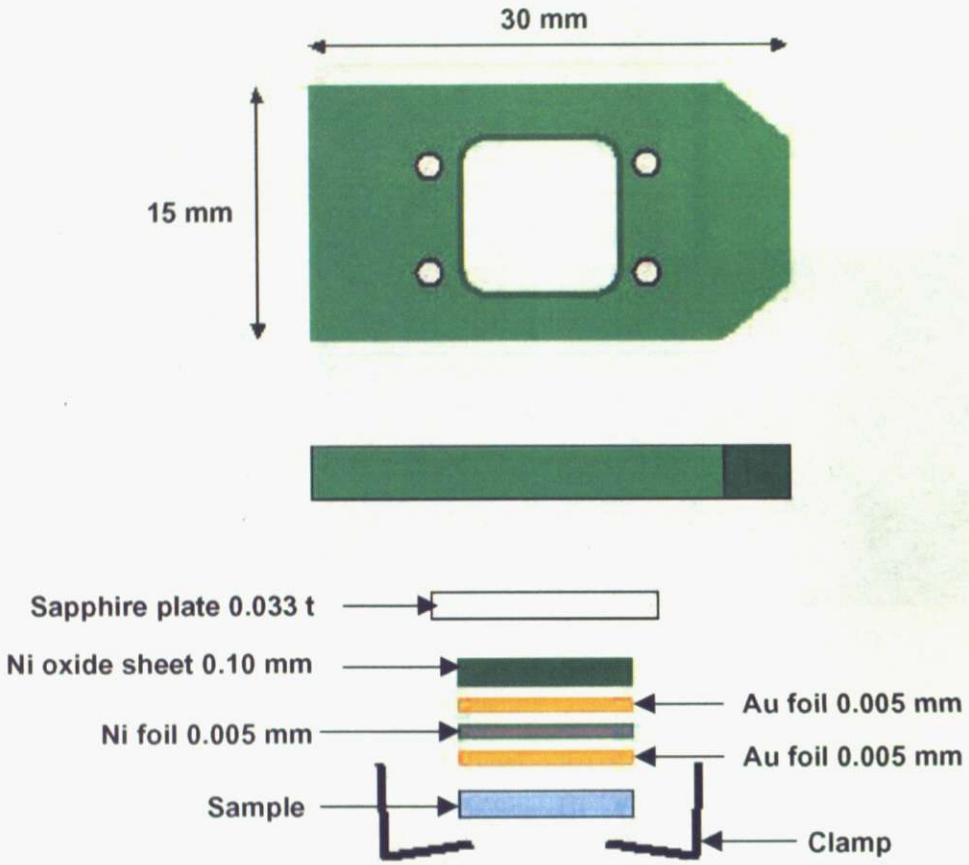


Figure 2.4 Schematic of the sample holder and the sandwich structure used for obtaining good thermal contact between the substrate crystal and the heating laser light absorber.

2.1.2 Reflection high-energy electron diffraction

Reflection high-energy electron diffraction (RHEED) uses a narrow beam of high-energy electrons to measure the diffraction pattern of a surface in a grazing incidence geometry. The energy of the electrons used for RHEED is usually in the range of 10 to 30 kV. In this work, the beam energy was 25 kV and the incident angle on the sample surface was 1 to 3°. Electrons interact very strongly with the surface layer of a crystal and electrons that penetrate deeper than one or two monolayers can no longer escape from the sample. Due to this, only electrons scattered from the topmost layer of the crystal can be detected in the diffraction pattern, giving this technique very high surface sensitivity. The diffraction spot distances can be used to directly calculate the in-plane lattice parameter of the surface. Diffraction spot shapes give information about disorder on the surface and the specular reflection intensity is a good measure of step edge density on the surface. For this reason, RHEED is a very effective tool for measuring the deposition rate of a film, when growth occurs in a layer-by-layer mode. Because in this growth mode the surface oscillates between very smooth (nearly full monolayer coverage) and very rough (half monolayer coverage), the specular reflection intensity also oscillates.

During epitaxial film growth, the intensity of the specular spot was monitored with a video camera and the intensity was analyzed on a computer. Surface diffraction patterns were also recorded before and after depositions to document the quality of the surfaces.

2.2 $SrTiO_3$ substrate

In this study single crystal $SrTiO_3$ (STO) (001) substrates were used as the field-effect transistor channel. $SrTiO_3$ shows many attractive properties, such as very high permittivity [3] and very high carrier mobility in doped crystals, reaching well above 10^4 cm^2/Vs at 4 K [4]. STO is wide-gap semiconductor with a band gap of approximately 3.2 eV [5]. The Fermi level of $SrTiO_3$ is located close to the conduction band bottom and it is easy to induce n-type conductivity at relatively low carrier densities of about 10^{18} cm^{-3} [4]. These characteristics make $SrTiO_3$ attractive as a channel material of a field-effect device.

2.3 Atomic force microscopy

Atomic force microscopy (AFM) is a flexible technique for real-space surface characterization. AFM measures the interaction force between a sharp tip and the sample surface. In noncontact measurement modes, AFM can give information about long-range forces between a sample and the tip. In that case the cantilever oscillates above the sample due to an applied driving force at the cantilever resonance frequency (Fig.2.5). In this study, the SPM-9600 (Shimadzu) microscope was used. This system is suitable for measuring surface topographies in the range of few μm with excellent vertical resolution, making it suitable for imaging the step-and-terrace structure of substrates and films. As an example, a topographic AFM image of an as-supplied $SrTiO_3$ substrate is shown in Fig 2.6 (a). In non-contact mode, it is possible to derive not only the height signal, but also to gain information about the chemical composition of the surface from the tip oscillation phase. A phase image is acquired together with the topography and is shown in Fig. 2.6(b).

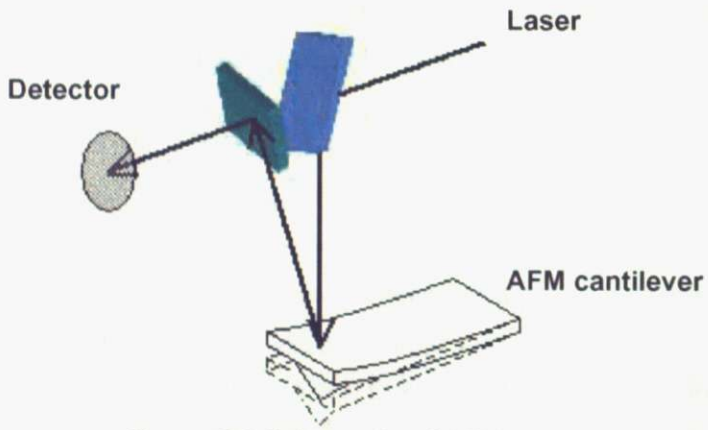


Figure 2.5 Schematic of AFM

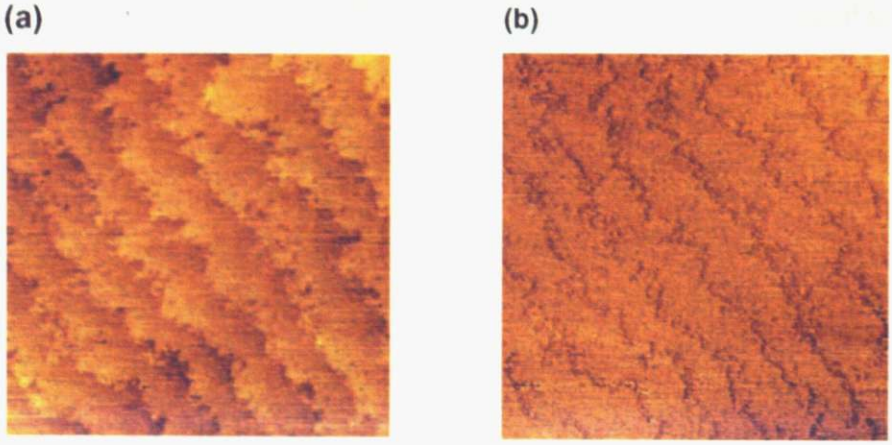


Figure 2.6 AFM 1x1 μm^2 topography (a) DFM mode and (b) Phase mode.

2.4 X-ray diffraction

X-ray diffraction (XRD) is used for evaluating the crystallinity of thin films. Conventional powder-type diffractometer is technically very simple and is used for measuring the out of plane lattice parameter of a thin film. The lattice parameter of a thin film can be determined by measuring the diffraction angle of film peak in a $2\theta/\theta$ diffraction pattern scan and calculating the atomic spacing from Bragg's law,

$$2d_{hkl} \sin\theta = n\lambda,$$

where λ is the x-ray wavelength and n is an integer giving the diffraction order. d_{hkl} is the lattice spacing and θ is the diffraction angle. The x-ray measurements were done with a Cu source, giving a wavelength λ=1.54056 Å. A typical $2\theta/\theta$ scan of a $SrTiO_3$ substrate is shown in Fig.2.7. Since the films have a nearly identical lattice parameter as the substrate, the (002) diffraction peak is usually measured for both the film and the substrate.

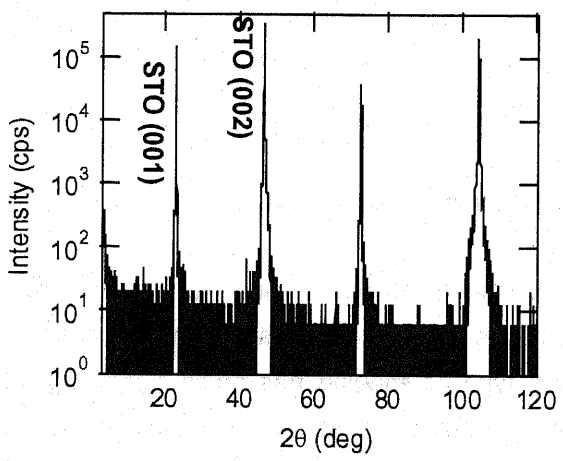


Figure 2.7 $2\theta/\theta$ scan of a $SrTiO_3$ substrate

2.5 Electron probe micro analysis

Electron probe micro analysis (EPMA) is a useful tool for measuring elemental composition of a sample. An EPMA system is usually built into a scanning electron microscope (SEM) and uses the same electron source as the SEM. This way the surface images can be taken in SEM scanning mode and the beam stopped for analysis at the desired point. The x-rays emitted from the sample under high-energy electron bombardment are analyzed with a energy-sensitive x-ray detector. Since each element emits a characteristic set of x-rays at different energies, it is possible to determine the relative atomic abundance of each element in the sample. Measurements can be done with good spatial resolution, allowing, for example, individual impurity particles to be analyzed independently from the rest of the sample.

EPMA analysis places some requirements on the sample. First of all, the sample needs to be at least moderately conducting. Otherwise it is impossible to obtain an SEM image due to sample charging. When film compositions are analyzed, there can be no overlap between the constituent elements of the substrate and the film. In this work, this was not a problem, since the films contained only Ca, Hf, Dy, and Sc. The absolute accuracy of the composition measurements is on the order of a few percent. However, comparisons between different samples can be done much more accurately. EPMA was used to determine how the thin film growth conditions affected the cation ratio in the insulator films.

2.5.1 Scanning electron microscopy

A scanning electron microscope (SEM) scans a finely focused electron beam over a rectangular area of a sample and measures the intensity of secondary electrons emitted from the sample surface at each point. This type of imaging has much better spatial resolution than optical microscopes, since the electron beam can be focused to a much smaller spot than visible light. Additionally, SEM images can give information about the conductivity of a sample. For example, insulating particles in a conducting film can be easily detected. For example, particles in a $DyScO_3$ thin film down to a diameter of about 100 nm can be seen in Fig.2.8. Another big advantage of SEM is the ability to freely change the magnification and freely scan very large areas.

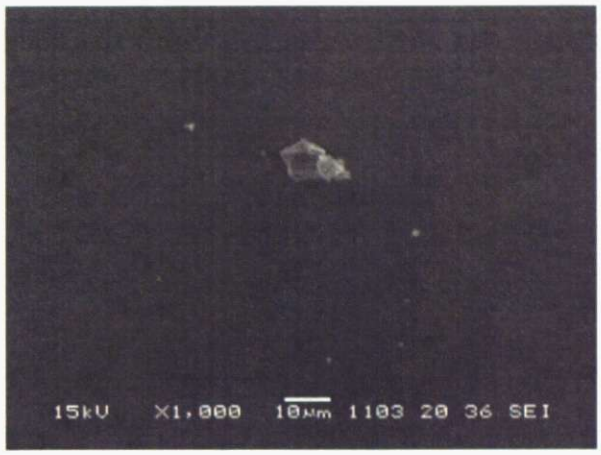


Figure 2.8 SEM image of particles in a $DyScO_3$ thin film grown on a $SrTiO_3$ substrate

2.5.2 Energy dispersive X-ray spectrometry

An energy-dispersive x-ray spectrometer (EDS) is a material composition analyzer that works by detecting characteristic x-rays from a material under intense high-energy electron bombardment. When an electron beam illuminates a small area on the sample surface, characteristic x-rays are emitted. These characteristic X-rays are picked up by an x-ray spectrometer.

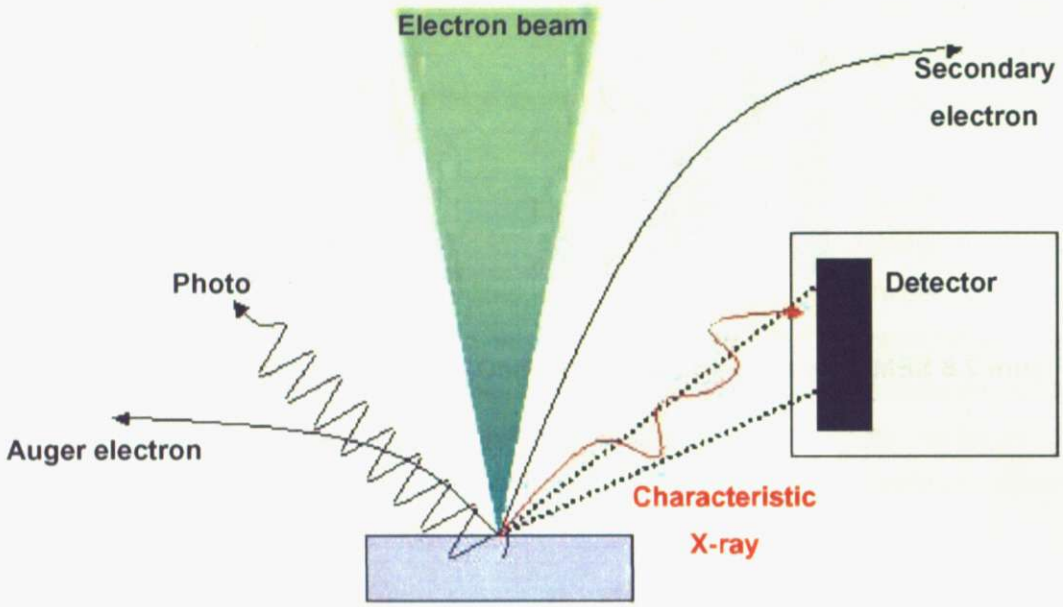


Figure 2.9 Schematic drawing of EDS

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Chapter3. The structure of field effect devices

3.1 The fabrication process of field-effect transistors

3.1.1 Introduction

Many different designs have been used to fabricate oxide-based field-effect transistors (FETs). There are three general types of transistors that are commonly used: top-gate devices, bottom-gate devices, and planar devices. Different structures can be selected depending on the intended uses of the device. In this work, the final goal is to use the carrier density tuning capabilities of an FET to induce electronic phase transitions in oxide heterostructures, it was decided that the best choice is to use a traditional top-gate design where the gate insulator is grown on the channel in a thin film deposition process. While more complicated multilayer structures can be considered for future studies, even the most basic transistor structure consisting of a single crystal channel and a thin-film gate insulator is pushing the existing oxide surface preparation and thin film growth techniques to the limit. While the basic device physics involved is well known from the 50-year history of traditional semiconductors, it is very challenging to obtain structurally and electronically clean epitaxial oxide interfaces due to the large number of elements involved.

One of the main tasks of this study was to improve the existing FET fabrication process in order to obtain a cleaner interface with a lower carrier trap density and also to scale down the device to a level where fully epitaxial gate insulators can be used. The latter task has proven to be particularly challenging, because the lattice mismatch between $SrTiO_3$, which is used as the channel material and available wide-gap insulators is typically on the order of 1 to 3 percent. This level of mismatch limits the maximum thickness of an epitaxial oxide layer that can be grown before strain relaxation forces the growth of grains in the insulator film. Grain formation, however, needs to be avoided, since grain boundaries create an inhomogeneous distribution of the gate bias field and reduce dramatically the maximum attainable gate breakdown field.

The fabrication steps of the FETs developed in this work are discussed below. The process is also illustrated in Fig. 3-1.

3.1.2 The substrate

Wet-etched $SrTiO_3$ (100) substrates were used for fabricating the transistors. The substrates show a regular step-and-terrace surface structure and can be used to grow high-quality thin films. The mask patterns used for lithography were designed to allow a large number of transistors to be fabricated on a single substrate. A typical sample size was $5x10x0.5mm^3$. In order to achieve a repeatable surface microstructure, it is possible to anneal substrates in the deposition chamber, typically at 10^{-6} Torr of oxygen in a 900 to 1000°C temperature range.

3.1.3 Insulator deposition

The insulator layer was grown directly on the as-received substrate surface. The insulator films were grown by pulsed laser deposition (PLD), using $CaHfO_3$ or $DyScO_3$ targets. The film growth parameters, such as laser fluence, oxygen pressure, and film growth temperature were selected according to objective. Depending on the type of channel interface, either amorphous or epitaxial films could be grown at this stage. It is important to note that performing the initial insulator growth at an early stage of fabrication helped to avoid interface contamination, which would otherwise result in a very high density of trap states at the interface.

3.1.4 Insulator post-anneal

The PLD process is a strongly non-equilibrium high-energy process that always damages a thin interface layer. The dominant damage mechanism is the loss of oxygen from the surface layer of the substrate. Oxygen vacancy states act as donors and result in an conducting channel interface. The channel current of devices that contain vacancy-rich interfaces can typically not be modulated. Effectively the off-state current of the device is very high. The oxygen loss is a particularly serious problem for samples grown at high temperature. For example, epitaxial films were typically grown at around 700°C.

In order to avoid this problem, oxygen needed to be loaded back into the sample. This can be done by annealing the sample at 300 to 400°C in an oxidizing atmosphere. In this work, the samples were annealed in air in a laboratory furnace.

3.1.5 Electrode definition

The most simple FETs can be fabricated by using simple metal stencil masks. The minimum feature size that can be reached with stencil masks is about 100 μm. In this work, my aim was to explore the scalability of the transistor structures and the only possibility was therefore to use photolithography. The first lithography step was used to define the source and drain electrode shapes and also the channel dimensions. The initial insulator film was spin coated with resist, exposed, and developed. The processing was done in a clean-room environment to avoid sample contamination. Various different mask patterns were used to fabricate devices with channel dimensions ranging from 100 x 500 μm^2 to 10 x 50 μm^2. At the end of the lithography step the source and drain regions of the FETs were left exposed.

3.1.6 Electrode etching

The samples were placed in an Ar electron cyclotron resonance (ECR) plasma milling machine.

The ion energy was typically set at 500 eV. This energy is sufficient to etch away the exposed part of the insulator film and etch into the substrate surface. Since the etching environment is reducing, the milling process results in the formation of an amorphous and strongly oxygen-deficient layer at the sides and bottom of the etched wells. The composition of the etched pit surface can be written as $SrTiO_{3-\delta}$. Considering that oxygen vacancies function as donors, such layers become metallic and can be used as source and drain electrodes.

3.1.7 Electrode plugs

In order to planarize the device after electrode pit etching, the sample was covered with a layer of SiO_x, which was evaporated thermally. The thickness of the SiO_x layer was adjusted to equal approximately the total etch depth. This step was necessary to obtain a flat surface for the second insulator layer deposition. The SiO_x layer deposition reduced the likelihood that the gate dielectric breakdown occurs at the source or drain electrode edge of the channel.

3.1.8 Second insulator layer

The first photoresist layer was removed, also removing the unwanted parts of the SiO_x layer by lift-off. After surface cleaning, the device surface was nearly flat, with the ion-milled source and drain electrode pits having been filled with SiO_x. The sample was moved back into the deposition chamber and a second, amorphous gate insulator layer was grown at room temperature. The second insulator layer was amorphous. The second layer was necessary in order to improve the breakdown characteristics of the gate stack. An amorphous layer was used because the oxygen-deficient electrode regions can not withstand the high temperature required by epitaxial growth.

3.1.9 Gate definition

A second photoresist patterning step was performed in order to define the shape of the gate electrode. Special care was required to align the second lithography mask accurately with the source and drain electrodes so that the gate electrode would cover the channel part of the device. The resist was developed, exposing the gate electrode region and parts of the source and drain electrode regions that would serve later as bonding pads.

3.1.10 Electrode deposition

The surface electrodes were formed by thermal evaporation of aluminum, covering the exposed parts of the gate, source, and drain electrode regions.

3.1.11 Liftoff and bonding

The photoresist mask was removed, lifting off excess aluminum. The sample was then mounted on a ceramic chip carrier and electrical contacts were made to the devices on the substrate. The gate electrodes can be attached by normal silver paste, but the source and drain electrodes need to make contact with the buried conducting layer at the bottom of the source and drain electrode pits. Contact to the buried electrode layers was made by ultrasonic wire bonding, which can easily crush the thin insulator layers. Ultrasonic bonding provided reliable contacts that could also be used at cryogenic temperatures.

The main merit of this process is the ability to maintain a contamination-free channel interface. Depositing the first insulator layer as the first step was thus critical to achieving devices with good switching performance. Good device performance was confirmed in this device structure with amorphous $CaHfO_3$ gate insulator, where the obtained mobility numbers and carrier trapping levels were comparable to epitaxial devices that were fabricated with simple stencil masks [1]. This showed that chemical and physical contamination of the original substrate surface is critical and has to be avoided if electronically useful devices are to be prepared.

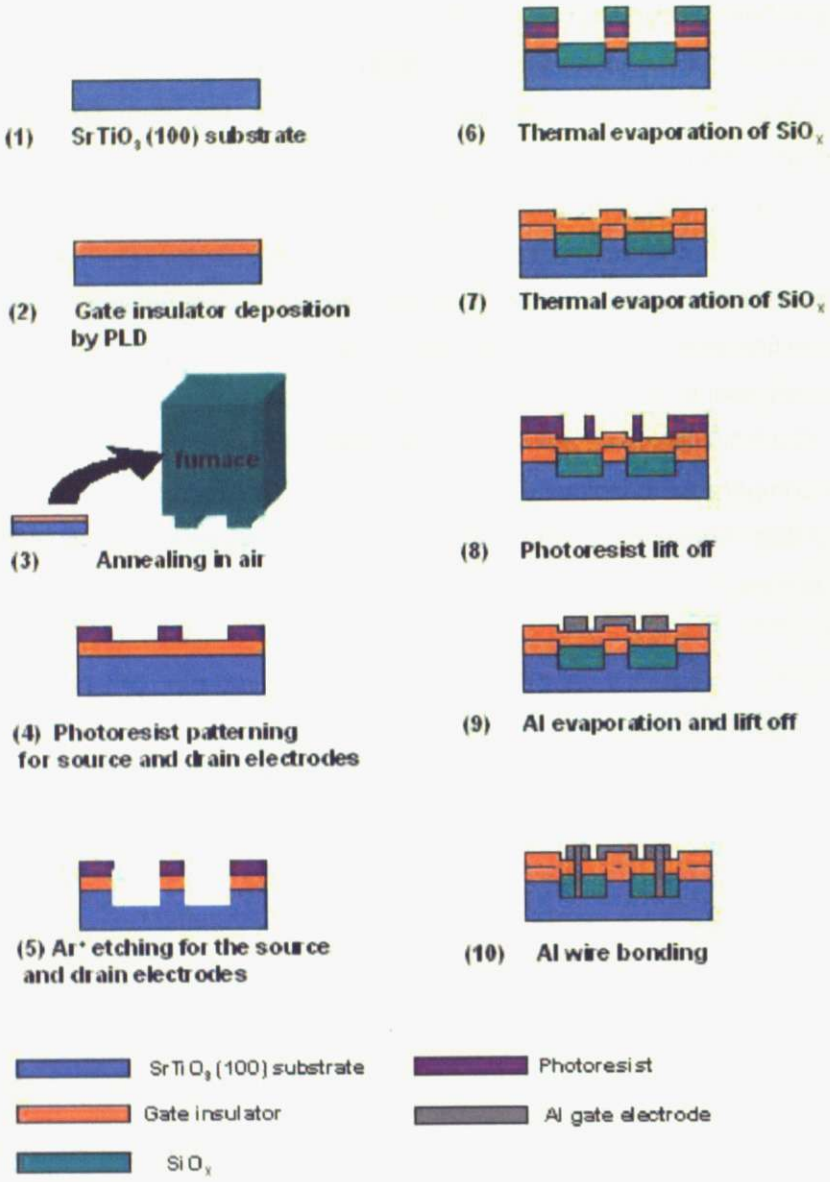

Figure 3.1. Fabrication steps of a field-effect transistor device.

3.2 Photolithography

Photolithography is used to transfer optically patterns from a mask to the surface of a resist-covered sample. In this work, the transfer process was done by using a chrome-on-quartz shadow mask that was brought into contact with the photoresist layer on the sample surface in a special mask aligner machine. Exposing the resist with an ultraviolet light source, results in polymerization in the exposed parts of the resist film. By using either a positive or a negative resist, either the exposed or unexposed part of the resist can be removed after the developing process. Positive-type resist was used in this study. In this type of resist, the exposed regions become more soluble and can thus be more easily removed in the developing process. The resist was Rohm and Haas S9912NX.

In order to prevent the contamination of the device surface during wet processing, lithography was performed in a clean environment room. The clean room has a nominal Clean room rating of JIS CLASS 5, although this is not always reached as the room has no air lock.

Before optical processing, the sample surface has to be coated with a thin layer of the photoresist material. This is done with a spin-coater, which has a rapidly spinning vacuum chuck in the middle, holding the sample crystal. A small amount of photoresist was applied to the center of the sample and the resist was allowed to spread while the sample rotation speed was accelerated. Initial spinning was done at a speed of 2000 rpm for 5 seconds, followed by spinning at 5000 rpm for 30 seconds. This process creates a uniform coating layer with a thickness of approximately 1 μm.

After spinning the resist is still liquid and can not withstand touching by the contact shadow mask. In order to prevent the contamination of the mask by resist material, the resist-coated sample was baked at 100°C for 13 minutes. This is a so-called soft-bake, which allows the resist to be easily removed at the lift-off stage.

The sample was mounted in the mask aligner and the position was adjusted so that the sample is parallel to the mask and can be brought into contact with the mask pattern. Position alignment is not critical at the initial lithography step where the source and drain electrodes are defined, but position alignment becomes critical at the second lithography step, when the gate electrodes are defined, since the strip-like gate lectrodes must be accurately positioned relative to the etched source and drain electrodes. This can be particularly challenging for the smallest, 10 μm devices.

Once the sample is properly aligned, the resist is exposed with a high-pressure mercury lamp for 13 seconds. The exposure time was optimized to obtain the best edge definition.

The exposed resist was developed using a Rohm and Haas MF CD-26 developer. The sample was dipped into developer and then rinsed for 25 seconds. After that, the sample was dipped and rinsed in ultra-pure water for 30 seconds two times. This step removed the unwanted resist from the sample surface. The sample was then dried and moved either into the ion milling machine for source and drain region etching or into the thermal evaporation machine for gate electrode evaporation.

Images of a sample taken after the lithography step are shown in Fig.3.2.

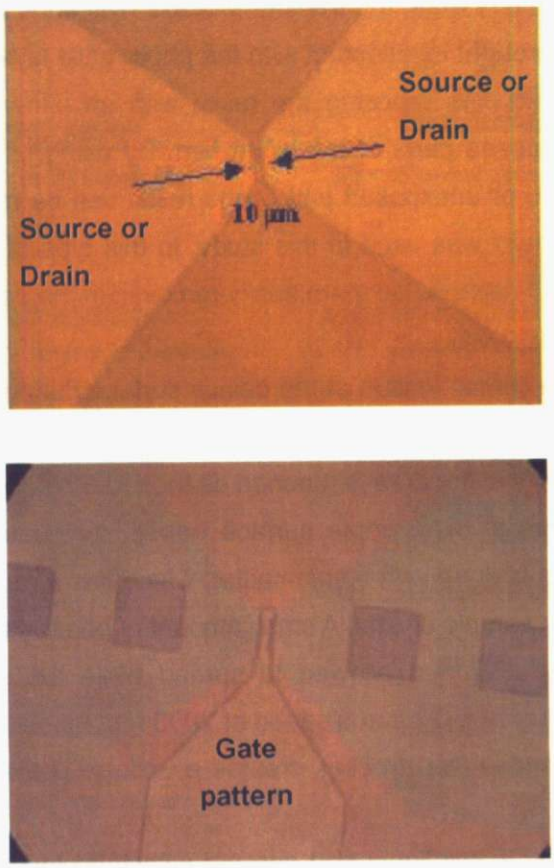

Figure 3.2. Top: patterning of the source and drain electrodes for an FET with a 10 μm channel length. Bottom: Source, drain and gate electrodes patterning, showing the aligned gate electrode covering the channel region.

3.3 Argon Ion milling

From the point of view of device fabrication, the easiest way to fabricate the source and drain electrodes in a top-gate device is to do so before the gate insulator is grown. Experiments, however, showed that this order of fabrication steps can lead to crystal surface contamination that has a negative effect on the device performance. It was therefore necessary to grow the insulator layer first and then insert the source and drain electrodes into the heterostructure.

The solution to this problem was to use Ar ion milling and instead of depostiong metal electrodes or metallic oxide electrodes, it is actually possible to use the $SrTiO_3$ substrate itself as a metallic electrode material. Metallic conductivity can be created in $SrTiO_3$ by strong doping, which happens naturally in the milling process, which removes oxygen from the crystal surface. Metallic conductivity of oxygen-deficient metallic $SrTiO_{3-\delta}$ electrodes has been studied in the past [1] and the thermal stability of the oxygen-deficient layers has been confirmed [2].

In the Ar ion milling process, the Ar gas is ionized within a microwave cavity operating at 2.45 GHz. In order to improve the ionization efficiency, the plasma generator uses a magnet to force electrons into circular orbits. The electron cyclotron resonance condition was obtained at a magnetic field of 875 Gauss, generating sufficiently ionized plasma in a comparatively high degree of vacuum. Argon ions were accelerated at 500 V and bombarded the sample surface. Ar gas flow rate was 10 sccm. The layout of the milling machine is shown in Fig. 3.3.

In this study $CaHfO_3$ or $DyScO_3$ films on $SrTiO_3$ samples were etched by Ar ions to obtain conducting oxygen-deficient $SrTiO_3$ source and drain electrodes. The etching rate is shown in Fig. 3.4. Samples were etched for different amount of time and the etched feature depth was measured by a stylus profilometer (Dektak). Measurements generally showed that there is a dead zone at the beginning of the etching process, but following that, the etching depth is a linear function of time.

A typical etching depth used in the FET process was 50 nm. Ohmic conductivity was confirmed in a $SrTiO_3$ sample that was etched to a depth of 50 nm. The current-voltage characteristic of the milled surface is shown in Fig.3.5.

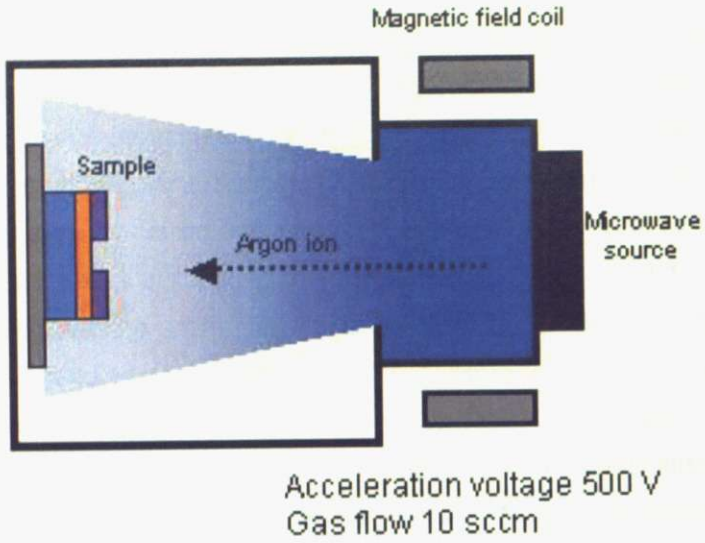

Figure 3-3. Schematic drawing of the Argon ion etching system

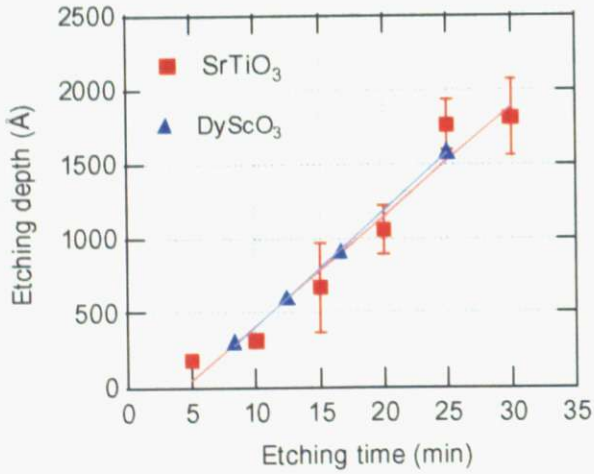

Figure 3-4 Etching rate for STO substrates and DSO film

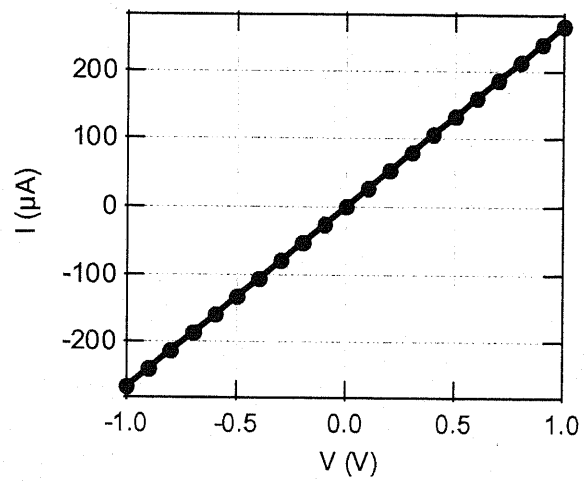

Figure 3-5. I-V characterization in the region of oxygen-deficient STO

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2. T.Sato, K.Shibuya, T.Ohnishi, K.Nishio, and M.Lippmaa, Jpn.J.Appl.Phys. 46, L515 (2007)

Chapter4. Growth and characterization of $DyScO_3$ thin films

4.1 Introduction

In this study, the $DyScO_3$ (DSO) wide-gap insulator was selected as the gate insulator material for $SrTiO_3$ (STO) single crystal FETs. $DyScO_3$ has a smaller lattice mismatch with $SrTiO_3$ than other commonly available gallate, zirconate or hafnate wide-gap insulators that are compatible with the perovskite structure. This material is therefore useful for growing atomically flat epitaxial thin films on STO substrates. In general, when a heteroepitaxial thin film has a different in-plane lattice parameter as the substrate, lattice relaxation occurs once the film thickness becomes larger than a critical value. This value depends on the level of mismatch between lattice parameters, with larger mismatch resulting in a faster relaxation in thinner layers. Strain relaxation, in turn, results in the formation of a polycrystalline grain structure in the film. From the point of view of FET operation, it is very important to maximize the breakdown strength of the insulator layer and also make sure that the electric field in the transistor channel is spatially homogeneous. This means that the formation of grains needs to be avoided. However, even materials that have smaller lattice mismatch, such as $NdGaO_3$ (NGO), may form three-dimensional structures and are therefore not good gate insulators [1]. So far, STO FETs with epitaxial $CaHfO_3$ (CHO) gate insulators have been fabricated and used for studies of the electrical properties of STO heterointerfaces. However, such devices with epitaxial CHO gate insulators did show degraded FET performances such as reduced breakdown strength due to the formation of grain structure. As can be seen in Table 4-1. DSO has a smaller mismatch with STO than does CHO. Consequently, it has been reported that DSO-base FET devices show better performance characteristics than CHO-based FETs [2]. For these reasons, DSO was selected for the process optimization work presented in this thesis.

	Lattice constants (Å)					
STO (cubic)	3.905	3.905	3.905			
	a	b	c	psudo-cubic $\sqrt{a^2+b^2}/2$	$,c/2$	Average mismatch
CHO	5.578	5.719	7.982	3.994	3.991	2.3%
DSO	5.44	5.713	7.887	3.944	3.943	0.99%

Table 4.1 Lattice constants of $SrTiO_3$, $DyScO_3$ and $CaHfO_3$. pseudo-cubic lattice constants and the average mismatch are also shown.

4.2 Growth of $DyScO_3$ films

The $DyScO_3$ thin films were grown by pulsed laser deposition (PLD). The ablation target was a polycrystalline DSO pellet (Toshima Manufacturing Co., Ltd.) with a density of 3.68 g/cm^3, which is 53% of the ideal density. Growth conditions were optimized by tuning the laser fluence (laser energy and spot size), oxygen pressure, and the film growth temperature. Ohnishi et al. have reported that thin film quality, including crystallinity and cation ratio depend on PLD conditios, especially laser fluence [3,4]. The influence of laser fluence on film properties was studied in the 0.3 J/cm^2 to 1.0 J/cm^2 range, while the oxygen pressure was varied from 1 mTorr to 100 mTorr. Based on earlier work on $DyScO_3$ film growth, the substrate temperature was fixed at 700°C.

The film growth was monitored by recording reflection high-energy electron diffraction (RHEED) specular intensity oscillations during the deposition. Typical RHEED patterns observed before and after $DyScO_3$ deposition along the (100) direction of the substrate are shown in Fig. 4.1. Streakiness of the film pattern shows that the surface has considerably larger roughness than the substrate. Oscillation of the specular intensity during $DyScO_3$ deposition is shown in Fig.4.2.

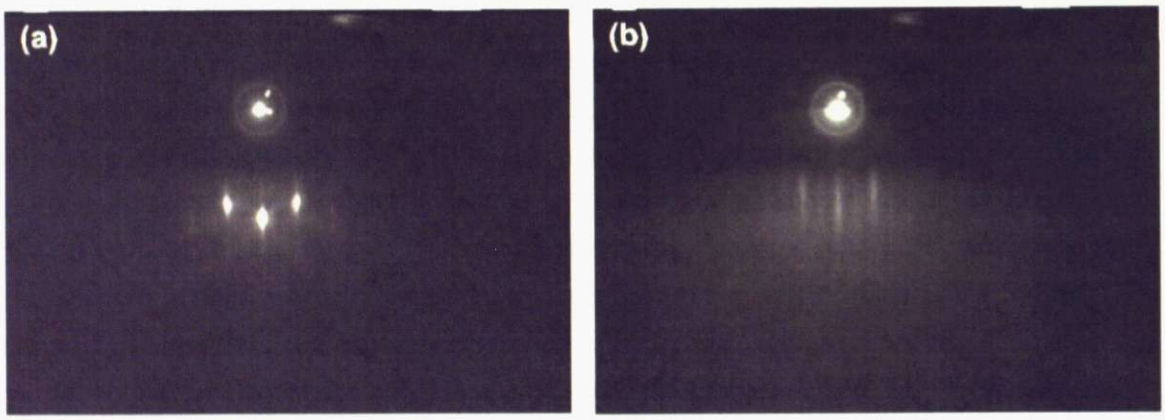

Figure 4.1. RHEED patterns of (a) STO surface, (b) DSO grown at 1 mTorr oxygen pressure

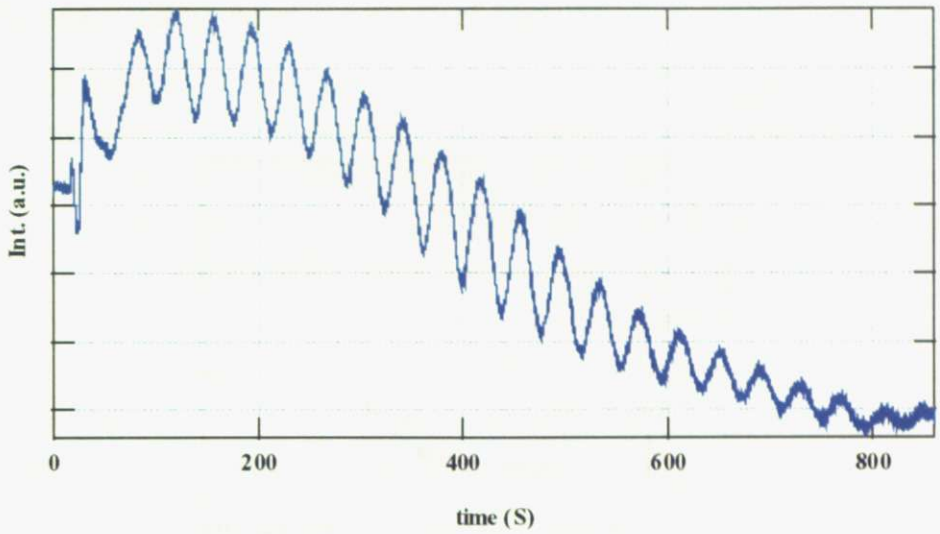

Figure 4.2. RHEED intensity oscillation observed during $DyScO_3$ film growth.

Two type of optimization were done for DSO thin films growth. In order to map the effects of background oxygen pressure on the morphology and composition of the films, the oxygen pressure was varied between 1 and 100 mTorr while the laser fluence was fixed at about 0.55 J/cm^2 and the film growth temperature also was fixed at 700°C.

The effect of laser fluence on the film properties was studied by varying the energy density of the excimer laser light on the target surface between 0.3 and 1.0 J/cm^2, while the oxygen pressure was fixed at 1 mTorr and the growth temperature was fixed at 700°C.

The inverse growth rates, given as laser pulses per monolayer of grown film, plotted as a function of laser fluence and oxygen pressure are shown in Fig. 4.3 (a). It can be seen that the growth rate drops rapidly above 10 mTorr, with more than 200 pulses being required to grow a single monolayer of film at 100 mTorr. This compares with the typical PLD growth rate of about 10 pulses per monolayer of film. The film growth rate is obviously also strongly affected by the fluence, with the rate increasing approximately linearly with the laser energy density. As shown in Fig. 4.3 (b), the deposition rate is also a function of the laser spot size on the target surface. By adjusting the laser pulse energy, it is obviously possible to achieve the same energy density for different spot sizes. For a larger spot size, the total energy delivered by the laser is higher, which means that the deposition rate is also larger, i.e. fewer pulses are needed to grow a single monolayer. This effect is further enhanced by changes in the shape of the ablation plume, with the plume becoming more focused along the target surface normal for larger spot sizes. For very small ablation spot areas, the plume tends to be more isotropic, reducing the amount of material that is actually transferred from the target to the film surface.

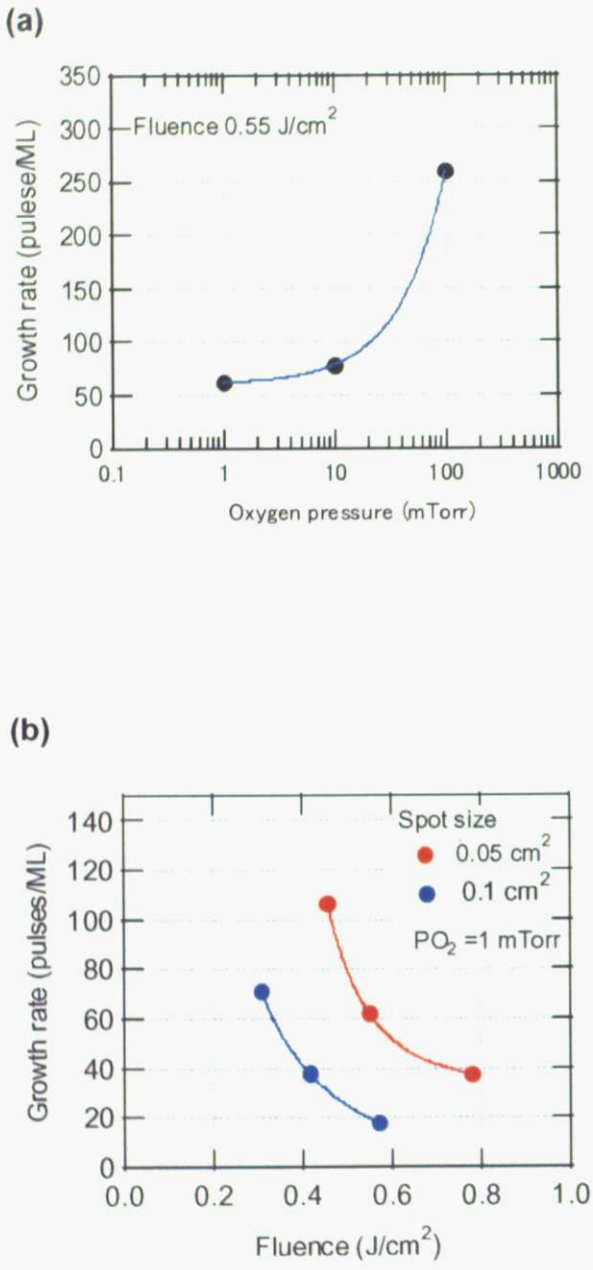

Figure 4.3. Growth rate plotted as a function of (a) oxygen pressure and (b) laser fluence. Spot size used two type, 0.05 and 0.1 cm^2

4.3 Crystallinity and cation ratio

The crystallinity of the $DyScO_3$ films was analyzed by x-ray diffraction (XRD). The cationratio was measured with an energy-dispersive spectrometer in a scanning electron microscope (SEM-EDS). A typical XRD 2θ–θ scan of a DSO thin film on STO is shown in Fig.4.4 (a). The measured out-of-plane lattice parameter of the film was 3.9958 Å. A more useful technique for crystllinity measurement is the rocking curve, shown in Fig. 4.4(b). The full width at half maximum (FWHM) of the curve is 0.616 degrees. The cation ratio was determined by measuring the relative intensities of Dy and Sc EDS peaks for each sample. While the absolute accuracy of EDS is limited to a few percent due to the unknown correction factors for each element, it is still possible to analyze accurately the changes of cation ratio as the deposition parameters are changed.

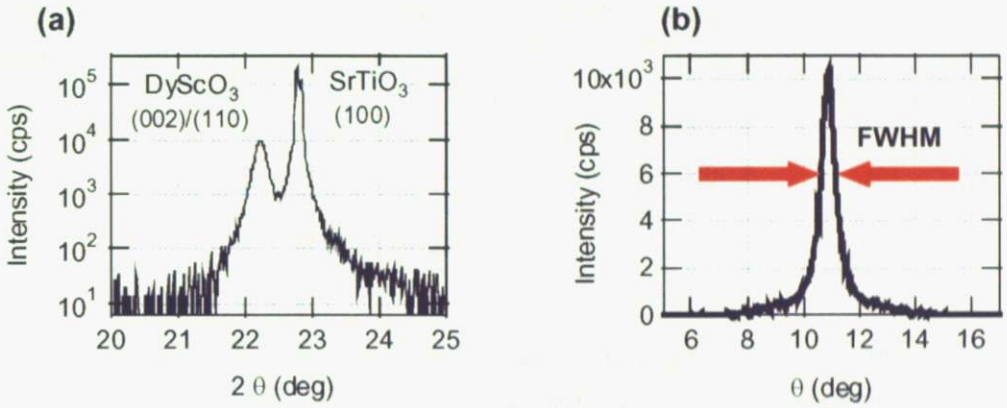

Figure 4.4. (a) Intensity of the DSO thin film on STO substrate by 2θ - θ scan. (b) Rocking curve of DSO thin film by θ scan

First, the effects of changing the oxygen pressure are discussed. A series of samples was fabricated at pressure from 1 mTorr to 100 mTorr while the laser fluence was fixed at 0.55 J/cm^2 and the film growth temperature was set at 700°C. The out-of-plane lattice parameter and the width of the rocking curve for these DSO thin films are shown in fig.4.5. As the oxygen pressure increased, the out-of plane axis length also increased. Since none of the cations in the insulator can assume multiple valence states, it was considered unlikely that oxygen content alone could account for the large lattice parameter change and the large increase of the rocking curve width. A more likely cause for the lattice constant change is the deviation of the film composition from the desired 1:1 Dy:Sc ratio.

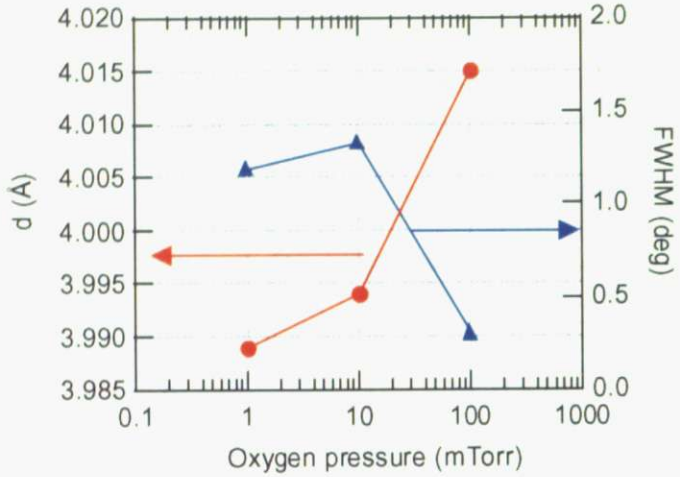

Figure 4.5. The effect of the oxygen pressure during deposition on the out of plane lattice parameter and the rocking curve width.

The cation ratio was therefore also studied as a function of oxygen pressure and the results are shown in Fig.4.6. It was found that the oxygen pressure has a very strong effect on the Dy:Sc ratio, with the deviation from the desired value increasing rapidly at pressures above 10 mTorr. This curve shape follows closely the deposition rate curve. It is unlikely that this effect is caused purely by changes in the composition of the ablated species, since the laser fluence was well above the ablation threshold of around 0.3 J/cm^2. It is more likely that this effect was caused by the change in the shape and size of the ablation plume, since at 10 mTorr the plume expansion is no longer in the molecular beam epitaxy regime. Instead, the plume strongly interacts with the background gas, evidently resulting in a nonstoichiometric transfer of material from the target to the film. This finding can have a serious impact on the fabrication of epitaxial transistors, since it may force the insulator growth to lower oxygen pressures, where oxygen loss from the substrate surface can become a serious problem. A strongly nonstoichiometric insulator film can also be assumed to have a reduced dielectric breakdown strength and increased charge trapping at low temperature.

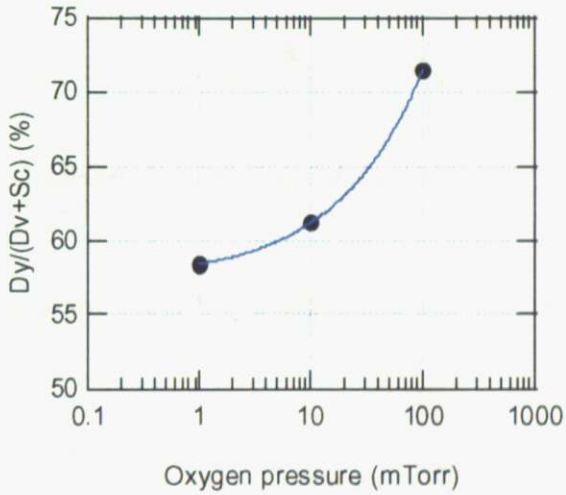

Figure 4.6. Cation ratio measured by SEM-EDS as a function of the oxygen partial pressure.

In addition to background pressure, the shape and size of the PLD ablation plume can also be changed by altering the size of the ablation spot and the laser energy, even when the energy density is kept constant. The effects of changing the laser fluence on the film crystallinity and composition were checked by XRD and SEM-EDS. The laser fluence was changed from approximately 0.3 to 1.0 J/cm^2. The size of the ablation spot was changed by moving the focus lens (f=300 mm). Two spot sizes on the target were selected, 0.05 cm^2 and 0.1 cm^2. The oxygen partial pressure was fixed at 1 mTorr and the film growth temperature was fixed at 700°C. The XRD results are shown in Fig.4.7. In this case, the crystallinity was compared by looking at the XRD 2θ scan film peak intensity, which was normalized by the intensity of the STO substrate peak

intensity and the film thickness. It was found that typically higher fluence gives better film quality. And another important finding was that different laser spot sizes, even at the same laser fluence gave different thin film quality: Larger spot size typically gave better quality films in terms of crystallinity.

The SEM-EDS result of the same films are shown in Fig.4.8. These plots show no conclusive changes in composition in the fluence range between about 0.4 and 0.6 J/cm^2. A larger spot size may have improved the cation ratio, bringing it closer to the Dy/Sc=1 ratio, but it is obvious that the effects of fluence are much less important than the background pressure.

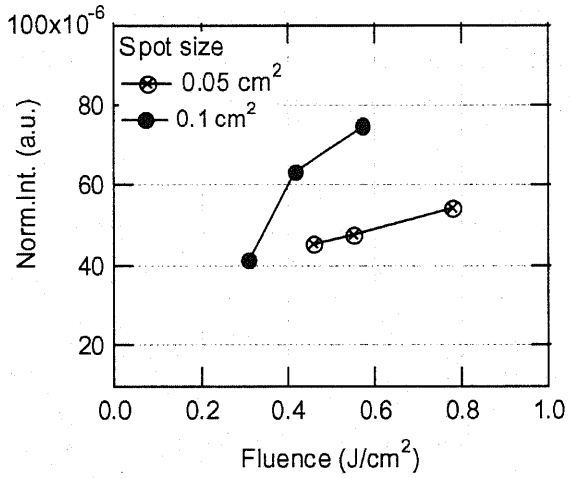

Figure 4.7. Normalized XRD 2θ scan intensity plotted as a function of fluence.

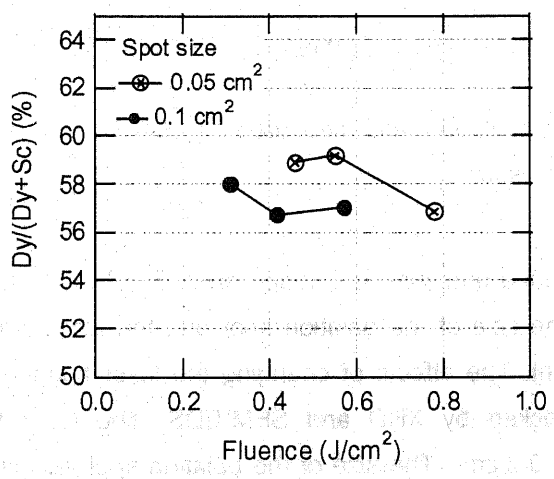

Figure 4.8. Cation ratio plotted as a function of fluence.

4.4 Electrical properties of $DyScO_3$ thin films

While the crystallinity and composition of the films are useful guides for optimizing crystal growth in general, for insulator films it is still necessary to determine the actual dielectric properties. Measurement of the breakdown field is the most interesting characteristic. For these measurements, planar capacitor structures were fabricated. First a thin insulator film was

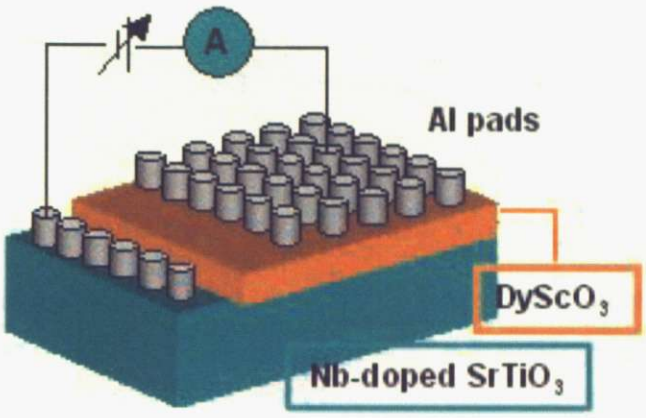

Figure 4.9. Schematic drawing of capacitor. Substrate is 0.5 wt% Nb-doped STO. After deposition DSO thin films on STO by PLD, Al electrodes were evaporated through the stencil mask with 200 μ m diameter.

deposited on a metallic Nb-doped (0.5wt%) STO substrate by PLD. Aluminum pads were evaporated on the thin film surface through a stencil metal mask. The pads were circular with a diameter of 200 μm, giving a pad area of approximately 0.03 mm^2. A schematic drawing of the capacitors is shown in Fig.4.9. There were about 100 pads on a sample surface. In order to obtain more reliable breakdown numbers, many pads were measured and the histograms were analyzed. For breakdown measurements, the breakdown current was defined as 1 $\mu A/cm^2$. Breakdown curves, like the one shown in Fig.4.10 were measured for each of the 100 pads and the average breakdown strength was estimated by fitting the histogram with a Gaussian curve (Fig.4.11).

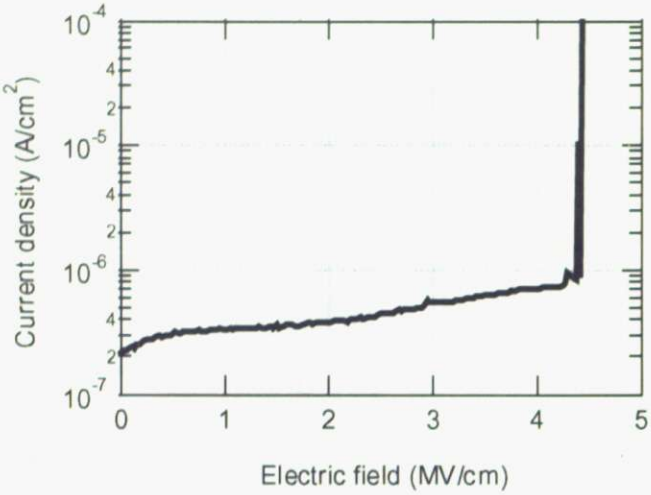

Figure 4.10. Typical current density-electric field curve of gate insulators.

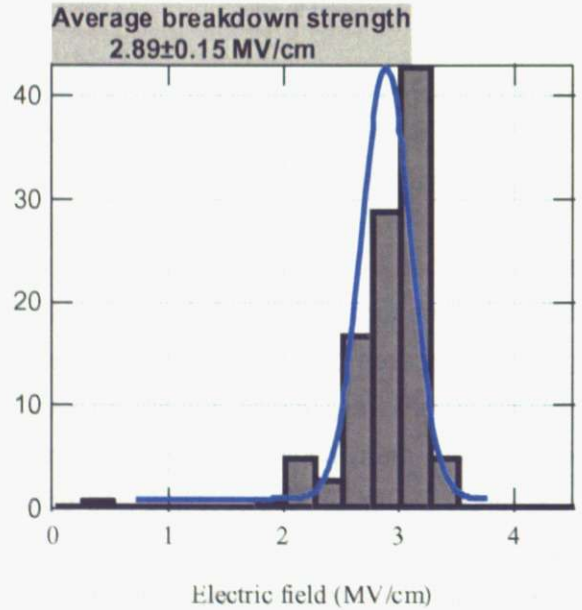

Figure 4.11. Gaussian fitting of breakdown strength. Average breakdown strength was obtained from Gaussian fitting.

The breakdown field strength was studied by changing the partial oxygen pressure and the laser fluence, since these parameters were found to affect the structural properties of the films most strongly. Film thickness for all samples was about 40 nm. The oxygen partial pressure was changed from 1 mTorr to 100 mTorr and two types of laser fluence were selected for film growth, 0.3 J/cm^2 and 0.6 J/cm^2. The results of these experiments are summarized in Fig.4.12. It was found that higher oxygen pressure typically resulted in lower breakdown strength. This tendency matches the crystallinity and cation ratio behavior, i.e. nonstoichiometric films with reduced crystallinity also break down more easily. The effect of changing the laser fluence was less dramatic, but it appeared that generally higher fluence and lower oxygen pressure is suitable for $DyScO_3$ film growth.

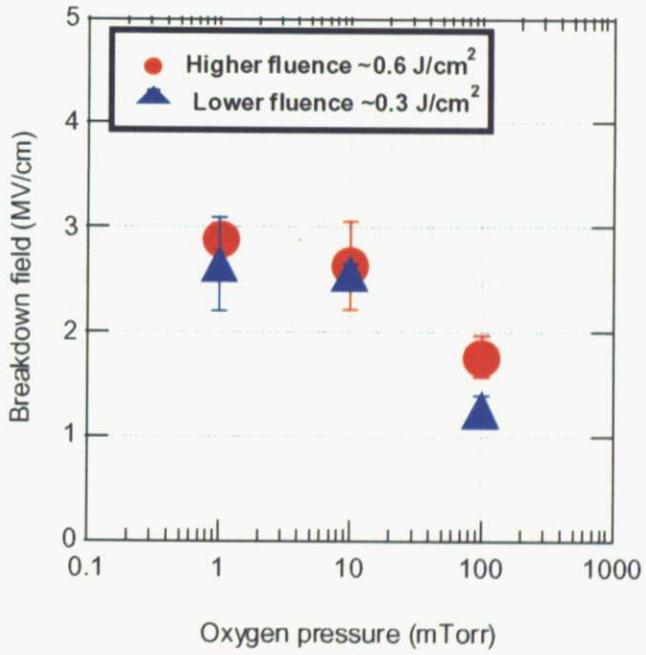

Figure 4.12. The results of breakdown strength measurements as a function of laser fluence and oxygen pressure during the $DyScO_3$ film growth.

4.6 Conclusions

Wide-gap insulator $DyScO_3$ thin films were fabricated on $SrTiO_3$(100) in order to estimate how the crystallinity and cation ratio are affected by the film growth conditions, laser fluence and oxygen pressure. Additionally films were fabricated on 0.5 wt% Nb-doped $SrTiO_3$(100) substrates in order to estimate the dielectric breakdown strength of the insulator. As a result, it was found that the optimal oxygen partial pressure during growth is around 1 mTorr and the laser fluence should be as high as possible, although limits are usually set by the level of damage that can be tolerated in the $SrTiO_3$ substrate surface layer. The most likely mechanism for the improvement of crystallinity under these conditions is the improvement of the cation ratio. Deviation of the cation ratio from the ideal value tended to increase strain, strengthen the grain structure and reduce breakdown strength. It is generally important to be mindful of cation ratio changes in case of PLD film growth. It is apparent that the assumption of stoichiometric material transfer from target to film is not always true and the errors can be very large, especially when films are grown under high background gas pressures. This kind of pressure dependence has been reported [5]. Film growth parameters such as laser fluence, partial pressure and film growth temperature need to be optimized in terms of XRD parameters, but the composition has to be monitored as well. SEM-EDS was found to be a good technique for this purpose, since systematic changes can easily be measured even if the absolute accuracy is low.

In this study, 1mTorr oxygen pressure and high fluence were found to be suitable for $DyScO_3$ growth from the point of view of crystallinity and breakdown strength. Even the best films, however, appeared to be slightly Dy rich, with Dy/(Dy+Sc)=57%.

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Chapter5. Scaling of channel size and insulator thickness

5.1 Introduction

As described in Chapter 4, the FET fabrication process was improved in order to reduce the defect density at the channel / insulator interface. This was mainly achieved by maintaining a cleaner interface and reducing the structural mismatch between the $SrTiO_3$ substrate and the insulator film. For comparison, FETs were fabricated using the new process, but still using the $CaHfO_3$ insulator, which had been used in simpler stencil-mask devices. It was found that the new fabrication process did indeed reduce the trap density at the interface, but the devices showed disappointingly poor breakdown strength. Therefore high electric field could not be applied to gate electrode, limiting the usefulness of the devices as tools for inducing phase transitions in oxides. The poor breakdown performance was not limited to epitaxial devices. The same problem also affected FETs where a purely amorphous insulator was used. This pointed to an extrinsic source for reduced dielectric strength of the insulator, such as the presence of particles in the film. It is known that the explosive evaporation process of PLD can generate very high local pressures on the target surface, ejecting solid particles from the target. These particles can end up on the film surface, and if a large particle does appear in the channel region of an FET, it can easily result in a quick breakdown of the insulator under MV/cm-order electric fields. Since it is difficult to modify the PLD evaporation process in such a way as to avoid the large particles from reaching the film, it was considered easier to attempt to scale down the FET devices, and thus increase the yield of clean devices that are not affected by the presence of particles. Additionally, even if grains do form in the insulator due to strain relaxation, the probability of a large grain boundary occurring at the channel position would also be reduced. A third advantage of a scaled-down FET is that the insulator layer could be made thinner, according to general FET scaling rules. For a scale-down by a factor of 10, it would be possible to avoid the use of a double-layer insulator completely.

In the devices described so far, the channel length and width were 100 μm and 500 μm, respectively. [1][2]. This channel size was originally set by the use of stencil masks for the device patterning and since photolithography is used in the new process, it would be just as easy to fabricate 10 μm-scale devices instead of the 100 μm feature size. The channel scaling studies were done by selecting 4 channel sizes, always maintaining the same width / length ratio of W/L=5. The channel length and width were 10 μm / 50 μm, 20 μm / 80 μm, 40 μm / 200 μm, and 100 μm / 500 μm (*W/L=5*).

Another scaling parameter is the film thickness. The merit of thin film gate insulator is the ability to achieve the same charge modulation at a lower gate voltage. The film thickness needs to be

closely optimized, because for films that are too thick, the grain structure due to in-plane strain relaxation could result in poor breakdown strength. Conversely, if the gate film was too thin, for example a few monolayers, the tunneling current could also result in poor breakdown strength.

5.2 The effects of device scaling

5.2.1 Sample preparation

All experiments were done with $DyScO_3$ films deposited on Nb-doped $SrTiO_3$ (001) substrates. The $SrTiO_3$ substrates were annealed in air at 900° for 1 hour in order to obtain a step-and-terrace surface, as shown in Fig.5.1. Aluminum pad electrodes were evaporated on the film surface for breakdown measurements. The Al pads had a 200μm diameter. The laser fluence was fixed at approximately 0.3 J/cm^2. Oxygen pressure was 1 mTorr and the film growth temperature was 700°C. Samples with film thicknesses of 2.5, 5, 10, 20 and 35 nm were prepared.

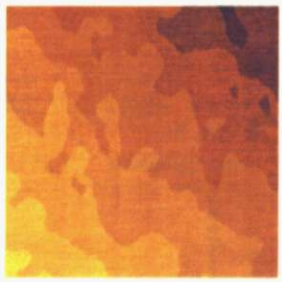


Figure 5.1. 1x1 μm^2 topography of an annealed Nb-doped $SrTiO_3$ substrate. 900°C for 1 hour in air

5.2.2 Measurement and results

The measurement geometry was the same as described in Chapter 4, Fig. 4-9. Result of film thickness optimization are shown in Figs.5.2 (a) and (b). Fig.5.2 (a) shows the current vs. electric field curves for each sample. The breakdown current was defined as 1 μA/cm^2. About 100 pads were measured for each sample and the average breakdown field strength was estimated by Gaussian fitting. It can be seen immediately in Fig. 5.2 (a) that the thinnest film has no definable breakdown field. It is possible that the 2.5-nm film suffered from structural defects, such as pinholes or, more likely, the current is simply caused by tunneling through the thinnest parts of the

film. The breakdown field can be seen to increase up to about 10 nm thickness, reaching about 3 to 4 MV/cm, For larger thicknesses, the breakdown field is again reduced, presumably due to the formation of grain boundaries. Fig.5.2 (b) shows current density vs voltage for the same samples. Samples with 2.5, 5, 10, 20 and 35 nm thick were measured. Average breakdown field strength for this series of samples is shown in Fig.5.3. Below 10 nm thickness, tunneling current became dominant. The 5-nm-thick $DyScO_3$ did not work as insulator at all. Breakdown strength started to drop also above 20 nm thickness because of grain formation. The optimum thickness appears in the 10 to 20 nm range, which is a good thickness range for FETs. Considering that the 100 x 500 μm^2 channel devices used an insulator film that was about 50 nm thick, the 20 nm films could work well in devices that are scaled down by a factor of 2 to 5, i.e. channel length of 20 to 50 μm, which is well above the feature sizes that can be fabricated with the simple lithography tools that were available for these experiments.

AFM surface topographies of four insulator films are shown in Fig.5.4. The 2.5, 5 and 10 nm-thick samples show a step-and-terrace surface. The steps start to disappear in the 20 nm sample due to the gradual formation of grain structure, which leads to surface roughening. Samples that were thicker than 20 nm showed very rough surfaces and also high leak currents and low breakdown fields.

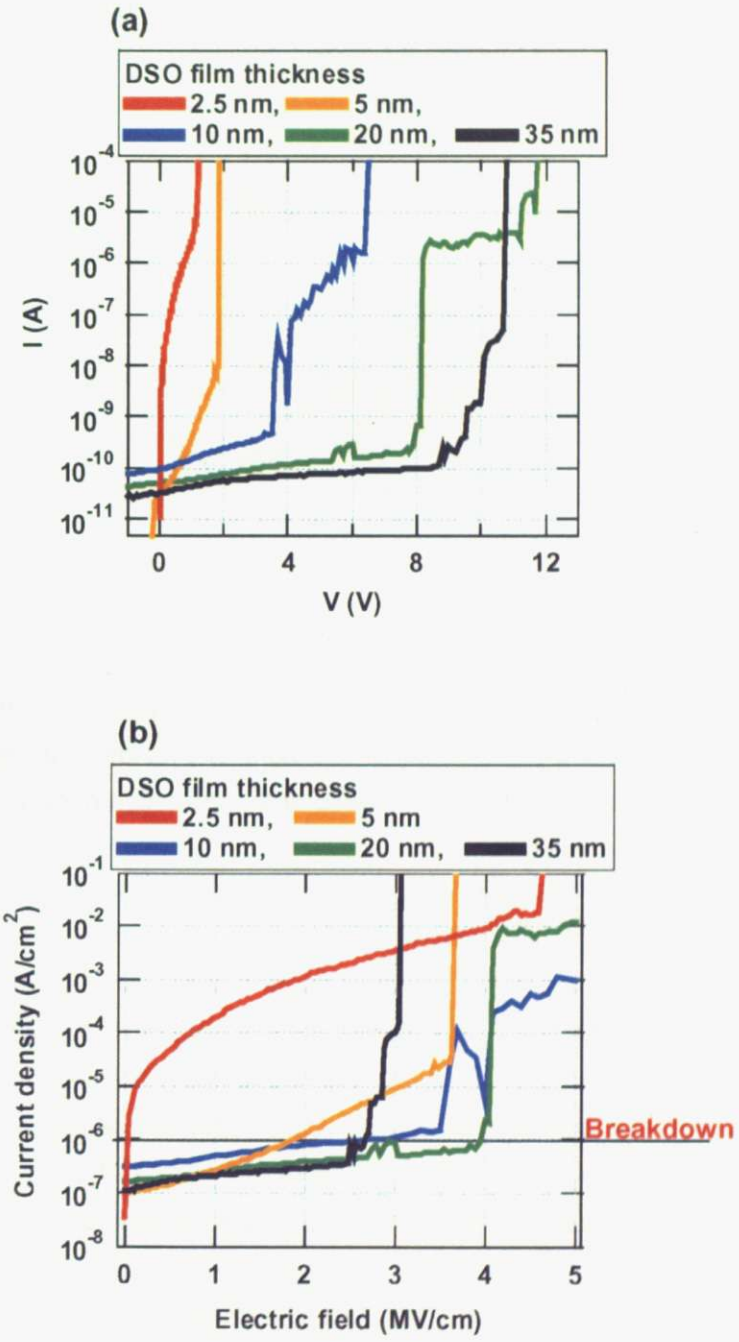


Fig.5.2. Breakdown measurement, (a) current plotted as a function of electric field and (b) current density plotted as a function of applied voltage. Breakdown was defined as current exceeding 1 $\mu A/cm^2$.

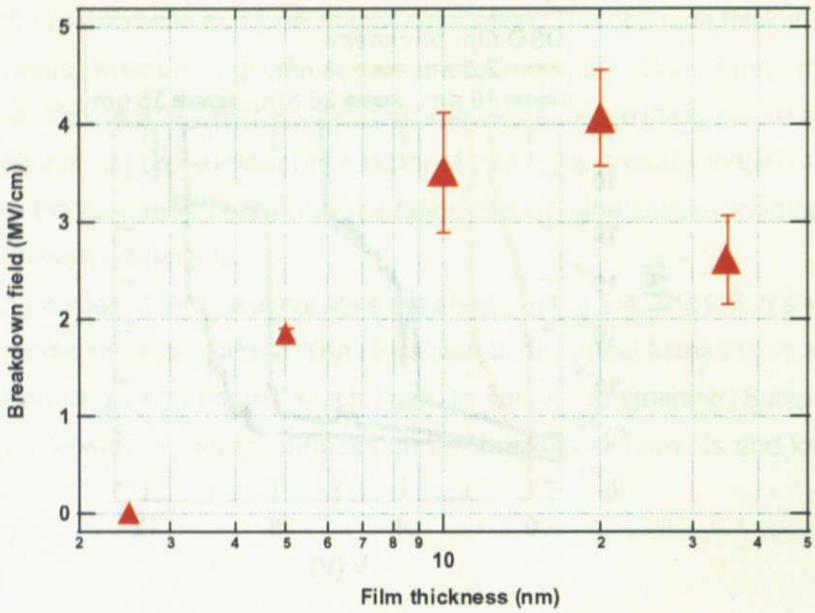


Figure 5.3. Breakdown field as a function of film thickness. Below 5 nm tunneling current became dominant and at over 30 nm breakdown strength was reduced because of the formation of grain structure due to strain relaxation.

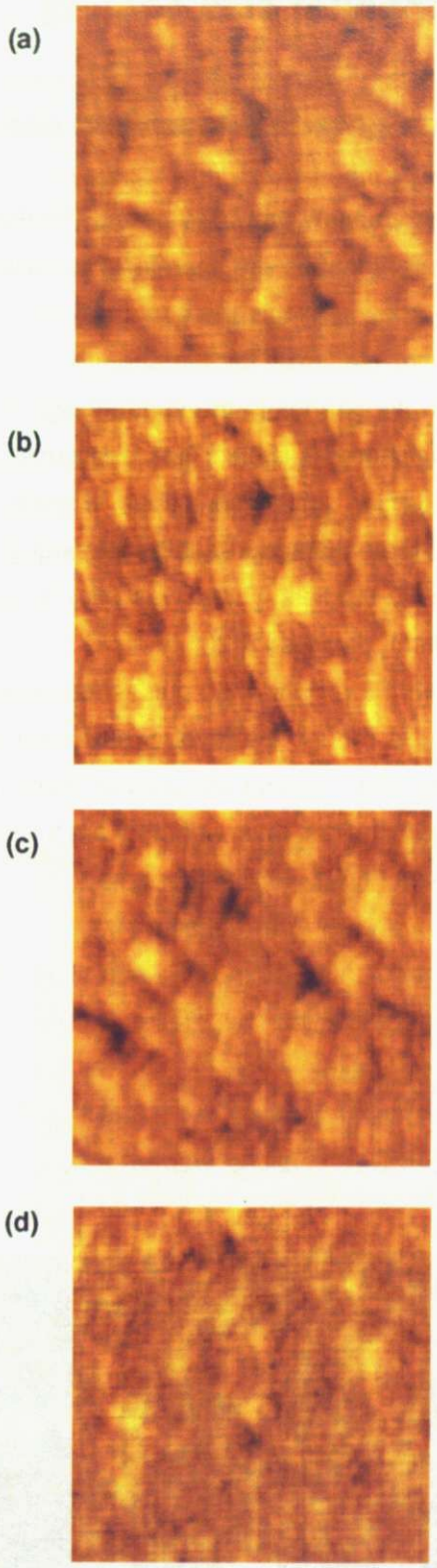


Figure.5.4. 2x2 μm^2 topographies of (a) 2.5 nm, (b) 5 nm, (c) 10 nm, and (d) 20 nm-thick $DyScO_3$ films grown on $SrTiO_3$. Surface roughening due to grains starts to appear in (d) and thicker films.

5.3 The effects of channel size scaling

5.3.1 $CaHfO_3$ amorphous gate insulator and sample preparation

The channel size scaling experiments were done before the $DyScO_3$ film growth optimization study was complete. These experiments were therefore done with $CaHfO_3$ since the optimal growth conditions were already known for this material from previous work. Since the main aim was to see the effect of particles ejected from the target on the FET properties and also see if the reduction of the number of grain boundaries in the channel region would reduce carrier trapping and scattering, $CaHfO_3$ was considered sufficient and applicable to any gate insulator material grown by the same technique under similar conditions. Because FETs with amorphous gate insulators are much easier to fabricate than good-quality epitaxial gate insulators, amorphous films were used for the particle density studies. There was also a large volume of reference data available for the amorphous $CaHfO_3$ devices [1][2].

$CaHfO_3$ was grown at a growth rate of about 60 pulses/monolayer of film growth (~0.7 J/cm^2). The low growth rate was known to reduce the level of structural damage created in the $SrTiO_3$ substrate at the channel interface. The oxygen pressure was fixed at 1 mTorr. The transistors used the double layer gate insulator, with the first layer about 25 nm thick and the second layer about 35 nm thick. The source and drain electrodes were patterned by photolithography and etched into the $SrTiO_3$ substrate by argon ion milling to form metallic oxygen-deficient electrode regions in the substrate. The electrode pits were about 50 nm deep and filled with thermally evaporated SiO_x. Finally, after second insulator deposition by PLD, Al gate electrodes were formed by photolithography and thermal evaporation.

A photograph of a sample containing an array of FETs with different channel sizes is shown in Fig.5.5. The channel length/width (L/W) values were 10/50, 20/100, 40/200, and 100/500 μm (L/W=1/5).

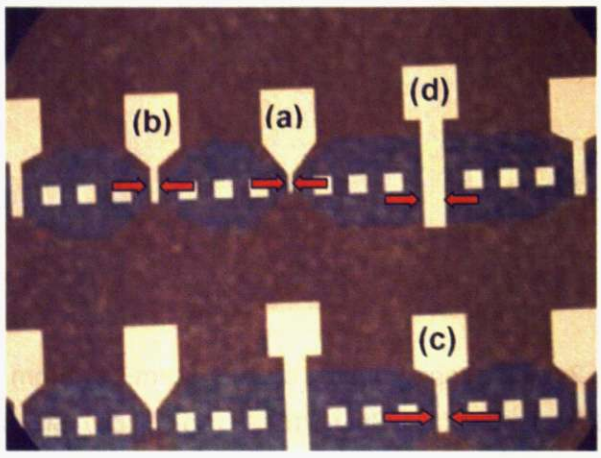


Figure.5.5. Photograph of a device array. Channel sizes are (length x width) (a) 10x50 μm^2 , (b) 20x100 μm^2, (c) 40x200 μm^2, and (d) 100x500 μm^2.

5.3.2 AFM topography of the channels

Topographic AFM images were measured after depositing the first insulator layer. Some particles with a height on the order of a few tens of nanometers can be seen on the sample surface (Fig.5.6). These are likely to be particles that have been ejected from the ablation target. The particle ejecetion was observed directly by observing the ablation plume with a CCD camera that was synchronized with the laser firing while ablating a $CaHfO_3$ target. The flight tracks of the hot ejected particles can be seen in Fig.5.7. By adjusting the camera shutter timing it was possible to image the particles without the very bright plume, as shown in Fig. 5.7 (b). If such particles stick to the film surface, they would result in an inhomogeneous electric field and degradation of breakdown strength. As can be seen in Fig. 5-6, there are fairly large clean spaces between the particles, which means that there is a large probability of obtaining particle-free channels, if the devices are scaled to about 10 μm feature size, as illustrated in Fig. 5-8.

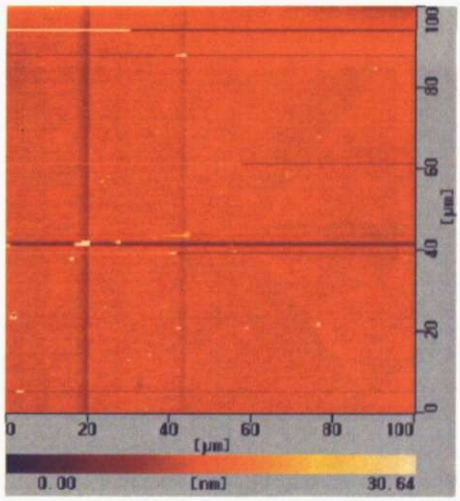


Figure 5.6. 100x100 μm^2 AFM topography after the first insulator layer deposition.

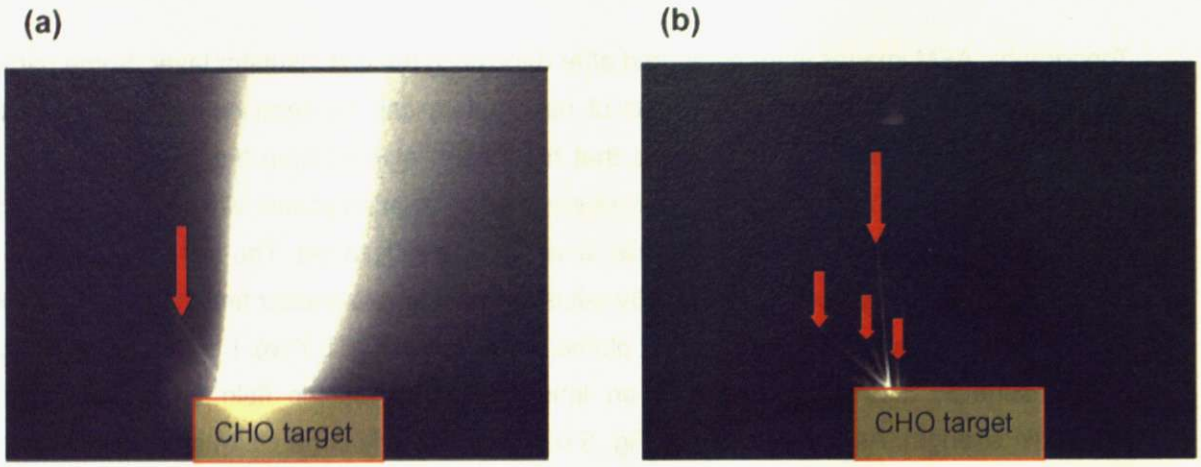


Figure 5.7. Ablation plume images taken with a synchronized CCD camera during the evaporation of a $CaHfO_3$ target by a laser at 5Hz, 0.8 J/cm^2. (a) The plume image and (b) an image taken immediately after the plume has disappeared. Particles frying can be clearly seen in (b).

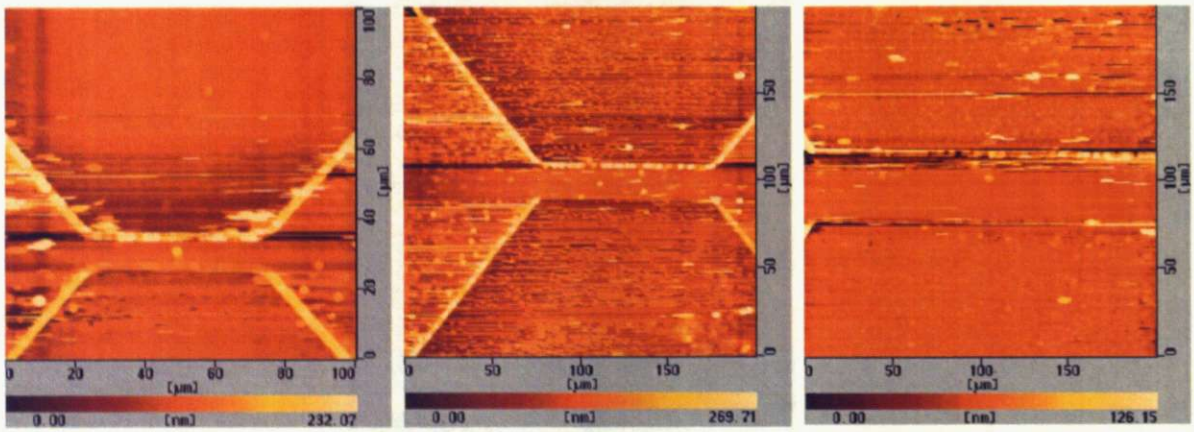


Figure 5.8. AFM topography of the channel region.
The number of particles in the channel region can be reduced by decreasing the channel size.

5.3.3 Performance of scaled FETs

The switching performance of the transistors was measured with a Keithley 4200 semiconductor characterization system. In typical samples, the channel resistance without gate bias was on the order of 2 GΩ (channel width 10 μm, length 50 μm). This value is high enough to see enhancement-type switching and means that oxygen vacancies could be filled by post-annealing the devices in air. The drain-source current I_{DS} is plotted as a function of the drain-source bias V_{DS} for various gate voltages V_{GS} in Fig.5.9. The channel current and the gate leak current are shown as a function of gate bias for three drain bias values (V_{DS} = 0.5, 1.0, 1.5 V) in Fig5.10 (a). Typically the on-off ratio was about 10^5 in these samples at room temperature. Field effect mobility was estimated from

$$\mu_{FE} = \frac{L}{W \times V_{DS} \times C_0} \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}=\text{const.}}, \quad (5\text{-}1)$$

where C_0 is the sheet capacitance of the gate insulator, given by

$$C_0 = \frac{\varepsilon_i \varepsilon_0}{t}, \quad (5\text{-}2)$$

where ε_i is the permittivity of the gate insulator, ε_0 is the permittivity of free space. The relative dielectric constant of $CaHfO_3$, ε_{CHO} was assumed to be 14, based on earlier measurements. [3]

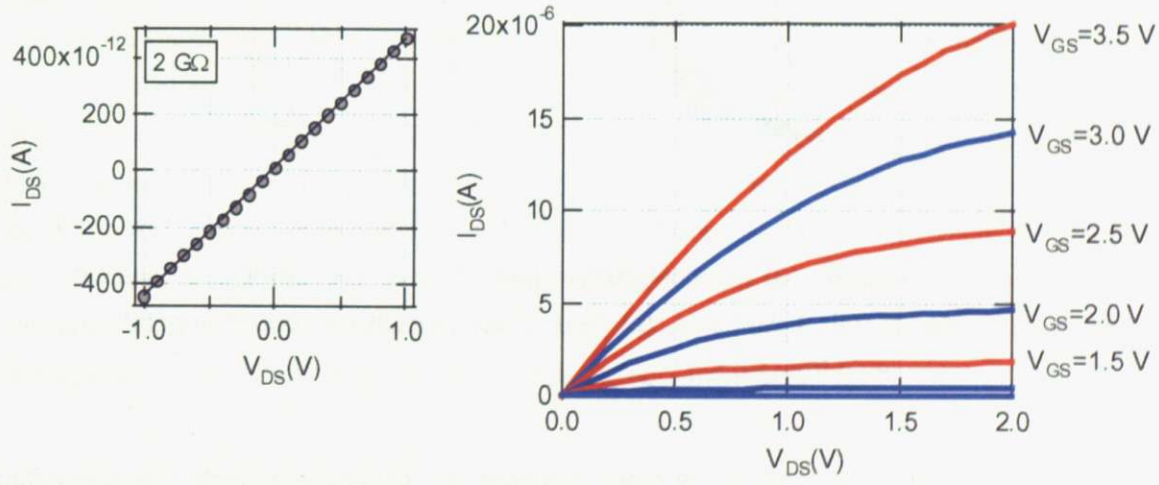


Fig. 5.9. (a) Channel current without gate bias.
(b) I_{DS}-V_{DS} at room temperature for various gate bias values.

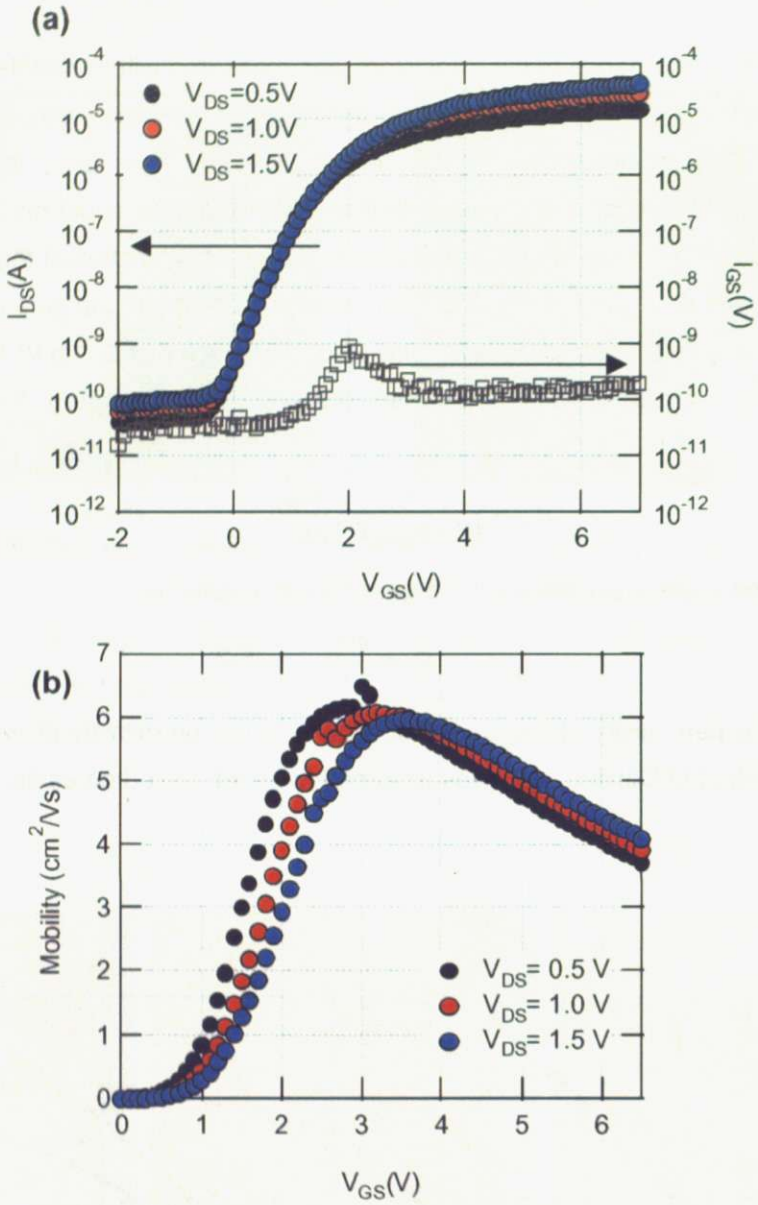


Figure 5.10. (a) Channel current plotted as a function of gate bias for V_{DS} = 0.5, 1.0, 1.5 V. (b) field effect mobility at room temperature, calculated from Eq.5-1.

The field effect mobility of the FET at room temperature is plotted as a function of gate voltage in Fig 5.10 (b). The field effect mobility reached a maximum value of about 6 cm^2/Vs, which is close to the expected Hall mobility at 300 K.

Identical measurements were done for all devices with different channel sizes. Additionally, the breakdown strength and gate leak current-voltage characteristics were measured, as shown in Fig. 5.11. Devices with smaller channels tended to have higher breakdown strength.

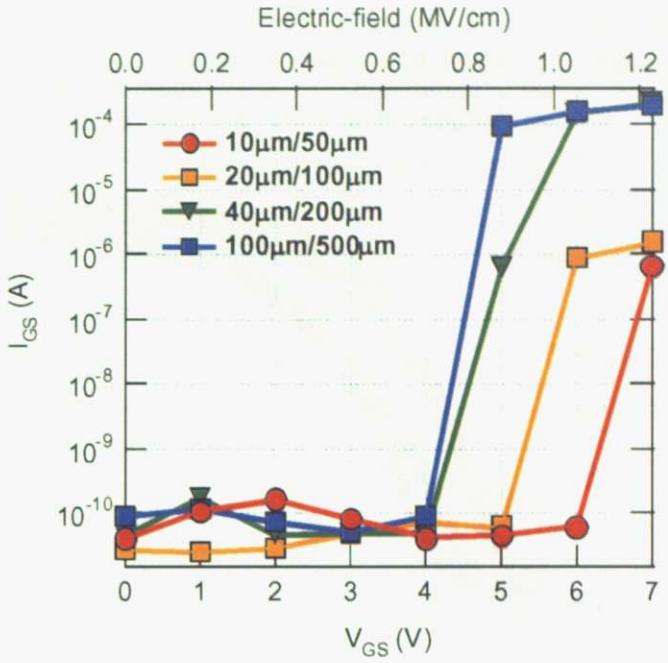
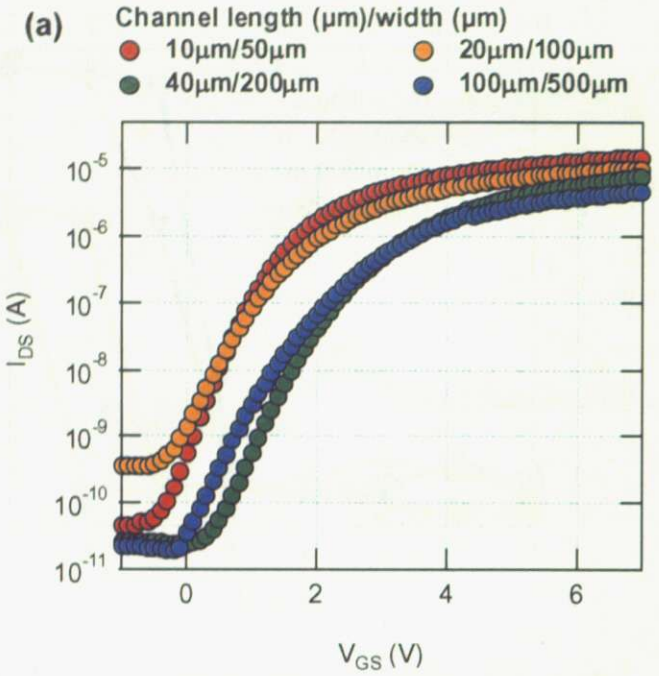


Figure 5.11.Smaller devices typically showed higher breakdown strength.

The switching characteristics of the scaled transistors are shown in Fig. 5.12. These measurements were done at a drain bias of V_{DS}=0.5 V. Some devices had slightly higher off-state conductivity, as the 20/100 device in Fig.12 (a). This indicates the residual carriers existed in the vicinity of the interface between $CaHfO_3$ and the $SrTiO_3$ substrate. Most of the devices showed an on-off ratio of over 10^5. Field effect mobility for all channel sizes is shown in Fig. 5.12 (b). The mobility plots clearly show that smaller devices had considerably better performance than larger devices, at least at room temperature. The maximum carrier mobility in the smallest FETs was about 6 cm^2/Vs at room temperature. By decreasing the scale of channel region, the transistor action improved. Since the main parameter that changed was the homogeneity of the electric field in the channel, it appears that the degraded performance of large devices is mostly due to an inhomogeneous gate field or the presence of particle contamination.



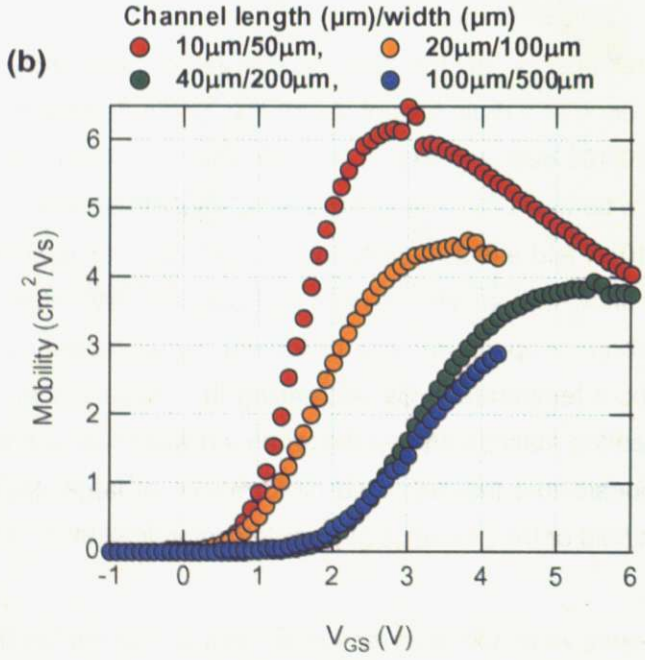


Figure 5.12. (a) I_{DS}-V_{GS} at room temperature for each device
(b) Field effect mobility at room temperature for each device size as a function of gate bias.

The field-effect mobility of the FETs was measured at low temperature as well. This measurement is useful for proving that the field-induced carriers do indeed dope the bulk $SrTiO_3$ substrate crystal. Since the carrier mobility in $SrTiO_3$ is known to increase rapidly at lower temperature, if the field-effect mobility of the FETs follows the known bulk performance, it is safe to conclude that the surface layer of the $SrTiO_3$ crystal was successfully doped with electrons in the FET. The Hall mobility in $SrTiO_3$ is about 6 cm_2/Vs at 300 K, but increases to over 10^4 cm^2/Vs at 4 K [4]. The performance of the largest device (L/W = 100/500) was compared with the smallest device (10/50). Fig. 5.13 shows the temperature dependence of the I_{DS}-V_{GS} curves from 300 to 50 K for a 10 μm /50 μm device. Threshold voltage shift was seen at temperatures below 150 K. This kind of shift has been reported in other oxide FETs [5] and organic FETs [6].

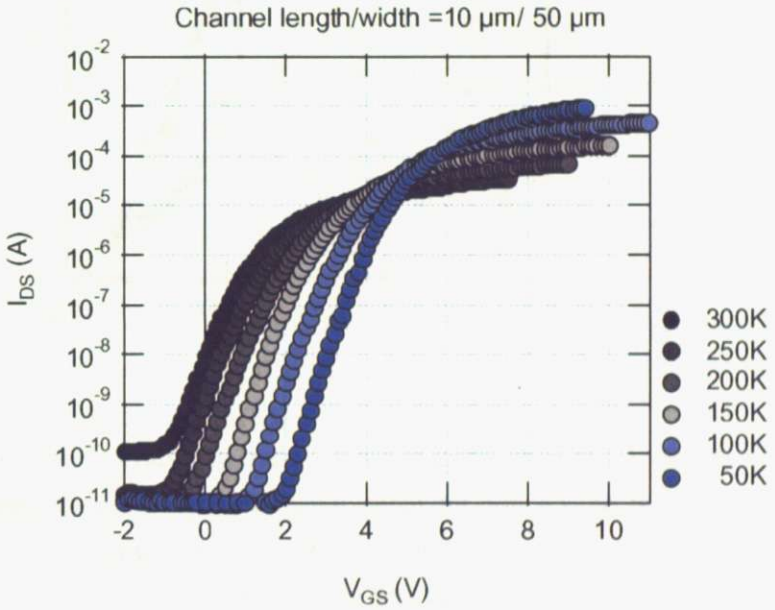


Figure 5.13. The temperature dependence of I_{DS}-V_{GS}
Threshold voltage shifted to higher gate bias with decreasing temperature.

Field-effect mobilities for the largest and smallest devices are compared with the published bulk Hall mobility of $SrTiO_3$ in Fig. 5.14. Red data points correspond to the smallest channel device (L/W=10/50) and closely follow the curve of bulk Hall mobility, showing that device scaling is effective in extracting true material properties from an oxide FET device.

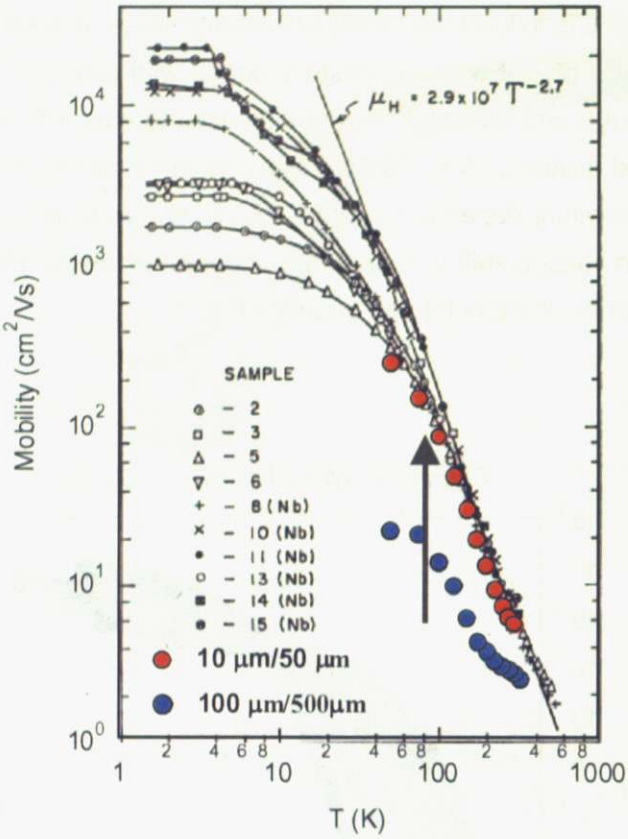


Figure 5.14. Field effect mobility plotted as a function of temperature. Largest device and smallest device showed different performance. Smallest device tended to show better performance. Background data shows Hall mobility [4].

5.4 Conclusions

5.4.1 Material optimization

The film thickness of epitaxial DSO gate insulator was optimized for maximum breakdown strength. It was shown that tunneling current increases for film thicknesses of 5 nm and less while the breakdown field drops at film thicknesses above 20 nm due to the formation of grains in the film. When FETs with epitaxial DSO gate insulator are fabricated, the optimal thickness was found to be between 10 and 20 nm.

5.4.2 Scaled FETs

Devices were fabricated by changing the channel size while maintaining the same channel width/length ratio of 5. Amorphous $CaHfO_3$ insulator films were used in these experiments, but the conclusions should apply to all similar insulators. The effects of device scaling were studies. At room temperature, FETs with the smallest channel showed the best performances, including highest breakdown strength and highest field effect mobility, close to 6 cm^2/Vs at room temperature. At low temperature, all devices showed a threshold voltage shifts with decreasing temperature. This sift is presumably related to trapping in the insulator. Again, the smallest device showed the highest field-effect mobility, reaching about 230 cm^2/Vs at 50K. This value was near the expected Hall mobility reported for $SrTiO_3$ [4].

These improvements were attributed to a decreasing particle density in the channel region. In conclusion, smaller channel would be useful for fabrication and characterization of field effect transistors based on oxide thin films.

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Chapter6. Conclusions

In order to improve the transistor performance, I focused on the scaling of the channel size and the thickness of gate insulator and the optimization of epitaxial $DyScO_3$ thin film growth conditions.

In Chapter 4, I described the characterization of epitaxial $DyScO_3$ thin films. First I checked the crystallinity by using XRD and SEM-EDS. Samples were fabricated by changing the film growth parameters including laser fluence and oxygen pressure. Epitaxial $DyScO_3$ thin films were fabricated at 1, 10 and 100 mTorr while the laser fluence and film growth temperature were fixed at 0.55 J/cm^2 and 700°C, respectively. It was found that samples fabricated at higher oxygen partial pressure showed large stoichiometry errors. Deviation of the cation ratio from the ideal value tended to increase strain, strengthen the grain structure and reduce breakdown strength. Laser fluence was also found to affect film quality, but to a much lesser degree than the oxygen partial pressure. The conclusion from the growth experiments is that the insulator film growth parameters have to be tuned very precisely in order to obtain films with the best breakdown characteristics. The main parameter that needs to be monitored is the cation ratio.

In Chapter 5, I discussed the scaling effect of the channel dimensions and the thickness of the gate insulator film. First I checked the effect of scaling by fabricating and characterizing the performance of field effect transistors that were based on amorphous $CaHfO_3$ gate insulator layers. With reducing channel size, the FET performance improved. Field-effect mobility of the carriers reached about 6 cm^2/Vs at room temperature and approximately 230 cm^2/Vs at about 50 K was reached. These mobilities are similar to the corresponding values of bulk $SrTiO_3$, obtained from Hall measurements. This improvement resulted from a decrease in the number of particles in the channel region of smaller devices. Particles are unfortunately unavoidable in the PLD process. Macroscopic particles in the channel insulator affect transistors action due to an inhomogeneous electric field and low breakdown strength. Therefore smaller devices are clearly better for field-effect studies. I also optimized the thickness of epitaxial $DyScO_3$ thin films. $DyScO_3$ has a very low lattice mismatch with $SrTiO_3$, promising lower strain in epitaxial films. Films were characterized by electrical breakdown measurement in a thickness range of 2.5 to 35 nm. For thicknesses above 30 nm, grain structure became clearly visible and the step-and-terrace surface morphology was lost as the surface roughness gradually expanded with increasing thickness. The best breakdown performance was found in films that were 10 to 20 nm thick.

Achievements Lists

Poster presentation

- OK.Nishio, T.Sato, K.Shibuya, T.Ohnishi and M.Lippmaa
  " Fabrication of Epitaxial Single Crystal $SrTiO_3$ Field-Effect Transistors"
  13th International Workshop on Oxide Electronics, October 8-11, (2006), Ischia, Italy
- OK.Nishio, T.Sato, K.Shibuya, T.Ohnishi and M.Lippmaa
  " Single Crystal $SrTiO_3$ Field-Effect Transistors"
  The 2nd Indo-Japan Seminar, February 27-March1, (2007) Univ. Tokyo, Japan
- OK.Nishio, T.Abe, T.Ohnishi and M.Lippmaa
  " Scaling of Single Crystal $SrTiO_3$ (100) Field-Effect Transistors"
  14th International Workshop on Oxide Electronics, October 7-10, (2007), Jeju Island, Korea

Oral presentation

- OK.Nishio, T.Sato, K.Shibuya, T.Ohnishi and M.Lippmaa
  " Fabrication of oxide field-effect transistors with reduced channel area"
  The 54th spring meeting of the Japan Society of Applied Physics, 2006, extended abstract vol. 2, p686
- OK.Nishio, T.Abe, T.Ohnishi, T.Yamamoto and M.Lippmaa
  " Fabrication of epitaxial $DyScO_3$ insulator films for $SrTiO_3$ single crystal field effect transistors"
  The 68th autumn meeting of the Japan Society of Applied Physics, 2006, extended abstract vol.2, p632
- OK.Nishio, T.Abe, T.Ohnishi and M.Lippmaa
  "Scaling of Single Crystal $SrTiO_3$ (100) Field Effect Transistors"
  The IMR mini workshop, December 21-22, (2007), Tohoku Univ.

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