Dielectric characterization of $DyScO_3$ gate stacks of oxide field-effect transistors

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Introduction

The gate insulator stack, including the gate-channel interface is the most critical part of an oxide field-effect transistor (FET), since the gate insulator directly determines the maximum field, and thus carrier density can be generated in the channel region of the device. In a top-gate structure, the insulator layer is grown directly on top of the channel material and thus the insulator growth has a large impact on the electronic properties of the transistor channel, notably the density of trap states at the interface, which can cause hysteretic behaviour in the transistor switching characteristics and seriously affects the carrier mobility when the device is in a conducting state.

It has been demonstrated that it is possible to induce metallic conductivity in intrinsic $SrTiO_3$ (STO) by field-effect doping[1]. These devices used $SrTiO_3$ as the channel material and various wide-gap insulators ($CaHfO_3$, $DyScO_3$) as gate dielectrics. However, the devices were found to function well only over 100 K. Below about 100 K, progressively larger hysteresis has been seen in device characteristics in $DyScO_3$ and a gradual shift of the transistor bias voltage. The most likely reason for this type of temperature-dependent threshold shift is charge trapping either in the insulator layer or at any of the electrode or channel interfaces in the device. In order to determine the origin of charge trapping, I have fabricated $DyScO_3$ capacitor structures and determined the dielectric properties, including zero bias frequency dependence of permittivity, capacitance- voltage and current-voltage characteristics and time-dependent stress measurements to determine what kind of charging type, such as mobile ionic charge, oxide trapped charge, fixed oxide charge or interface trapped charge.

Experimental

The capacitors were fabricated on as supplied 0.5 wt% Nb-doped $SrTiO_3$(100) substrates. As the first step, gate insulator layers were grown by pulsed laser deposition at an oxygen pressure of 1 mTorr. A KrF excimer laser (λ=248 nm), operating at 5 Hz was used for ablation. The laser fluence on the surface of the ceramic ablation target was around 0.9 J/cm^2, resulting in a deposition rate of approximately 0.1 Å per pulse on the Nb-$SrTiO_3$ surface. Then, Aluminum was thermally evaporated on the insulator film surface through a stainless steel stencil mask. Aluminum was selected because it has been reported that Ohmic contact can be obtained between aluminum electrodes and wide-gap oxide materials[2]. The whole capacitor fabrication process was done at room temperature. It was therefore not necessary to care about substrate surface reconstruction, Nb-diffusion and strain effects.

The electrical properties of these capacitors were characterized as follows: The initial capacitance –frequency, C-F at zero bias, capacitance-voltage, C-V and leak current-voltage, I-V characteristics were investigated for all capacitors. The capacitors were then kept under large positive bias field to study the effect of field stress on the dielectric properties. Transient capacitances were measured during application of pulsed bias at a field strength of 1 MV/cm for trap 'filling' and relaxation to zero for 'emission'. The capacitors were measured with an Agilent 4284 precision LCR meter at a frequency of 100 kHz for C-V and Keithley 4200 for I-V.

Results and Discussions

A possible interfacial layer contribution to the device capacitance can be separated from the bulk film permittivity by measuring a series of samples with different thicknesses and assuming a two-layer capacitor model, which gives a so-called 'EOT plot'[3]. This model assumes a bulk region of thickness d and permittivity ε_B, and the two interface regions with thickness d_i, which yield two capacitors of a lower permittivity ε_i, as shown in Fig. 1 (a) and (b). Assuming that the interface layers are identical, the resulting reciprocal capacitance of the film is given by next equation and the slope of a 1/C plot versus film thickness yields the bulk permittivity. The zero-thickness intercept represents the interface capacitance.

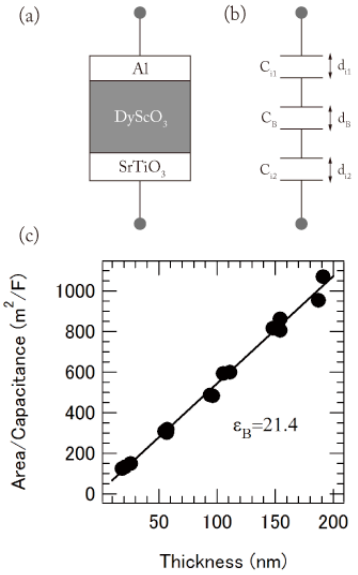

Fig. 1 Schematic diagram of (a) capacitor and (b) two layer capacitor assumption. (c) dependence of reciprocal zero bias capacitance density as a function of thickness.

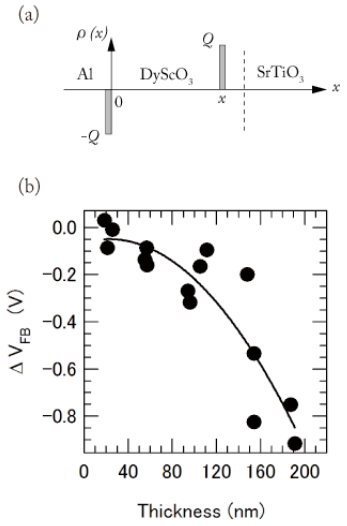

Fig. 2 (a) An illustrating of the effect of a sheet charge of areal density Q within the insulator layer of an MIS capacitor biased ar flat-band condition. (b) Flat-band voltage shift as a function of thickness.

$$\frac{A}{C} = \frac{A}{C_{i1}} + \frac{A}{C_B} + \frac{A}{C_{i2}}$$

$$\approx \frac{2A}{C_i} + \frac{A}{C_B} = \frac{2d_i}{\varepsilon_0 \varepsilon_i} + \frac{d - 2d_i}{\varepsilon_0 \varepsilon_B} \approx \frac{2d_i}{\varepsilon_0 \varepsilon_i} + \frac{d}{\varepsilon_0 \varepsilon_B}$$

As shown in Fig.1 (c), the data points fall on a straight line nicely, confirming the validity of the two-layer model. The slope of the plot gave the bulk dielectric constant of 21.4. This is comparable to the reported value ε = 22[4] and ε = 24, which has been calculated for $DyScO_3$ molecular polarizabilities of Dy_2O_3 and Sc_2O_5[5]. Also, the extrapolation of the linear fit to d = 0 gave an interface layer capacitance of 12.6 nF, from which accompanied interface thickness of 2.8 nm was obtained.

Generally, Oxide Metal-Insulator-Metal (MIM) capacitor follows a semi-quadratic C-V curve shape, called a 'voltage linearity' plot. Assuming that this also applies for $DyScO_3$ case, flat-band voltage could be obtained by differentiating the quadratic fitting results. Fig. 2 (b) shows that flat-band voltage shift as a function of thickness. Theoretically, flat-band shift is expressed as the work function difference of the top (Al) and bottom electrodes. Due to that, it should be about -0.1 eV for these capacitors. However, the observed flat-band voltage shifted downward, suggesting that there are positive charges trapped in the capacitor. Here I only consider fixed oxide charge. In this charge, it exists near or at the interface between Nb-doped $SrTiO_3$ and $DyScO_3$, as shown in Fig. 2 (a). Thus, it can be given by

$$\delta V_g = -\frac{Q}{\varepsilon_{Ins}} x$$

where Q is sheet of trapped charge which is placed at a distance x from the gate electrode, ε_{Ins} is dielectric constant of $DyScO_3$. If the only Q exists in the insulator originating from fixed oxide charge, it should follow a straight line in Fig. 2 (b). However, obviously this is not the case. It indicates that there are other charges in the capacitor, either mobile ionic charge or oxide trapped charge.

The thickness dependence of capacitance relaxation under 1MV/cm C(t) and zero field strength C(t) is shown in Fig. 3. A field step from 1 MV/cm to zero was applied and the capacitor was kept under bias while the capacitance was measured. Capacitance transients were seen for all thicknesses. In thinner film capacitors, the relaxation amplitude showed a large increase. The variation still remained below 1% over a few-minute measurement period. Compared to the results of FET I_{DS} transient, FET has large decrease which was around 50 % variation. This indicates that the interface layer affected transient relaxation. I have calculated the fitting by using transient equation, which is expressed as

$$C(t) = C_0 \left[1 + \alpha_1 \exp\left(-\frac{t}{\tau_1} \right) + \alpha_2 \exp\left(-\frac{t}{\tau_2} \right) \right]$$

where, C_0 is the capacitance at zero time, α_1 and α_2 are the amplitudes of the two exponential components derived from each trapped carrier density, t is the time, and τ_1 and τ_2 are the corresponding time constants.

The slope could be fitted with a double exponential model, suggesting that there are two mechanisms

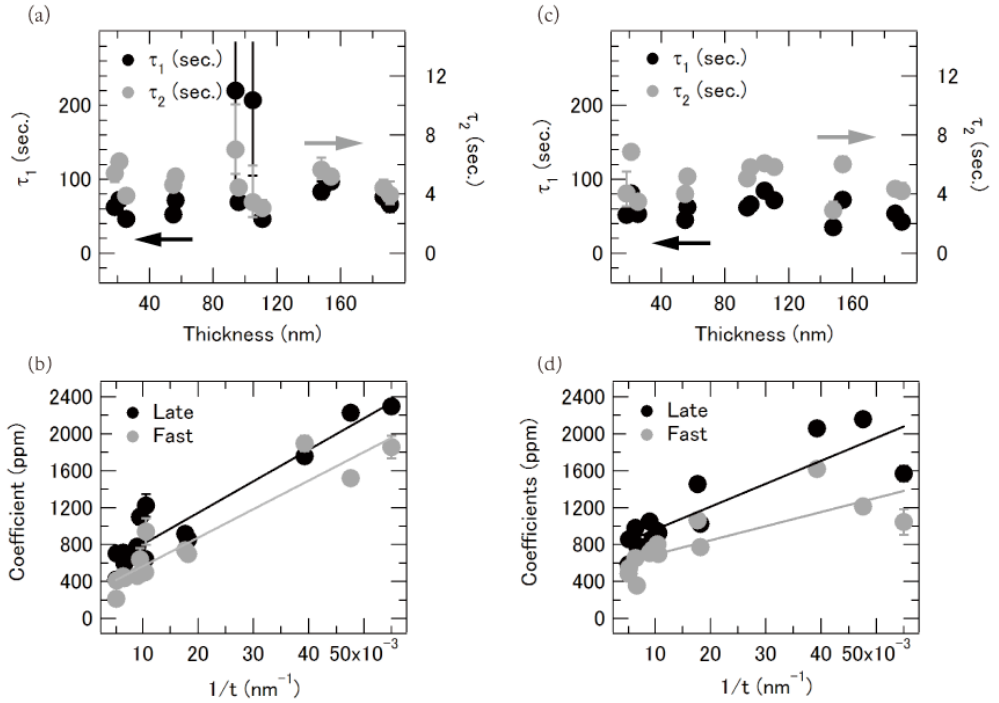

Fig. 3 Double exponential fitting results of (a), (b) charging transient charactris and (c), (d) emission transient characteristics. (a), (c) Time constant as a function of thickness and (b), (d) coefficients as that of inversion thickness.

for the transient relaxation. The fitting results are shown in Fig. 3. In time constant case, both capture and emission mechanisms have the same values with a fast 6-second time constant and a slow 80-second process. Usually at room temperature, the time constant is given by

$$\tau \propto \frac{1}{\sigma}$$

where σ is capture cross section. Consider this equation, the capture cross section of filling sequences has the same as that of emission sequences since there are almost same time constant in all thickness. These charge are positively charged as I mentioned in Fig 2 (b), thus it suggest that these mechanisms occurs at the same capture cross section, *'Coulomb attractive traps'* which has at least 10^{-14} cm^2 trapped density. In coefficient case, we could see the amount of charge. As we could see, thinner capacitor have large amount of charge and this amount of charge increase linearity at thinner capacitors, strongly suggested that these charges are near or at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$, as I expressed in Fig. 2 (a). Since both mechanisms of charging are located around the interface, I could determine that fast time constant mechanisms connected fixed oxide charge, while the slow time is related to mobile ionic charge. It could be said that mobile ionic charge was close to the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ since positively charged mobile ions could drift when applying positive bias to the top electrode. This changes the charge balance at the $SrTiO_3$ interface, causing surface electron current to flow among n^+ diffusion regions in a $SrTiO_3$. We could also think this trap center is not a deep level but instead a shallow level since the time constant of capture and that of emission is almost the same, and both of charges also have similar values.

Conclusions

Based on a two-layer model, the presence of an interface layer was confirmed and the thickness was determined to be at most 2.8 nm. The dielectric constant of bulk $DyScO_3$ was 21.4 according to the same two-layer model and the assumption that the 'the voltage linearity' plot is approximately quadratic. In the field-effect section, oxide fixed charge near or at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ and mobile ionic charge in the $DyScO_3$ were investigated. In transient measurements, this fixed oxide charge had a relatively fast time constant of 6 seconds, while mobile ionic charge had a much slower response at about 80 seconds. Both trapped centers had at least 10^{-14} cm^2 capture cross section, and were assumed to be *'Coulomb attractive traps'*. The trap level appears to be very shallow in $DyScO_3$.

[1] K. Shibuya *et al.*, Appl. Phys. Lett., **88**(2006)212116
[2] C.H. Ahn *et al.*, Rev. Mod. Phys., **78**(2006)1185
[3] P. Ehrhart, R. Thomas, JAP, **99**(2006)114108
[4] R. Thomas *et al.*, J. SSC., **05**(2008)014
[5] R.D Shannon, Acta Crystallogr. **A32**(1976)751