MASTER THESIS

Dielectric characterization of DyScO$_3$ gate stacks of oxide field-effect transistors

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To my parents and grand-s

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*Keywords: **Oxide electronics, Dielectric properties, Trapped charge***

Introduction

The gate insulator stack, including the gate-channel interface is the most critical part of an oxide field-effect transistor (FET), since the gate insulator directly determines the maximum field, and thus carrier density can be generated in the channel region of the device. In a top-gate structure, the insulator layer is grown directly on top of the channel material and thus the insulator growth has a large impact on the electronic properties of the transistor channel, notably the density of trap states at the interface, which can cause hysteretic behaviour in the transistor switching characteristics and seriously affects the carrier mobility when the device is in a conducting state.

It has been demonstrated that it is possible to induce metallic conductivity in intrinsic SrTiO₃ (STO) by field-effect doping[1]. These devices used SrTiO₃ as the channel material and various wide-gap insulators (CaHfO₃, DyScO₃) as gate dielectrics. However, the devices were found to function well only over 100 K. Below about 100 K, progressively larger hysteresis has been seen in device characteristics in DyScO₃ and a gradual shift of the transistor bias voltage. The most likely reason for this type of temperature-dependent threshold shift is charge trapping either in the insulator layer or at any of the electrode or channel interfaces in the device. In order to determine the origin of charge trapping, I have fabricated DyScO₃ capacitor structures and determined the dielectric properties, including zero bias frequency dependence of permittivity, capacitance - voltage and current - voltage characteristics and time-dependent stress measurements to determine what kind of charging type, such as mobile ionic charge, oxide trapped charge, fixed oxide charge or interface trapped charge.

Experimental

The capacitors were fabricated on as supplied 0.5 wt% Nb-doped SrTiO₃(100) substrates. As the first step, gate insulator layers were grown by pulsed laser deposition at an oxygen pressure of 1 mTorr. A KrF excimer laser (λ=248 nm), operating at 5 Hz was used for ablation. The laser fluence on the surface of the ceramic ablation target was around 0.9 J/cm², resulting in a deposition rate of approximately 0.1 Å per pulse on the Nb-SrTiO₃ surface. Then, Aluminum was thermally evaporated on the insulator film surface through a stainless steel stencil mask. Aluminum was selected because it has been reported that Ohmic contact can be obtained between aluminum electrodes and wide-gap oxide materials[2]. The whole capacitor fabrication process was done at room temperature. It was therefore not necessary to care about substrate surface reconstruction, Nb-diffusion and strain effects.

The electrical properties of these capacitors were characterized as follows: The initial capacitance –frequency, C-F at zero bias, capacitance-voltage, C-V and leak current-voltage, I-V characteristics were investigated for all capacitors. The capacitors were then kept under large positive bias field to study the effect of field stress on the dielectric properties. Transient capacitances were measured during application of pulsed bias at a field strength of 1 MV/cm for trap 'filling' and relaxation to zero for 'emission'. The capacitors were measured with an Agilent 4284 precision LCR meter at a frequency of 100 kHz for C-V and Keithley 4200 for I-V.

Results and Discussions

A possible interfacial layer contribution to the device capacitance can be separated from the bulk film permittivity by measuring a series of samples with different thicknesses and assuming a two-layer capacitor model, which gives a so-called 'EOT plot'[3]. This model assumes a bulk region of thickness d and permittivity ε_B, and the two interface regions with thickness d_i, which yield two capacitors of a lower permittivity ε_i, as shown in Fig. 1 (a) and (b). Assuming that the interface layers are identical, the resulting reciprocal capacitance of the film is given by next equation and the slope of a *1/C* plot versus film thickness yields the bulk permittivity. The zero-thickness intercept represents the interface capacitance.
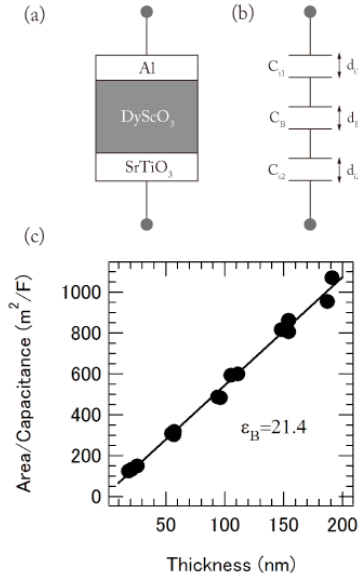
Fig. 1 Schematic diagram of (a) capacitor and (b) two layer capacitor assumption. (c) dependence of reciprocal zero bias capacitance density as a function of thickness.
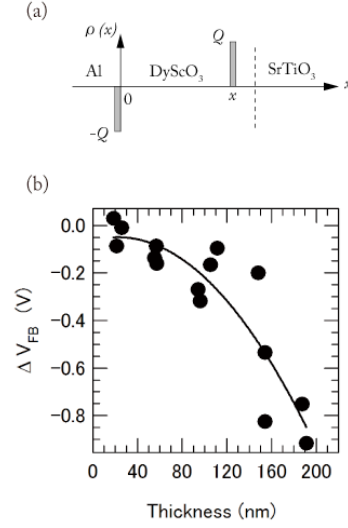

Fig. 2 (a) An illustrating of the effect of a sheet charge of areal density Q within the insulator layer of an MIS capacitor biased at flat-band condition. (b) Flat-band voltage shift as a function of thickness.

$$\frac{A}{C} = \frac{A}{C_{i1}} + \frac{A}{C_B} + \frac{A}{C_{i2}}$$

$$\approx \frac{2A}{C_i} + \frac{A}{C_B} = \frac{2d_i}{\varepsilon_0 \varepsilon_i} + \frac{d - 2d_i}{\varepsilon_0 \varepsilon_B} \approx \frac{2d_i}{\varepsilon_0 \varepsilon_i} + \frac{d}{\varepsilon_0 \varepsilon_B}.$$

As shown in Fig.1 (c), the data points fall on a straight line nicely, confirming the validity of the two-layer model. The slope of the plot gave the bulk dielectric constant of 21.4. This is comparable to the reported value $\varepsilon = 22$[4] and $\varepsilon = 24$, which has been calculated for DyScO$_3$ molecular polarizabilities of Dy$_2$O$_3$ and Sc$_2$O$_5$[5]. Also, the extrapolation of the linear fit to $d = 0$ gave an interface layer capacitance of 12.6 nF, from which accompanied interface thickness of 2.8 nm was obtained.

Generally, Oxide Metal-Insulator-Metal (MIM) capacitor follows a semi-quadratic C-V curve shape, called a 'voltage linearity' plot. Assuming that this also applies for DyScO$_3$ case, flat-band voltage could be obtained by differentiating the quadratic fitting results. Fig. 2 (b) shows that flat-band voltage shift as a function of thickness. Theoretically, flat-band shift is expressed as the work function difference of the top (Al) and bottom electrodes. Due to that, it should be about -0.1 eV for these capacitors. However, the observed flat-band voltage shifted downward, suggesting that there are positive charges trapped in the capacitor. Here I only consider fixed oxide charge. In this charge, it exists near or at the interface between Nb-doped SrTiO$_3$ and DyScO$_3$, as shown in Fig. 2 (a). Thus, it can be given by

$$\delta V_g = -\frac{Q}{\varepsilon_{Ins}} x,$$

where Q is sheet of trapped charge which is placed at a distance x from the gate electrode, ε_{Ins} is dielectric constant of DyScO$_3$. If the only Q exists in the insulator originating from fixed oxide charge, it should follow a straight line in Fig. 2 (b). However, obviously this is not the case. It indicates that there are other charges in the capacitor, either mobile ionic charge or oxide trapped charge.

The thickness dependence of capacitance relaxation under 1MV/cm $C(t)$ and zero field strength $C(t)$ is shown in Fig. 3. A field step from 1 MV/cm to zero was applied and the capacitor was kept under bias while the capacitance was measured. Capacitance transients were seen for all thicknesses. In thinner film capacitors, the relaxation amplitude showed a large increase. The variation still remained below 1% over a few-minute measurement period. Compared to the results of FET I_{DS} transient, FET has large decrease which was around 50 % variation. This indicates that the interface layer affected transient relaxation. I have calculated the fitting by using transient equation, which is expressed as

$$C(t) = C_0 \left[1 + \alpha_1 \exp\left(-\frac{t}{\tau_1}\right) + \alpha_2 \exp\left(-\frac{t}{\tau_2}\right) \right],$$

where, C_0 is the capacitance at zero time, α_1 and α_2 are the amplitudes of the two exponential components derived from each trapped carrier density, t is the time, and τ_1 and τ_2 are the corresponding time constants.

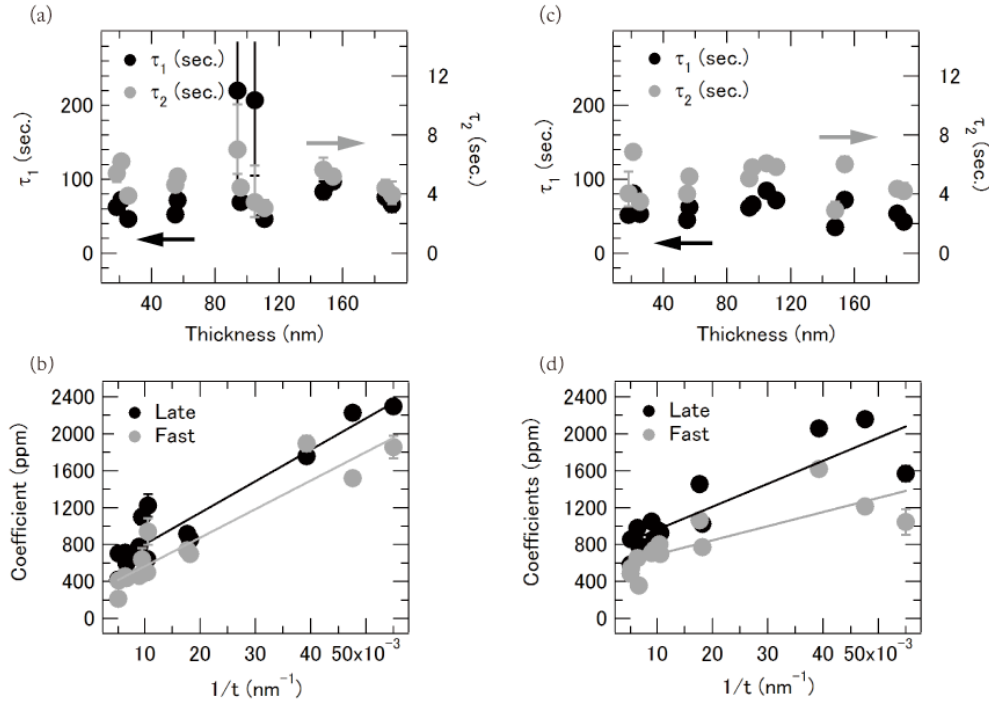The slope could be fitted with a double exponential model, suggesting that there are two mechanisms

Fig. 3 Double exponential fitting results of (a), (b) charging transient charactris and (c), (d) emission transient characteristics. (a), (c) Time constant as a function of thickness and (b), (d) coefficents as that of inversion thickness.

for the transient relaxation. The fitting results are shown in Fig. 3. In time constant case, both capture and emission mechanisms have the same values with a fast 6-second time constant and a slow 80-second process. Usually at room temperature, the time constant is given by

$$\tau \propto \frac{1}{\sigma},$$

where σ is capture cross section. Consider this equation, the capture cross section of filling sequences has the same as that of emission sequences since there are almost same time constant in all thickness. These charge are positively charged as I mentioned in Fig 2 (b), thus it suggest that these mechanisms occurs at the same capture cross section, *'Coulomb attractive traps'* which has at least 10^{-14} cm^2 trapped density. In coefficient case, we could see the amount of charge. As we could see, thinner capacitor have large amount of charge and this amount of charge increase linearity at thinner capacitors, strongly suggested that these charges are near or at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$, as I expressed in Fig. 2 (a). Since both mechanisms of charging are located around the interface, I could determine that fast time constant mechanisms connected fixed oxide charge, while the slow time is related to mobile ionic charge. It could be said that mobile ionic charge was close to the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ since positively charged mobile ions could drift when applying positive bias to the top electrode. This changes the charge balance at the $SrTiO_3$ interface, causing surface electron current

to flow among n^+ diffusion regions in a $SrTiO_3$. We could also think this trap center is not a deep level but instead a shallow level since the time constant of capture and that of emission is almost the same, and both of charges also have similar values.

Conclusions

Based on a two-layer model, the presence of an interface layer was confirmed and the thickness was determined to be at most 2.8 nm. The dielectric constant of bulk $DyScO_3$ was 21.4 according to the same two-layer model and the assumption that the 'the voltage linearity' plot is approximately quadratic. In the field-effect section, oxide fixed charge near or at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ and mobile ionic charge in the $DyScO_3$ were investigated. In transient measurements, this fixed oxide charge had a relatively fast time constant of 6 seconds, while mobile ionic charge had a much slower response at about 80 seconds. Both trapped centers had at least 10^{-14} cm^2 capture cross section, and were assumed to be *'Coulomb attractive traps'*. The trap level appears to be very shallow in $DyScO_3$.

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Contents

Chapter 1
General Introduction

The innovations in electronics that occurred in the 20th century have changed our lives. Now that electronics has become an indispensable part of our existence. The transistor - a key device in present-day electronics, is the foundation of practically all electronic appliances that we have come to depend on. Nowadays LSI (Large Scale Integration) circuits that combine more than 10^9 transistors in a single chip are paving the way for dramatic advances in manufacturing industry, biology, medical technology, and many scientific fields. This dramatic advance is based on Silicon because practically all modern LSI products use the complementary metal-oxide-semiconductor (CMOS) technology. In this field, Silicon is the driving force. The spectacular success of Silicon technology is illustrated by the Moor's law (scaling law). Since the continuous scaling of Si-CMOS devices will eventually reach fundamental limits, various other approaches to device scaling have been tried. In this regard, oxides are among the most interesting materials. Devices based on transition metal oxide heterostructures, especially perovskite type oxides, are very promising for next generation electronics because of the variety of functions that those materials make accessible. Obvious extensions to silicon technology make use of their relatively wide energy gaps that can be combined with large permittivity, the so-called high-k materials. Other functional properties that may find use on device level are superconductivity, ferroelectricity, colossal magnetoresistance[i,ii,iii,iv], etc. In this thesis, I focus on

the characterization of high-permittivity oxide insulators that are used in all-oxide field-effect devices.

1.1 Field effect modulation

Small changes in carrier density can give rise to large changes in materials properties. This is especially true in various oxides, where electronic phase transitions can be driven by carrier density changes. There are a number of approaches that can be used to control the density of carriers in a material. Some techniques, such as chemical doping, are more suited for materials characterization. Chemical doping can cover wide doping ranges and is commonly used to study bulk properties. However, this method also has various problems. Chemical doping always causes changes in the lattice, especially in the vicinity of dopant atoms and also affects the band gap (kinetic energy of electrons) due to a shift of the lattice constant, especially when the concentration of dopant atoms increases. To enable fine tuning of carrier density in a material, electrostatic charging and electrodynamic carrier injection have been used. Although these methods can access only a limited doping range, they also have advantages over chemical doping. Carrier injection by field effect does not change the physical structure of a material such as lattice parameters or lattice composition and ordering as happens with chemical doping[v,vi]. It may therefore be possible to study intrinsic material properties if field effect modulation is used.

A Field-Effect Transistor (FET) is a three-terminal semiconductor device. Since 1960s, FETs based on conventional semiconductors, such as Si, Ge, and GaAs, have been investigated, because such devices can switch current quickly with very low power consumption. At an initial stage of semiconductor device development, Ge was mainly used but Si based FETs are now the most popular devices among all semiconductor components due to various manufacturability advantages. Various different FET designs exist, including the Junction Field-Effect Transistor (JFET), the Metal-Semiconductor Field-Effect Transistor (MESFET), and the Metal-Insulator-Semiconductor (MISFET). In this thesis, I focus on the oxide-based MISFET structure and in particular investigate the Metal-Insulator-Semiconductor (MIS) gate stack structure.

The basic structure of a MISFET is illustrated in Fig. 1.1 (a). It is a three-terminal device and consists of an n-type semiconductor channel. The electrodes attached to the

semiconductor are called "source" and "drain" and the metal contact on the insulator is named "gate" as the scheme shows. The basic device parameters are the channel length L, which is the distance between the source and the drain electrodes; the channel width W; and the insulator thickness d. When no voltage is applied to the gate, as we can see in Fig.1.1 (b), no current flows between the source and the drain electrodes because ideally no carriers exist in the channel. In case a positive gate bias V_{gs} is applied, as shown in Fig.1.1 (c), an accumulation region is formed in the channel and the channel current, I_{DS}, can flow if a small drain voltage, V_{DS}, is applied. The current is proportional to V_{DS} as long as the drain bias remains small compared to V_{GS}. This is called the "linear region". As V_{DS} increases, the channel current saturates. This happens because the potential difference between the gate and the drain becomes small and the accumulation state vanishes near the drain electrode. This is known as the "saturation region". The channel current I_{DS} in the linear and saturation regions are given by Eqs. 1.1 and 1.2, respectively

$$I_{DS}^{lin} = \frac{W}{L} \mu C_i (V_{GS} - V_{TH}) V_{DS} , \qquad (1.1)$$

$$I_{DS}^{sat} = \frac{W}{2L} \mu C_i (V_{GS} - V_{TH})^2 , \qquad (1.2)$$

where μ is the carrier mobility, C_i is the sheet capacitance of the insulator, and V_{TH} is the threshold voltage. As we can see, the carrier mobility is one of the most important parameter used to characterize a transistor[vii].

In addition to being an important part of a transistor, a MIS capacitor is also a very useful device for studying the properties of an interface between a semiconducting oxide material and an insulator. Fig. 1.2 shows schematic band diagrams of MIS capacitors under various biasing conditions. When an ideal MIS capacitor is biased with positive or negative voltages, basically three cases may exist at the semiconductor interface. Let me consider an n-type semiconductor like various oxide materials that are of interest for constructing FETs. When a positive voltage (V>0) is applied to the top electrode, the conduction-band edge E_C bends downward and moves closer to the Fermi level (Fig. 1.2 (b)). For an ideal MIS capacitor, no current flows in the structure, so the Fermi level remains flat in the semiconductor. Since the carrier density depends exponentially on the energy difference (E_C-E_F), this band bending causes and accumulation of majority carriers (electrons) near the semiconductor surface. This is the accumulation case. When a small negative voltage (V<0) is applied, the bands bend upward, and the majority carriers are depleted (Fig. 1.2 (c)). This is the depletion case[viii].

Similar results can be obtained for a p-type semiconductor. The polarity of the voltage, however, should be changed for the p-type semiconductor. Detailed discussion of this type action is not repeated here because the aim of this thesis is not to replicate today's silicon technology but to investigate the electronic properties of oxide heterostructures.

1.2 Transition metal oxides

The devices studied in this work are all based on oxides that have a perovskite structure. This kind of material contains three different atoms with a general formula ABO_3. In a unit cell, the corner position, i.e. the B-site, which occupies the body center position, is occupied by a transition metal, which is 6-fold coordinated with neighboring oxygen atoms. The oxygen lattice thus forms corner sharing oxygen octahedra. The A-site cation is coordinated with twelve nearest-neighbor oxygen ions. Thus, the A-site cation is normally larger than the B-site cation. As shown in Fig. 1.3, along any of the three principal axes, the structure can be viewed as a stack of alternating AO and BO_2 planes. The various and unusual physical properties of oxide materials are derived from the varieties of BO_2 layers which consists of 3d transition metals, such as Ti, V, Cr, Mn, Fe, Co, Ni, and Cu, where d electronic states make the main contribution. The AO layers provide a frame for the lattice and act as charge storage. Variations of the A-site cation can also be used to fine-tune the lattice parameter of the material.

1.3 Oxide heterostructures

Small changes of carrier density in oxide material can lead various phycal properties as I mentioned above. Takahashi *et al.* recently demonstrated switching of superconducting properties for two carrier density states[ix], as shown in Fig.1.4. They fabricated a stack structure consisting of a thin superconducting oxide film and a ferroelectric cover layer. By polarizing the ferroelectric layer with the tip of an atomic force microscope, they succeeded in controlling the local switching of two-dimensional superconductivity. This is just one illustration of the potentially useful electronic properties that transition metal oxides exhibit[x,xi]. However, for high-quality device applications, there are still many challenging issues[xii,xiii]. One of the biggest problems is the difficulty of controlling the electronic properties of oxide heterointerfaces. It goes without saying that we need to find ways of designing and fabricating electronically

clean heterointerfaces for device applications. The silicon FET development passed a similar phase about 40 years ago.

1.4 Physical properties of SrTiO$_3$

SrTiO$_3$ is a uniquely suitable material for oxide electronics development not only as a high dielectric constant (high-k) insulator[xiv] but also as a wide-gap semiconductor with a band gap of approximately 3.2 eV[xv]. Even slight doping by introducing oxygen vacancies can turn the material into a semiconductor, metal or even a superconductor. This is possible, because the Fermi level of intrinsic SrTiO$_3$ is located only about 100 meV below the conduction band bottom. Due to that, it is easy to induce conductivity by cation substitution or the introduction of oxygen vacancies at a very low carrier density, with an insulator-to-metal transition occurring at a carrier density of about 10^{18} cm^{-3} [xvi]. Hall mobilities above 10,000 cm^2/Vs have been observed at low temperatures as shown in Fig. 1.5. The graph shows that Hall mobilities change dramatically as a function of temperature, saturating below 10K.

1.5 Objective of this study

The field-effect device structure, as explained in Section 1.2, is an attractive device for systematic studies of material properties as a function of carrier concentration, since the carrier density in the surface layer of the semiconductor can be modulated by field effect. As I suggested in Section 1.3, the gate insulator stack, including the gate-channel interface is the most critical part of an oxide field-effect transistor (FET), since the gate insulator directly determines the maximum field, and thus the maximum carrier density modulation amplitude that can be generated in the channel region of the device. In a top-gate MIS capacitor structure, the insulator layer is grown directly on top of the channel material and thus the insulator growth has a large impact on the electronic properties of the transistor channel, notably the density of trap states at the interface, which can cause hysteretic behavior in the transistor switching characteristics and seriously affects the carrier mobility when the device is in a conducting state.

It has been demonstrated that it is possible to induce metallic conductivity in intrinsic SrTiO$_3$ by field-effect doping[xvii]. These devices used SrTiO$_3$ as the channel material and various wide-gap insulators (i.e. CaHfO$_3$, DyScO$_3$) as gate dielectrics. However, the

devices were found to function well only at temperatures above 100 K. Below about 100 K, progressively larger hysteresis has been seen in device characteristics of $SrTiO_3$ / $DyScO_3$ FETs, together with a gradual shift of the transistor bias voltage, as shown in Fig. 1.6. The most likely reason for this type of temperature-dependent threshold shift is charge trapping either in the insulator layer or at any of the electrode or channel interfaces in the device. In order to determine the origin of charge trapping, I have fabricated $DyScO_3$ capacitor structures and determined the dielectric properties, including frequency-capacitance characteristics, capacitance-voltage characteristics, current-voltage characteristics and time-dependent stress measurement. What is the origin of charge traps? Is it due to insulator? Or interface? I have detailed investigated insulator and interface by using field effect modulation in $DyScO_3$ capacitors.

1.6 Outline of this thesis

This thesis describes detailed studies of electronic characteristics of oxide heterointerfaces between semiconducting or metallic $SrTiO_3$ single crystals and amorphous $DyScO_3$ wide-gap insulator layers grown by pulsed laser deposition.

The thesis is composed of 5 chapters. Chapter 2 describes the main experimental techniques; Pulsed Laser Deposition, the choice of electrodes and insulators, and the measurement of electrical characteristics. The most important fabrication and characterization techniques are also presented in this chapter. Dielectric characteristics of Al/$DyScO_3$/Nb-doped $SrTiO_3$ capacitors are studied in Chapter 3. In this chapter, I discuss interface and insulator properties based on various capacitance measurements. The main results are derived from frequency- and voltage-dependent capacitance and time-dependent stress measurements. Possible equivalent circuits of the capacitor structures are investigated as well. Conduction mechanisms in oxide capacitors are explored in Chapter 4. Temperature and electric field dependence of capacitors properties are also presented. Chapter 5 is devoted to conclusions and my propositions including all results.
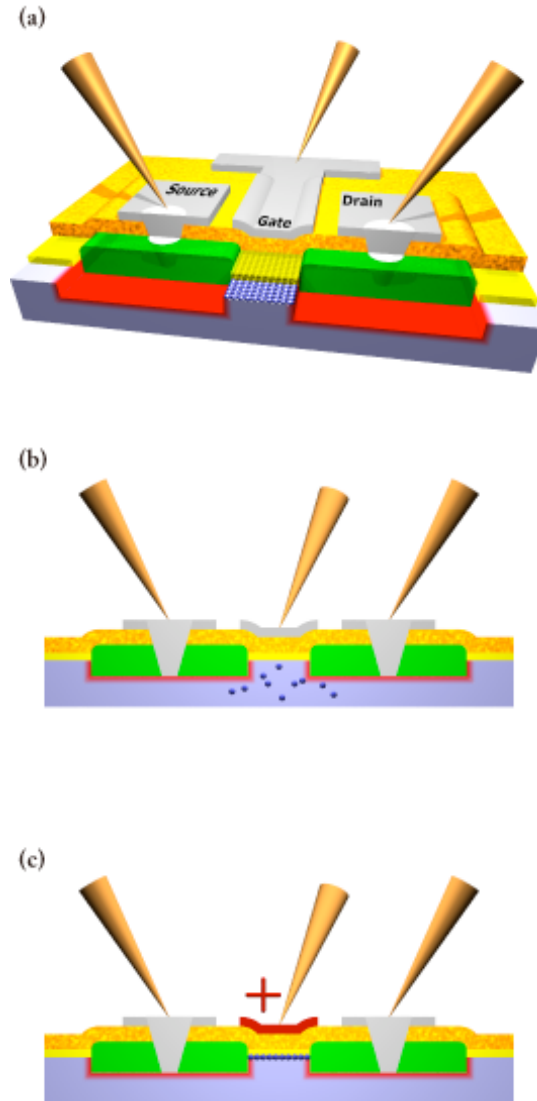
Fig. 1.1 Schematic drawing of (a) a Metal-Insulator-Semiconductor Field-Effect Transistor, (b) zero-bias conditions, and (c) accumulation of carriers in the channel region under positive bias. Red color is Source and Drain which are $SrTiO_{3-\delta}$, yellow is epitaxial $DyScO_3$, dotted yellow is amorphous $DyScO_3$, green is SiO_x, light blue is substrate which is $SrTiO_3$, and Gate is Al, respectively.
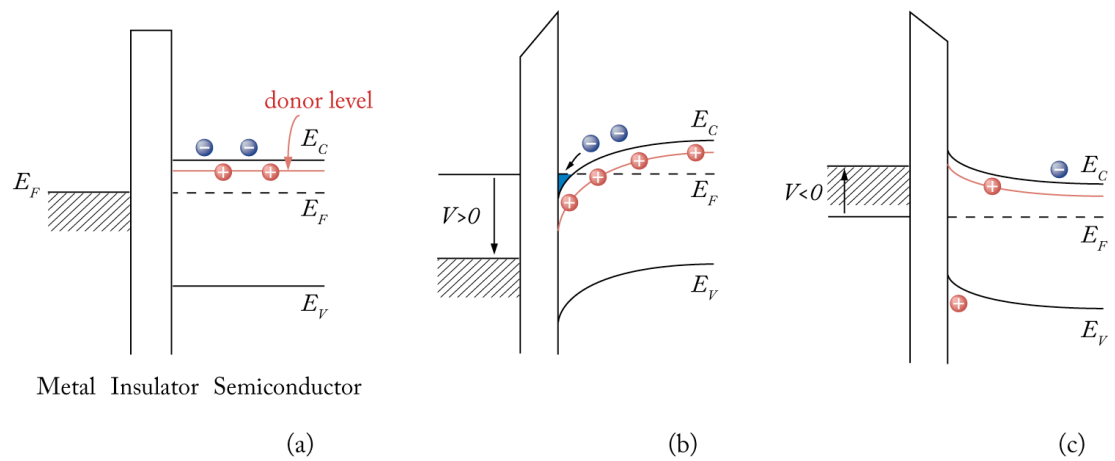
Fig. 1.2 Energy-band diagrams for ideal MIS diodes (a) zero bias, (b) accumulation under positive bias, and (c) depletion under negative bias.
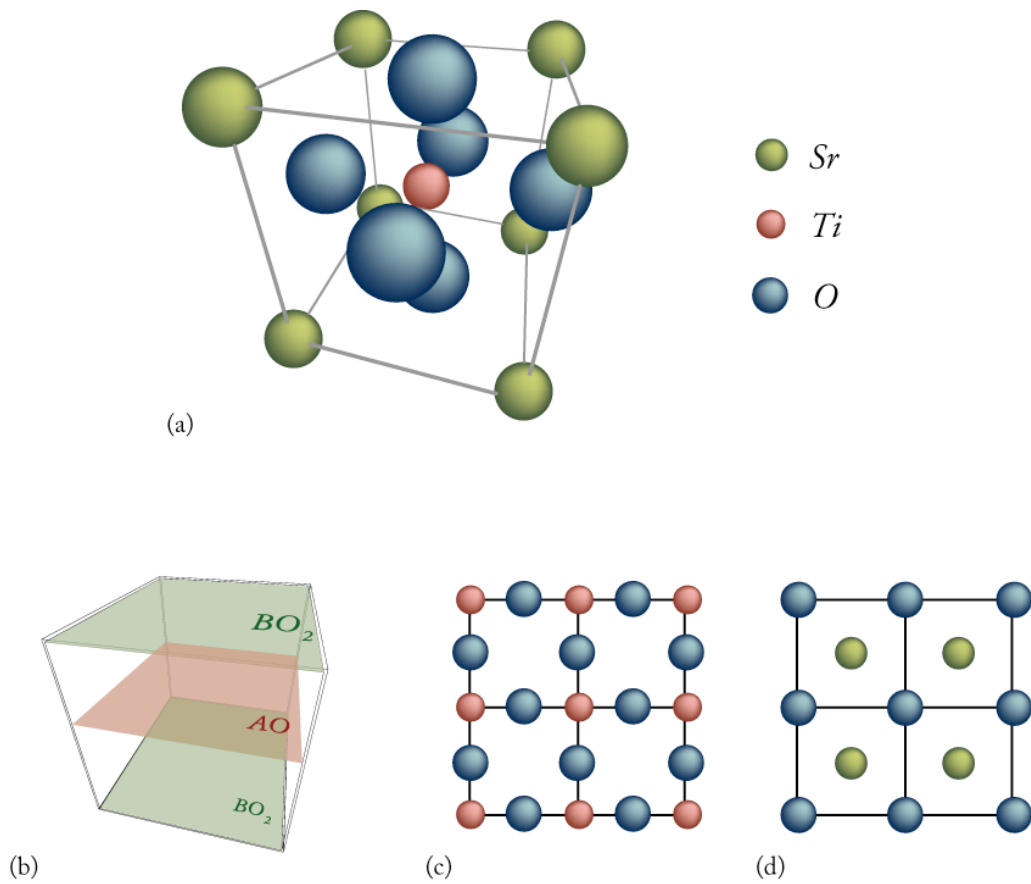
Fig. 1.3 (a) The ABO_3 perovskite crystal structure, using $SrTiO_3$ as an example. In this case, A-site is Strontium and B-site is Titanium. (b) possible terminating planes of the (001) surface, (c)TiO_2-terminated surface and (d) SrO-terminated surface.
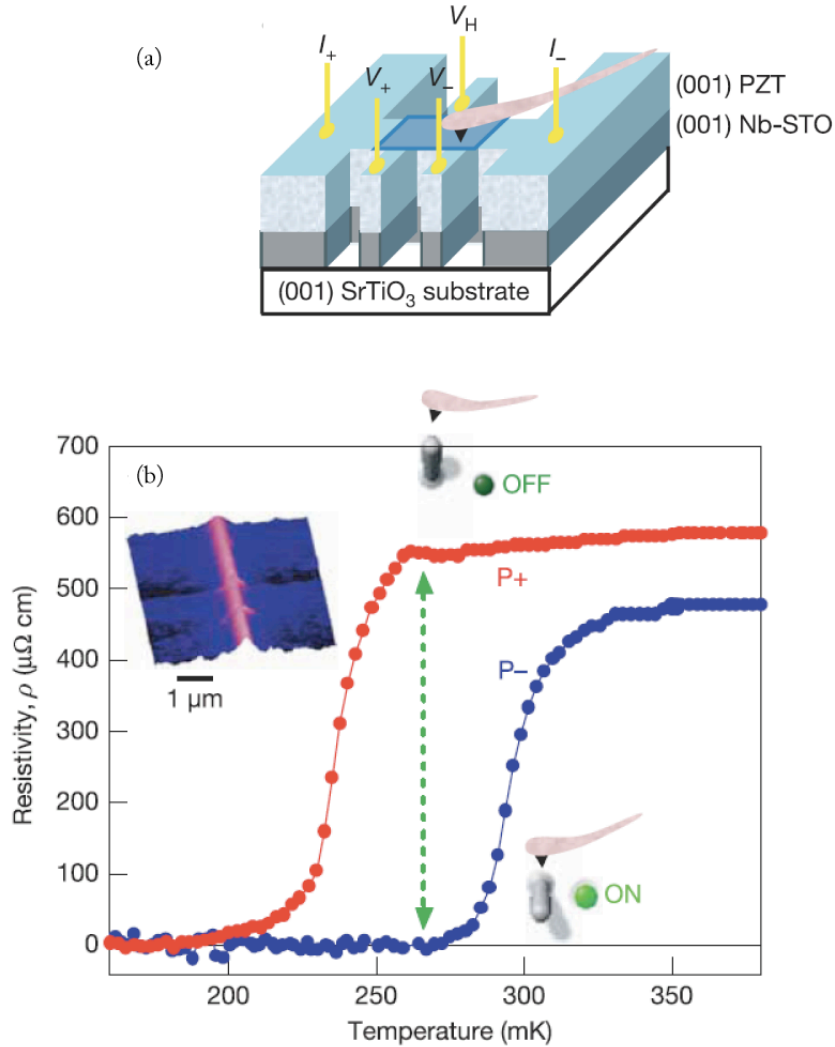
Fig. 1.4 (a) Diagram of the superconducting device and (b) superconducting properties for the two polarization state. The resistivity vs. temperature plot is shown close to the superconducting transition point. As indicated by the arrow and the associated insets, a superconducting on-off switching is observed around 270 mK, illustrated by the 'Atomic Force Microscope switch' shown in the inset. The left inset shows the piezoresponse image after poling a P+ state line in the P- state background (ref. 9).
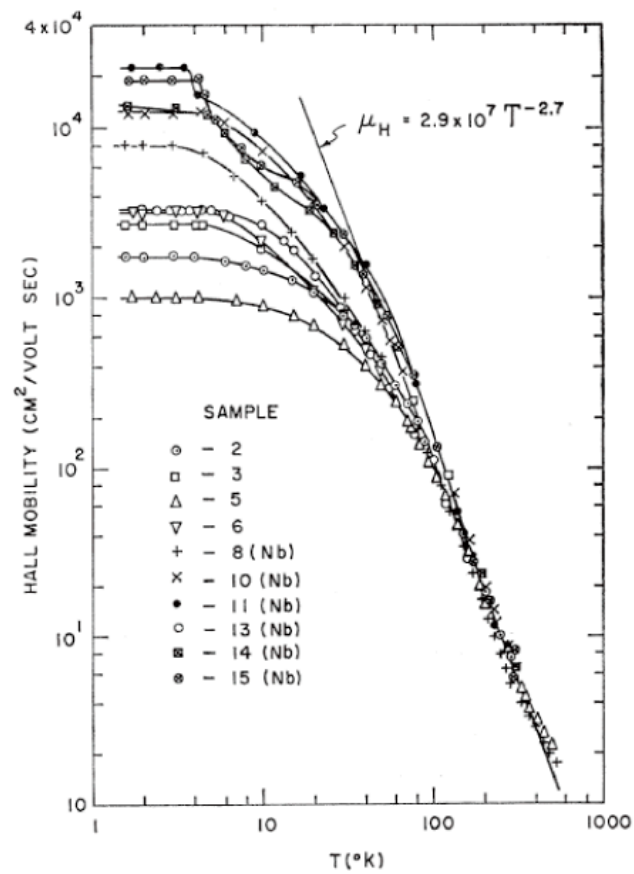
Fig. 1.5 The temperature dependence of Hall mobility in chemically doped $SrTiO_3$ (Ref. 16).
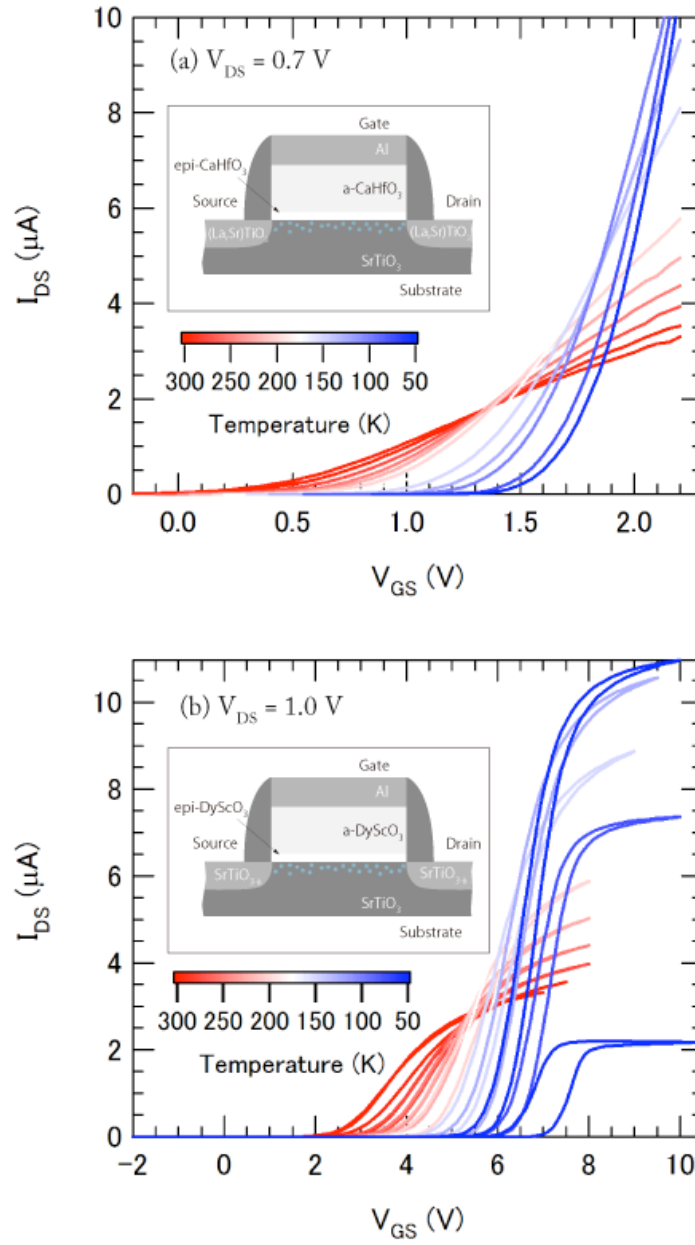
Fig. 1.6 The temperature dependence of I_{DS}-V_{GS} characteristics of (a) epitaxial CaHfO$_3$ FET and (b) amorphous DyScO$_3$ FET. V_{DS} is 0.7 V and 1.0 V, respectively.

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Chapter 2
Equipment and Techniques

In order to investigate the structure and properties of a nanoscale gate stack structure, it is necessary to control the crystal growth on an atomic scale and the electrical measurements need to be very accurate. In this chapter, I will introduce the experimental equipment – the pulsed laser deposition setup used for thin film growth and the electrical measurement system used for dielectric characterization. I will also discuss data analysis techniques – how to calculate real physical parameter values, such as thickness and pad area. The choice of materials, – why I chose $DyScO_3$, is also explained.

2.1 Pulsed Laser Deposition

The development of an oxide thin film deposition technique that can achieve atomic-scale control of crystal growth is a prerequisite for the fabrication of next-generation low-dimensional oxide superstructures and the investigation of novel physical properties in oxide heterostructures. Pulsed laser deposition (PLD) is an efficient thin film growth technique for oxides, many of which have very high melting points and contain many different elements in a unit cell[i]. This thin film deposition method is has been used widely to study many different types of oxide materials, including high-temperature superconductors, ferroelectrics, giant magnetoresistance manganites, and various types of dielectrics.

However, even the PLD method presents many experimental challenges. A common problem with PLD systems is limited experimental reproducibility. Thin film growth conditions typically need to be re-optimized for each deposition system and it is difficult to rely on the particular numerical parameters provided in literature. Even when using the same PLD system, it can be difficult to obtain perfectly repeatable result over long time periods, especially if the chamber operator is changed[ii]. The main reason for this is the difficulty of reproducing accurately the ablation laser conditions, such as the shape an size of the ablation plume. To achieve adequate repeatability, it is primarily necessary to control precisely the laser ablation area and energy density. Other parameters, such as temperature or gas pressure are easier to control, using conventional vacuum equipment.

The system described here used a pulsed KrF excimer laser operating at a wavelength of 248 nm for ablation of oxide targets. As shown in Fig. 2.1, the chamber was quite compact, with a diameter of 200 mm and a height of 300 mm. The chamber was kept very clean, with a base pressure in the 10^{-9} Torr range. Samples were loaded into the chamber through a loading-lock system to prevent chamber contamination and do *in-situ* clean measurement. Reactive gases, typically pure oxygen, could be introduced into the chamber at accurately controlled rates through a piezoelectric gas dozer which was controlled by a LabVIEW program, as shown Fig. 2.3. The sample stage holding the substrate crystal was mounted about 40 mm above the target.

Fig. 2.2 shows a schematic drawing of the deposition system and a detailed diagram of the chamber. The excimer laser light was introduced into the chamber at a 30 degree incidence angle to the target surface. The energy of laser pulses was adjusted with an optical attenuator. Low-energy edges of the laser beam were cut off with a suitable aperture and the light was focused on the target surface with a single plano-convex lens with a focal length of 300 mm. This lens was mounted on a x-y-z stage so that the position on the target and the imaging spot size could be adjusted. Ablation position adjustments are necessary in order to align the center of the ablation plume with the center of the sample. The spot size needed to be adjusted to tune the energy density and plume shape. The target rotates to control stable plume oriented. The laser energy density is one of the most important parameters for controlling the ablation process[iii]. The actual energy density on the surface of a target can easily change due to the unavoidable contamination of the entrance view port[iv]. It was therefore necessary to measure the actual laser energy for every film deposition. A thermoelectric power meter connected to an oscilloscope was used for monitoring the laser energy in front of the

focus lens. Fig. 2.3 (a) shows the film growth rate vs. laser fluence. The ablation spot size was 0.046 cm^2. Obviously, the growth rate increases with laser fluence. Earlier work performed by Nishio has shown that in terms of crystallinity and breakdown strength, the most suitable growth conditions for DyScO$_3$ films is 1 mTorr oxygen pressure and high laser fluence[v]. In this work, I selected similar conditions. Despite these efforts, even the best films appeared to be slightly Dy rich, with Dy/(Dy+Sc)=57 %.

2.2 Selection of electrode and oxide materials

In this thesis, electrical characteristics of insulating oxides and MIS capacitors were studied and are discussed. To study the detailed electrical properties of an insulator or an oxide heterointerfaces, it is necessary to choose contact metals so that an Ohmic contact is achieved. In order to find the most suitable materials for electrodes, various metals were deposited on 0.5 wt.% Nb-doped SrTiO$_3$ substrates. Fig. 2.4 shows typical current-voltage characteristics for different metals, such as Pt, Au, Ag, and Al. Only Al could obtain ohmic contact with the substrate. Work functions of Pt, Au, Ag, and Al metals are 5.3, 4.9, 4.5, and 4.2 eV, respectively. The metal materials with large work functions obviously formed a Schottky barrier when deposited on Nb-doped SrTiO$_3$. In such cases, precise electrical properties cannot be measured due to the Schottky barriers and it becomes difficult to extract true insulator properties. Ahn *et al.* have recently also shown that Ohmic contact can be obtained between aluminum electrodes and wide-gap oxide materials [vi]. Therefore, only Al electrodes were used for all electrical measurements in this thesis.

Among possible substrate materials, Nb-doped SrTiO$_3$ was chosen to work as an n-type semiconductor since SrTiO$_3$ is a standard substrate for the deposition of perovskite oxides, as was discussed in Chapter 1. Nb-doped SrTiO$_3$ is an n-type semiconductor with an energy band gap of 3.2 eV and an electron affinity of 4 eV[vii,viii,ix]. It is therefore understandable that between Al and Nb-doped SrTiO$_3$ a good Ohmic contact is possible due to the similar work functions. DyScO$_3$ was chosen as a wide-gap insulator on Nb-doped SrTiO$_3$ for three reasons. Firstly, the oxide insulator material should have low leakage current since lower leakage current ultimately limits device scaling and the maximum achievable electrostatic carrier modulation level. Secondly, it is compatible with SrTiO$_3$ in terms of lattice parameters, with a mismatch of about 1%. Larger lattice mismatch with SrTiO$_3$ would result in a defect rich interface, with a large

interface density of states, and the formation of grains. Grain boundaries are the main source of electrostatic breakdown for thin films and should therefore be avoided. Finally, oxide insulator should have a band gap larger than 3.2 eV, which is the gap energy of $SrTiO_3$. This is necessary in order to form a MIS capacitor. In case of Si, the intrinsic oxide is the most suitable insulator materials. As I mentioned in Chapter 1, $SrTiO_3$ is an attractive and alternate material for next generation device development, but the list of suitable insulator candidate materials is very limited. Since the gap of $SrTiO_3$ is already quite large, the gap energy of the insulator has to be larger than 5 eV. Wide-gap materials also tend to have lower dielectric constants, so the benefits of using such wide-gap oxides are lost in case of field-effect device applications, since reduction of the dielectric permittivity also reduces the accumulated charge for a given gate bias. The crystallographic data for the materials evaluated in this work: $CaZrO_3$, $CaHfO_3$, $NdGaO_3$, $LaGaO_3$, and $DyScO_3$, are listed in Table 2.1[x,xi]. All of these compounds have a noncubic perovskite structure. The materials that have an average mismatch with $SrTiO_3$ of less than 3 % were selected. The band gap of these materials is not well known, especially in thin films. However, estimates based on the values published[xii] for $BaZrO_3$, ZrO_2, and HfO_3, put the gap width above 5 eV. The band gap is useful for a gate insulator material because it is possible to achieve lower leakage currents than with $SrTiO_3$ thin films, which generally cannot be used at fields above 1 MV/cm[xiii] in accumulation-type devices. As we can see in Table 2.1, $NdGaO_3$, $LaGaO_3$ and $DyScO_3$ have smaller average mismatch than $CaZrO_3$ and $CaHfO_3$. While these three materials have an advantage in terms of average mismatch with $SrTiO_3$, $CaZrO_3$ and $DyScO_3$ have slightly larger dielectric constants than $CaHfO_3$, $NdGaO_3$ and $LaGaO_3$. It is superior these two materials in terms of permittivity. Among the listed wide-gap oxides, $DyScO_3$ was selected as the best epitaxial insulator material for combining with $SrTiO_3$. In this thesis I investigate electrical properties of thin $DyScO_3$ films due to these reasons..

2.3 Characterization of electrical properties

The main theme of this work is the control of the electronic properties of oxide heterointefaces. This is a very broad and large research topic, since there are many aspects of properties such as the density of defects, impurities, and accumulated carriers that can affect the material behavior at the interface. Due to that, suitable electrical measurement was needed for investigating each material parameter. In this work, I used

an Agilent 4284 LCR meter for capacitance measurements and a Keithly 4200 semiconductor analyzer for leakage current measurement. Capacitance measurements were carried out in a four-terminal probe configuration, while the leak current was measured in a simple two-terminal geometry. Assuming that no Schottky barriers form at the electrode interface, the contact resistance does not have a significant effect on the leak current measurement. Capacitance measurements, especially if a wide frequency range should be covered, can be very sensitive to contact effects and a four-point measurement is therefore mandatory.

In capacitor measurement case, the LCR meter was operated in the *Cp-D* mode, which displays the capacitance and the loss tangent of a device assuming a parallel capacitor-resistor equivalent circuit. In the following, the MIS capacitor equivalent circuit is assumed to have a resistance (R_p) and capacitance (C_p). D is *tan δ* (dissipation). Since the equivalent circuit is relatively simple, it is also possible to calculate the complex impedance (Z_p) from the measured C_p and D values. This impedance is given by

$$Z_p = \frac{R_p}{1 + \omega^2 C_p{}^2 R_p{}^2} - j\frac{\omega C_p R_p}{1 + \omega^2 C_p{}^2 R_p{}^2} = R + jX , \qquad (2.1)$$

$$\omega = 2\pi f , \qquad (2.2)$$

where the impedance has a real part (R) and a complex part (X), ϖ is the angular frequency which is given by Eq. (2.3) and f is the measurement frequency. From these equations, parallel capacitance and dissipation is given by

$$C_p = \frac{|X|}{\omega(R^2 + X^2)} , \qquad (2.3)$$

$$D = \frac{R}{|X|} , \qquad (2.4)$$

This is the *Cp-D* measurement mode and I used this mode for characterizing the dielectric properties of the MIS capacitors.

2.4 Physical parameters: Thickness and Pad area

Two physical parameters of test devices need to be accurately known, namely the true insulator thickness and the real measurement pad area. Uncertain of either value causes

big errors in the derived dielectric characteristics. The measured capacitance value for a parallel-plate capacitor is given by

$$C = \varepsilon \frac{S}{d},$$
(2.5)

where C is the measured capacitance, ε is the dielectric constant, S is the pad area, and d is the film thickness. The pad area and film thickness are the capacitor's physical values, so uncertain or incorrect value of this has large incorrect value of dielectric constant. To avoid this problem, I have used two strategies. First is calculating the pad area by counting pixels in a digital camera image using Image J software, as shown Fig.2.6. Image J is open-source Java program that can run on various platforms, such as Linux, Mac OSX, and Windows. It can be used to measure object area, mean size, standard deviations, minimum and maximum intensity values in an image, etc. For capacitor measurements, the pixel area counting function was used. If the images are calibrated, the pad area can be accurately determined, even if the shape is slightly irregular. Second technique was calculating the true film thickness by Capacitance Equivalent Thickness (CET), which can be obtained from Eq. 2.5. Using these two techniques, it was possible to perform accurate and reliable electrical characteristics measurements. In this thesis, I used 0.00185 cm^2 pads for C-V and 0.00036 cm^2 pads for I-V measurement. C-V measurements used larger pad area in order to obtain a large enough device capacitance to exceed the noise and cable effects of the measurement setup. For I-V measurements, it was beneficial to use the smallest practical area in order to avoid the chance of having a large defect or particle within the measurement pad area.

2.5 Sample fabrication

The capacitors were fabricated on as-supplied 0.5 wt.% Nb-doped SrTiO$_3$ (100) substrates which were cleaned chemically in acetone (5 min. ultrasonic agitation) to remove organic contamination from the surface. As the first step, gate insulator layers were grown by Pulsed laser deposition at an oxygen pressure of 1 mTorr. A KrF excimer laser (λ=248 nm), operating at 5 Hz was used for ablation. The fluence on the surface of the ceramic ablation target was around 0.9 J/cm^2, resulting in a deposition rate of approximately 0.1 Å per pulse on the Nb-doped SrTiO$_3$ surface. After insulator film growth, Aluminum was thermally evaporated on the insulator film surface through a stainless steel stencil mask. Aluminum was selected because we can get clearly ohmic

contact on Nb-doped $SrTiO_3$ (Fig. 2.4) and it has been reported that Ohmic contact can be obtained between aluminum electrodes and wide-gap oxide materials[xiv]. The whole capacitor fabrication process was done at room temperature for amorphous insulator samples. It was therefore not necessary to care about substrate surface reconstruction or Nb-diffusion or strain effects. Capacitors with different thicknesses (20 – 200 nm) were fabricated by using this procedure.

   The electrical properties of these capacitors were characterized as follows: The initial capacitance and a capacitance vs. frequency (C-f) scans were take first at zero applied bias, followed by capacitance - voltage (C-V) and leakage current – voltage (I-V) characteristics for all capacitors. In I-V measurement, the breakdown field was also determined for some devices on each substrate. The capacitors were then kept under large positive gate field to study the effect of field stress on the dielectric properties. Transient capacitances were measured during application of constant bias voltage. Charge trapping and charge de-trapping behaviors were investigated by measuring transient capacitance during stress voltages application and relaxation. The capacitors were measured with an Agilent 4284 precision LCR meter in a four-terminal measurement and a Keithly 4200 semiconductor analyzer for I-V in simple two-terminal measurements while the devices were mounted in a manual probing station. In LCR meter measurements, the *Cp–D* mode was used. The complex impedance was calculated from these results when necessary. Also, temperature dependence measurement was done for leak current. In this measurement, the sample was placed in dipping-type probe and inserted slowly into a liquid Helium dewar.
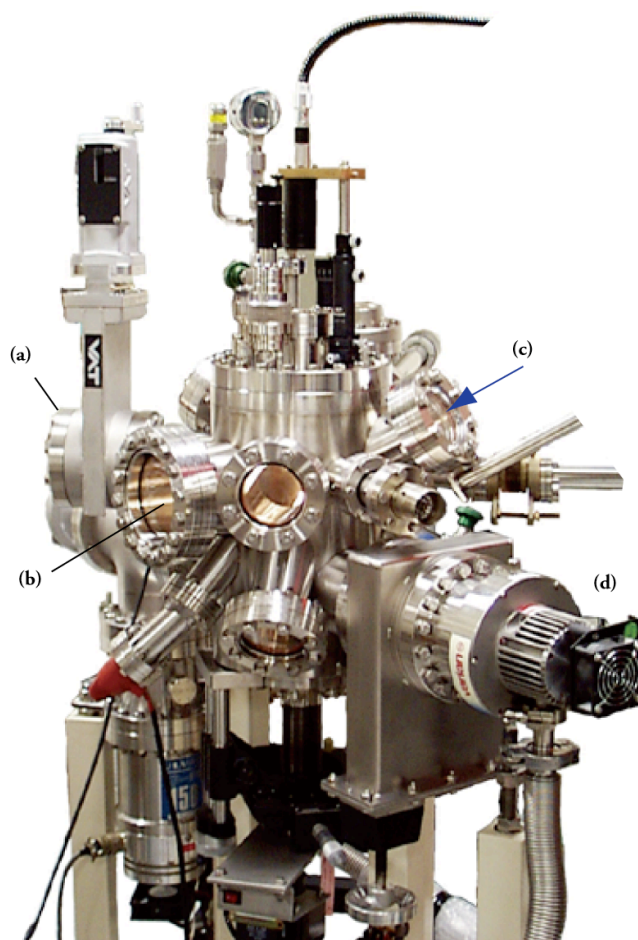
Fig. 2.1 A photograph of the deposition system. (a) Side port for additional surface analysis apparatus, (b) RHEED screen, (c) Excimer laser entry port for ablation, and (d) Vacuum pump.
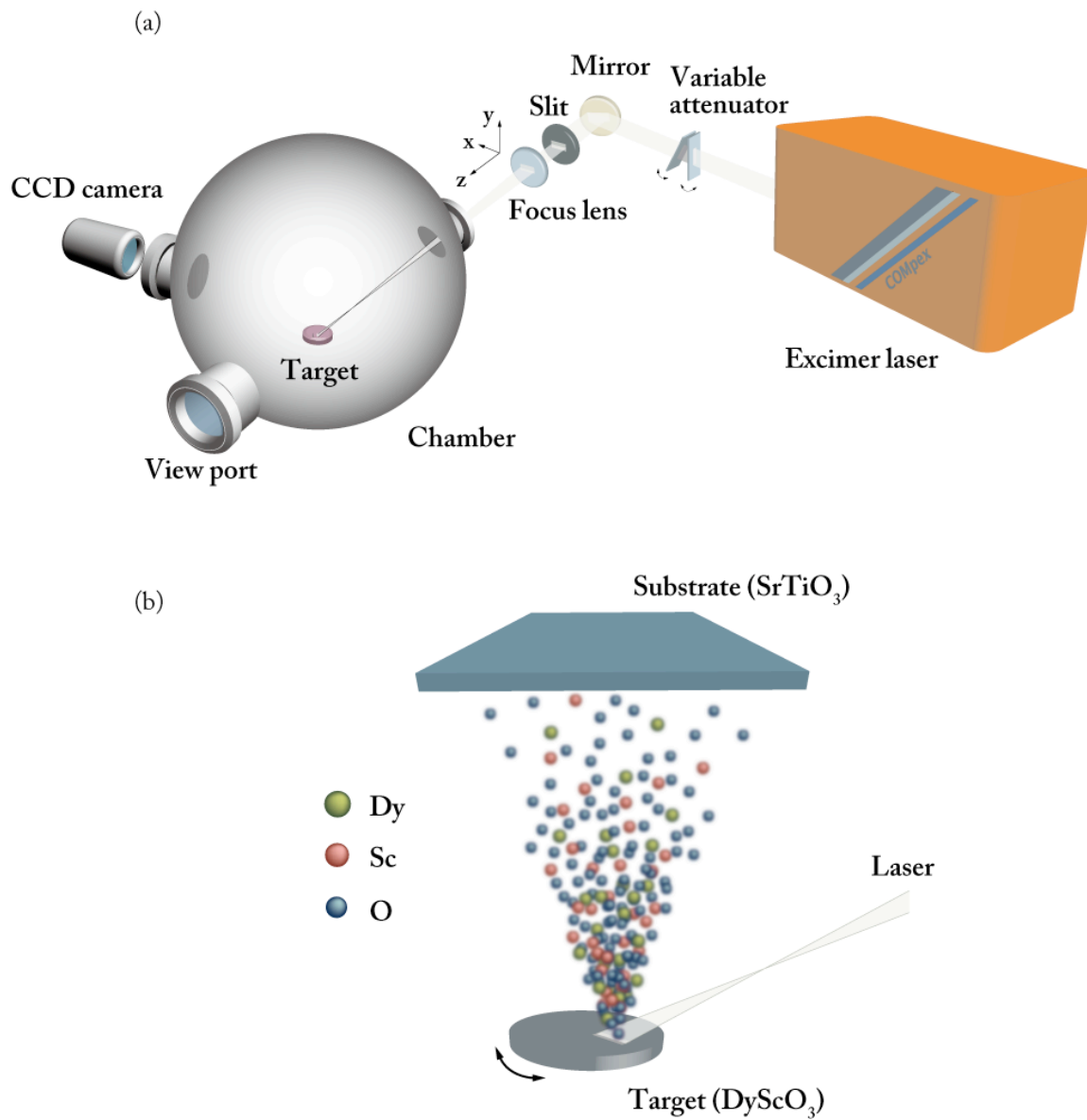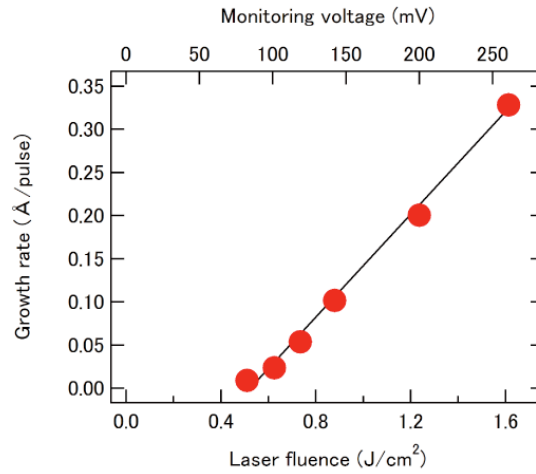
(a)

(b)

Fig. 2.2 (a) Schematic drawing of the optical beam path of the deposition system and (b) a conceptual drawing of the Pulsed laser deposition film growth process.
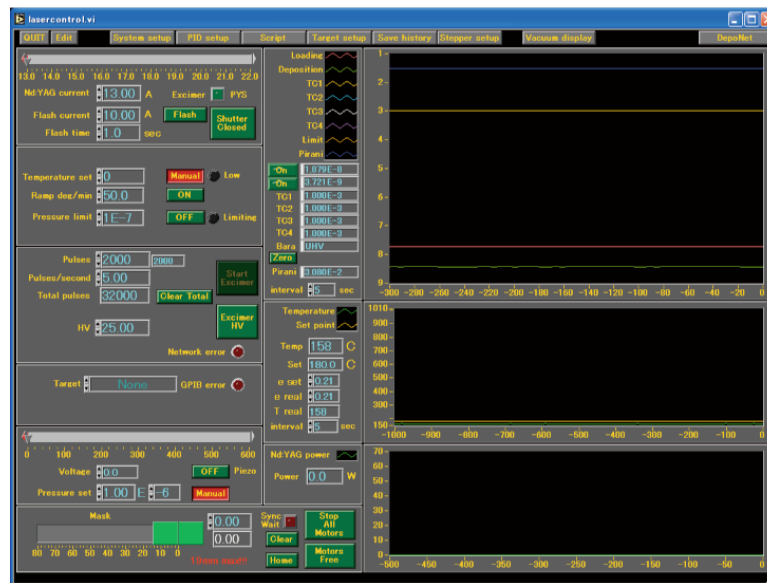
(a)

(b)

Fig. 2.3 (a) Growth rate vs. laser fluence plot. The target material was $DyScO_3$ and growth oxygen pressure was 1 mTorr. (b) Pulsed laser deposition control system LabVIEW program front panel.
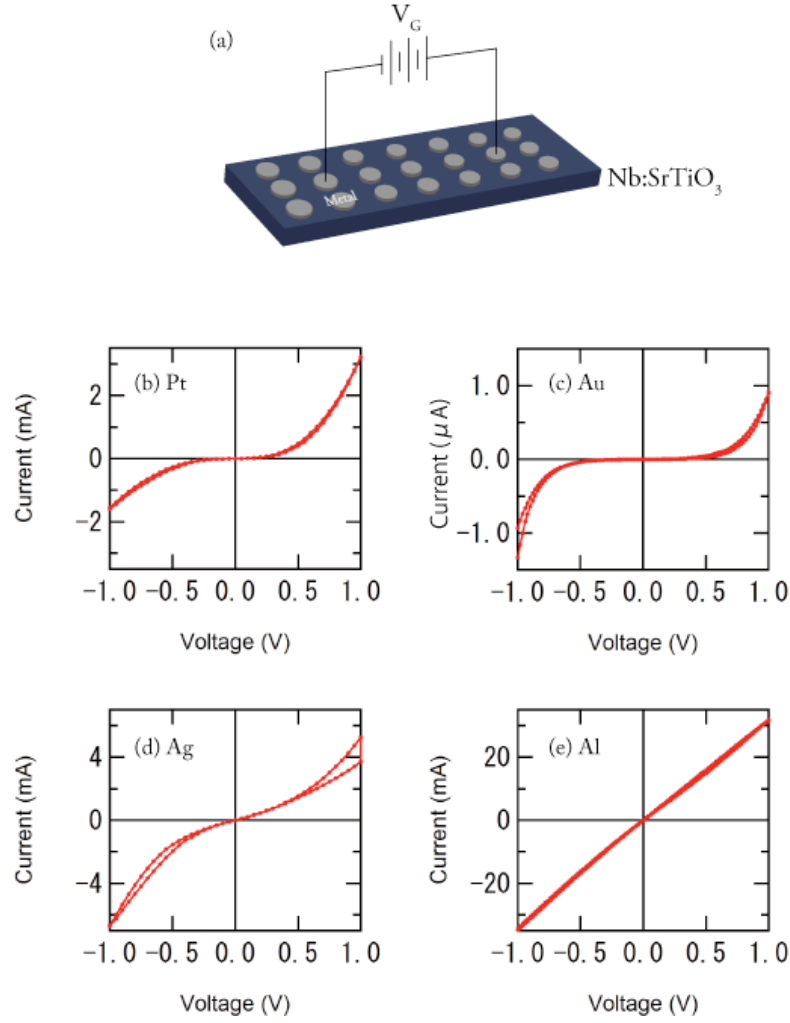
Fig. 2.4 (a) Schematic diagram of various metal pads on a SrTiO$_3$ substrate and (b-e) I(V) measurements for different metal electrodes on 0.5 wt.% Nb-doped SrTiO$_3$ substrates. The metals are (b) Pt, (c) Au, (d) Ag, and (e) Al, respectively.

Table 2.1 Lattice constants of various wide-gap insulator materials, which are nearly lattice-matched with $SrTiO_3$. Lattice mismatch was calculated assuming an orthorhombic unit cell for $SrTiO_3$. Average mismatch means lattice mismatch with $SrTiO_3$, and epsilon is the dielectric constant.

	a (Å)	b (Å)	c (Å)	crystal structure	average mismatch	ε
$SrTiO_3$	3.905 (5.523)	3.905 (5.523)	3.905 (7.810)	cubic (orthorhombic unit cell)	–	–
$CaZrO_3$	5.756 (4.22 %)	8.010 (2.56 %)	5.593 (1.27 %)	orthorhombic	2.7 %	25 – 33
$CaHfO_3$	5.719 (3.55 %)	7.982 (2.20 %)	5.578 (1.00 %)	orthorhombic	2.3 %	16 – 17
$NdGaO_3$	5.433 (−1.61 %)	5.504 (−0.34 %)	7.716 (−1.21 %)	orthorhombic	−1.0 %	20 – 22
$LaGaO_3$	5.527 (0.08 %)	5.494 (−0.51 %)	7.777 (−0.42 %)	orthorhombic	−0.3 %	20 – 22
$DyScO_3$	5.440 (−1.50 %)	5.713 (3.44 %)	7.887 (0.99 %)	orthorhombic	1.0 %	22 – 30

(a)

V_G

a-DyScO$_3$
Nb:SrTiO$_3$

Al

(b)

LCR meter

Low curr Low pot Hi curr Hi pot

Agilent A4284

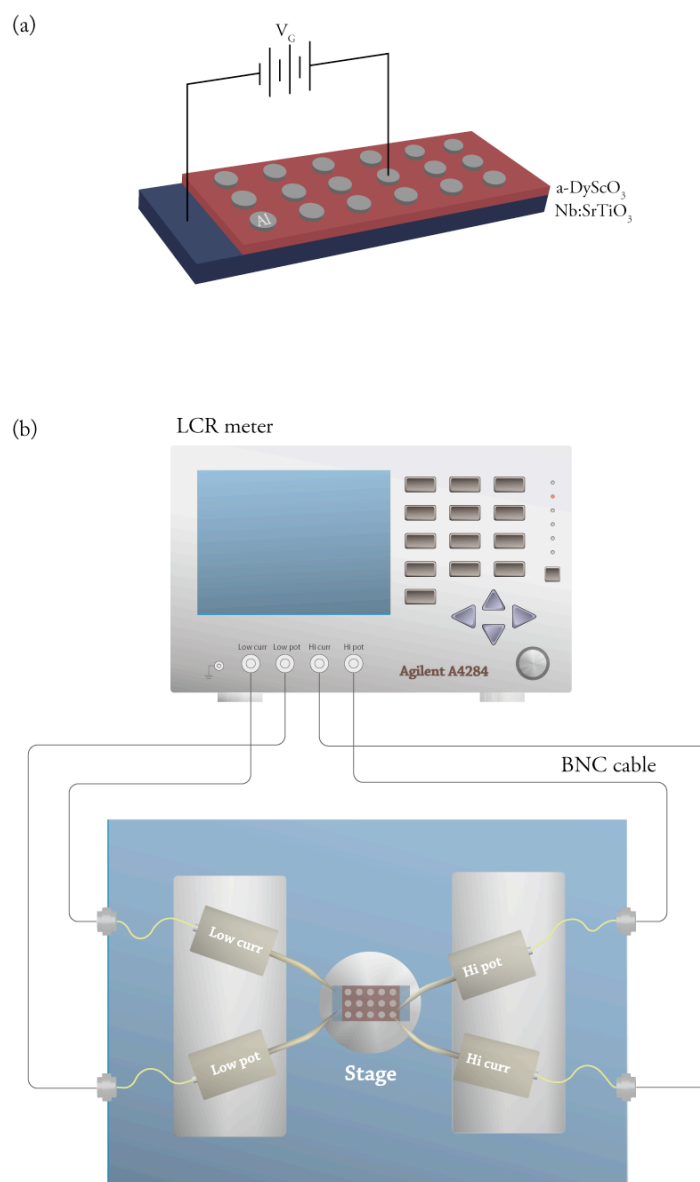BNC cable

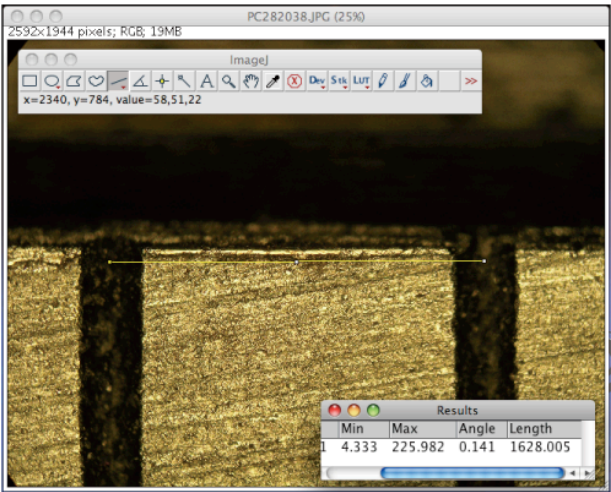Low curr

Hi pot

Low pot

Stage

Hi curr

Fig. 2.5 Schematic diagram of a measurement system. The sample geometry is shown in (a) and the placement of a sample in a manual probing station, connected to an LCR meter is illustrated in (b).
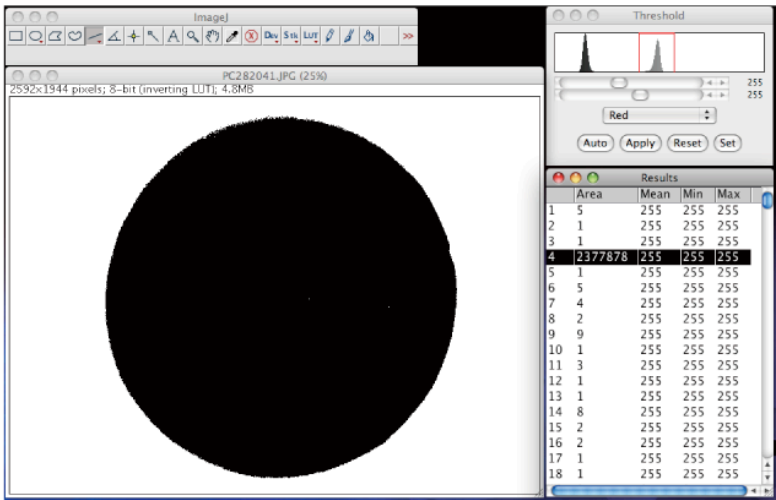
(a)

(b)

Fig. 2.6 (a) A photograph of a 1 mm scale used for pad size calibration. (b) The pad area was analyzed with Image J.

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Chapter 3
Dielectric properties of Al/DyScO₃/Nb -doped SrTiO₃ MIS capacitors

Generally, in real MIS devices, the interface between an insulator and a substrate is never completely electrically neutral. This is true even for the silicon dioxide-silicon interface. As shown in Fig. 3.1 (a), there can be mobile ionic charges[i], electrons or holes trapped in the insulator layer. For example, in silicon devices, mobile ionic charges in the insulator are usually due to sodium or potassium contamination introduced during device fabrication. Such charges can move from one end of the insulator layer to the other when an electric field is applied across the insulator. If electron-hole pairs are generated in an insulator, i.e. by ionizing radiation, some of these electrons and holes can be trapped in the insulator. Also, if electrons or hole are injected into an insulator layer by tunneling or hot-carrier injection, some of those carriers may become trapped in the insulator as well. These mechanisms give rise to trapped charge. There can also be fabrication-process-induced fixed oxide charges near the insulator-substrate interface. These charges can be caused by charged defects at the interface or by surface states of the substrate[ii]. In case of complex oxide insulators, such as DyScO₃, fixed charge can be created by defects associated with excess cations of a specific type, for

example Dy or Sc. For oxides, carriers can also be injected by the lack of oxygen introduced during deposition, oxidation, and post-oxidation heat treatment. Electrons or holes can accumulate in or be released from defect states or substrate surface states near the substrate-insulator interface under applied bias. At the substrate and insulator interface, the lattice of bulk the substrate and all the properties associated with its periodicity terminate with either SrO or TiO_2 in the case of $SrTiO_3$. As a result, localized states within the forbidden energy gap of $SrTiO_3$ are introduced at or very near the $SrTiO_3$ and $DyScO_3$ interface[iii]. These localized surface states are illustrated schematically in Fig. 3.1 (b). This accumulated charge is known as interface trapped charge. In this chapter, I have investigated these charges in $DyScO_3$ MIS capacitors and tried to clarify the threshold voltage shift in oxide field effect transistor heterostructures.

3.1 Zero-bias characteristics

Among dielectric properties, frequency dependence of permittivity at zero bias is a very important measurement since there are various effects that can be sampled by this technique, such as electrode contact effects, tunneling current and parasitic capacitances in the device or the measurement setup. If the secondary effects are large, it may become impossible to determine the true dielectric properties of a sample. It is often therefore necessary to use a frequency scan to determine the optimum frequency for permittivity measurements. Fig. 3.2 shows the frequency dependence of permittivity as a function of insulator ($DyScO_3$) thicknesses in Nb-doped $SrTiO_3$/a-$DyScO_3$/Al devices. A typical insulator thickness in field-effect devices is between 20 and 60 nm. A similar thickness range, from 20 to 200 nm, was selected for the MIS capacitor studies. Initial measurements were conducted at zero applied bias in order to avoid charge movement or charge injection into the devices. Measurements were done at room temperature. For each measured sample, the frequency dependence was related to the inverse thickness of the insulator film[iv]. This procedure is explained in Section 3.3. As the plot in Fig. 3.2 shows, the apparent permittivity started to drop sharply at frequencies above about 100 kHz. There is also a strong thickness dependence in permittivity. In thicker films, the estimated dielectric constant was close to 21, which is similar to bulk samples. In thinner films, however, there was a systematic drop of permittivity to about 16. Tis drop became particularly large below a thickness of about 40 nm. As the insulator film was

amorphous, it would be reasonable to expect that the insulator material properties themselves do not have such a strong thickness dependence. What the apparent permittivity drop with thickness shows, is actually a manifestation of a common problem in dielectric film analysis, namely the presence of interface layers that have unknown dielectric properties. In further work, it was very important to know the true dielectric constant of the films. This was done by using a simple two-layer capacitor model[v,vi], which can be used to produce so-called 'Equivalent oxide thickness plots'. A rather good estimate of the true insulator permittivity can be extracted from such plots. For the two-layer capacitor model analysis, I selected a measurement frequency of 100 kHz at zero bias. The equivalent circuit analysis is discussed in Section 3.2.

   This model makes the following assumptions: a possible interfacial layer contribution to the device capacitance can be separated from the bulk film permittivity by measuring a series of samples with different thicknesses and assuming a two-layer capacitor model. Although a device includes two interfaces on either side of the insulator film, as a first approximation, these interfaces can be lumped together, since it is not possible to extract accurate dielectric properties of the interfaces independently anyway. This model assumes there exists an undisturbed bulk region of thickness t_B and permittivity ε_B, and the two interface regions with a total thickness t_{ix}, and an average, typically lower permittivity ε_{ix}. Here interface 1 ($x = 1$) is between the top aluminum electrode and insulator and interface 2 ($x = 2$) is between the insulator and the substrate, as shown in Fig. 3.3 (a). Assuming that the interface layers can be lumped together, the resulting reciprocal capacitance of the film is given by Eq. (3.1) and the slope of inverse capacitance, i.e. a $1/C$ vs. film thickness plot, yields the bulk permittivity. This equation assumes that the thickness change does not change the dielectric properties of the bulk of the film and that the interface layers, whatever their dielectric properties may be, also remain constant. In such a case, the total capacitance of a stack is given by

$$\frac{A}{C} = \frac{A}{C_{i1}} + \frac{A}{C_B} + \frac{A}{C_{i2}}$$

$$\approx \frac{2A}{C_i} + \frac{A}{C_B} = \frac{2t_i}{\varepsilon_0 \varepsilon_i} + \frac{t - 2t_i}{\varepsilon_0 \varepsilon_B} \approx \frac{2t_i}{\varepsilon_0 \varepsilon_i} + \frac{t}{\varepsilon_0 \varepsilon_B}, \qquad (3.1)$$

where C_B is the bulk capacitance and C_{ix} is the interface capacitance, and A is the capacitor area, calculated with 'Image J' from digital camera images of actual sample pads. Obviously, the thickness of the films should be larger than the interface layer, i.e. $t \gg t_i$. For any reasonable interface layer thickness, this condition should be true for films that have a thickness of 40 nm or more. Any deviations would in any case show

up as nonlinearities in the reciprocal capacitance plot. The actual bulk permittivity, ε_B, can then be extracted from the slope of a linear fit. Also, the zero-thickness intercept represents the total interface capacitance, as shown in Eq (3.1). The Equivalent Oxide Thickness (EOT) plot as a function of thickness is shown in Fig. 3.3 (b). When oxide insulators are combined with silicon devices, the same plots are often called equivalent oxide thickness (EOT) plots, where EOT is the thickness of a hypothetical SiO_2 layer that would give the same capacitance as the high-permittivity oxide:

$$EOT = \varepsilon_{SiO_2} \varepsilon_0 \frac{A}{C},$$ (3.2)

where ε_{SiO2} is the dielectric constant of SiO_2. For purely oxide devices, this parameter has no direct value and the actual EOT numbers are not evaluated here. As we can see in Fig. 3.3 (b), the measured data points do fall nearly perfectly on a straight line, indicating that the two-layer model is valid in this case. The slope of the plot gave a dielectric constant of 21.4. This is comparable to the reported value $\varepsilon = 21.2$[vii] and $\varepsilon = 24$, which have been calculated for $DyScO_3$ from molecular polarizabilities of Dy_2O_3 and Sc_2O_5[viii]. Also, the extrapolation of the linear fit to t = 0 gave an interface layer capacitance of 12.6 nF. This number can be used to obtain at least an order-of-magitude estimate for the interface layer thickness. The permittivity of the interface layers is at most equal to that of the bulk insulator. If the permittivity of the interface layer is equal to bulk ($\varepsilon_{max} = 21.4$), the interface capacitance would correspond to a layer thickness of 2.8 nm, which equals about 7 unit cells of $SrTiO_3$ and includes both the substrate and electrode interface layers. Assuming that the interface layers are similar, this would mean that either interface is about 1.4 nm thick, or about 3 unit cells. In the following Capacitance equivalent thickness (CET) calculations a permittivity of 21.4 will be used (except in Section 3.3).

3.2 Equivalent circuit

In Section 3.1, I obtained the bulk insulator permittivity of 21.4 and an interface capacitance of 12.6 nF from a two-layer model analysis. In this Section, I further evaluate the validity of such a model.

Equivalent circuit is a simplified model of a real sample. The purpose is to reproduce the behavior of a measured device with a circuit that only contains pure resistances, capacitances, and inductances. If the model is chosen appropriately, individual model

circuit component parameters, such as resistance or capacitance, can be related to actual physical parameters of a heterostructure, such as leak current or interface layer permittivity. In this case, I used a circuit with a total of 6 parameters, as shown in Fig. 3.4 (a). The first parallel section is composed of a capacitance (C_{P1}) and a resistance (R_{P1}). This circuit simulates the bulk $DyScO_3$ response with a fixed permittivity and ohmic leak current. The second parallel circuit is also composed of a capacitance (C_{P2}) and resistance (R_{P2}), which corresponds to a leaky interface layer with a different permittivity from the bulk of the film. Other series resistance (R_S) and inductance (L_S) correspond to the contact resistance and the measurement setup cable inductance. The dielectric characterization is performed by measuring the complex impedance of a sample. The complex impedance measurement produces two numbers, the real and imaginary parts of the circuit response. It is therefore clear that it is impossible to derive all six model parameters from a single measurement. The solution here is to use data from several measurements done at different frequencies. In practice the model is used to fit the frequency dependence of measured capacitance and loss figures. This fitting was conducted by using Igor data analysis software. The detailed program used for fitting is attached in Appendix 1. In order to obtain a satisfactory fit, it was necessary to add one more parameter, D_{CP} which corresponds to frequency-dependent permittivity component of the bulk insulator. This frequency-dependent component was added as

$$C_{P1} = C_{P1} + D_{CP} \log(f),\qquad(3.3)$$

$$\tan\delta = D + D_{OFF},\qquad(3.4)$$

where f is the variable measurement frequency, and D is the loss tangent, calculated from the equivalent circuit. The loss tangent offset D_{off} has no physical meaning but is simply added to allow the fitting routine to converge. The physical origin of the loss figure offset is in the impedance meter (Agilent 4284) itself. Figs. 3.4 (b) and (c) show the results of the frequency dependence measurements at zero bias. The measurement was done in the C_p-D, where the LCR meter recalculates the measured complex impedance in terms of a parallel capacitance and $tan\ \delta$ loss figure. Continuous lines are the fitting results. The data in Fig. 3.4 was obtained from a sample that was 190 nm thick (Fig. 3.2). Other data sets did not show significant differences.

The fitting showed that the cabling-related series inductance (L_S) caused the observed capacitance drop at high frequency. Since the samples need to be measured either in a probing station or in a low-temperature dipping probe, relatively long cables are inevitable. This means that measurements should be performed at frequencies below about 100 kHz. The high-frequency part of the frequency dependence curve is also very

sensitive to series resistance (R_S), mostly causing the sharp rise of the loss coefficient at high frequency. The slope of capacitance between 1 kHz and 100 kHz was fitted by adding the D_{CP} parameter, as discussed earlier. The fitting results are shown in Fig. 3.4 (a). Especially, C_{P2}, which is the interface capacitance, was 45.1 nF. The resistance of the interface layer, R_{P2}, was only 20 kΩ, which shows that the interface layers are very leaky dielectrics. The interface region (which could be expressed as parallel equivalent circuit), has a maximum thickness of 0.8 nm, corresponding to only 2 unit cells of $SrTiO_3$, if the dielectric constant is assumed to be 21.4 (equal to $DyScO_3$ bulk). This is a comparable value to that obtained from the two-layer model, so it can be concluded that the two analysis techniques are consistent and the thickness of the interface layer is a few nanometers at most. As shown by the capacitance measurements, however, even such a thin interface layer can have a very strong dielectric effect. This is significant for field-effect device design with high-permittivity dielectrics.

3.3 Thickness dependence of field effect

In Sections 3.1 and 3.2, I concluded that interface regions are present in the MIS devices. The thickness of these layers was estimated to be between 0.8 nm to 2.8 nm. The dielectric constant of the bulk insulator is 21.4. In this section, I use these results and study field-effect modulation in Al /$DyScO_3$ /Nb: $SrTiO_3$ MIS capacitors.

Fig. 3.5 shows the thickness dependence of normalized capacitance as a function of applied voltage. For all thicknesses, positive curvature was observed. Possible mechanisms responsible for this positive behavior are space charge effects and dipolar relaxation, as suggested by Blonkowski et al.[ix]. As we could also see, these plots are nearly, but not quite symmetric around the zero bias point. There is also a slight thickness dependence, but the capacitance change under bias remains under 1 %. The film thickness is determined by physical measurement with a profilometer. This number contains a fairly large statistical error. The capacitance variation with bias voltage, which is also known as voltage linearity, is an important parameter for ceramic capacitor design, such as Metal-Insulator-Metal devices, especially for analog applications[x,xi,xii,xiii]. The voltage linearity can be described by

$$C(V) = C_0(\alpha V^2 + \beta V), \qquad\qquad (3.5)$$

where, V is the applied voltage, C_0 is the capacitance at zero bias, α and β are the

quadratic and the linear coefficients, respectively and are usually expressed in parts per million (ppm). The recommended α value for capacitors should be less than 100 ppm/V^2 for RF bypass applications and 1000 ppm/V^2 for precision analog devices, while the linear coefficient (β) value is not a very crucial factor because it can be canceled out by using a differential technique[xiv]. Hence this assumption also follows as

$$\alpha \propto \frac{1}{t}, \qquad\qquad\qquad (3.6)$$

where t is the effective thickness. This relationship can be used to derive an effective thickness from the C-V data and can be justified by considering that the 0.5 wt% Nb-doped SrTiO$_3$ substrate cannot be guaranteed to be metallic on the surface[xv]. In this case, the difference between the top (Al) and bottom (Nb-doped SrTiO$_3$) electrodes may cause a slight asymmetry. For more detailed investigation, I used quadratic fitting of the C-V curves in a field strength range from around 0.25 MV/cm to 1 MV/cm at 100 nm to 190 nm thick capacitors, as shown in Fig. 3.5. These thicknesses were selected because thicker samples have smaller statistical noise. As we can see in Fig. 3.6 (a), the bias-dependent capacitance deviation is fairly small, but generally follows a quadratic shape. It appears that α values strongly depend on the film thickness and the range was from 40 to 140 ppm/V^2. Figs. 3.6 (b), (c), and (d) show the normalized capacitance as a function of bias field strength. The film thicknesses of these three samples are 190 nm, 60 nm, and 20 nm, respectively. As we can see, a large hysteresis appeared in thinner capacitors, where the contribution of the interface layers to the total capacitance is expected to increase. This can be understood in terms of charge injection or movement in the interface layers, i.e. interface charge trapping. Fig. 3.6 (d) also shows the hysteresis direction, which supports the idea that the origin of this kind of behavior is trapped charge. Hysteresis is generally caused by mobile ionic charge or charge injection. From this data alone, it is not possible to determine which type of charging mechanism is the cause, since the hysteresis loop direction is opposite on the positive and negative sides, as shown in Fig. 3.6 (d).

As discussed in the previous paragraph, interface layers appear to contain trapped charge. For further analysis of this kind of charge trapping, I have investigated the flat-band voltage shift as a function of insulator thickness. Theoretically, for a MIS structure, the flat-band bias, i.e. where no band-bending exists, can be calculated from the difference of work functions between the top and bottom electrodes. In my case, the flat-band voltage shift is approximately -0.1 eV since there are approximately -0.1 eV difference between the work function of Al, which is around 4.1 to 4.3 eV for top

electrode, and the work function of Nb-doped $SrTiO_3$ which is around at most 4.1 eV for bottom electrode, as shown in Fig. 3.7 (a). In literature[xvi,xvii] i.e. S. M. Sze, 'Physics of Semiconductor Devices', realistic flat-band shift δV_g is derived from the one-dimensional Poisson equation given by

$$\frac{d^2}{dx^2} \Psi_P(x) = -\frac{\rho(x)}{\varepsilon_{Ins}},$$
(3.7)

where Ψ_P is the potential, $\rho(x)$ is total space-charge density, which is illustrated in Fig. 3.1 (a), and ε_{Ins} is the dielectric constant of the insulator. If I assume that a sheet of trapped charge Q is placed at a distance x from the top electrode, and a bias voltage δV_g has been applied to restore the MIS structure to its 'flat-band' conditions. By restoring the substrate surface potential to its original value, the sheet of trapped charge has induced no change in the charge distribution in the substrate, which is a function of the surface potential, but a charge of magnitude $-Q$ now exists on the metal electrode. This is illustrated in Fig. 3.7 (b). If the potential Ψ_P exists at surface, this is expressed by

$$\Psi_P(x = 0) \equiv \Psi_S.$$
(3.8)

In this assumption, integrating Eq. (3.7) from the electrode to the substrate is simply given by

$$\delta V_g = -\frac{Q}{\varepsilon_{Ins}} x.$$
(3.9)

This means δV_g is proportional to the amount of charge and the distance between the fixed charge and the gate electrode. Usually, the fixed charge exists near the interface between the insulator and the substrate, as shown in Fig. 3.1 (a). From these equations, the flat-band voltage shift as a function of thickness (x) decreases linearity if there is only fixed charge. For distributed charge, Eq. (3.9) can be rewritten as

$$\Delta V_g(\Psi_S) = -\frac{Q_{Ins}(\Psi_S)}{C_{Ins}},$$
(3.10)

$$Q_{Ins}(\Psi_S) \equiv \int_0^{t_{Ins}} \frac{x}{t_{Ins}} \rho(x, \Psi_S) dx.$$
(3.11)

Fig. 3.7 (c) is the result of flat-band voltage shifts calculation as a function of insulator thickness. The flat-band shift decreases (moves to negative side) in thick films, indicating that there is positive charge in the insulator or at the interface. Since the shift is thickness dependent, fixed charge in the insulator appears to be the more likely explanation. Large number of positive fixed charge for electron traps have been found

in various deposited oxide films[xviii,xix]. The most likely reason for such charge would be the presence of residual oxygen deficiency, which is induced by the fabrication-process. However, the calculated flat-band shift appears to be a non-linear function of thickness. This seems to indicate that the situation is more complicated and either there is additional charge at the substrate interface, or the defects responsible for the fixed charge have a density profile in the insulator. It was not possible to separate these two scenarios in the present experiments.

3.4 Transient characteristics

The carriers emitted from traps or captured in charge traps can be detected as a change in capacitance[xx,xxi]. Generally the capacitance, consisting of an initial capacitance followed by a transient, is given by

$$C(t) = C_0 \left[1 + \sum_{i=1}^{n} \alpha_i \exp\left(-\frac{t}{\tau_i} \right) \right], \tag{3.12}$$

where $C(t)$ is transient capacitance, C_0 is initial capacitance, t is time, τ_i is time constant, and α_i is coefficient which is generally expressed as

$$\left. \frac{dn_T}{dt} \right|_{G-R} = \frac{dp}{dt} - \frac{dn}{dt}$$

$$= (c_n n + e_p)(N_T - n_T) - (c_p p + e_n)n_T, \tag{3.13}$$

where n is the electron density in the conduction band, p is the hole density in the valence band, N_T is the total density $N_T = n_T + p_T$, n_T and p_T is the density of Generation-Recombination (G-R) centers occupied by electrons and holes, c_n, e_p, c_p, e_n is the coefficient of electron capture, electron emission, hole capture, hole emission, respectively as shown in Fig. 3.8 (a)-(d). This model applies generally to semiconductors. In the present case, I have investigated the transient capacitance of the DyScO$_3$ capacitors by using a double-exponential model, which is given by

$$C(t) = C_0 \left[1 + \alpha_1 \exp\left(-\frac{t}{\tau_1} \right) + \alpha_2 \exp\left(-\frac{t}{\tau_2} \right) \right]. \tag{3.14}$$

Eq. (3.14) would apply if there are two separate mechanisms of charge trapping. Fig.

3.9 shows the measured transient characteristics of normalized capacitance during initial application of a 1 MV/cm field and after the field has been switched off, i.e. the trapping and emission characteristics for various film thicknesses. In this measurement, a pulse wave was applied to the capacitor. Upper graph's zero point corresponds to the time when the field was applied. In the lower graph the zero point corresponds to the point in time when the field was turned off. It is clear that the relaxation effect is larger in thinner capacitors in both graphs, although the same field strength was applied in all samples. The relaxation amplitude is at most a few % over few minutes time interval. For further analysis, I have attempted to fit the data with the double-exponential model, as shown in Fig. 3.10 for capture and Fig. 3.11 for emission sequences. In both Figures, the upper graph shows the extracted charge lifetime as a function of thickness, while lower graph shows relative amplitude of an exponential component as a function of thickness. In time constant case, both capture and emission mechanisms have the same values, approximately 6 seconds for the fast time constant, and 60 seconds for the slow time constant. Usually, such time constants are expressed as

$$\tau = \frac{1}{\sigma v_{th} n_T} , \qquad\qquad\qquad (3.15)$$

where σ is capture cross section, v_{th} is thermal velocity, and n_T is each trap density. Traps are usually characterized by their capture cross sections, as shown in Fig. 3.8 (e) – (g). In traditional semiconductors, electron traps with cross sections in the range of 10^{-14} to 10^{-12} cm^2 are usually *'Coulomb-attractive traps'*, i.e., the trap centers are positively charged prior to electron capture. Electron traps with cross sections in the 10^{-18} to 10^{-14} cm^2 range are usually due to *'Coulomb neutral traps'*, and those with cross sections smaller than 10^{-18} cm^2 are usually associated with *'Coulomb-repulsive traps'*, i.e., the trap centers are already negatively charged prior to electron capture. In Section 3.3, trap charge in a particular capacitor had positive charge, which would lead to the interpretation that these traps are the so-called *'Coulomb-attractive traps'* with an area of at least 10^{-14} cm^2. These measurements were performed at room temperature and the time constant can therefore be directly connected to capture cross section, which is given by

$$\tau \propto \frac{1}{\sigma} . \qquad\qquad\qquad (3.16)$$

Considering Eq. 3.16, the capture cross section for trap filling is the same as that for emission from traps since all time constants for all thicknesses are similar. The amplitude coefficients correspond to the amount of charge that is involved in a

particular trapping mechanism. As shown in Fig. 3.10 (b) for capture and 3.11 (b) for emission, thinner capacitors have larger amount of charge although the same field was applied, as mentioned earlier. The amount of charge appears to increase linearly in thinner capacitors, strongly suggesting that this charge is near or at the interface between $DyScO_3$ and $SrTiO_3$, as expressed in Fig. 3.7 (b). I concluded in Section 3.3 that there are fixed oxide charges in the insulator and possibly mobile ionic charge or oxide trapped charge. Considered coefficient linearity, the faster time constant mechanisms appear to relate to fixed oxide charge, and the slower relaxation component to mobile ionic charge, which is different from the oxide trapped charge. Linearity of amplitude with thickness still suggests that charge movement remains close to the interface. Why mobile ionic charge exists around the interface? A possible answer is as follows; As these positively charged mobile ions drift close to the interface between substrate and insulator, they repel holes from, and attract electrons to, the substrate surface, often causing unwanted surface electron current to flow among n^+ diffusion regions in a substrate. We could also think this trap center is not deep level but shallow level since time constant of capture and that of emission is almost the same, and both charges have similar magnitudes.

Finally, I have compared this result with transient characteristics that have been observed in FET I_{DS} characteristics. Fig. 3.12 (b) shows the charging transient characteristics of drain current under 0.5 V for drain bias and 2 V for gate source bias for a $DyScO_3/SrTiO_3$ FET device. Fig. 3.12 (a) shows a schematic illustration of this FET structure. This transient also has a faster, 7-second time constant and a very slow 100-second order process. The channel current decreased to around 50 % within about 100 seconds. In my case, both relaxation amplitudes showed a change that was at most 1%. There are fixed oxide charge and mobile ionic charge around the interface. Presumably in an FET device there is a strong change in charge distribution on the intrinsic $SrTIO_3$ side of the interface, which can not be seen directly in the present capacitor structures that were grown on heavily Nb-doped substrates.

3.5 Conclusions

In Sections 3.1 and 3.2, it was shown that capacitance measurements are consistent with the presence of an interface layer with a thickness between 0.8 nm to 2.8 nm. The bulk dielectric constant of $DyScO_3$ was derived from the thickness dependence of capacitance, giving a value of 21.4. A similar value was obtained from two types of

analysis, a simple two-layer model and from the assumption that the quadratic factor of a bias scan follows a general 'voltage linearity' shape, as explained in Section 3.2. Also in Section 3.2, the presence of oxide fixed charge near or at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ and mobile ionic charge in the $DyScO_3$ were indicated. In transient analysis Section 3.4, this fixed oxide charge was shown to have a relaxation time of about 6 seconds, while mobile ionic charge responded much more slowly, with a time constant of 80 seconds. Both trapped centers had at least 10^{-14} cm^2 area of capture cross section, which would correspond to *'Coulomb attractive traps'* in a traditional semiconductor picture. These trap level were found to be relatively shallow. In summarizing this section, there is both fixed trapped charge and mobile ionic charge in Al /$DyScO_3$ /Nb-doped $SrTiO_3$ capacitors, as shown in Fig. 3.13 (a) and (b). These effects can strongly affect the performance of field-effect devices and it is clearly necessary to carefully control the stoichiometry of the insulator, both in terms of cations and oxygen in order to reduce charge trapping and charge injection into the insulator interface layer.
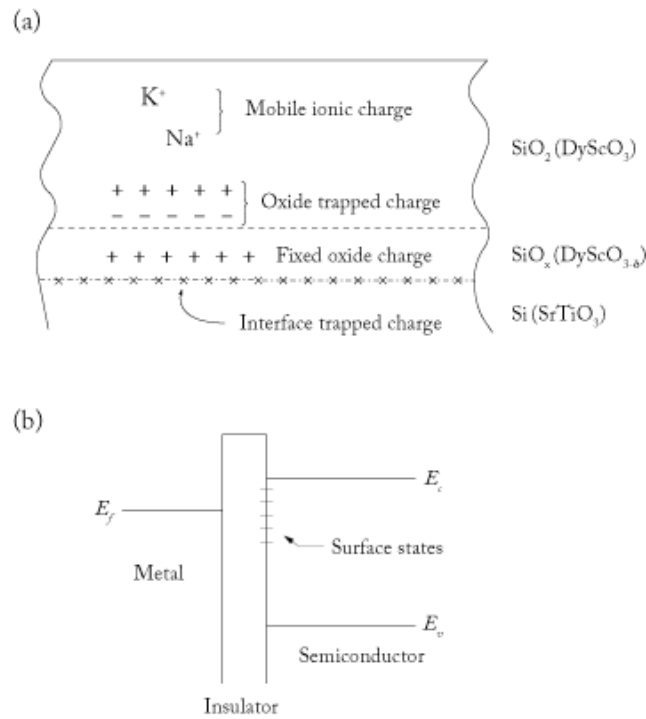
Fig. 3.1 (a) Charges and their location in thermally oxidized silicon. These charges can be applied to oxide heterostructure, like the interface between $SrTiO_3$ and $DyScO_3$. (b) Schematic energy band diagram of a Metal Insulator Semiconductor structure, illustrating the presence of of surface (interface) states.
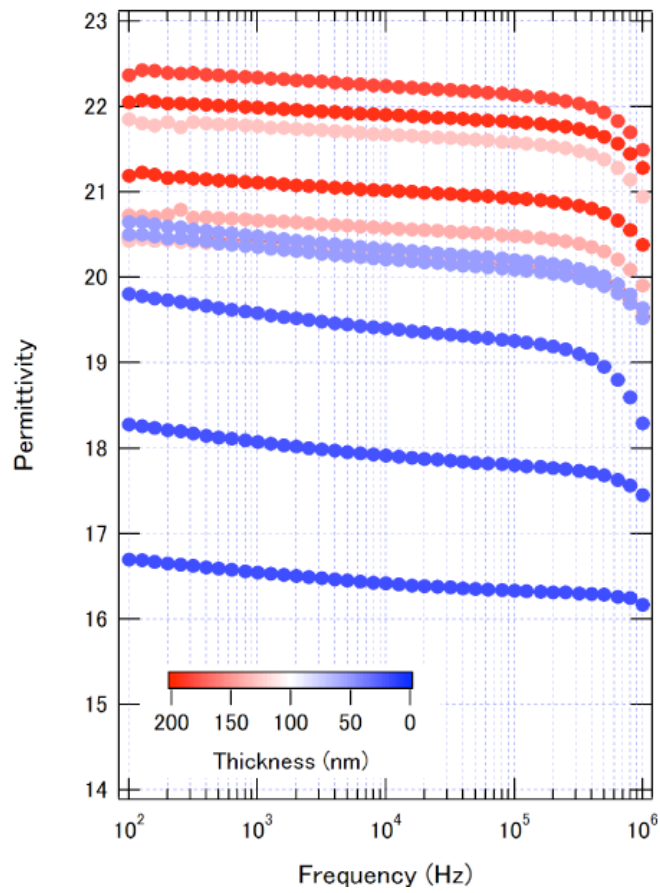
Fig. 3.2 Frequency dependence of dielectric constant (permittivity) as a function of insulator (DyScO$_3$) thickness. This measurement was conducted at zero applied bias and at room temperature.
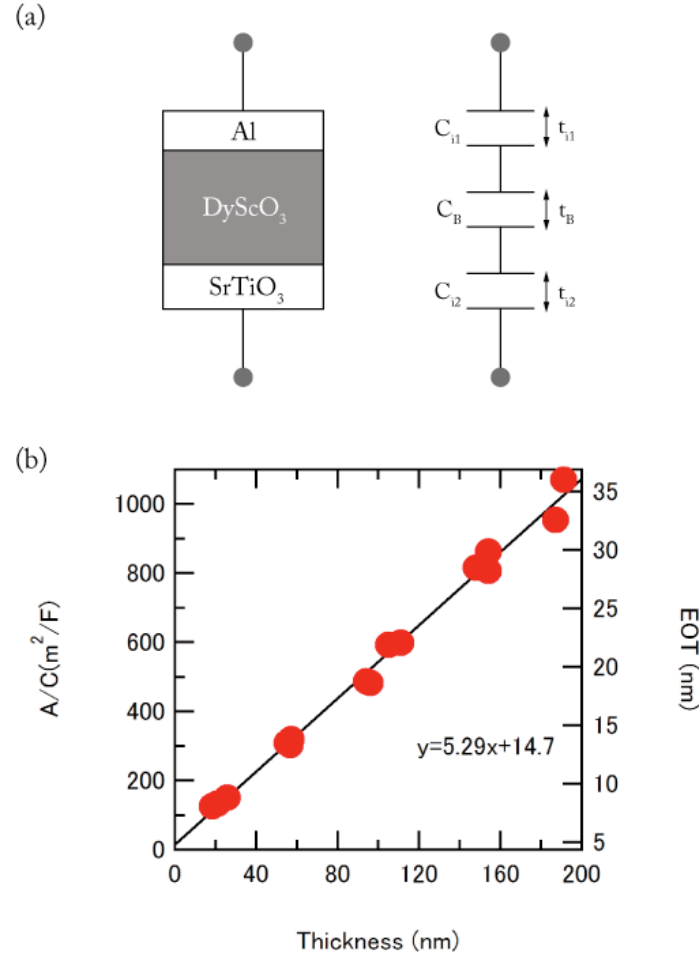
(a)

(b)

Fig. 3.3 (a) Schematic diagram of a two-layer capacitor model. Left figure shows a drawing of the capacitor structure, while right diagram shows the equivalent circuit of this capacitor structure. C_B and t_B are the bulk capacitance and thickness, C_{i1} and t_{i1} are the Al / DyScO$_3$ interface layer capacitance and thickness, and C_{i2} and t_{i2} are the DyScO$_3$ / SrTiO$_3$ interface capacitance and thickness, respectively. (b) Thickness dependence of the reciprocal zero bias capacitance density for Al /DyScO$_3$ /Nb-doped SrTiO$_3$ stacks with Equivalent Oxide Thickness (EOT) at 100 kHz.
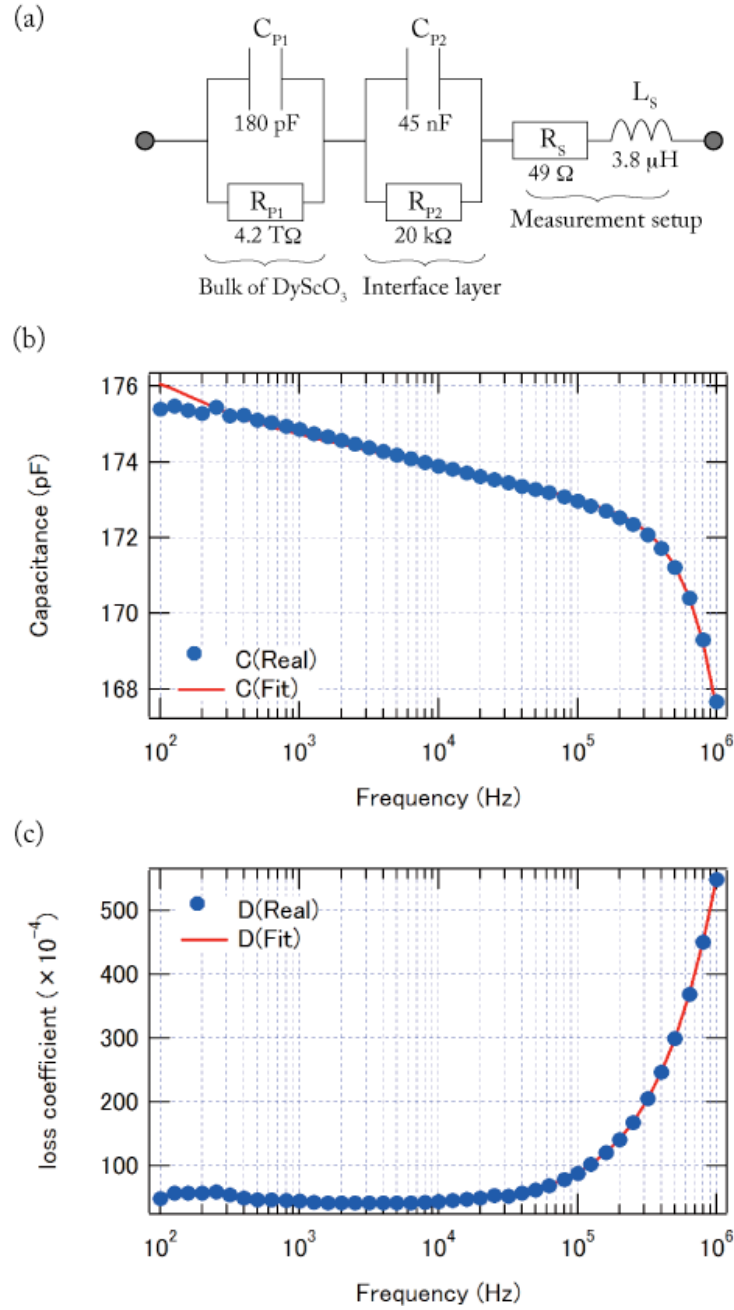
Fig. 3.4 (a) Equivalent circuit of realistic capacitor measurement model. Left side parallel circuit represents bulk, middle part corresponds to the interface between DyScO₃ and SrTiO₃, and right part models the measurement setup, i.e. contact resistance and cable inductance. Numerical values show fitting results. Frequency dependence of zero bias (a) capacitance and (c) loss coefficient (*tan δ*). Continuous lines are the fitting results.
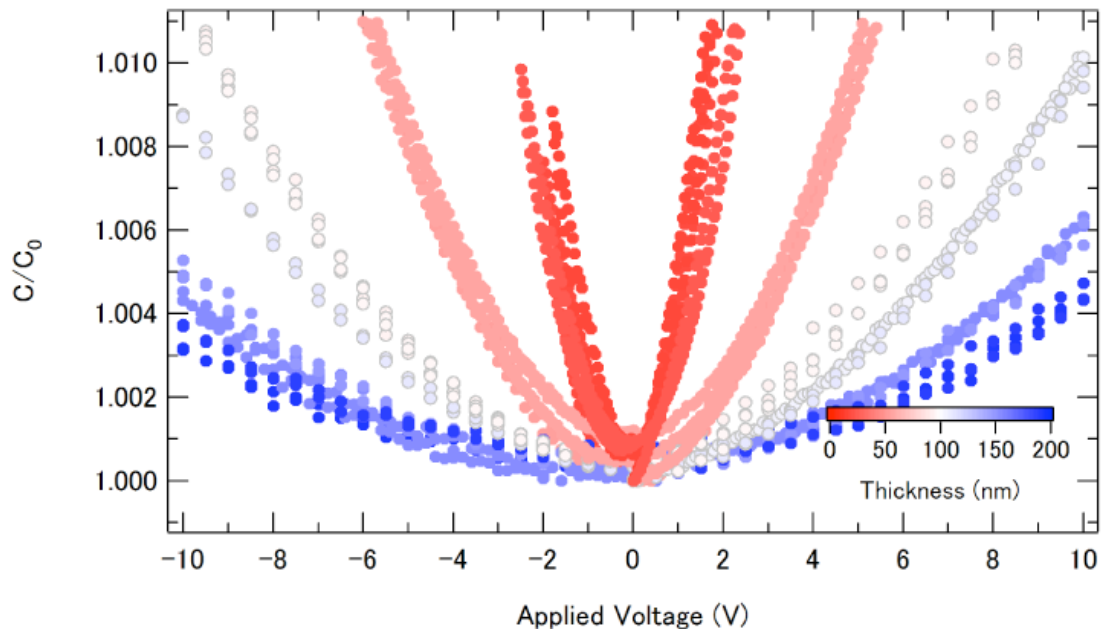
Fig. 3.5 Thickness dependence of normalized capacitance as a function of applied voltage. The sample were Al /DyScO$_3$/ Nb-doped SrTiO$_3$ Metal Insulator Semiconductor (MIS) capacitor.
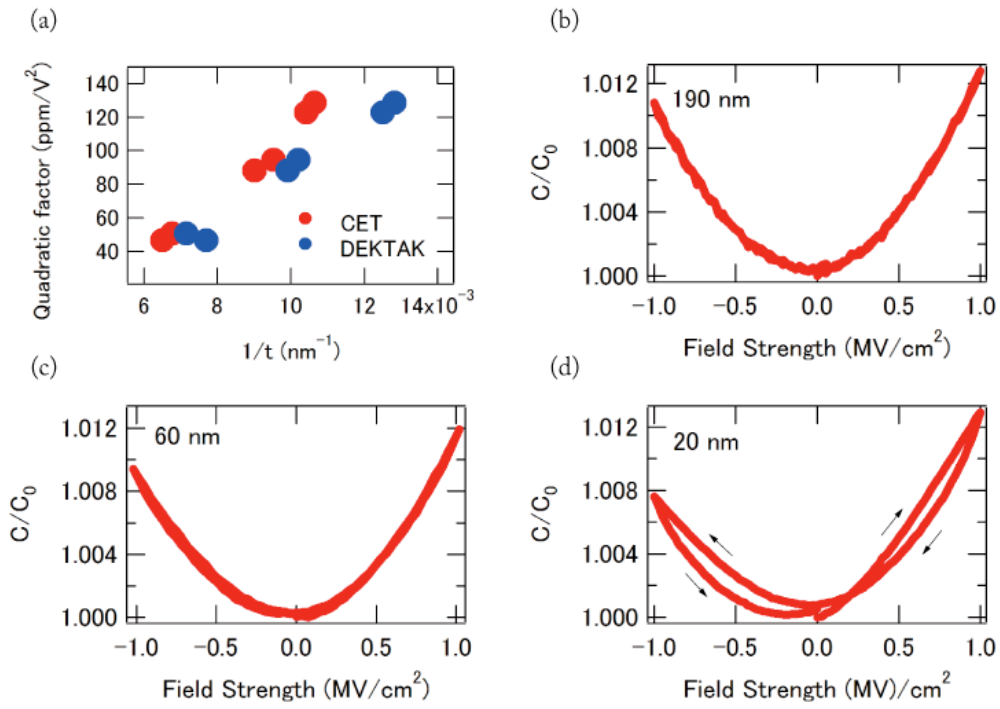
Fig. 3.6 (a) The experimental and simulating result of quadratic factor (α) as a function of $1/t$ for DyScO₃ capacitors, where Capacitance Equivalent Thickness (CET) was assumed that the 190 nm of α was fixed. Normalized capacitance as a function of field strength with thicknesses of (b) 190 nm, (c) 60 nm, and (d) 20 nm.
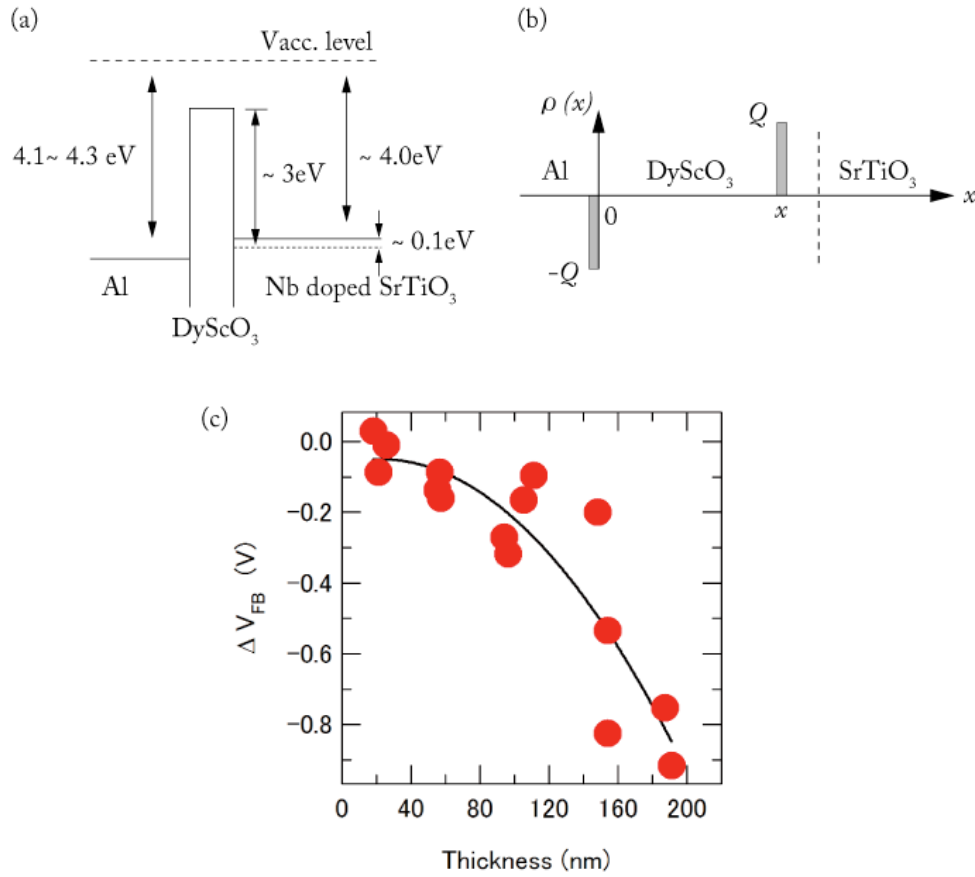
Fig. 3.7 (a) Energy band diagram of Al /DyScO₃ /Nb doped SrTiO₃. Theoretical flat bad voltage equals the difference between Nb-doped SrTiO₃ and Al metal work functions. (b) Schematic illustration of the effect of a sheet charge of areal density Q within the insulator layer of an MIS capacitor biased at flat band conditions. (c) Thickness dependence of the flat band voltage shift in Al /DyScO₃ /Nb-doped SrTiO₃ capacitors.
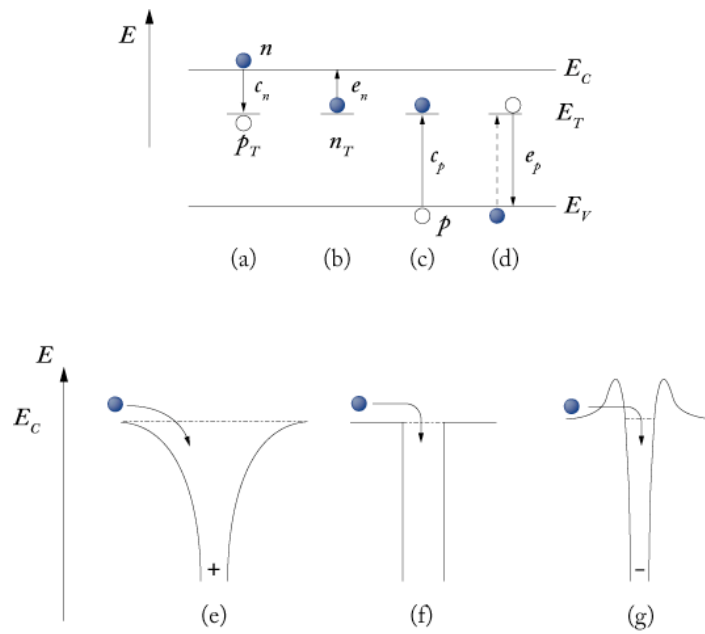
Fig. 3.8 (a) - (d) Electron energy band diagram for a semiconductor with deep-level impurities. The capture and emission processes are described in text. Schematic illustration of the potential wells of electron traps in $DyScO_3$: (b) Coulomb-attractive trap where the trap center is positively charged, (c) neutral trap with a neutral trap center, and (d) Coulomb-repulsive trap which is negatively charged. Dotted lines are capture cross sections.
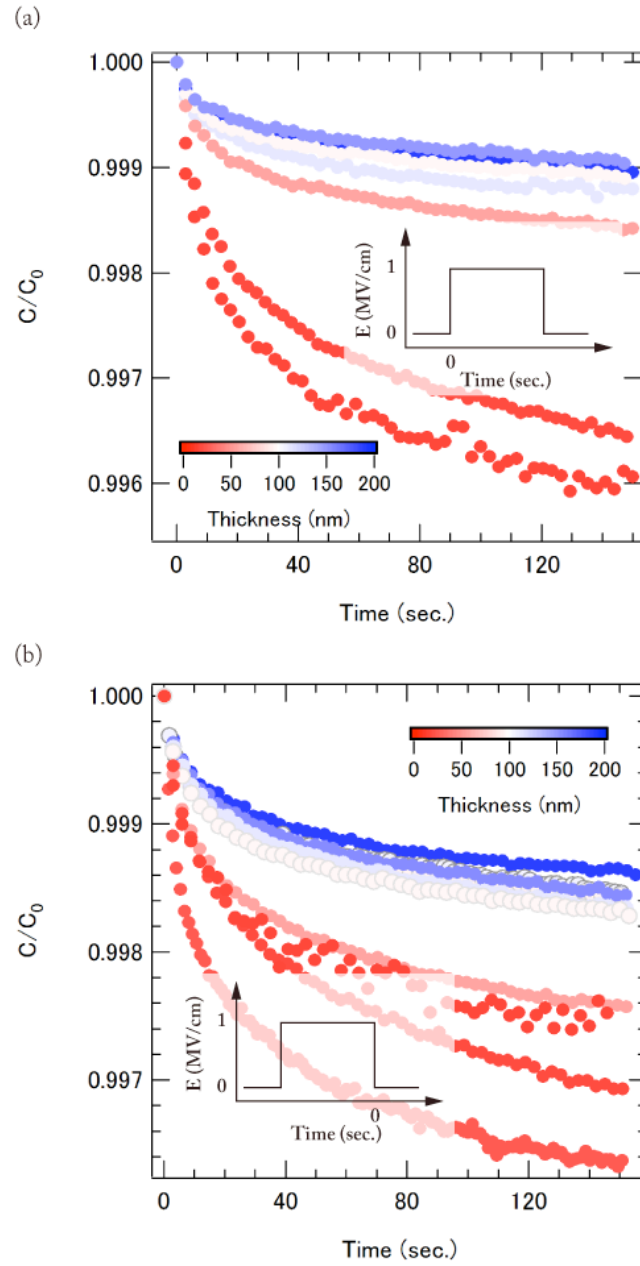
Fig. 3.9 Transient characteristics of normalized capacitance under 1 MV/cm field for charging (a) and emission under zero bias (b) as a function of insulator thickness. Pulse wave was applied to capacitor. Zero time corresponds to the switching on (a) or switching off time (b).
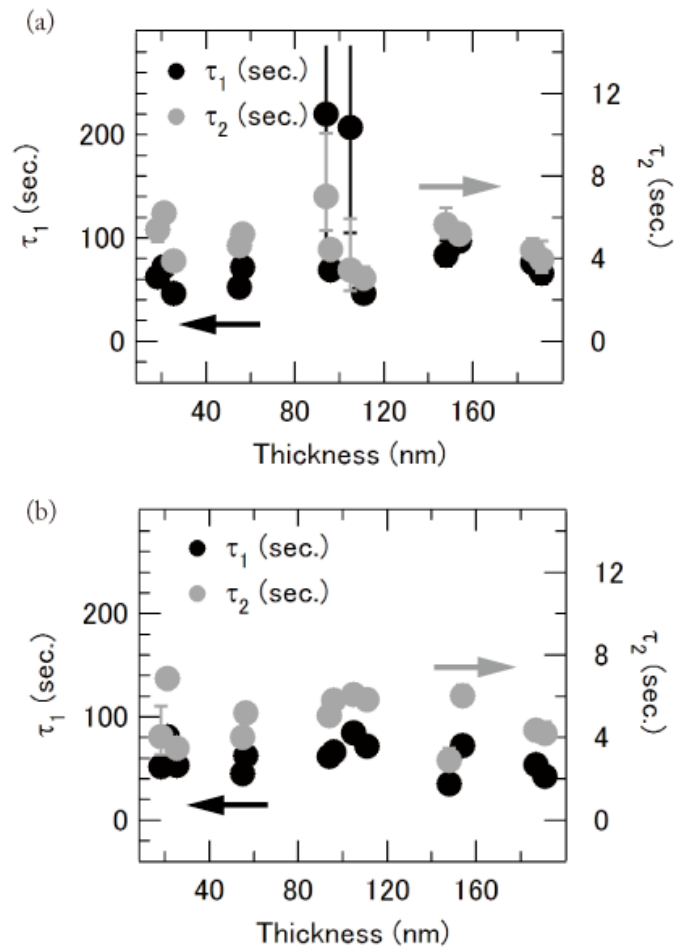
Fig. 3.10 Double-exponential fitting results of charging transient characteristics. (a) Time constants as a function of thickness and (b) exponential component amplitude as a function of inverse thickness.
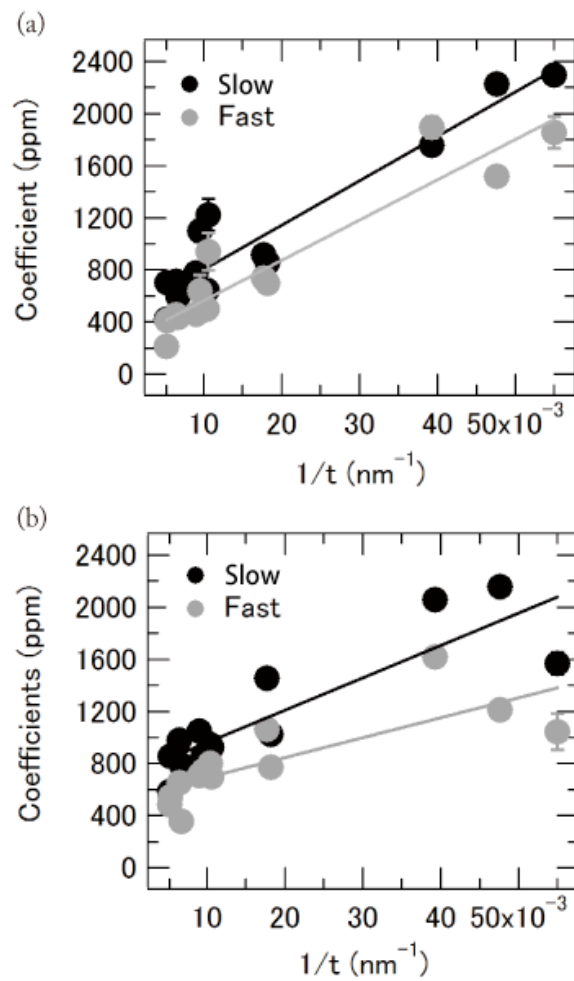
Fig. 3.11 Double-exponential fitting results of emission transient characteristics. (a) Time constants as a function of thickness and (b) amplitude coefficients as a function of inverse thickness.
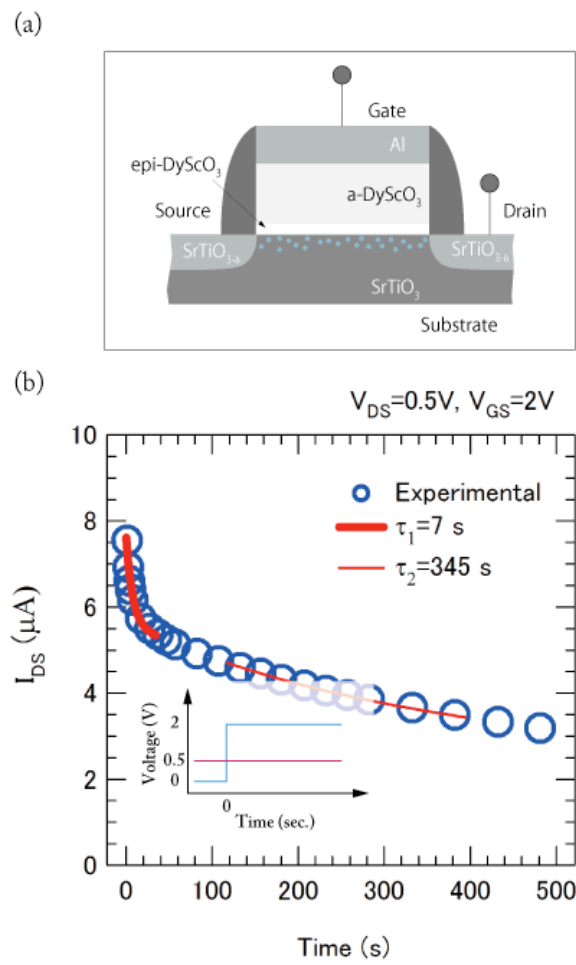
Fig. 3.12 (a) Schematic diagram of measurement FET. (b) Channel current transient characteristics of under 0.5 V drain bias and 2 V for gate source bias.
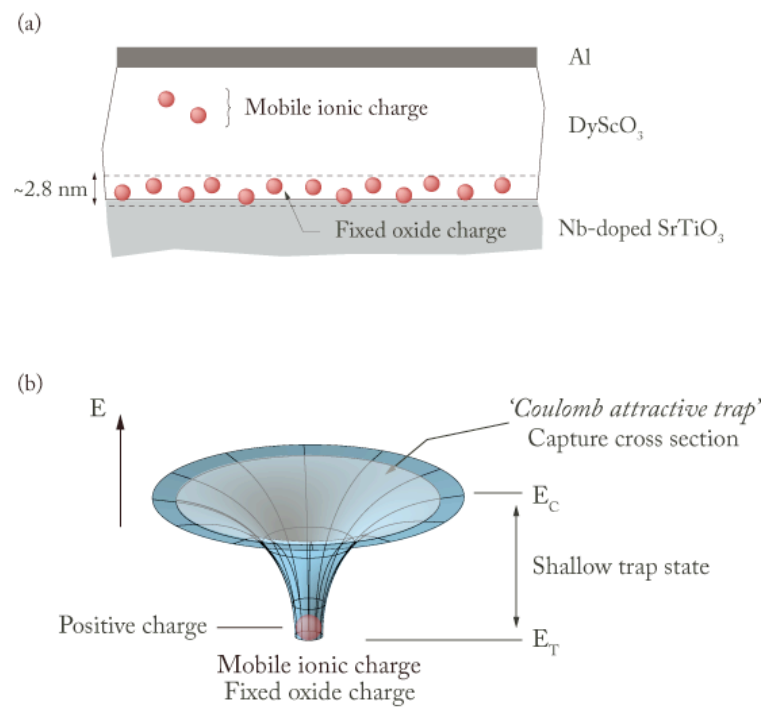
Fig. 3.13 (a) Charges and their location in Al/DyScO$_3$/Nb-doped SrTiO$_3$ MIS capacitors. (b) Schematic illustration of "*The Coulomb Attractive Traps*" type potential wells in real DyScO$_3$

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Chapter 4

Conduction mechanisms of Al/DyScO$_3$ /Nb-doped SrTiO$_3$ MIS capacitors

In practical MIS capacitors, there are always several carrier transport mechanisms. Some mechanisms, such as direct tunneling, appear when the insulator layer is very thin. Most other mechanisms relate in some way to defects in the insulator, such as thermally activated hopping, Generation-Recombination (G-R) center related transport, and others. A list of various mechanisms, together with characteristic leak current equations is given in Table 4.1[i]. In a real device, it is common to have several competing mechanisms. In this Chapter my aim is to determine the dominant leak mechanisms in the temperature and bias ranges that are relevant for oxide field-effect devices. In the previous Chapter, the presence of an interface layer with a thickness of at most 2.8 nm was deduced, based on a two-layer model. In the field-effect Section, it was shown that oxide fixed charge exists near or at the interface between DyScO$_3$ and Nb-doped SrTiO$_3$ and that mobile ionic charge is present in the DyScO$_3$ insulator. In transient characteristics, this fixed oxide charge had a relatively fast relaxation time constant of 6 seconds, while mobile ionic charge had a much slower response, at about 80 seconds. Trapped centers had at least 10^{-14} cm^2 capture cross section, and were assumed to be 'Coulomb attractive traps'. It was also suggested that this trap level appears to be shallow in DyScO$_3$. In this Chapter, I attempt to correlate

the various conduction mechanisms with the results presented in Chapter 3 and discuss how the conduction mechanisms change with temperature and affect field-effect devices.

4.1 Temperature dependence of leakage current

Fig. 4.1 shows typical current density vs. field strength characteristics as a function of temperature for a 48 nm thick $Al/DyScO_3/Nb$-doped $SrTiO_3$ MIS capacitors. The true insulator thickness was determined by using Capacitance Equivalent Thickness (CET), which was calculated from the measured capacitance assuming a permittivity of 21.4 and a pad area of 0.00036 cm^2, as was explained in the previous Chapters. Temperature was changed from 274 K to 4 K. The current density was a strong function of electric field and temperature. It is immediately clear from the curve shape, that no single leak mechanism describes the whole field dependence curve. Competing contributions are overlapping, but different mechanisms dominate in low and high field regions. Decreasing temperature did not change the basic curve shape, but did result in a monotonic drop of current. This is a strong indication that there were thermally activated carriers in the insulator. Thermally activated current in the insulator implies that charge can be injected into the insulator under relatively high bias. This may affect the field-effect transistor threshold voltage shift below 100 K. A possible scenario is that the threshold voltage of a FET shifted since carriers were prevented from accumulating at the interface between $DyScO_3$ or $CaHfO_3$ and $SrTiO_3$ because the presence of charge in the insulator reduced the effective field strength in the transistor channel. In order to accumulate a sufficient number of carriers for a metallic channel to form, a higher electric field had to be applied. Leak behavior was quite different at low and high fields. Under high field (~2MV/cm), the current density dropped by only one order of magnitude when the device was cooled from 300K to 4K. This change increased to three orders of magnitude at low electric field (~0.5 MV/cm). For further investigation of this thermally activated conduction at various field strengths, Arrhenius plots were examined. The derivation of an Arrhenius plot is the following. Usually, current density J is given by

$$J = qnv , \qquad\qquad (4.1)$$

where q is the electronic charge, n is the carrier density, and v is the carrier velocity, which is related to carrier mobility. Although both carrier density and mobility can be

thermally activated, from the point of view of an Arrhenius plot, the usual expectation is that one or the other dependence dominates the current density temperature dependence. For example, assuming that carrier velocity is close to saturation, it can be considered a constant in this case. Due to that, current would be proportional to carrier density, which can be expressed as

$$J \propto n = n_0 \exp\left(-\frac{E_a}{k_B T}\right), \tag{4.2}$$

where n_0 is a constant, E_a is the activation energy, k_B is the Boltzmann constant, and T is the operating temperature. Thus, an Arrhenius plot is obtained by plotting $\ln(J)$ vs. $1/T$ since

$$\ln(J) = -\frac{E_a}{k_B T} + J_0, \tag{4.3}$$

where J_0 is constant. If J is thermally activated, data points in an Arrhenius plot would fall on a straight line, where the slope gives the activation energy, E_a.

Fig. 4.2 (b) shows the Arrhenius plot of the temperature-dependent leakage current density for a $DyScO_3$ capacitor. Inset in the figure shows the high-temperature range for T>160 K. There several distinct activation energies for the high-temperature regime (160K~274K), middle-temperature regime (60K~160K), and low-temperature regime (~60K). It strongly indicates that three different conduction mechanisms were dominant in each temperature range, as shown in Fig. 4.2 (a). Only at the lowest field of 0.5 MV/cm, there was no distinct high-temperature region. As the fitting results in Fig. 4.2 (a) show, the activation energy in the medium temperature range is ten times larger than at lower temperatures. Above 60K, there is also a slight field dependence, with the activation energy decreasing at higher fields by a factor of about two. This appears to indicate that a field-dependent conduction mechanism is involved. Especially at higher fields, there was no detectable slope in Arrhenius plots at high temperature. This shows that carrier mobility saturated and any activated processes that do exist in the insulator, only become significant below 160 K. This, incidentally, is the same temperature range where threshold shifts tend to prevent the operation of amorphous insulator FETs based on $CaHfO_3$. In next section, I have determined which conduction mechanisms were dominant at each electric field in the three different temperature ranges.

4.2 Conduction mechanisms

In this section, I have investigated this carrier transport strictly for further analysis. Before analysis, I will explain each conduction mechanisms. Theoretically, in an ideal MIS capacitor the conductance of the insulating film is assumed to be zero, since the film should be an insulator. But realistically, the insulators have some value of carrier conduction under high field, at high temperature, or when the insulator becomes very thin. To estimate the field effect in $DyScO_3$ insulator under bias, it is necessary to account for the difference of electric fields in the insulator and in the substrate. Oxide charges can be neglected if the flat-band voltage shift and the substrate band bending Ψ_S are much smaller than the applied voltage. The substrate can also be considered to be almost metallic, since I have used heavily Nb-doped $SrTiO_3$. Under these assumptions, the electric field in the insulator is given by

$$E_I = E_S\left(\frac{\varepsilon_S}{\varepsilon_i}\right) \approx \frac{V}{d} , \qquad (4.4)$$

where E_I and E_S are the electric fields in the insulator and the substrate, and ε_i and ε_S are the corresponding dielectric constants. Table 4.1 summarizes the basic conduction processes in insulators. It also emphasizes the voltage and temperature dependence of each process that can be used to identify the precise conduction mechanism empirically. Here I will briefly explain each of these carrier transport mechanisms.

Tunneling is the most general conduction mechanism through insulators, especially under high fields. The tunnel emission could be expressed quantum mechanically by considering electron wave function on either side of the insulator penetrate through the potential barrier. Tunneling has a strong dependence on the electric field, but is essentially independent of temperature. Tunneling could be also divided into direct tunneling and field-enhanced type, the latter is the so called Fowler-Nordheim tunneling[ii], where carriers tunnel through only a partial width of the barrier because the effective barrier height has been modified by the applied field, as shown in Fig. 4.3 (a). When the insulator layer is extremely thin, tunneling behavior increases such that the conduction approaches that of the top and bottom electrode contact where the barrier is measured at the substrate (bottom electrode) surface instead of the insulator, and the thermionic emission current is multiplied by a tunneling factor. But this only happens in the case of very thin insulators and does not apply to the materials like $DyScO_3$, where the capacitor thicknesses are generally larger than 10 nm. It is therefore possible to limit

discussion to only Fowler-Nordheim tunneling in such capacitors.

Schottky emission is another thermionic emission mechanism, where electrons are excited over the metal-insulator barrier or the insulator-substrate barrier. As shown in Table. 4.1, the term subtracting from ϕ_B is due to image-force lowering which is the image-force-induced lowering of the barrier energy for charge carrier emission in the presence of an electric field like Poole-Frenkel type, as I will explain next subsection. A plot of ln[J(V)] vs. 1/T yields a straight line with a slope determined by the barrier height, as shown in Fig. 4.3 (b).

The Poole-Frenkel emission[iii,iv], which is illustrated in Figs. 4.3 (c) and (d), is a classical mechanism in which the electron is thermally emitted over the top of a potential barrier which has been lowered by the presence of an electric field into the conduction band. The supply of electrons from the traps is through thermal excitation and field-enhancement. For trap states with Coulomb potentials, as shown in Fig. 4.3 (d), it is similar to that of Schottky emission. The barrier height, however, is the depth of the trap potential well. The barrier reduction is larger than in the case of Schottky emission by a factor of 2, since the barrier lowering is twice as large due to the immobility of the positive charge. As discussed in Section 3.3, such positive charge is present in the $DyScO_3$ insulator and, consequently, the leak current appears to be dominated by this type of transport. As is shown in Fig. 4.3 (d), for a Coulombic potential in an electric field F aligned in the $-z$ direction, the potential can be written as

$$V(r) = \frac{-q^2}{4\pi\varepsilon_S\varepsilon_0 r} - qFr\cos\vartheta,\qquad(4.5)$$

where $V(r)$ is the potential as a function of r, and ε_r is the relative dielectric constant of the host insulators. For $0<\theta<\pi/2$ there is a well-defined potential minimum found by setting $\delta V\delta/r$ at $r = r_{max}$:

$$r_{max} = \left(\frac{q}{4\pi\varepsilon_S\varepsilon_0 F\cos\vartheta}\right)^{1/2}.\qquad(4.6)$$

The charge in the potential barrier due to the presence of the field is found by evaluating $V(r)$ at $r = r_{max}$,

$$\delta E_i = V(r_{max}) - q\left(\frac{qF\cos\vartheta}{\pi\varepsilon_S\varepsilon_0}\right)^{1/2},\qquad(4.7)$$

where E_i is the ionization energy of the trap level and δE_i is the field-induced energy. Frenkel's one-dimensional result is given by setting $\theta = 0$[v].

At low field and high temperature, current is transferred by thermally excited electrons hopping from one isolated state to another state[vi]. This mechanism yields an Ohmic characteristic exponentially dependent on temperature, as shown in Table 4.1.

Ionic conduction is similar to a diffusion process. The direct current (DC) ionic conductivity decreases during the time that the electric field is applied because ions cannot be readily injected into or extracted from the insulator, as I showed in C-V stress measurements. After an initial current flow, positive and negative space charges will build up near the metal-insulator and the substrate-insulator interfaces, causing a distortion of the potential distribution. When the applied field is removed, large internal fields remain which cause some, but not all, ions to flow back toward their equilibrium position. Due to that, hysteresis results in I-V and C-V sweeping traces. Since measurement in this thesis have been done by stepping the electric field to positive direction from zero to around 2 MV/cm with a step rate of 0.02 V/ 0.23 sec., it is unlikely that ions can respond so quickly. Due to this, the ionic conduction mechanism could be discounted.

The space-charge-limited current (SCLC) model has been developed and used with great success since 1960s[vii,viii]. The basic SCLC equation is sown in Table 4.1. It has been reported that ultra-high vacuum annealing increases the trap density of oxide film due to an increase of oxygen deficiency, enhancing the leak current density, e.g. in case of SiO_2[ix]. On the contrary, decrease of leak current with in the presence of high oxygen deficiency, which can induce large oxide trap density, has been reported[x]. This behavior has been explained well by using the SCLC theory. The reasoning is that a high trap density prevents the movement of the quasi-Fermi level in the band gap of the insulator upon carrier injection. At steady-state injection, the quasi-Fermi level of the insulator is determined by trap characteristics, such as the trap density, trap levels, and the number of trapped carriers. Due to that, when the insulator has a large trap density at concentrated energy levels in the energy band gap, some of the injected electrons are captured but the position of the quasi-Fermi level remains practically constant at the concentrated energy levels until all the traps are filled. In the SCLC mechanism, shallow and deep trap levels are defined by this quasi-Fermi level[xi]. Shallow trap levels are above the quasi-Fermi level. As the carrier injection increases, the quasi-Fermi level shifts higher and gradually the in-gap trap levels become less effective in reducing current flow. Thus, SCLC conduction is affected by a distribution of trap energy levels

as well as trap level density, which is often described with an exponential distribution model[xii]. A similar SCLC model with exponential trap distribution was used in this work. Exponentially distributed traps are characterized by two parameters, namely trap density N_t and a characteristic constant of the distribution T_C, through the expression

$$N(E) = \frac{N_t}{k_B T_C} \exp\left(\frac{E - E_C}{k_B T_C}\right),$$

(4.8)

where $N(E)$ is the trap concentration per unit energy range at an energy (E) below the conduction band edge, E_C is the conduction band edge energy. The current density J for the exponential trap distribution case of SCLC is given by

$$J = \frac{q\mu N_C}{2L} V \left(\frac{2\varepsilon_i}{qL^2 N_t} V\right)^{T_C/T},$$

(4.9)

where q is the electronic charge, μ is carrier mobility, N_C is the density of states in the conduction band, V is the applied voltage, L is the insulator thickness, ε_i is the dielectric constant of the insulator, and T is the temperature. When T_C/T is abbreviated as n, we could obtain a more simple expression in the form of a power law for the applied voltage

$$J(T,V) \propto aV^{n+1},$$

(4.10)

$$n = \frac{T_C}{T},$$

(4.11)

where a is a constant. I have tried to fit the MIS capacitor leak data with this equation. Also, the space charge could be determined by the injected carriers giving rise to the Poisson equation of the form

$$\frac{d^2\psi_S(x)}{dx^2} = \frac{qN(E)}{\varepsilon_i}.$$

(4.12)

Integrating Eq. (4.12) from the electrode to the substrate is again given by Eq. (3.9). This surface potential ψ_S is equal to the applied voltage. Thus, the number of carriers occupying deep Generation-Recombination (G-R) centers increases at higher applied bias voltage.

Each conduction process may dominate in a certain temperature and voltage range. The processes are also not quite independent of one another since there are possibilities of complex mechanisms. Because of this, leak current behavior should be carefully

examined but it may still not be possible to give a unique answer as to which processes are present. Fig. 4.4 shows the same leakage current data as was shown in Fig. 4.1, but plotted in a Poole-Frenkel plot (Fig. 4.4(a)) and as a Schottky plots (Fig. 4.4(b)). The dotted lines correspond to the best fit to experimental results following each conduction mechanisms. Usually, the Poole-Frenkel emission and Schottky emission could be expressed as shown in Table 4.1, but the basic expressions have often been expanded in the following way

$$J = \sigma(0)E \exp\left(\frac{-q(\phi_B - n\sqrt{qE/\pi\varepsilon_i})}{k_B T}\right), \qquad (4.13)$$

$$J = A^*T^2 \exp\left(\frac{-q(\phi_B - n\sqrt{qE/4\pi\varepsilon_i})}{k_B T}\right), \qquad (4.14)$$

where $\sigma(0)$ is the low-field conductivity, ϕ_B is a barrier height, and n is the expanding constant. Generally, the n in Schottky emission is determined as 1. For Poole-Frenkel emission various values between 1 and 2 are commonly used[xiii]. Theoretically, n should be around 1, so I have used $n = 1$ as a starting value in the fitting. As shown in Fig. 4.4 (a), for the current density divided by electric field characteristics, a linear relationship exists in a relatively low electric field regime ($E^{0.5}$ between 0.2 and 0.8), but only above 60 K. The temperature limit is partly caused by the current dropping below the semiconductor parameter analyzer's noise limit, resulting in a noisy cut-off of the low-field data at about 10^{-8} A/cm^2. At 274 K, n could be determined to be 0.88, while at 90 K, n was 0.8. These values are close to 1, which is the theoretical value, suggesting that in this field region, the dominant mechanism is Poole-Frenkel conduction. On the hand, in Schottky emission case, n was determined to be 3.8 at 252K and 1.6 at 90 K in very low electric field region, indicating that this type of emission was not significant in the insulator. In the Poole-Frenkel region, the activation energy was around 0.2 eV, which should thus correspond to the field-modified depth of the trap sites. A similar energy of 0.23 eV was obtained from Fig. 4.3 (d) and Eqs. 4.5-7.

Fig. 4.5 shows the leak current characteristics in (a) Space-Charge-Limited current plots and (b) Fowler-Nordheim plots as a function of temperature. The inset in the upper graph shows Ohm's law plots. Experimental results can be compared with the fitting results, shown with dotted lines. In Fowler-Nordheim plots, I have used the equation as shown in Table 4.1. In this equation, I have used the known values of the electron effective mass $m_e^* = 0.4 m_e$, where m_e is the free electron mass[xiv,xv]. In a log (J/E^2) vs.

(1/E) plot of the leak current of this capacitor, a linear region appears in the high electric field regime (1~2 MV/cm), as predicted by Table 4.1 tunneling model. It is also evident that at high temperatures the slope goes flat, suggesting that this tunneling conduction mechanism vanishes. From the slope at 4K, I could get a 0.16 eV barrier height. Considering that the activation energy was approximately 0.01 eV in the 1 to 2 MV/cm field range above 60 K, the barrier height also suggests that there was almost no Schottky emission. In Space-Charge-Limited current case, a plot of ln(J) vs. ln(V) showed a power law relationship in the high-field region, suggesting that a SCLC with exponential trap distribution model might also be applicable. As I mentioned above, this SCLC is related to Generation-Recombination process. If so, the traps responsible for the SCLC behavior should also be correlated with soft breakdown, as shown in Fig. 4.6 (a). In Ohmic conduction case, as shown in Fig. 4.5 (a), a plot of ln(J) vs. ln(V) indicates that for very low fields (0-0.5 V) and at high temperature (above 184 K as shown in Fig. 4.5 inset), the relationship is Ohmic. This could be due to electronic conduction by a hopping mechanism, where there is a thermal excitation of trapped electrons from one isolated trap site to the next. It also suggested that there must be very shallow trap sites in the insulator. The various mechanisms that were identified for various temperature and field combinations are summarized in Fig. 4.6 (b).

4.3 Conclusions

In this chapter, I have investigated the conduction mechanisms in a 48 nm Al/ $DyScO_3$/ Nb-doped $SrTiO_3$ MIS capacitor. Current density vs. electric field characteristics had large temperature dependence, suggesting that this insulator has thermally excited carriers. Thus, it is reasonable to conclude that charge injection into the insulator results in FET threshold voltage shift at low temperature. Temperature and electric field dependence of conduction mechanisms were summarized in Fig. 4.6 (b). In the high-field regime (1 MV/cm~) and below 160 K, Fowler-Nordheim tunneling could be seen with a 0.16 eV barrier height between $DyScO_3$ and Nb-doped $SrTiO_3$. In high-field (1 MV/cm~) and high temperature (from 160 K to 274 K) regime, however, Space-Charge-Limited current appeared to be dominant, resulting in a lower current density. In a medium field range (0.5~1 MV/cm) at high temperature (from 60 K to 274 K) case, Poole-Frenkel emission was dominant, with a 0.02 eV barrier height and a 0.23 eV of trap level. Below 60 K, no activation energy was seen. In this region, tunneling conduction could be relatively high. In the low-field regime (~0.5 MV/cm), Ohmic

conduction mechanism could be seen, suggesting that shallow, 0.02 eV trap state exist and resulting in thermally excited hopping.

Table 4.1 Basic carrier transport processes in insulators. J is carrier density, E is electric field, q is electron charge, ε_ι is insulator permittivity, m^* is effective mass, A^{**} is effective Richardson constant, ϕ_B is barrier height, d is insulator thickness, ΔE_{ac} is activation energy of electrons, ΔE_{ai} is activation energy of ions, V is applied voltage which is equal to Ed. b, c, and d' are constants (Ref. 1).

Process	Expression	Voltage and Temperature dependence
Tunneling	$J \propto E^2 \exp\left[-\dfrac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right]$	$\propto V^2 \exp\left(\dfrac{-b}{V}\right)$
Thermionic emission	$J = A^{**}T^2 \exp\left[\dfrac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right]$	$\propto T^2 \exp\left[\dfrac{q}{kT}\left(a\sqrt{V} - \phi_B\right)\right]$
Poole–Frenkel emision	$J \propto E \exp\left[\dfrac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right]$	$\propto V \exp\left[\dfrac{q}{kT}\left(2a\sqrt{V} - \phi_B\right)\right]$
Ohmic	$J \propto E \exp\left(\dfrac{-\Delta E_{ac}}{kT}\right)$	$\propto V \exp\left(\dfrac{-c}{T}\right)$
Ionic conduction	$J \propto \dfrac{E}{T}\exp\left(\dfrac{-\Delta E_{ai}}{kT}\right)$	$\propto \dfrac{V}{T}\exp\left(\dfrac{-d'}{T}\right)$
Space-charge-limited	$J = \dfrac{9\varepsilon_i\mu V^2}{8d^3}$	$\propto V^2$

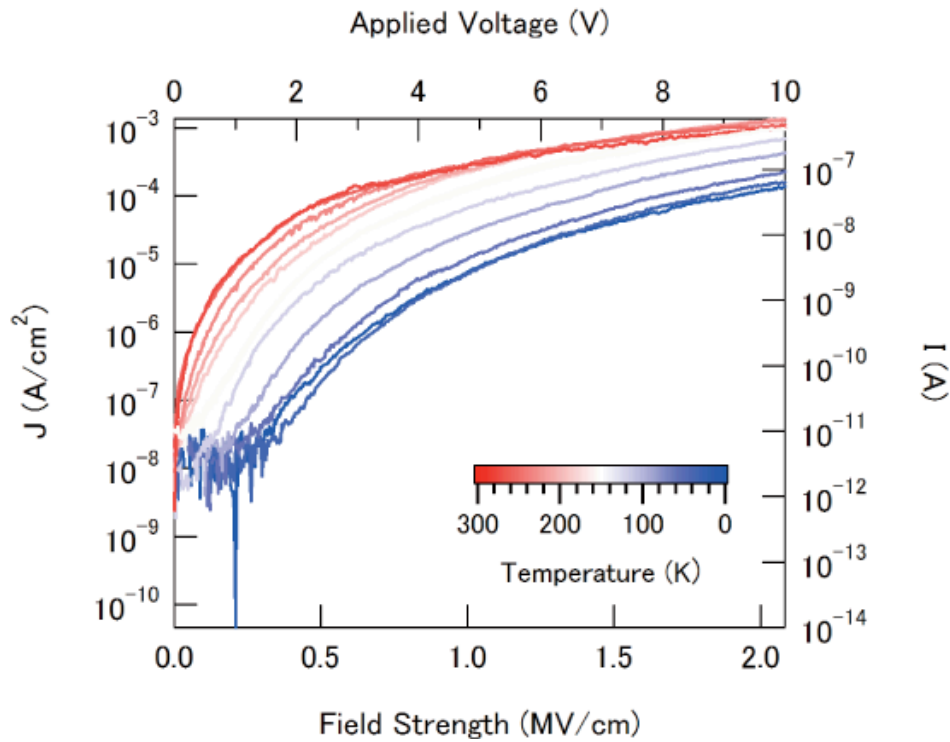$$a = \sqrt{q/4\pi\varepsilon_i d}$$

Fig. 4.1 Typical current density vs. field strength characteristics as a function of temperature for a 48 nm thick Al/DyScO$_3$/Nb-doped SrTiO$_3$ MIS capacitor. Thickness is Capacitance Equivalent Thickness (CET), which was calculated from bulk permittivity of 21.4, a pad area of 0.00036 cm^2, and the measured capacitance.

(a)

Field strength	Activation energy		
	T > 160 K	*160 K > T > 60 K*	*T < 60 K*
2 MV/cm	(a) –	(e) 0.0084 eV	(i) 0.001 eV
1.5 MV/cm	(b) –	(f) 0.011 eV	(j) 0.0012
1 MV/cm	(c) 0.0049 eV	(g) 0.014 eV	(k) 0.0016 eV
0.5 MV/cm	(d) 0.02 eV	(h) 0.02 eV	(l) 0.0022 eV

(b)
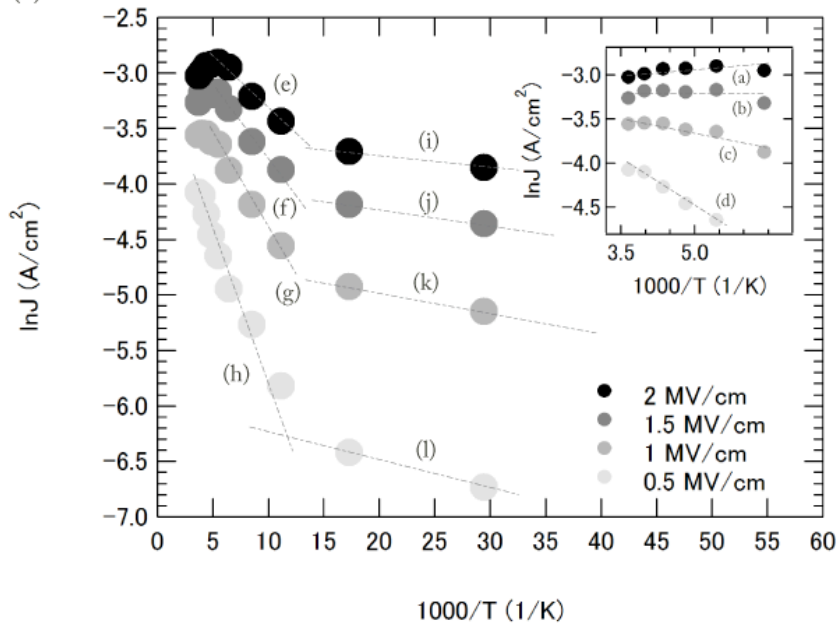
Fig. 4.2 (a) Temperature dependence of activation energy as a function of field strength. (b) Arrhenius plot of temperature-dependent leak current density for Al/ DyScO$_3$/ Nb-doped SrTiO$_3$ MIS capacitors. High-temperature range of plots is shown in the inset.
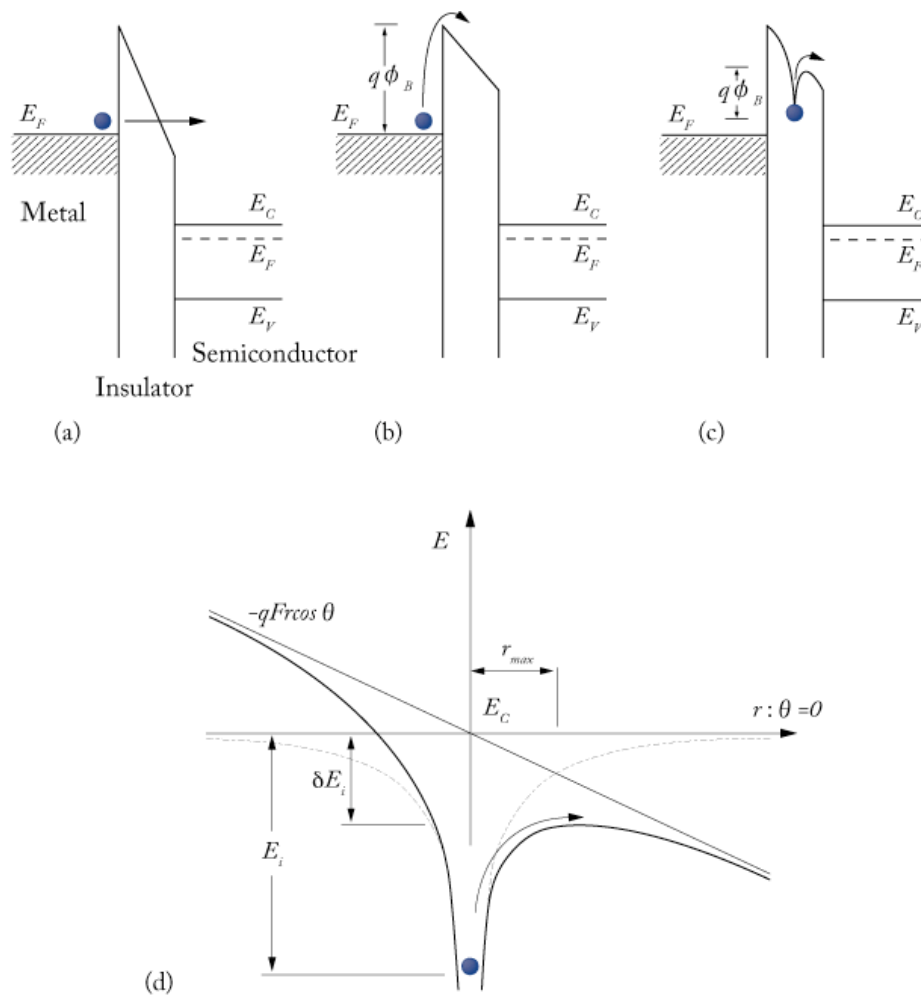
Fig 4.3 Energy-band diagrams of MIS capacitors showing various conduction mechanisms: (a) Fowler-Nordheim tunneling, (b) thermionic emission, (c) Poole-Frenkel emission. (d) Electron energy diagram in the presence of an electric field. This is field enhanced emission, Poole-Frenkel type. Dotted line represents equilibrium conditions.
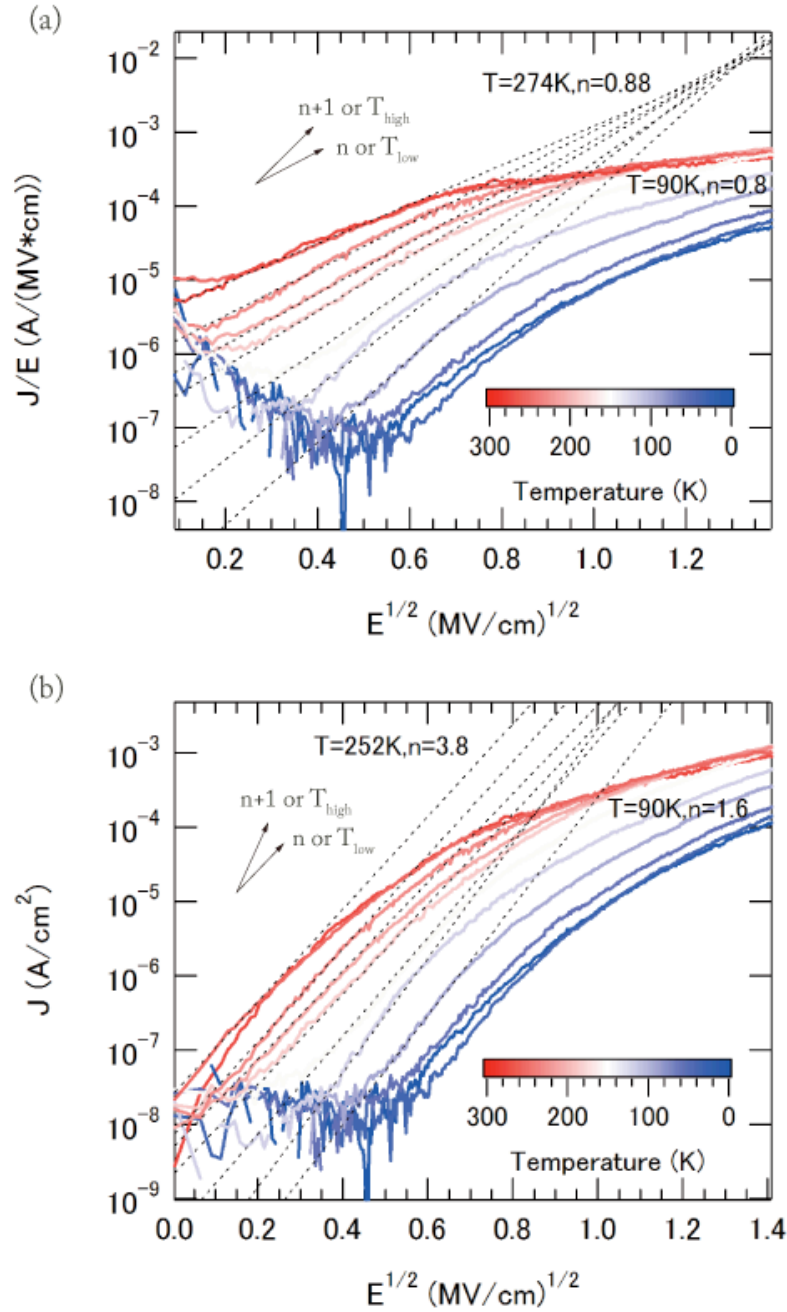
Fig. 4.4 Leak current characteristics shown as (a) Poole-Frenkel plot and (b) Schottky plot as a function of temperature. Dotted lines correspond to the best fits to experimental results following each conduction mechanisms.
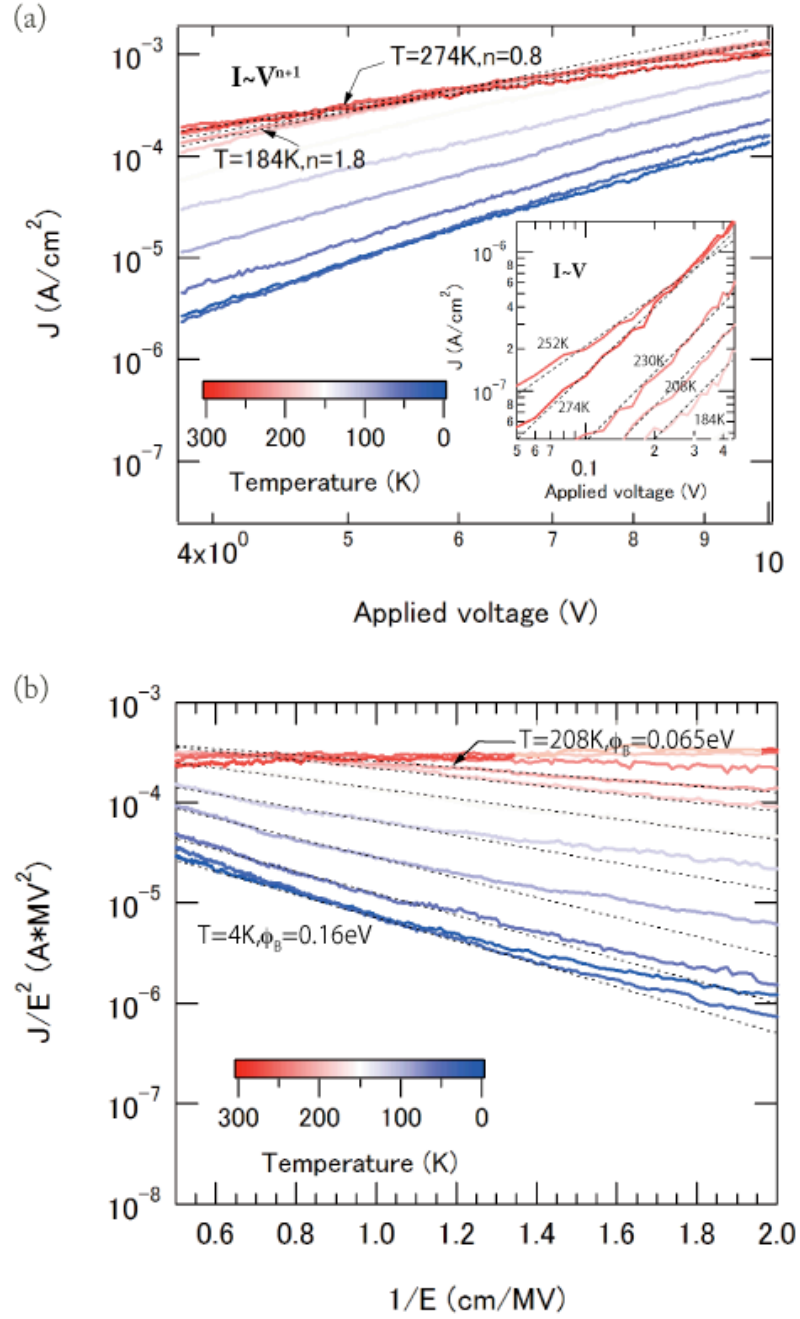
Fig. 4.5 Leak current characteristics shown as (a) Space-Charge-Limited plot and (b) Fowler-Nordheim plot as a function of temperature. The inset in the upper graph shows an Ohmic or ionic conduction plot. All experimental results were fitted as shown with dotted lines, which were derived for each conduction mechanism.

Temerature	Low field ~0.5 MV/cm	Middle field 0.5 ~ 1 MV/cm	High field 1 MV/cm~
160K~R.T.	Ohmic	Poole-Frenkel	Space-Charge-Limited
60K~160K	-	Poole-Frenkel	Fowler-Nordheim
~60K	-	Fowler-Nordheim	Fowler-Nordheim
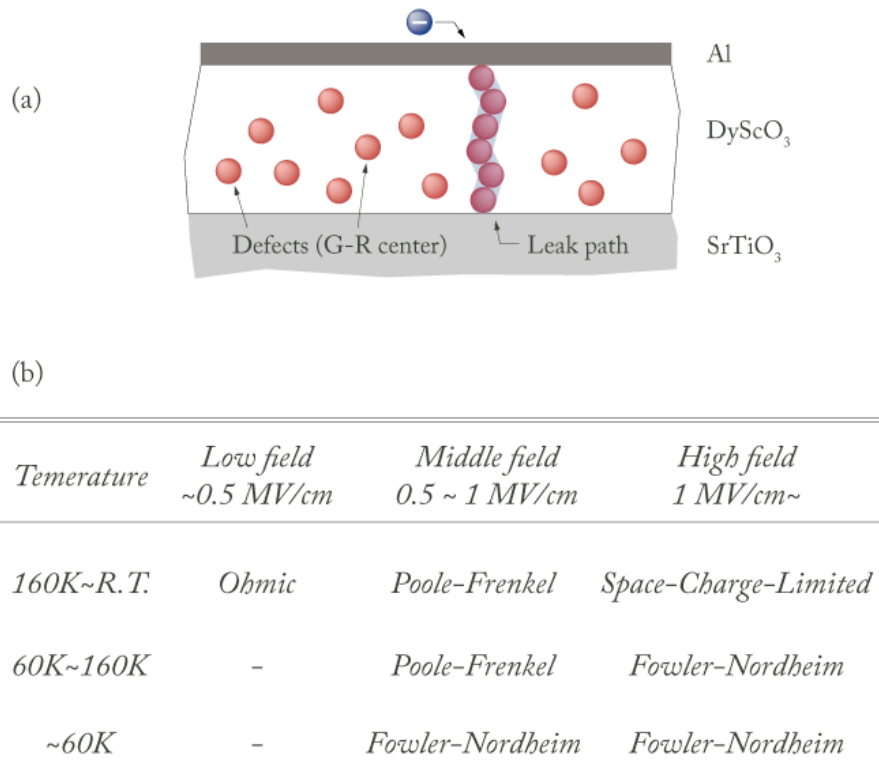
Fig. 4.6 (a) Percolation theory: breakdown occurs when random defects form a chain-like line between the gate electrode and the substrate. In this case, the defects are oxygen vacancies or possibly G-R centers. (a) The matrix of field effect dependence of carrier transport mechanisms as a function of temperature.

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Chapter 5
Concluding Remarks

In the world of electronic device design, it is the age of rapid change. Si, which has dominated electronics since 1960s, is close to the limit of scaling laws in digital applications. Under these circumstances, attention has turned to oxide electronics, mostly due to the availability of high-permittivity oxides, but also because new functions can be integrated into the fundamental devices themselves, such as diodes and transistors. This change of focus has also resulted in growing interest in the physical properties of oxide materials, and especially oxide heterostructures. However, work on device application and even the basic understanding of the electronic behavior of oxide heterointerfaces has proven to be a very challenging task. Oxide systems are generally not as clean as pure semiconductors and for that reason, there are often many competing mechanisms that determine the properties and behavior of a practical heterostructure. In this thesis work, I have focused on the characterization of high-permittivity oxide insulators that are used in all-oxide field-effect devices.

Based on a two-layer model, it was shown that capacitance measurements are consistent with the presence of an interface layer at the substrate / insulator interface with the thickness of the layer being between 0.8 nm to 2.8 nm. This interface layer was the first obstacle to accurate characterization of the insulator itself. The bulk dielectric constant of $DyScO_3$ was therefore derived from the film thickness dependence of capacitance, giving a fairly reliable bulk value of 21.4. A similar value was obtained from two types of analysis, a simple

two-layer model and from the assumption that the quadratic factor of a bias scan follows a general 'voltage linearity' shape, as explained in Section 3.2. Also in Section 3.2, the presence of oxide fixed charge near or at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ and mobile ionic charge in the $DyScO_3$ were identified. In transient analysis in Section 3.4, this fixed oxide charge was shown to have a relaxation time of about 6 seconds, while mobile ionic charge responded much more slowly, with a time constant of about 80 seconds. Both trapped centers had at least 10^{-14} cm^2 area of capture cross section, which would correspond to *'Coulomb attractive traps'* in a traditional semiconductor picture. These trap level were found to be relatively shallow. Summarizing the dielectric characterization, the conclusion is that there is both fixed trapped charge and mobile ionic charge in Al /$DyScO_3$ /Nb-doped $SrTiO_3$ capacitors. These effects can strongly affect the performance of field-effect devices and it is clearly necessary to carefully control the stoichiometry of the insulator, both in terms of cations and oxygen in order to reduce charge trapping and charge injection into the insulator interface layer.

In leak conduction chapter, the conduction mechanisms in a 48 nm $DyScO_3$ MIS capacitor were investigated. The current density vs. electric field characteristics showed a strong temperature dependence, suggesting that this insulator contained thermally excited carriers. Thus, it is reasonable to conclude that charge injection into the insulator can result in a FET threshold voltage shift at low temperature. Temperature and electric field dependence of the conduction mechanisms were evaluated and are summarized in Fig. 4.6 (b). In the high-field regime (1 MV/cm~) and below 160 K, Fowler-Nordheim tunneling could be seen with a 0.16 eV barrier height between $DyScO_3$ and Nb-doped $SrTiO_3$. In high-field (1 MV/cm~) and high temperature (from 160 K to 274 K) regime, however, Space-Charge-Limited current appeared to be dominant, resulting in a lower current density. In a medium field range (0.5~1 MV/cm) at high temperature (from 60 K to 274 K) case, Poole-Frenkel emission was dominant, with a 0.02 eV barrier height and a 0.23 eV trap level. Below 60 K, no activation energy was seen. In this region, tunneling conduction could be relatively high. In the low-field regime (~0.5 MV/cm), Ohmic conduction mechanism could be seen, suggesting that shallow, 0.02 eV trap state exist and resulting in thermally excited hopping.

Considering both dielectric properties and conduction mechanisms, I assign

thermally excited hopping and Ohmic conduction to very shallow defect states, mostly based on the analysis of transient characteristics. Ohmic conduction and Poole-Frenkel emission results in charge being injected into the bulk of the insulator, resulting also in trapped charge, at least on the timescale of transistor measurements. The trap states are thus ultimately responsible for the creation of fixed oxide charge near or at the substrate interface. Assuming that most of the fixed oxide charge is at the interface between $DyScO_3$ and Nb-doped $SrTiO_3$, I propose a band diagram for a MIS device, as shown in Figure 5.1. This band diagram corresponds to the Al/ $DyScO_3$/ 0.5wt.% Nb-doped $SrTiO_3$ MIS capacitor under ~0.5 MV/cm bias field at room temperature and appears to contain all the features observed in realistic devices. Under these conditions, hopping conduction and field-enhanced emission are thermally activated and a small current can flow in the insulator since the electron activation energy is only about 0.02 eV. The trap levels are apparently between 0.02 eV and 0.23 eV below the bottom of the conduction band. The density of this kind of type trap levels increases close to the interface between $DyScO_3$ and Nb-doped $SrTiO_3$ although bulk current injection means that some trap states exist in the bulk of the $DyScO_3$ film as well. This has a strong effect on the field-effect device performance. Below 100 K, even under a moderate field of 0.5 MV/cm, electrons are no longer thermally activated, presumably due to a semi-permanent filling of trap levels at the interface, which becomes more insulating in the field-effect device case.

I have proposed that fixed oxide charge, injected under high field, is a possible origin of threshold voltage shift in field-effect devices. I hope the present work will be of help to contribute to filed-effect carrier control in oxide heterostructures for future applications in the world of oxide electronics and, through this small step, make the world a better place in the future.
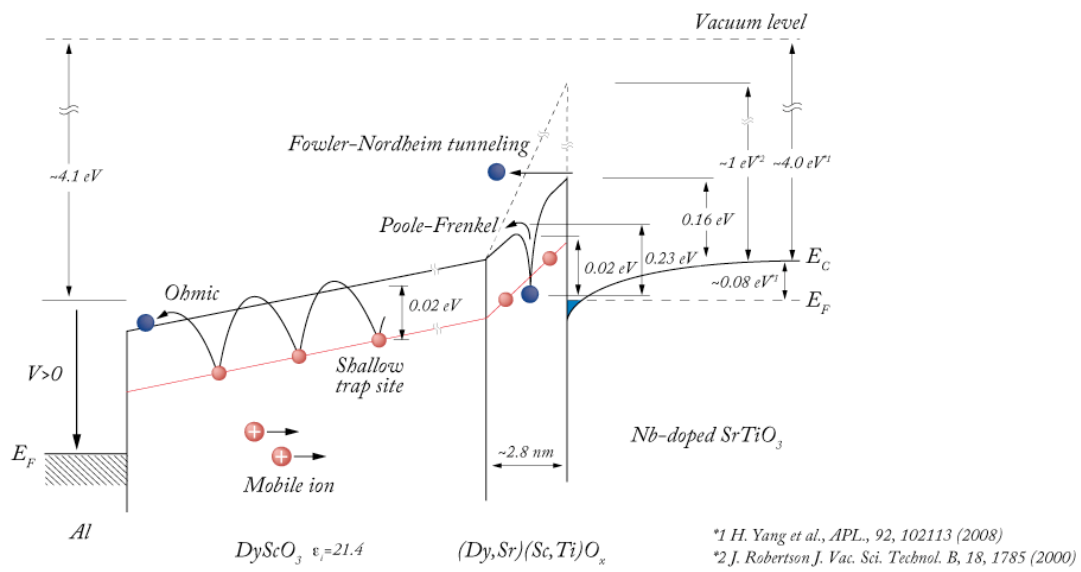
Figure 5.1 A proposed energy band diagram of an Al/ DyScO₃/ Nb-doped SrTiO₃ MIS capacitor under ~0.5 MV/cm bias field at room temperature.

Appendix α

The source code of equivalent circuit C(f) fitting

This function implements the equivalent circuit fitting routine for analyzing the frequency dependence of a MIS capacitor in the Igor macro language.

```
1    #pragma rtGlobals=1   //Use modern global access method.
2
3       Function/D cpd(w,x)
4
5          Wave/D w; Variable/D x
6          //w: Cp1, Rp1, Cp2, Rp2, Rs, Ls, Dcp, and Doff
7             Variable/D Cp1=w[0]*1e-12
8             Variable/D Rp1 = w[1]
9             Variable/D Cp2 = w[2]*1e-12
10            Variable/D Rp2 = w[3]
11            Variable/D Rs = w[4]
12            Variable/D Dcp = w[5]*1e-12
13            Variable/D Ls=w[6]*1e-6
14            Variable/D Doff=w[7]*10000
15            Wave Flist $"Flist"
16            Variable/D f = Flist[x]
17            Variable/D Omega
18
19              if (f>1e6)
20                  Omega = 2*Pi*(f-1e6)
21              else
22                  Omega = 2*Pi*f
```

```
23              endif
24
25          Variable/C R1,C1,R2,C2,R3,L1
26
27            R1=cmplx(Rp1,0)
28            R2=cmplx(Rp2,0)
29            R3=cmplx(Rs,0)
30            C1=cmplx(0,1/(Omega*(Cp1+Dcp*log(f)) ))
31            C2=cmplx(0,1/(Omega*Cp2))
32            L1=cmplx(0,Omega*Ls)
33
34          Variable/C z
35
36            z = R1*C1 / (R1+C1)
37            z = z + R2*C2/(R2+C2)
38            z = z + R3 + L1
39
40            if (f>1e6)
41                return(10000*real(z)/imag(z)+Doff)
42            else
43                return(imag(z) /(Omega*magsqr(z))*1e12)
44            endif
45
46      End
```

Appendix β
Achievements list

"Low-temperature dielectric characteristics of $DyScO_3$ thin films for $SrTiO_3$ single crystal Field Effect Transistors" (Poster), The 68th autumn meeting of the Japan Society of Applied Physics, 2007

"Low-temperature dielectric characterization of $DyScO_3$ thin films" (Poster), The 14th World of Oxide Electronics, 2007 (abstract only)

"Influence of interface layers on the dielectric properties of $DyScO_3$ capacitors" (Oral), The 69th autumn meeting of the Japan Society of Applied Physics, 2008

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