特　集　4
研　究　速　報

Micro Electrical Connectors by Silicon Anisotropic Etching

シリコン基板の異方性エッチングによるマイクロコネクタ

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1. Introduction

MEMS (micro electro mechanical systems) is a powerful technology to integrate micro actuators and sensors with electrical circuits on a single silicon chip. However, the combination of materials is strongly limited by the process compatibility with IC (integrated circuit) fabrication. Therefore, hybrid assembling of micro mechanical chips with IC chips will remain as a practical method of device packaging.

We have recently developed silicon micro connectors and receptacles for three-dimensional electrical interconnection of MEMS devices. This note deals with the new idea of micro connectors and receptacles along with the experimental results on fabrication and interconnect characteristics.

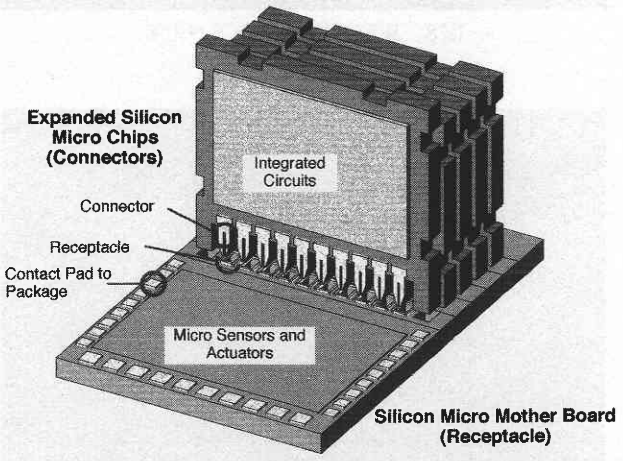

Figure 1　Micro connector chips assembled on a micro receptacle chip for high density three-dimensional MEMS interconnection.

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2. Silicon Micro Mother Board by MEMS

Most of the conventional three-dimensional packaging is done by stacking IC chips [1]. In this case, however, the chips needed to have electrical connection through the substrate, and thus the fabrication process becomes complicated. For high density packaging of MEMS devices, we propose a new three-dimensional micro electrical interconnection, which consists of silicon micro connector-chips sitting normal to a receptacle base-chip as illustrated in Fig. 1. The connector chips are small IC substrates, whose fringes are patterned into pin structures, and plugged into the slots on the base-chip to make physical and electrical contact. Since the structure looks like a miniaturized computer mother board with expansion slots, we call it a silicon micro mother board. The technique proposed here allows us to assemble integrated circuits with MEMS devices at the chip level. It reduces not only the size of packaging but also the electrical resistance and the stray capacitance of electrical interconnection.

Figure 2 shows the fabrication flow of the connectors and the receptacles. After IC or MEMS fabrication, a silicon wafer is covered with a photoresist mask and patterned into structures of a high aspect ratio by ICP-RIE (inductively coupled plasma - reactive ion etching), which has no mechanical or electrical damage to IC and MEMS devices. The chips are isolated from the frame by the deep trenches but suspended with small silicon bridges. Silicon oxide is sputtered on the surface for insulation, and then chromium and gold are deposited by evaporation. These metal layers are patterned by the ordinal photolithography step and wet etching to make metal contact on the connectors and receptacles. After snapping the chips off from the frame, they are assembled into the slots. The structure is

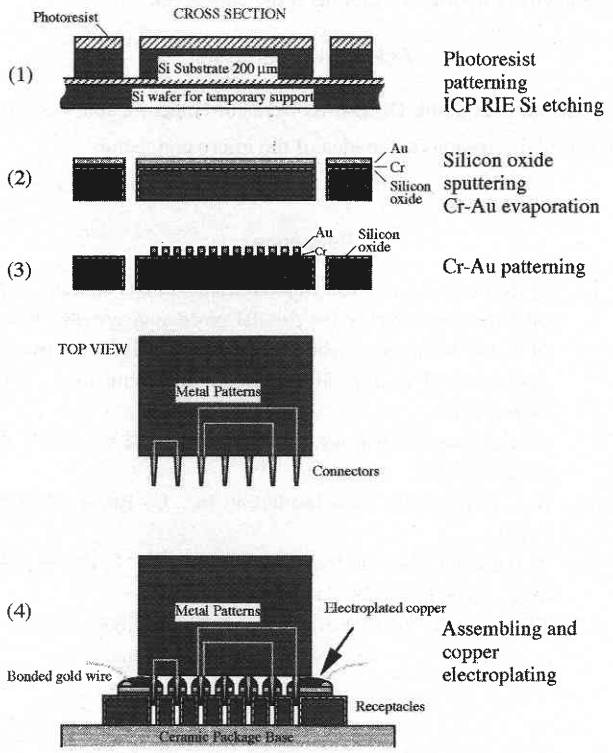

Figure 2　Fabrication process of the micro connector and receptacle. Through holes are formed by anisotropic dry etching, and contact is finished by electroplating of copper.

mounted on a ceramic package and wire-bonded. Subsequently a thick layer of copper is electroplated in a $CuSO_4$ based solution to assure the electrical and mechanical contact. The IC and MEMS devices do not necessarily share the same fabrication steps but they can be processed independently on different chips. Therefore, processes hazardous to IC devices are permitted to make MEMS devices.

Similar types of three-dimensional packaging have been proposed [2, 3, 4, 5]. They used a dicing saw or anisotropic wet etching to form receptacle slots of trenches in silicon. Therefore, they could not have an access to the devices over the trenches. In our method, on the other hand, it is possible to arrange metal patterns going around the receptacle holes to reach over.

To verify the idea of micro mother board, we patterned a bare silicon wafer of 200 microns thick into connector chips (3.0 mm × 3.4 mm × t 0.2 mm) and a receptacle chips (5.5 mm × 6.5 mm × t 0.2 mm) and assembled by manual control under the microscope. No IC or MEMS structures were implemented on the chip, but metal patterns of different path length were formed to test the electric contact charact. The edges of the receptacle holes were also covered with metal. In Fig. 3 we show an SEM (scanning electron microscope) view of an assembled micro mother board. Six chips are sitting normal to the base. The dimensions of a connector tip are 100 microns wide and 200 microns long.

The electrical resistances including those of contacts and bonding wires were measured at the pins of a ceramic package and plotted as a function of the pattern length on the connector chip in Fig. 4. Measurement was carried out every 15 minutes of electroplating of copper, after a careful rinsing and drying

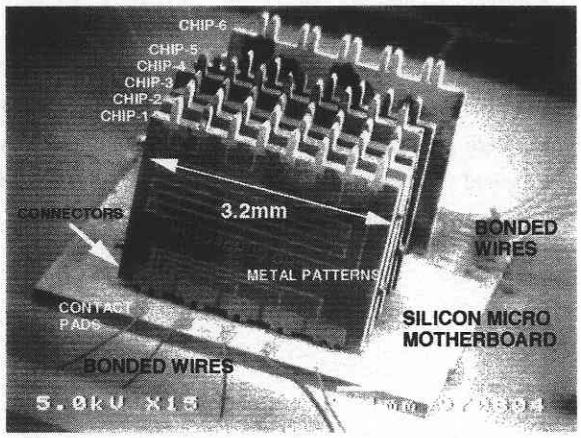

Figure 3　SEM view of the micro connector chips.

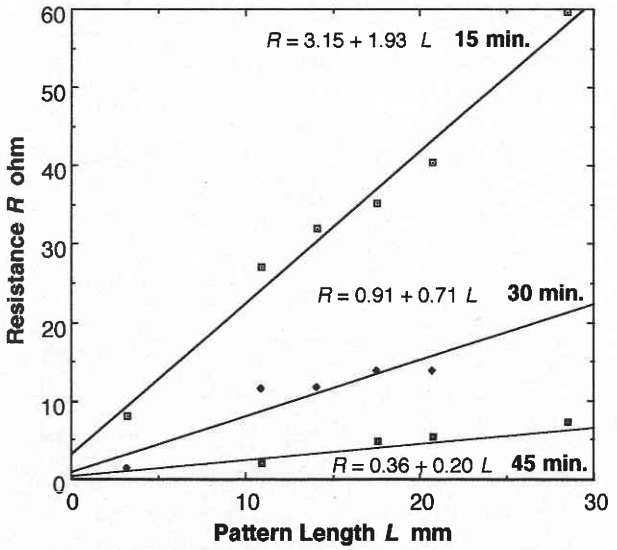

Figure 4　Electrical resistance R as a function of pattern length L. Contact resistance is known by extrapolating the resistance at $L = 0$

process. Drastic reduction of resistance was observed as extending the plating time. The contact resistance is known by extrapolating the resistance curve to the Y-axis, where the pattern length is equal to zero. Since the connection is made via two contacts, the resistance at a single contact was calculated only 0.18 ohms after electrodeposition of 45 minutes. On the identical sample a stray capacitance of 50 pF was found. Thus, the cut-off frequency through the path is as high as 17.7 GHz.

Besides the permanent contact by plating after assembling, temporal contact is also possible by making copper bumps on the connector tips and the receptacles before assembling. Such contact was found to persist through several repetitions of connection and disconnection.

3. Conclusions

A three-dimensional micro electrical interconnection by silicon connectors and receptacles was proposed, and preliminary devices were fabricated by using ICP-RIE process. Contact resistance and stray capacitance as low as 0.18 ohms and 50 pF, respectively, were obtained. The technique expands the range of material combination for integrated MEMS devices and allows high density hybrid assembling at the chip level.

Acknowledgements

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