Prototype of a Compact Imaging System for GEM Detectors

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***Abstract*—We have developed a prototype of a compact imaging system for gas electron multiplier (GEM) detectors, which we applied to thermal neutron imaging. The developed system consists of three devices: a detector, an Ethernet hub, and a PC. The readout electronics are integrated into the detector. Ethernet is used to communicate between the detector and the PC. The detector is directly connected to the PC with Ethernet. This system is simple and cost-effective, and provides high flexibility for system design. We have measured system performance and tested the system with a thermal neutron beam. This system enables use of an imaging system in various fields where it has not previously been possible to use such systems.**

***Index Terms*—Field-progammable gate arrays (FPGAs), gas electron multiplier (GEM) detectors, imaging applications, neutron imaging.**

I. Introduction

THE Gas Electron Multiplier (GEM), which was first introduced in 1996 [1], has been applied to detectors for noncharged particles, such as neutrons and X-rays. [2], [3]. In these detectors, the GEMs are used both as converters and as multipliers. Since a GEM can transfer electrons to the next region through its holes, multiple converters can be used. Thus, a detector using these converters has an advantage for detecting noncharged particles with low detection efficiency. We have developed imaging detectors for thermal neutrons [4] and X-rays, which can be used in many fields, including materials science and nondestructive inspection. The current system, however, is large and complex, making it applicable in a limited number of fields. To overcome the size limitation, we have developed a compact readout system using the GEM detector. This system is small, simple, and cost-effective, and can be moved, constructed, and used easily. Thus, this system can be applied readily in various fields where it has not been possible to use such systems to date. The discussion will focus on the use of this system for thermal neutron imaging.

II. System

Fig. 1 shows a block diagram of the developed system, which consists of a detector, an Ethernet hub, and a PC. The detector and the PC are connected with Ethernet. The detector consists of a GEM-chamber [4] and readout electronics. The GEM-chamber detects thermal neutrons. The readout electronics process signals from the chamber, and generate event data on an event-by-event basis. The PC, located remotely from the detector, receives the event data through Ethernet. The event data consists of a time stamp and the detected position information. The time stamp is useful for pulsed neutron experiments. The PC stores and analyzes the event data.

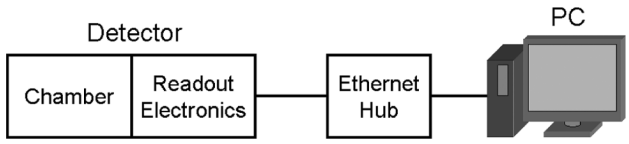

Fig. 1. Block diagram of the developed system.

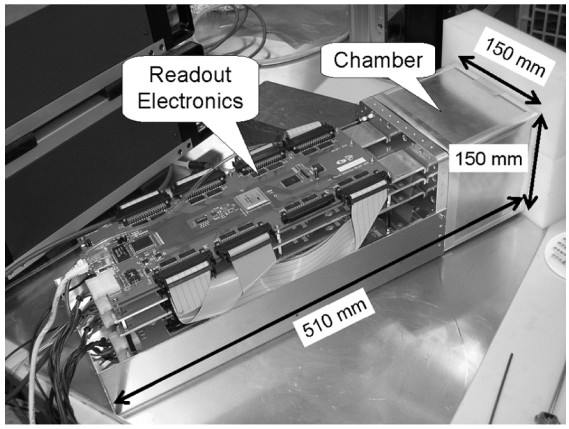

Fig. 2. Photograph of the detector.

Transmission Control Protocol (TCP) and Internet Protocol (IP) are used for communication between the PC and the detector. The use of Ethernet, TCP, and IP has many advantages, including the ability to construct a flexible system; i.e., there are essentially no limitations of distance between the PC and the detector, and multiple detectors can be controlled by a single PC. In addition, TCP and IP are *de facto* standards, which have been widely adopted and implemented by many commercial devices and standard Operating Systems (OS). This enables us to employ various commercial devices, as well as to develop application software using standard functions of a standard OS known as socket functions.

Fig. 2 shows a photograph of the detector, which consists of the chamber and the readout electronics, and measures 150 mm $\times$ 150 mm $\times$ 510 mm. The detector has only a single interface cable, which is for Ethernet—the other cables shown in the photograph are used for power supply. In addition, the detection area of this system can be easily expanded by employing

Manuscript received June 17, 2008; revised August 04, 2008. Current version published December 04, 2008.

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Digital Object Identifier 10.1109/TNS.2008.2004772

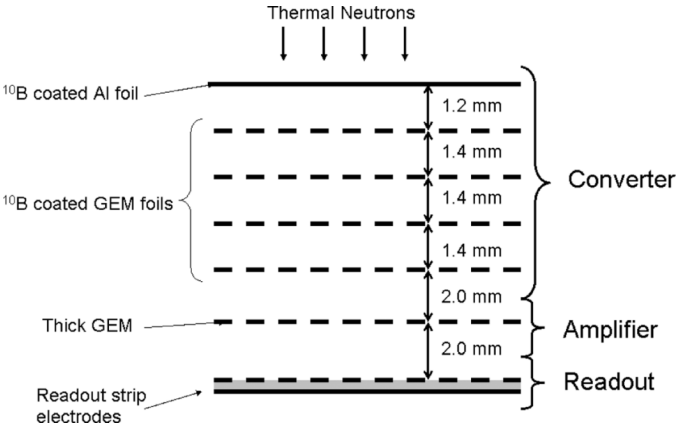

Fig. 3. Structure of the chamber of the prototype detector.

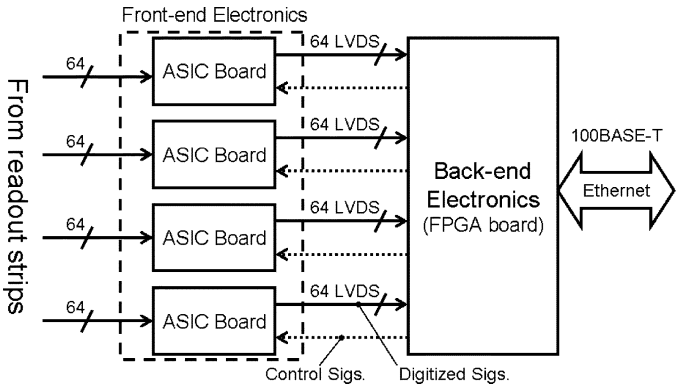

Fig. 4. Block diagram of the readout electronics.

multiple detectors. To cover the area, the detectors are stacked. These detectors are connected with Ethernet, with the Ethernet links aggregated by an Ethernet Hub. Event data generated by these detectors can be processed by one or more PCs. Thus, we can design a system architecture that is suitable for the required performance.

III. Chamber

Fig. 3 shows the structure of the chamber, which consists of three parts: a converter, an amplifier, and a readout component. Ar/CO_2 (70/30) gas is used at atmospheric pressure. Each GEM foil measures 100 mm $\times$ 100 mm.

The converter consists of four ^{10}B-coated GEM foils and an Al foil. Boron is used to detect thermal neutrons, which can be detected as alpha particles through the following reactions: n $(^{10}B, \alpha)^7\mathrm{Li} + \gamma$, 93%, and n $(^{10}B, \alpha)$, 7% [6], [7]. In boron, the ranges of alpha and lithium particles are each less than 6 μm. The Al-foil is a drift plane. Boron of 1.2 μm thick is coated on the both surfaces of a standard GEM foil. Each standard GEM foil has holes of 70 μm diameter with a 140 μm pitch, and consists of three layers—a polyimide insulator 50 μm thick and copper electrodes 5 μm thick. Since electrons generated by alpha particles are transferred to the next region through the holes of the GEM foils, multiple converters can be used. To reduce variations in total gain, the gain of the converters should be set to unity.

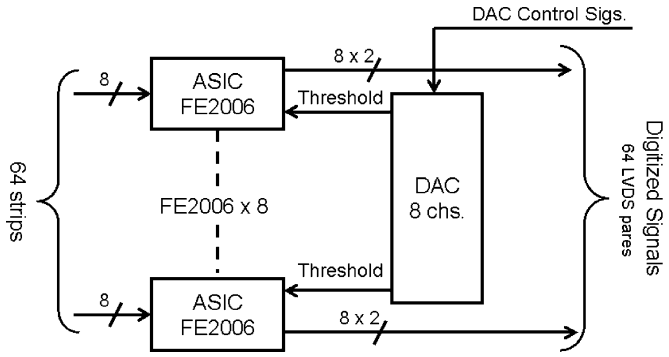

Fig. 5. Block diagram of the ASIC board.

The amplifier uses a thick GEM foil [5]. The insulator of the GEM foil is a liquid crystal polymer (LCP) 100 μm thick, and the surfaces are copper layers 5 μm thick. The foil has holes of 70 μm in diameter with pitch of 140 μm. Gain of the amplifier is set to about 100.

The readout part uses a two-dimensional strip, of pitch 0.8 mm, with 120 strips on each side (i.e., 120 X-strips, 120 Y-strips). The effective detection area of the readout board is 96 mm $\times$ 96 mm.

IV. Readout Electronics

The readout electronics are integrated into the detector and are connected to a PC with Ethernet. All signals from the readout strips are processed and transferred to the PC as event data. Fig. 4 shows a block diagram of the readout electronics, consisting of front-end (FE) and back-end (BE) electronics. The readout strips and the FE are connected via a printed wiring board (PWB). The FE consists of four application-specific integrated circuit (ASIC) boards, which process detector signals from the readout strips and digitize these signals with comparators. These digitized signals are transmitted to the BE using low voltage differential signaling (LVDS). The BE generates event data from these signals, and transfers the data to a PC through Ethernet. The FE can be controlled to set threshold voltages for the comparators by a PC through Ethernet. Control signals from the BE to the FE are used for this purpose. The digitized signals and the control signals are transmitted using flat cables.

In designing the compact system, we have adopted ASICs and field-programmable gate arrays (FPGAs). The ASICs process analog signals in the FE, and the FPGA processes digital signals in the BE.

A. Front-End Electronics

The FE consists of four ASIC boards. Fig. 5 shows a block diagram of the ASIC board, which consists of a single digital-to-analog converter (DAC) and eight ASICs named FE2006 [8]. The DAC has eight channels and supplies threshold voltages to the FE2006s for digitizing. The FE2006, which was designed as a front-end device for micro pattern gaseous detectors (MPGDs), processes and converts detector signals to digital signals.

1) FE2006: Each FE2006 has eight independent amp-shaper-discriminator (ASD) circuits for each signal input, and an analog sum amplifier with an attenuator to

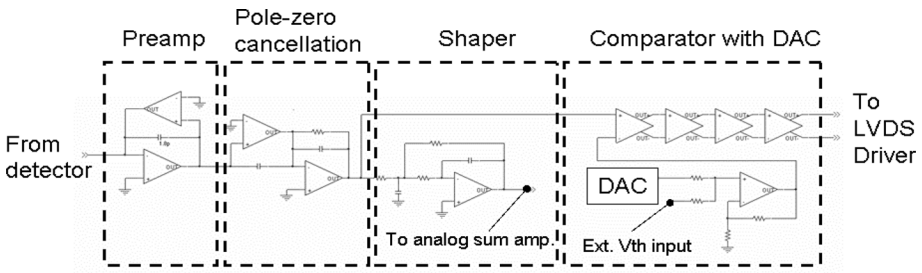

Fig. 6. Circuit diagram of a channel.

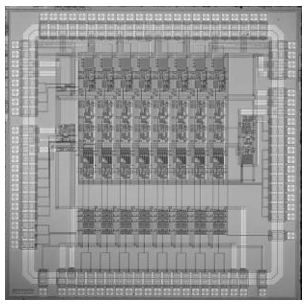

Fig. 7. Chip layout of FE2006.

achieve a wide dynamic range, up to 4.5 pC input. Fig. 6 shows a circuit diagram of a channel. The circuit consists of a low noise charge amplifier, a pole-zero cancellation circuit, a filter, a comparator, a DAC, and an LVDS driver. The preamplifier consists of a folded-cascode amplifier with a transconductance amplifier for DC feedback. The feedback capacitance is 1.8 pF and the input device is an N-well enclosed 7800 μ/0.7 μ size PMOSFET. The drain current is set to 1.8 mA. Pole-zero cancellation is achieved by a similar current feedback amplifier used in the preamplifier for different settings of discharging time. The shaper is a RC(CR)^2 low pass filter with peaking time of 20 ns based on an operational amplifier. We determined the peaking time to meet requirements for the Japan Proton Accelerator Research Complex (J-PARC) experiments and for X-ray measurements at high counting rate. The comparator is comprised of four differential inverters. The 5-bit DAC is implemented to adjust the channel-to-channel variation of threshold voltage in the 30 mV range. The operational amplifier in analog sum is a class AB amplifier capable of loads up to 1 kΩ. The LVDS driver is a type of CSDA amplifier capable of a 100 Ω load to 200 mV swing and sufficient for typical LVDS receivers.

Fig. 7 shows a micrograph of an FE2006 chip. The die area is 4 mm $\times$ 4 mm, and the channel pitch is 250 μm. FE2006 specifications are shown in Table I. The preamplifier has a sufficient signal-to-noise ratio for a large area MPGD ($\sim$30 $\times$ 30 cm^2), the detector capacitance of which increases up to 100 pF. The integral nonlinearity is less than 3% in the whole signal range. The crosstalk is typically 0.3%, at most 0.6% except for next channel. The comparator time-walk is less than 9 ns from 7 fC to 1.5 pC input. The total power dissipation is typically 29 mW per channel and the analog part, except for the LVDS driver with a load of 100 Ω, is 19 mW per channel.

TABLE I
FE2006 SPECIFICATION

Power supply	2.5V, –2.5V
Channel	8
Input charge	–1.5 pC ~ 1.5 pC
Conversion gain	0.44 V/pC
Integral non linearity	< 3%
Peaking time	20 ns
Noise	5100 e @ Cd = 100 pF
Crosstalk	< 0.6% (1~3% next channel)
Timewalk	< 9 ns
Vth compensation DAC	1 ~ 30 mV @ 1 mV/bit
Readout clock	10 MHz
Power dissipation	29 mW/ch
Die size	4 mm × 4 mm

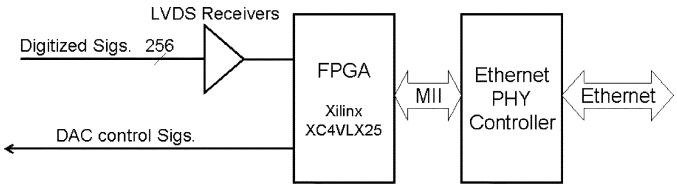

Fig. 8. Block diagram of the back-end electronics.

B. Back-End Electronics

The BE generates event data from digitized signals coming from the FE, and transfers these data to a PC through Ethernet. Fig. 8 shows a block diagram of the BE. The main components are LVDS receivers, a single FPGA [9], and an Ethernet physical layer controller (PHY). The receivers terminate the LVDS signals and transmit these signals to the FPGA using 2.5 V CMOS signaling. The FPGA processes these signals and generates event data as Ethernet frames. These frames are processed by PHY, which converts signals to meet Ethernet specifications [10] and transmits these to the PC. The FPGA and the PHY device are connected with a media independent interface (MII) specified by IEEE802.3 [10]. This interface standard has been adopted by many PHY products.

1) FPGA: Fig. 9 shows a block diagram of the FPGA, which consists of a sampler, an event filter, an event data generator, a time clock, a network processor (SiTCP) [11], [12], and a DAC controller. Detector signals from the FE are sampled at 100 MHz by the sampler. The event filter selects events and determines the detected position from the sampled signals. The event filter is the main block, and its details will be described in the next section. The event data generator builds event data

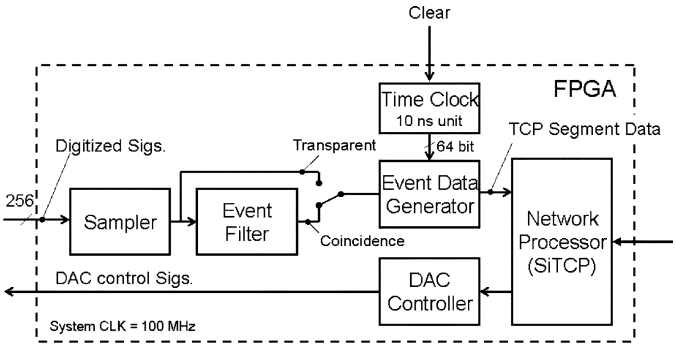

Fig. 9. Block diagram of the FPGA.

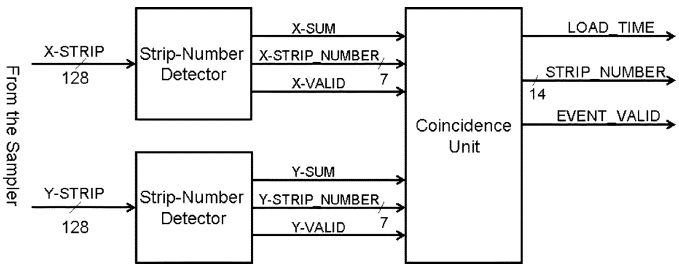

Fig. 10. Block diagram of the event filter.

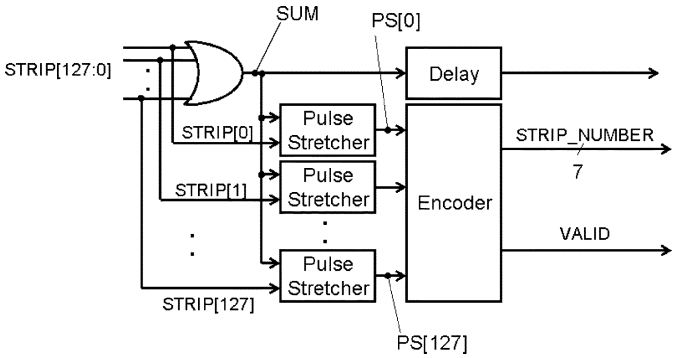

Fig. 11. Block diagram of the strip number detector.

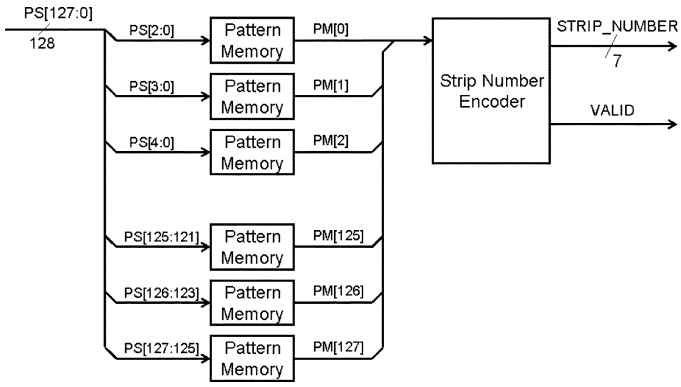

Fig. 12. Block diagram of the encoder.

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PM [  0] = (PS[2:0]==3'b011) | (PS[1:0]==2'b01);
PM [  1] = (PS[3:1]==3'b011) | (PS[2:0]==3'b010) | (PS[2:0]==3'b111);
PM [  2] = (PS[4:2]==3'b011) | (PS[3:1]==3'b010) | (PS[3:0]==4'b1110);
PM [  3] = (PS[5:3]==3'b011) | (PS[4:2]==3'b010) | (PS[4:1]==4'b1110);
   :                :                :                :
PM [124] = (PS[126:124]==3'b011) | (PS[125:123]==3'b010) | (PS[125:122]==4'b1110);
PM [125] = (PS[127:125]==3'b011) | (PS[126:124]==3'b010) | (PS[126:123]==4'b1110);
PM [126] = (PS[127:126]==2'b11 )  | (PS[127:125]==3'b010);
PM [127] = (PS[127:126]==2'b10);
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Fig. 13. Source code of the pattern memories.

from the sampler or event filter. Event data are built from raw data of the sampled signals when one or more signals are asserted in transparent mode. The data consist of a 256-bit hit pattern and a 64-bit timestamp of resolution 10 ns. In coincidence mode, event data are built with a timestamp and the position detected by the event filter. The data consist of the 16-bit position and the 64-bit timestamp. The SiTCP processes network protocols and generates Ethernet frames from the event data. The SiTCP is a hardware-based TCP processor. Although network protocols are generally processed by software, in this FPGA, these protocols are processed by the hardware. The processor is designed for small devices, such as detectors and front-end devices. The event data are transmitted as TCP packets. The SiTCP has a mechanism for slow control with a user datagram protocol (UDP) [11], through which the DACs in the FE and the threshold voltages of the comparators in the FE2006s are set with the DAC controller.

2) Event Filter: The event filter selects the most likely true events from the signals. Fig. 10 shows a block diagram of the event filter, which consists of two strip number detectors and a coincidence unit. The strip number detector rejects noise signals and finds a detected position of X or Y. The coincidence unit detects the two-dimensional position from the X and Y positions detected by the strip number detectors.

Fig. 11 shows a block diagram of the strip number detector, which consists of pattern memories, an OR logic circuit, and an encoder. All signals from the sampler are input into an OR logic circuit and pulse stretchers. The OR logic circuit sums the inputs and generates SUM, which is delayed and transmitted to the coincidence unit. The pulse stretcher generates PS. The signal is active when an input signal from the sampler is asserted. To reject noise signals and sampling errors, the PS is kept in the active state while SUM is active. The encoder finds position of an event. We assumed that an event induced one X-STRIP and one Y-STRIP because in principle the strip readout method can detect only one event at a time. However, neighboring strips could detect signals at the same time [13], because electrons multiplied by GEMs are spread. To treat these neighboring strip signals, the central strip number value of the detected signals is used. The encoder consists of pattern memories and a strip number encoder, as shown in Fig. 12. The pattern memory selects a central strip number from three neighboring active strips. A source code of the pattern memory is shown in Fig. 13, written in *Verilog* hardware description language (HDL). The strip number encoder determines when an event is valid and its encoded strip-number, when just one PM is active.

Fig. 14 shows a circuit diagram of the coincidence unit. When a likely true event is detected, this circuit asserts STRIP_NUMBER, EVENT_VALID, and LOAD_TIME. Basically, EVENT_VALID is asserted when X-EVENT_VALID and Y- EVENT_VALID are asserted at the same time. However, that is not sufficient to determine that an event is likely true because accidental coincidence events can occur. We have

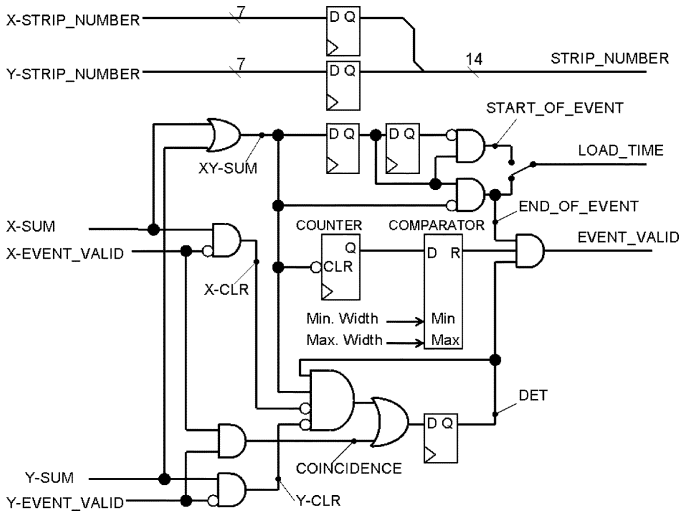

Fig. 14. Circuit diagram of the coincidence unit.

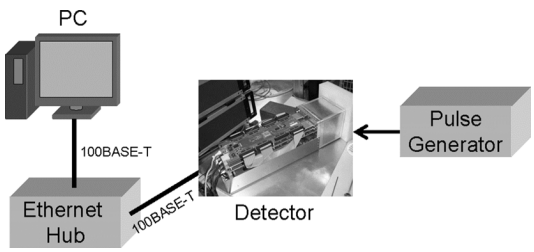

Fig. 15. Test setup for processing rate.

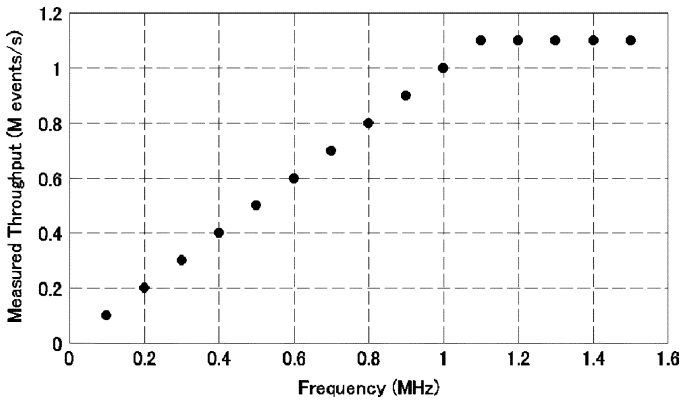

Fig. 16. Measured throughputs.

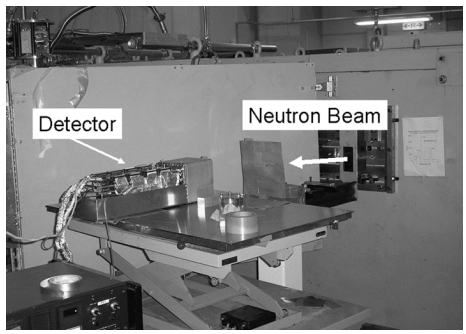

Fig. 17. Photograph of the thermal neutron beam test setup at the Japan Atomic Energy Agency (JAEA-Tokai).

therefore designed this circuit to reject these false events. When X- EVENT_VALID and Y- EVENT_VALID are asserted at the same time, COINCIDENCE and DET are asserted. The active state of DET is kept by a D-flip flop (DFF) when XY-SUM is active. When DET is active, X/Y- EVENT_VALID is negated even if X/Y-SUM is active, X/Y-CLR is asserted and DET is negated. This circuit selects an event by a pulse width of X- or Y-SUM. Detector signals generated by a GEM detector have a specific signal width, because thus width is determined by the spacing of its induction region. Thus, this signal filtering method is effective for GEM detectors. COMPARATOR and COUNTER are used for this function. COUNTER measures a pulse width of XY-SUM. When the pulse width is between its minimum and maximum, COMPARATOR output is asserted. Finally, EVENT_VALID is asserted when END_OF_EVENT, DET, and the output of COMPARATOR are active at the same time. END_OF_EVENT is used because it can be decided immediately, before any signals are negated, whether the event is an event is a likely event or not. LOAD_TIME is the time to load the event time, and the assertion timing can be selected as the start or end of the event.

V. Test and Results

We measured processing rate, detection efficiency and position resolution, and took absorption images.

Processing rate was measured as throughputs with test pulses generated by a pulse generator. Fig. 15 shows the test setup, which consists of a pulse generator, a detector, an Ethernet hub and a PC. The test pulses were generated periodically and fed to the X- and Y-strips of the detector through capacitors. The detector was running on the coincidence mode. The PC running Linux was connected to receive and store event data from the detector using the socket functions. Fig. 16 shows measured throughput as a function of test pulse frequency. The maximum processing rate was 1.1 MHz. The limit was determined by the transfer rate of Ethernet, 100 Mb/s. The maximum throughput of TCP-segment data was limited to about 95 Mb/s because protocol overheads reduce throughput. At the size of event data in the TCP segment—timestamp (8 bytes), X-strip number (1 byte), and Y-strip number (1 byte)—we calculated that the maximum throughput was 1.1 M events/s.

Detection efficiency and position resolution were measured, and absorption images were taken [4] with a thermal neutron beam from Japan Research Reactor No. 3 (JRR3) of the Japan Atomic Energy Agency in Tokai, Ibaraki, Japan (JAEA-Tokai). Fig. 17 shows a photograph of the test setup. A PC for acquisition located remotely from the detector (not shown) was connected to the detector with Ethernet. The detection efficiency was 30% compared with a ^{3}He gas detector of 1 inch diameter working at 10 atm pressure. The position resolution was measured using a Cd-plate with a pin-hole of 0.5 mm diameter. Fig. 18 shows measured counts as a function of the readout strip number, with the strips spaced 0.8 mm apart. Using Gaussian curve fitting, we estimated that the position resolution was 0.5 mm. The absorption images were taken with a Cd-plate mask as

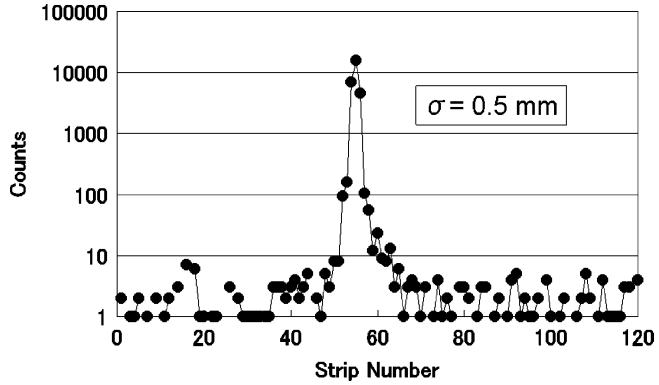

Fig. 18. Measured counts with 0.5 mm diameter pin-hole as a function of the readout strip number.

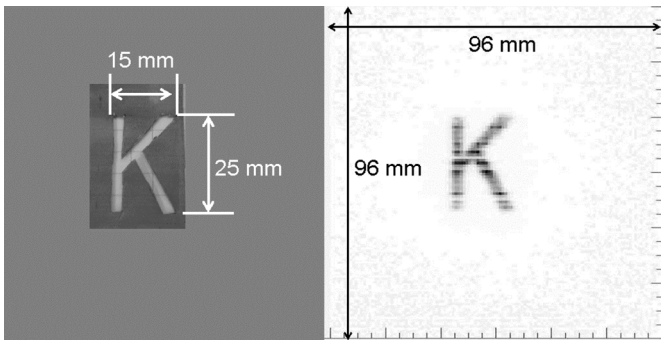

Fig. 19. (Left) Photograph of Cd-plate mask. (Right) Neutron absorption image of the mask.

shown in Fig. 19, left. The image on the right in Fig. 19 shows the result obtained with the mask.

VI. Conclusion

We have developed a prototype of a compact imaging system for GEM detectors. The readout electronics are integrated into the detector, which is connected directly to a PC with an Ethernet hub. Thus, we were able to construct a system consisting of only three main devices: a detector, an Ethernet hub, and a PC. This is a simple and highly flexible system, which can be moved easily. We measured processing rate and tested the system with the thermal neutron beam at JAEA-Tokai. The maximum processing rate was 1.1 M events/s. The measured detection efficiency and position resolution were about 30% and 0.5 mm, respectively. We succeeded in obtaining neutron absorption images. This system allows the use of an imaging system in various fields where it has not previously been possible to use such systems.

Acknowledgment

This work was performed within the framework of the KEK Detector Technology Project (KEKDTP) of High Energy Accelerator Research Organization (KEK), Japan.

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