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CMOS IMAGE SENSOR FOR AMBIENT LIGHT SUPPRESSION BY MEANS OF CURRENT-MODE PIXEL CIRCUIT

電流モードピクセル回路による背景光除去機能付 CMOS イメージセンサ

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CHAPTER ONE

INTRODUCTION

1.1 Background

In recent years, solid-state image sensors market has been experiencing great growth due to increasing demands of mobile imaging, digital still and video cameras, internet-based video conferencing, surveillance and biometrics. As illustrated in Figure 1.1, with over 4000 million $ expected revenues in 2008, image sensors have become a significant silicon technology driver.

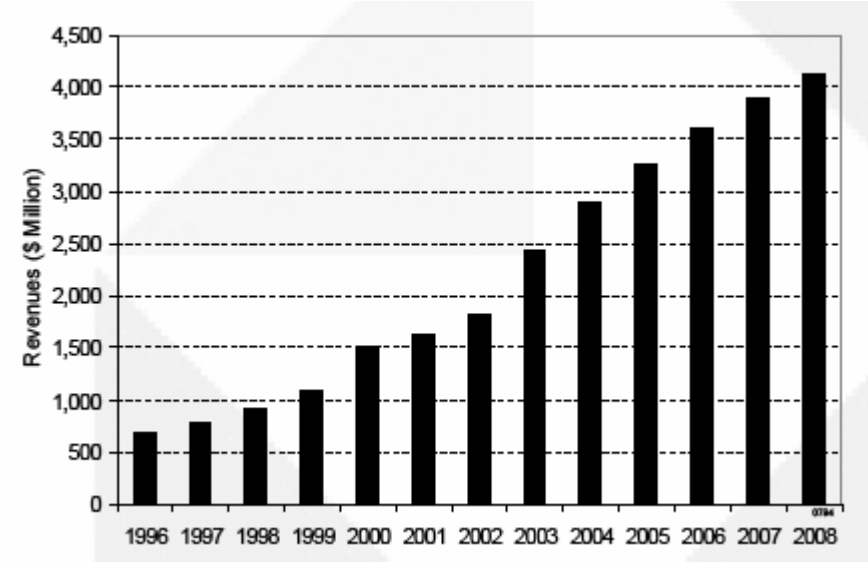


Figure 1.1: Strong long-term growth of the image sensor market [1]

Charge-coupled devices (CCDs) have traditionally been the dominant image-sensor technology. Recent advances in the design of image sensors implemented in complementary metaloxide semiconductor (CMOS) technologies have led to their adoption in several high-volume products, such as the optical mouse, PC cameras, mobile phones, and high-end digital cameras, making them a viable alternative to CCDs. Additionally, by exploiting the ability to integrate sensing with analog and digital processing down to the pixel level, new types of CMOS imaging devices are being created for manmachine interface, surveillance and monitoring, machine vision, and biological testing, among other applications. CMOS image sensors present lower noise at high frame rates and lower power consumption as illustrated in Figure 1.2. They can utilize different applications and function on a single power supply.

As time passes the pixel sizes of CMOS image sensors are shrinking. As pixel size decreases, the image area and sensitivity decrease. In contrast, fabrications costs increase. As number of pixels increases, the file size increases and the frame rate decreases.

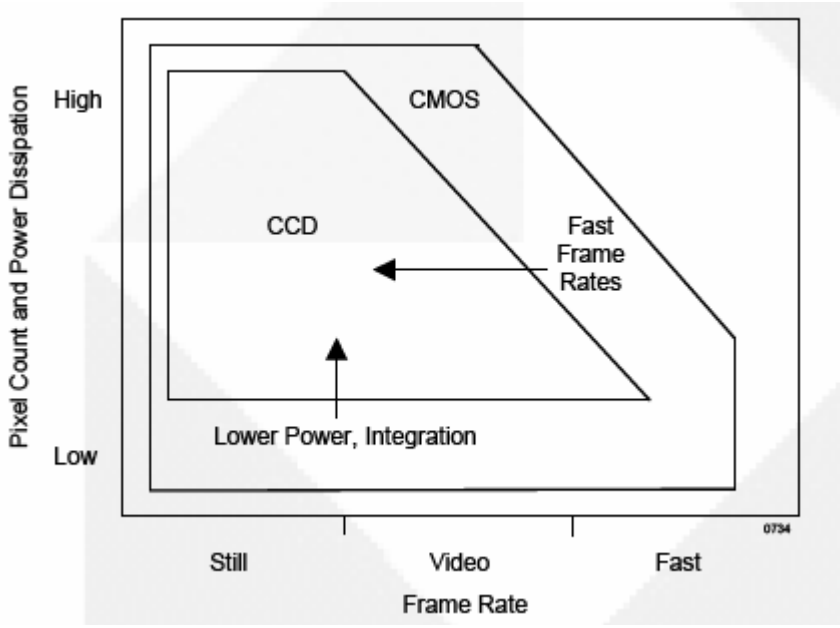


Figure 1.2: CCD vs CMOS [1]

Some of the CCD versus CMOS comparison points made here should become clearer as we discuss image sensor technology in more detail in the following sections.

1.2 CMOS Image Sensing

1.2.1 Photodetection

The most popular types of photodetectors used in image sensors are the reverse-biased positive-negative (PN) junction photodiode and the P+/N/P pinned diode (see Figure 1.3). The structure of the pinned diode provides improved photoresponsivity (typically with enhanced sensitivity at shorter wavelengths) relative to the standard PN junction [2]. Moreover, the pinned diode exhibits lower thermal noise due to the passivation of defect and surface states at the Si/SiO2 interface, as well as a customizable photodiode

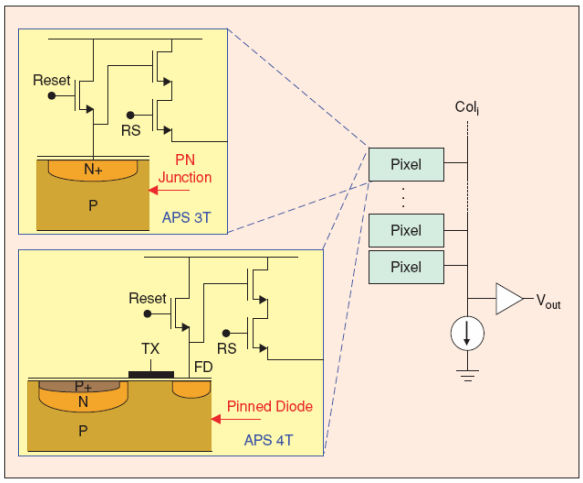


Figure 1.3 Schematics of 3-4T active pixel sensor (APS)

capacitance via the charge transfer operation through transistor TX. However, imagers incorporating pinned diodes are susceptible to incomplete charge transfer, especially at lower operating voltages causing ghosting artifacts to appear in video-rate applications.

If we look at the basic photodetection mechanism utilized inside the pixel, as the range of photocurrents produced under typical illumination conditions is too low (in the range of femto- to picoamperes) to be read directly, it is typically integrated and read out as charge or voltage at the end of the exposure time. This operation, known as *direct integration*, is illustrated in Figure1.4.

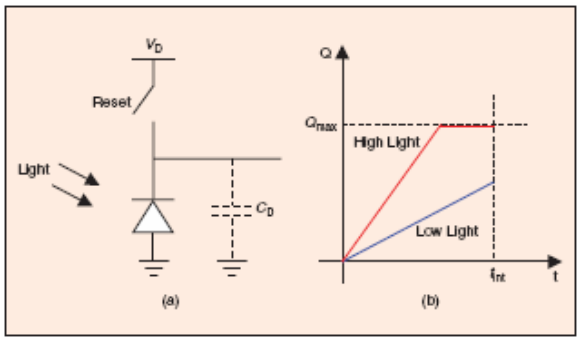


Figure 1.4. (a)A schemantic of pixel operating in direct integration
(b)Charge versus time for two photocurrent values

The photodiode is first reset to a voltage V_D. The reset switch is then opened and the photocurrent i_{ph} as well as the dark current, i_{dc}, are integrated over the diode capacitance C_D. At the end of integration, the charge accumulated over the capacitance is either directly read out, as in CCDs or PPS, and then converted to voltage or directly converted to voltage and then read out as in APS. In both cases, the charge-to-voltage conversion is linear and the sensor *conversion gain* is measured in microvolts per electron. The charge versus time for two photocurrent values is illustrated in Figure 1.4(b). In the low light case, the charge at the end of integration is proportional to the light intensity, while in the high light case, the diode saturates, and the output charge is equal to the well capacity Q well, which is defined as the maximum amount of charge (in electrons) that can be held by the integration capacitance. Figure 1.5 depicts the signal path for an image sensor from the incident photon flux to output voltage.

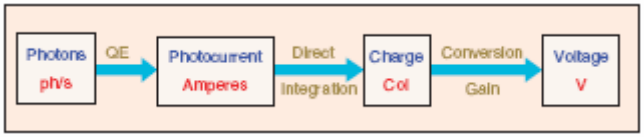


Figure 1.5: A block diagram of signal path for an image sensor

This conversion is nearly linear and is governed by three main parameters; external quantum efficiency, integration time (t_{int}), and conversion gain.

1.2.2 CMOS Image Sensor Architectures

There are different flavors of CMOS image sensor readout architectures. The earliest CMOS image sensor architecture, PPS is shown in Figure 1.6.

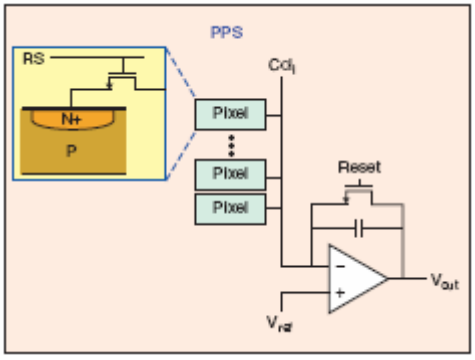


Figure 1.6: A schematic of a passive pixel sensor (PPS)

The PPS pixel includes a photodiode and a row-select transistor. The main advantage of PPS is its small pixel size. The column readout, however, is slow and vulnerable to noise and disturbances. The APS and DPS architectures solve these problems, but at the cost of adding more transistors to each pixel.

The 3-T APS pixel which is shown in Figure 1.7 includes a reset transistor, a source follower transistor to isolate the sense node from the large column bus capacitance and a row select transistor.

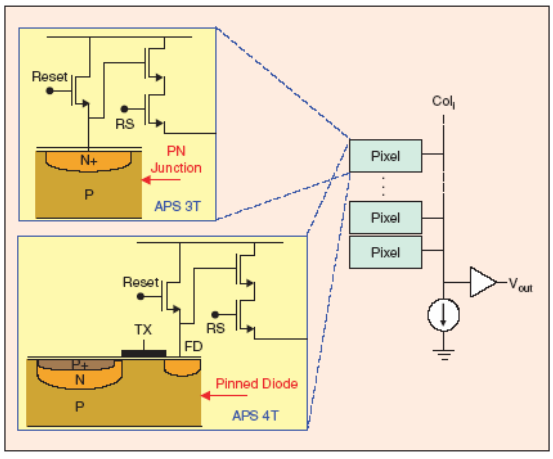


Figure 1.7: A Schematic of a 3-T and 4-T active pixel sensor (APS)

The current source component of the follower amplifier is shared by a column of pixels. Readout is performed one row at a time. Each row of pixels is reset after it is read out to the column capacitors via the row access transistors and column amplifiers.

1.3 Ambient Light Suppression Concept

In recent years different imaging applications have been forcing us to design new application-specific sensor architectures other than the conventional CCD and CMOS APSs. These sensor types are called the smart image sensors which include processing elements on the same chip. Recently many smart image sensors have been reported for various configurations and various functions. For example, an edge detection function [3], a noise reduction function [4], a variable resolution scan [5], a motion detection function [6,7], an image compression function [8] have been implemented as a smart image sensor. Moreover a smart image sensor has a potential capability of a high-speed and high-quality 3-D imaging system, and then some smart image sensors have been developed [9,10] as a high-speed range finder based on the light-section method which has a capability of high range accuracy, and it is efficient for high-quality 3-D image capture in a middle-range target scene. A light-section range finding system consists of a sheet beam projector and a position sensor as shown in Figure 1.8.

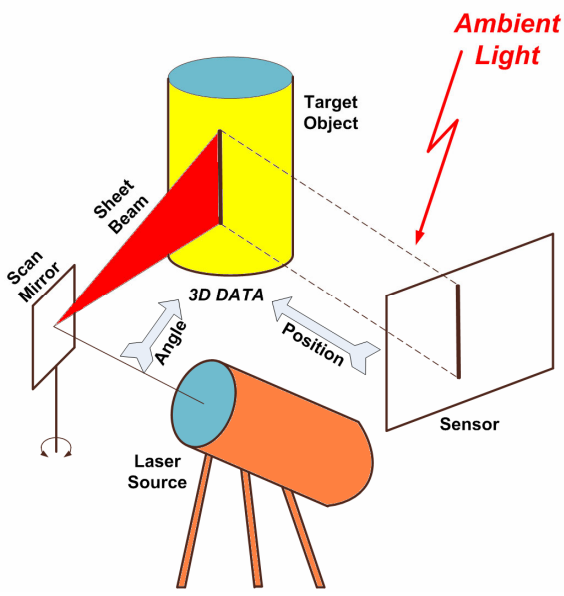


Figure 1.8: Light section range finding system

A sheet beam is projected on a target object at a certain angle, and a position sensor obtains a target scene image. The sensor detects a position of the reflected beam on the sensor

plane, and it provides the incidence angle. The distance between a target object and a position sensor is acquired by triangulation and range information is obtained.

For an accurate range finding four points are essential: High-speed image acquisition, high pixel resolution, high robustness and availability in wide dynamic range of ambient light illumination. Mainly among these we have been concentrating on the sensor which is capable of operating in various ambient light illumination conditions with a weak laser source which in turn decreases the consumed system power. Moreover using a weak laser will enable us to construct a more convenient system in concern with the human health as the strong laser beam is harmful for the human eye. Furthermore, some errors due to reference problems will be eliminated by means of the ambient light suppression. For example, in Figure 1.9 the same amount of projected laser beam is applied to two different pixels one of which is in a dark part of the target surface and the other one is in a bright part. The one in the dark part becomes undetectable whereas the one in the bright part is detectable. This leads to an unfair evaluation. Hence ambient light causes an error-prone operation.

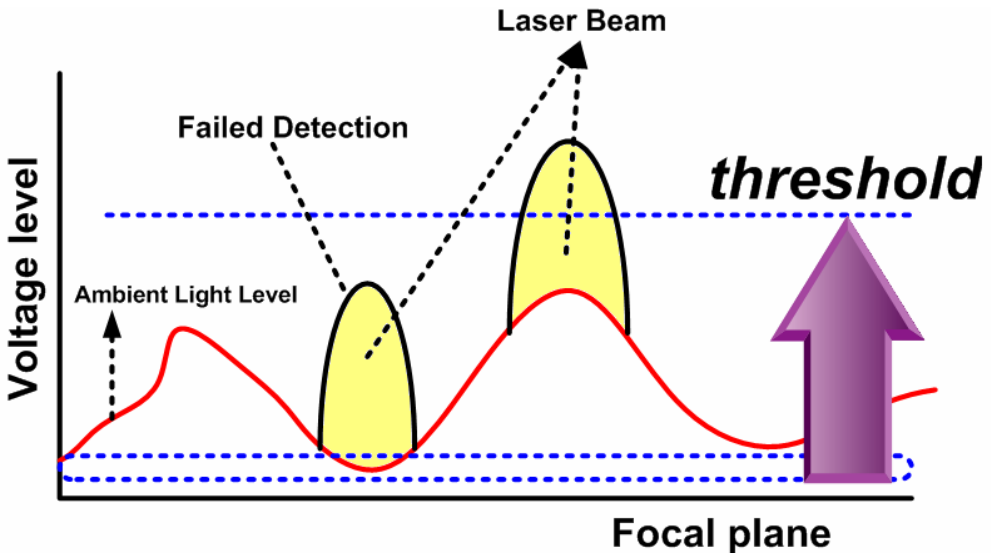


Figure 1.9: Error condition due to the ambient light

To conclude, efficient ambient light suppression is required for having a less error-prone, safer and low power imaging system.

1.4 Overview on Conventional Ambient Light Suppression Methodologies

1.4.1 Voltage-mode Techniques

Several voltage-mode ambient light suppression techniques [11]-[13] have been implemented so far. The operation principle of these sensors is based on two capacitances for the memorization of the ambient light and the total light (ambient plus source). This structure is shown in Figure 1.10.

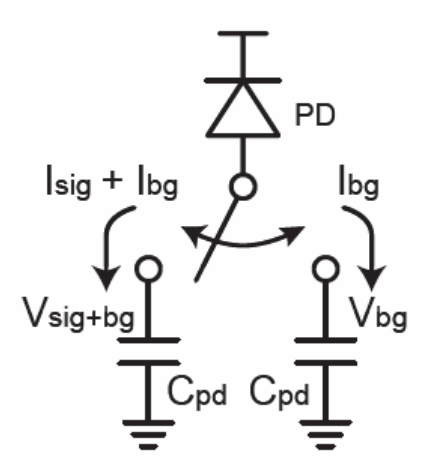


Figure 1.10: Conventional voltage mode ambient light suppression

In the first frame the flashlight is turned on and the total photocurrent namely I_{sig} plus I_{bg} is accumulated in one of the switched capacitors as shown in Fig.10. Then in the second frame the ambient current I_{bg} is accumulated in the other switched capacitor after turning off the flashlight. Then the subtraction signal V_{sig} is given by,

$$V_{sig} = V_{sig+bg} - V_{bg}$$

$$= \sum_{i=0}^{n} \frac{(I_{sig} + I_{bg}).\Delta T}{C_{pd}} - \sum_{i=0}^{n} \frac{I_{bg}.\Delta T}{C_{pd}} \quad [1]$$

Because the capacitances are used as the memory, a voltage saturation problem arises especially in high ambient light conditions. V_{sig} becomes limited by the below equation.

$$V_{sig} < V_{sat} \quad [2]$$

Hence this lowers the dynamic range. The voltage mode ambient light suppression techniques can be classified into two branches as pixel-level and column parallel techniques which are described in detail in the following subsections.

1.4.1.1 Pixel-parallel Voltage-mode Ambient Light Suppression

In Figure 1.11 a pixel circuit employing ambient light suppression is shown. It is based on in-pixel Correlated Double Sampling(CDS) method which is reported in [14]. To mention about its operation principle, first the photodiode is reset to VDD by RST signal. In the photocurrent integration phase, V_{sh} is initialized to V_{ini} by means of ϕ_2. Then in the second frame V_{pd} is reset again by turning on ϕ_1. Finally, the output voltage, V_{out}, is obtained according to the signal level, V_{sig}, when ϕ_1 turns off. In the next frame during the photocurrent integration, the pixel values are readout.

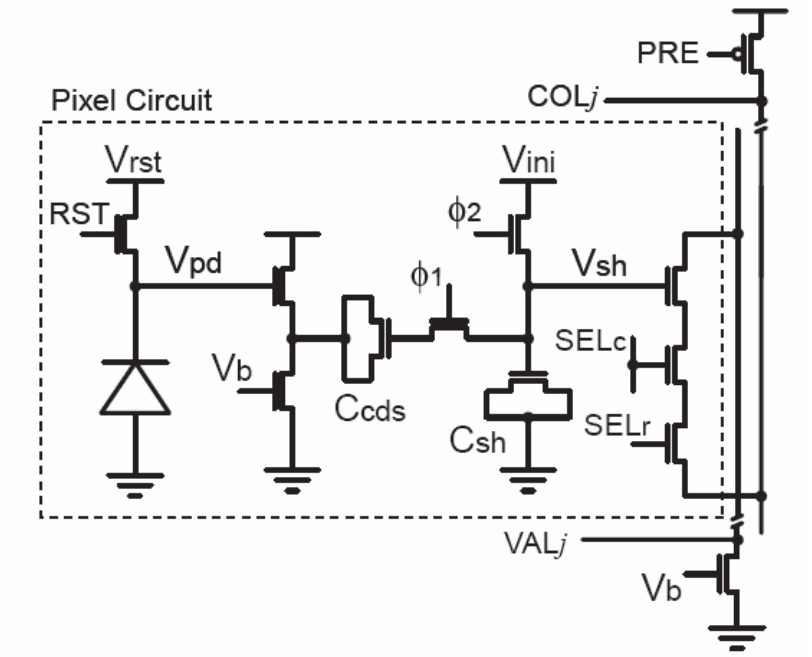


Figure 1.11: In pixel CDS ambient light suppression

This operation is capable of reset noise suppression by the in-pixel CDS operation. On the other hand, the pixel circuit is also capable of ambient light suppression as shown in Figure 1.12. In the first frame, a sheet beam projector turns off, and the pixel circuit acquires an ambient light level, V_{bg}. V_{sh} is boosted from V_{ini} by V_{bst}, which keeps up with V_{bg}. that, a sheet beam projector turns on, and then the pixel receives the total level, V_{sig}, of the ambient light and the projected beam. Finally, the pixel circuit provides the output level, V_{out}. The output level represents the project beam intensity since V_{sh} has been boosted according to the ambient light level.

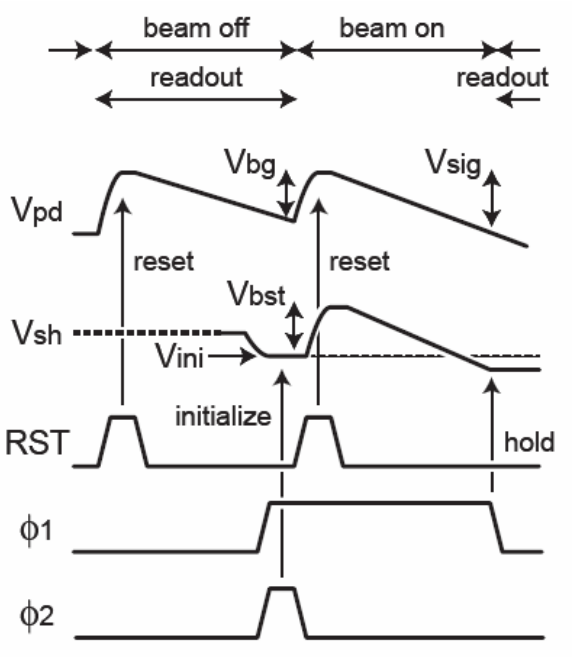


Figure 1.12: Signal flow of in pixel CDS ambient light suppression

1.4.1.2 Column-parallel Voltage-mode Ambient Light Suppression Techniques

Column-parallel suppression technique [14] is based on adaptive reset level control which is shown in Figure 1.13.

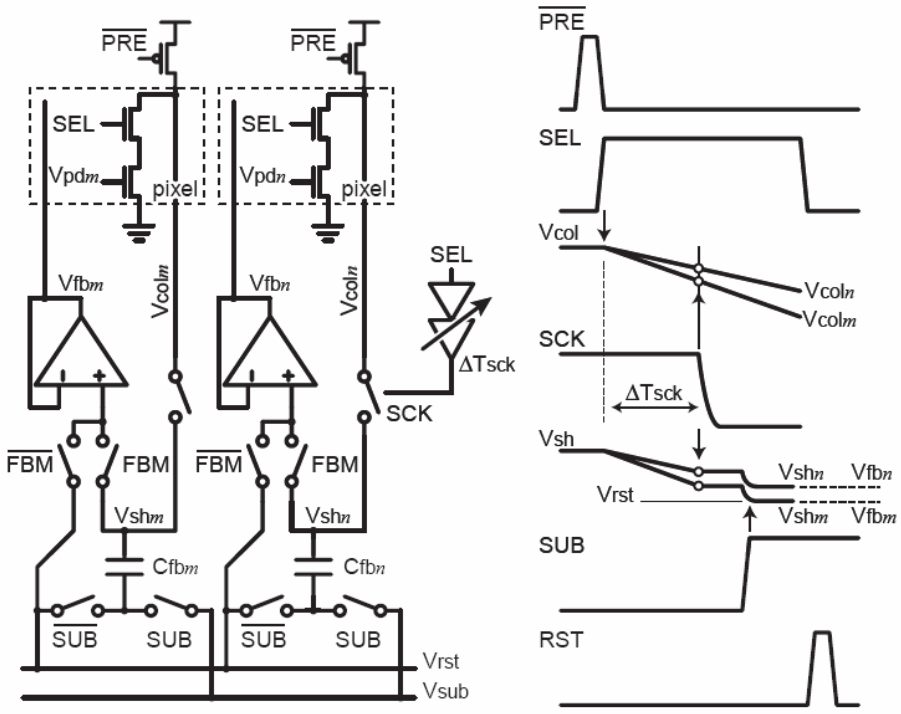


Figure 1.13: Column-parallel ambient light suppression technique

Here the pixel circuit is composed of a photodiode and 3 transistors which are for reset, source following and selection purposes. The column voltages are obtained by the column-parallel feedback circuits by means of switch SCK. These sampled voltages which correspond to pixel values resulting from the ambient light, are used for the next reset levels. So the next reset levels, V_{fb}, are boosted from the initial reset level by the ambient light level. Note that the projected sheet beam is turned on in the next frame. So actually the ambient light is suppressed in the next frame. It also has a capability of suppression of the select timing variations among column lines and the device fluctuations of the readout transistors which is not present in the pixel-level suppression.

1.4.2 Current-mode Techniques

Actually, until now there is no work which is specifically based on current-mode ambient light suppression. Recently a demodulation position sensor has been presented which has also ambient light suppression capability [14]. The pixel circuit of this work is shown in Figure 1.14.

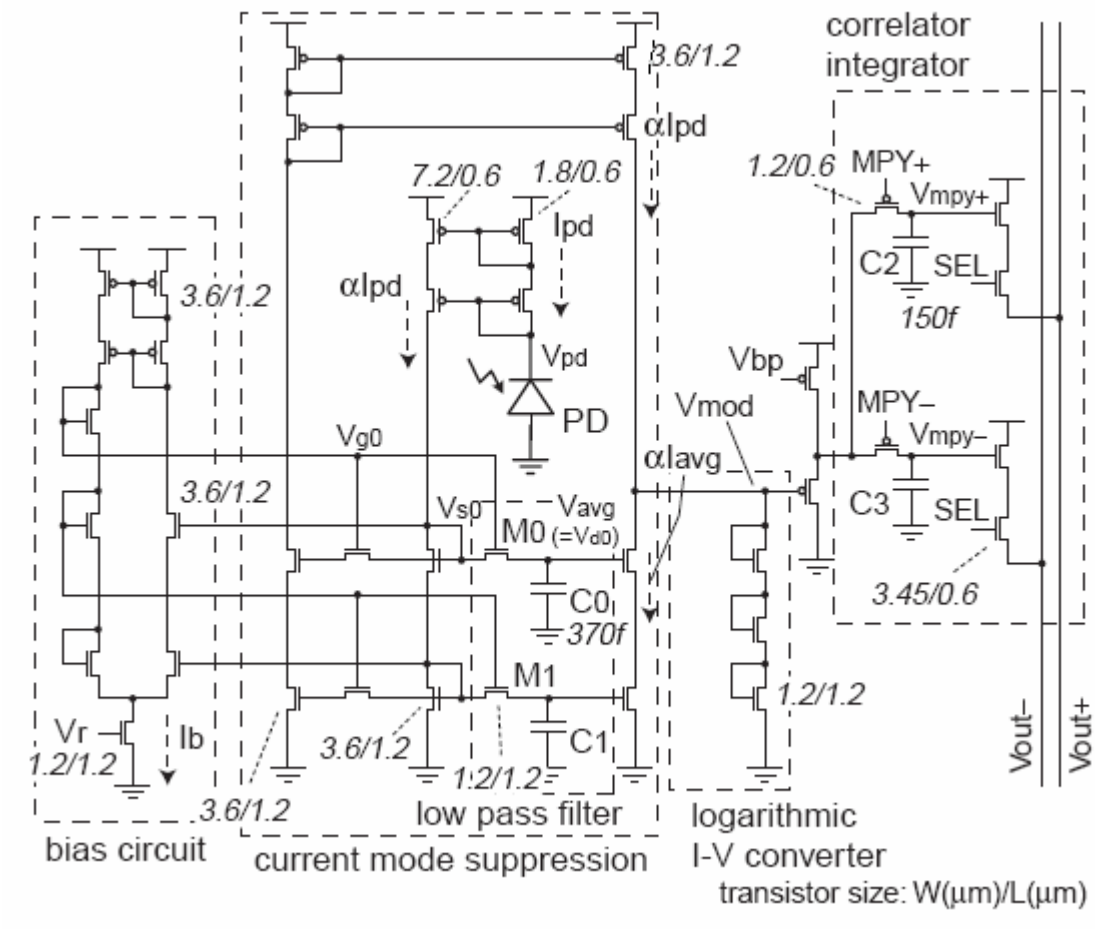


Figure 1.14: Pixel circuit schematics of current-mode ambient light suppression technique

In this work, a laser beam modulated by a pulse generator is projected on the target object. The photo detector receives a reflection of the projected laser beam and the background illumination together. A photo current generated by the incident light is fed into a low-pass filter. An output current of the low-pass filter is subtracted from the original photo current. The subtraction is realized using a current mode circuit instead of a voltage mode circuit to avoid saturation. The output current is alternating when the incident light includes a modulated light.

The main drawback with this sensor is that it is suffering from large pixel circuit area. This results in a very low fill factor. There is not so much room for implementing the photodiode so photodetection capability of the sensor is drastically lowered to provide a reasonable sensor resolution.

Traditionally, the switched-capacitor technique [15,16] has been employed extensively in the analogue interface portion of mixed-mode designs. However, switched-capacitors are not fully compatible with digital CMOS processing technology and, as the technology advances further, the drawbacks of switched-capacitors are becoming more significant. Switched-capacitors traditionally require high quality linear capacitors, which are usually implemented using two layers of polysilicon. The second layer of polysilicon used by switched-capacitors is not needed by purely digital circuits and may become unavailable as process dimensions shrink to the deep submicron range. The trend towards submicron processes is also leading to a reduction in supply voltages, directly reducing the maximum voltage swing available to switched-capacitors and consequently reducing their maximum achievable dynamic range. With lower supply voltages the realization of high speed high gain operational amplifiers will become more difficult.

The difficulties faced by switched-capacitors, and other ‘voltage-mode’ analogue interface circuits, in coping with the advance of digital CMOS processing technology has revived interest in ‘current-mode’ techniques [17]. The switched-current technique is a relatively new analogue sampled-data signal processing technique which fully exploits digital CMOS technology [18]. Switched-current circuits do not require linear floating capacitors or operational amplifiers.

Because of all of these benefits introduced by the switched-current technique, we found it more convenient to use a switched-current ambient light suppression method for our CMOS smart image sensor.

1.5 Purpose and Composition of this thesis

Ambient light suppression research has been conducted in Asada & Ikeda Lab, since the former Phd student Mr. Oike. His research was mainly based on voltage-mode ambient light suppression. Although one sample [18] of current-mode ambient light suppressing CMOS smart image sensor was developed, because of the large pixel area and low fill factor, that research couldn't meet the reasonable pixel resolution requirements. So as a continuation of that work, we decided to implement a new current-mode ambient light suppression cell in order to utilize it as a pixel circuit for the CMOS smart image sensor. This novel architecture would enable us to have a better sensor resolution and higher fill factor in other words higher imaging quality.

To conclude, the purpose of this thesis is designing a CMOS smart image sensor employing a current-mode pixel-level ambient light suppression which will combine considerable linearity with the detailed pixel-level suppression quality.

CHAPTER TWO

CELL DESIGN

2.1 Operation Principle of the Proposed Pixel Circuit

As the voltage-mode techniques have been suffering from several problems mentioned in the first chapter, a current-mode technique has been implemented in the proposed architecture. The ambient light is memorized in its current form as the photodiode current and then suppressed in each pixel parallely. There is a current memory in each pixel and the ambient light is suppressed in two steps. In Figure 2.1 the step diagram of the suppression operation is shown.

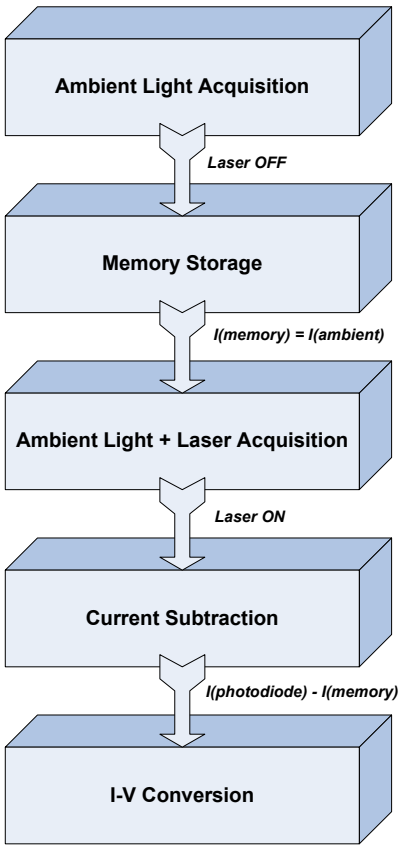


Figure 2.1: The block diagram of the operation principle

At first, the source light is turned off and the ambient light is memorized in the current memory as the photodiode current. Then in the second step, the source light is also turned on and the total light namely ambient plus the source is induced in the photodiode. Finally the previous memorized ambient current is subtracted from this total current and the sole source current is obtained. Then I-V conversion takes place in each pixel and this analog voltage information is transferred to the column line after the pixel is selected by the row and column decoders. Note that this is a pixel-parallel operation so all the suppression process is done simultaneously enabling the system operate in high frame rates. In the next section, the

current memory used for storing the ambient light is introduced and its operation details are explained.

2.2 Switched Current Memory

2.2.1 Basic Switched Current Memory Cell Architecture

The switched current circuit technique is a current-mode signal processing technique which utilizes the ability of a MOS transistor to maintain its drain current, when its gate is open-circuited, through the charge stored on its gate oxide capacitance. Switched current (SI) memory is a basic building block in switched-current circuits. It can be employed in different signal processing and data conversion operations, e.g., current differentiation [19], sigma-delta-modulation [20], and A/D or D/A conversion [21]. The basic memory cell constructed with this technique is illustrated in Figure 2.2.

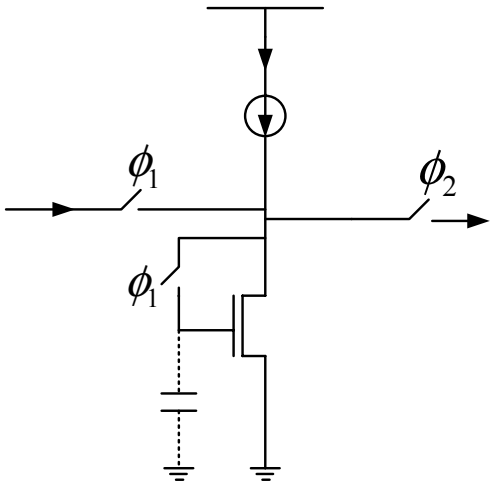


Figure 2.2: Basic switched current memory cell

On phase ϕ_1, the input current ***i*** is supplied to memory cell. This input current adds to the bias current ***J*** and the current ***J+i*** flows initially into the discharged gate-source capacitor C. As C charges, the gate-source voltage V_{gs} rises and when it exceeds the threshold voltage, M_1 conducts. Eventually, when C is fully charged, the whole current ***J+i*** flows in the drain of M_1.

During phase ϕ_2, gate switch of M_1 is opened and the value of V_{gs} at the end of phase ϕ_1 is held on capacitor C and sustains current ***J+i*** in the drain of M1. With the input switch now open and output switch closed, the imbalance between the bias current, J and the drain current, ***J+i***, forces an output current, $i_0 = -i$, to flow throughout phase ϕ_2. The output current,

i_0, is a memory of the input current i. Of course this is achieved by virtue of the charge retained on capacitor C. The current memory operates without the need for linear floating capacitors and so retains the important advantage of being compatible with digital VLSI processes.

2.2.2 Switched Current Memory Cell for Low-Power and Weak-Current Operations

Related with the basic switched current memory there are several drawbacks which prevent us to use it for very low currents such as a photodiode current. Charge injection, channel-length modulation effect and voltage coupling through parasitic capacitors can be considered among these important drawbacks.

As the photodiode current is generally considered to be low, a switched current memory [22] which can operate in a pico-to-nanoampere range with good accuracy, is employed in the pixel circuit which is illustrated in Figure 2.3.

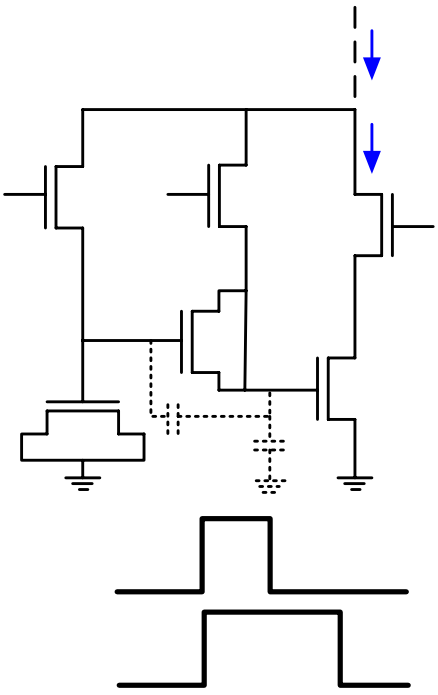


Figure 2.3: A switched current memory cell for weak current applications

Here, T_1 is the storage transistor, T_2 and T_5 act as switches, and T_3 and T_4 serve as capacitors. A fixed voltage V_b is applied at the gate of T_6 to stabilize the drain voltage of T_1 in order to shield the critical gate node of T_1 from the voltage variation at node V_{d2} and also to reduce the channel-length-modulation effect on the current of T_1.

To explain the current memorization, at first both SW1 and SW2 are turned on for a coarse adjustment of V_{g1}. In this case as V_{g1} becomes equal to V_{g3}, the gate-to-source voltage of T_3 is zero so T_3 is off. Then T_5 is turned off and T_2 remains on for a fine adjustment of the gate voltage. When T_5 is turned off, Vg1 is lowered by the charge injection of T_5, resulting in i(memory)<i(in). Consequently V_{d2} increases, raising the source-to-gate voltage of T_3. A channel is then created in T_3 and, as its drain and source are shorted, T_3 operates in the triode mode, drawing charge from the gate capacitance of T_1. This charge redistribution between gate capacitance of T_1 and the channel of T_3 restores V_{g1} to a value that is required to support i(memory) = i(in).

When T_2 is turned off, , the charge released from the source of T_2, is divided into two parts: Δq_{13} ,the charge injected into the branch of C_3 in series with C_1, and Δq_1, the charge injected in the branch of C_4, where C_4 is the equivalent capacitance of transistor T_4. The released Δq causes a voltage change of ΔV_{g3} at the gate of T_3, whereas Δq_{13} induces a voltage change of $\Delta V_{g1} = \Delta q_{13} / C_1$ resulting in an error in the current of T_1. The ratio $\lambda = \Delta q_{13} / \Delta q$ is given by

$$\lambda = \frac{\Delta q_{13}}{\Delta q} = \frac{\frac{C_1.C_3}{C_1 + C_3}.\Delta V_{g3}}{(C_4 + \frac{C_1.C_3}{C_1 + C_3}).\Delta V_{g3}} = \frac{1}{1 + \frac{C_4}{C_3} + \frac{C_4}{C_1}} < 1. \quad [3]$$

This charge injection scheme is illustrated in Figure 2.4.

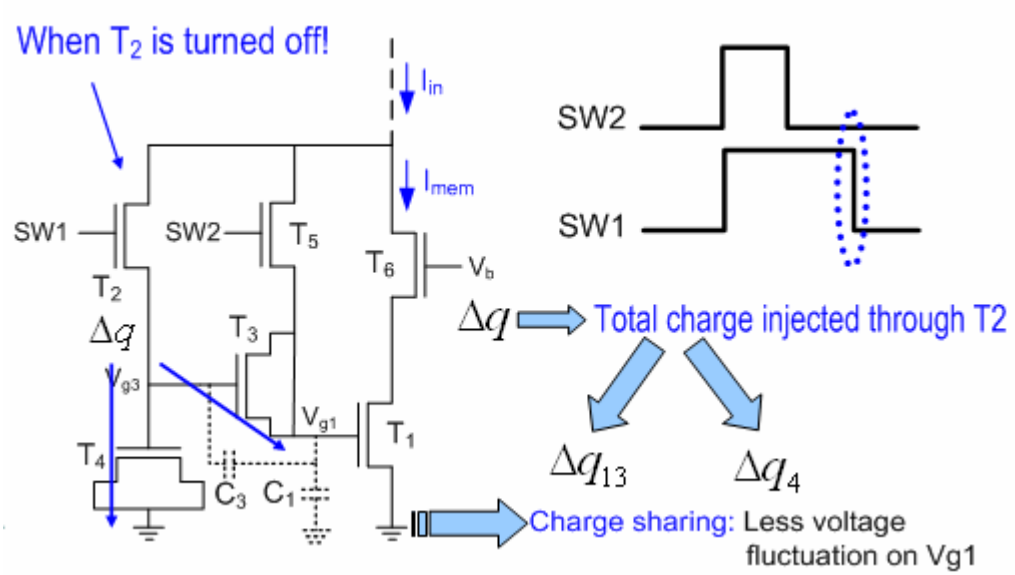


Figure 2.4: Charge injection elimination scheme

The capacitances C_1, C_3, and C_4 can be estimated from the transistor sizes. If node V_{g1} is directly connected to V_{d2} through T_3, the quantity of charge injected into node V_{g1} is Δq .In this switched current memory circuit, the charge injected into the critical node V_{g1} is $\Delta q_{13} = \lambda \Delta q$ which is less than Δq , as λ is always less than unity. If, for example, $C_1 = C_4$ and $C_4 / C_3 = 8$, a reduction of 90% in gate voltage variation can be obtained. This reduction of charge injection is realized by passing a large portion of the charge Δq to the gate capacitor of T_4. So this circuit topology enabled us to have a better ambient light storage performance compared to the conventional switched current memory architectures. In the next section, the pixel circuit in which this SI memory was utilized will be introduced and pixel-level ambient light suppression scheme will be described.

2.3 Proposed Pixel Circuit Architecture

As mentioned in the previous section the ambient light suppression process takes place in each pixel. So a specific switched current memory is placed in each one. In Figure 2.5 the block diagram of the pixel circuit is shown. The pixel circuit consists of a photodiode, a switched current memory , an I-V conversion circuitry and a source follower acting as a signal amplifier isolating the highly capacitive column bus from the pixel.

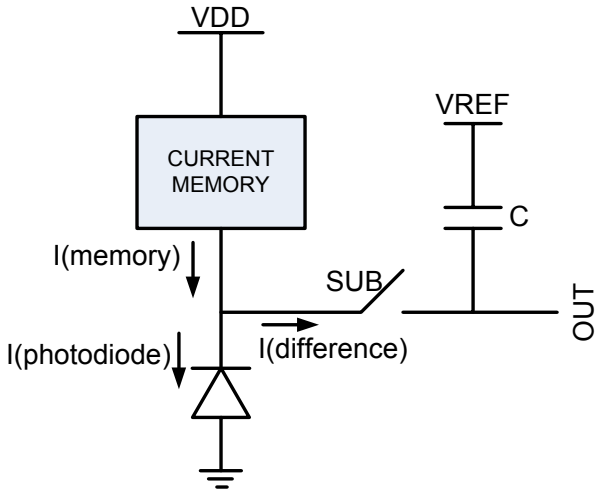


Figure 2.5: Block diagram of the proposed pixel circuit

Here in the first frame the source light is turned off. So the current passing through the photodiode corresponds to the ambient light current. At this moment the subtraction switch (SUB) is open and as a result, the ambient current is stored inside the current memory. Then in the second frame source current is also turned on and the photodiode current becomes the source current plus the ambient current. Right at the point the source light is turned on, the SUB switch is closed and a current subtraction operation takes place giving the sole source

current as the result. Next, I-V conversion operation takes place inside the pixel and integration capacitance C is integrated by this source current. This integration is done for a certain small duration not to decrease the output voltage down to GND. The same reference voltage is applied to all pixels so the different reference problem is eliminated because of the ambient light. After the integration, the pixel value is readout by the output source follower.

As to give a better understanding, the pixel circuit schematics is illustrated in Figure 2.6

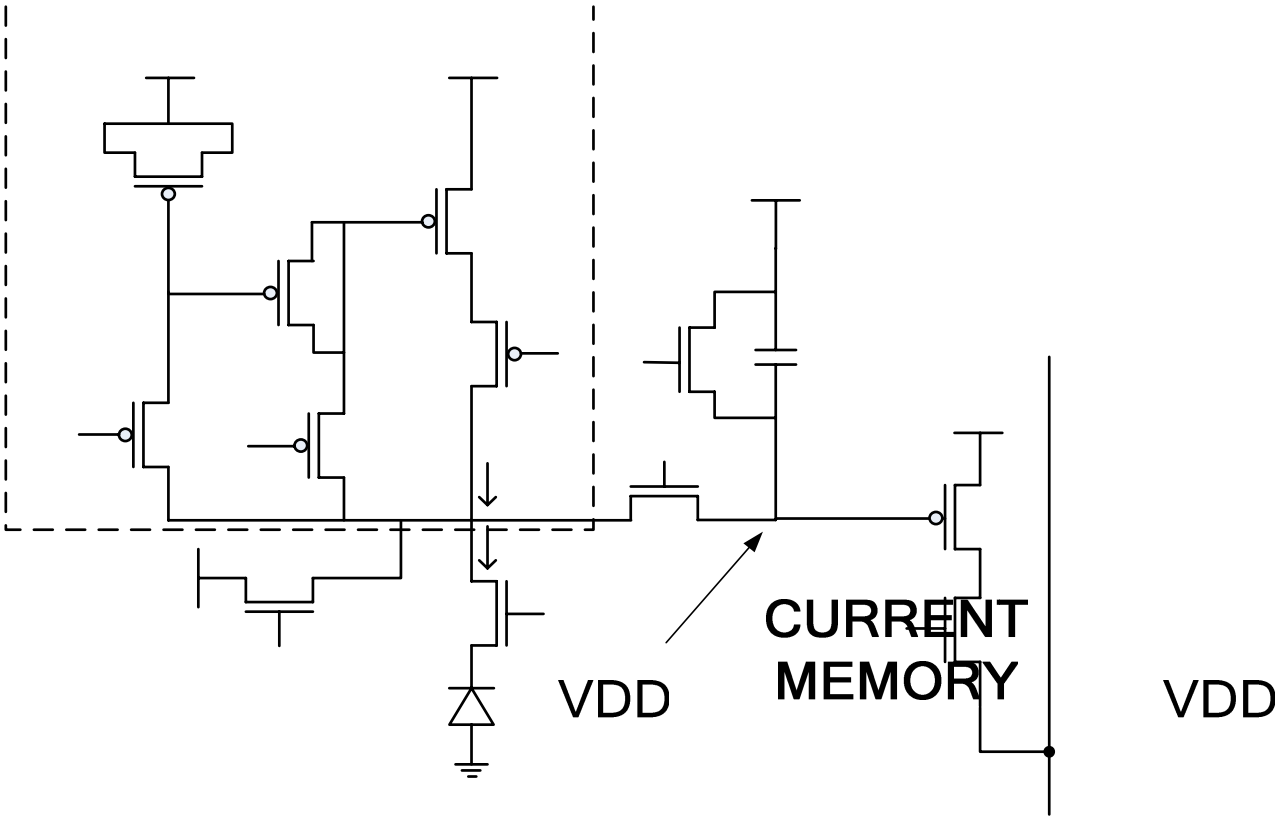


Figure 2.6: Proposed Pixel Circuit Schematics

Related with the pixel circuit design of the proposed sensor, a PMOS version of this switched current memory is employed. Here T_1 is the storage transistor and T_2 and T_5 act as current sampling switches. T_7 is placed for making it sure that the photodiode is always operating at the reverse bias. A constant voltage bias is applied from node V_n. Inside the current memory, T_6 is used in order to shield the drain voltage of the memory transistor, T_1 from the node V_{mem} as it is subject to change during subtraction. Otherwise the channel length modulation effect will considerably disturb the current on the memory transistor and this will yield performance loss for the switched current memory. Until the subtraction phase the integration capacitance is reset by the *cap_reset* switch and this switch is opened right at

the time SUB is closed. The reference voltage V_{ref} is adjusted according to the average of the typical values of V_{d2} in order to provide a stable current subtraction operation.

The signal waveform for image acquisition in pixel circuit is shown at Figure 2.7. These signals were constructed at Hspice and various schematics simulations were performed. The circuit was designed at CMOS 0.18um technology with 1.8V VDD supply.

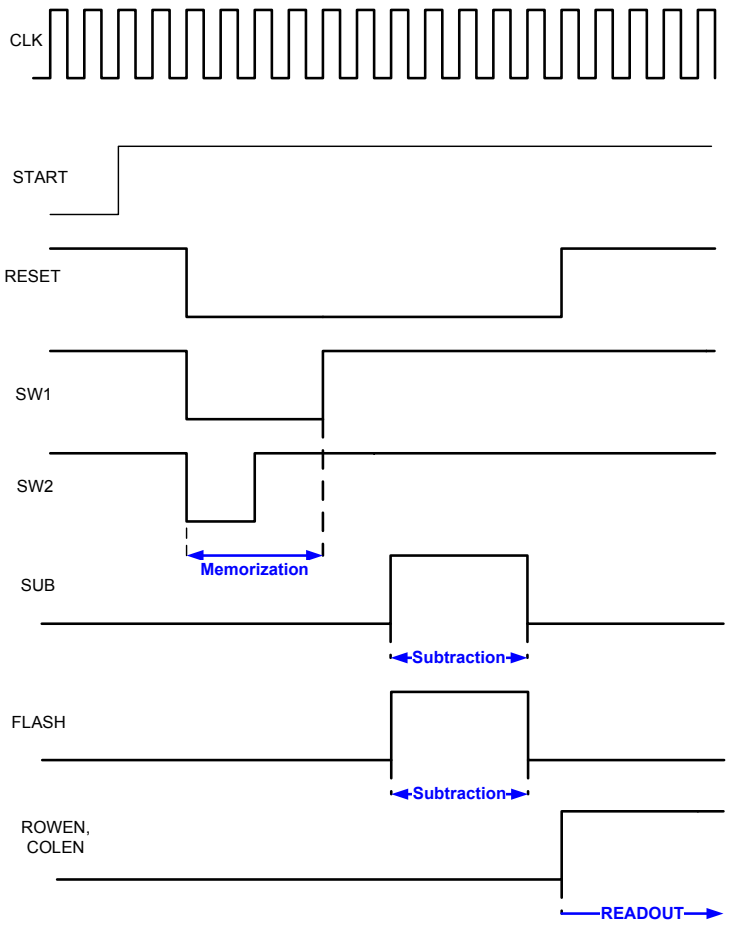


Figure 2.7: Input signal waveform for the pixel circuit

So, as to explain the operation principle, at first current memorization is realized as explained above and illustrated in Figure 2.8.

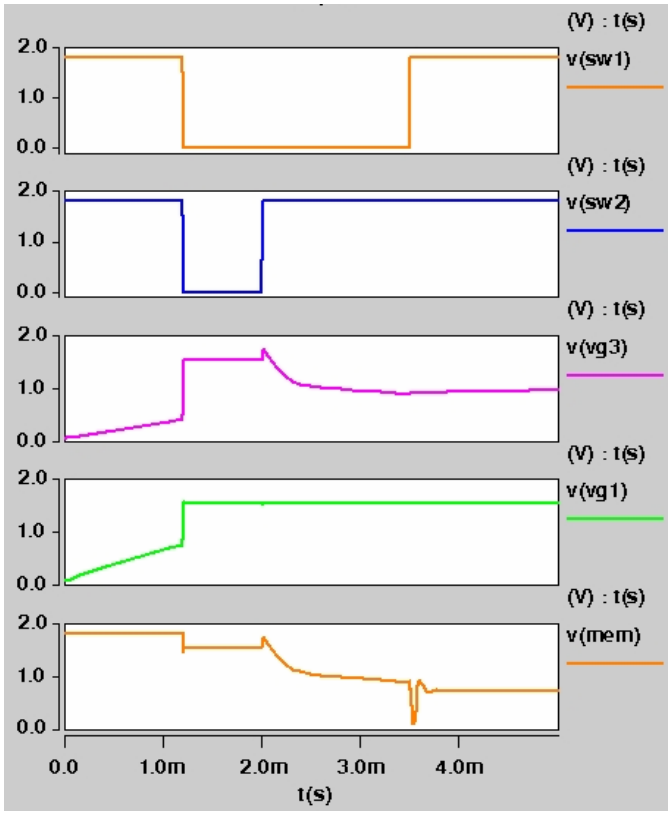


Figure 2.8: Current Memorization Simulation

After the current memorization, the laser is turned on and SW3 is closed simultaneously as shown in Fig.5. So the memorized ambient current is subtracted from the photodiode current which results in the sole laser current. That laser current integrates the capacitor C for a certain duration, decreasing the output node's voltage. After the SW3 is opened at the end of this certain subtraction duration, we have a voltagewise information on the output node according to incoming laser amount. If no laser comes on the pixel there is no voltage change in the output node and there will be a corresponding voltage decrease in the output node with respect to the incoming laser amount. This subtraction operation is shown in Figure 2.9 for different laser current values.

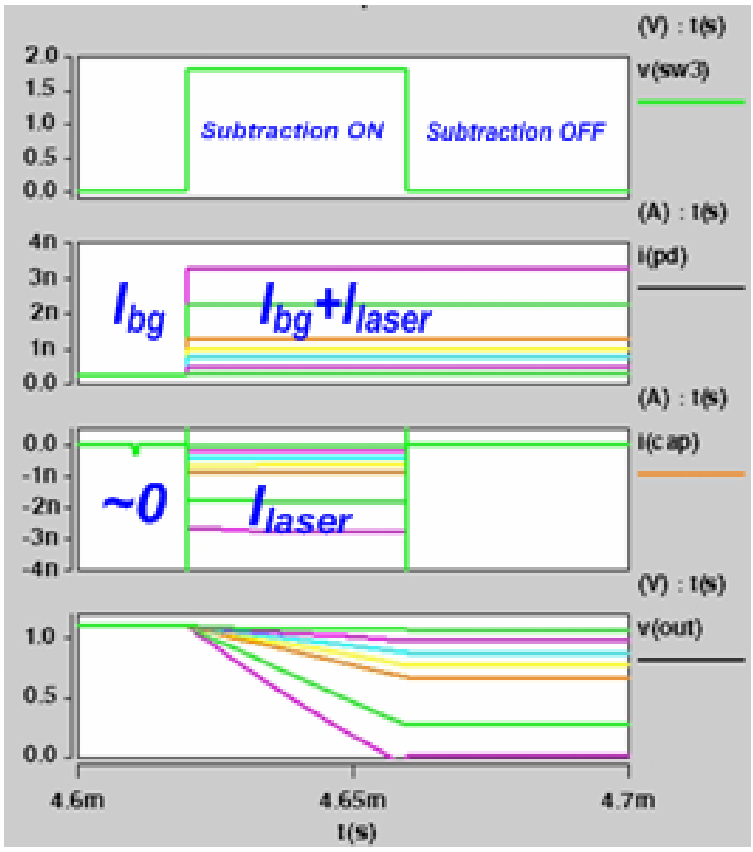


Figure 2.9: Subtraction simulation

The family of curves in Fig. 5 belongs to different values of laser current as the laser amount coming to each pixel will be different according to the distance of the sensor to the reflection point on the target scene. This is a pixel-parallel operation so ambient light suppression takes place on whole pixel array simultaneously. This parallelism will increase the operation speed also. Further, because the ambient light is suppressed, not a powerful laser will be needed for imaging. This will in turn decrease the system power. Moreover with a weak laser source the system will be more suitable for the human eye as a powerful laser beam is harmful for the human eye.

The layout of the pixel circuit is illustrated in Figure 2.10. It has a square shape of area 15umx15um. The sensor has a resolution of 256x256. The fill factor namely the ratio of photodiode area to whole pixel area is %24.

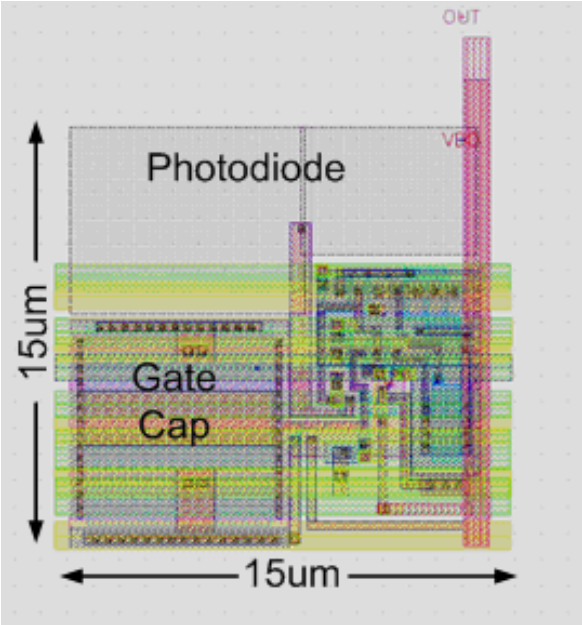


Figure 2.10: Layout of the pixel circuit

2.4 Simulation Results

In order to evaluate the performance of the proposed sensor, various simulations were performed in Hspice. These were all based on 0.18um CMOS technology. In the next section the simulation results are presented starting from the pixel performance.

Both schematics and layout simulation were held on the pixel which ended up with almost similar results. Memorization, subtraction and readout phases were carefully simulated. In Figure 2.11 the simulation environment, generated signals and responses of some important nodes are illustrated.

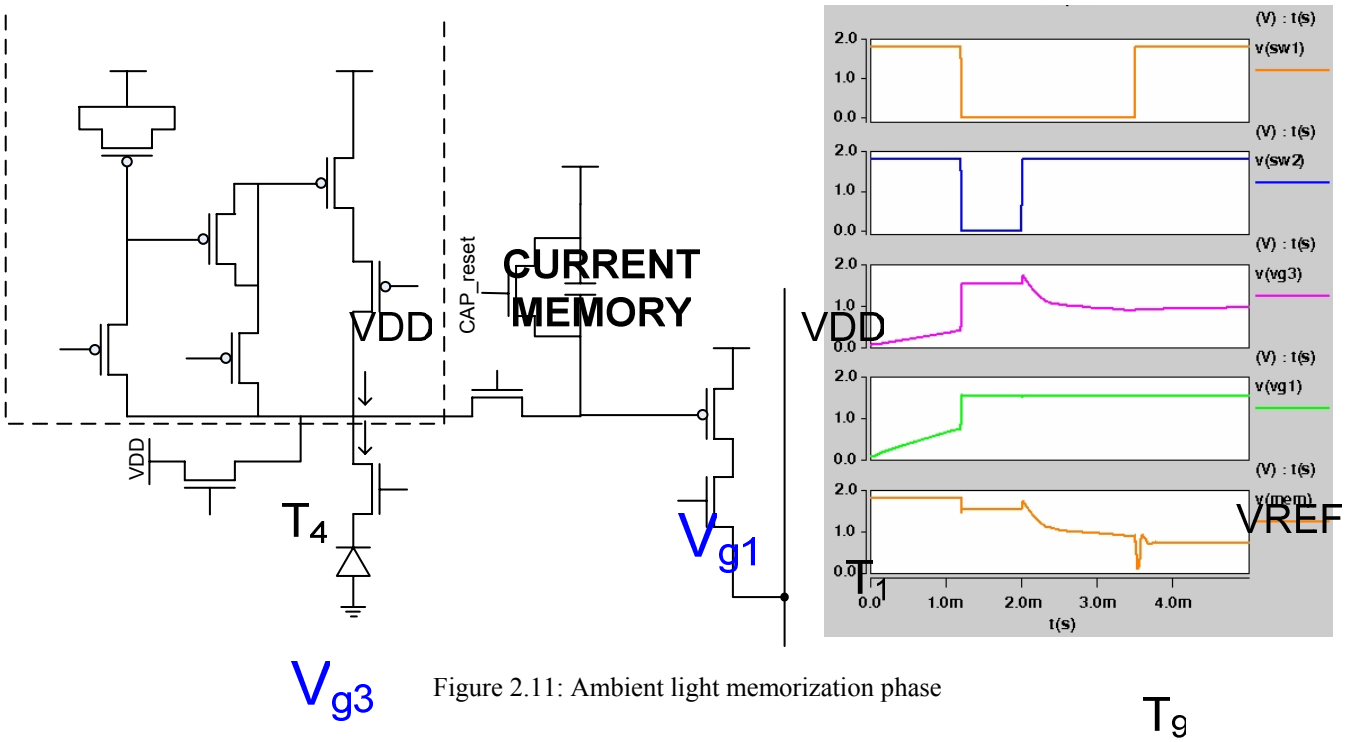


Figure 2.11: Ambient light memorization phase

First a positive pulse of RESET turns the transistor T_{10} on, setting the voltage Vmem to a high level. Then SW1 and SW2 are closed so current sampling starts. The ambient current is stored on the transistor T_1. A constant analog voltage is applied to V_p and V_n. Through this interval the node voltages V_{g1} and V_{g3} are tuned according to the ambient current stored. So at the end of this interval I_{mem} becomes approximately equal to I_{bg} namely the ambient current.

The simulation results show that the switched current memory can store the ambient light successfully in the range 0.5pA-20nA. For the currents greater than 20nA, the node voltage V_{mem} decreases drastically so the reverse bias voltage room for the photodiode becomes very narrower which results in nonlinear operation. In other words, the relation between the light coming on the photodiode and the current induced on it becomes nonlinear. This is an undesired situation.

Through the memorization simulations, the ambient current is swept inside the 0.5pA-15nA interval, a 250pA source light was assumed which is very weak. This was done by placing an independent current source instead of the photodiode. The results show that the switch current memory can store the current with an efficiency of more than 99%. This is illustrated in Figure 2.12 in the next page.

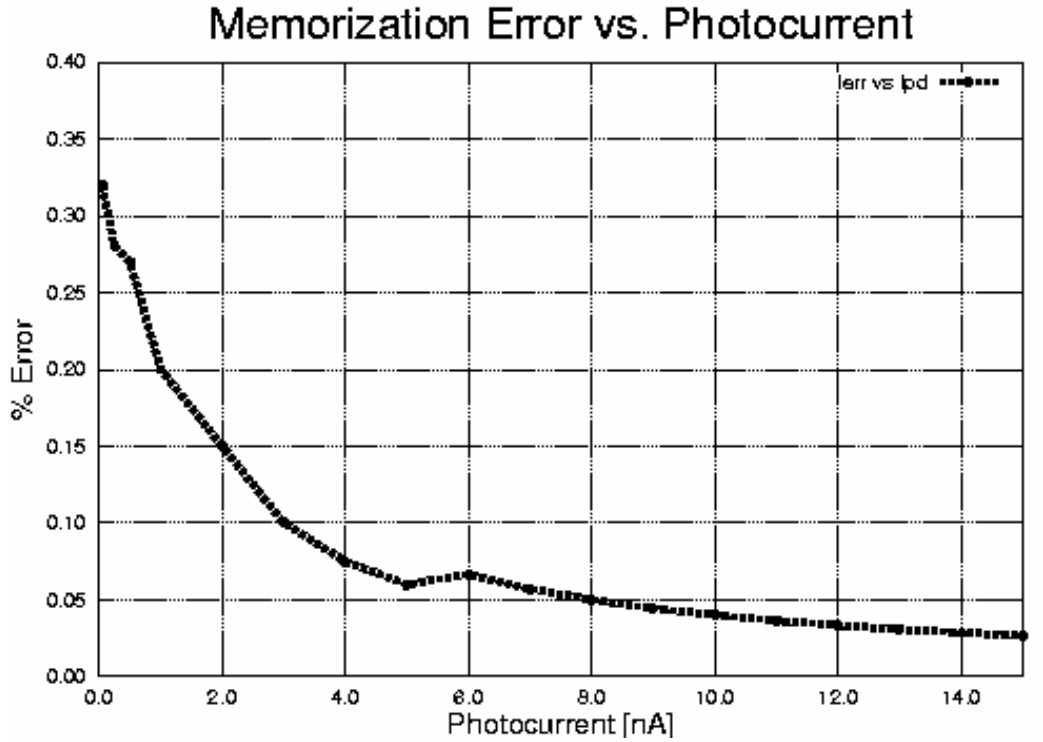


Figure 2.12: Memorization Performance of the Pixel Circuit

The ambient light suppression namely the subtraction phase was also carefully simulated and shown in Figure 2.13. In this phase the switch SW3 is closed for a certain duration. Just before this time interval the transistor T_9 is turned off by a low pulse from CAP_RESET. Through this time interval, only the source current is integrated on the integration capacitance so the node voltage V_{out} starts to decrease. This voltage decrease is directly proportional with the source current. Finally, after SW3 is turned off again, a certain voltage information is acquired on V_{out}.

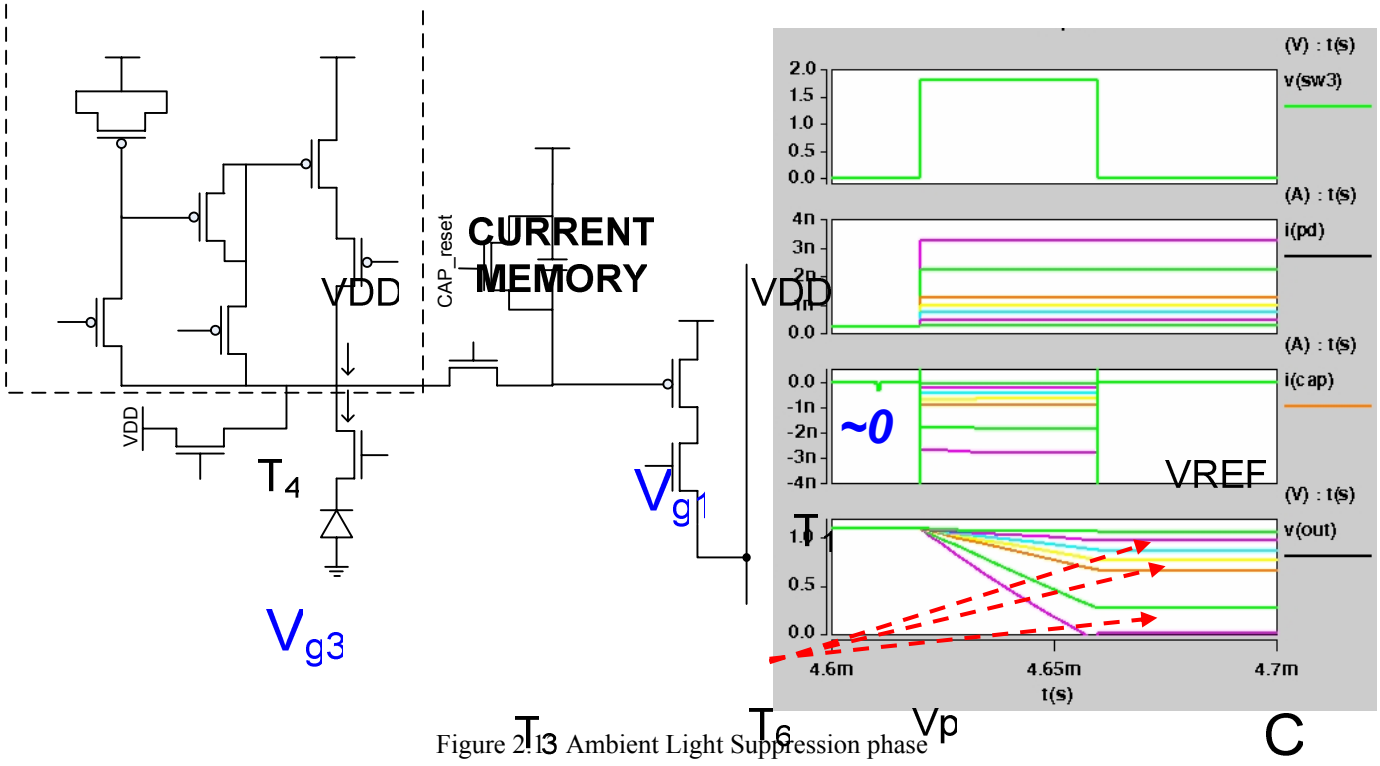
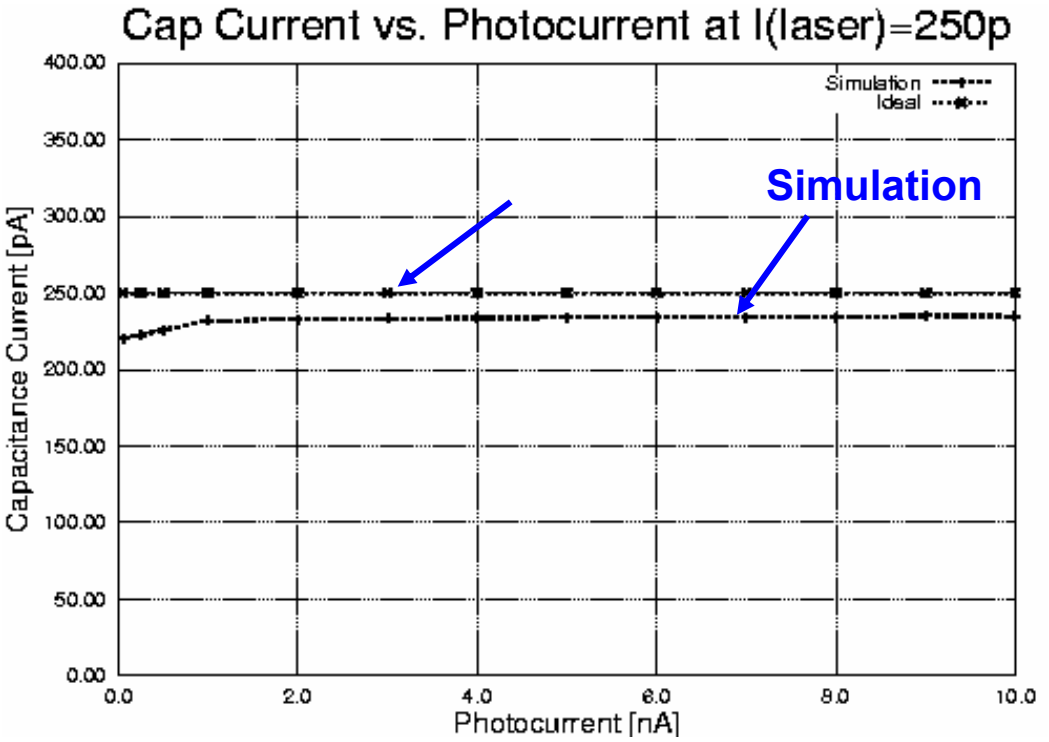


Figure 2.13 Ambient Light Suppression phase

The simulation results show that the subtraction efficiency is around 90% when the ambient current is swept inside interval 50pA to 10nA. As shown in Figure 2.14 when a weak source light of 250pA is applied the capacitance current becomes very approximate to that value. This ensures an accurate current operation over a very wide current range, particularly when the transistors of the switched current memory are operating in very weak inversion mode. As a result this enables us to suppress the ambient light by using a very weak source light.

A different voltage value will be obtained i
pixel according to the laser intensity on that



Ideal (2

Figure 2.14: Capacitance Current vs Ambient Light Photocurrent

By using the above data we can extract that the suppression efficiency of the proposed sensor is around %99 for the high ambient current interval. This high suppression ability is illustrated in the logscale graph in Figure 2.15.

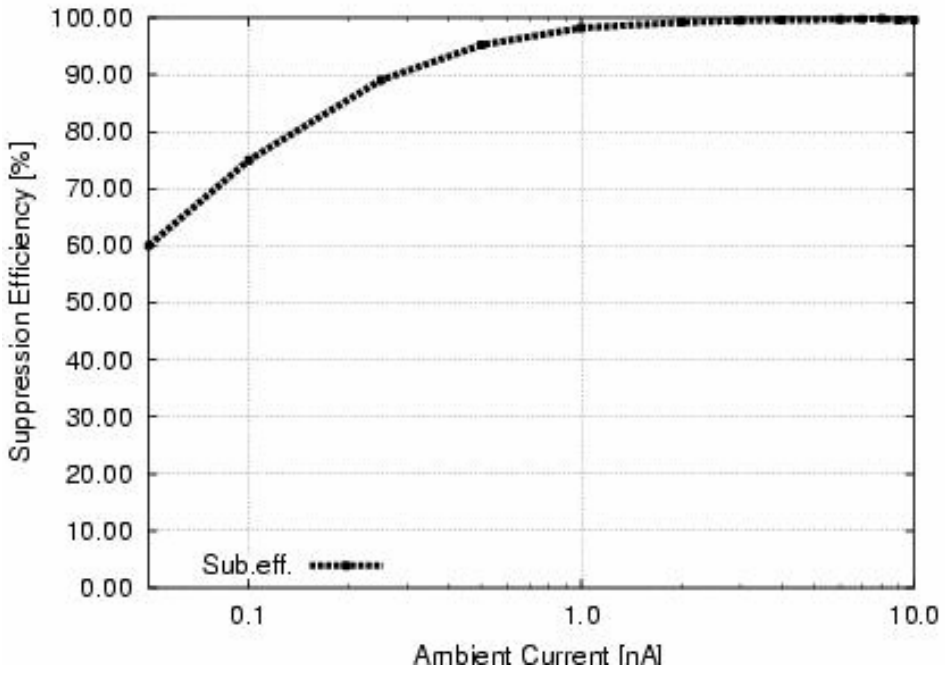


Figure 2.15: Suppression Efficiency vs Ambient Light Photocurrent

In ambient light suppression the term Signal-to-Background Ratio (SBR) which stands for the sensitivity of the light detection, is a very important parameter. It is defined as follows:

$$SBR = 10\log\frac{E_{sig\_\min}}{E_{bg}} \quad [4]$$

The minimum SBR of the present sensor is -32.8 dB as illustrated in Figure 2.16. The latest work about ambient light suppression could achieve a -22dB SBR, so the proposed sensor has a remarkable improvement on ambient light suppression.

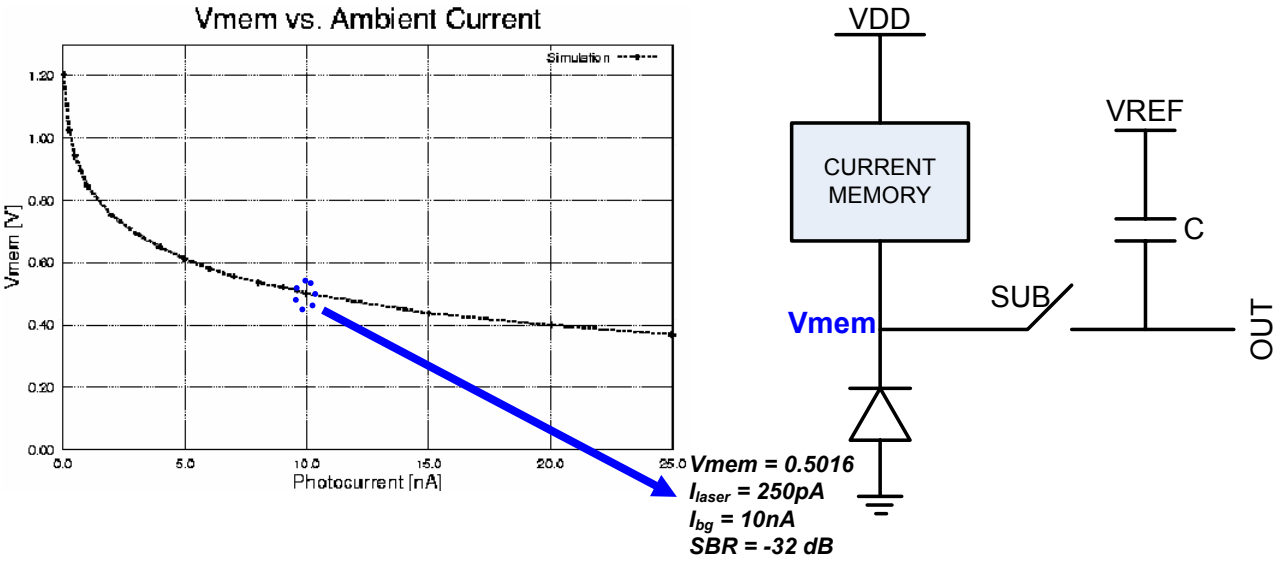


Figure 2.16: Signal-to-Background Ratio (SBR) of the Pixel Circuit

Actually it is also possible to obtain a better SBR but this causes a lower V_{mem} which in turn result in lower reverse bias on the photodiode hence an undesired nonlinear operation.

2.5 Conclusion

The switched current memory is a good solution for ambient light storage purpose for the pixel circuit. The pixel can successfully suppress the ambient light with high suppression efficiency. The source light used for suppression can be very weak as the sensor can achieve a -32dB Signal-to-Background ratio. In the next chapter, a CMOS Smart Image Sensor implementation by employing this pixel architecture will be described.

CHAPTER THREE

ARRAY DESIGN

3.1 Overall Sensor Architecture

A CMOS Smart Image Sensor was designed using the proposed pixel circuit described in Chapter 2. The block diagram of the proposed CMOS Image Sensor architecture is illustrated in Figure 3.1. The sensor is composed of a 256x256 pixel array, row and column decoders for pixel selection, column readout circuitry for sampling the analog column values and an 8 bit subranging ADC for digitizing the analog pixel values.

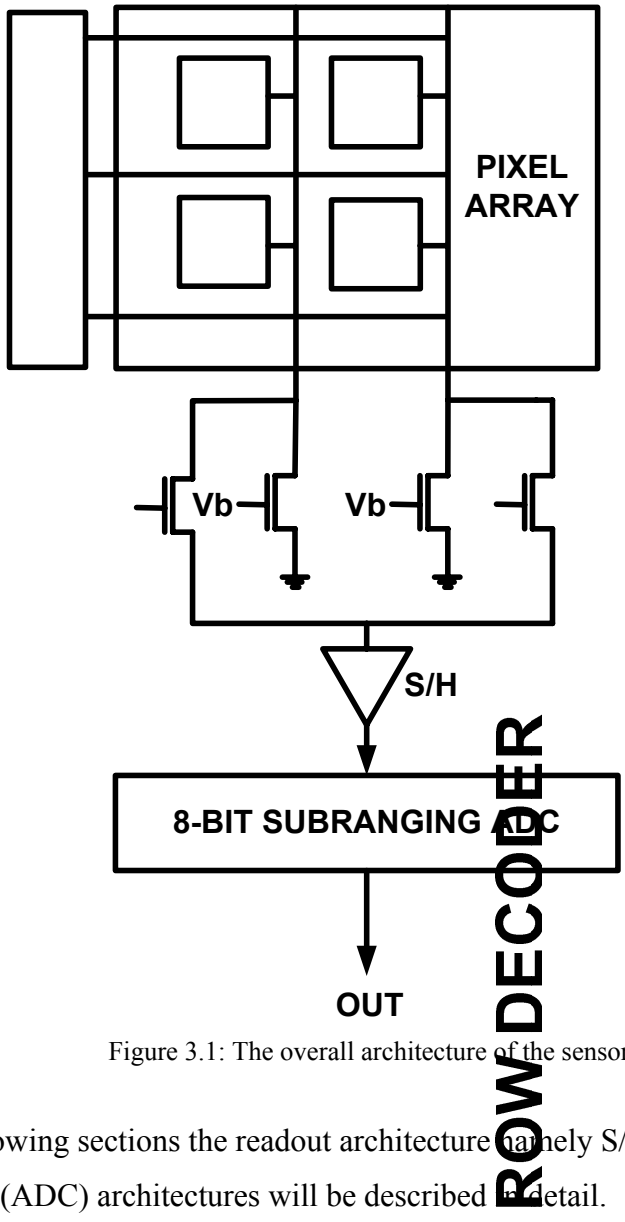


Figure 3.1: The overall architecture of the sensor

In the following sections the readout architecture namely S/H circuitry and Analog-to-Digital Converter (ADC) architectures will be described in detail.

3.2 Readout: ADC Operation

As the speed is extremely important in CMOS imaging and also because of the leakage problem in downscaled CMOS processes, a high-speed Analog-to-Digital Converter (ADC) architecture had to be employed in this work. In high speed A/D converters the all-parallel conversion method gives the best speed performance. Actually these converters are the flash ADCs. In flash ADCs, signal sampling can be done digitally by latching comparators, avoiding the need for a high speed sample-hold circuit at the input. The penalty for the flash ADCs is the increased circuit complexity.

An 8 bit flash ADC, for example, needs 255 comparators which consume a lot of power and need a large chip area. Such a converter in itself is already a large-scale integrated circuit and high volume production may be troublesome. When digital signal processing is needed, the A/D converter may only use a small part of the total LSI chip. A good optimum between speed, power consumption, and circuit complexity is found with the two-step parallel technique. A two clock-cycle subranging approach provides an effective alternative, to the single clock cycle Flash ADC. Table 3.1 Illustrates tradeoffs at the 8b level for the flash and subranging ADC architecture. Potential performance and cost advantages for the subranging approach are due entirely to the reduced number of comparators and smaller chip size. At the 8b level, the necessary 256 comparators in flash designs load the input signal, as well as the power and reference supplies. Such loading impacts integral linearity, power dissipation, and input signal drive specifications. The subranging approach reduces the comparator count from 256 to 31. This produces a relatively small die size with the input loading and power dissipation greatly reduced. A major disadvantage of the subranging approach is the reduction in throughput rate (1/2 of flash), since two clock-cycles are required per measurement cycle. A second potential disadvantage is poorer differential linearity due to piecing of MSB and LSB resistor ladder networks at 16 places. However, this has not found to be significant at the 8b level.

In CMOS imagers because of the importance of the resolution, the area dedicated for the readout and peripheral circuitry should be kept as small as possible, without decreasing the speed drastically. So 8 bit subranging type ADC is a good candidate for this purpose.

	Flash ADC	Subranging ADC
Total comparators	256	31
Clock cycles /conversion	1	2
Relative speed	1	0.5
Rel. input loading	1	0.12
Rel. power dissipation	1	0.2
Die size	1	0.4
Differential linearity	Better	Good
Integral linearity	Good	Better

Table 3.1: Comparison of Flash and Subranging ADCs

The ADC employed in the CMOS image sensor employing ambient light suppression is illustrated in Figure 3.2

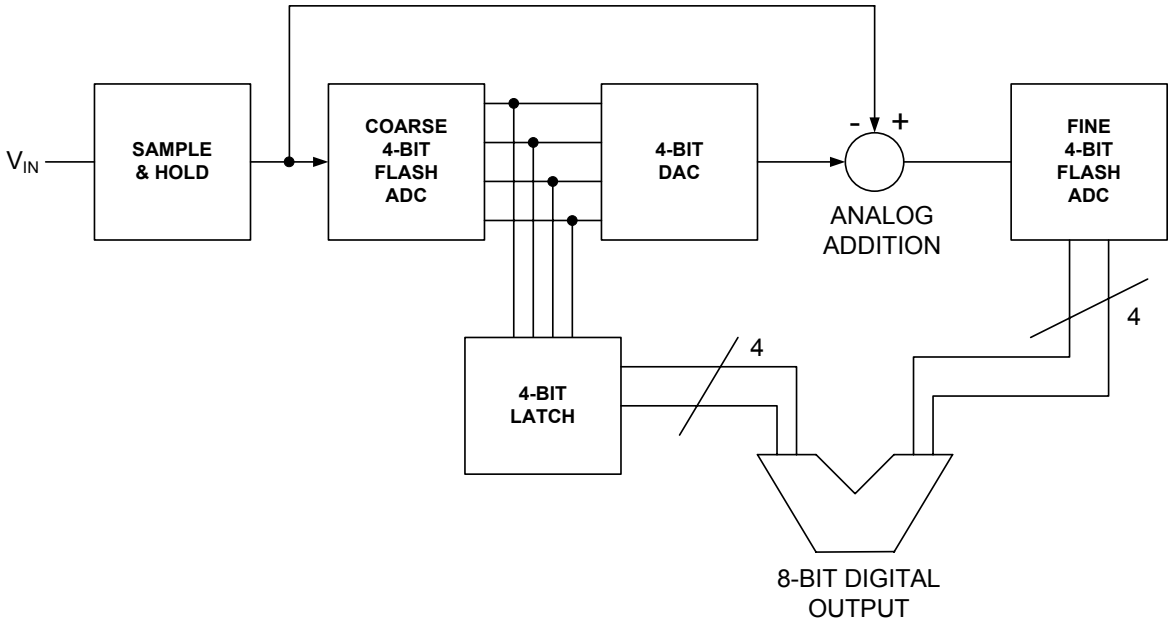


Figure 3.2 Block diagram of the subranging ADC

As stated above, the selected pixel values are transferred to the columns and through columns they are sampled by the sample & hold circuit which is shown in Figure 3.3.

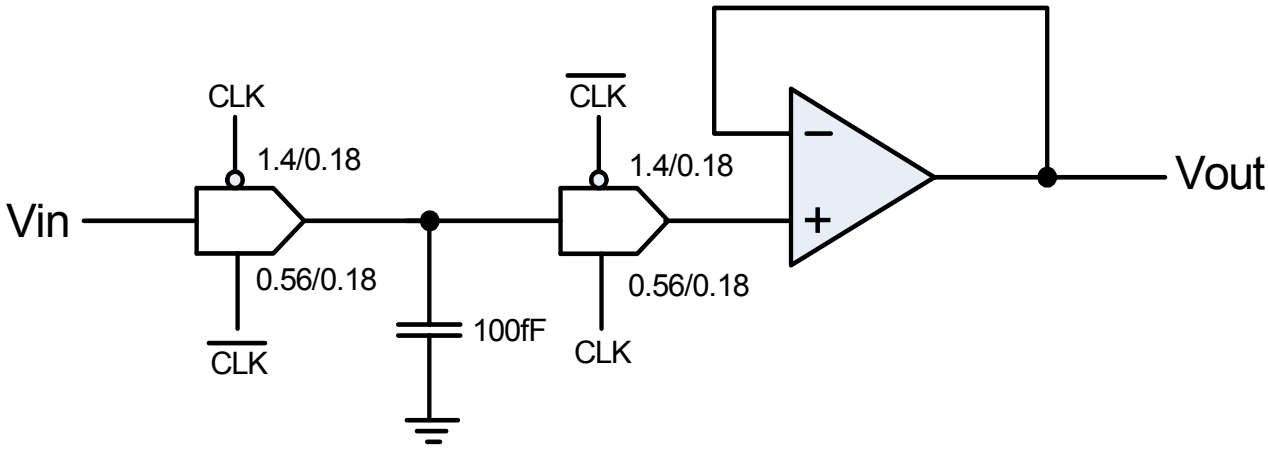


Figure 3.3: S/H Circuit Schematics

Here pass transistor logic is used to sample both high and low values accurately. The input values are first integrated on the 100fF capacitor at the high level of CLK. When CLK goes to low the capacitance voltage is buffered to the output and ADC operation starts. The operational amplifier circuitry employed in this S&H circuit is illustrated in Fig.

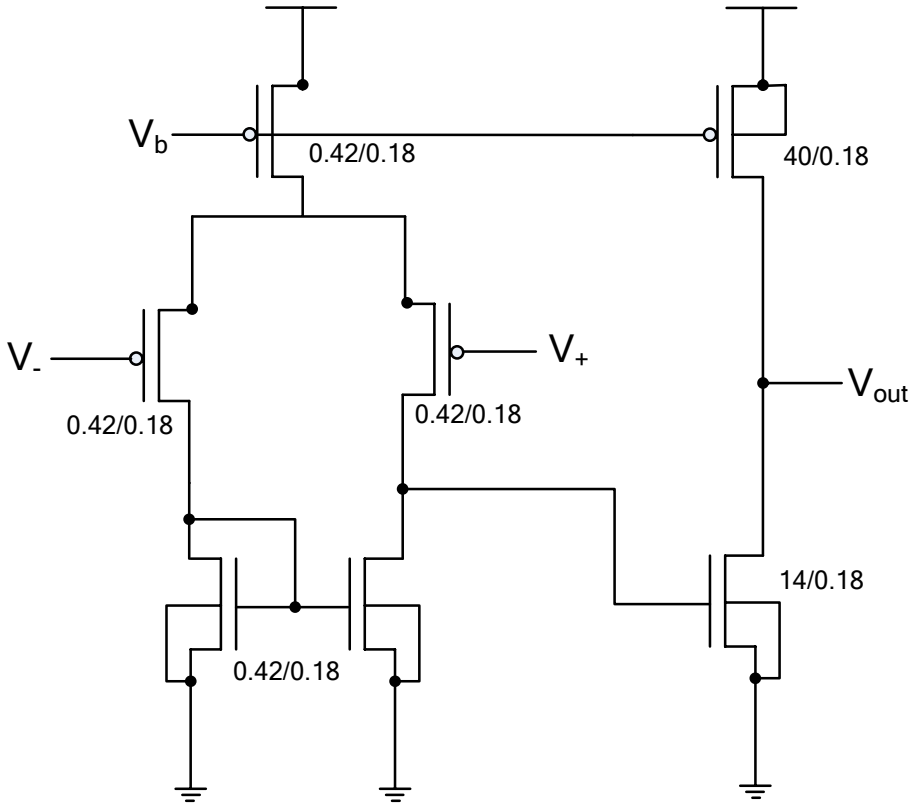


Figure 3.4 Opamp Schematics

As stated above, two-clock cycles are required for a complete conversion. In the first cycle the input signal is sampled-and-held and with the help of first 4 bit flash ADC 4 MSBs are determined as shown in Figure 3.5.

Here 15 comparators are used so N is equal to 4. The Verilog HDL code of the decoder was written and designed by using automatic place&route in Synopsys Astro. As the column values of the CMOS imager are generally below half VDD a PMOS differential amplifier architecture was used as the comparator. Actually it is the same comparator architecture with the operational amplifier utilized in S&H circuitry. As the resistance ladder a 69ohm R value was utilized to give enough current room for the comparators. After the 4 MSB bits are determined they are latched in a 4 bit latch and do not sent to the output until the 4 LSB bits are obtained for the sake of synchronization.

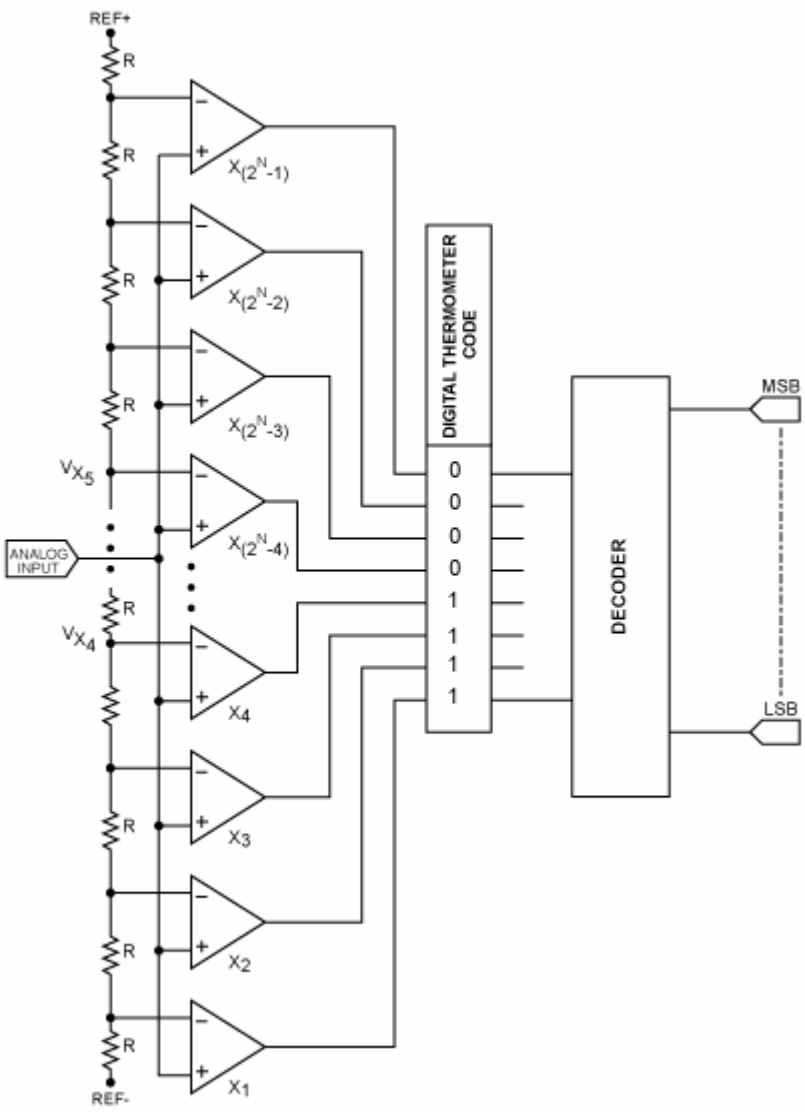


Figure 3.5 Flash ADC architecture

As shown in Fig. 4 MSBs are not only sent to the 4 bit latch but also they are again converted to an analog value by 4 bit DAC which is shown in Fig. The DAC operates with the same principal as the 4 bit flash ADC using the same resistance ladder. The corresponding switch is closed according to the incoming 4 bit digital value. Each time only one switch is ON and the voltage of that specific switch connection on the resistance ladder is transferred to the output. Like the decoder of the ADC, the encoder of the DAC is automatically placed&routed in Synopsys Astro. In Figure 3.6 its block diagram along with its Verilog HDL code is shown.

```
module encoder (compin, encoderout);
input [14:0] compin;
output [3:0] encoderout;
reg [3:0] encoderout;
always begin
case(compin)
    15'b000000000000000: encoderout=4'd0;
    15'b000000000000001: encoderout=4'd1;
    15'b000000000000011: encoderout=4'd2;
    15'b000000000000111: encoderout=4'd3;
    15'b000000000001111: encoderout=4'd4;
    15'b000000000011111: encoderout=4'd5;
    15'b000000000111111: encoderout=4'd6;
    15'b000000001111111: encoderout=4'd7;
    15'b000000011111111: encoderout=4'd8;
    15'b000000111111111: encoderout=4'd9;
    15'b000001111111111: encoderout=4'd10;
    15'b000011111111111: encoderout=4'd11;
    15'b000111111111111: encoderout=4'd12;
    15'b001111111111111: encoderout=4'd13;
    15'b011111111111111: encoderout=4'd14;
    15'b111111111111111: encoderout=4'd15;
endcase
end
endmodule
```

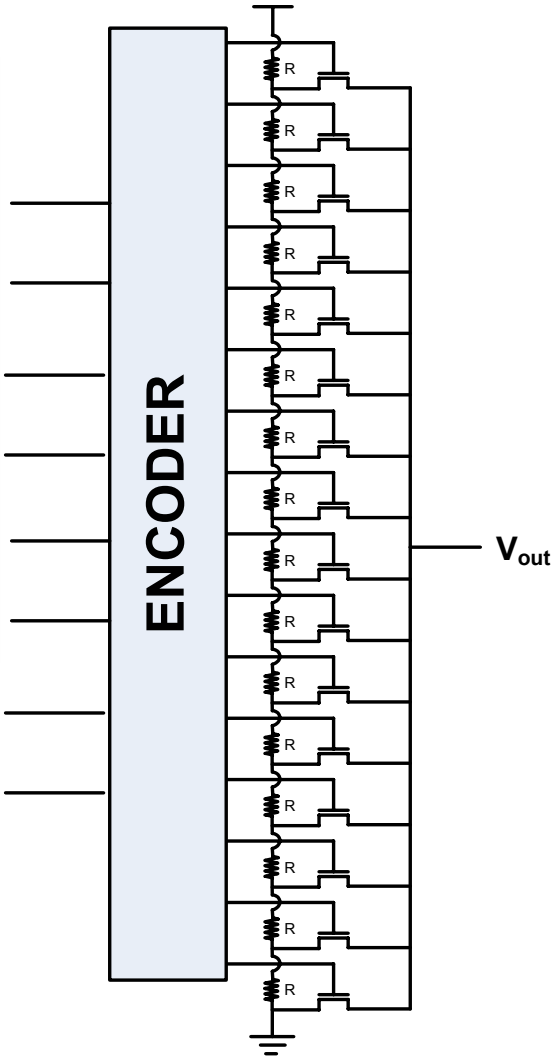


Figure 3.6 Encoder block diagram and its verilog HDL code

The subtractor circuit for subtracting the reconverted analog values from the original input values is done again by means of an opamp circuitry which is shown in Figure 3.7.

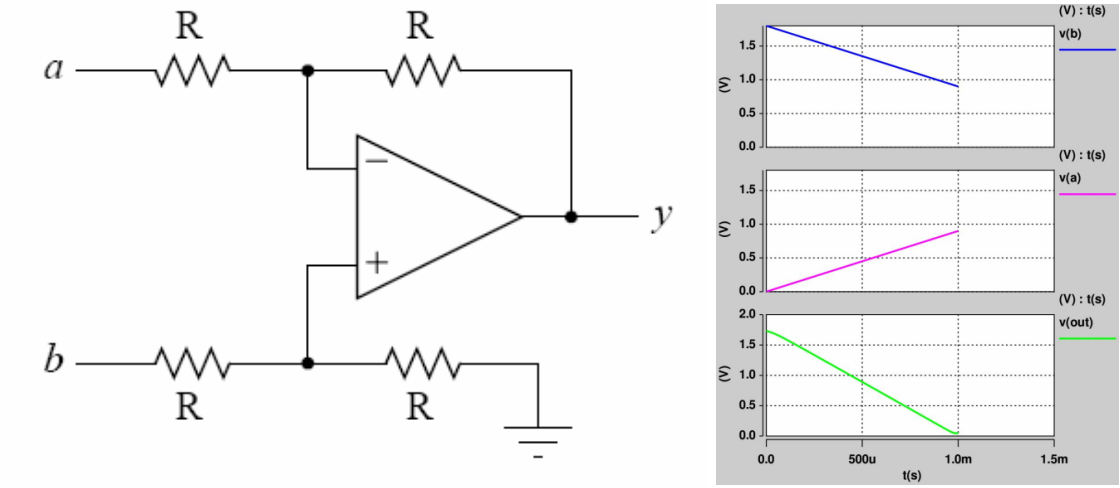


Figure 3.7 Subtractor schematics with its simulation

In the designed ADC, R is taken to be 5 KΩ and the same opamp circuit is used in the comparators of flash ADC. After the subtraction operation the result is again converted to digital by means of the second 4 bit flash ADC and sent to the output latch. In the end, the 8 bit digital value is obtained from the input column value. This operation is done for all of the pixel array and the digital grayscale image is constructed accordingly. The whole layout of the 8 bit subranging ADC is shown in Figure 3.8.

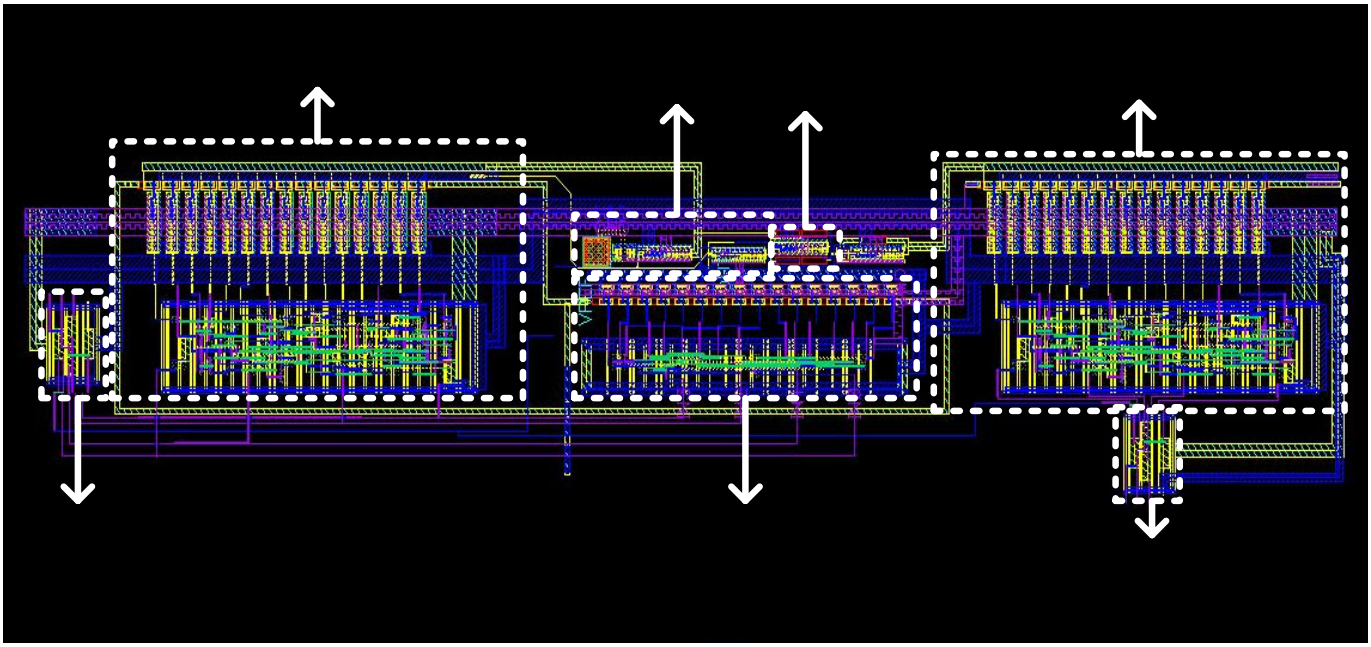


Figure 3.8 ADC Layout

3.3 Pipeline Readout Operation

As high speed light detection is very important in CMOS imaging, a pipelined array readout architecture was also utilized in the present sensor. As shown in Figure 3.9 when the readout phase of the first frame takes place the memorization phase of the second frame is operated.

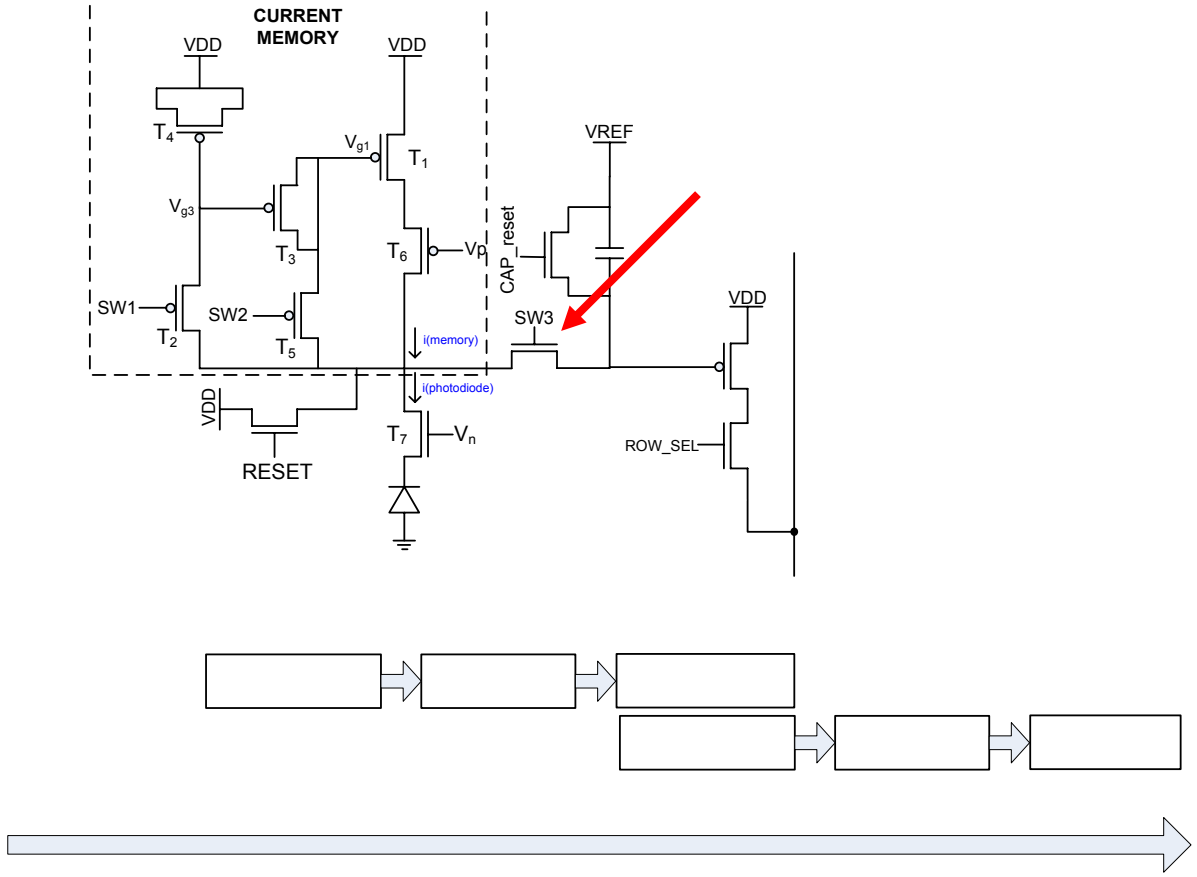


Figure 3.9 Pipeline readout architecture

This simultaneous operation enables us a big time advantage. In this operation the most important component is the subtraction switch namely SW3. It acts as a pipeline switch. By controlling it, different operations can be held at left and right sides of it. By opening SW3 and cuting the relation between the left and right sides, a memorization operation on the left side and a readout operation on the right side can be done simultaneously.

The layout of the chip was drawn the in the 0.18um CMOS process. The size of the chip is 5mmx5mm. The resolution of the array is 256x256. Some components were additionally put in order to test them separately. These additional components are the Subranging ADC and some pixel TEGs. In Figure 3.10 the whole chip layout is shown.

First Frame: Memorize Subtract

Second Frame:

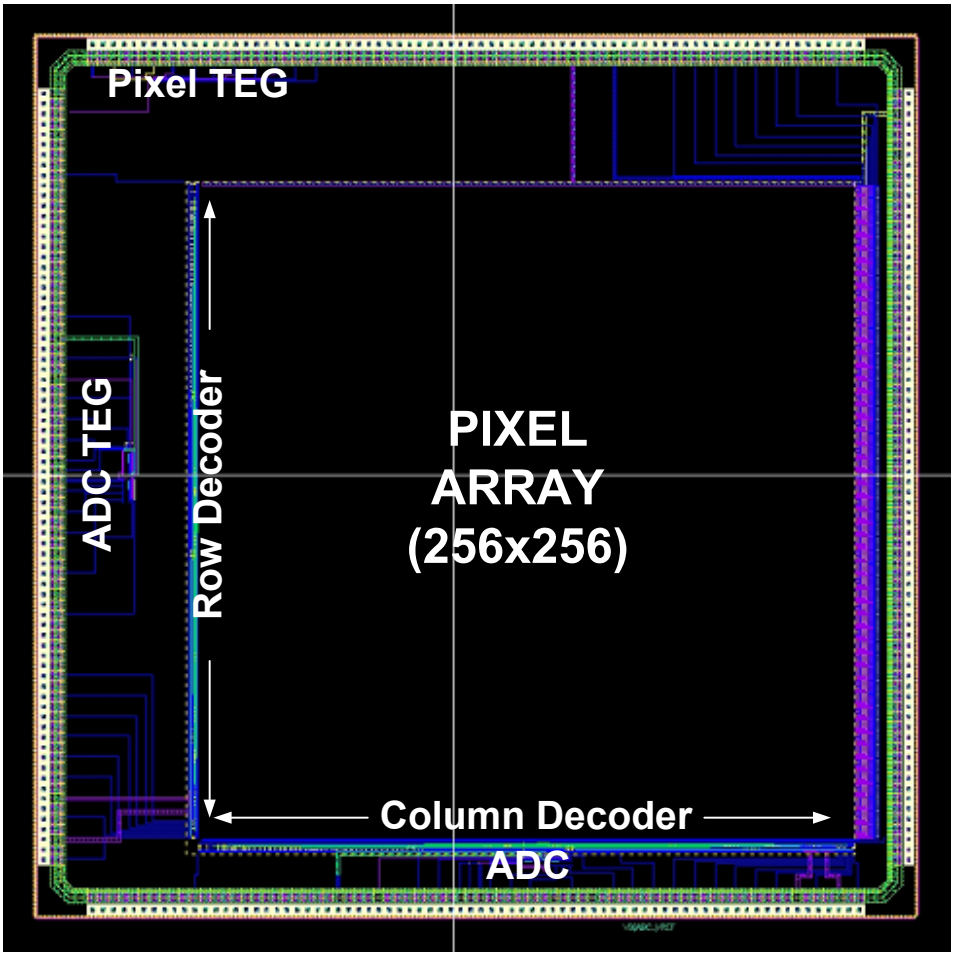


Figure 3.10: Full chip layout

The row and column decoders are also designed through automatic place&route. They acquire 8bit address information as input and select one channel out of 256 channels. The output, input and analog buffers were also placed next to the pads for accurate operation.

3.4 Simulation Results

3.4.1 Sample & Hold Circuit Simulation

The sample & hold circuit was simulated for different bias conditions and the most optimum condition was investigated. For this the PMOS bias of the voltage follower opamp was swept. The V_{out} vs V_{in} graph shown in Figure 3.11 demonstrated that Vb = ~1.2 V is a good solution for optimum linearity.

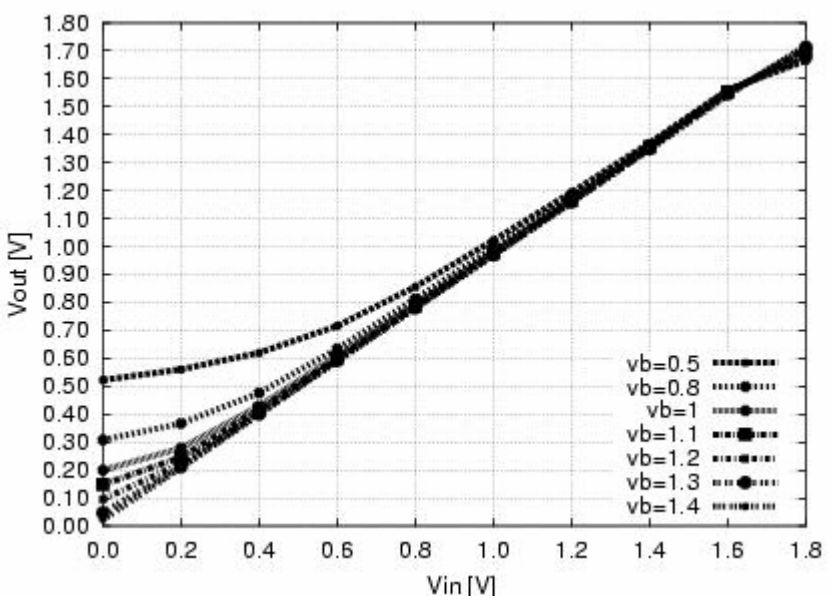
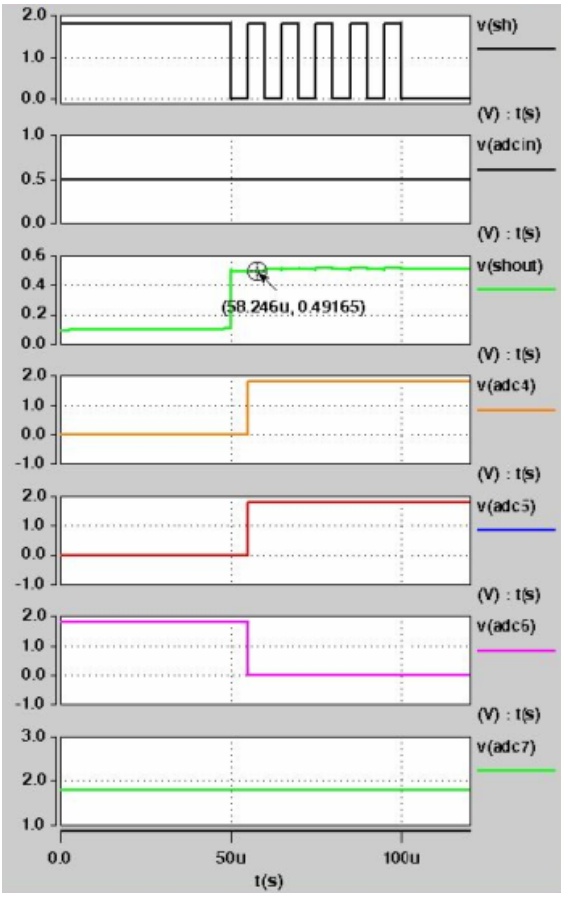


Figure 3.11: S&H Circuit characteristics for different bias conditions

3.4.2 ADC Simulation

Full-chip simulations were done for the ADC TEG present in the sensor and correct operation was approved. In Figure 3.12 the simulation of the first stage Flash ADC is shown. Here the upper reference voltage for the resistance ladder is 0.7 V. The input voltage is 0.5 V. So the 4 bit MSB becomes 1011.

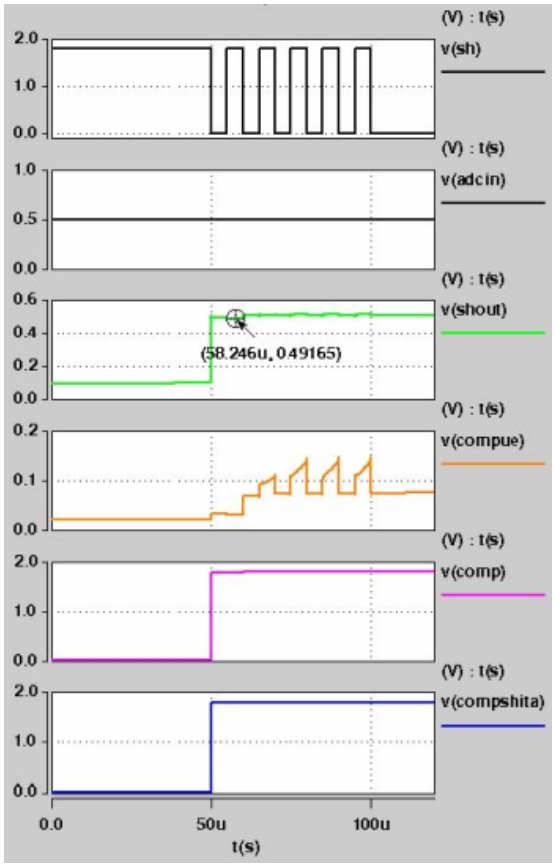


In Figure 3.13 the comparator operation is illustrated. The transition between up adjacent two comparators is shown. Output of the one becomes LOW whereas the other becomes HIGH.

The maximum operation speed for the ADC is 20 Msamples/sec. Over that speed it becomes error-prone.

In the next section the measurement results will be covered.

Figure 3.12 ADC Simulation



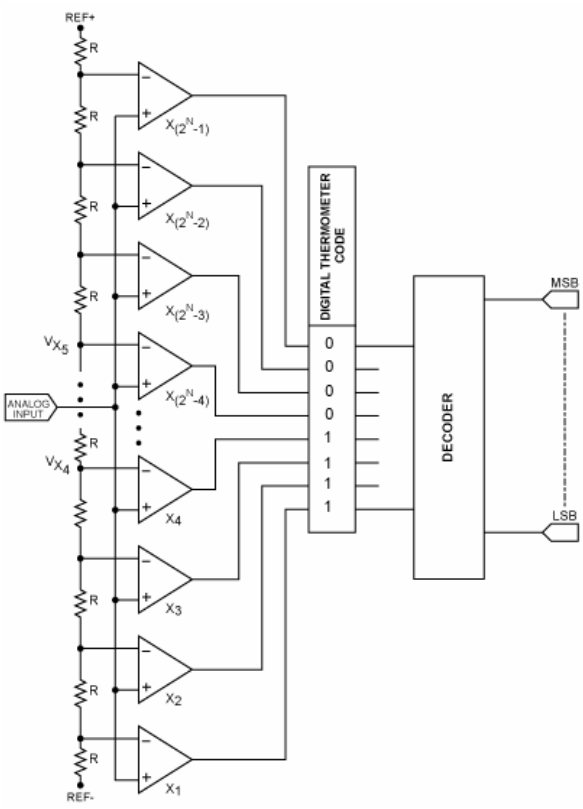


Figure 3.13: Comparator operation illustration

3.5 Measurement Results

The image sensor chip was measured by the help of a 40MHz FPGA and a measurement board. The sensor photomicrograph is shown in Figure 3.14 As the FPGA was operating in 3.3V VDD voltage which is not compatible with the sensor of 1.8V VDD, some pull-up and pull-down ICs were utilized for logic level conversion. The analog biases were applied by means of voltage divison technique on variable resistances.

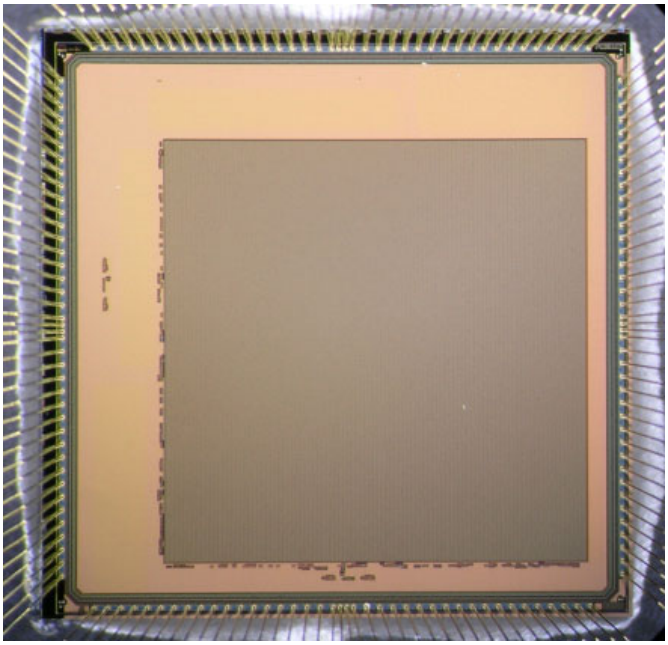


Figure 3.14: Sensor Chip photomicrograph

The measurement board is illustrated in Figure 3.15.

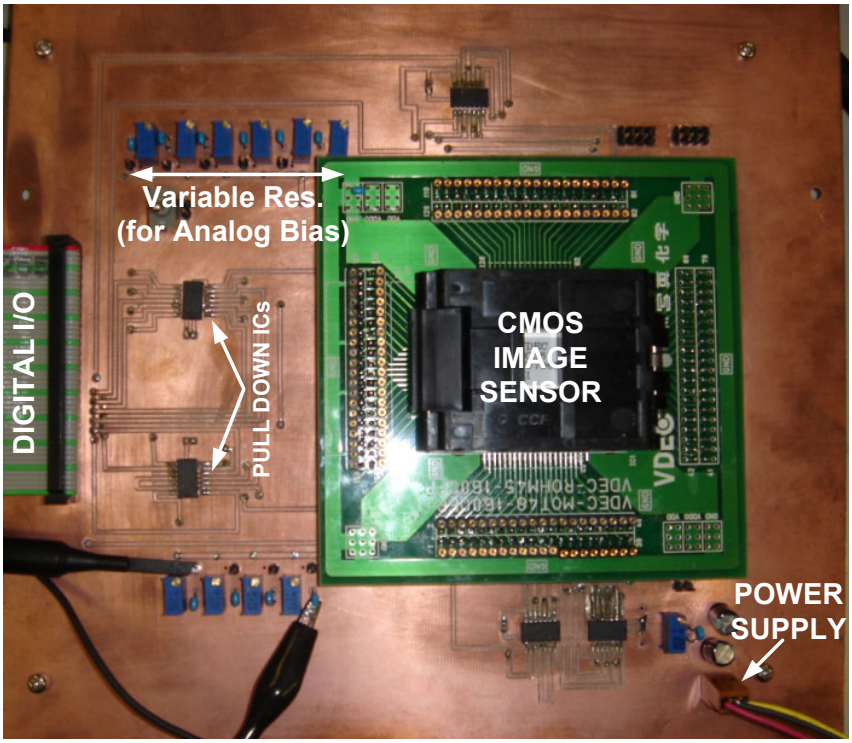


Figure 3.15 Sensor chip measurement board

Firstly, ADC TEG was measured and unfortanetely an unexpected result was obtained. Regardless of all input and bias sweeps, all of the outputs were stuck at VDD. To understand whether there was a mistake with the layout, full chip simulation was employed but we did not face with a mistake with the layout.

To test the column readout, firstly CAP_RESET switch was turned on and SUB switch was turned off. Hence VREF voltage was reflected to the gate of the source follower as shown in Figure 3.16.

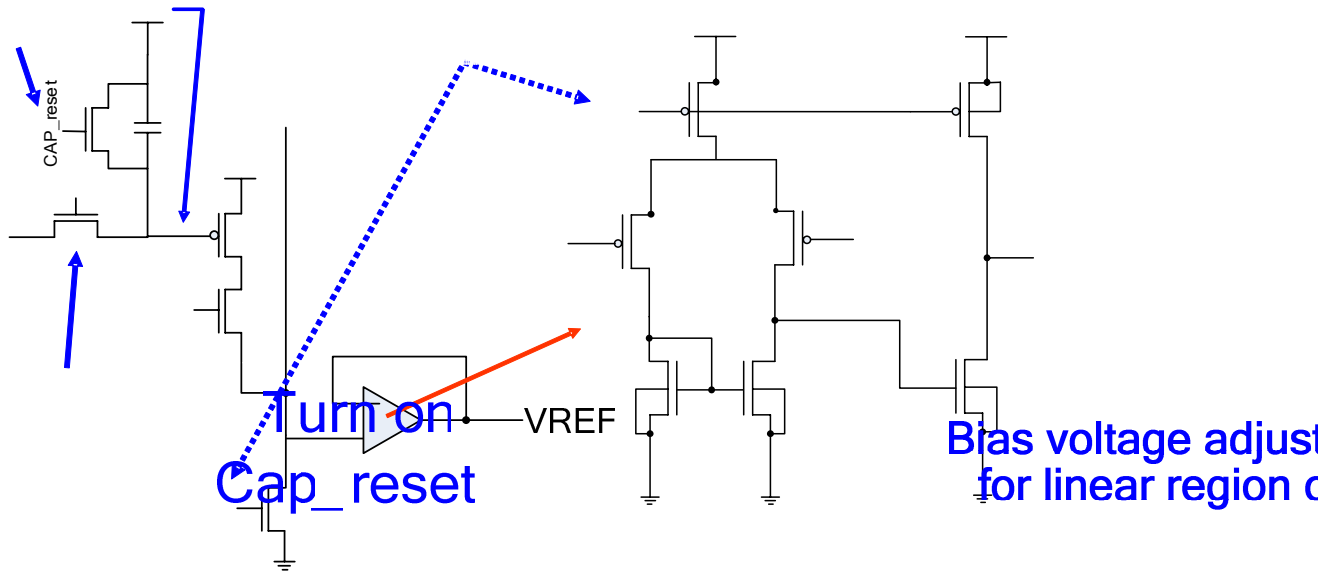


Figure 3.16 Column readout test

So the output of the voltage follower connected to the column line was measured by sweeping the VREF voltage to investigate the column linearity. The Vout vs Vref graph is shown in Figure 3.17.

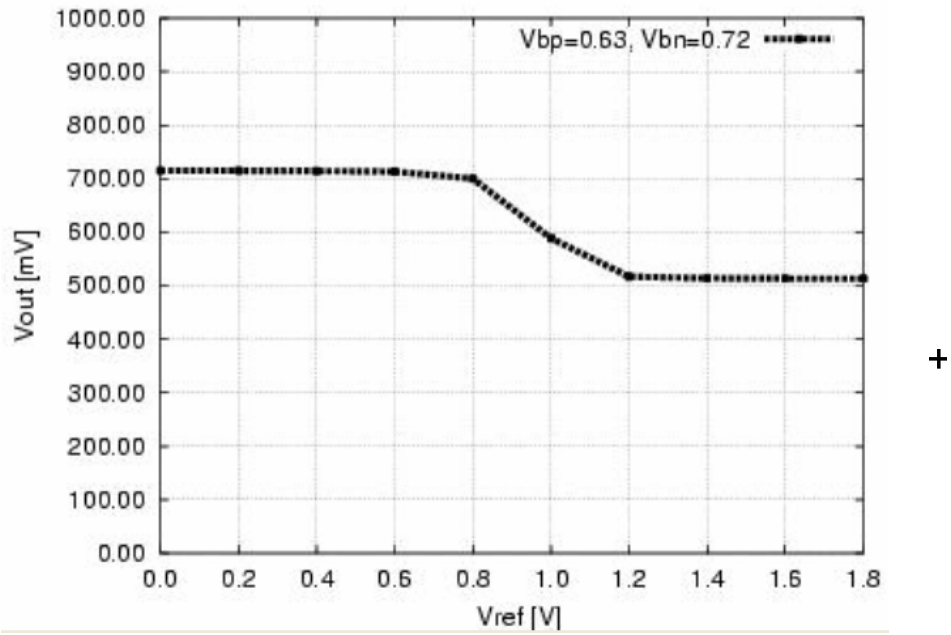
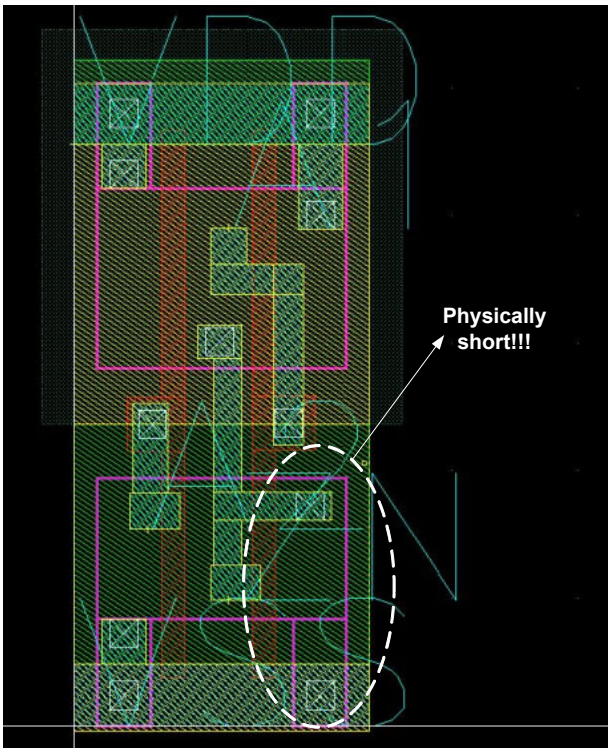


Figure 3.17 Measurement result for the column test

As the output voltage swing in the linear region is only 200mV, it was very hard to make a healthy evaluation for the operation of the chip. Actually the reason for this small linear region was a mistake at the column source follower. Because of the tail NMOS transistor which Vb is applied, it is functioning as inverting amplifier instead of a source follower. There was another deadly mistake more critical than the source follower. After careful investigation we understood the reason for the overall chip failure. The standard cell library used for the automatic place & route of the digital circuits was containing a critical error. For example in the layout of the NAND cell ,shown in Figure 3.18, the output is physically shorted to GND but it is not seen in the extraction file as it is not a metal line short. So this mistake can not be realized in the simulation and made all of the digital circuits out of service.



As a result, we are planning to design one more chip after fixing the errors in standard cell library. Also a new follower should be designed having the characteristics in Figure 3.19.

Figure 3.18 Layout error of the NAND cell

The new version of the source follower along with its simulation is shown in Fig. 3.19.

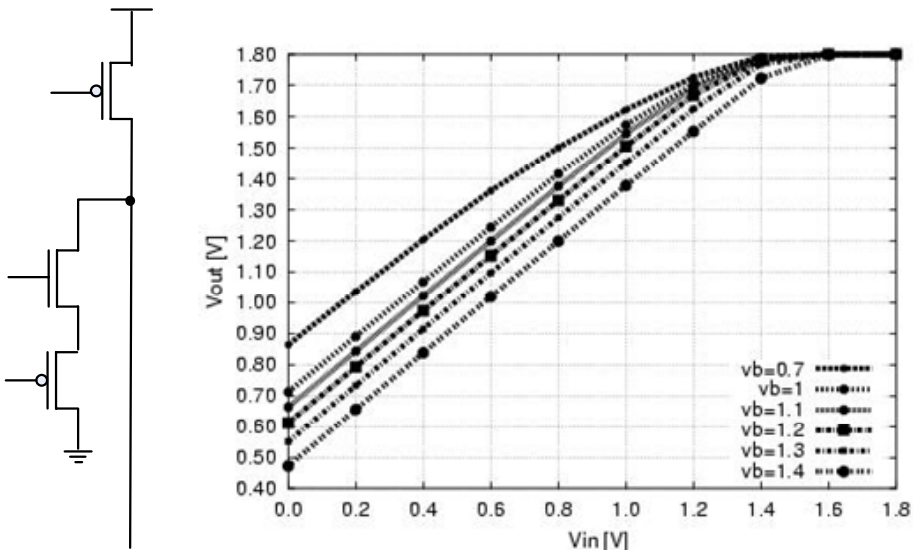


Figure 3.19: Simulation of the PMOS source follower

So the new pixel circuit is supposed to have the schematics shown in Figure 3.20.

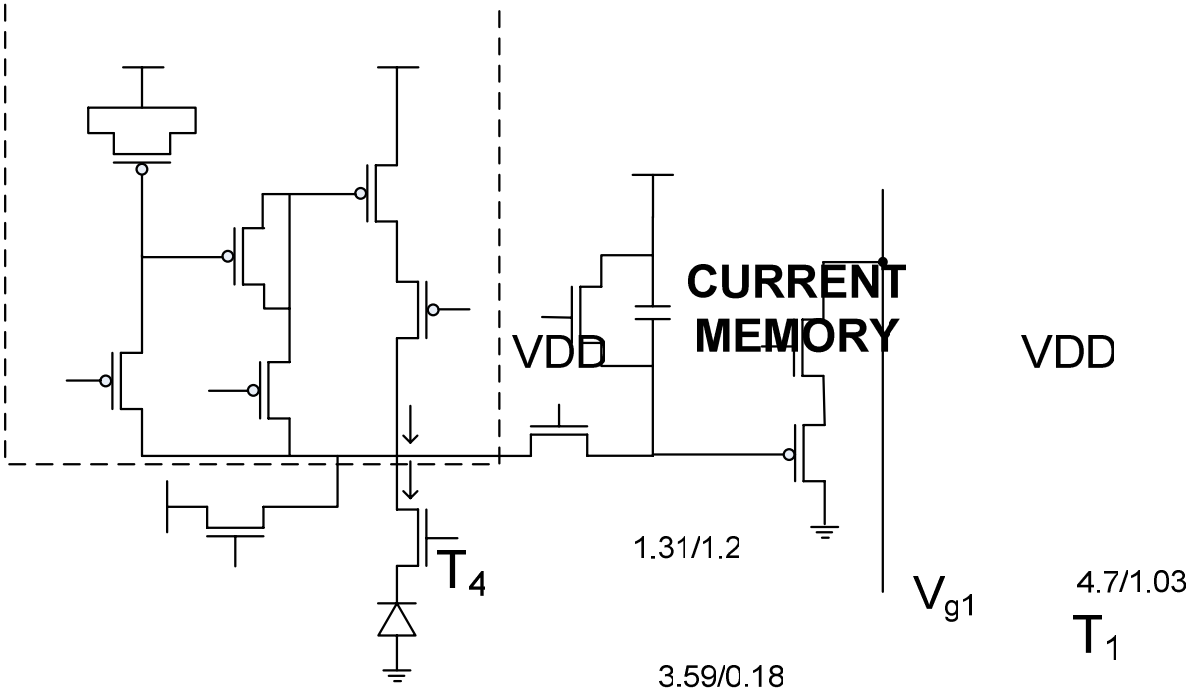


Figure 3.20 : The new pixel circuit schematics

3.6 Possible Tradeoffs

As the CMOS technology gets smaller, the leakage problem becomes more severe. This effects the performance of the voltage memories inside a chip. Hold operation becomes harder with smaller capacitance sizes. But if this memory is inside a pixel, it becomes almost impossible to have big capacitance sizes due to resolution concern. So this negative leakage effect brings us a serious issue especially for CMOS imagers. Similarly in the proposed work we faced with this problem. To give a better understanding this is illustrated in Figure 3.21

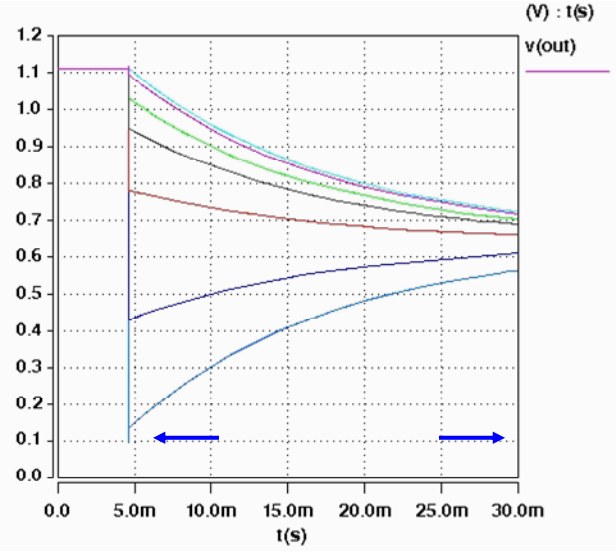


Figure 3.21: Process leakage effect on the capacitor memory

Here in this figure, some sample Vout voltages are simulated for a capacitance value of 50fF. These voltage values belong to the region right after the SUB is turned off after the current subtraction. In the ideal case we expect no current flowing on C but it is not the case in real. A small leakage current, $I_{leakage}$ flows on C and this leakage current increases proportionally with the downshrinking of the CMOS technology. As seen in the graph, along the readout interval, the memory voltages are altering drastically due to the leakage current I(leakage). This results in inaccurate operation and lack of information. In order to diminish this effect, a fast readout scheme or a high capacitance value should be utilized. The leakage current was found to be around 1.5pA for a weak source current case. This is illustrated in Figure 3.22

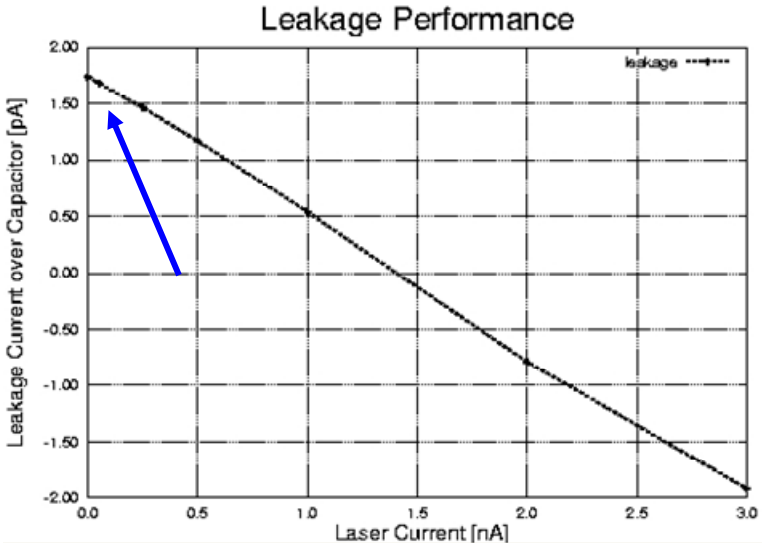


Figure 3.22 Leakage current vs source current

As the design rules don't allow us to put a MIM capacitor inside the pixel, a gate capacitor was placed. A gate capacitance is formed by short-circuiting the drain and the source terminals of a MOS transistor. Gate capacitance values were investigated for difference capacitor sizes, by applying constant currents I and observing the capacitance voltage Vc. According to these investigations and area concerns of the pixel a 117fF capacitance was selected. The graph showing the gate capacitance values versus the transistor sizes that are forming the capacitors is shown in Figure 3.23. The transistor utilized as a gate capacitance inside the pixel has a length of 5.91um and a width of 9.07um which is considerably large when compared with the total pixel area. This was the maximum area that can be dedicated for a gate capacitance in a 15umx15um pixel.

~1.5pA for

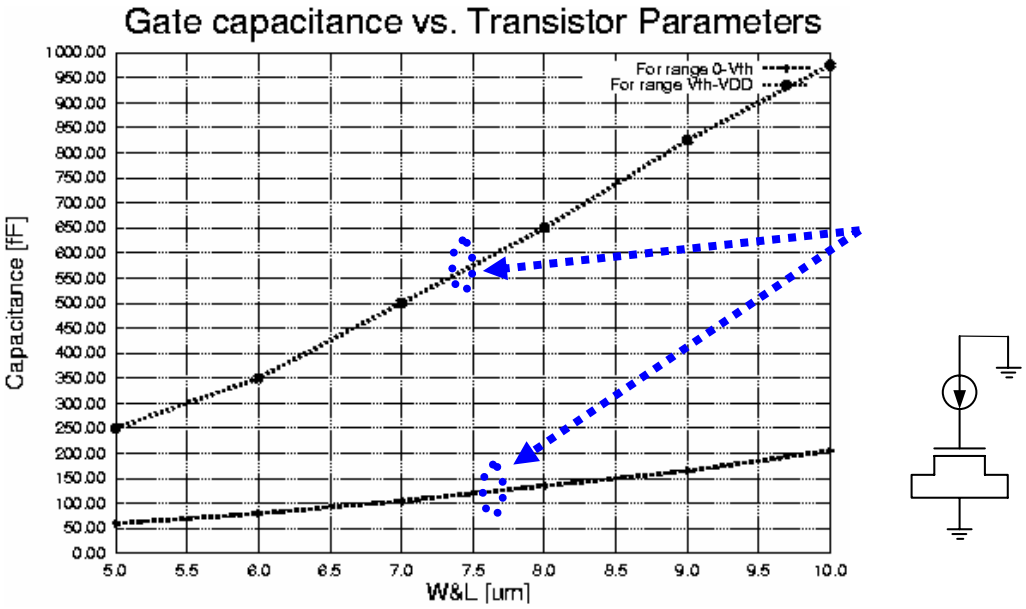


Figure 3.23 Gate Capacitance Characteristics of the CMOS 0.18um Process

3.7 Comparison with the Past Research

Although there is not so much research about ambient light suppression on CMOS image sensors, to give a better understanding of the advantages and disadvantages of proposed work, making a comparison with the past research is useful. In table 3.2 various specifications of some works and this work are listed. This comparison is based on 3 recent researches and this work.

	Proposed	**[23]**	**[24]**	**[25]**
Suppression Method	Current	Current	Voltage	Voltage
Signal-to-Background Ratio	**-32 dB**	-22.8 dB	-	-
Suppression Ratio	**% 2.5 (10nA to 250pA)**	-	% 5 (2V to 100mV)	-
Frame Rate	200 fps	400 fps	-	100 fps
Chip Area	5mm x 5mm	8.9mm x 8.9mm	4.9mm x 4.9mm	6.8 mm x 6.8 mm
Pixel Area	15um x 15um	60 um x 60 um	12.8 um x 12.8 um	47.5 um x 47.5um
Fill Factor	**24 %**	13.5 %	22 %	45 %
Dynamic Range	??	48 dB	-	62dB
Array Size	**256 x 256**	120 x 110	176 x 144	80 x 85
ADC Resolution	8b	8b	8b	8b
Process Type	0.18 um	0.6 um	0.35 um	0.6 um

Table 3.2 Comparison of the proposed work and the recent works

As seen from the above table, the suppression performance of this work is better than the others. The other specifications are also considerable compared to the other researches.

Note that, the specifications belonging to the other researches are the measurement results, whereas the ones for this work are the simulation results. Hence, to make a more fair comparison and evaluation, the most recent work[24] was simulated in the same process technology with this work and a subtraction performance investigation was done on both. The conventional method [24] which employs a voltage mode suppression along with in-pixel correlated double sampling to eliminate the saturation problem were simulated in 0.18um CMOS technology and the simulation results were compared. This work was mentioned in Chapter 1 and related with its operation principle, it boosts the reset level in the second frame according to the voltage decrease due to ambient light in the first frame. The circuit schematics of the pixel is shown in Figure 3.24.

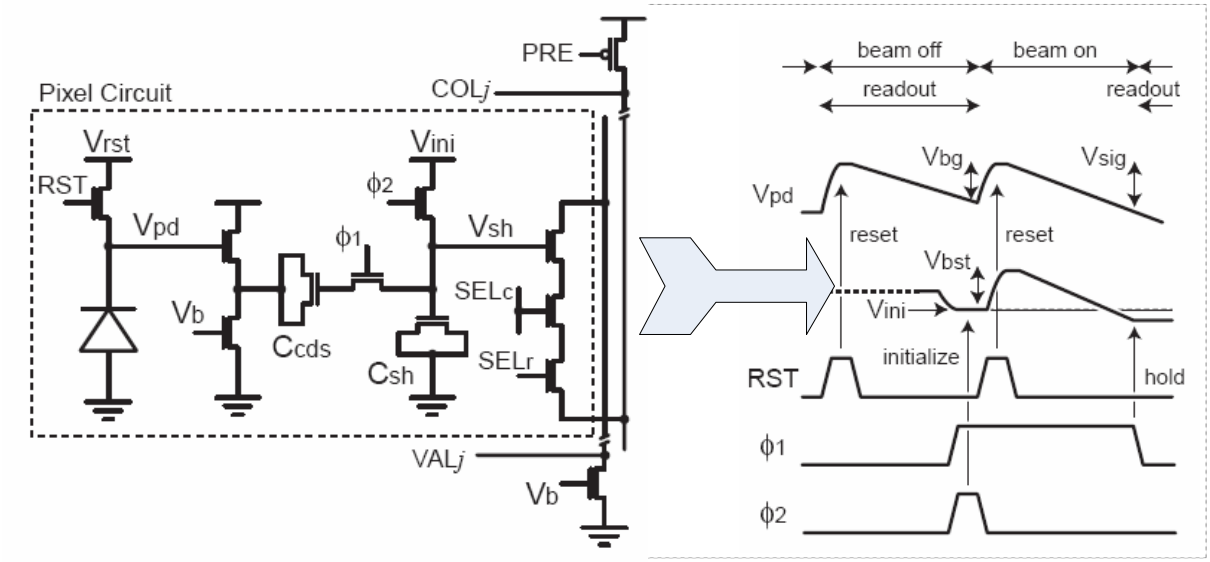


Figure 3.24 Conventional in-pixel CDS ambient light suppression method

The ambient light level is swept in a 50pA to 100nA range along with a 250pA source current and suppression efficiencies of the two schemes were observed. As illustrated in Figure 3.25, the suppression efficiency of the proposed scheme is considerably better than the voltage mode one. Moreover because of the reduction in the negative effects of charge injection and channel length modulation, the ambient light suppression efficiency is found out to be more than % 99.

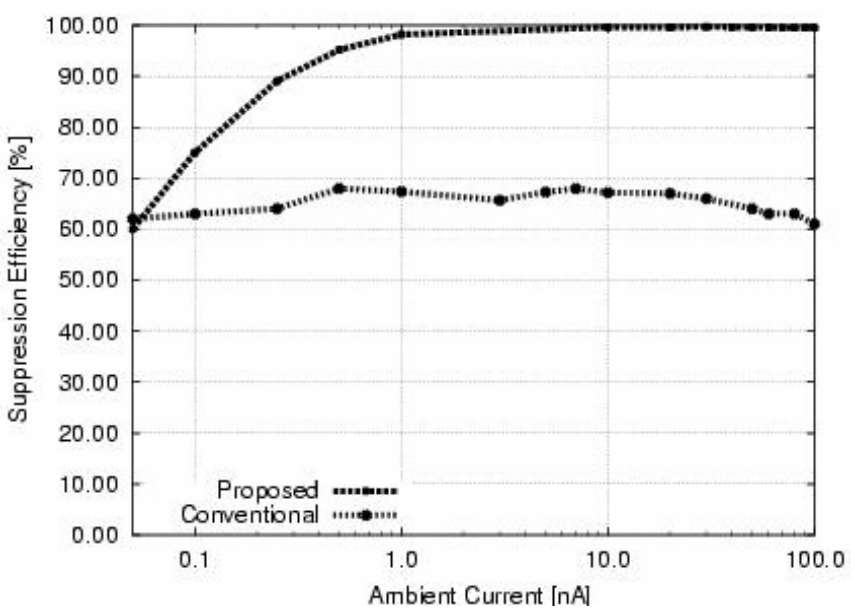


Figure 3.25 Suppression efficiency comparison between the proposed and conventional methods

3.9 Conclusion

In this work, the design and implementation of a new and efficient current-mode ambient light suppression scheme for CMOS 3D range finders has been described and the simulation results of the pixel circuit designed in a 0.18-um CMOS process have been presented. The circuit operates with a high accuracy in a very weak current range and the effect of the charge injection related with the ambient light storage is reduced significantly by employing an efficient charge compensation scheme. The range finder is capable of operating in very high illumination environments with a weak laser beam source. Hence the laser source is not significantly harmful for the human eye. Moreover the system uses less power when compared with conventional range finding system as the source laser power is very low.

CHAPTER FOUR

INTERFACE DESIGN USING OPEN CORE PROTOCOL

4.1 Proposed Sensor Controller Architecture

Market trends are ample evidence that SoCs are growing in importance in the semiconductor industry. The reasons are not far to look: SoCs make available, on a single piece of silicon, the embedded IP and high system-level integration required for performance demanding applications today. This enables semiconductor manufacturers to cost-effectively meet specific system requirements while delivering competitive time-to-market advantage. In that sense, a sensor controller was decided to be placed inside the CMOS Image Sensor chip to provide compatibility for a SoC design concept. The sensor described in Chapter 3 has some disadvantages in terms of manageability. Because the number of pins is too many, it is not easy to manage. Therefore there is a need for a complicated device like FPGA or a PC. This causes the system performance to be limited with the FPGA or PC performance. For instance the maximum FPGA speed was 40MHz whereas the sensor could tolerate a higher frequency in the readout phase. So, we decided to implement a sensor controller for generating the necessary digital signals required for the sensor.

The block diagram of the sensor architecture described in Chapter 3 is shown in Figure 4.1. All the pixel signals, row and column address signals, ADC sampling clock have to be sent from the outside FPGA. Hence, a sensor controller was designed to enable the sensor, to be compatible with a SoC platform and moreover because of the logic level difference of FPGA and the sensor, it eliminated the need for a pull down/up IC which has to be placed between FPGA and sensor.

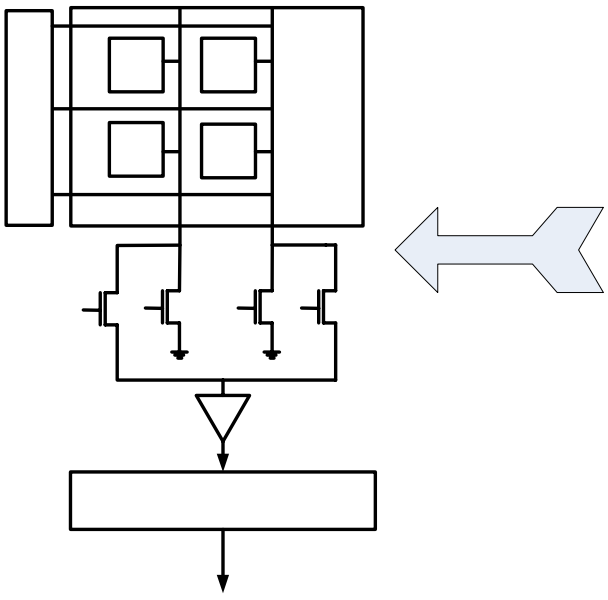


Figure 4.1: Sensor controller realization for the previous sensor

The proposed sensor controller generates the necessary timing signals for the pixel, decoder and ADC after the START pulse comes from the user. It also sends the enable signal for the source flash light at the time of current subtraction to synchronize it with subtraction switch inside the pixel. The overall block diagram along with the sensor controller is shown in Figure 4.2.

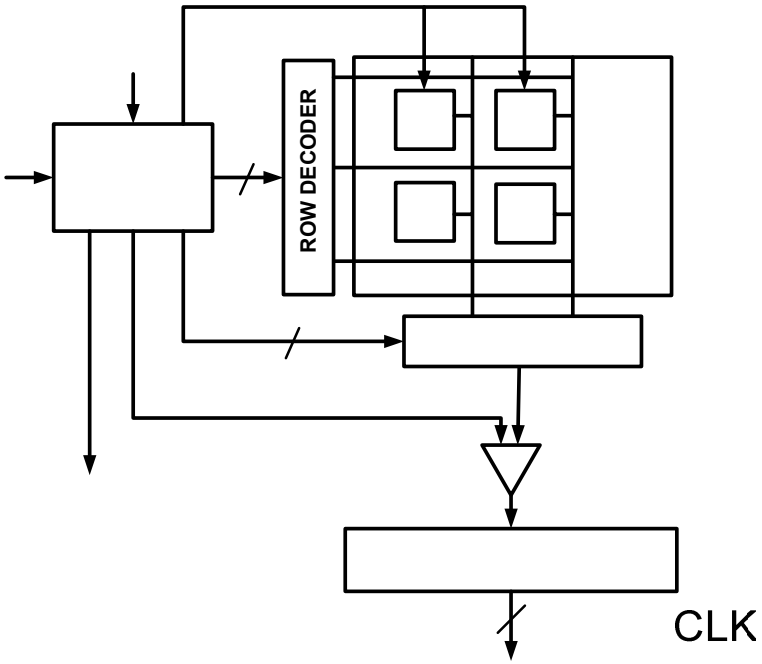


Figure 4.2 Block diagram of the sensor containing sensor controller

4.2 Open Core Protocol (OCP) Interface Design

The SoC application of the CMOS image sensor is realized via Open Core Protocol (OCP). OCP is a common standard for IP core interfaces, or sockets, that facilitate “plug and play” SoC design. Making complex SoC design more efficient for the widest audience, the industry strongly supports the Open Core Protocol as the universal complete socket standard, regardless of on chip architecture or which processor cores are featured. The basic OCP is a very simple interface, allowing simple cores to be plugged into a system. Besides the clock, it includes the request, which consists of command, address, write data signals from the master to the slave, and command accept, response, and data read signals from the slave to the master. Figure 4.3 shows a simplified view of an OCP interface. Address and data bus widths are configurable to match the core’s requirements.

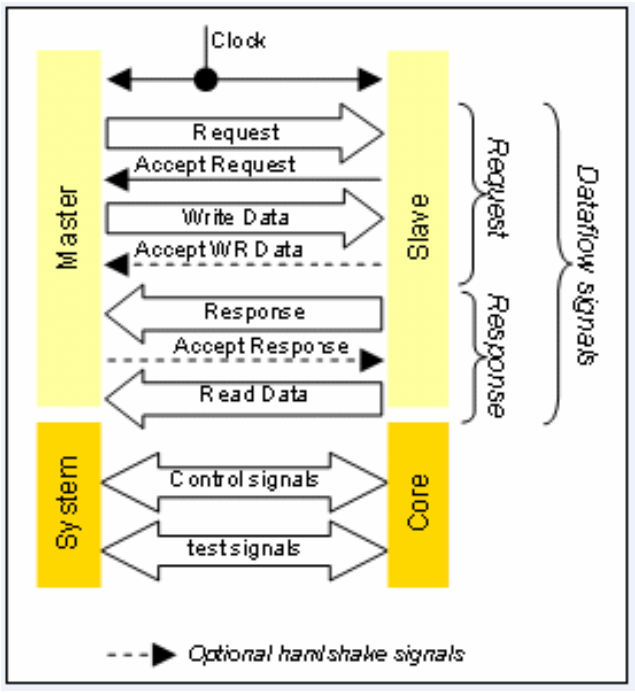


Figure 4.3: Simplified view of OCP interface

Commonly an OCP transfer is made of two separate and temporally decoupled phases, one for the request, and one for the response. Progression within a phase is controlled by a two-way handshake between the communicating entities. A phase begins with one side asserting the signals associated with that phase. In the illustration shown in Figure 4.4, the master asserts Request 1 during cycle 1, and Request 2 during cycle 3. The phase completes when the other side acknowledges that phase with a dedicated accept signal. In the example, the slave accepts Request 1 immediately (in cycle 1), while Request 2 is accepted a cycle after it is presented (in cycle 4). Any phase can be handled using a similar two-way flow control if required. The initiator of a phase is required to hold all signals associated with that phase steady until the target of that phase signals acceptance. This feature reduces the number of storage elements required to build an OCP interface.

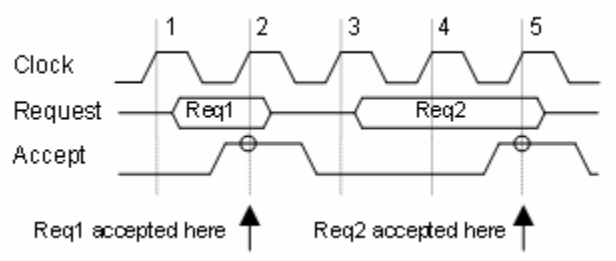


Figure 4.4: Master Slave Handshake in OCP

The sensor controller operation is also based on the OCP interface. It communicates with the OCP bus for getting the commands and sending the image data to the SoC CPU. In

this operation the master and the slave are SoC CPU and the CMOS image sensor respectively. The controller contains a timing generator which generates the following signals:

- **Inputs**: CLK, OCPCLK, ADCOUTPUT
- OCP Bus Signals (MData, MAddr, MRespAccept, MCmd)
- **Outputs:**
- *Pixel Signals*
  - RESET, SW1, SW2, SUB, CAP_RESET
- *Decoder Signals*
  - ROWADDR, COLADDR, ROWEN, COLEN
- *ADC Signals*
  - *S/H Clock*
- *External communication signals*
  - FLASH
- *OCP Bus Signals (*SData, SResp, SCmdAccept)

The block diagram of the controller architecture and the signal flow is also shown in Figure 4.5.

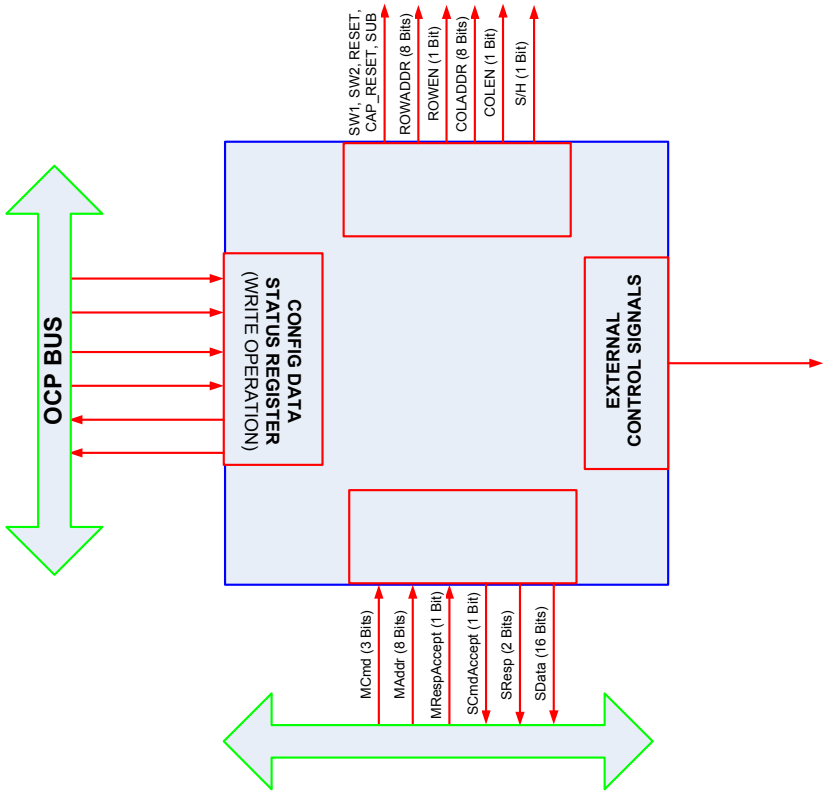


Figure 4.5 Controller architecture and its signal flow

As to concentrate on the pixel operation first, the timing diagram of the pixel signals generated by the sensor controller is shown in Figure 4.6

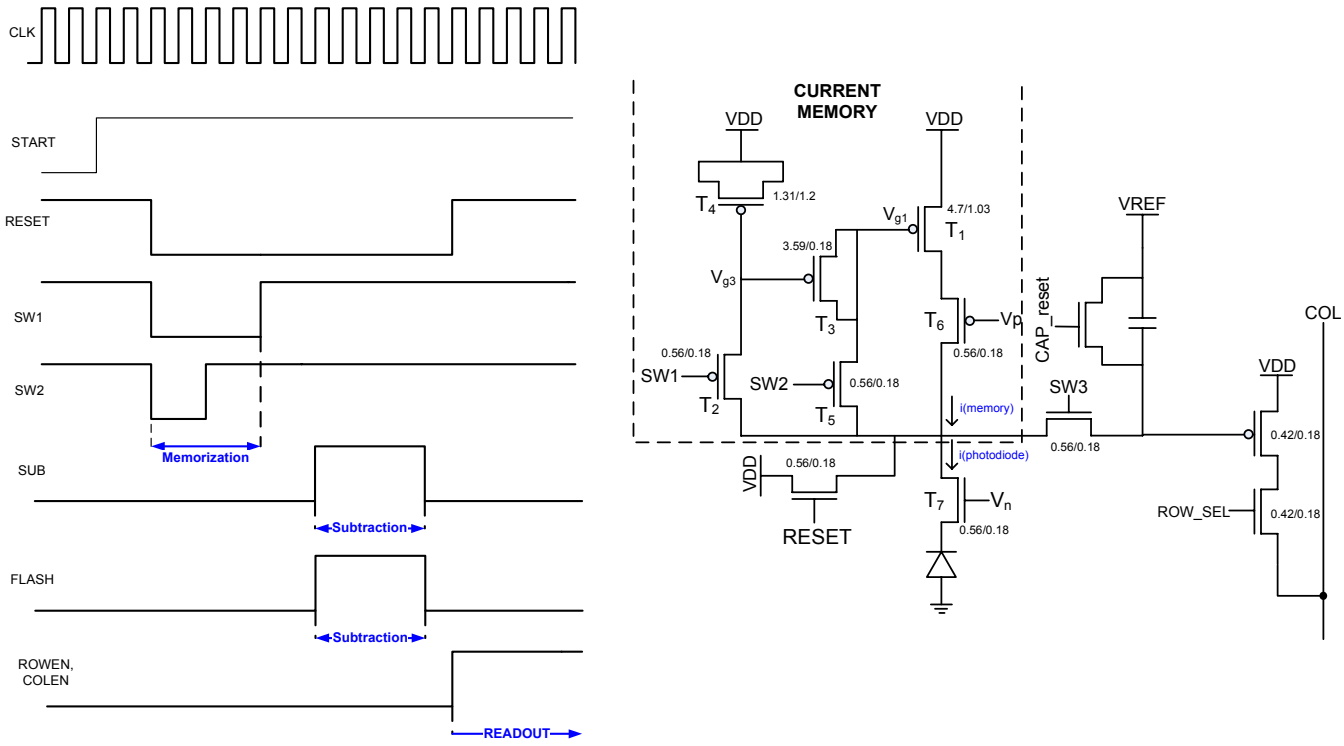


Figure 4.6 Pixel Signals to be generated by the sensor controller

After the start pulse comes from the OCP bus, the photodiode is reset by the reset signal. Then current memorization starts by sending low signals to the SW1 and SW2 PMOS transistors. After the ambient light is completely memorized the subtraction signal SUB synchronized with the FLASH signal is sent to the sensor for the ambient light suppression phase. Then the output voltage is transferred to the column via sending the enable signals for row and column decoders.

The image data namely the ADC output is first buffered and then sent to the bus. This is done to synchronize the sensor with the OCP bus because it has separate clocks which can probably have different frequencies.

All of the off-chip communication is handled via OCP bus of 32 bit width. The data is sent to the sensor along with the sensor's address. This communication process is controlled with the handshaking signals present in the 32 bit OCP bus. In table 4.1, the signals carried on the OCP bus is shown.

Signal Name	Width (bit)
ocpClk	1
ocpReset_n	1
ocpMCmd	3
ocpMAddr	Desired
ocpMData	16
ocpMConnID	Target数
ocpMRespAccept	1
ocpSCmdAccept	1
ocpSResp	2
ospSData	16

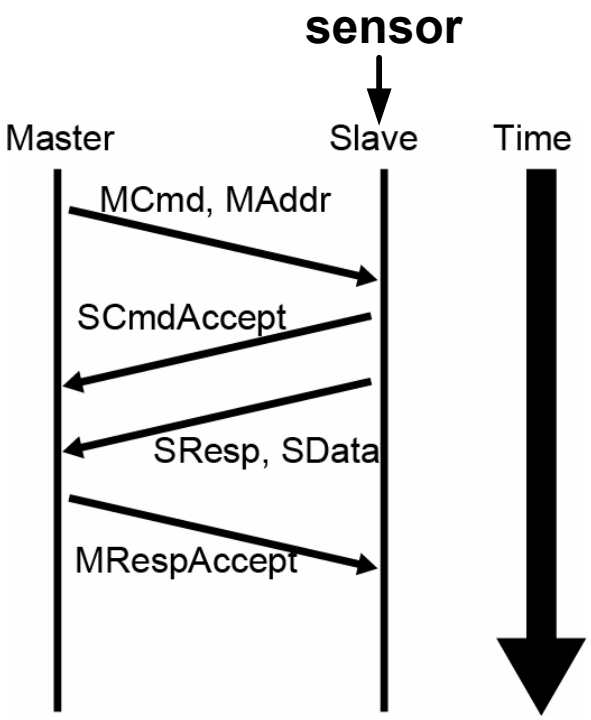


Table 4.1: OCP Bus Signals

The bus operation is controlled on the edges of *ocpClk*. It contains a *ocpReset_n* pin for resetting the components on the SoC platform. 3 bits are dedicated for the command control. Among these commands mainly the read and write commands are used for the CMOS image sensor. The sensor has a spesific address which Soc CPU can access. 16 bit data package can be read or written at once. *ocpMRespAccept*, *ocpSCmdAccept*, *ocpSResp* are the handshaking signals for accurate data transmission between the sensor and the OCP bus.

To describe this handshaking operation, in the beginning, the master command and address signals are passed to the sensor. Then sensor sends a high pulse via *ScmdAccept* bit indicating the acceptance of the command from the OCP bus. Note that, simultaneously the sensor data is also latched to the OCP bus. Finally the SoC CPU, namely the master, sends a high pulse from the *MrespAccept* bit and the data transmission is completed.

All of the important aspects of the sensor are parametrized to be easily input by the user. The timing adjustments, Region of Interest (ROI) readout and the ambient light suppression selection can be easily handled by the user via the data bits sent by the SoC CPU as shown in Figure 4.7. Instead of the whole pixel array, the user may want to acquire an image corresponding to a certain part of it and this is defined as the ROI readout. In this case, the column and row start/end addresses must be sent to the sensor.

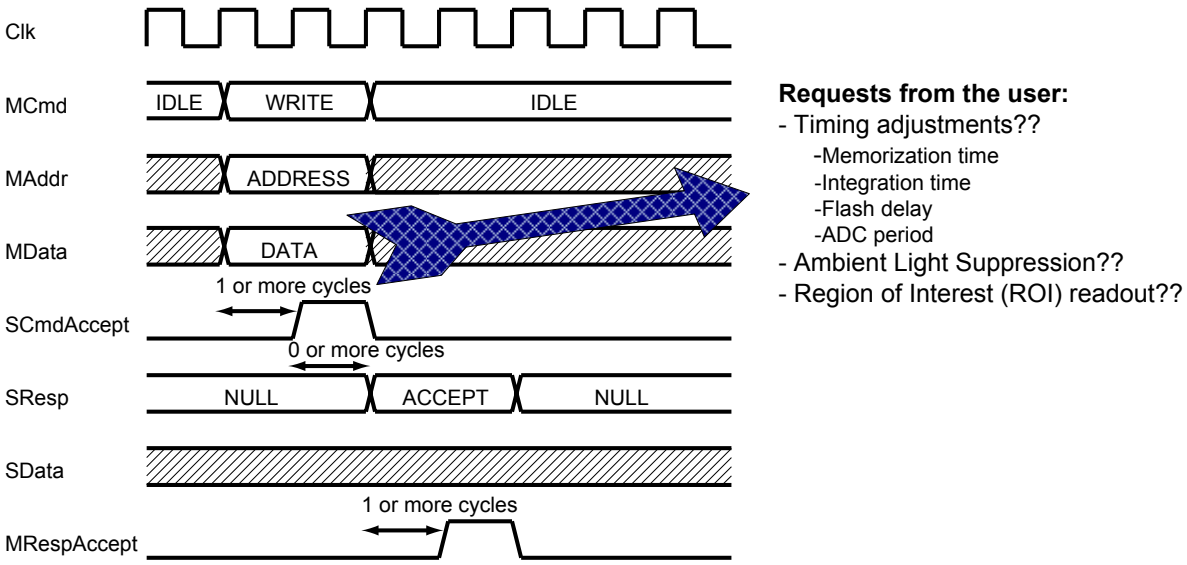
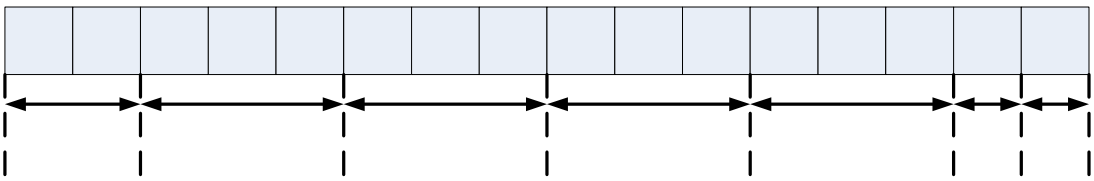


Figure 4.7 Compatible user requests

Among the timing adjustments, memorization time stands for the time interval in which the ambient light is memorized inside the switched current memory. The integration time is the subtraction duration of the ambient current. Actually ambient light suppression takes place inside this duration. As the subtraction switch and the source light must be turned on at the same time and as there can be some delay between these two signals, the flash delay timing is done to completely synchronize these two signals. The ADC period adjustment indicates the amount of time used for the analog-to-digital conversion.

The ambient light suppression and the region of interest (ROI) readout choices also depend on the user. These operations can be enabled by the user by means of the data package sent to the sensor.

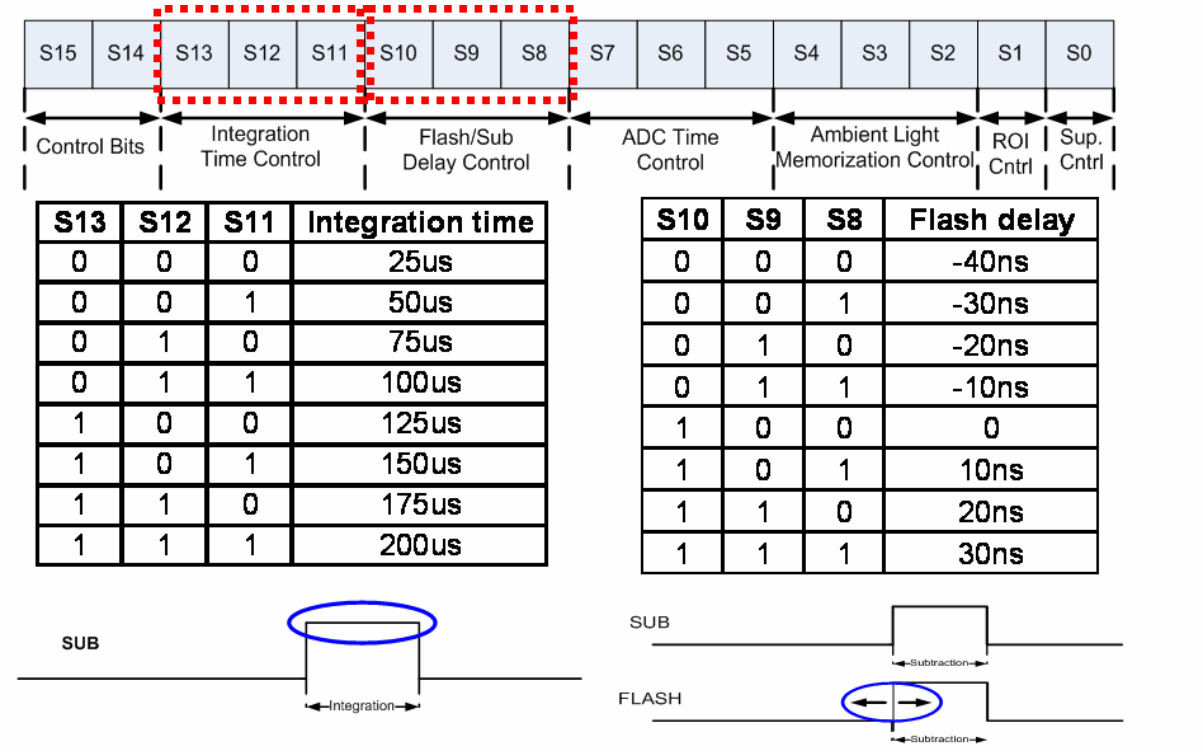
For the sensor to encode the incoming information correctly, a 16 bit status register was formed in the sensor controller and each bit of this register was dedicated to different purposes as seen in Figure 4.8.



S15	S14	Function
0	0	Timing adjustment
0	1	ROI readout: colstartaddr + MSB of colendaddr
1	0	ROI readout: LSB of colendaddr + rowstartaddr
1	1	ROI readout: rowendaddr

Figure 4.8: Function and timing control

The first two significant bits of the status register are used for encoding the type of information sent to the sensor. It can be either timing adjustment information or a Region of Interest (ROI) readout information. 3 bits are dedicated for each timing adjustment as illustrated in Figure 4.9. This means that there are 8 different possibilities for each value. The integration time namely the ambient light subtraction time can be arranged in the 25-200us interval. There are negative and positive value possibilities for flash delay.

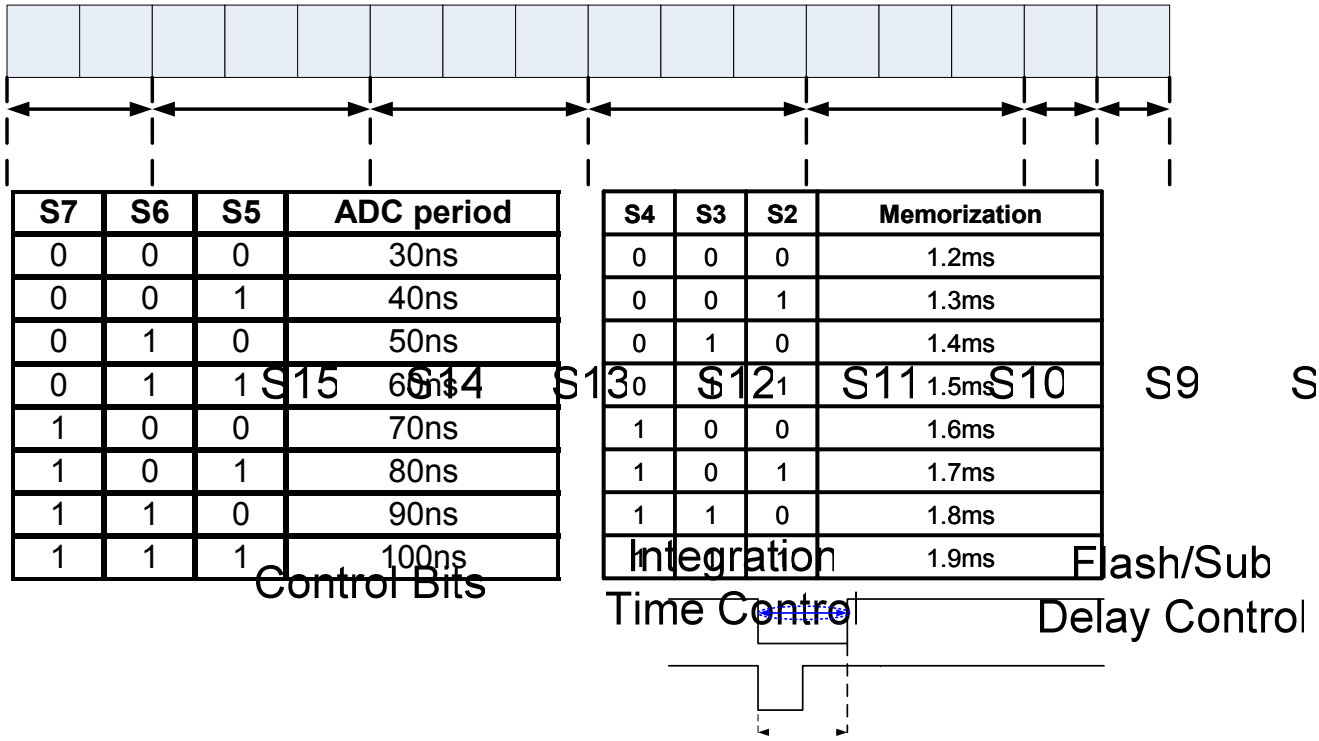


S13	S12	S11	Integration time
0	0	0	25us
0	0	1	50us
0	1	0	75us
0	1	1	100us
1	0	0	125us
1	0	1	150us
1	1	0	175us
1	1	1	200us

S10	S9	S8	Flash delay
0	0	0	-40ns
0	0	1	-30ns
0	1	0	-20ns
0	1	1	-10ns
1	0	0	0
1	0	1	10ns
1	1	0	20ns
1	1	1	30ns

Figure 4.9: Integration time & Flash delay control

Similarly, ADC period and ambient light memorization time are also controlled by dedicated 3 bits in the STATUS register as illustrated in Figure 4.10.

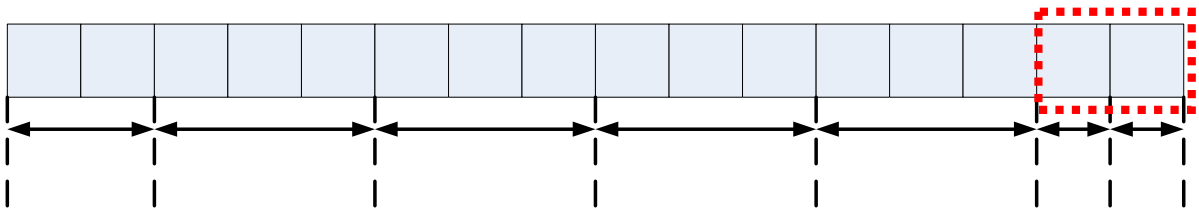


S7	S6	S5	ADC period
0	0	0	30ns
0	0	1	40ns
0	1	0	50ns
0	1	1	60ns
1	0	0	70ns
1	0	1	80ns
1	1	0	90ns
1	1	1	100ns

S4	S3	S2	Memorization
0	0	0	1.2ms
0	0	1	1.3ms
0	1	0	1.4ms
0	1	1	1.5ms
1	0	0	1.6ms
1	0	1	1.7ms
1	1	0	1.8ms
1	1	1	1.9ms

Figure 4.10: ADC period and Memorization time control

The other functions of the sensor controller can also be controlled by the user. These functions are the ROI readout and ambient light suppression choices. They can be also initiated by means of the STATUS register as shown in Figure 4.11.



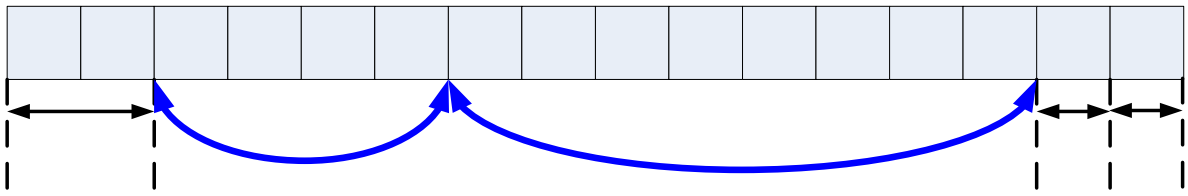
S0	Ambient
0	Suppression OFF
1	Suppression ON

S1	Region of interest
0	ROI OFF
1	ROI ON

Figure 4.11: Ambient light suppression and ROI readout control

In case of a ROI readout the row and column start/end addresses should also be sent to the sensor. This operation can be done in 3 write strobes as we need to transfer 32 bits. The control bits are used for describing the sensor which address, whether it is *colstart*, *colend*, *rowstart* or *rowend* address, is sent to the sensor. This description encoding is shown

in Figure 4.12. The default start and end addresses for column and row are h'00 and h'FF respectively.



S15	S14	Function
0	1	ROI readout: colstartaddr + MSB of colendaddr
1	0	ROI readout: LSB of colendaddr + rowstartaddr
1	1	ROI readout: rowendaddr

Figure 4.12: Address requests of the ROI readout

The ADC outputs are read through the 16x 8bit First-In-First-Out (FIFO) buffer present in the sensor controller. This read command is employed in OCP bus as shown in the following timing diagram in Figure 4.13

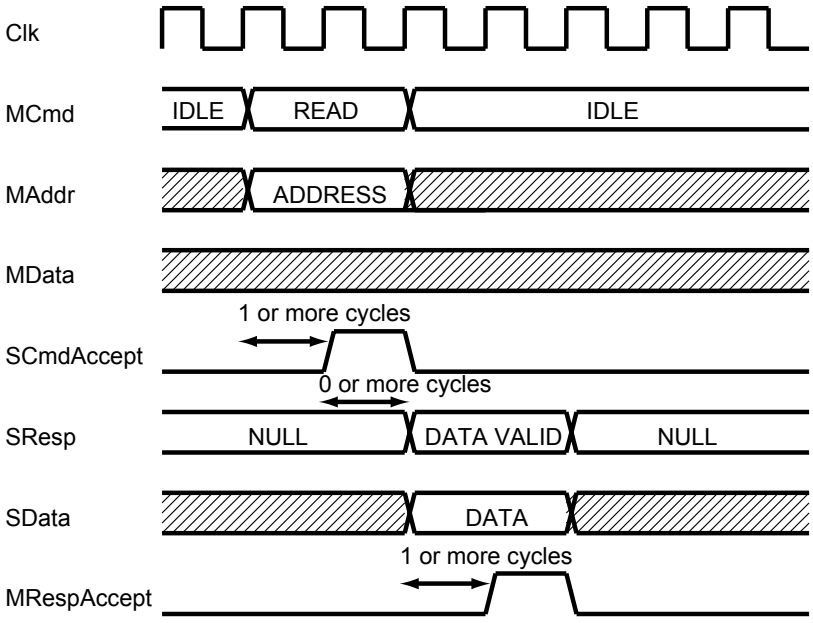


Figure 4.13: ADC output readout

16 pixel data can be stored into this FIFO buffer before the synchronization between the sensor CLK and the OCP CLK is completely realized.

The sensor controller's software code was written in Verilog HDL and then the hardware corresponding to this code was designed in Synopsys Astro by automatic place&route. For this purpose 0.18um CMOS technology standard cell library was used. The generated layout is shown in Figure 4.14. The specifications of the controller block are given in Table 4.2

Specifications	Value
# of ports	82
# of cells	2600
# of nets	2775
# of references	16

Table 4.2: Controller specifications

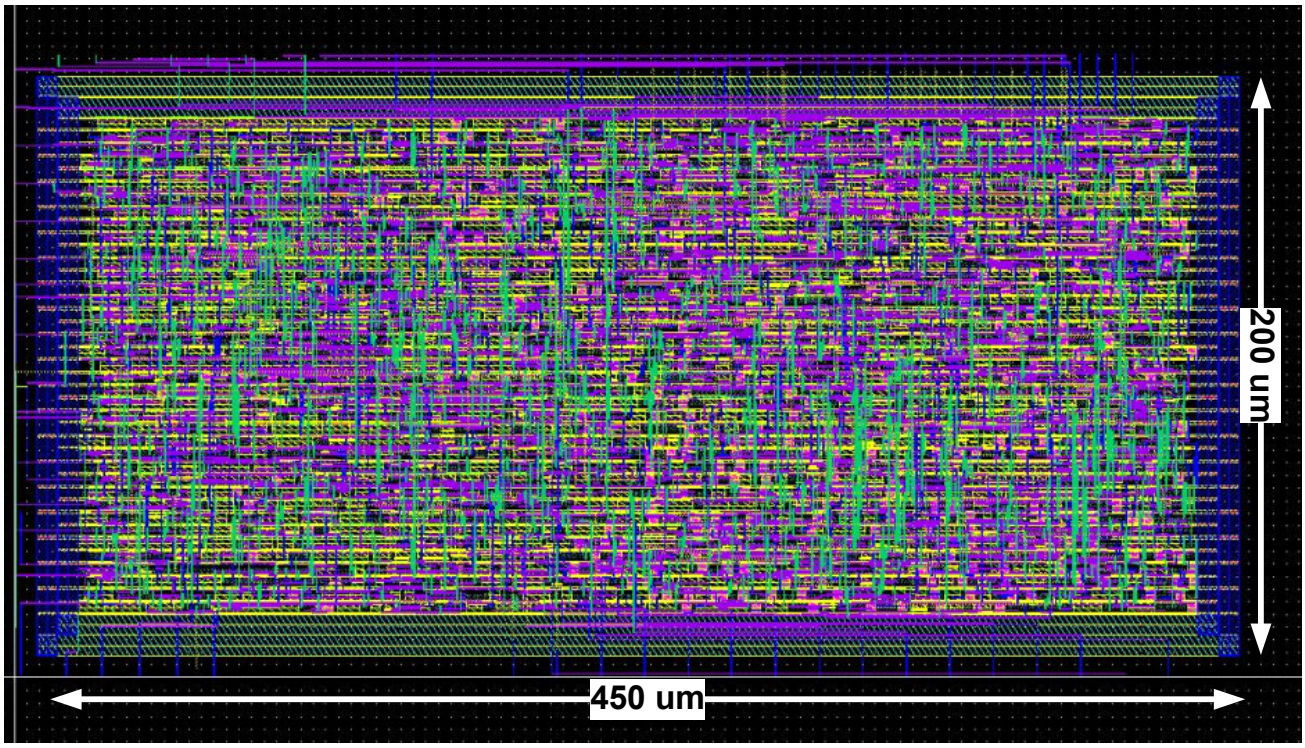


Figure 4.14: Automatically generated layout

The controller layout was embedded to the all sensor layout. In Figure 4.15, it is shown inside the sensor layout associated with its inputs and outputs. For high speed operation inverter buffers were placed to the outputs. Relatively large buffers were chosen for the array signals which are distributed to the all pixels. The CLK of the sensor controller can be fed from two sources. It can be either external or internal. The internal CLK choise is realized by means of a ring oscillator. There is a 2x1 multiplexer, connected to the ring oscillator, for selecting the external or the internal clock.

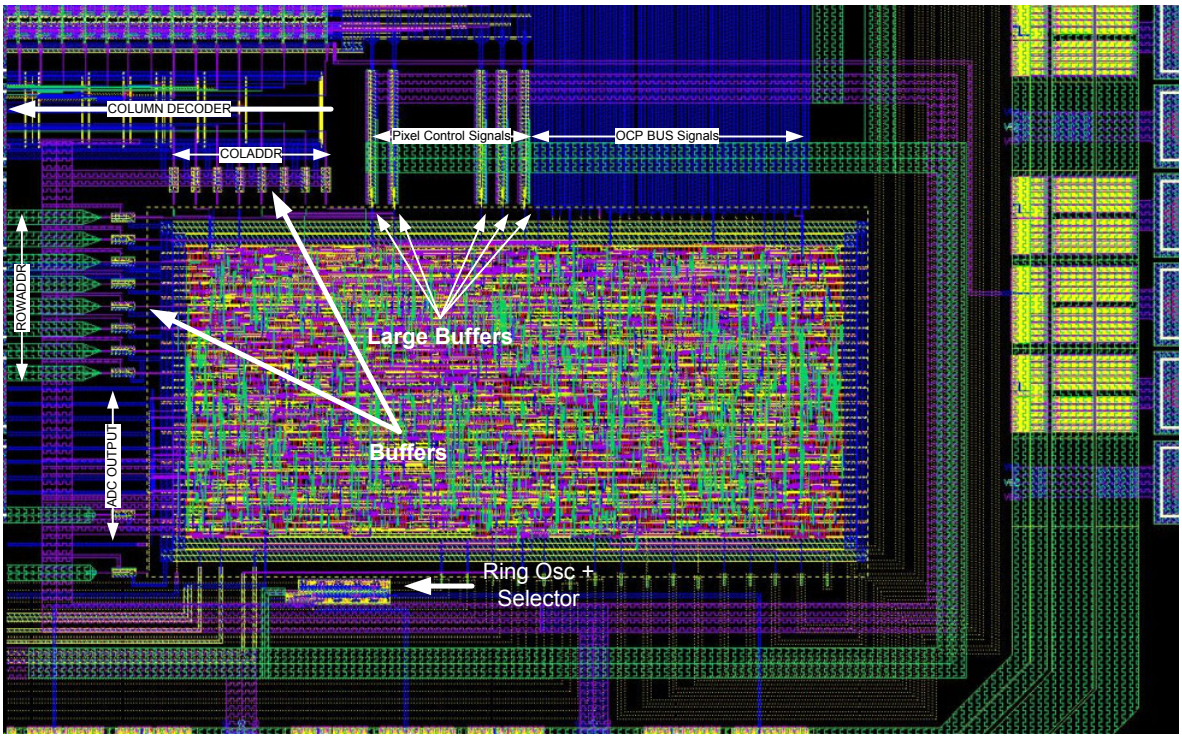


Figure 4.15: Controller layout inside whole sensor layout

The ring oscillator architecture consists of 9 cascaded CMOS inverters. The circuit schematics is shown in Figure 4.16. The frequency can be tuned by a bias voltage applied to the tail NMOS transistors.

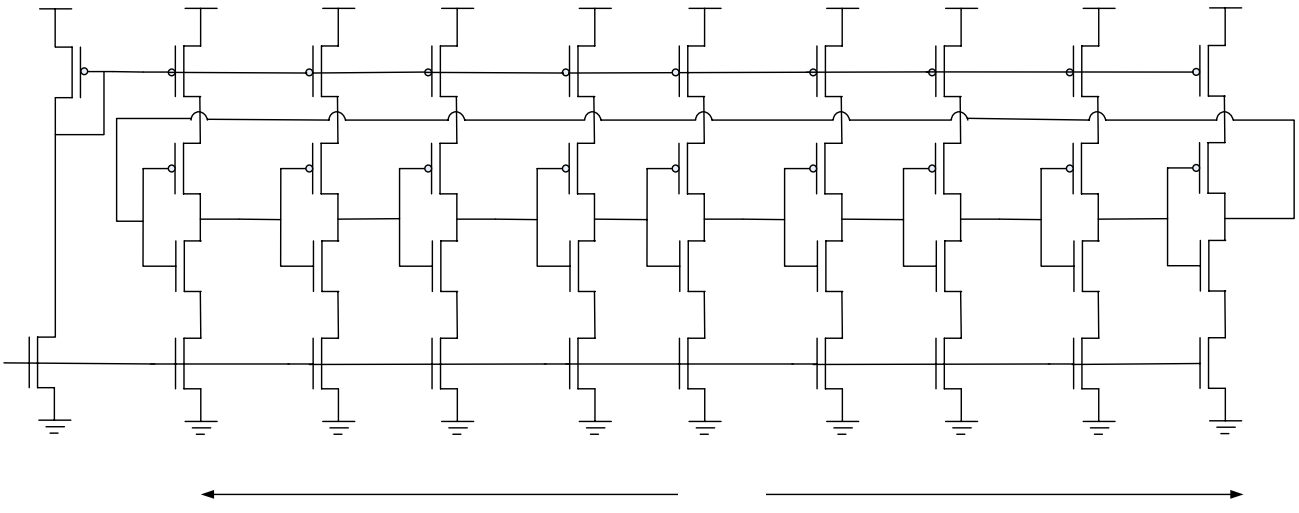


Figure 4.16: Ring oscillator schematics

The internal/external clock selector is a pass transistor logic circuit. Either ring oscillator output or the external clock is transmitted to the output according to the SEL bit. The schematics of the circuit associated with its layout are shown in Figure 4.17.

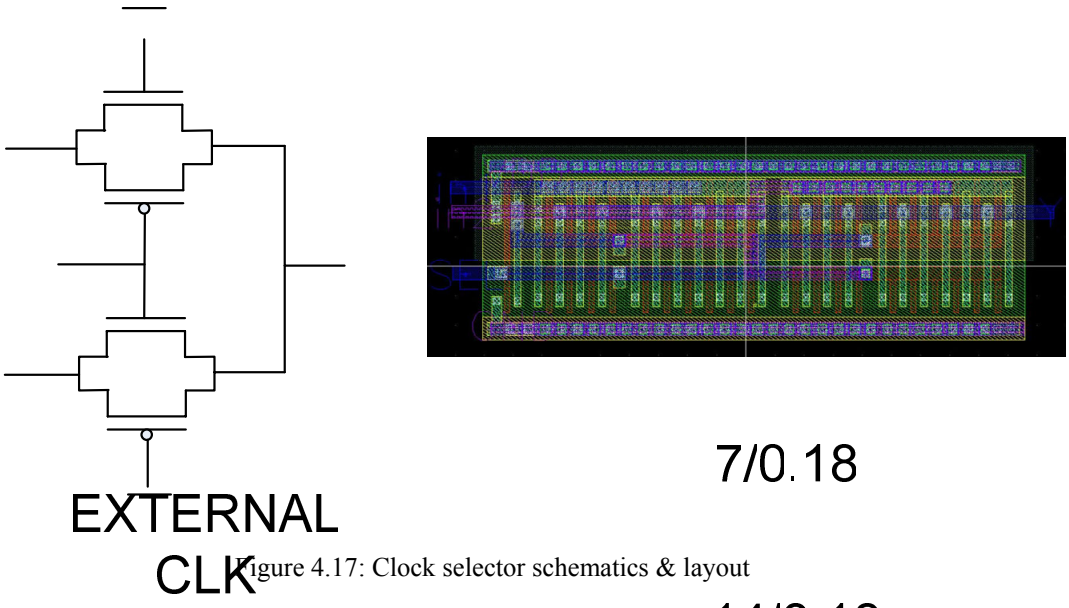


Figure 4.17: Clock selector schematics & layout

The whole layout of the sensor drawn in 0.18 um CMOS process associated with the controller is shown in Figure 4.18. The die size is 5mmx5mm and the resolution is 256 x 256.

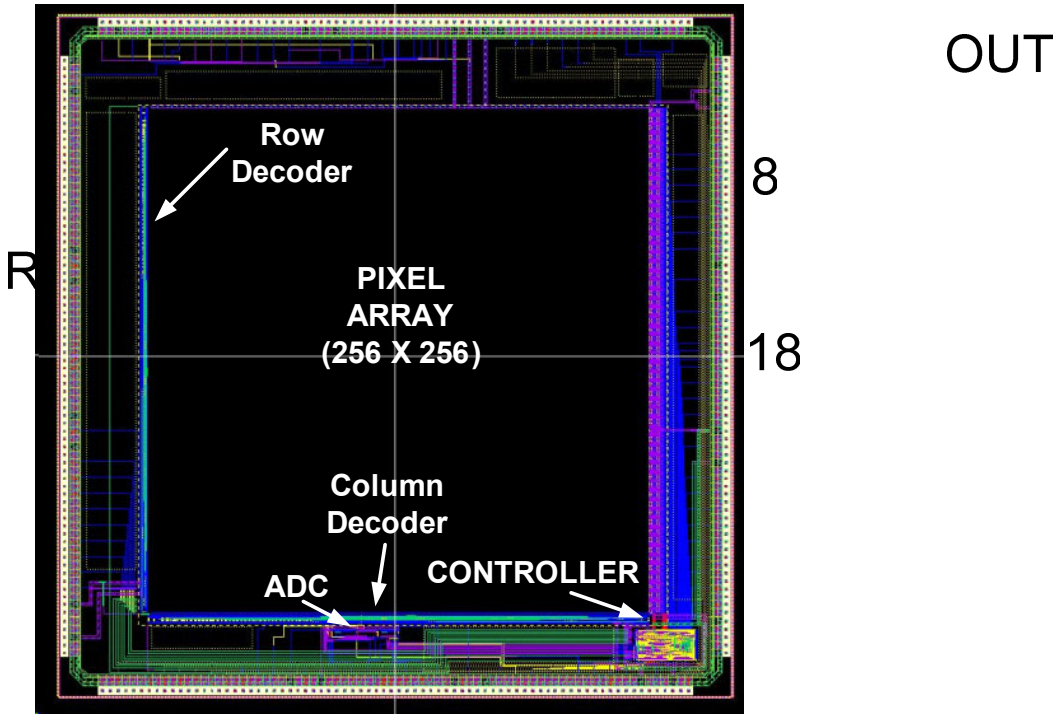


Figure 4.18: Full chip layout

4.3 Simulation Results

Some logic simulations were done on the sensor controller for the configuration, ambient light suppression and readout phases to assure the correct operation. For the configuration phase 3 write strobes are required for completely sending the timing, ROI and

ambient light suppression information as shown in Figure 4.19. In the first write strobe all of the timing information can be transmitted. Actually the sensor controller operation is based on a counter. When the counter counts until some certain number, a signal is made high or low so pulse width modulation is utilized. For instance, integration time is determined according to two numbers. When the counter reaches the first number a high pulse is sent to SUB (the subtraction switch) and when it comes to the second number a low pulse is sent to SUB. So the count difference multiplied by the clock period becomes the integration time.

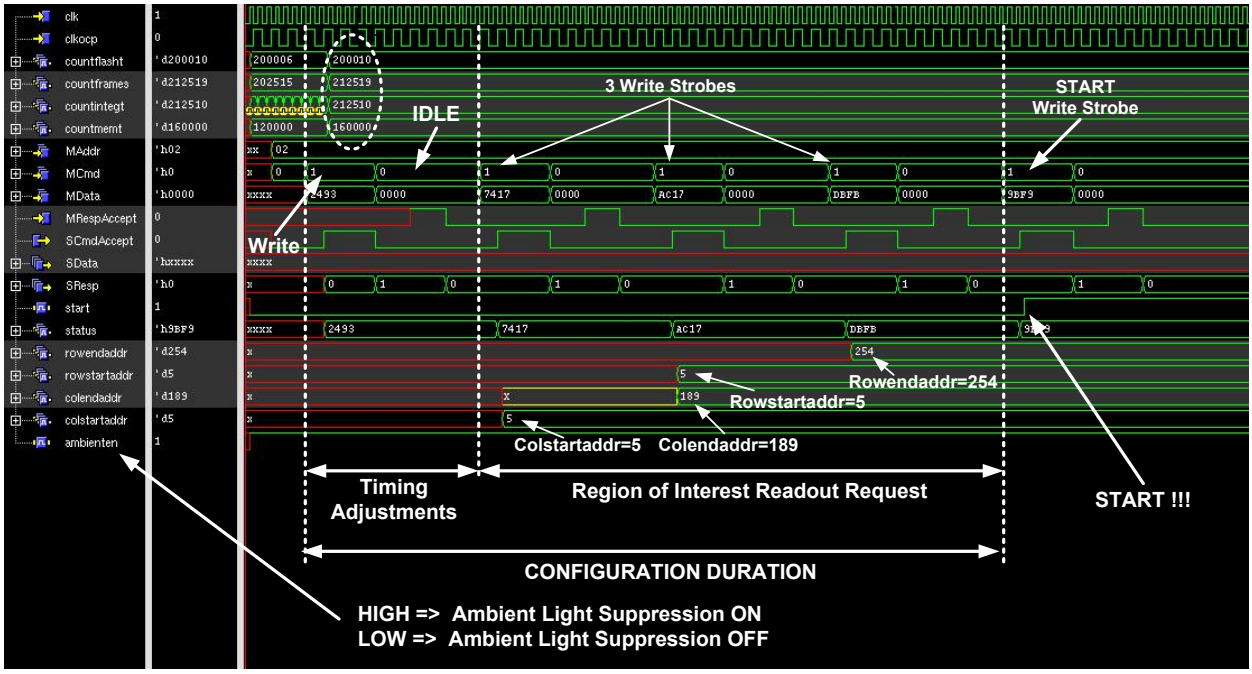


Figure 4.19: Sensor configuration

After the timing configuration in the next 3 write strobes the ROI readout request is sent to the sensor controller. In the first strobe the *colstartaddr* and the 4 MSB of *colendaddr* are sent. In the second, 4 LSB of the *colendaddr* and the *rowstartaddr* are sent. And this request is completed by sending the *rowendaddr* in the third write strobe. By the way through these configurations ambient light suppression function is also enabled or disabled simultaneously. This is identified according to the *ambienten* signal.

After all of the configurations are completed, a high start pulse is sent to the sensor controller and it starts the imaging process. The ambient light is memorized, suppressed and the pixel data is readout respectively. Then it is transmitted from the output FIFO buffer.

The ambient light suppression process inside the pixel is illustrated in Figure 4.20. The current sampling signals, SW1&SW2, the subtraction signals, SUB & FLASH, and the readout signals are successfully generated by previously configured sensor controller. Note

that the starting addresses for the row and column decoders take the value which is previously determined in the ROI configuration.

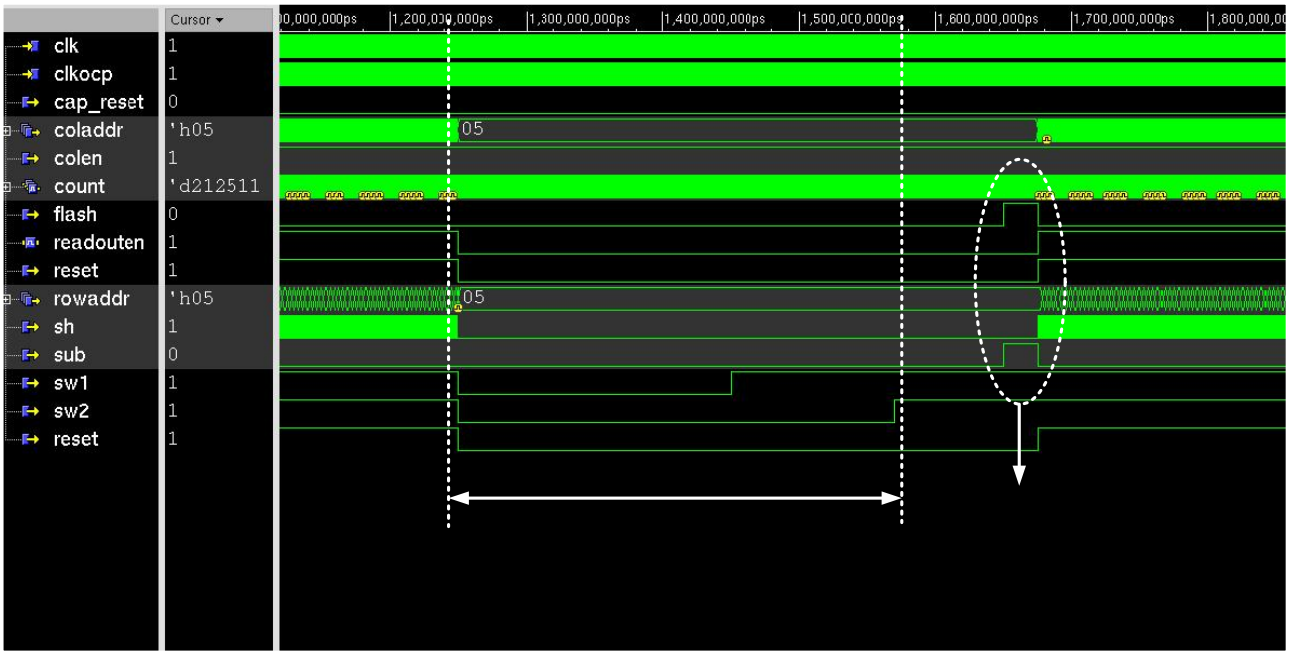


Figure 4.20: Ambient Light Suppression Simulation

After the ambient light suppression takes place inside all of the pixels, readout operation which is shown in Figure 4.21 starts. The pixels are selected one by one by the row and column decoders and analog column values are converted to digital by means of the A/D converter.

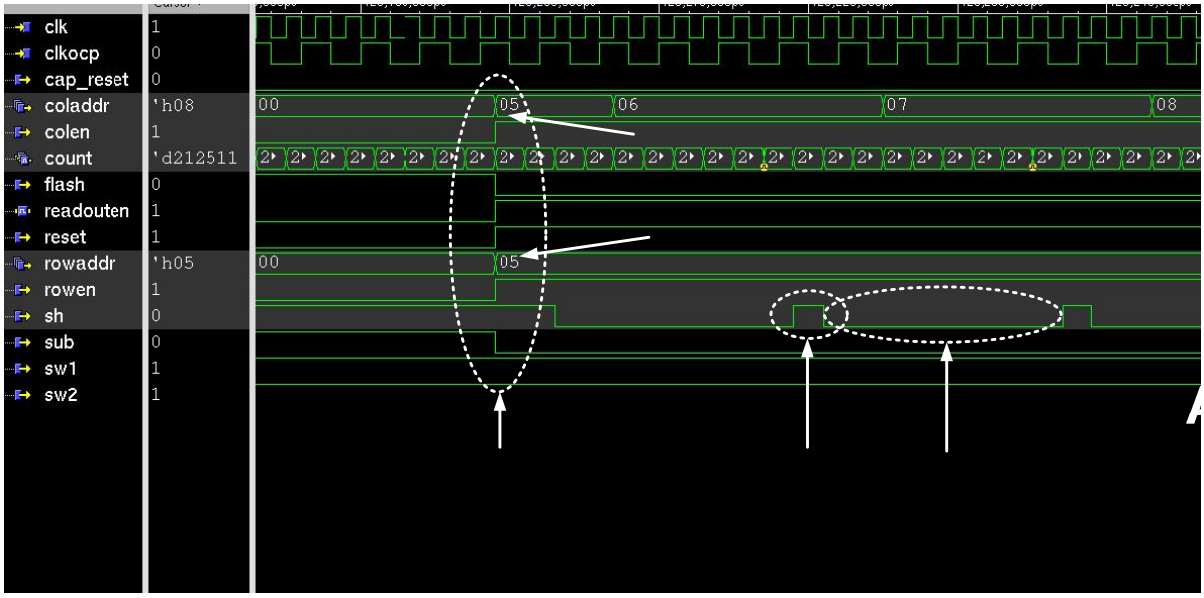


Figure 4.21 Readout Simulation

It should be noticed that the A/D conversion duration also takes its previously configured value.

As mentioned in the previous section the controller clock can be generated either by the ring oscillator or applied externally. The ring oscillator simulation is shown in Figure 4.22. The frequency has been tuned to 100 MHz which is an optimum frequency for the sensor readout operation.

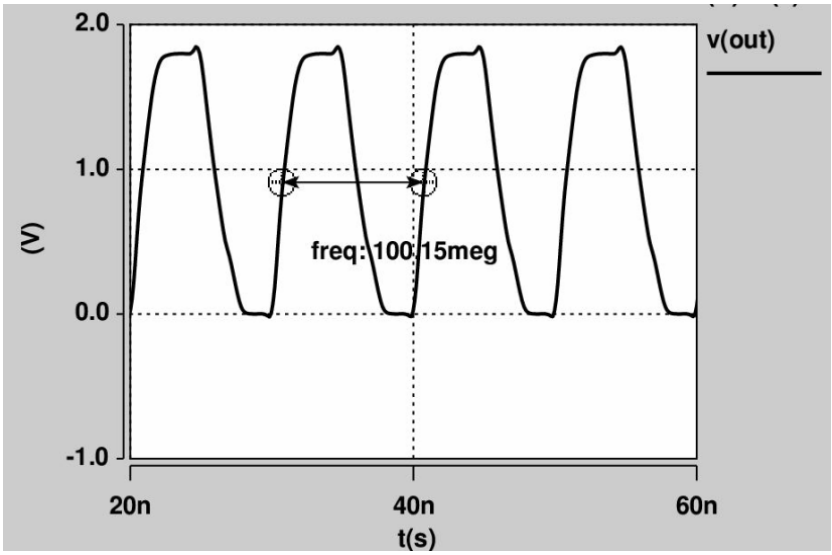


Figure 4.22: Ring Oscillator Simulation

4.4 Measurement Results

The chip photomicrograph is shown in Figure 4.23. It was measured on the measurement board shown in Figure 4.24. A 80 MHz FPGA was used to generate the OCP bus signals for the chip.

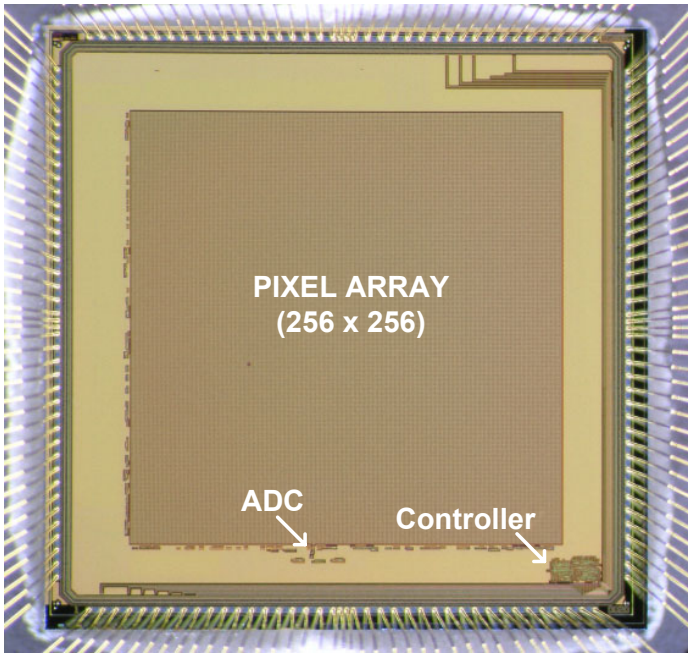


Figure 4.23: Chip photomicrograph

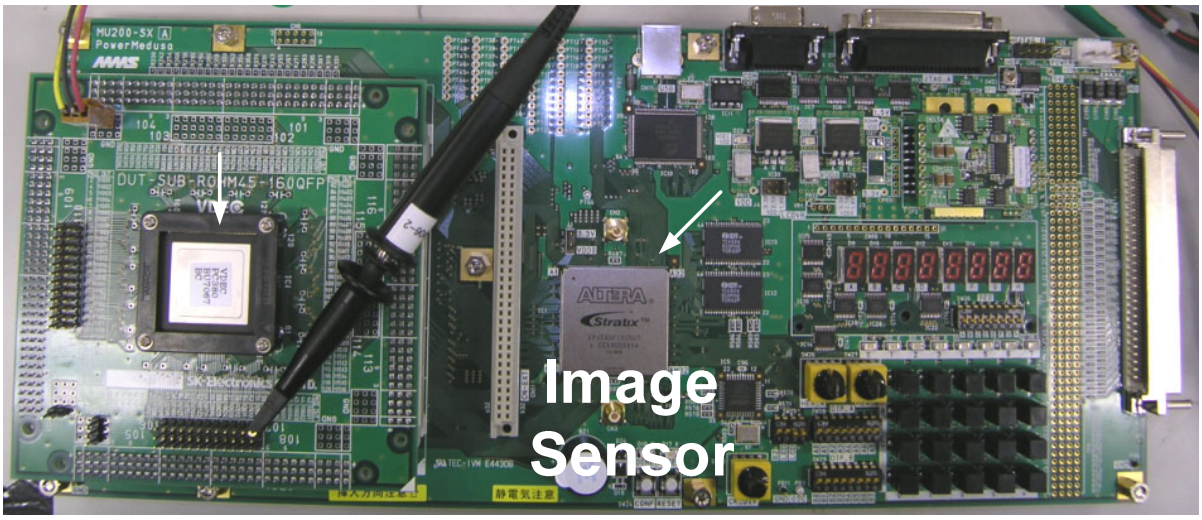


Figure 4.24: Measurement board for the CMOS image sensor

Unfortunately the same reason with the chip described in chapter 3 caused an operation failure for this chip too. Because the sensor controller block is completely digital, it is composed of the erroneous standard cells. So it didn't operate as expected. The manually designed clock selector worked but the other automatically placed and routed parts did not work. Hence we couldn't obtain the image.

4.5 Conclusion

A sensor controller was designed to make the sensor independent of a complicated device like FPGA or PC. The controller has a timing generator and a function selector blocks inside. The timing generator generates the necessary signals for the pixel circuit and ADC. The sensor is capable of Region of Interest readout or ambient light suppression. This is achieved by using the function selector. The clock signal can be either internally generated by the ring oscillator or applied as off chip.

CHAPTER FIVE

CONCLUSION

5.1 Conclusion

Due to the importance of accurate image sensing in various environment conditions, ambient light suppression is a key concept to be achieved. Recently considerable research has been conducted on this topic which could achieve this aim up to some extent. This work will contribute a new improvement to this area with its considerable suppression efficiency performance.

Unfortunately the theory could not be supported by the experimental results but in near future with the error-free chip we believe that good results will be obtained from the measurements.

To sum up, in this work, the design and implementation of a new and efficient current-mode ambient light suppression scheme for CMOS 3D range finders has been described and the simulation results of the CMOS smart image sensor designed in a 0.18-um CMOS process have been presented. The sensor operates with a high accuracy in a very weak current range and the effect of the charge injection related with the ambient light storage is reduced significantly by employing an efficient charge compensation scheme. The sensor is capable of operating in very high illumination environments with a weak source light. Because of that, the sensor can achieve a -32 dB Signal-to-Background Ratio(SBR). Hence in case of a laser source, it is supposed to be significantly harmful for the human eye. Moreover the system uses less power when compared with conventional range finding system as the source laser power is very low.

The switched current memory is a good solution for ambient light storage purpose for the pixel circuit. The pixel can successfully suppress the ambient light with a very high suppression efficiency which is found to be approximately %99.

Because the sensor has an internal sensor controller, it does not need a complex controlling device like FPGA or PC. So its performance is not affected in that regard. Because of this beneficial independence, it can be used in various System-on-Chip environments.

As a future work this pixel circuit can be adopted to a 3D range finding system so a 3D imaging can be achieved without the effects of the ambient light. Moreover this system can be used for outdoor environments enabling it a good base for various applications.

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