

Abstract

The large-scale integrated circuit (LSI) industry has been rapidly developed for more than 30 years thanks to semiconductor scaling. However, metal-oxide-semiconductor field-effect transistors (MOSFETs), which are elements of LSIs, are now too small and suffer from performance degradation due to quantum-mechanical effects. Therefore semiconductor scaling will face more problems in the future.

With that background, the needs for alternatives other than scaling have become pointed out more and more. One of the alternatives is to introduce novel devices into conventional complementary-MOS (CMOS) LSIs and achieve more efficient, functional information processing. Single-electron transistor (SET) is one of such devices, which has a different operation principle to that of MOSFET and show unique characteristics called Coulomb oscillation. Exploration of circuit configurations is necessary for practical LSI use to take advantages of such unique characteristics and cover disadvantages of SETs. Improvement of SET fabrication techniques are also required to achieve practical reproducibility and yield.

The objective of this work is to explore the feasibility of SET/CMOS fused information processing systems as a possible future LSI configuration by circuit simulation. Improvement of a room-temperature operating SET fabrication process is also discussed for practical use of SETs.

Analog pattern matching is one of promising LSI applications of SETs. Although device-level demonstration of that was achieved, there are a lot of things to do in order to realize circuit-level operation. As a first step, the feasibility of automatic characteristics control of floating-gate SETs (FG-SETs) using CMOS digital/analog peripheral circuits was evaluated by mixed-signal simulation. An analytical model of FG-SETs was developed for this simulation based on an existing analytical model of SETs which considers discrete energy levels in the island of a SET, and it was confirmed that the model reproduces characteristics of an actually fabricated device. A Coulomb oscillation peak position detection and control circuits were simulated, incorporating a modeled FG-SET with the parameters extracted from the actual device. Simulation results showed that the proposed circuits work well in principle.

Several fabrication techniques of Si-based SETs have been reviewed, and compared in terms of possibility to realize high-yield room-temperature operating single-dot SETs. Si nanowire channel SETs are attractive because clear characteristics are already obtained at room temperature. However, its fabrication process suffers from poor controllability and yield due to wet etching of silicon and insufficiently-optimized electron-beam (EB) lithography process. By optimizing EB drawing condition, precisely width-controlled sub-20-nm wide Si nanowires were obtained. That will improve controllability and yield of the conventional room-temperature operating SET fabrication process.