博士論文（要約）

Study on Performance Improvement of Ge-source/Si-channel Hetero-Junction Tunneling Field-Effect Transistors

（Ge ソース/Si チャネルヘテロ接合トンネル FET の性能向上に関する研究）

1th June, 2018

37-157286

Tae-Eon Bae (裵　泰彦)

Supervisor　Prof. Shinichi Takagi

論 文 の 内 容 の 要 旨

論文題目　Study on Performance Improvement of Ge-source/Si-channel Hetero-Junction Tunneling Field-Effect Transistors
(Geソース/Siチャネルヘテロ接合トンネルFETの性能向上に関する研究)

氏　名　裵 泰彦

Tunneling field-effect transistors (TFETs) with a gate-modulated band-to-band tunneling (BTBT) mechanism have been considered as one of the promising switching devices to replace Si metal-oxide-semiconductor FETs (MOSFETs) for ultra-low power applications. By employing the BTBT mechanism, TFETs can achieve sub-60 mV/decade subthreshold swing (SS) at room temperature, which is lower than the lowest limitation of SS in MOSFETs, determined by the thermionic emission mechanism. Tunneling probability of the TFET strongly depends on the energy band gap of materials. Ge with the small band gap is expected as a suitable material for the TFET sources. Ge has approximately half the band gap compared Si and small effective mass, which provide larger I_{on}. Thus, a Ge-source/Si-channel hetero-junction TFET is one of the promising device structures. Here, the Ge/Si hetero-structure with the staggered type-II band alignment can effectively reduce the tunneling width in the source junction. In addition, the large bandgap of the Si channel and drain can suppress the leakage current. However, the impact of the device parameters on the electrical properties in the Ge/Si TFETs has not been fully examined yet. Therefore, in this thesis, we examined the impact of the device parameters on the electrical properties of Ge-source/Si-channel TFET including its physical understanding.

For high quality Ge/Si hetero-interface, Ge layer was grown with the in situ B doping and without heat treatment by low temperature MBE. Ge films were grown on SOI substrates in a layer-by-layer manner and flat surface roughness. The highly B doping concentration in the Ge layers was confirmed both sheet resistance measurement and Raman spectra analysis. Also, abrupt junction profiles of Ge and B with steepness values of 4 and 5 nm/dec, respectively, were realized. It was confirmed that low temperature Ge growth with in situ B doping is quite

effective for the formation of a high-quality Ge/Si hetero-junction satisfying the high B concentration and the abrupt B profile simultaneously.

The impact of the interface properties on device performance of Ge/Si TFET was investigated by annealing gas ambient and the gate metal, respectively. The on current and SS are better in the forming gas PMA than in the N_2 gas ambient. The low D_{it} values in Al_2O_3/Si interface were revealed in forming gas PMA due to the effective hydrogen passivation. In addition, the electrical properties of the Ge/Si TFETs are enhanced in the Al gate metal due to the reduction in D_{it} between Al_2O_3 and Si. It was found that interface properties are strongly affected by gate metal materials and it can affect the TFET performance improvement. The dominant tunneling current in device operation is confirmed by independent temperature and channel length properties.

The effects of the drain and source concentration on the Ge/Si TFET characteristics were also investigated. Firstly, it was found that off current and SS are more improved at lower drain doping concentration due to the decrease in tunneling current near the drain side. The large I_{on}/I_{off} ratio of $2x10^6$ and steep SS_{min} and SS_{avr} values of 64.2 and 78.4mV/dec are obtained at the I/I dose of $3x10^{14}$ cm^{-2}. Next, we also found that I_{on} and SS are significantly affected by the B concentration in the Ge source. The large I_{on}/I_{off} ratio of $5.7x10^6$ and low SS_{min} of 63.8 mV/dec are obtained for the mid-level Ge source concentration of $9x10^{18}$ cm^{-3}. We concluded that SS value was degraded in the highest source concentration because of the depression of the energy filtering effect in the band edge between Ge and Si.

To enhance the drive current and electrostatic characteristic, tensile strain in Si channel and EOT scaling were suggested in Ge/Si TFET. Firstly, unstrained SOI and two types of strained SOI substrates with 0.8 and 1.1 % biaxial tensile strain are used and the strain values are confirmed by Raman spectra. It was confirmed that an increase in tensile strain leads to the increase in I_{on} due to the reduced effective energy band gap and the decrease in I_G because of the higher barrier height between insulators and sSi. Next, in order to improve device performance, HfO_2 layer with thin EOT instead of Al_2O_3 was used as gate dielectric. It was found that HfO_2 is appropriate material as gate oxide in terms of CET, leakage current, and interface properties by evaluating the MOS capacitor. As a result, the large I_{on}/I_{off} ratio of $9.2x10^6$ and steep SS value of 60.6 mV/dec in the Ge/Si TFET with HfO_2 are obtained.