博士論文

Physics of soft error due to radiation-induced noise under the buried oxide layer in SOI devices

(SOI デバイス埋め込み酸化膜下で発生したノイズに起因するソフトエラーの物理)

37-157287

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Abstract

Fully depleted (FD) silicon-on-insulator (SOI) technology with buried oxide layer (BOX) has various advantages. One of these advantages is the reduction in power consumption which is achieved by adding a bias to the body from below the BOX, called the back-bias, thereby reducing the leakage current at standby mode. The soft error sensitivities to terrestrial neutrons is also less than 1/15 of that of conventional bulk device, drawing the attention for the technology's potential in space application, making the thin-BOX FD SOI device a good candidate for realizing Internet of Things (IoT). Considering these advantages, thin-BOX FD SOI devices may also have high potential in space application, where energy is limited, and great radiation hazard is expected.

To evaluate their endurance against radiation, recently, a heavy ion test was carried out by our research group. In the test a 65-nm thin-BOX FD SOI SRAM was used. Each chip consists of 2-Mb memory cells. Each of them contained 512 banks of 4-kb subarrays. Each bank had a 64 x 64-bit matrix. A 2-V back-bias was applied to the chip, which served as the standby mode of the device. Heavy ions with linear energy transfer (LET) up to 70 MeV·cm^2/mg were irradiated on to the chip. Without the back-bias, most soft errors took the form of SBU and a small number of MCU. For the case of 2-V back-bias, MCUs with a long line-type pattern along the bit line were observed, and these MCUs dominated the response from heavy ion strikes. While the line-type MCU should be correctable by ECC since only one cell was disrupted in every word it crossed, it is highly probable that multiple MCUs may overlap the same word, resulting in errors unfixable by ECC.

It has been suggested by previous work that temporal potential changes under the BOX layer due to the ion strike is what caused the cell upsets on top of the BOX. These noises travel along the bit line inside the structure under BOX and disrupt multiple cells along the path. To investigate the radiation-induced noise under the BOX and the line-type MCU it causes, a novel theoretical model discussing the physics taking place inside the ion-struck triple-well structure was proposed.

This work paved way to several methods to reduce the noise under the BOX and the line-type MCU it causes without interfering with the operation of the device or changing the structure of the device significantly. By eliminating the line-type MCU, the reliability of the thin-BOX SOI technology is strengthened, and its application in IoT may be safely expanded to environments with radiation concerns.

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Chapter 1 Introduction

1.1Research Background and Purpose

1.1.1 Background

Radiation has been known as one of the sources to causes reliability problems for Large-Scale Integrated Circuits (LSI). Radiation generates electron-hole pairs inside the device, and these charges are collected by the device terminals, causing abnormal signals either on the device level or the system level. While it is possible that the device suffers no permanent damage, these abnormal signals are still capable of disrupting stored data or producing unexpected output. This phenomenon is called soft error. For instance, Static Radom-Access Memories (SRAMs) may suffer from change of memory state once hit by radiation.

One of the earliest reports of soft errors came from space missions. While in space, LSIs experience a radiation hazard much more severe than inside earth's atmosphere. To counter these soft errors, several measures have been taken which mostly involves increasing redundancy to the device. However, decreasing the device sensitivity to soft error by design should be a solution that solves the problem by the root. And with the constantly ongoing scaling of the circuits and the increase of complexity in modern space missions, the call for reliability against soft errors is growing. On the earth's surface, even though the presence of radiation is often not as hazardous as that of space, soft errors still cause critical problems. Major radiation sources include alpha particles, terrestrial neutrons.

To discuss the reliability of the device against soft error, failure in time (FIT) is often used as the way of evaluation. FIT is usually expressed as the number of errors per billion hours. As memory device scales down, the sensitive area of each memory cell becomes smaller. However, the critical charges required to disrupt the cell, Q_{crit}, also reduces, and the number of cells in a unit area of the device also increases. All these factors must be considered for reliability evaluation. The sum of these factors differs from on case to another. Consequently, sensitivity to soft error for different device has shown different trend of changes. For Dynamic Random-Access Memories (DRAMs), the soft error sensitivity drops with scaling trend [1], [2], as depicted in Fig.1.1. On the other hand, SRAMs become more sensitive to soft error as device scales down [2], [3], [4]. This opposite trend is shown in Fig. 1.2. Therefore, SRAM protection against soft error has been gaining importance.

For SRAMs, most soft errors take the form of single bit upsets (SBUs), where one radiation particle strike results in one disrupted cell [Fig. 1.3]. In some relatively rarer cases, one strike can disrupt multiple cells at the same time, called multi-cell upsets (MCUs). In many applications, error correction code (ECC) is used to correct the soft errors. It's typical to expect multiple ions strikes at the same time. For the case of MCU, it is easy to accumulate multiple errors in a single word, making the correction by ECC more difficult [5], [6]. Therefore, it is crucial to study and prevent the occurrence of MCUs in SRAMs.

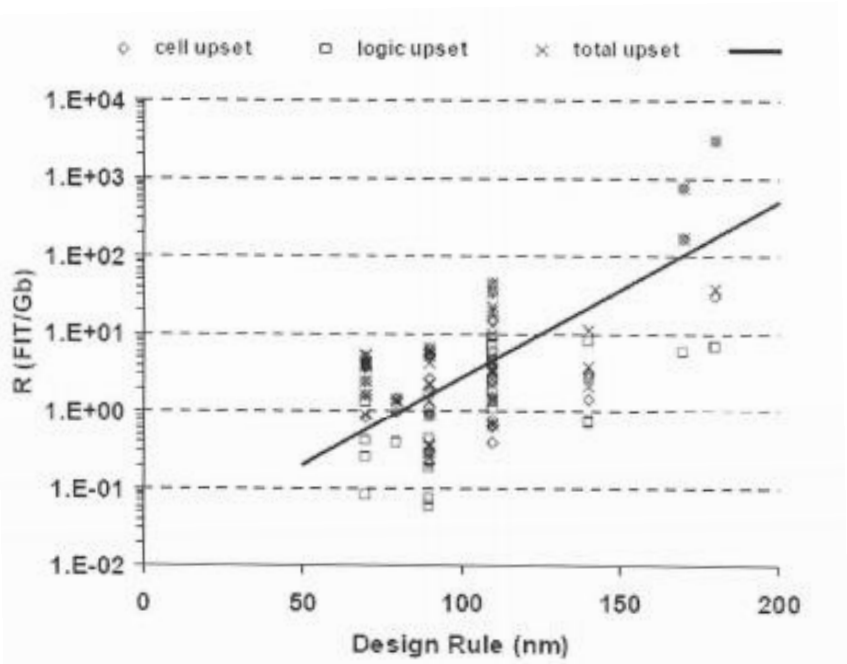

Figure 1.1. Scaling trend for the FIT/Gb rate of DRAM normalized to the neutron flux at New York City for a 1-Gb chip [1].

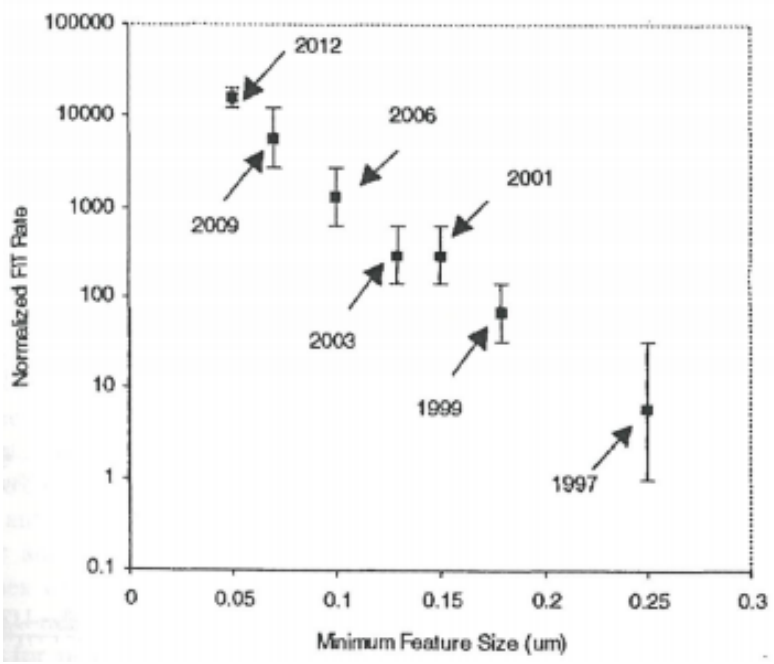

Figure 1.2. Scaling trend for the FIT/bit of SRAM and dynamic logic arrays, predicted in 1999 [3].

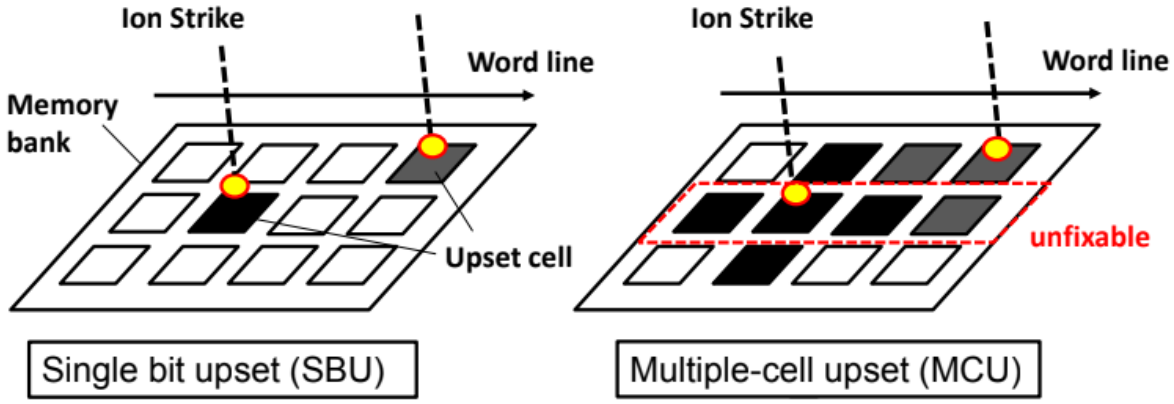

Figure. 1.3 Conceptual drawings showing SBU (left) and MCU (right) in a memory bank.

Fully depleted (FD) silicon-on-insulator (SOI) technology with buried oxide layer (BOX) thinned down to around 10 nm has various advantages [7], [8]. One of these advantages is the reduction in power consumption. This is achieved by adding a bias to the body from below the BOX, called the back-bias, V_B, thereby reducing the leakage current at standby mode [9], [10], [11]. Figure 1.4 shows the leakage current at standby mode for different V_B. In one study, the leakage current has been reduced by 1/1000 times the one in convention counterparts [12].

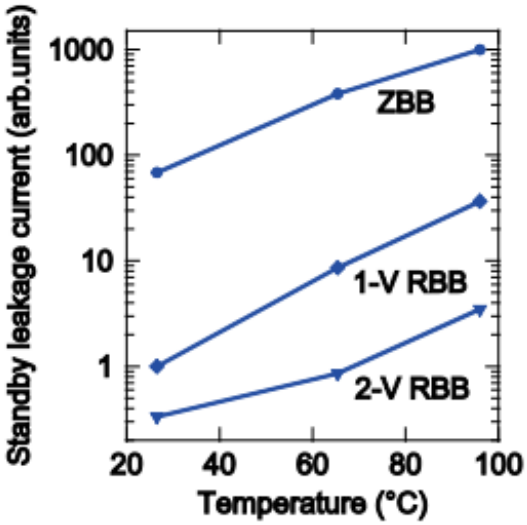

Figure 1.4. Leakage current at standby mode for different V_B [11].

The implementation of the V_B is shown in Fig. 1.5 [13]. The soft error sensitivities to terrestrial neutrons is also less than 1/15 of that of conventional bulk device, drawing the attention for the technology's potential in space application [14], [15]. This makes the thin-

BOX FD SOI device a good candidate for realizing Internet of Things (IoT). Considering these advantages, thin-BOX FD SOI devices may also have high potential in space application, where the source of energy is limited, and great radiation hazard is expected.

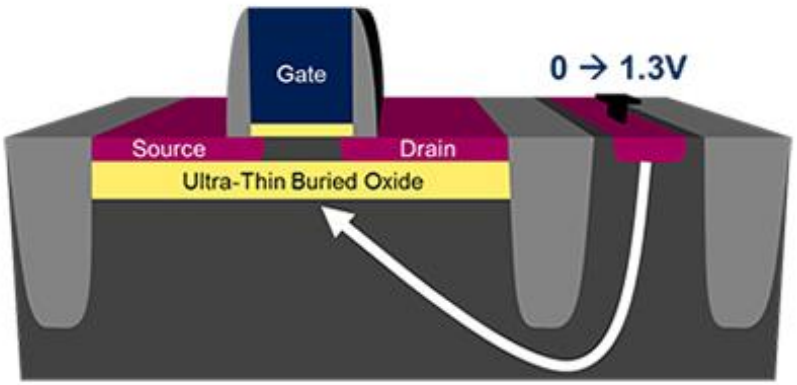

Figure 1.5. Conceptual drawing of FD SOI transistor receiving a back-bias [12].

To evaluate their endurance for space application, a heavy ion test is required to represent the space environment. The ion test was carried out by our research group [16], [17]. In the test a 65-nm thin-BOX FD SOI SRAM was used. Each chip consists of 2-Mb memory cells. Each of them contained 512 banks of 4-kb subarrays. Each bank had a 64 x 64-bit matrix. A V_B = 2-V was applied to the chip, which served as the standby mode of the device. The relation between the bias at the p-well, n-well and the back bias, V_B, is defined as: $V_B = V_{Bn} - V_{DD} = -V_{Bp}$. Here V_{Bn} and V_{Bp} are the bias fed to the n-well and the p-well, respectively, and V_{DD} is the power supply voltage. Heavy ions with linear energy transfer (LET) up to 70 MeV·cm^2/mg were irradiated on to the chip with all the cells initially at logic "0". After the ion irradiation, cells that switched their state from "0" to "1" were recorded [Fig. 1.6]. Without the back-bias, most soft errors took the form of SBU and a small number of MCU. For the case of V_B = 2-V, MCUs with a long line-type pattern along the bit line were observed, and these MCUs dominated the response from heavy ion strikes. While the line-type MCU should be correctable by ECC since only one cell was disrupted in every word it crossed, it is highly probable that multiple MCUs may overlap the same word, resulting in errors unfixable by ECC.

Besides the physical pattern of the upsets, the cross section, namely the sensitive area of the chip to radiation, also increased by nearly 100 times when the back-bias was applied to the chip [Fig. 1.7]. This proves that thin-BOX FD SOI technology may not be as robust to radiation as we would hope, and its advantage of reducing standby power consumption by applying back-bias may also be one of its biggest disadvantage. This notion limits the range of application for the technology.

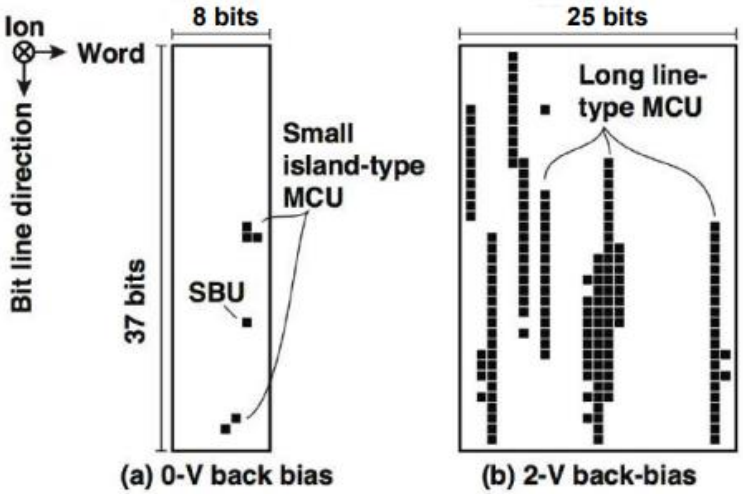

Figure 1.6. Physical map of the upset cells in (a) 8 x 37 partial array and (b) 25 x 37 partial array under Kr irradiation [16].

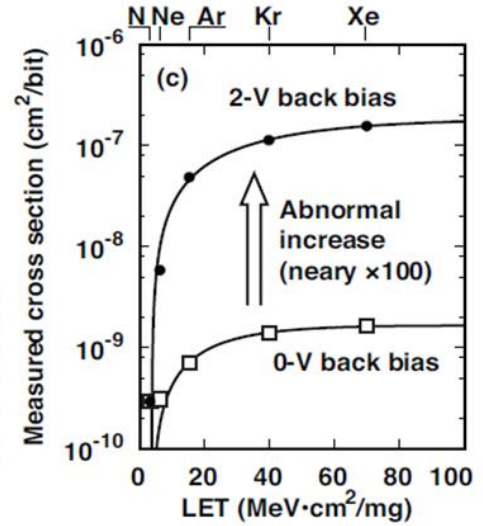

Figure 1.7. Measured cross section for the tested 65 nm thin-BOX FD SOI SRAM chip [16].

1.1.2 Purpose of Research

The line-type MCU is a unique phenomenon. It has been suggested by previous work that temporal potential changes under the BOX layer due to the ion strike is what caused the cell upsets on top of the BOX. These noises travel along the bit line inside the structure under BOX and disrupt multiple cells along the path. However, not much research has been carried out on the physics taking place under the BOX that generate these noises. To fully evaluate the sensitivity of the technology under various circumstances and eventually optimize the design against soft error, the physics of the phenomenon must be understood. The important

part is to recognize how the carriers generated by radiation changes the potential profile of the structure.

A theoretical model based on the physics is proposed in this work. While it is already sufficient to rely on only simulation for the prediction of soft error response of devices, a theoretical model provides a much faster and efficient way of evaluation that does not require long computation time and adjustments based on different device settings, since physics is universal. In this way, evaluation of the line-type soft error and optimization methods can be obtained in an efficient manner.

1.2Thesis Outline

The current chapter introduces the background, including a brief description of the soft error and the influence of technology scaling. The recently discovered line-type MCU is also briefly introduced. The purpose of the research is brought out at the end of the chapter.

Chapter 2 provides more detail on soft errors found in silicon devices. The soft error mechanisms in bulk and SOI technology are introduced and compared. The previously proposed mechanism of line-type MCU and a formula to estimate the length of the MCU are discussed in the latter half of the chapter.

The main work of the author consists of Chapter 3 to 6. A proposed theory on radiation effect on junctions in silicon devices is explained in Chapter 3. This theory allows the derivation of a theoretical formula that estimates the radiation-induced noise. Chapter 4 and 5 each investigates different parameters found in the theoretical formula effecting the noise. Predictions made by the theoretical formula are then verified by TCAD simulation at the end of each chapter. Chapter 6 discuss another important factor of the noise, the duration. To cause cell disruptions, the noise must last longer than the response time of the cells.

Chapter 7 summarize this thesis and discuss the possible directions for further study in the near future.

Chapter 2 Soft Errors in Silicon Devices

2.1 Overview

This chapter talks about soft errors in silicon devices. First, basic knowledge on radiation and soft error is given. Then mechanisms behind soft error in devices of different technology are explained. Comparison is made between conventional (bulk) and SOI devices. Also, for SOI devices, two scenarios are compared. The difference between these two scenarios lies in which region the radiation effect takes place: above or below the BOX layer. The latter mechanism is what contributes to the line-type MCU introduced in the previous chapter.

After the discussion of soft error mechanism for line-type MCU, a method to estimate the length of the line-type MCU proposed by previous work is introduced. It is based on this method that the investigation on the radiation-induced noise can be deemed as important to evaluate the line-type MCU and the sensitivity of the device to radiation.

2.2 Fundamentals of Radiation and Soft Error

Radiation exists in almost everywhere. It is in our surrounding and in space. Fig. 2.1 conceptual drawing showing the radiation sources. Galactic rays and solar particles are main root of radiation. In space, proton, electron and heavy ion consists of the radiation sources in space. On earth, after the shielding effect from the earth's atmosphere, alpha particle and neutron are the main concern in the scope of device reliability from radiation effects.

Radiation particles in space usually have higher particle energy and higher LET than terrestrial ones. In space, heavy ions are the main cause for SEE, while in earth's atmosphere, the effect from neutrons dominate over that from other particles. These particles also react with the device material in the nuclear scale, generating secondary particles that also deposit EHPs in the device. Generally, different particles have different LET in silicon devices, so does the same particle with different particle energy. The flux distribution as a function of LET also differs from one particle to another. Therefore, it is important to sort out the type and profile of the radiation particles in the environment the device is implemented in for a proper investigation.

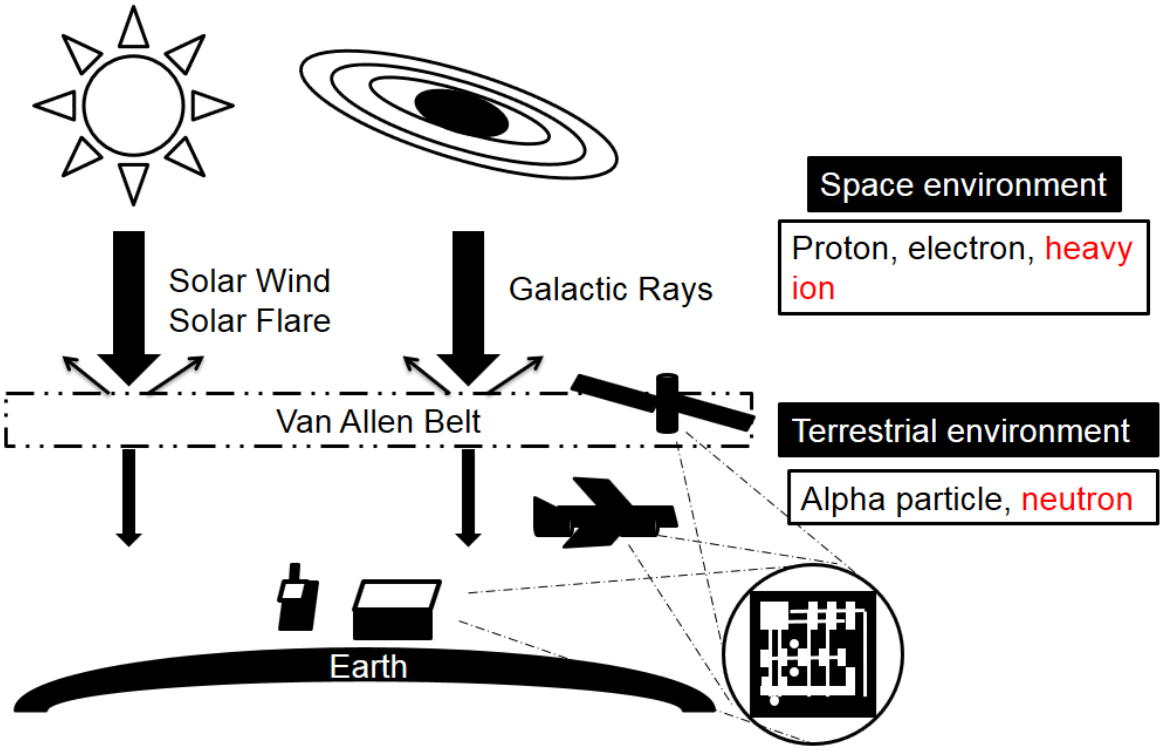

Figure 2.1. Conceptual drawing of the radiation environment in space and on the earth.

In modern era, electronic devices can be found in both space and terrestrial environment, from consumer electronics to aerial vessels. Then ions hit these electronic devices, electron-hope-pairs (EHPs) are generated along the particle track. The higher the LET, the more EHPs are produced. These EHPs travels according to the structure and potential distribution of the region, eventually either dissipated via recombination or collected by the device terminals. Carriers collected by the terminals form a transient current at the device terminal. Even though not a permanent damage, the transient current may cause the memory state of cell to change or an incorrect read by the system. Fig. 2.2 shows the conceptual drawing of the phenomenon.

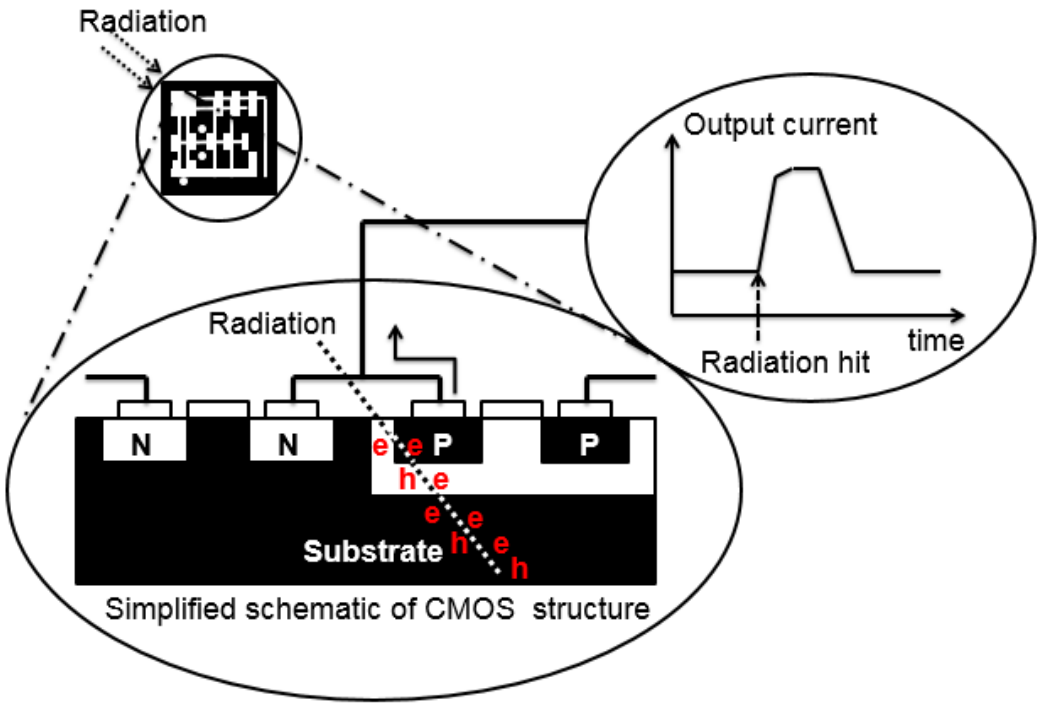

Figure 2.2. Conceptual drawing of EHPs deposition from a radiation particle strike.

Whether or not the ion-struck device will experience a soft error depends on the structure of the device, the position, trajectory, mass and energy of the irradiated particle. The latter two decide the LET of the irradiated particle, or the density of the EHPs generated by the ion along the particle track. The sensitive region of the device, namely the cross section, generally depends of the LET and the flux of the ion. The cross section, σ , is generally expressed as the number of upsets over particle fluence:

$$\sigma\left(\frac{cm^2}{bit}\right) = \frac{upsets\ (n)}{fleunce\left(\frac{n}{cm^2}\right) \times memory\ size\ (bit)} \tag{2.1}$$

To evaluate the soft error rate (SER) of a device under certain radiation environment, two aspects must be considered: the flux distribution of the radiation particles and the cross section distribution of the device, both as a function of LET.

Conventional analyses of soft error provide static modeling [18] and typically involve testing the device with either an ion accelerator [16], [17], [19], or a laser [20], [21]. The number of upsets is recorded after the test, and the cross section of the device is obtained. For a dynamic analysis, the transient current induced by radiation and the charges collected at the terminal over time are investigated [22]. Dynamic analysis is usually carried out using TCAD simulation. One of the benefits of the analysis in the time domain is that it helps to determine whether an effect from radiation is longer than the response time of the device, or in the scope of this study on SOI SRAMs, the flipping time of the cells.

2.3 Soft Errors in Conventional (Bulk) Devices [19]

In bulk technology, the movement of the radiation-induced EHPs are mainly affected by the built-in electric field in the depletion region at the junction. The carriers drift according to the direction of the built-in electric field before the radiation strike and are collected at the device terminals. For a conventional n-type transistor, the sensitive area corresponds to depletion region of the drain region and a portion of the gate [Fig. 2.3].

When a back-bias (negative) is applied to the body of the device, the junction between the drain and the substrate is reverse biased. This widens the depletion region and increase the corresponding sensitive area. Carriers also experience larger electric field and are collected more efficiently. Therefore, an increase in sensitivity to soft error as well as an increase in sensitive area of the device can be expected when V_B is applied [19]. For most cases, one particle strike disrupts one transistor, leading to one single upset bit, or SBU. However, it is still possible for MCUs to occur due to the fact that the transistors are connected by wells. The wells allow the sharing of the radiation-induced carriers between the transistors [6]

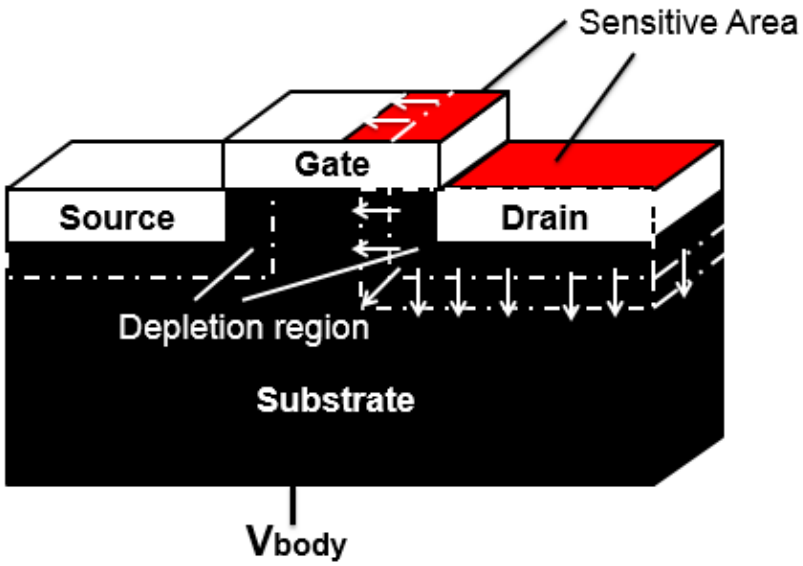

Figure 2.3. Conceptual drawing of a n-type MOS transistor and its sensitive area to radiation.

2.4 Soft Errors in FD SOI Devices

2.4.1 Radiation Effects above the BOX [19]

In FD SOI technology, the body is confined directly below the gate and between the source and the drain. The depletion region between the drain and the substrate is also suppressed. Due to this structure, the mechanism of the movement of the radiation-induced EHPs is different than the bulk technology. A parasitic bipolar transistor is formed by the source, the body, and the drain. The parasitic bipolar effect is what contributes to the collection of charges, Q_{col}, by the terminals, which results from the bipolar amplification of the radiation-induced EHPs, Q_{ind} by a factor of β. The corresponding sensitive area is the gate and the lightly doped drain (LDD).

As explained briefly in the previous chapter, the performance of the FD SOI Device can be enhanced by adding V_B (negative for n-type transistor) from the back side of the BOX [Fig. 2.4]. The result of the potential change to the body counters the parasitic bipolar effect. Thus, the efficiency of the carrier collection rate is reduced, so does the device sensitivity to soft error.

Up to this section, it should be obvious that by applying V_B, the trend of soft error sensitivity for bulk and FD SOI device are different. The former increase with V_B, while the latter decreases with V_B. Investigations have been made to compare the difference in SER for 65-nm technology process [Fig. 2.5, Fig. 2.6]. In the conventional notion, it should be noted that despite the different trend, the SER of SOI device is significantly lower than that of the bulk device. Also, the occurrence of MCU is lower than that of the bulk counterparts, since in SOI technology, most transistors are isolated from each other, which prevents the sharing of the radiation-induced carriers [23], [24]. For the same reason, the size of the MCU is often limited [25]. Typical value of the size is less than 4-bit [26].

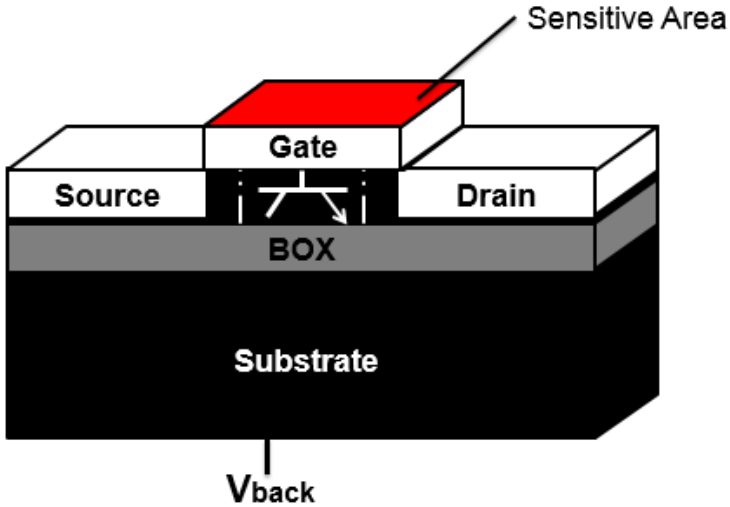

Figure 2.4. Conceptual drawing of a n-type MOS transistor and its sensitive area to radiation.

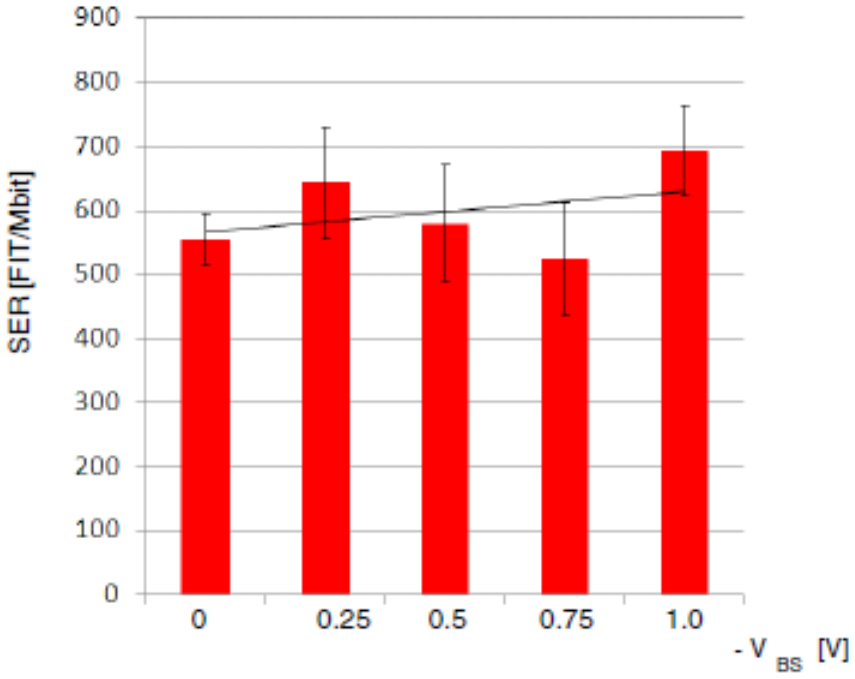

Figure 2.5. Measured SER/Mbit of a 65-nm bulk device plotted against applied V_B [19].

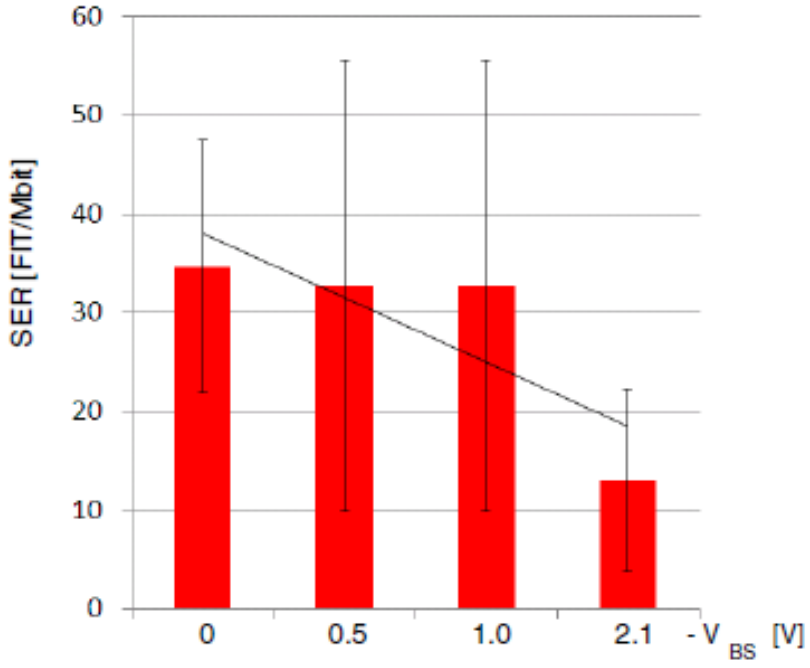

Figure 2.6. Measured SER/Mbit of a 65-nm SOI device plotted against applied V_B [19].

2.4.2 Radiation Effects below the BOX [16] [17]

As introduced in Chapter 1, it has been discovered recently through a heavy ion experiment that EHPs generated below the BOX by radiation particles can result in long line-type MCU. The structure under the BOX is called the triple-well structure, which consists of long p-well and n-well columns imbedded in a large deep n-well [Fig. 2.7]. The n-well and p-well columns are in repeating pattern along the word line while each column stretches along the bit-line from one end of the memory bank to another. At the end of these columns, the wells are biased through contacts from the top of the device. To reduce power consumption at standby mode, the p-well columns are located below the n-type transistors, and the n-well columns are located below the p-type transistors. The formers are fed with a negative bias, V_{Bp}, while the latter are fed with a positive bias, V_{Bn}. The relation between the value of back-bias, V_B, and the bias condition at other terminals is: $V_B = V_{Bn} - V_{DD} = -V_{Bp}$. It has been discovered that by applying a 2-V back-bias to a 65-nm FD SOI SRAM with a thin BOX, the line-type MCU takes place.

The mechanism of the line-type MCU can be explained using the potential diagram in Fig. 2.8. For a 2-V back-bias, the p-well is biased at -2 V. After the ion strike, its electrostatic potential, however, will experience an increase due to the carrier movement. Consequently, the electrostatic potential inside the body of the n-type transistor on top of the BOX will also increase. If this increment is above certain threshold value and lasts longer the response time of the n-type transistor, originally at off state, the n-type transistor will be turned on. This leads to a flipping of the memory state. This fluctuation of the p-well electrostatic potential is what this work describes as the radiation-induced noise under the BOX for SOI devices.

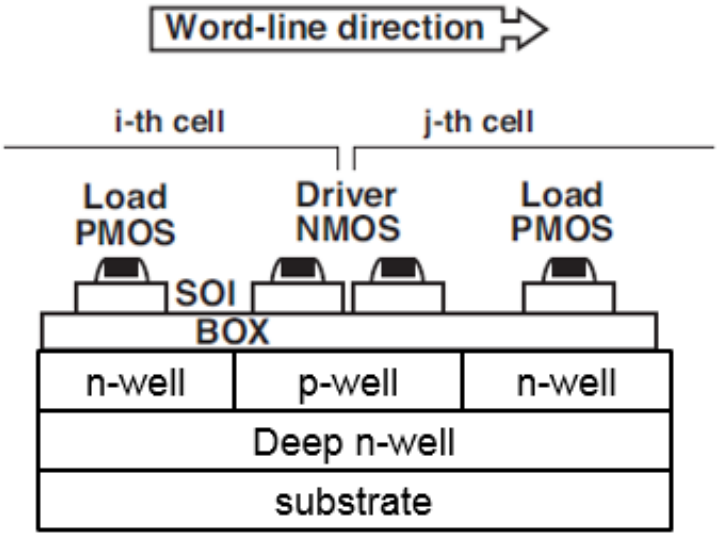

Figure 2.7. Conceptual drawing of a n-type MOS transistor and its sensitive area to radiation.

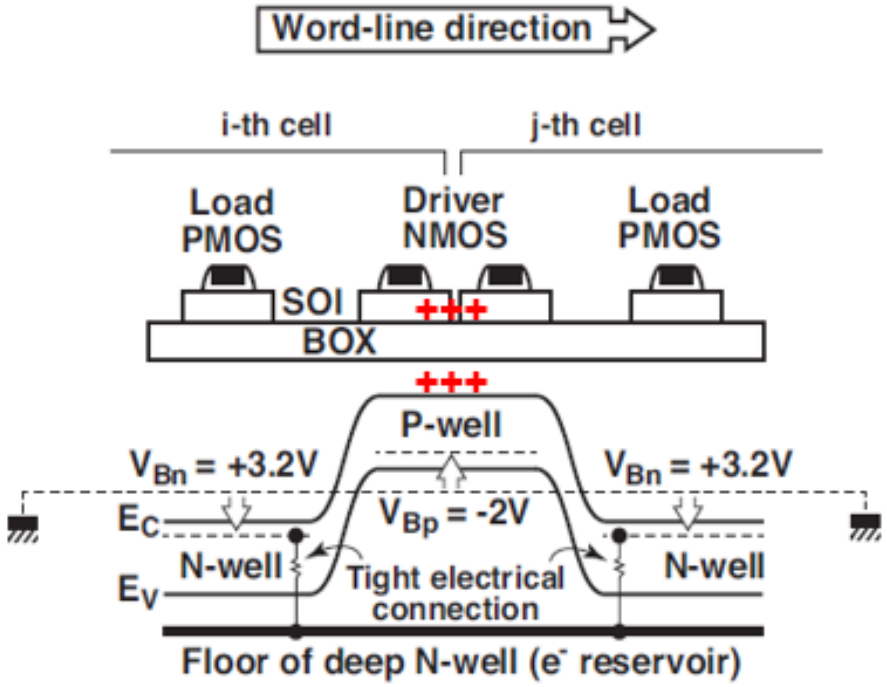

Figure 2.8. Potential diagram of the triple-well structure after an ion strike [16]

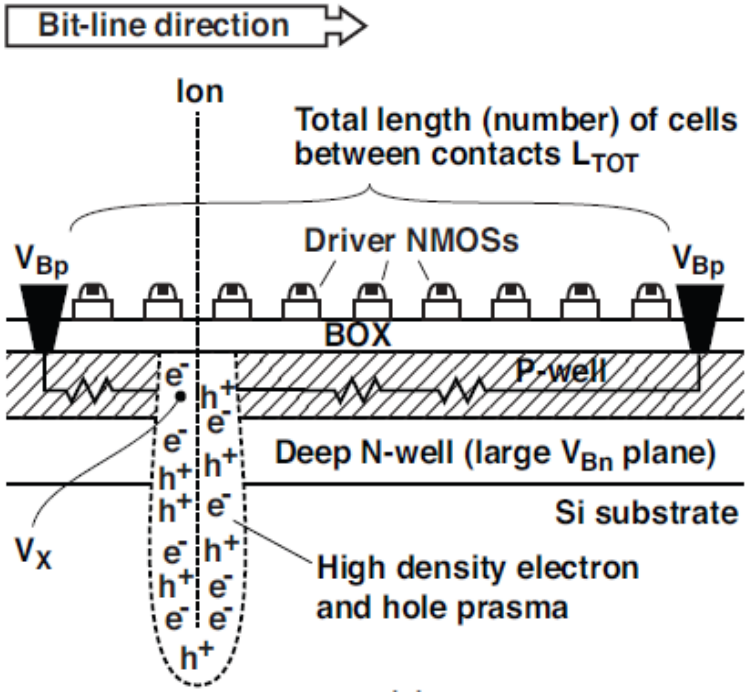

Figure 2.9. Carrier movement path inside the p-well after an ion strike [16].

The noise generated by the ion strike is not just a regional effect. Due to the fact that the p-well stretches along the bit-line, the noise also travels along the bit-line inside the p-well, disrupting multiple transistors on top of the BOX [Fig. 2.9]. This is what causes the line-type MCU. This mechanism is somehow similar to the bipolar-mode soft error found in bulk devices [27], [28]. The main difference is that, in bipolar-mode soft error, the wells must be directly connected to the transistor to generate soft errors. In the case of SOI device, such direct connection is not required.

The cross section of the device increased by nearly 100 times, due to the line-type MCU, which only takes place when V_B is applied. This trend is opposite to the one discussed in Section 2.4.1 for SOI devices. Soft error sensitivities of devices fabricated with the 65-nm SOI technology from different radiation tests are compared in Fig. 2.10. The sensitivities were normalized because from the heavy ion test measured the cross section, represented by the black dotted data, while the terrestrial neutron test measured SER of the device, which is represented by the white-dotted data [19]. This difference in sensitivity for the same technology is contributed by the different mechanisms of the soft error. However, it also brings out the question why the line-type MCU was only observed in heavy ion test but not in terrestrial neutron test. One possible answer to this question will be presented in Chapter 4.

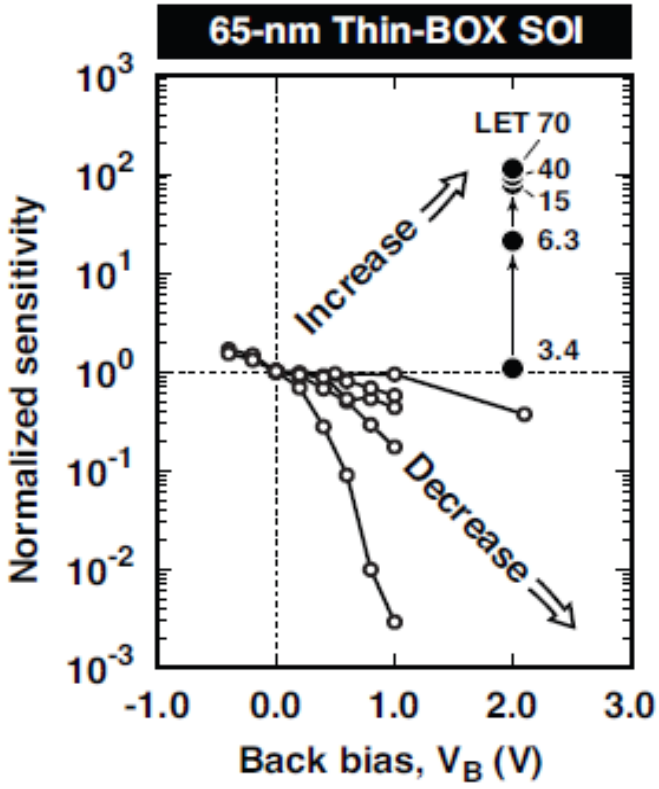

Figure 2.10. Comparison of soft error sensitivity for 65-nm SOI devices measured in different radiation tests [16], [17], [19].

2.5 Evaluation of the Line-Type MCU

To evaluate the line-type MCU, the length the radiation-induced noise can travel must be estimated. Based on Fig. 2.9, a resistance-based model was created to calculate the length of the MCU [29], [30]. The electrostatic potential on the p-well surface at the ion strike position is labeled as $\emptyset_x$. From the strike position to both ends of the p-well column, resistance paths can be drawn [Fig. 2.11]. This is the path the carriers would take: from the highest potential ($\emptyset_x$) to the lowest potential (negatively-biased p-well contacts). Assuming the potential distributes along p-well column linearly, a potential diagram along the p-well column can be created as shown in Fig. 2.12. The maximum length of the line-type MCU can be estimated as:

$$L = \frac{\emptyset_x - \emptyset_c}{\emptyset_x - V_{Bp} - \emptyset_p} L_{TOT}. \tag{2.2}$$

Here L_{TOT} is the total length of the p-well column, $\emptyset_p$ is the potential difference between the intrinsic Fermi energy and the Fermi energy inside the p-well. $\emptyset_c$ is the electrostatic potential of the back-gate threshold for the transistors above the BOX.

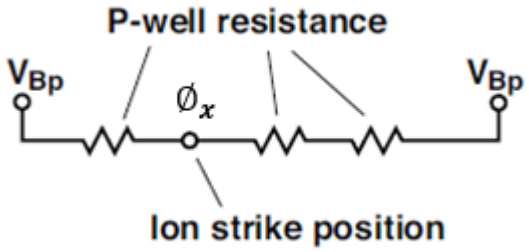

Figure 2.11. Resistance diagram built based on Fig. 2.9 [15].

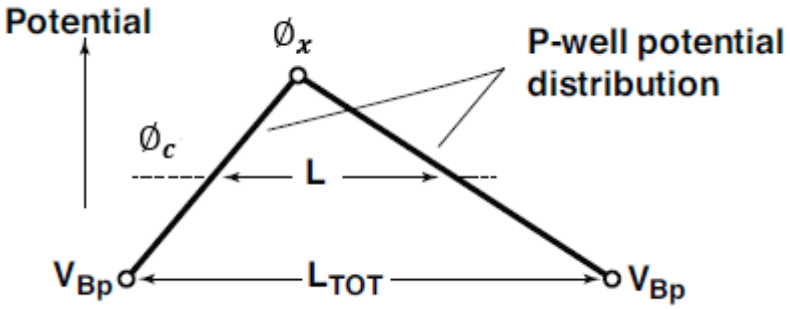

Figure 2.12. Potential distribution inside the p-well [16].

The previously established model uses a static expression for a dynamic phenomenon that is the line-type MCU. As long as the evaluation of the line type MCU is concerned, the static expression is sufficient. However, two aspects of the model was not discussed thoroughly in the previous work: the value and duration of the noise.

This work defines τ_L as the duration during which $\emptyset_x$ is higher than $\emptyset_c$. Only when τ_L is longer than τ_0, the response time of the latches above the BOX, can line-type MCUs be generated. Before Chapter 6, for the calculation of *L*, the effect of τ_L is ignored for simplicity, so that the effect from $\emptyset_x$, which is the key discussion of this work, can be focused. In Chapter 6, the effect of τ_L will be discussed.

From Eq. (2.2), it is evident that $\emptyset_x$ is the key factor that decides the length of the line-type MCU since other parameters are constants for a specific device at a specific bias. In Ref [16] it is assumed that under high LET, $\emptyset_x$ would saturate to the value of $\emptyset_{Bn}$ + V_F, where V_F is the forward bias. It is widely believed that after an ion strike, the junction temporarily exhibits a forward bias characteristic [31] – [34]. However accurate the assumption may be, it cannot reflect the influence of LET and device parameters. Both should affect the length of the line-type MCU. The former was already observed as shown in Fig. 1.6, where the device sensitivity increased with higher LET [16].

To fully evaluate the line-type MCU, a more complex model is required for $\emptyset_x$, so that it can be expressed as a function of various parameters. First the physics and carrier dynamics must be investigated, so that a more complete model can be built. The proposed model is presented in Chapter 3.

2.6 Conclusion

In this chapter, basics of radiation and soft error were introduced, followed by soft error observed in devices of different technology. For FD SOI device, the soft error mechanism cab be classified into two categories: above and below the BOX.

The recently discovered line-type MCU originates from the radiation-induced noise below the BOX. It increases the device soft error sensitivity significantly. While the basic mechanism behind the line-type MCU phenomenon has been made clear, there is still great room for improvement. To fully evaluate the phenomenon, the physics behind the radiation-induced noise must be investigated.

Chapter 3 Radiation Effects on the Depletion Region

3.1 Overview

In this chapter, the effects of radiation on the junction's depletion region is investigated. The investigation leads to a development of a resistance model for the ion track. Using this model, carrier movement can be explained, and the path of current flow can be drawn. The corresponding resistance along the current path helps to evaluate the value of noise under the BOX. A quasi-static model is developed based on the resistance path, which helps to evaluate the peak value of the noise under the BOX. This model contains several parameters that effect the value of the noise, and they are discussed and verified individually in the following chapters.

Preliminary verification of the proposed models was done by simulation and presented in this chapter.

3.2 Redistribution of the Junction Electric Field

It is widely known that radiation-induced EHPs can interact with the depletion region and cause a redistribution of the electric field inside [Fig. 3.1]. It is because originally, the depletion region is formed by the separation of the carriers on both side of the junction, thus the formation of the built-in electric field. The concentration of radiation-induced EHPs at the time of creation significantly higher than the density of the carriers separated in the depletion region. The potential withheld by the depletion region before the ion strike is then released and rearranged along the ion track.

Due to the redistribution of the electric field, the movement of the carriers are no longer restricted by the junction and can cross the junction. Along the ion track, the carriers rapidly drift according to the newly formed electric field. This phenomenon is called the field funneling effect [35] - [40]. At the same time, the EHPs also diffuse laterally away from the ion track or dissipate through recombination. As a result, the carrier density along the ion track drops, and eventually the depletion region will be restored to its original state.

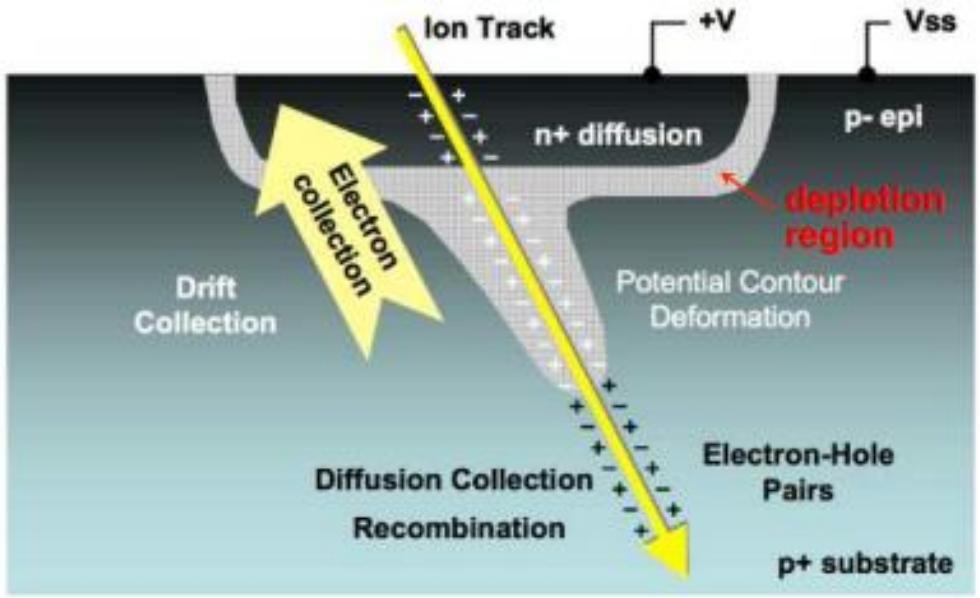

Figure 3.1. Conceptual drawing showing charge collection by the funneling effect [37]

3.3 Theoretical Ion Track Resistance Model

Several works have used the conception of high resistance region (HRR) and low resistance region (LRR) for radiation study [41], [42]. These regions along the ion track are identified by observing the electric field profile. In a similar manner, this work characterizes the ion track at the junction region as a resistance, R_{ion}, but only this part of the ion track is defined specifically. Also, different from previous works, this work aims to provide a mathematical expression for the resistance. How the carriers generated by the ion affects the resistance is the physics proposed by this work. The proposed theoretical R_{ion} is not a constant value and largely depends on the amount of EHPs originally induced by the ion. Fig. 3.2 shows a schematic drawing of R_{ion} inside the junction. It is located across the junction along the ion track connected to the bottom of the p-well and the top of the deep n-well. How mobile the carriers become after the ion strike across the junction is represented using R_{ion}. The lower the R_{ion}, the more freedom of movement the carriers gain.

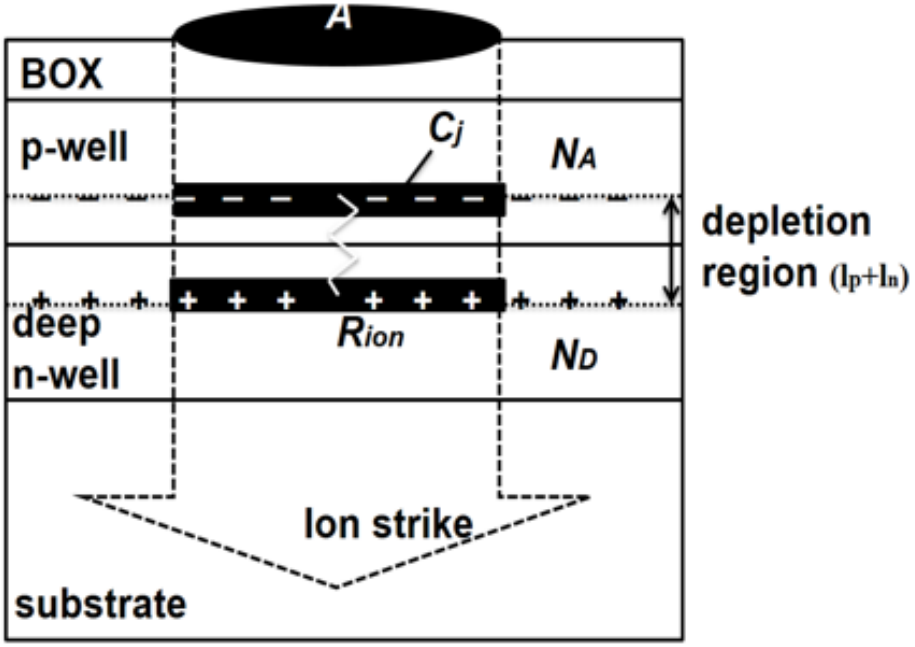

Figure. 3.2. Schematic drawing showing the junction and the proposed R_{ion}.

When the linear energy transfer (LET) of the ion is high enough and the density of the generated EHPs surpasses that of the fixed charges inside the depletion region, the potential difference across the junction becomes negligibly small, meaning R_{ion} is reduced to 0 [Fig. 3.3]. This relation is expressed as [43]:

$$Q_{crit} = \left(N_D l_n + N_A l_p\right) \times A, \tag{3.1}$$

Here Q_{crit} is defined as the critical amount of ion-generated charges required to surpass the fixed charges inside the depletion region, N_D and N_A are the doping concentration in the n-region and p-region of the junction, respectively, l_n and l_p are the depletion width at the n-region and p-region of the junction, respectively, and A is the area of the EHPs cloud generated by the ion. While the size of the EHPs cloud can be determined from the Gaussian distribution as a function of time [Fig. 3.4], to determine the size of the depletion region affected by the EHPs, our static model requires a value for easy comparison between the ion-generated EHPs and Q_{crit}. It has been reported that A is confined by the width of the body (0.5 μm) of the n-p-n structure in a n-type transistor and reaches a stabilized value shortly after the creation of the EHPs, following a Gaussian characteristic [44] [45]. The reported device is a 0.35 μm SOI CMOS transistor. Since the n-p-n structure is similar to the triple-well structure, we will adopt the notion and simply use the width of the well for A for simple comparison.

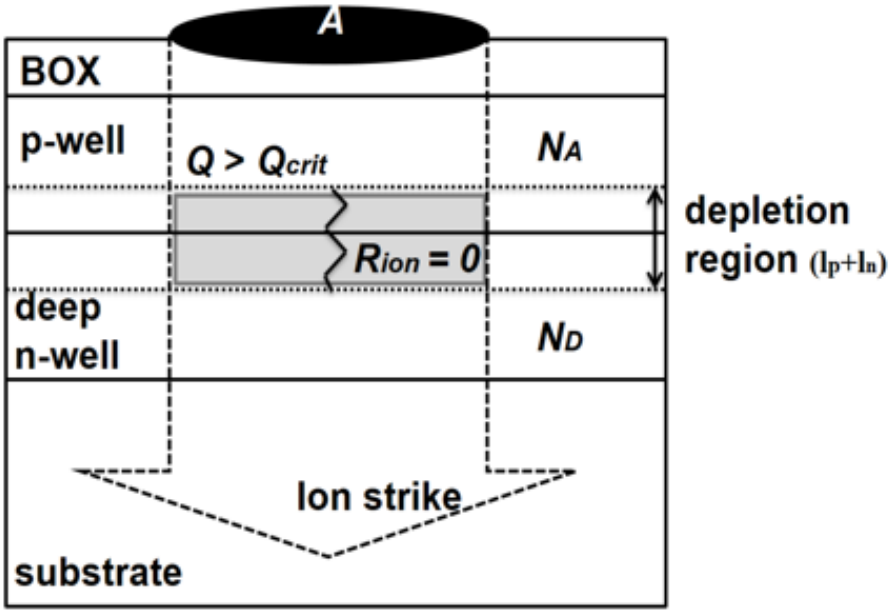

Figure 3.3. Schematic drawing showing the junction and the proposed R_{ion} for $Q > Q_{crit}$.

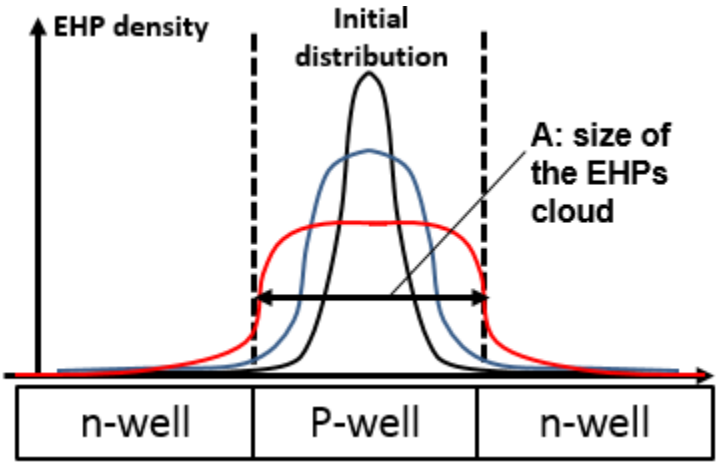

Figure. 3.4. Simplified representation of the size of the EHPs cloud after initial distribution by the ion.

For a device structure with a given junction profile, we can calculate Q_{crit}. This theory implies a threshold of LET above which the carriers experience the least total resistance in their collection path. Consequently, the carrier collection rate increases, and so does the device sensitivity to soft error.

Without the ion-induced EHPs, R_{ion} is close to being infinite since the junction is not crossable due to the built-on electric field. In the presence of the EHPs, the fixed charges forming the depletion region are partially screened, but not enough to reduce R_{ion} to. This scenario is modeled as follows.

Fig. 3.5 shows R_{ion} for $Q < Q_{crit}$. The two regions in black at either end of the junction represents the plates consisted of the fixed charges forming the junction capacitance. Before the ion strike, the carriers forming the junction capacitance, C_j, is expressed as [46]:

$$C_j(V_{bi} + V_R)A = \{\frac{e\epsilon_s N_A N_D (V_{bi}+V_R)}{2(N_A+N_D)}\}^{1/2} A. \tag{3.2}$$

Here e is the quantity of electric charge per carrier, ϵ_s is the permittivity of the semiconductor, V_{bi} is the built-in potential, V_R is the reverse bias applied externally to the junction. The carriers forming the junction capacitance after the EHPs are created by the ion strike is simply assumed to be [43]:

$$C_j(V_{bi} + V_R)A - Q = \{\frac{e\epsilon_s N_A N_D (V_{bi}{}' + V_R)}{2(N_A+N_D)}\}^{1/2} A \tag{3.3}$$

where $V_{bi}{}'$ is the built-in potential after the ion strike and Q is the amount of charges induced by the ion and is the product of the ion LET and the range of the ion inside the junction, r.

Combing Equation (3.1), (3.2), and (3.3), the ratio of the potential across the junction before the ion strike to the one after the ion strike is:

$$\frac{V_{bi}+V_R}{V_{bi}'+V_R} = \{\frac{Q_{crit}}{Q_{crit}-Q}\}^2 \tag{3.4}$$

Assuming after the ion strike, a current, I_{ion}, flows through R_{ion}, an expression for R_{ion} can be made:

$$R_{ion} = \frac{V_{bi}'+V_R}{I_{ion}} = \frac{V_{bi}+V_R}{I_{ion}}\{\frac{Q_{crit}-Q}{Q_{crit}}\}^2 \tag{3.5}$$

Equation (3.5) is applicable when A is stabilized and when $I_{ion} \neq 0$, $Q < Q_{crit}$. When $Q \geq Q_{crit}$, R_{ion} reduces to 0. Since R_{ion} is a function of Q, its value is at the lowest right after the EHPs generation and increases as carriers diffuse out of the A. This lowest value of R_{ion} is implemented for the calculation of maximum $\emptyset_x$, since a lowest R_{ion} results in a largest I_{ion} and a largest potential perturbation inside the p-well.

With the potential across the junction after the ion strike and the current flowing through the junction known, the resistance of the ion track across the junction can be obtained. To obtain the current, the full structure of the triple-well and the carrier movement inside must be considered. This is presented in the next section.

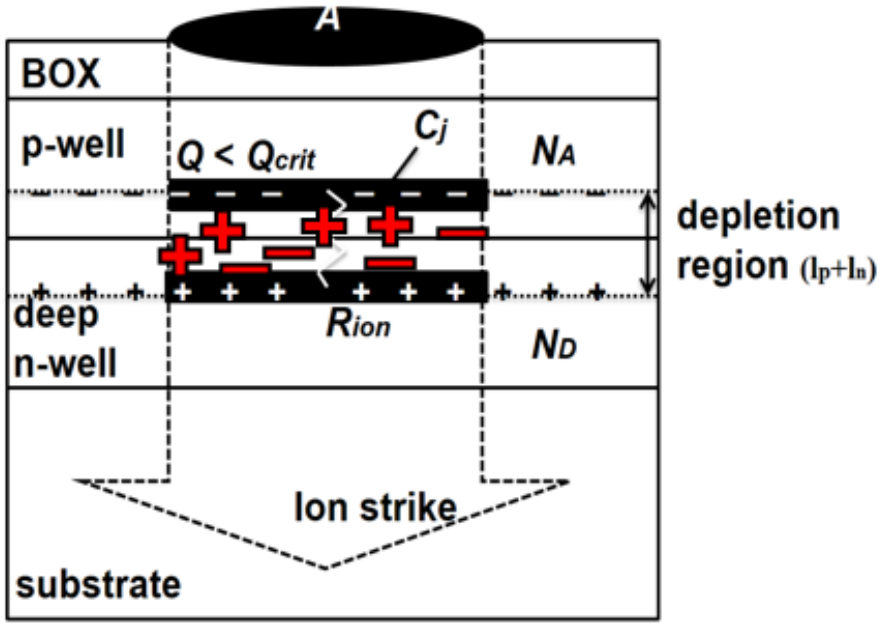

Figure 3.5. Schematic drawing showing the junction and the proposed R_{ion} for $Q < Q_{crit}$.

3.4 Quasi-Static Resistance-Based Model for Evaluation of Noise under the BOX

3.4.1 Carrier Movement

With the concept of the junction between the p-well and the deep n-well along the ion track region functioning temporarily as a passable bridge, the movement of the carriers after the ion strike can be modeled. Fig. 3.6 displays the current flow inside the triple well structure predicted based on the potential distribution inside the triple-well structure. When the device is applied with V_B, the highest potential is established at the n-well contact terminals, while the lowest is at the p-well contact terminals. As soon as the potential barrier at the junction between the p-well and the deep n-well is lowered by the radiation induced EHPs, I_{ion} starts to flow and reaches a stabilized maximum value.

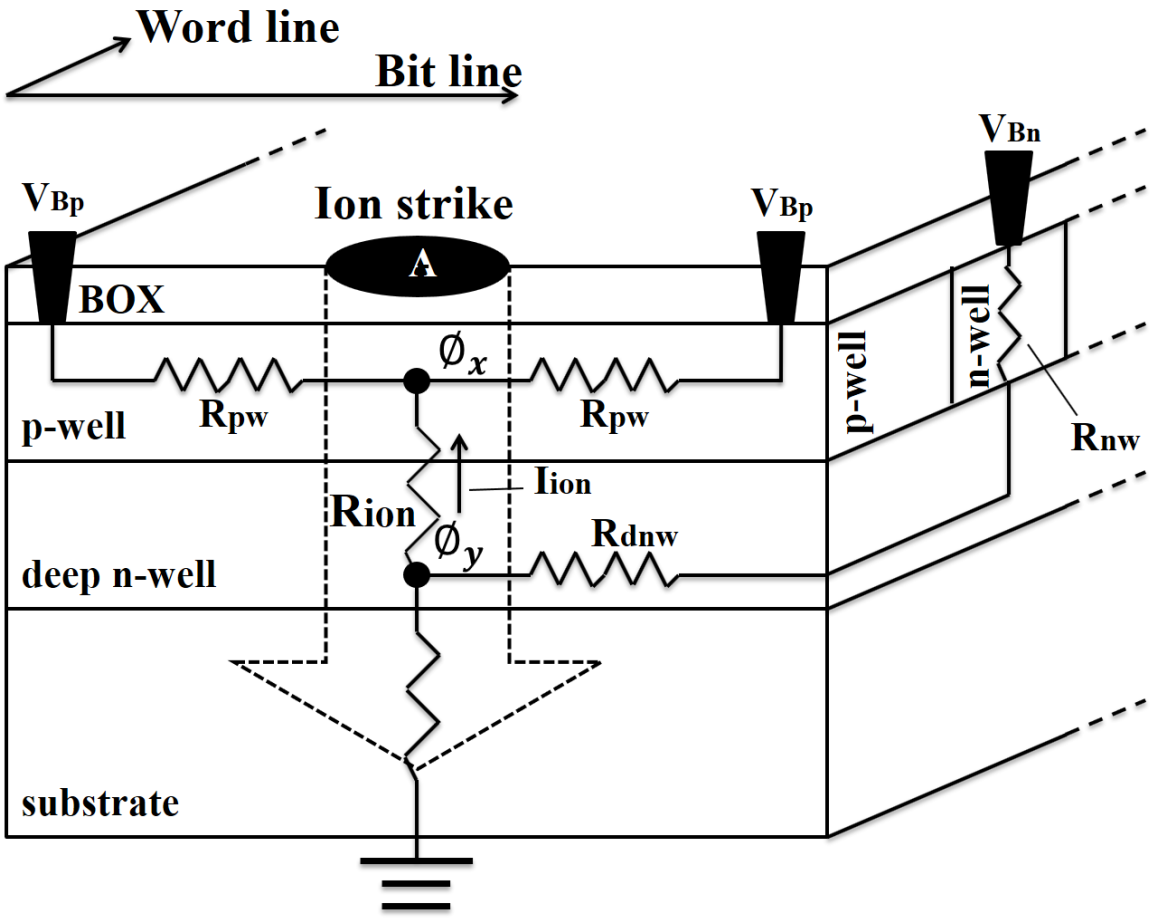

Figure 3.6. Conceptual drawing of the triple-well structure and the predicted current flow after the ion strike [41].

The origin of I_{ion} starts from the contact terminal of the n-well, through the deep n-well and the ion track, then entering either into the p-well, ending at the p-well contact terminal, or the substrate. The resistance of the p-well, n-well and the deep n-well are labeled as R_{pw}, R_{nw}, and R_{dnw}, respectively. Since the resistance of the substrate is significantly larger than the rest of the triple well structure, the current going into the substrate should be negligible. In this study, for the sake of simplicity, vertically, only the upward current component (I_{ion}) flowing into the p-well is considered. When I_{ion} is at maximum ($I_{ion(0)}$), the potential inside the p-well experiences the greatest fluctuation, and so does $\emptyset_x$. According to Equation (2.1), the length of the MCU increases with larger $\emptyset_x$, given that the duration of the fluctuation is long enough for the transistors to respond.

The expression for $I_{ion(0)}$ can be made:

$$I_{ion(0)} = \frac{V_{Bn}+\emptyset_n-V_{Bp}-\emptyset_p}{R_{ion}+R_{pw}+R_{nw}+R_{dnw}}. \tag{3.6}$$

$\emptyset_n$ is the difference between intrinsic Fermi energy and Fermi energy inside the n-well. $I_{ion(0)}$ is obtained when R_{ion} is at minimum. Combining Equation (6) and (7), another expression for R_{ion} is be obtained:

$$R_{ion} = \frac{(Q_{crit}-Q)^2}{2Q_{crit}Q-Q^2}(R_{pw}+R_{nw}+R_{dnw}) \tag{3.7}$$

Equation (3.7) directly connects the value of R_{ion} to Q and the resistances inside the triple-well structure.

3.4.2 Modeling $\emptyset_x$

Based on the flow of I_{ion} shown in Fig. 3.6, first a quasi-static expression for $\emptyset_y$, the potential inside the deep n-well at the lower end of R_{ion}, is expressed as [41]:

$$\emptyset_{y(0)} = V_{Bn} + \emptyset_n - I_{ion(0)} \times (R_{nw} + R_{dnw}) \tag{3.8}$$

This is obtained the during the same time as $I_{ion(0)}$.Then, to evaluate the potential perturbation inside the p-well, a quasi-static expression for $\emptyset_x$ is obtained [47]:

$$\emptyset_{x(0)} = V_{Bp} + \emptyset_p + (\emptyset_y - V_{Bp} - \emptyset_p)\frac{R_{pw}}{R_{pw}+R_{ion}}. \tag{3.9}$$

Equation (3.9) is the main result of the proposed model.

Using Equation (3.7), (3.8), and (3.9), $\emptyset_x$ is modeled as a function of resistance values at each region, the profile of the junction, and Q. They show the adaptability of the proposed model. As long as the bias condition, the doping concentration and the dimensions of the structure are given, the noise under the BOX can be evaluated. As long as the $Q \geq Q_{crit}$, R_{ion} reduces to 0, and $\emptyset_x$ approximately equals to $\emptyset_y$ using Equation (3.9). For the typical case,

as in the previous investigations [16], [17], the doping concentrations in the n-region (n-well and deep n-well) and the p-region (p-well) are about the same, $R_{nw} + R_{dnw} \ll R_{pw}$ since the cross-sectional area of the n-well and the deep n-well in the combined in the bit-line direction is much larger than that of the p-well.. This simplifies the expression for $\emptyset_x$ from Equation (3.7), (3.8), and (3.9) [47]:

$$\emptyset_{x(0)} = \emptyset_{y(0)} = V_{Bn} + \emptyset_n. \tag{3.10}$$

This conclusion is consistent with the assumption in the L model from the previous study. For the case when $Q < Q_{crit}$, the relation is changed to [41]

$$\emptyset_{x(0)} < \emptyset_{y(0)} = V_{Bn} + \emptyset_n \tag{3.11}$$

Equation (3.10) and (3.11) suggest that $\emptyset_x$ is strongly influenced by the Q and would saturate to $V_{Bn} + \emptyset_n$. It should be understood that even though so far $\emptyset_x$ has been described as the potential at a point, its evaluation can be extended to the surrounding region within *A*.

For both cases of $Q \geq Q_{crit}$ and $Q < Q_{crit}$, $\emptyset_x$ is influenced by parameters including the bias value at the n-well and the p-well, the resistance in the p-well, the n-well and the deep n-well, and the LET and the range of the ion. This indicates that the line-type soft error may only take place under certain condition of LET and bias condition, and a countermeasure can be made by altering the resistance inside the triple-well structure.

The value obtained for $\emptyset_{x(0)}$ is the maximum potential perturbation inside the ion-struck p-well at the ion strike position. Even though it is a static model and the potential perturbation fluctuates with time, the value obtained with the proposed model is enough to provide estimation to the length of the line-type soft error using the *L* model, which only requires a maximum value of $\emptyset_x$.

It should be noted that even though Fig. 3.6 shows an ion strike at the center of the p-well, the proposed model is applicable to not just an ion strike at the center of the p-well. For ion strikes at positions other than the center, the carrier movement remains the same, but the value of R_{pw}, R_{nw}, and R_{dnw} will be different. When the ion strike is closer to the end of the wells, their equivalent values increase. However, since they increase at the same time, the effect is minimal to $\emptyset_x$ during calculation. Heavy ion result from previous work also showed that the length of the MCU is not dependent on the strike position [Fig. 1.6]. Therefore, in this work, for simplicity, only ion strike at the center position of the p-well is discussed.

3.5 Simulation

3.5.1 Setup

To investigate the validity of the proposed model, simulation was carried out to examine the carrier movement and potential profile inside the structure, I_{ion}, and $\emptyset_x$ for the investigation of the observed line-type soft error. Fig. 3.7 shows the structure simulated and its dimensions. The dashed arrow represents the ion track. Since the triple-well structure under the BOX layer plays the key role of the line-type soft error, the region above the box as well as the BOX itself was omitted for simplicity, and only the bottom part that includes the triple well structure and the substrate was modeled

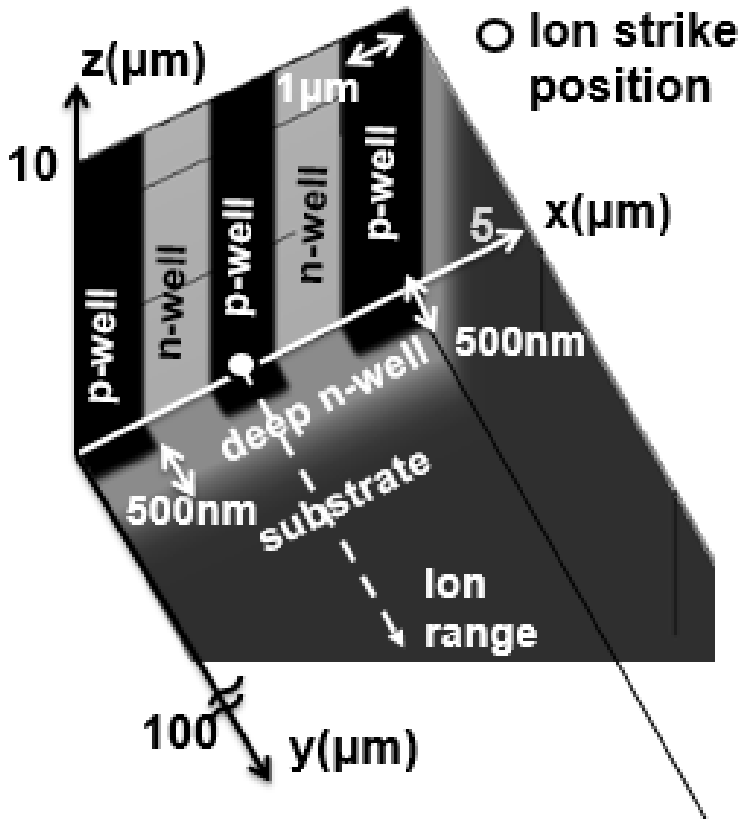

Figure 3.7. Simulated triple-well structure.

Simulation was carried out by HyENEXSS TCAD simulator [47]. For simplicity and the efficiency of simulation runs, only the triple-well structure is modeled in the simulator. Structure on top of the BOX as well as the BOX itself was omitted. A mirrored symmetrical structure was also used to save computing time. Well columns in the pattern of p-n-p-n were embedded inside the deep n-well. The width (x direction) of the well columns was 1 μm and

the length (y direction) was 10 μm. The thickness of the well columns and the deep n-well was 0.5 μm each. The substrate thickness was 100 μm. While the thickness of the substrate may differ from one design to another, in the current study of soft error, it is a rather irrelevant factor. The p-wells had a constant doping profile with $1x10^{18}$ cm^{-3} B, while the n-wells and deep n-well had $1x10^{18}$ cm^{-3} As. As for the substrate, the constant doping profile was $5x10^{15}cm^{-3}$. These values were chosen based on previous works [7], [16]. [17], [48], [49], [50].

The structure received a V_B = 2-V: V_{Bn} = 3.2V, V_{Bp} = -2 V, and the substrate was grounded. The well columns were biased at the end of each well columns (y = 0 μm, z = 10 μm). This bias condition represents the one used in the heavy ion experiment where the line-type MCU was discovered [16], [17].

The ion strike took place at the position of (x = 2.5 μm, y = 0 μm, z = 0 μm), the center on top of the p-well. The ion track length in the literature typically ranges from 1 μm to 100 μm [16], [17], [51], [52]. Therefore 10 μm was chosen as a representative value (unless otherwise noted). The ion strike position was chosen to achieve a symmetrical condition to save computational time and memory. The ion hit at a vertical angle and deposited EHPs following the Gaussian distribution function, which is used widely in SEU studies [16], [19], [34], [43], [48], [53], [54]. 50 nm was used for its 1/e characteristic width, based on Ref. [16], [19], [43], [48], [53], [54]. For the Gaussian temporal parameters of the peak time, 1 ns was selected, while 5 ps was used for the 1/e characteristic width.

The ion generated charges along the ion track, with a LET of 40 $MeV{\cdot}cm^2/mg$, which is about 0.4 fC/nm inside Si. This value was within the range of the value used in the ion experiment [16], [17]. Another value of LET was used for a representation of secondary ions generated by terrestrial neutrons: 3 $MeV{\cdot}cm^2/mg$ [43]. A detail study of the effect of LET on $\emptyset_x$ is presented in Chapter 4. Physic models for charge generation (except from the ion strike) and recombination were turned off in the simulator to reduce computation time, because for the case of present study, the result was almost identical when they were present. Band gaps were set at constant while the carrier mobility values were affected by doping densities only. For the carrier transport equation, this study solved the drift-diffusion transport equations and did not use hydrodynamics and heat transport equations.

3.5.2 Result

First, the size of *A* is checked to see if our assumption of using the width of the well for *A* is reasonable. Fig. 3.8 and Fig. 3.9 shows the electron and hole density along (y = 0.25 μm, z = 0 μm), respectively for an ion strike with LET = 40 MeV·cm^2/mg. The width of *A* was kept at around 1 μm shortly after the EHPs generation at 1.040 ns. Both the electron and hole density surpassed the doping concentration in the p-well (1x10^{18} cm^{-3}) after the ion strike until t = 1.2 ns. Before t = 1.2 ns, the condition for Q_{crit} in Equation (3.1) was satisfied, and R_{ion} was reduced to 0. The Q_{crit} obtained using this value of *A* together with Equation (3.1) is about 0.02 pC. Since the length of the ion track covered the whole depletion region, *r* equals to the width of the depletion region (0.126 μm based on calculation). The corresponding LET is 16 MeV·cm^2/mg to acquire Q_{crit}. This means that the LET used in the simulation represents the case for $Q > Q_{crut}$.

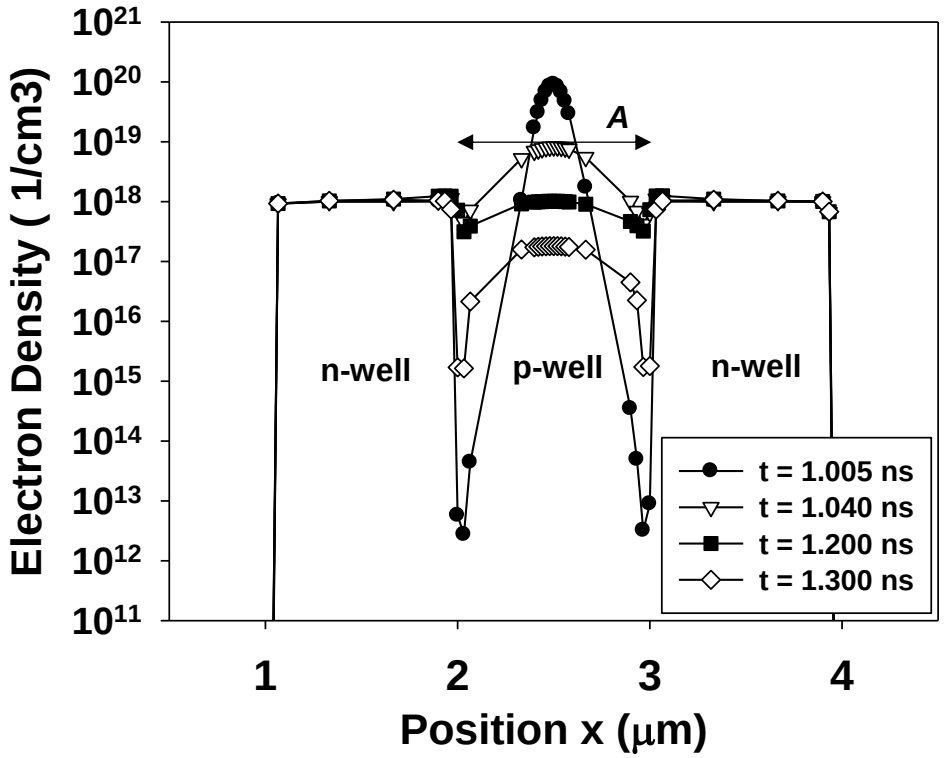

Figure 3.8. Electron density along y = 0.25 μm, z = 0 μm at various times for LET = 40 MeV ·cm^2/mg.

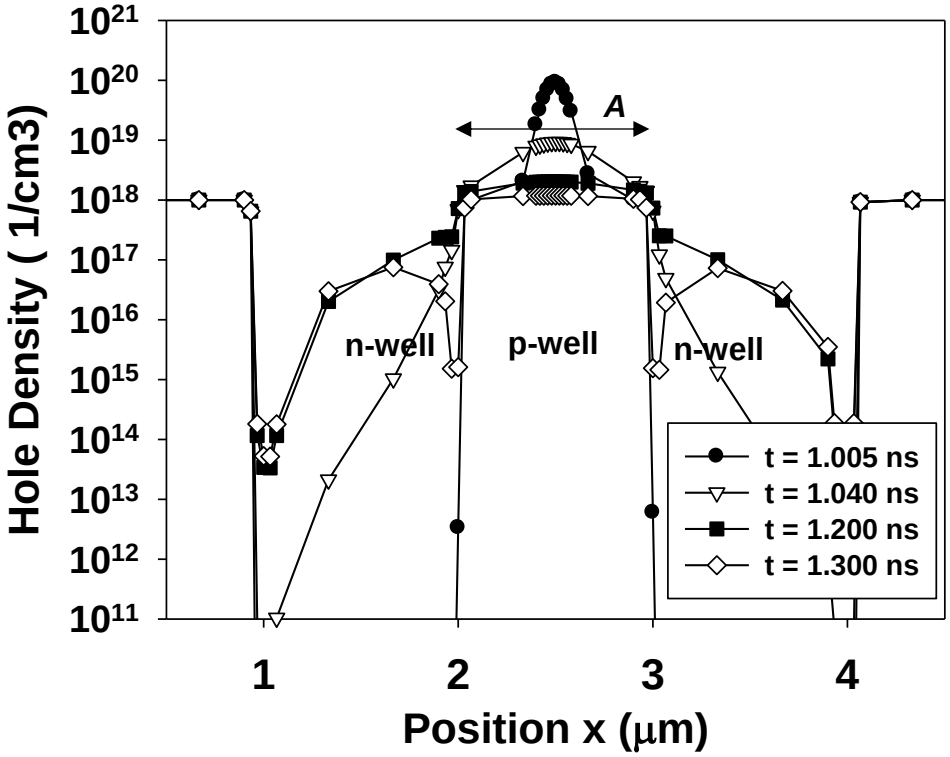

Figure 3.9. Hole density along y = 0.25 μm, z = 0 μm at various times for LET = 40 MeV·cm^2/mg.

Fig. 3.10 and Fig. 3.11 show the electron and hole density along (y = 0.25 μm, z = 0 μm), respectively for an ion strike with LET = 3 MeV·cm^2/mg. The width of *A* was also kept at around 1 μm shortly after the EHPs generation at 1.040 ns. However, not enough EHPs were generated to cancel out the fixed charges in the depletion region. This is expected since the LET used here is lower than the 16 MeV·cm^2/mg required to achieve Q_{crit}. In this case, R_{ion} was not 0. Using our proposed model, R_{ion} was calculated as 8.5 kΩ for its lowest value at the beginning of a stabilized *A*, around 1.040 ns This value will be used to obtain I_{ion} and $\emptyset_x$.

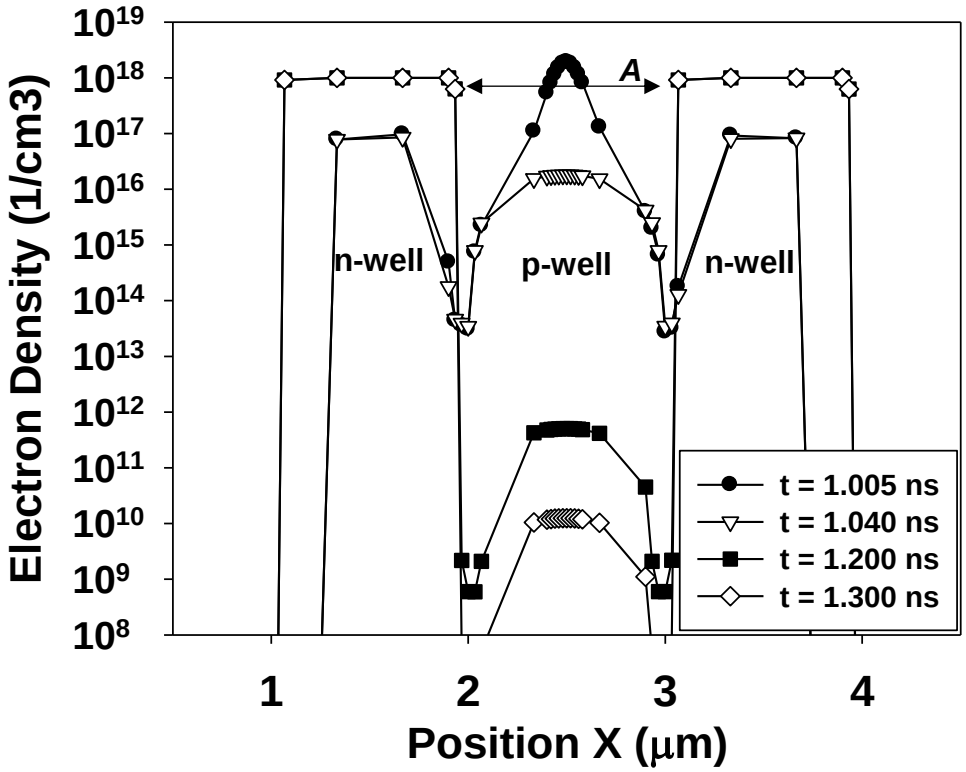

Figure 3.10. Electron density along y = 0.25 μm, z = 0 μm at various times for LET = 3 MeV ·cm^2/mg.

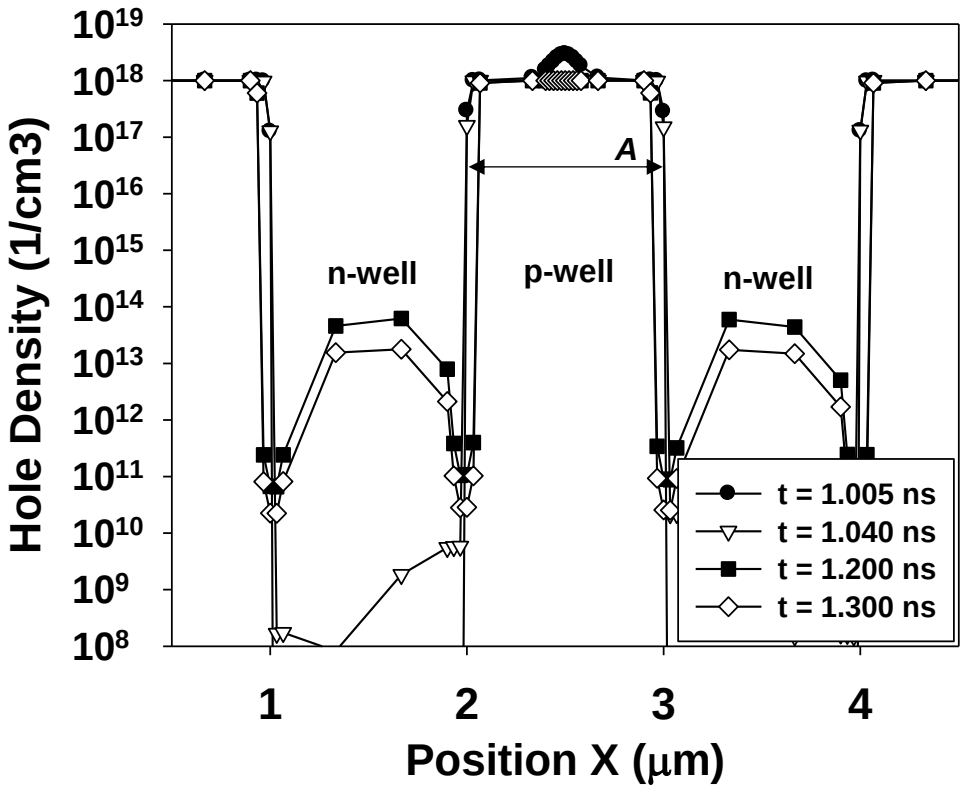

Figure 3.11. Hole density along y = 0.25 μm, z = 0 μm at various times for LET = 3 MeV·cm^2/mg.

Fig. 3.12 shows the potential profile along the ion track from the top of the p-well (2.5 μm, 0 μm, 0 μm) to the bottom of the deep n-well (2.5 μm, 10 μm, 0 μm) at various time points. The LET of the ion strike was 40 MeV·cm^2/mg. At 1 ns, just before the ion strike, the potential difference due to the bias condition was contained by the depletion regions at the interface between the p-well and the deep n-well and that between the deep n-well and the substrate. At 1.001 ns, the potential was redistributed, and carriers started to move vertically into the p-well from the deep n-well ($J_{drift\text{-}up}$) and into the substrate from the deep n-well ($J_{drift\text{-}down}$). The former corresponds to I_{ion}, and the latter is negligible compared to the former in the calculation for $\emptyset_x$. Along the ion track, these currents caused the potential of the deep n-well to drop lower than the initial value before the ion strike and that of the p-well and substrate to rise above the pre-ion-strike values. Due to the size of the deep n-well, sufficient number of carriers inside the deep n-well were able to move and compensate for the initial drop of potential after the ion strike. The potential at the deep n-well is therefore more tolerant to changes caused by the ion. Around 1.2 ns, the potential profile had reached a stabilized state. The result verifies Equation (3.10), showing that along the ion track from $\emptyset_x$ to $\emptyset_y$ the potential is almost uniform and approximately equal to V_{Bn} + $\emptyset_n$, which add up to 3.67 V.

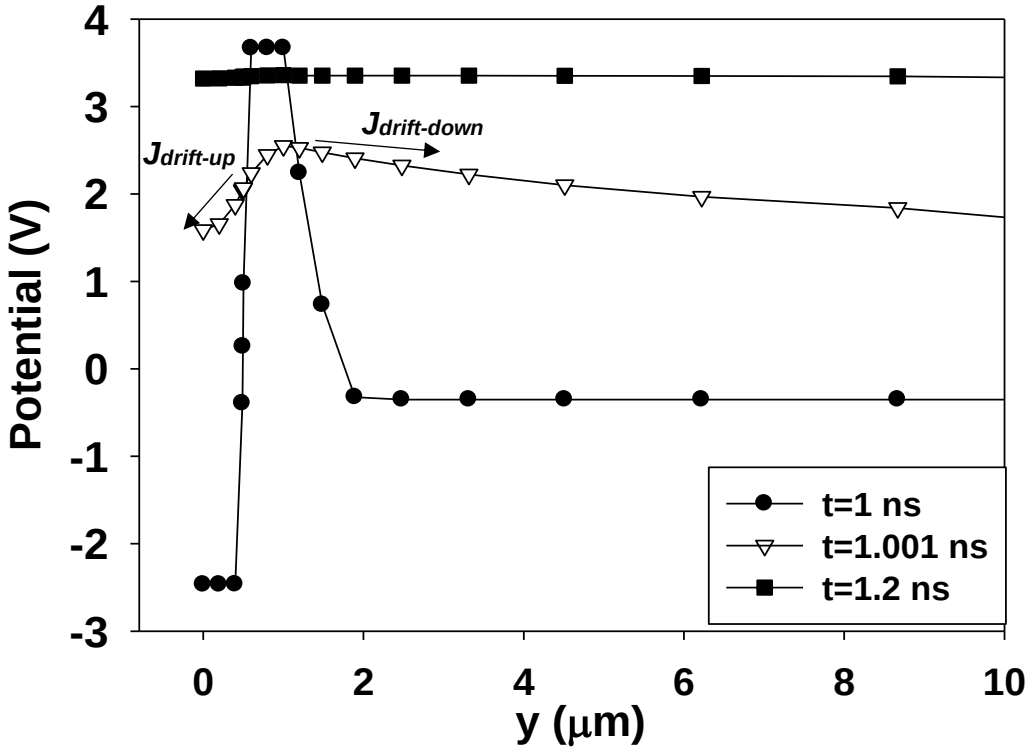

Fig. 3.12. Potential profile along the ion track at 1 ns, 1.001 ns, and 1.2 ns for LET = 40 MeV·cm^2/mg.

The current collected at the ion-struck p-well contact terminal as a function of time is displayed in Fig. 3.13. According to our proposed model, I_{ion} flows vertically upward into the p-well from the deep n-well and is collected at the terminal of the ion-struck p-well. I_{ion} calculated using Equation (3.6) was about 1.4 mA. The values for R_{pw}, R_{nw}, and R_{dnw} were obtained based on their individual dimensions and doping profiles identical to the simulation setup. On the other hand, the current collected by the ion-struck p-well in the simulation was about 1.2 mA, which was close to the prediction. The difference was caused by the small current flowing into the substrate, which was omitted in our model for simplicity. I_{ion} started to decrease around t = 1.2 ns, corresponding to the time when the electron density started to drop below the doping density of p-well, and the requirement to sustain Q_{crit} inside the p-well was lost.

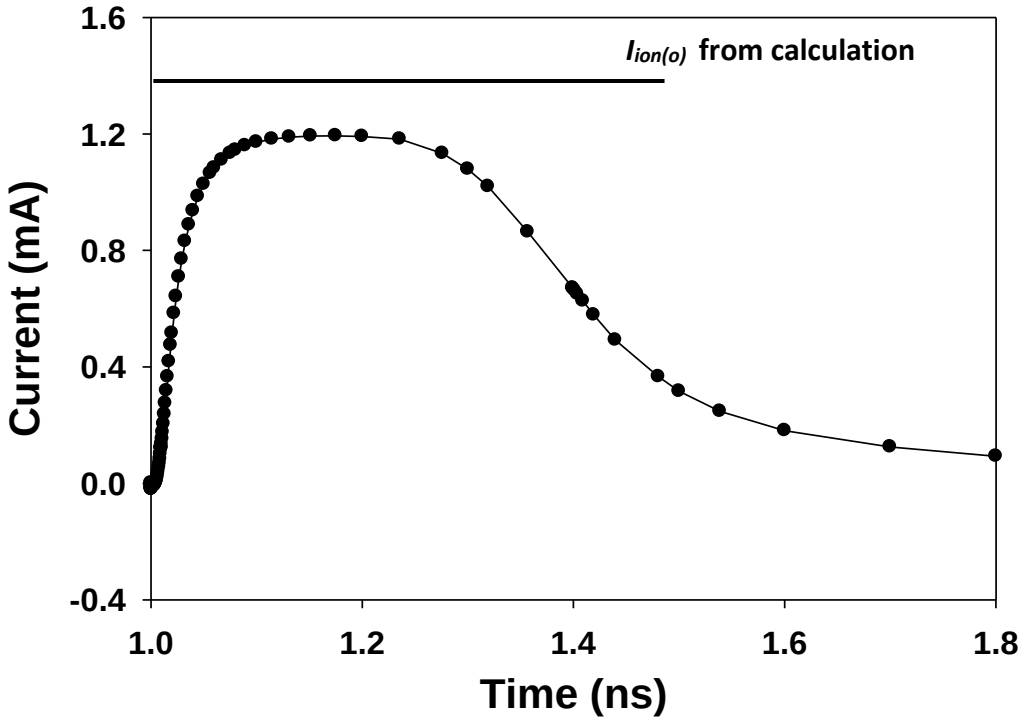

Fig. 3.13. Current collected at the ion-struck p-well contact terminal after the ion strike for LET = 40 MeV·cm^2/mg.

The evolution of $\emptyset_x$ in the time domain is shown in Fig. 3.14. The calculated value using the proposed model is put onto the graph for comparison and agrees well with the simulation result. The duration of $\emptyset_x$ is longer than the typical response time to flip the latches on top of the box (100 ps) [7], as suspected. Inputting the value of $\emptyset_x$ from the simulation as well as the bias condition into (2.2), and assuming $\emptyset_c$ to be 1.8 V as a typical value [16], L is obtained as 7.19 μm, or up to 14~15 upset cells considering a bit height of 0.5 μm. This indicates the information obtained using our proposed model is sufficient in evaluating the line-type soft error. The length of the observed line-type soft error in the ion experiment was about 10 cells or more [16], [17], which is close to what this work predicted. The discrepancy may be caused by V_c, a parameter that depends on one device to another.

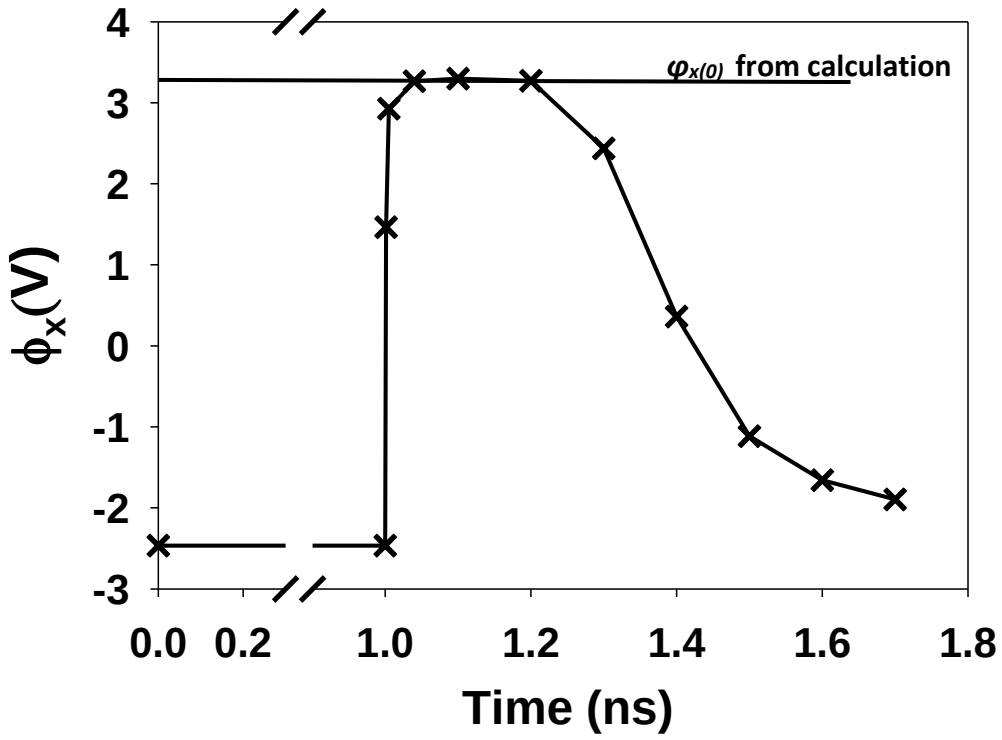

Fig. 3.14. $\emptyset_x$ as a function of time compared with calculated result from the proposed model for LET = 40 MeV·cm^2/mg.

For LET = 3 MeV·cm^2/mg, the current collected at the ion-struck p-well contact terminal as a function of time is displayed in Fig. 3.15. The calculated $I_{ion(0)}$ was about 0.47 mA, which agreed well with the simulation result. The reason for a $I_{ion(0)}$ lower than that in Fig. 3.13 is that R_{ion} was not 0 for LET = 3 MeV·cm^2/mg but 8.5 kΩ at 1.040 ns and increases as carriers diffuse out of *A* with time. Therefore, the plateau-like curve observed in Fig. 3.13 was not present in the low LET case.

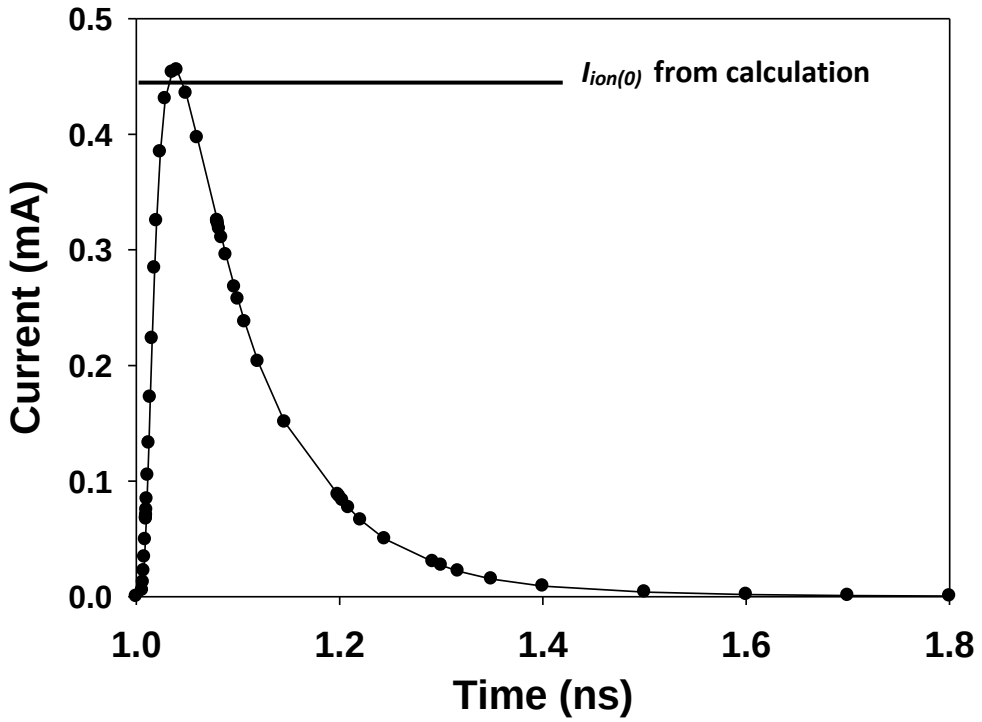

Fig. 3.15. Current collected at the ion-struck p-well contact terminal after the ion strike for LET = 3 MeV·cm^2/mg.

$\emptyset_x$ in the time domain for LET = 3 MeV·cm^2/mg is shown in Fig. 3.16. It should be noted that the value of $\emptyset_x$ here is too low for line-type MCU to occur. Due to a shorter I_{ion}, the curve of $\emptyset_x$ also shortened compared to the high LET case. The calculated value for $\emptyset_{x(0)}$ using the proposed model also agreed well with the simulation result. This indicates that the proposed model can be applied to both high and low LET cases. The proposed model, despite being a static one, agrees well with the simulation result, which is dynamic, because the maximum I_{ion} can be obtained from the minimum R_{ion}, formed shortly after the EHPs generation. This is the physics taking place when the crucial maximum value of $\emptyset_x$ is obtained for the L model.

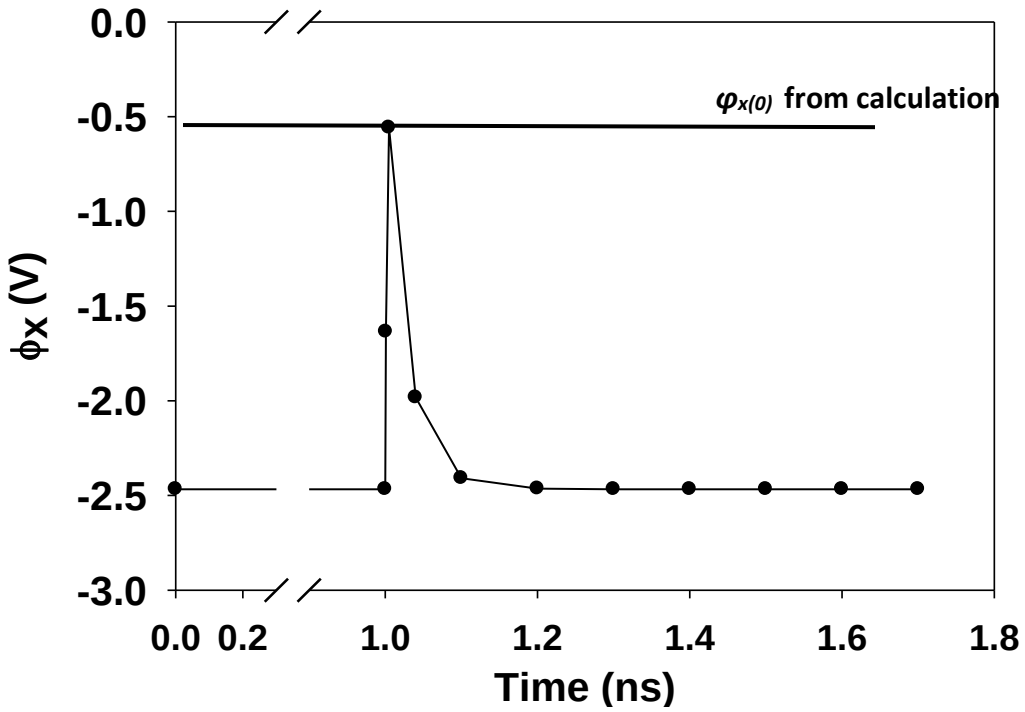

Fig. 3.16. $\emptyset_x$ as a function of time compared with calculated result from the proposed model for LET = 3 MeV·cm^2/mg.

3.6 Conclusion

In this chapter, the physics taking place inside the junction struck by ion was discussed. This work proposed a theoretical resistance-based model to represent a ion-struck junction. Based on this resistance model, an analytical expression for the radiation-induced noise under the BOX could be obtained. The equations from the proposed theoretical analysis provided estimation for the value of the radiation-induced transient current and the noise under the BOX. Theses estimation, however, were only static ones that describe the critical information required to evaluate the line-type MCU. The estimation made in this chapter have been verified by simulation, proving the proposed model has the potential to help in the study of the line-type MCU.

The proposed model contains various parameters including the bias condition, the dimension and doping concentration of each region, and the profile of the ion. These variables must be further analyzed and verified to prove the usefulness of the proposed model. They will be presented in the following chapters individually.

Chapter 4 Radiation Parameters of Radiation-Induced Noise Under the BOX

4.1 Overview

This chapter investigates the effect of radiation parameters, introduced in the previous chapter, on the radiation-induced noised under BOX. It has been observed from previous works that the sensitivity of the thin-BOX SOI device to soft error changes differently according to different radiation sources. It is suspected that the difference is caused by different radiation sources, and the relation between them may be predicted using the proposed theoretical model in Chapter 3.

The prediction will be verified using HyENEXSS simulation, in which the range and LET of the ion are set as variables. The result of the simulation will then be compared with calculated theoretical result. Then Particle and Heavy Ion Transport code System (PHITS) is used to investigate the profile of the secondary ions generated by terrestrial neutrons. The flux and energy of each type of secondary ion, combined with the LET/range table from The Stopping and Range of Ions in Matter (SRIM) help to determine whether the noise under the BOX can be induced in a terrestrial environment.

4.2 Difference in Soft Error Sensitivity between Radiation Sources

In chapter 1, the increment of soft error with increasing ion LET for thin-BOX SOI device observed by previous work was discussed [Fig. 1.7]. The sensitivity response of the device was a strong function of LET and showed a saturated trend when the LET increased. The cross section (cm^2/bit) of the device saturates at around an order of magnitude of -7.

In Fig. 2.10 in Chapter 2, soft error responses of thin-BOX SOI devices measured.in different radiation test performed by previous studies were presented. In the heavy ion test, the soft error sensitivity increased with increasing back-bias, while under terrestrial neutron irradiation, the soft error sensitivity of the same device technology decreased with increasing back-bias, and the line-type MCU phenomenon was not observed.

The above two cases strongly suggested the implication of LET in the soft error sensitivity and the occurrence of the line-type MCU. It is suggested that above certain value of LET, the line-type MCU phenomenon saturates and becomes most severe, and below that value, the occurrence of the line-type MCU rapidly decreases and becomes difficult to be observed. In Chapter 3, the theoretical model proposed for the radiation effect on the junction along the ion track suggested such an idea, and it may have the potential to provide a reasonable explanation to the observed phenomenon.

4.3 Radiation Parameters from Proposed Theoretical Model

4.3.1 Ion LET

In Chapter 3, the ion LET was predicted as a parameter that affects R_{ion} and $\emptyset_{x(0)}$. A plot for $\emptyset_{x(0)}$ can be made as a function of ion LET [Fig. 4.1]. Assuming the ion range is longer than $l_n + l_p$, we can define LET_{crit} as the critical LET required to induce Q_{crit}. When $LET > LET_{crit}$, the proposed theoretical model suggests that $\emptyset_{x(0)}$ saturates to $V_{Bn} + \emptyset_n$, according to Equation (3.10) since R_{ion} has become negligible.

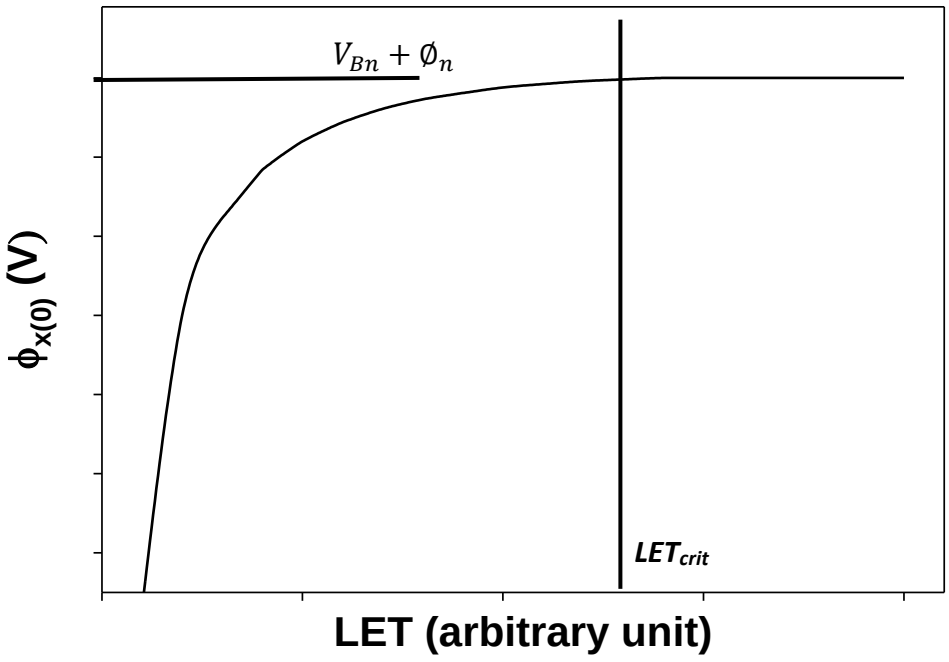

Figure 4.1. Trend of $\emptyset_{x(0)}$ as a function of ion LET predicted by proposed model with a constant ion range longer than the depletion region width.

Figure 4.2 shows a schematic of the memory chip under study. The cross section of the device caused by line-type MCU can be estimated based on the proposed model. For a given $\emptyset_{x(0)}$, the length of the MCU, *L*, can be obtained with Equation (2.2). In a 2M-bit chip, there are 512 memory banks, each having a 64×64-bit array. Assuming each array has an area of *C*, and *N* ions were irradiated on to the array, statistically, half of these ions would hit the p-well and cause the line-type MCU, while the other half would hit the n-well, which result in no MCU. Each ion strike may generate 2 rows of line-type MCU along the bit line [16]. The cross section is expressed as:

$$\sigma\left(\frac{cm^2}{bit}\right) = \frac{upsets(n)}{fluence\left(\frac{n}{cm^2}\right) \times memory\ size(bit)} = \frac{{}^{N}/_{2} \times L \times 2}{{}^{N}/_{C} \times ({}^{2\times 10^6}/_{512})}. \quad (4.1)$$

Considering a typical bit height of 0.5 μm, A can be roughly estimated as 60 μm × 30μm = 1800μm^2. Then from Equation (4.1), $\sigma = 0.92L \times 10^{-8}$cm^2/bit. Here, the cross section is expressed as a function of L, which is a function of ion LET. According to the estimation from the proposed model, when $LET \geq LET_{crit}$, $\emptyset_{x(0)}$ = 3.19 V, and the corresponding L is about 14~15 cells. Therefore, it is predicted that the saturated cross section of the device at high LET is around 1.38×10^{-7}cm^2/bit. When $LET < LET_{crit}$, $\emptyset_{x(0)}$ decreases with LET as discussed previously. In Section 4.4, simulation is carried out to verify this and the cross section obtained from theoretical calculation and simulation will be plotted side by side for comparison.

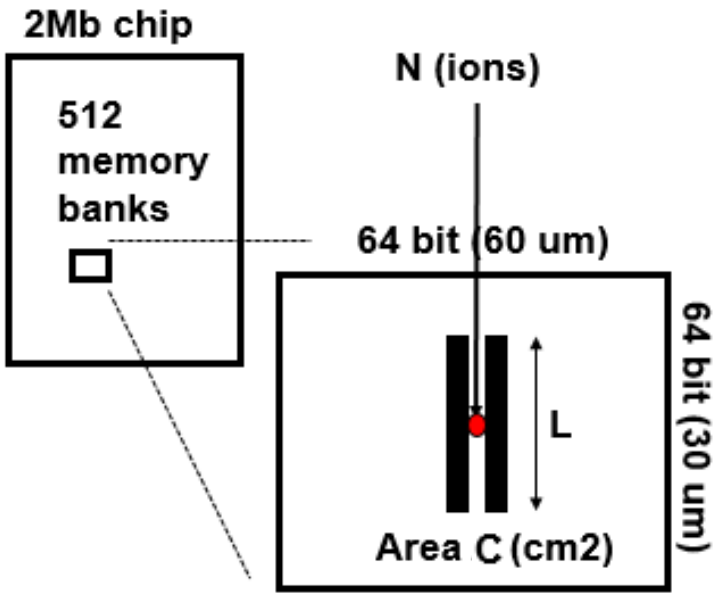

Figure 4.2. Schematic drawing of the memory chip under study for the evaluation of the cross section.

4.3.2 Ion Range

Another factor affecting R_{ion} is the range of the ion inside the junction. In reality, ions can start their track in different regions inside the device, from the passivation to the bottom of the substrate. Also, along a neutron track, secondary ions are generated. These ions start the track anywhere along the neutron track. Therefore, it is reasonable to expect different lengths if ion track inside the triple-well structure. A plot describing this relation is shown in Fig. 4.3. Since the maximum number of EHPs are deposited by the ion when the range of the ion fully occupies the whole junction, the R_{ion} curve saturates when the range is equal or longer to the junction width, so does $\emptyset_{x(0)}$, given that the ion LET remains the same. The response of $\emptyset_{x(0)}$ predict also follow the same trend [Fig. 4.4]. In typical cases, the range of most ion strikes should be much longer than the width of a junction. Therefore, most of the time, considering the effect of ion LET would suffice. However, it is still possible for the beginning or the end of an ion track to partially cover the junction. This study aims to provide evaluation even for the non-typical cases, and with the help of simulation tool, these cases can be examined, and the proposed model may be verified.

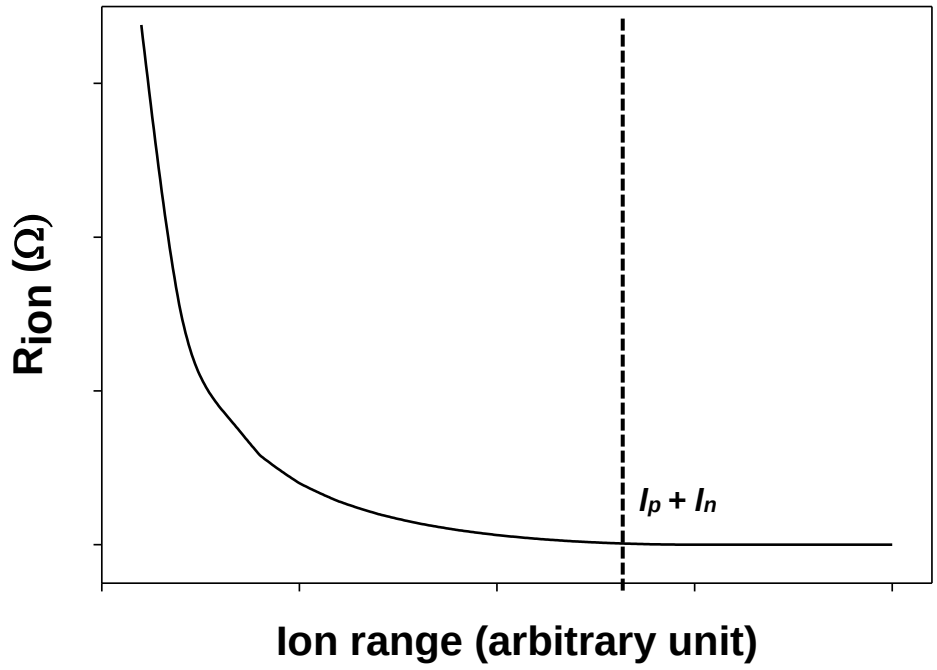

Figure 4.3. Normalized R_{ion} as a function of ion range at constant LET (LET > LET_{crit}).

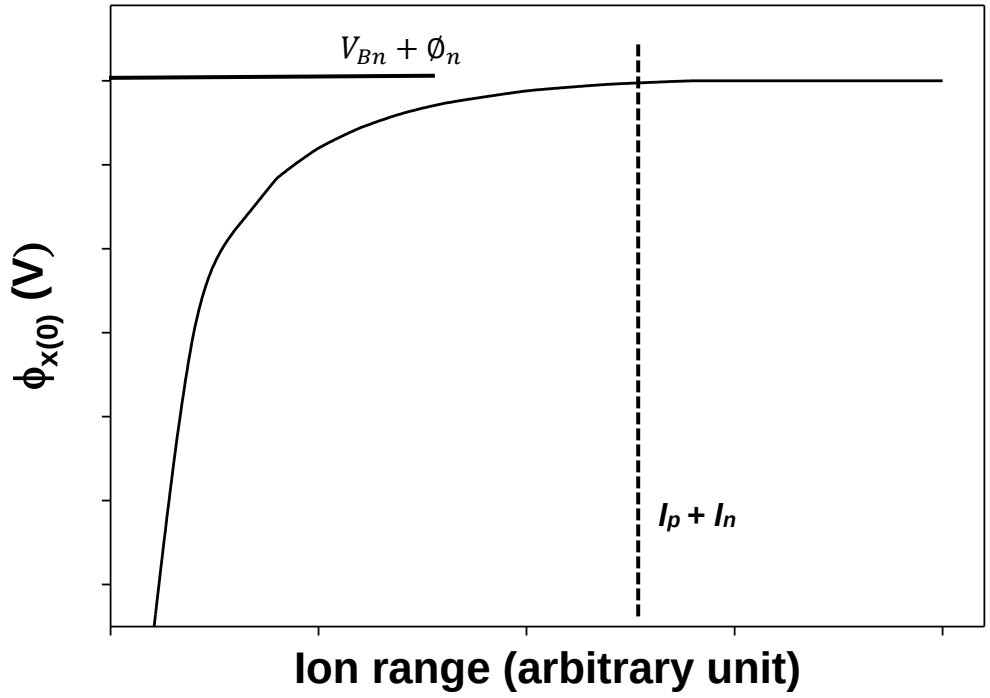

Figure 4.4. Normalized $\emptyset_{x0}$ as a function of ion range at constant LET (LET > LET_{crit}).

4.4 HyENEXSS Simulation

4.4.1 Setup

The dimension, bias condition, and doping concentration of the simulated structure were identical to the setup used in Section 3.5. In this section, only the profile of the ion strike was used as a variable. The ion still took place at 1 ns, generating the same Gaussian- distributed EHPs.

For the study of ion LET dependency, various ion LET were used: 3, 5, 10, 16, 20, 40, and 60 MeV•cm^2/mg. These values were chosen to represent radiation in both terrestrial and space environment. The ion struck the top of the p-well at the center (x = 2.5μm, y = 0 μm, z = 0 μm) with a fixed range of 10 μm vertically. In the following sections, a more detailed look into the LET distribution of the secondary ions generated by terrestrial neutron will take place.

For the ion range study, the ion LET was fixed at 40 MeV•cm^2/mg and was positioned at the top of the center p-well (x = 2.5 μm, y = 0 μm, z = 0 μm). This value of LET wss chosen so that $LET > LET_{crit}$. The range varied from 0.3, 0.5, 0.7, 3, 10, to 30 μm [Fig. 4.5].

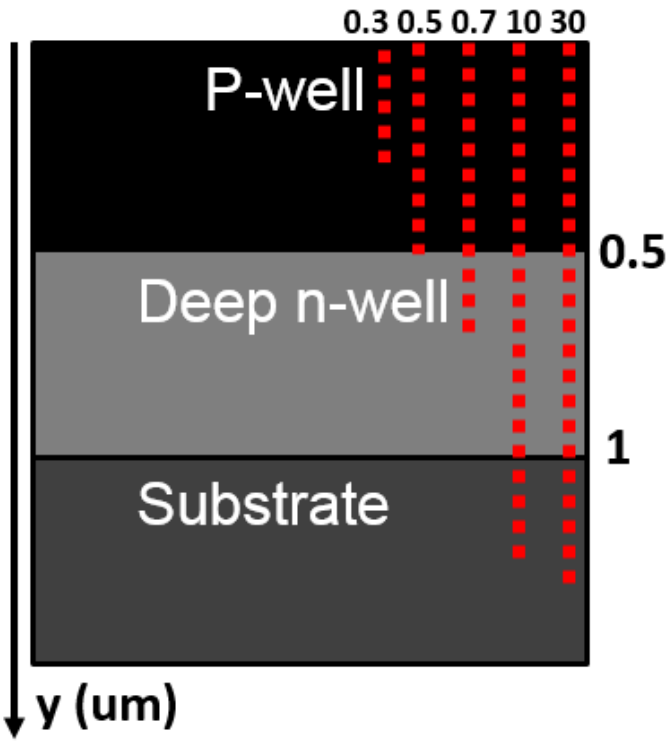

Figure 4.5. Schematic drawing showing the arrangement of the ion track inside the triple-well structure in the simulation (not in scale).

4.4.2 Result

Figure 4.6 shows $\emptyset_{x(0)}$ as a function of ion LET. The simulation result is put side by side with the one calculated from the proposed model. Both follow the similar trend of saturation according to Equation (3.10) when $LET > LET_{crit}$(16 MeV•cm^2/mg from calculation with Equation (3.1)). Some discrepancy was observed in low LET section of the figure. It may be caused by the simplicity of the proposed model for calculating R_{ion} when $LET < LET_{crit}$. However, with the discrepancy within 1 V, it is safe to say the simulation result agrees well with the theoretical one and our proposed model can predict the response of the noise under the BOX as a function of LET.

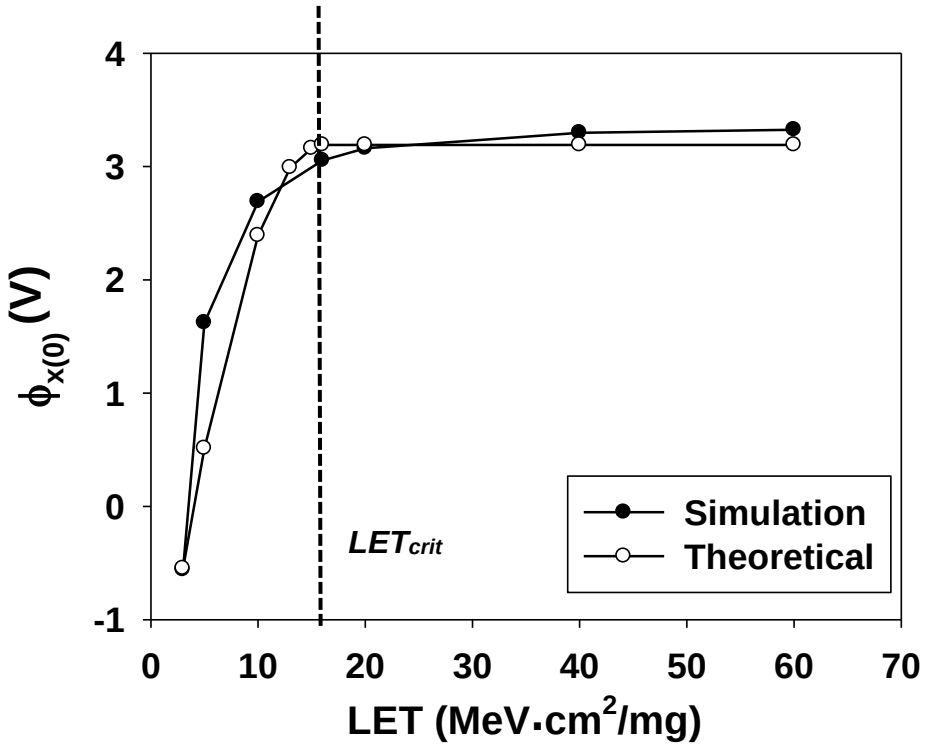

Figure 4.6. $\emptyset_{x(0)}$ as a function of ion LET when ion track range = 10 μm.

The correspond cross section from simulation, theoretical calculation, and experiment measurement [16], [17] are plotted in Fig. 4.7 for comparison. Even though the structure simulated was not based on the actual device tested in the heavy ion test, similar response can still be expected. The goal of the comparison to the experiment test is to examine if a similar trend can be recreated. Both the simulation and the proposed model couldn't characterize the slight increment of cross section in the high LET region. On the other hand, in the low LET region, the measured cross section from the heavy ion test decreased more rapidly than non-experiment results. One possible explanation for the discrepancy is that while calculating L, τ_L was not considered. From Fig. 3.14 and Fig. 3.16, it is evident that for the case with lower LET, τ_L is much shorter than the high LET case. This affects the length of the line-type MCU and hence the device cross section in the low LET region. A detailed analysis into τ_L is done in Chapter 6. Another possible explanation is that the value used for A was still rather simplified in this work, which may cause the discrepancy in both high and low LET regions. However, it is quite evident that there exists a threshold of LET for the device cross section, as predicted by the proposed model.

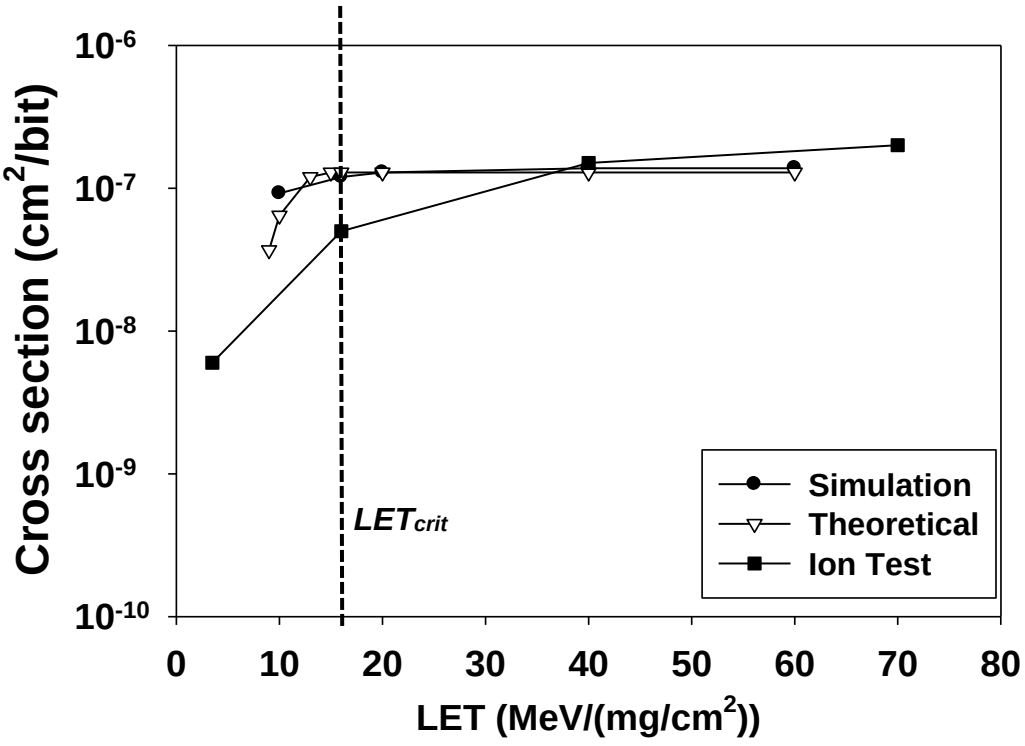

Figure 4.7. Device cross section as a function of ion LET when ion track range = 10 μm.

The result of the ion range's effect on $\emptyset_{x(0)}$ is displayed in Fig. 4.8. Simulation result agrees well with theoretical result. As predicted in the earlier section, due to the changes to R_{ion}, when the range of the ion shortens the noise under the BOX decreases, and as long as the ion track is longer than the junction width, the value of noise under the BOX is independent of the ion range. This is evidence that the length of the MCU has an upper limit regardless of the range of the ion.

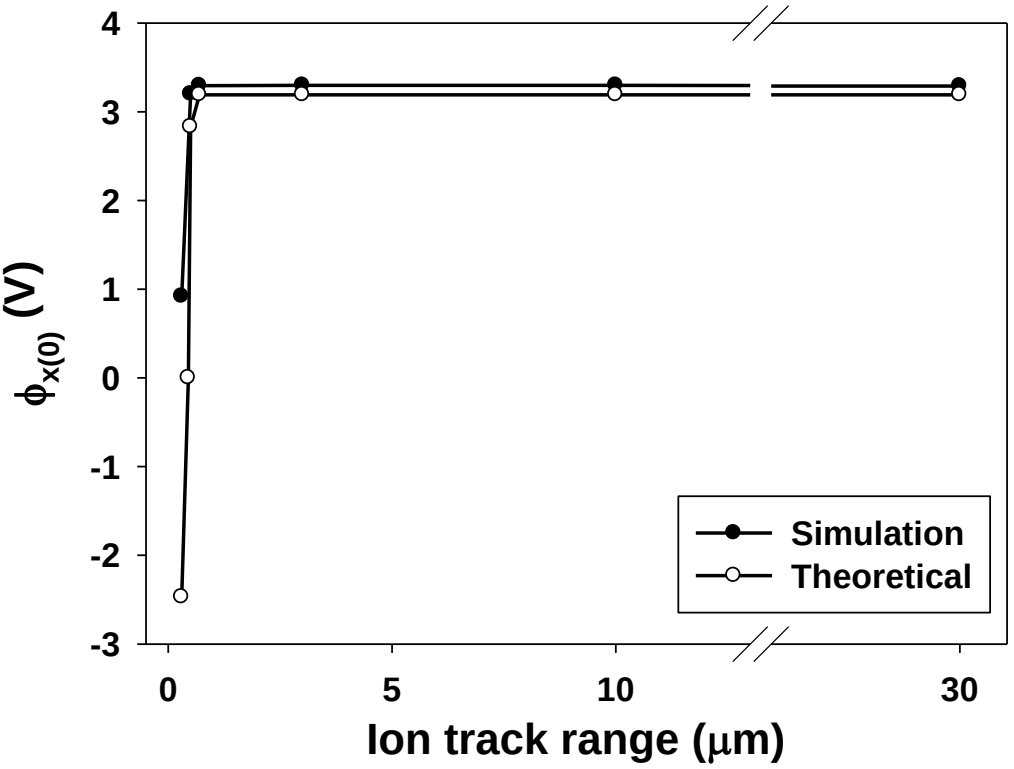

Figure 4.8. $\emptyset_{x(0)}$ as a function of ion track range at 40 MeV•cm^2/mg.

4.5 PHITS Simulation

4.5.1 Setup

In the previous section, it has been discussed that the line-type MCU is influenced by the LET of the ion. While in space, heavy ions with high LET are common and the chance of the occurrence of the line-type MCU is high, in a terrestrial environment, it remains a question if the secondary ions generated by terrestrial neutrons have LET that is high enough to generate line type MCUs. A 0.2 cm by 0.2 cm neutron source was used in the simulation. The spectrum of the terrestrial neutron was obtained from JADECS [55]. The neutron source was located 0.2 cm above a silicon bulk, which has a length, width and height of 0.2 cm. The schematic drawing of the simulation is displayed in Fig. 4.9. Neutrons were irradiated vertically into the silicon bulk, and the type, energy, and yield of the resultant secondary ions were recorded inside the silicon.

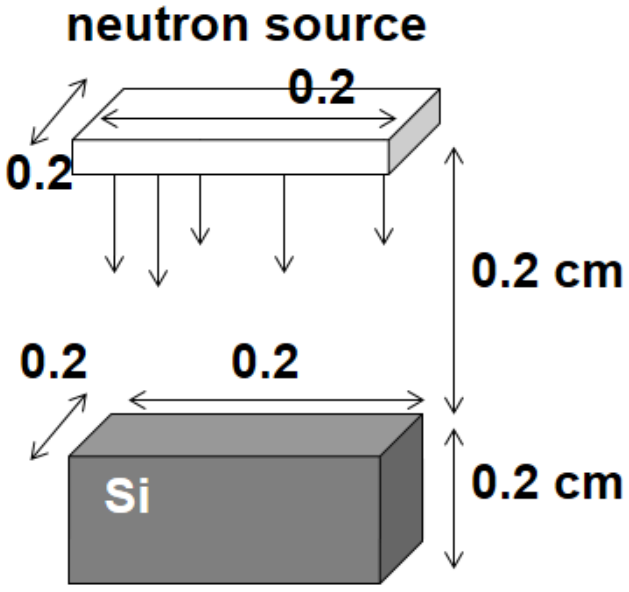

Figure 4.9. Schematic drawing of the simulation setup.

4.5.2 Result

According to previous discussions, the higher the LET, the higher the cross section of the device caused by line-type MCU. Therefore, secondary ions that generate the largest LET are the focus of this study. Here the three heaviest secondary ions were examined: Mg, Al, and Si. The yield vs. energy of each of these types of ions are shown in Fig. 4.10, Fig. 4.11, and Fig. 4.12, respectively.

The majority of these ions have energy between 0.01 to 10 MeV, with the peak of the spectrum located around 0.1 to 1 MeV. Of all the heavier secondary ions, 28 Si has the highest yield. It also generates the highest LET due to its mass. It is reasonable to assume that 28 Si is most possible ion capable of increasing the device SER by generating the line-type MCUs.

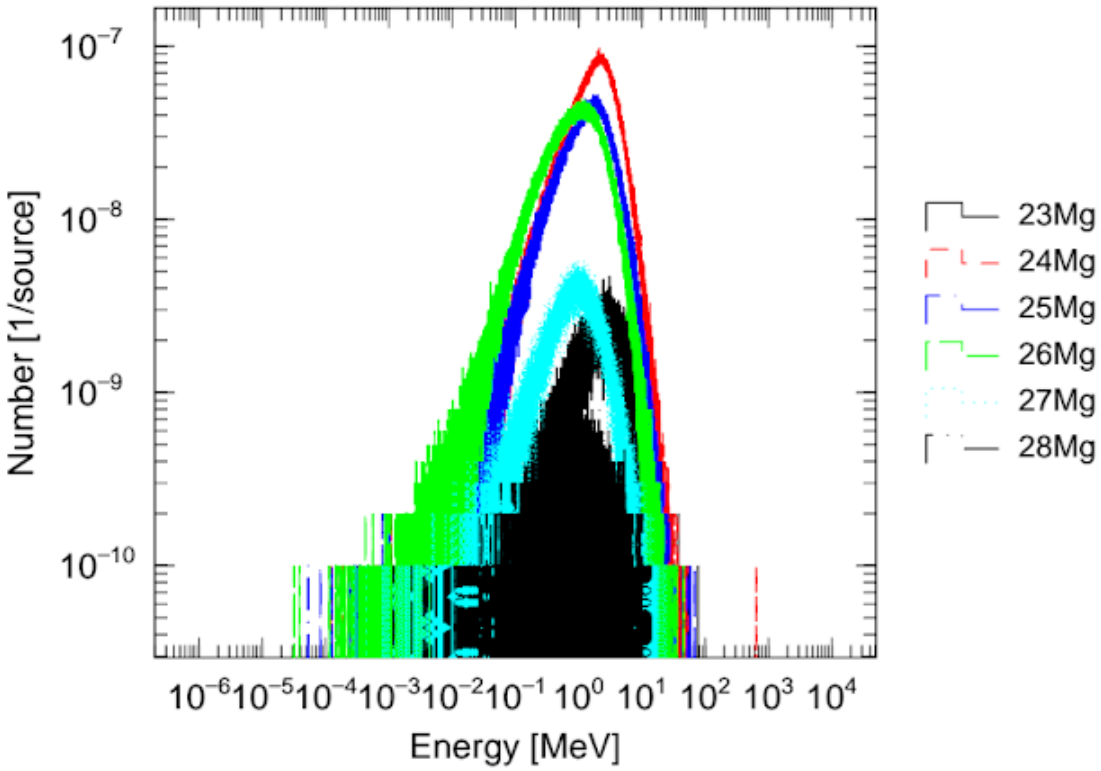

Figure 4.10. Yield vs. ion energy for Mg ions.

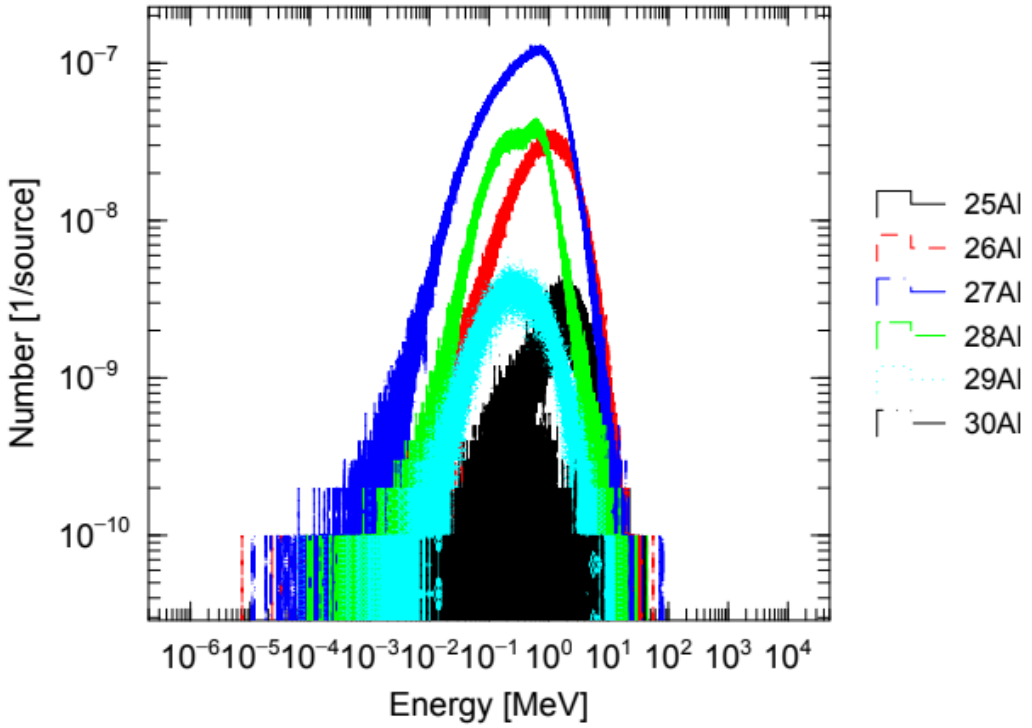

Figure 4.11. Yield vs. ion energy for Al ions.

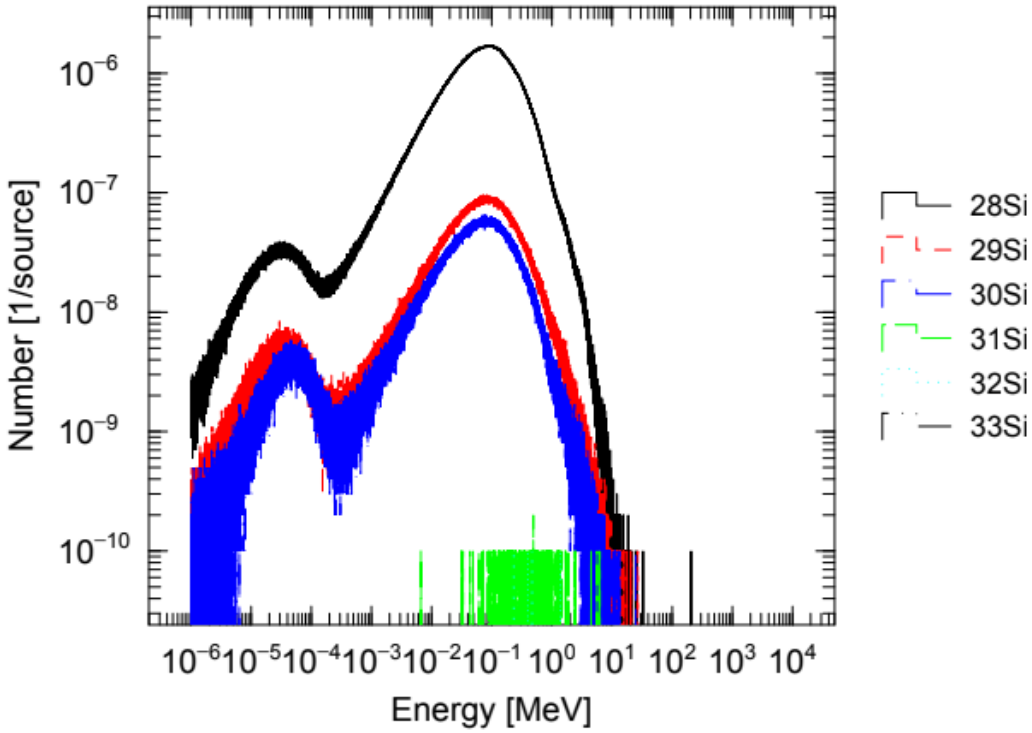

Figure 4.12. Yield vs. ion energy for Si ions.

4.6 SRIM

In the previous section, the energy and yield of the secondary ions generated by terrestrial neutrons were obtained. Here in this section, the goal is to obtain the range and LET of each ions of different energy so the reason behind the absence of the line-type MCU in the terrestrial neutron test [19] can be found. Figure 4.13 shows the data collected from the SRIM table for the secondary ions. The high end of the Si ion spectrum, 28Si with 10 MeV energy is also indicated in the figure. Most of the ions have ranges longer than the width of typical junctions. Also, most have LET lower than 16 MeV•cm^2/mg, even for 28 Si, which produces up to 13 MeV•cm^2/mg. Referencing the LET_{crit} (16 MeV•cm^2/mg) from previous discussions, these ions do not generate enough carriers inside the junction between the p-well and the deep n-well, thus the noise under the BOX is significantly reduced. This is one possible explanation why the line-type MUC was not observed in the terrestrial neutron test.

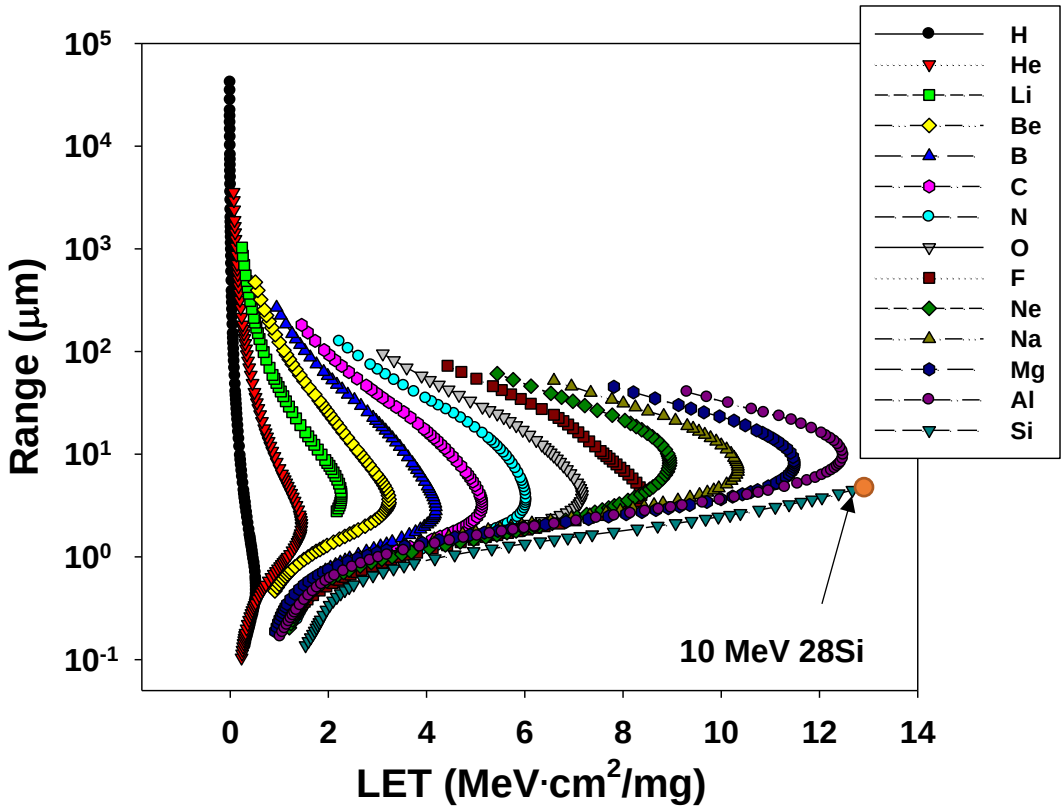

Figure 4.13. Range vs. LET for Si ions from SRIM table.

4.7 Conclusion

In this Chapter, the effect of ion LET on the radiation-induced noise under the BOX was discussed. Proposed model in Chapter 3 helped to predict the response of the noise as well as the cross section of the device as a function of LET. The prediction was compared and verified by simulation. The calculated cross section was also compared with the measured data from the heavy of test of previous work. Some discrepancies exist. Nonetheless, the agreement between the theory and simulation was good enough for the characterization of the noise.

One possible explanation for the different cross section profile of the device between heavy ion test and terrestrial neutron test was proposed. The main reason for the difference was the ion LET. Most secondary ions generated by terrestrial neutrons simply do not generate enough LET to contribute to the noise under the BOX.

Chapter 5 Device Parameters of Radiation-Induced Noise Under the BOX

5.1 Overview

This chapter investigates the effect of device parameters on the radiation-induced noised under BOX. According to the proposed model, resistance at each region and the bias of the device can affect the level of the noise.

The prediction will be verified using HyENEXSS simulation, in which the doping concentration in the p-region and the n-region, as well as the value of back-bias are set as variable. Possible measures to reduce the noise under the BOX and increase the device tolerance against the line-type MCU are also proposed in this chapter.

5.2 Device Parameters from Proposed Theoretical Model

5.2.1 Well Resistance

From Equation (3.8), (3.9), and (3.10), the resistance value of p-well, n-well and deep n-well have a strong impact of the noise under the BOX. Assuming the case when $Q > Q_{crut}$ and R_{ion} becomes 0, $\emptyset_{x(0)} = \emptyset_{y(0)}$. Then the following expression is obtained:

$$\emptyset_{x(0)} = \emptyset_{y(0)} = V_{Bn} + \emptyset_n - (V_{Bn} + \emptyset_n - V_{Bp} - \emptyset_p)\frac{R_{nw}+R_{dnw}}{R_{pw}+R_{nw}+R_{dnw}}. \quad (5.1)$$

Typically, when the doping concentrations inside the p-region and the n-region are close, the ratio of resistance at the end of Equation 5.1 will be reduced to negligibly small, since the size of the n-region is large, making the resistance of the n-region much lower than the p-region. This results in the simplified estimation (3.10). However, when a large difference exists between the doping concentration of the p-region and the n-region, the resistance ratio becomes no longer negligible, and Equation 3.10 becomes:

$$\emptyset_{x(0)} = \emptyset_{y(0)} < V_{Bn} + \emptyset_n, \quad (5.2)$$

indicating that the noise under the BOX now saturates at a lower value which can be obtained from Equation 5.1 and is strongly dependent on the resistance at each region. Fig. 5.1 demonstrates how the ratio of n-region resistance to p-region resistance effects $\emptyset_{x(0)}$. Section 5.3 will verify this prediction be changing the n-region and p-region resistance separately. Simply put, when R_{pw} is much larger than R_{nw} and R_{dnw}, most of the potential drop between V_{Bn} and V_{Bp} will be distributed inside the p-well, making closer to the V_{Bn}.

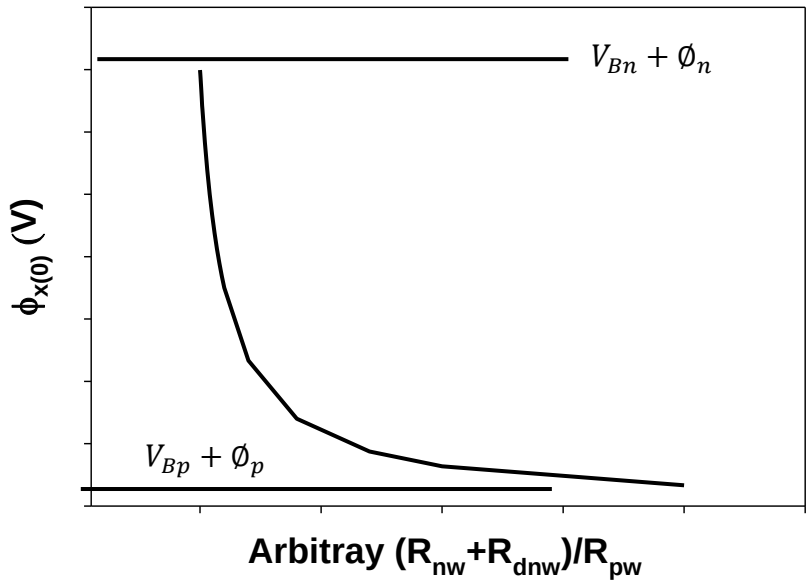

Figure 5.1. Predicted $\emptyset_{x(0)}$ as a function of the ratio between n and p-region resistance.

When the ion $Q < Q_{crit}$, $R_{ion} \neq 0$, and Equation (5.2) becomes:

$$\emptyset_{x(0)} < \emptyset_{y(0)} < V_{Bn} + \emptyset_n. \quad (5.3)$$

Here $\emptyset_{x(0)}$ is obtained from Equation (3.9) without simplification. In Fig. 4.6, it has been shown that when $LET < LET_{crit}$, $\emptyset_{x(0)}$ decreases rapidly, due to the increment of R_{ion}, which becomes greater than the well resistances.

5.2.2 V_B

Equation (3.10) describes the case when R_{ion} becomes 0 and when $(R_{nw} + R_{dnw})/R_{pw}$ is small. Under these circumstances, it is predicted by our proposed model that the noise under the BOX is equal to the bias value at the n-well, which is the back-bias value plus the power supply bias. Various values of V_B will be implement in the simulation to verify this prediction. This investigation helps evaluate how V_B contribute to the noise under the BOX.

5.3.3 Well Width

In the proposed model, our assumption of A in Equation (3.1) is assumed be confined by the width of the p-well. In other words, the width of A is the same as the width of the well. According to Equation (3.1), increasing the width of the well results in a larger Q_{crit}. This means that under the same ion LET, a wider well leads to a larger R_{ion} (if Q becomes lower than Q_{crit}), hence a lower $\emptyset_{x(0)}$. Simulation will be carried out to verify this predicted relation. The investigation is crucial to understanding whether our proposed model can be implemented on other triple-well structure of different dimensions.

5.3 Simulation

5.3.1 Setup

The dimension of the simulated triple-well structure is the same as that used in Section 3.5.1. For the study of well resistance as a variable, several doping concentrations of the p-region and the n-region were simulated: $1x10^{17}$ cm^{-3}, $3x10^{17}$ cm^{-3}, $5x10^{17}$ cm^{-3}, $1x10^{18}$ cm^{-3}, and $3x10^{18}$ cm^{-3}. In each simulation run, either the p-region or the n-region was fixed at $1x10^{18}$ cm^{-3}, while the other region varied from the above values, so that the effect from changing only one of the well resistance can be isolated. The ion track range at strike position were kept the same as that used in Section 3.5.1, except that two values of LET were used: 3 and 40 MeV•cm^2/mg. The former represents the secondary ion generated by terrestrial neutrons [43], and the latter represents heavy ion in space [16], [17]. The purpose is to verify the scenarios with negligible and nonnegligible R_{ion} separately.

For the study of effect from V_B, the doping concentration in both p-region and n-region were kept at $1x10^{18}$ cm^{-3} throughout the study, while V_B changes from 0, 1, 2, to 3 V. The ion track range and strike position were also kept the same as that used in Section 3.5.1.

Finally, to investigate how the width of the well affect $\emptyset_{x(0)}$, the width of the well has been set to various values: 1, 2, and 3 μm. The LET of the ion is 40 MeV•cm^2/mg, while other parameters remains the same as that used in Section 3.5.1.

5.3.2 Result

Simulation results of LET = 40 MeV•cm^2/mg for the study of n-region and p-region doping concentration effect were displayed in Fig. 5.2 and 5.3, respectively. In base cases, the simulation results agreed very well with calculations using the proposed model. The discrepancies were less than 0.2 V. The results show how designers can manipulate the noise under the BOX by simply changing the doping profile of the wells.

For the cases when LET = 3 MeV•cm^2/mg, the trends of the noise under the BOX were very much different than the ones resulted from a 40 MeV•cm^2/mg ion strike, since the ion LET is lower the LET_{crit}. As expected, decreasing the doping of either the n-region or the p-region (higher resistance) made R_{ion} less dominant in determining $\emptyset_{x(0)}$ (Equation (3.6), (3.8), and (3.9)), hence $\emptyset_{x(0)}$ rose [Fig. 5.4, 5.5]. Here the doping concertation in the p-region played a greater role, and decreasing it resulted in a higher increment of $\emptyset_{x(0)}$, compared to decreasing the doping concertation in the n-region. This is because of the relation in Equation (3.9) between $\emptyset_{x(0)}$ and R_{pw}. The discrepancies between simulation and theoretical calculated values were large when n-region doping concentration was decreased. It is speculated that the higher resistance in the n-region made the RC response of the structure slower, and the effect from the ion-induced EHPs may be too fast. In other words, the EHPs already starts to dissipate before $\emptyset_x$ can rise. The different response of $\emptyset_{x(0)}$ between LET 40 and 3 MeV•cm^2/mg is cause by whether R_{ion} is 0.

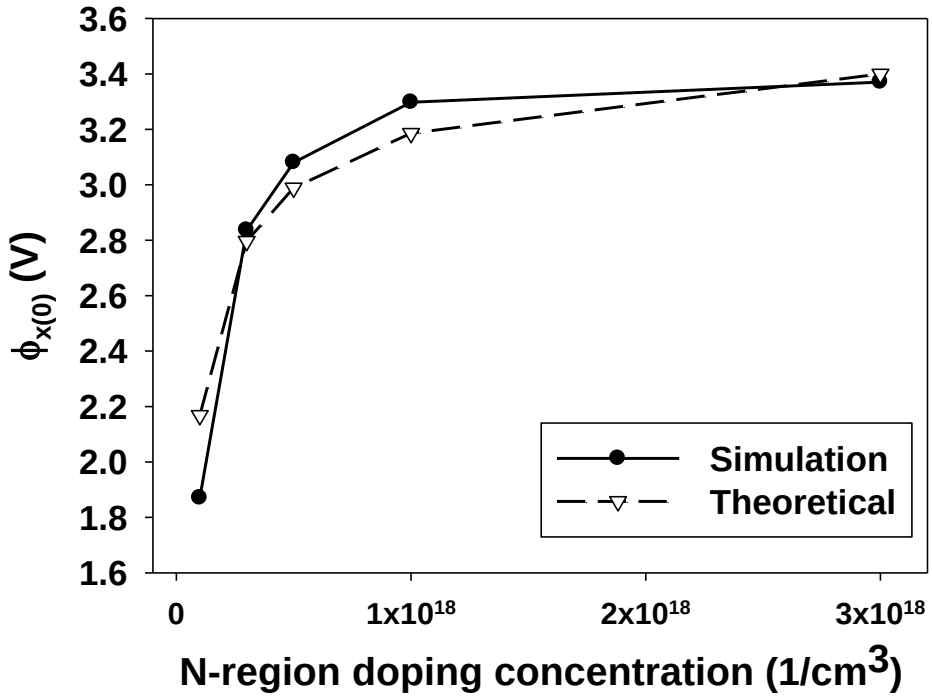

Figure 5.2. $\emptyset_{x(0)}$ as a function of the n-region resistance under a LET of 40 MeV•cm^2/mg.

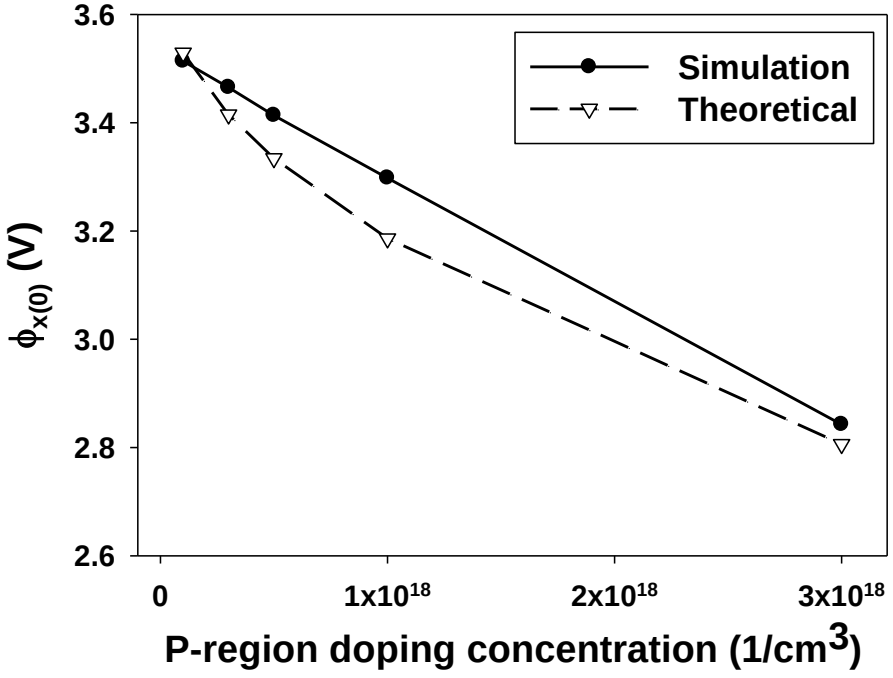

Figure 5.3. $\emptyset_{x(0)}$ as a function of the p-region resistance under a LET of 40 MeV•cm^2/mg.

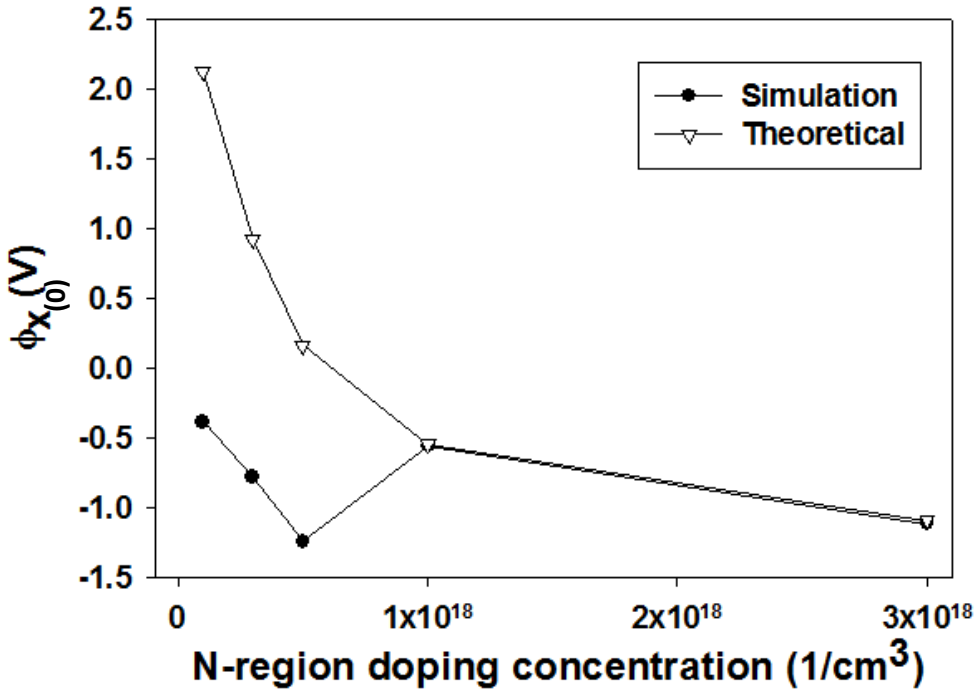

Figure 5.4. $\emptyset_{x(0)}$ as a function of the n-region resistance under a LET of 3 MeV•cm^2/mg.

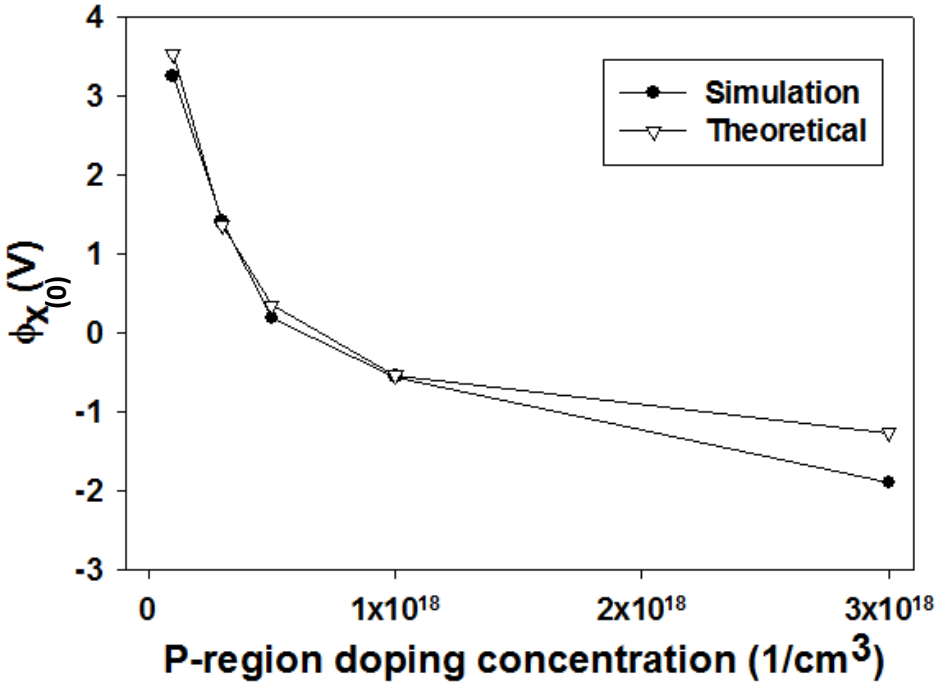

Figure 5.5. $\emptyset_{x(0)}$ as a function of the p-region resistance under a LET of 3 MeV•cm^2/mg.

Figure 5.6 shows the simulation result of $\emptyset_{x(0)}$ for different V_B. The discrepancy between simulation and calculation using the proposed theory was smaller than 0.2 V. This result confirms (3.10) and demonstrate the influence of V_B on $\emptyset_{x(0)}$, which was only partially proven in the heavy ion experiment [16], [17] since only one value for V_B was used.

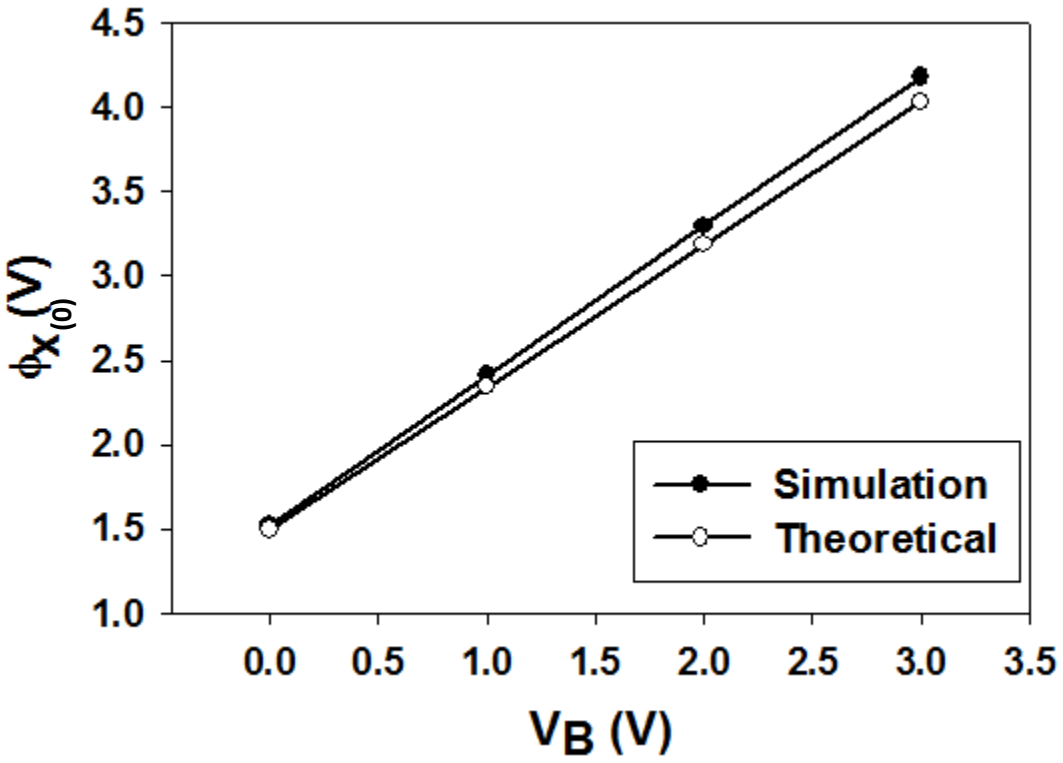

Figure 5.6. $\emptyset_{x(0)}$ as a function of the V_B under a LET of 40 MeV•cm^2/mg.

The effect from changing the width of the well is shown in Fig. 5.7. Qualitatively, the trend of $\emptyset_{x(0)}$ predicted is verified by simulation, despite the discrepancy. The discrepancy becomes larger as the width of the well increases. It is possible that our simplified assumption of *A* being the width of the well does not provide accurate result for structure with larger dimension. However, for smaller dimension, it evident from the trend of the curve that the discrepancy would be smaller. This means that while the *A* requires a better definition for the proposed model to provide accurate result for larger dimension of wells, for smaller dimensions, the current simplified assumption of *A* should work fine. The width of the well is not a flexible parameter since it has to match the width of the cells on top of the BOX. It is reasonable that large variation to the dimension of the well can be expected only when the technology fabricating the device changes. Since the technology of the studied device is a 65 nm FD SOI technology, it is possible that our proposed model is best applicable to a 65 nm process or a possibly a more advanced process with smaller scaling.

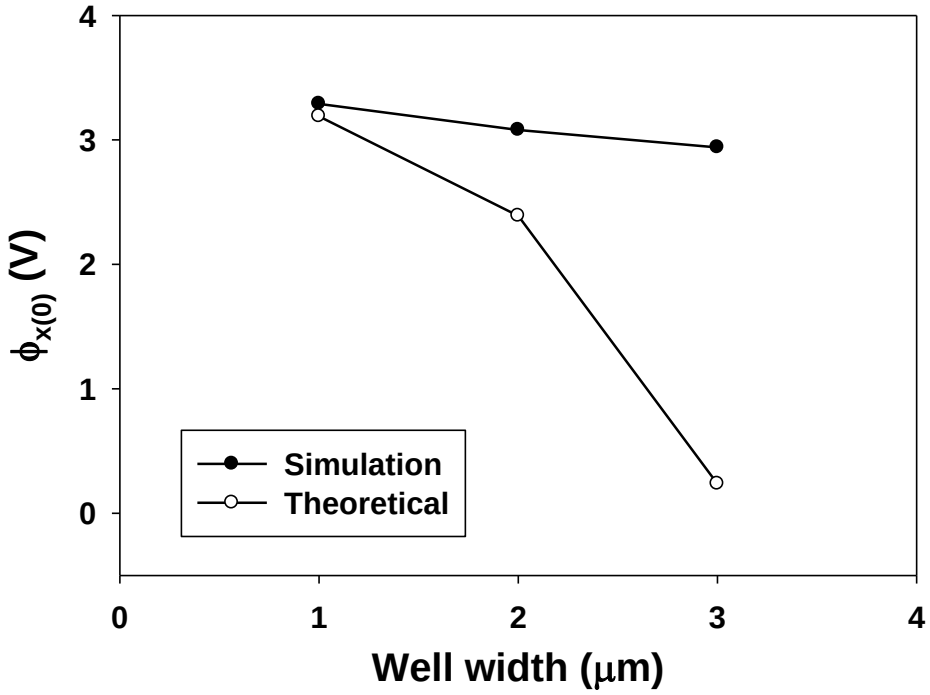

Figure 5.7. $\emptyset_{x(0)}$ as a function of the width of the well under a LET of 40 MeV•cm^2/mg.

5.4 Device Optimization Guidelines based on Device Parameters

From the previous sections, it is known that changing the device parameters allows the manipulation of radiation-induced noise under the BOX. This section provides some guidelines on how to increase the device tolerance against the line-type MCU. Here the discussion will be limited to not changing the characteristics of the transistor, the BOX, and the dimension of the wells.

First, it was already experimentally proven that applying a larger back-bias to the device increases the device sensitivity to line-type MCU. However, the purpose of back-bias is to save static power consumption at the device stand-by mode. Consequently, decreasing the back-bias for the sake of eliminating the line type MCU is not a practical approach.

Simulation and theoretical results from this chapter also showed that under high LET, increasing the ratio $(R_{nw} + R_{dnw})/R_{pw}$ can cause the noise under the BOX to decrease. In this sense, the n-region doping should be made as low as possible and the p-region doping as high as possible. However, this cannot be carried out indefinitely. If the n-region's doping concentration was made too low, punch-through may take place when back-bias is applied. Fig. 5.8 shows the depletion region width inside the n-well as a function of n-region doping calculated using the same setup as the triple-well structure in the simulation with V_B = 2 V. Since the width of the wells are 1 μm, l_n must be shorter than 0.5 μm to avoid punch-through, which sets the limit to how low the n-region doping concertation can be decreased.

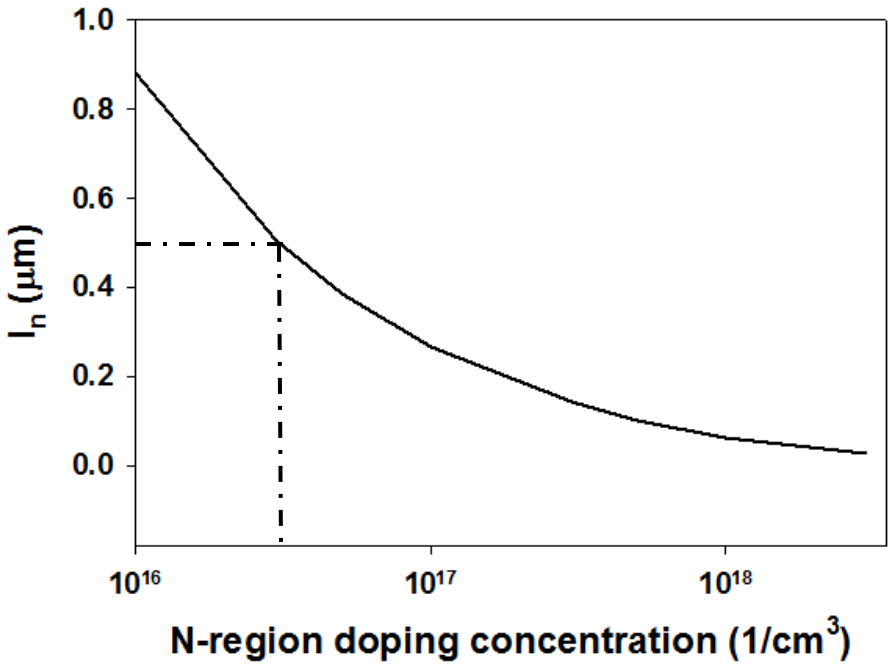

Figure 5.8. Depletion region width inside the n-well as a function of n-region doping under a 2-V back-bias.

Another limitation in changing the doping concentration is that when the LET is low, decreasing both either the p-region and the n-region doping concentration by too much may result in a higher noise under the BOX.

In the case of our study, to reduce the occurrence of the line-type MCU in both high LET and low LET regions, the n-region doping should be kept low but above $5x10^{17}$ cm^{-3}, while the p-region doping should be made as high as possible, within the confine of an efficient manufacturing process. It was also suggested by the simulation result that the p-region doping concentration should be at least 3 times the doping of the n-region. This method ensures the noise under the BOX is kept low at all times without interfering with the rest of the device function.

Table 5.1 shows the simulation result for different combinations of n-region and p-region doping concentration. It is evident that by altering the doping concentration at both regions has a combined effect. Even though $\emptyset_{x(0)}$ is still higher than the assumed $\emptyset_c$ of 1.8 V, a lower $\emptyset_{x(0)}$ shortens *L*, which makes the MCU more likely to be correctable by ECC.

Table 5.1. Simulation result of $\emptyset_x$ for different combinations of n-region and p-region doping concentration

n-region doping	**p-region doping**	$\emptyset_{x(0)}$
$1x10^{18}$ cm^{-3}	**$1x10^{18}$ cm^{-3}**	**3.19 V**
$5x10^{17}$ cm^{-3}	**$1x10^{18}$ cm^{-3}**	**2.8 V**
$1x10^{18}$ cm^{-3}	**$3x10^{18}$ cm^{-3}**	**2.84 V**
$5x10^{17}$ cm^{-3}	**$3x10^{18}$ cm^{-3}**	**2.44 V**

5.4 Conclusion

Device parameters' effects on the radiation-induced noise under the BOX has been discussed. It has been shown that the doping concentration and the back-bias each can affect the level of the noise. Simulation was used to verify the proposed theory and the prediction made based on the device parameters. The discrepancies were small, for most cases.

Using the information obtained, one method to reduce the occurrence of the line-type MCU has been proposed. This method should work in both space and terrestrial environment without interfering with the function of the device.

Chapter 6 Duration of Radiation-Induced Noise Under the BOX

6.1 Overview

In this chapter, the significance of the duration of the noise under the BOX, τ_L, and how it affects the occurrence of the line-type MCU is discussed. Then several parameters that affects the duration of the noise are introduced. These effect from these parameters will be tested using simulation.

Using the information obtained, this study can propose a countermeasure to reduce the line-type MCU.

6.2 Parameters Affecting the Duration of Noise Under the BOX

In Fig. 4.7, discrepancy was observed between device cross section calculated using the proposed model and that measured in the heavy ion test [16], [17]. It is suspected that τ_L becoming shorter as LET is lowered is the cause behind the observed discrepancy.

To evaluate the length of the line-type MCU using (2.1), besides $\emptyset_x$, τ_L is also an important factor, for it has to be long enough for the transistors on top of the BOX to respond to the change of $\emptyset_x$ caused by radiation. Otherwise, regardless of how large $\emptyset_x$ becomes, no line-type MCU would occur. While it is difficult to obtain a direct expression for τ_L or determine what parameters affects it, some clues can be obtained. In Fig. 3.14, a plateau for the curve of $\emptyset_x$ was present due to $R_{ion} = 0$. The plateau started to disappear at t = 1.2 ns, which corresponds to the density of the electrons inside the p-well decreasing below N_A [Fig. 3.8]. According to the proposed model, as long as $Q \geq Q_{crit}$, $R_{ion} = 0$. We therefore define τ_P as the duration of the plateau of $\emptyset_x$, which also correspond to the duration during which $R_{ion} = 0$. A shorter τ_P results in a shorter τ_L.

τ_P should be affected by Q and the escaping speed of the ion-induced EHPs out of A. Assuming the escaping speed of the EHPS is not a function of Q, we can expect a linear relation between τ_P and Q. When the r is longer than the width of the depletion region, τ_P should also be a linear function of LET [Fig. 6.1]. The LET at which τ_P becomes 0 should idealistically be LET_{crit}, since below LET_{crit}, $R_{ion} > 0$.

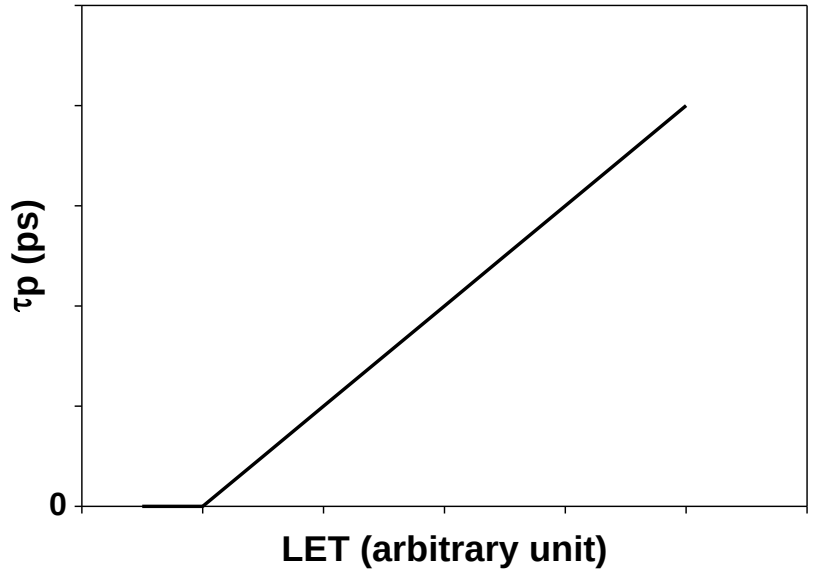

Figure 6.1. τ_P as a function of ion LET for a fixed r based on prediction.

Another factor that affects τ_P is Q_{crit} since Q - Q_{crit} represents the surplus EHPs and determines how long R_{ion} remains 0 at a fixed escaping speed of the EHPs induced by the ion. According to Equation (3.1), Q_{crit} is influenced by many factors: A, N_A, N_D, l_p, and l_n.

l_p, and l_n are both proportional to $(V_{bi} + V_B)^{1/2}$. Therefore, increasing V_B results in a shorter τ_P. The relation is shown in Fig. 6.2. The effect from changing the doping concentration at the junction is more difficult to present with a simple relation since it modifies both N_A (or N_D), l_n, and l_p at the same time. However, we can expect τ_P to decrease when either N_A or N_D increases.

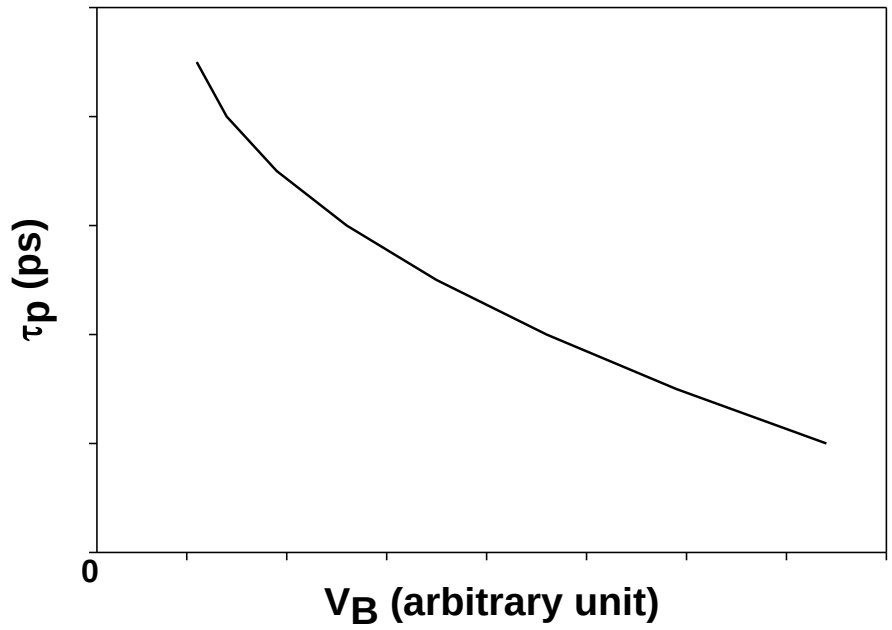

Figure 6.2 τ_P as a function of V_B based on prediction.

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6.3 Simulation

6.3.1 Setup

Various parameters have been discussed that affect τ_P, which is suspected to share the same response to these parameters as τ_L. Using the HyENEXSS TCAD simulation, both τ_P and τ_L are investigated to verify our predictions. Here $\emptyset_c$ is assumed to be 1.8 V for obtaining τ_L. It should be noted that the goal is not to obtain τ_L from τ_P, but to understand how the parameters affect τ_L.

To investigate the effect of ion LET on τ_P and τ_L, the simulation setup is the same as the one used in Section 3.5, except that instead of a fixed LET, several values were used: 5, 10, 16, 20, 40, and 60 MeV•cm^2/mg.

The investigation of the effect of V_B on τ_P and τ_L also adopts the same simulation setup from Section 3.5 with LET = 40 MeV•cm^2/mg, but with various values of V_B: 0, 1, 2, 3 V.

Same setup as Section 3.5 with LET = 40 MeV•cm^2/mg was used for investigating how the doping concentration in either the p-region or the n-region modifies the noise duration. The only difference is that these doping concentrations are not fixed values but ranges from 1x10^{17} cm^{-3}, 3x10^{17} cm^{-3}, 5x10^{17} cm^{-3}, 1x10^{18} cm^{-3}, to 3x10^{18} cm^{-3}.

6.3.2 Result

Fig. 6.3 shows the curves of $\emptyset_x$ for different LET. As predicted, higher LET results in a longer τ_P as well as τ_L. These were plotted in Fig. 6.4. For τ_P only LET > 16 MeV•cm^2/mg is focused, since it is defined as the duration when R_{ion} = 0. Both follow a similar linear trend predicted in Fig. 6.1. Even though τ_P is not defined for $LET < LET_{crit}$, we can still deduce a similar response of τ_L at low LET region. This result implies that, ions with low LET may generate a $\emptyset_x$ that is high enough (above $\emptyset_c$) but the resultant τ_L is too short to cause line-type MCUs. This can be used to explain the discrepancy in Fig. 4.7. At low LET region, cross section of the device decreased faster than prediction because τ_L is too short to cause line-type MCUs. This is also an explanation to why in terrestrial neutron test, no such MCU was observed. τ_L of the secondary ions might be too short to generate line-type MCUs.

The curves of $\emptyset_x$ for different values of V_B are shown in Fig. 6.5. Following the trend predicted in Fig. 6.2, both τ_L and τ_P shortens with higher V_B [Fig. 6.6]. This verifies the prediction and indicates that while increasing the V_B result in higher $\emptyset_x$ [Fig. 5.6], τ_L decreases, and may ultimately lead to the disappearance of the line-type MCU. It should be noticed that for V_B = 0 V, since $\emptyset_x$ is below $\emptyset_c$(1.8 V) at all times, the resultant τ_L in Fig. 6.5 is therefore 0 by definition.

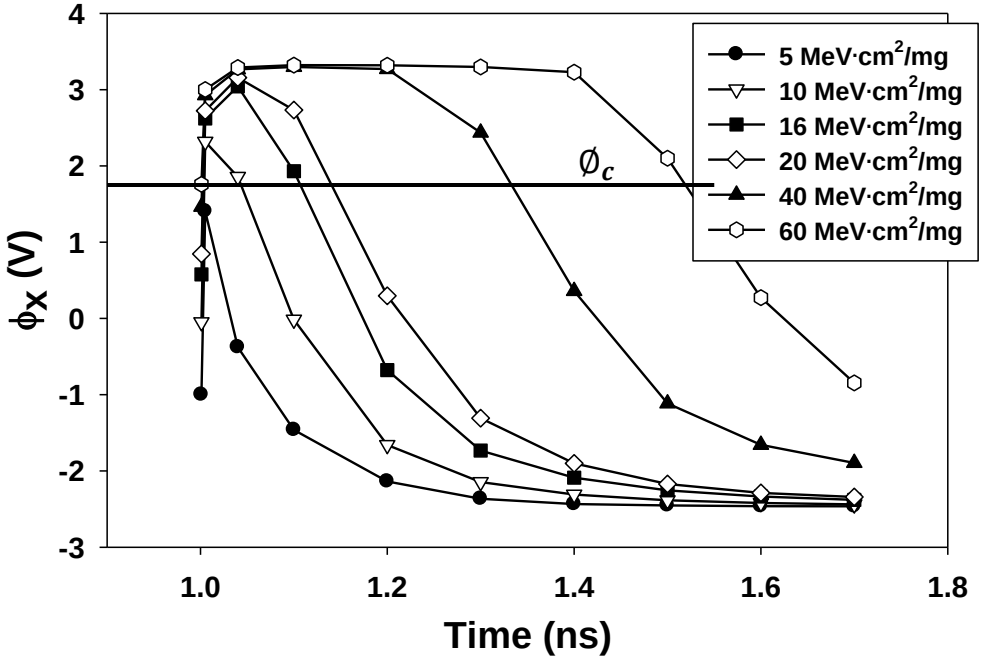

Fig. 6.3. Curves of $\emptyset_x$ for different values of LET.

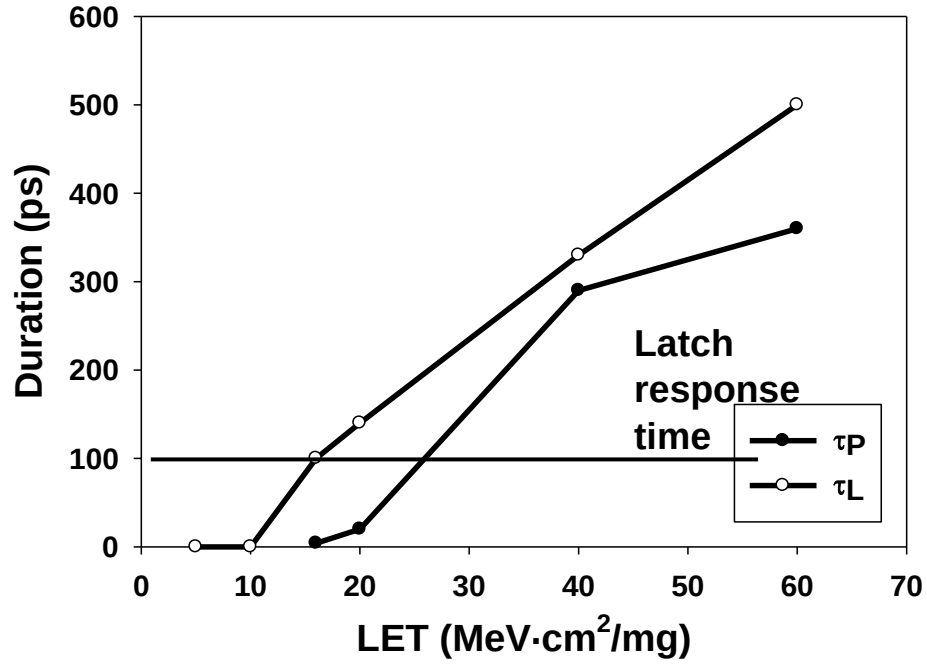

Fig. 6.4. Curves of τ_L and τ_P as functions of LET.

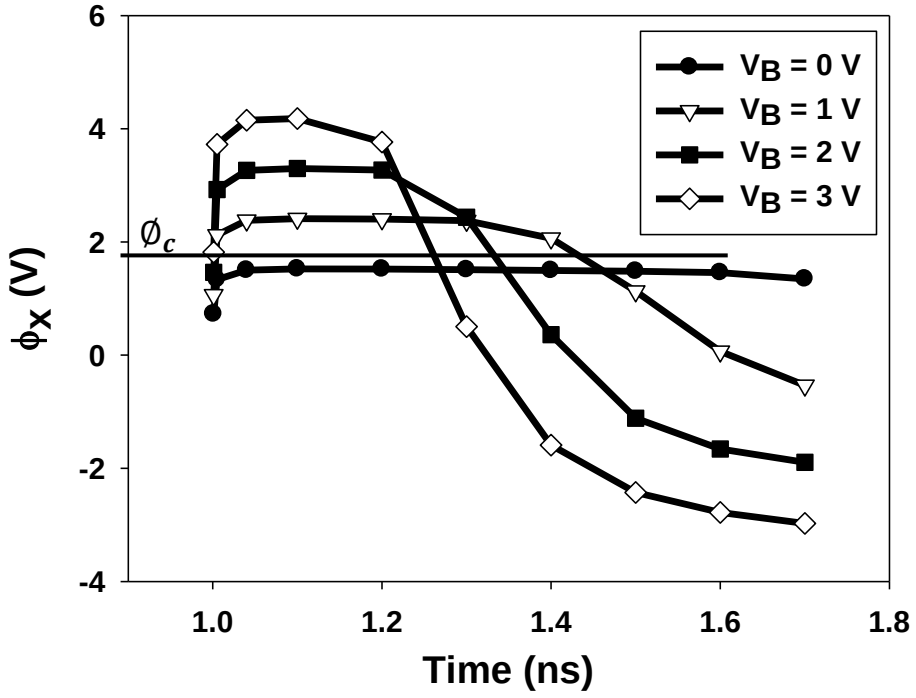

Fig. 6.5. Curves of $\emptyset_x$ for different values of V_B.

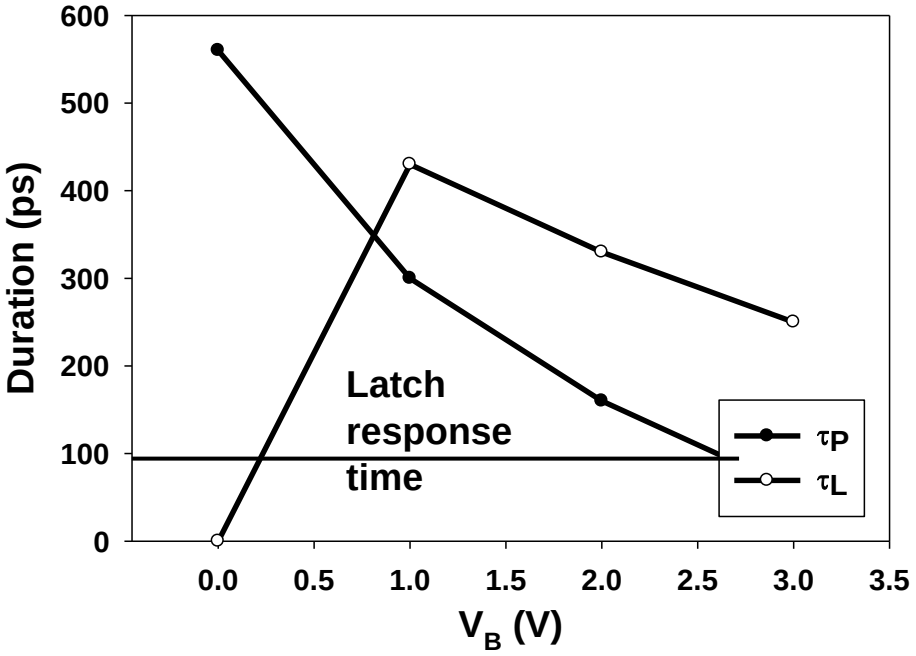

Fig. 6.6. Curves of τ_L and τ_P as functions of V_B.

Fig. 6.7 shows the curves of $\emptyset_x$ for different doping concentration in the p-region. The corresponding τ_L and τ_P are shown in Fig. 6.8 As predicted in Section 6.2, increasing the doping concentration in decreases τ_L. For the case of $3x10^{18}$ cm^{-3}, τ_L is barely higher than the typical response time of a latch. This gives a clue to the optimization of the device.

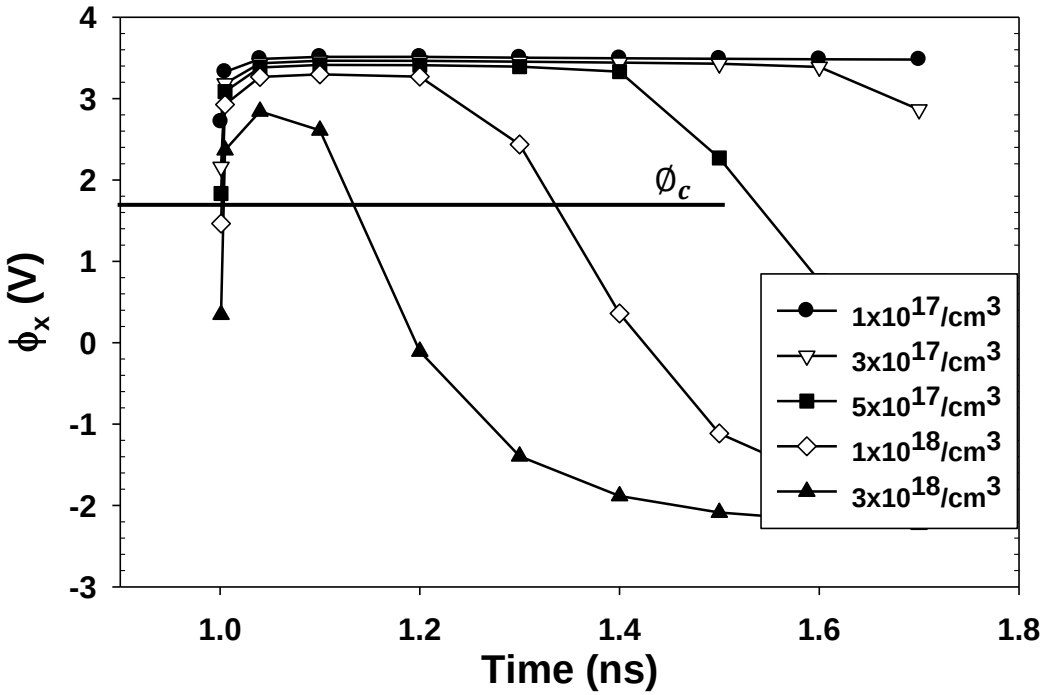

Fig. 6.7. Curves of $\emptyset_x$ for different values of p-well doping density.

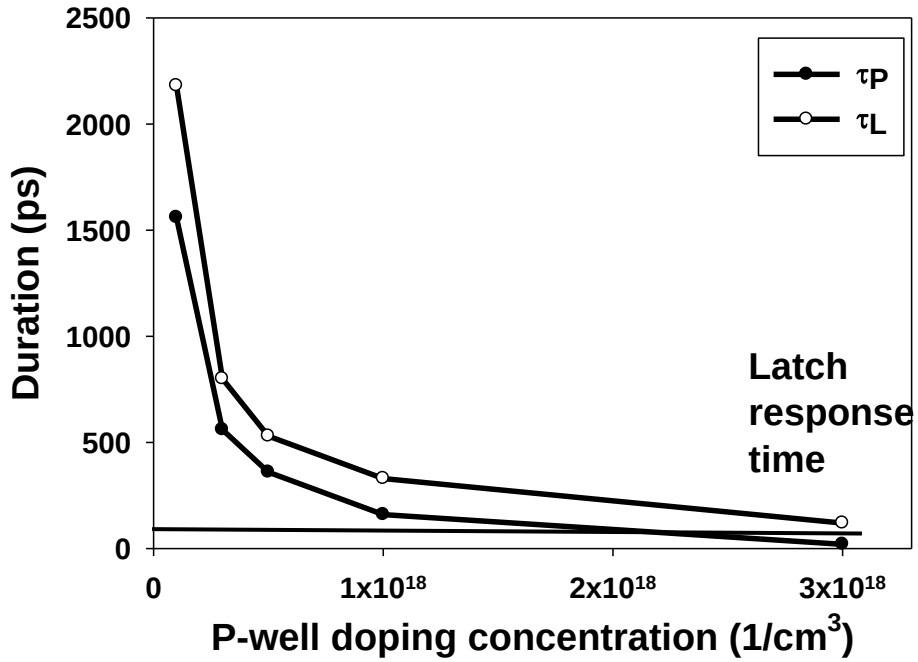

Fig. 6.8. Curves of τ_L and τ_P as functions of p-well doping concentration.

6.4 Device Optimization Guidelines based on Noise Duration

In the previous chapter, device optimization against line-type MCU was made based on how the device parameters effect the value of $\emptyset_{x(0)}$. In this section, another proposal will be made based on how the parameters affect τ_L. Similar limits will be set for this investigation: the proposal shall not involve the change of transistors on top of the BOX, the BOX, and the dimensions of the triple-well structure.

One possible direction is to significantly increase V_B. Even though this makes $\emptyset_{x(0)}$ much higher, the corresponding τ_L should also decrease significantly. As long as the duration is kept within 100 ps, no matter how high $\emptyset_{x(0)}$ is, no line-type MCU will occur. However, one must be aware of possible punch-through or avalanche effect inside the triple-well structure under such high V_B.

Increasing the doping in the p-region, which is a proposed optimization method in Chapter 5, also provides another benefit: the shortening of τ_L. This is the most promising method since it can reduce $\emptyset_{x(0)}$ and τ_L at the same time. The drawback of this action is the increased difficulty during process for a heavily doped well is harder to control.

6.5 Conclusion

In this chapter, the importance of the duration of the noise under the BOX was discussed. This work revealed several parameters that may potentially affect the duration of the noise and predicted the its trend from the changes of these parameters. Then the prediction was verified using simulation. A final proposal to reduce the occurrence of the line-type MCU was made: increasing the doping concentration inside the p-well.

Chapter 7 Summary

7.1 Contributions of This Work

To investigate the radiation-induced noise under the BOX and the line-type MCU it causes, a novel theoretical model discussing the physics taking place inside the ion-struck triple-well structure was proposed. It was theorized by this work that the junction struck by an ion can be characterized as a small resistance and becomes passable for the carriers. An assumption was made for the size of the ion-induced EHPs to stabilize to the width of the ion-stricken p-well, so that a simple comparison can be made between the amount of charges induced by the ion and the fixed charges in the depletion region. Based on this simple comparison, the ion track resistance can be estimated using the formula from the proposed model. This provides a simple yet effective method to estimate the radiation-induced noise under the BOX. A way to estimate the duration of the noise qualitatively is also provided. The proposed model, even though being a static one, is therefore able to describe the dynamic phenomenon of the line type MCU by proving the peak value of the noise.

Simulations were carried out and successfully verified the proposed theoretical model while discussing the effect from several parameters individually. They helped to explain the previous mystery in why the line-type MCU was not observed in the previous low LET terrestrial neutron test and provided the answer to the response of the noise under the BOX under different ion LET, which was observed in previous heavy ion test. The proposed theoretical model also helped to estimate the device cross section. The proposed model has been verified through dynamic simulation and is less time-consuming for the evaluation of the line-type MCU compared to using just simulation tools.

This work paved way to several methods to reduce the noise under the BOX, the duration of the noise, and the line-type MCU it causes without interfering with the operation of the device or changing the structure of the device significantly. By eliminating the line-type MCU, the reliability of the thin-BOX SOI technology is strengthened, and its application in IoT may be safely expanded to environments with radiation concerns.

7.2 Future Work

Several directions can branch from the current work. First, more investigation is required to improve Chapter 6 and present a formula that can estimate τ_L , which may be complex. However, it is the next improvement to better understand the noise under the BOX. For the cases when $\emptyset_x$is lower than $\emptyset_c$, the line-type MCU would not occur. On the other hand, if $\emptyset_x$is higher than $\emptyset_c$, τ_L is critical in deciding whether the line-type MUC will occur or not.

The second potential improvement from this work is the simulation used to verify the proposed theory. Inclusion of more simulation results using a wider range for the proposed parameters will make the verification more convincing, even though this work has used many values for them. Then the investigation becomes more complete, particularly with the doping concentration at each region. Also, the simulated triple-well structure used in this work is still rather simple, will abruptly defined junctions. To better represent the actual case of the device, a more realistic structure should be used. However, it should be stressed that this action will not affect the proposed model in any way. The third part is a better definition of *A*, which effect how the proposed model may be applied to other structure with different dimension.

The final possible direction is the application of the proposed theoretical model to other structure similar to the triple-well. Since this work discuss the physics inside an ion-struck n-p-n structure, which may also be found in various device such as bulk SRAM, it is not confined to only the thin-BOX SOI technology. By making some adjustment to the current theory, it is quite possible that the application can be extended to other devices.

7.3 Conclusion

The physics behind the radiation-induced noise under the BOX which takes place inside the triple-well structure of the thin BOX SOI technology and the line-type MCU it causes was investigated in this work. A theoretical model was proposed to characterize the ion-struck junction inside the triple-well structure as a passable tunnel with low resistance. Based on this, the carrier movement inside the structure after an ion strike is predicted and so is the value of the noise under the BOX. It's also predicted that several parameters from the proposed formula can affect both the value and the duration of the noise under the BOX. These predications were tested and verified by simulation. Under typical cases and when the ion LET is large, we can expect to be roughly equal to the bias condition at the n-well. For other cases, the proposed model helps to estimate the value of the noise.

To determine whether the line-type MCU will occur, both the value and the duration of the noise under the BOX have to be considered. The proposed model only provides the estimation of the value of the noise, but not the duration of the noise. However, if noise is too small, the line-type MCU will not occur no regardless of the duration. The information provided by the proposed model is therefore useful in confirming the cases where the line-type MCU would definitely not occur.

Based on the simulation-verified model, several approaches for device optimization were proposed, which may improve the device reliability and reduce the noised under the BOX. The most practical approach is to increase the p-well doping concentration to above $3x10^{18}$ cm^{-3}. This reduces both the value and the duration of the noise, consequently reduced the occurrence of the line-type MCU. Even though evaluation and prediction can also be made using only simulation, the proposed model is more efficient and universal. It can be adapted to other devices given that the profile of structure (doping density and dimensions) is known.

Appreciation

First of all, I cannot give more thanks to Professor K. Hirose and Professor D. Kobayashi for the tireless care and guidance on my research as well as the resources provide by the lab. Appreciation also goes to Mrs. Nishikawa. Couldn't have made it without her care and assistance with various paperwork. Thanks to the support from the lab, I managed to make presentations at two international conferences. I have learned what it is like to think and carry out research independently, which is crucial to my career after my graduation.

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Last but not the least, gratitude to all the family and friends who supported me throughout this exhausting, lonely, yet fruitful journey. Special thanks to: Yuki, who accompanied me in the early stage of my study and a critical part of my life; C. Chu, for the yearly visit and ideas few shared with me; Wilson Chang, for many things since high school; and Katrina Lin, for the hourly conversations and the emotional support, *du bist meine Engel*; May we never be distant.

Publication List

Journal Paper

1. C. Chung, D. Kobayashi, and K. Hirose, "Resistance-based modeling for soft errors in SOI SRAMs caused by radiation-induced potential perturbation under the BOX," *IEEE Transactions on Device and Materials Reliability*, submitted.
2. C. Chung, D. Kobayashi, and K. Hirose, "Understanding the difference in soft-error sensitivity of back-biased thin-BOX SOI SRAMs to space and terrestrial radiation," *IEEE Transactions on Device and Materials Reliability*, in preparation.

Proceeding

1. C. Chung, D. Kobayashi, and K. Hirose, "Mechanism behind long line-type MCUs in thin-BOX SOI SRAMs: resistance-based modeling and countermeasure," in *Proc. Radiation and its Effects on Devices and Systems (RADECS)*, Geneva, Switzerland, Oct. 2-6, 2017, paper C-4.
2. C. Chung, D. Kobayashi, and K. Hirose, "Threshold Ion Parameters of Line-Type Soft-Errors in Biased Thin-BOX SOI SRAMs: Difference between Sensitivities to Terrestrial and Space Radiation," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, San Francisco, CA, USA, Mar. 13-15, 2018, paper 4C.3

International Conference

3. C. Chung, D. Kobayashi, and K. Hirose, "Mechanism behind long line-type MCUs in thin-BOX SOI SRAMs: resistance-based modeling and countermeasure," in *Radiation and its Effects on Devices and Systems (RADECS)*, Geneva, Switzerland, Oct. 2-6, 2017, paper C-4.
4. C. Chung, D. Kobayashi, and K. Hirose, "Threshold Ion Parameters of Line-Type Soft-Errors in Biased Thin-BOX SOI SRAMs: Difference between Sensitivities to Terrestrial and Space Radiation," in *IEEE International Reliability Physics Symposium (IRPS)*, San Francisco, CA, USA, Mar. 13-15, 2018, paper 4C.3

Domestic Conference

1. C. Chung, D. Kobayashi and K. Hirose, “Heavy ion generated current leading to long line-type soft errors in thin BOX SOI SRAMs”, *Japan Society of Applied Physics (JSAP)*, paper 8a-A411-4, Fukuoka, Japan, September 9-5, 2017.
2. C. Chung, D. Kobayashi and K. Hirose, “Device simulation study on the physics of SOI devices in space- effects of galactic cosmic rays on a well structure under the buried oxide”, *Japan Society of Applied Physics (JSAP)*, Waseda Univ., Tokyo, Japan, paper 18p-A202-8, March 17-20, 2018.

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