論 文 の 内 容 の 要 旨

論文題目　Physics of soft error due to radiation-induced noise under the buried oxide layer in SOI devices

（SOIデバイス埋め込み酸化膜下で発生したノイズに起因するソフトエラーの物理）

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Fully depleted (FD) silicon-on-insulator (SOI) technology with buried oxide layer (BOX) has various advantages. One of these advantages is the reduction in power consumption which is achieved by adding a bias to the body from below the BOX, called the back-bias, thereby reducing the leakage current at standby mode. The soft error sensitivities to terrestrial neutrons is also less than 1/15 of that of conventional bulk device, drawing the attention for the technology's potential in space application, making the thin-BOX FD SOI device a good candidate for realizing Internet of Things (IoT). Considering these advantages, thin-BOX FD SOI devices may also have high potential in space application, where energy is limited, and great radiation hazard is expected.

To evaluate their endurance against radiation, recently, a heavy ion test was carried out by our research group. In the test a 65-nm thin-BOX FD SOI SRAM was used. Each chip consists of 2-Mb memory cells. Each of them contained 512 banks of 4-kb subarrays. Each bank had a 64 x 64-bit matrix. A 2-V back-bias was applied to the chip, which served as the standby mode of the device. Heavy ions with linear energy transfer (LET) up to 70 MeV·cm^2/mg were irradiated on to the chip. Without the back-bias, most soft errors took the form of SBU and a small number of MCU. For the case of 2-V back-bias, MCUs with a long line-type pattern along the bit line were observed, and these MCUs dominated the response from heavy ion strikes [Fig. 1]. While the line-type

MCU should be correctable by ECC since only one cell was disrupted in every word it crossed, it is highly probable that multiple MCUs may overlap the same word, resulting in errors unfixable by ECC.

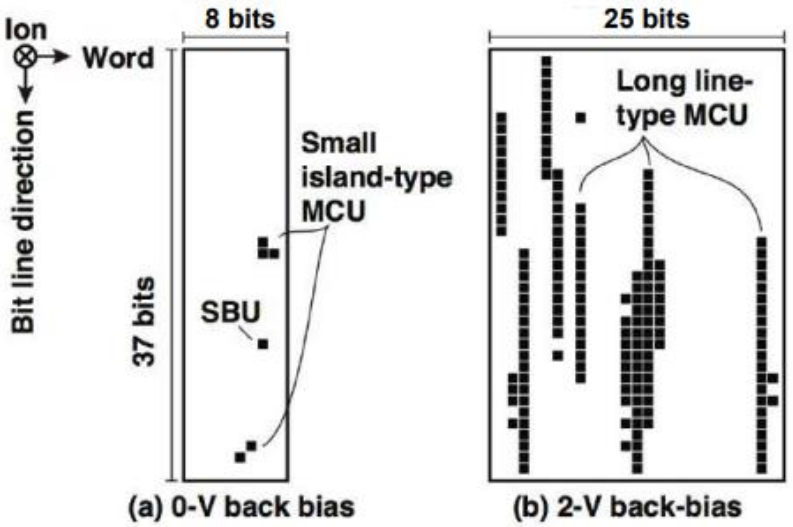

Figure 1. Physical map of the upset cells in (a) 8 x 37 partial array and (b) 25 x 37 partial array under Kr irradiation.

It has been suggested by previous work that temporal potential changes under the BOX layer due to the ion strike is what caused the cell upsets on top of the BOX. These noises travel along the bit line inside the structure under BOX and disrupt multiple cells along the path. To investigate the radiation-induced noise under the BOX and the line-type MCU it causes, a novel theoretical model discussing the physics taking place inside the ion-struck triple-well structure was proposed. This work characterizes the ion track at the junction region as a resistance. The proposed theoretical ion track resistance is not a static value but largely depends on the amount of EHPs induced by the ion. Without the ion-induced EHPs, the ion track resistance is close to infinite since the junction is impassible due to the built-on electric field. In the presence of the EHPS, the separated carriers in the depletion region are overlapped and canceled out. This lowers the potential barrier at the junction. When enough EHPs are induced by the ion, the potential will be lowered completely at the junction, allowing carrier movement.

Then, the movement of the carriers after the ion track can be modeled. Figure 2 displays the current flow inside the triple well structure predicted based on the potential distribution inside the triple-well structure. When the device is applied with a back-bias,

the highest potential is established at the n-well contact terminals, while the lowest is at the p-well contact terminals.

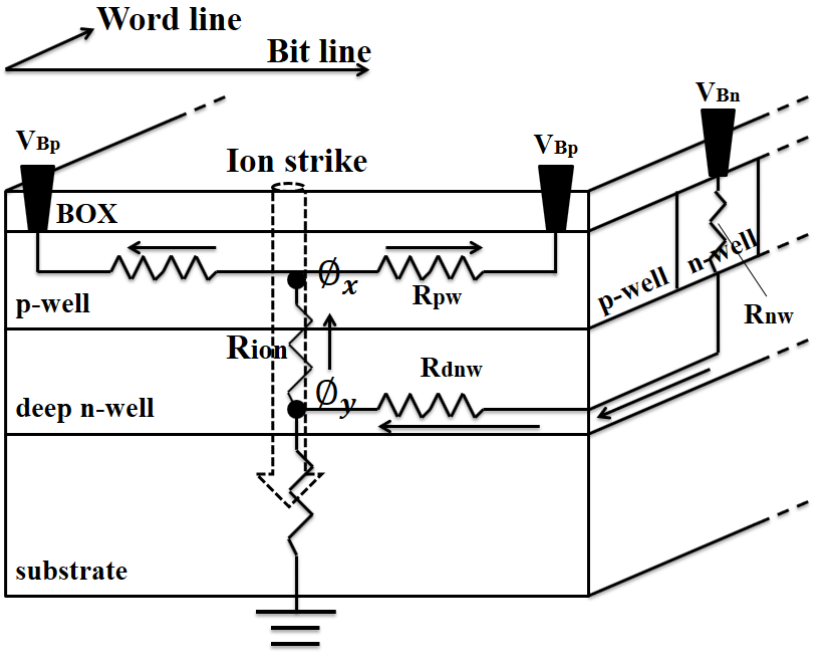

Figure 2. Conceptual drawing of the triple-well structure and the predicted current flow after the ion strike.

Based on the current path predicted in the previous section, analytical expression of $\emptyset_x$ can be created:

$$\emptyset_x = V_{Bp} + \emptyset_p + (\emptyset_y - V_{Bp} - \emptyset_p)\frac{R_{pw}}{R_{pw}+R_{ion}},$$

where $\emptyset_y$ is the electrostatic potential at the end of R_{ion} inside the deep n-well. Using the current flowing through R_{ion}, I, $\emptyset_y$ is expressed as:

$$\emptyset_y = V_{Bn} + \emptyset_n - I \times (R_{nw} + R_{dnw}).$$

Here $\emptyset_n$ is the difference between the intrinsic Fermi energy and the Fermi energy inside the deep n-well. The current I can be obtained by dividing the potential difference from the start of the current (n-well contact) to the end of the current (p-well contact) by the total resistance along the path:

$$I = \frac{V_{Bn}+\emptyset_n-V_{Bp}-\emptyset_p}{R_{ion}+R_{pw}+R_{nw}+R_{dnw}}.$$

In typical cases when the LET of the ion is high enough, R_{ion} is negligible, and $R_{pw} \gg R_{dnw} + R_{nw}$ because the cross-sectional area of the combined n-region

perpendicular to the flow of the current is much larger than that of the p-well. This allows the simplification of the expression for $\emptyset_x$:

$$\emptyset_x = \emptyset_y = V_{Bn} + \emptyset_n.$$

Figure 3 shows the simulation result of $\emptyset_x$ for different V_B. The discrepancy between simulation and calculation using the proposed theory was smaller than 0.2 V, which confirms the accuracy of the theory.

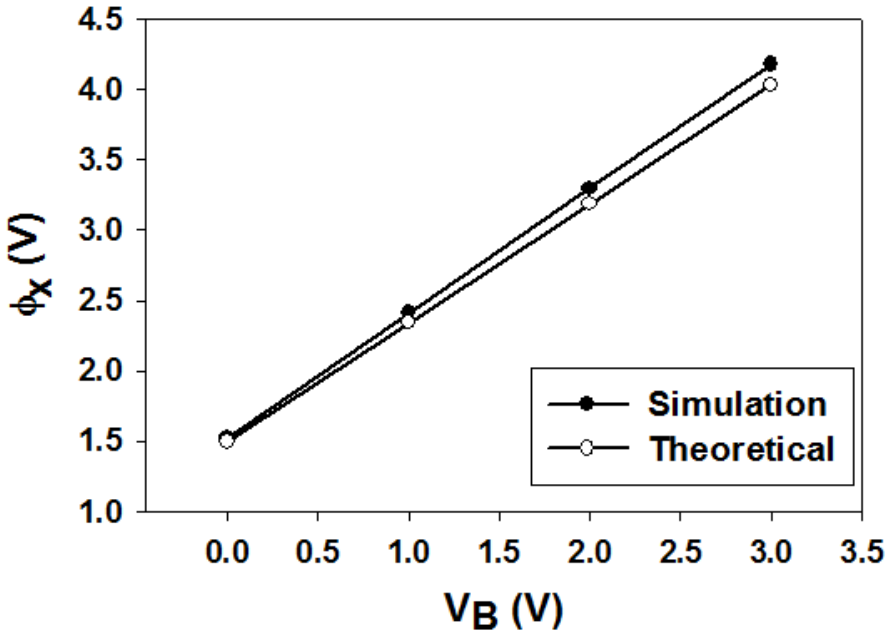

Figure 3. $\emptyset_x$ as a function of the V_B under a LET of 40 MeV•cm^2/mg.

The theoretical model paved way to several methods to reduce the noise under the BOX and the line-type MCU it causes without interfering with the operation of the device or changing the structure of the device significantly. By eliminating the line-type MCU, the reliability of the thin-BOX SOI technology is strengthened, and its application in IoT may be safely expanded to environments with radiation concerns.