博士論文

Study of operation mechanism and interfacial properties in two-dimensional layered materials based FET

(2 次元層状物質を用いた FET における動作機構と界面特性に関する研究)

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Abstract

From the successful demonstration that graphene can be exfoliated by scotch tape, two-dimensional(2D) materials have been the hot research spot because of its intriguing properties of optical, mechanical, and electrical characteristics. Although the carrier mobility of graphene is extremely high, an absence of the energy band gap hinders its application for electron devices. Another group of 2D materials, transition metal dichalcogenides (TMDC), has attracted much attention in ultimate scaled device research due to its large tunable band-gap. However, the operation mechanism of 2D-FET has not been fully investigated. Moreover, a capacitance measurement of 2D-FET is ambiguous from both experimental and theoretical view. The lack of full understanding of electrical measurements of 2D-FET makes 2D/high-*k* interfacial properties still unclear. Therefore, this study will explore the operation mechanism of 2D-FET and high-*k*/2D interfacial properties.

Firstly, the key issues in the device fabrication process of high-quality MoS_2 dual-gate FET have been demonstrated. The operation mechanism of 2D-FET is discussed based on *I-V* characterization. Accumulation-mode FET is proposed and developed to explain the observed behavior.

Then, *C-V* characterization of MoS_2 FET structure has been systematically studied. Parasitic capacitance is totally removed by using the insulating quartz substrate. Resistance effect is carefully checked, which is one of the main origins for the observed frequency dispersion in the fully-depleted region of MoS_2 FET. Quantum-mechanical effect is observed and investigated, which is important in terms of device physics and application prospect.

Based on the achievements in *I-V* and *C-V* characterization, D_{it} - energy distribution has been successfully extracted from the monolayer to bulk MoS_2. The origin of D_{it} is investigated. For conduction band side, band-tail shape D_{it} close to CB is observed with the range of ~10^{12} cm^{-2}eV^{-1}, which is attributed to Mo-S bond bending due to the strain caused by the high-*k* deposition and/or the surface roughness of the

SiO_2 surface.

Nb-doped *p*-type MoS_2 has been investigated to study D_{it} at valance band side. The extracted D_{it} of *p*-MoS_2 for valance band side is of ~10^{13} $cm^{-2}eV^{-1}$, which cannot be reduced by using atomically flat *p*-MoS_2/*h*-BN/graphite hetero-FET. Several interesting phenomena are found in *p*-type MoS_2. One is the surface electron accumulation in *p*-type MoS_2, which prevents the fabrication of atomically thin *p*-FET even from a *p*-MoS_2 crystal. Another one is the asymmetry between electron and hole transport. All of these behaviors are mainly due to the formation of surface sulfur vacancy.

Based on the achievements above, the crystal quality of most of the 2D materials is evaluated based on the bulk doping concentration by depletion width maximum. The thickness scaling rule is proposed for 2D-FET.

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1 Introduction

1.1 MOSFET technology

Semiconductor industry becomes more and more important in many fields. MOSFET (metal-oxide-semiconductor field effect transistor), which is the fundamental device in an integrated circuit(IC), has experienced rapid progress. To increase integration level, MOSFET dimension has been reduced, which is called “scaling”. The scaling speed was forecast by Moore in 1964, which is called “Moore`s law”. It states that MOSFET density on IC doubles about every 1.5 years as shown in **Fig. 1-1** [1]. Moore’s law has guided IC development for almost half a century.

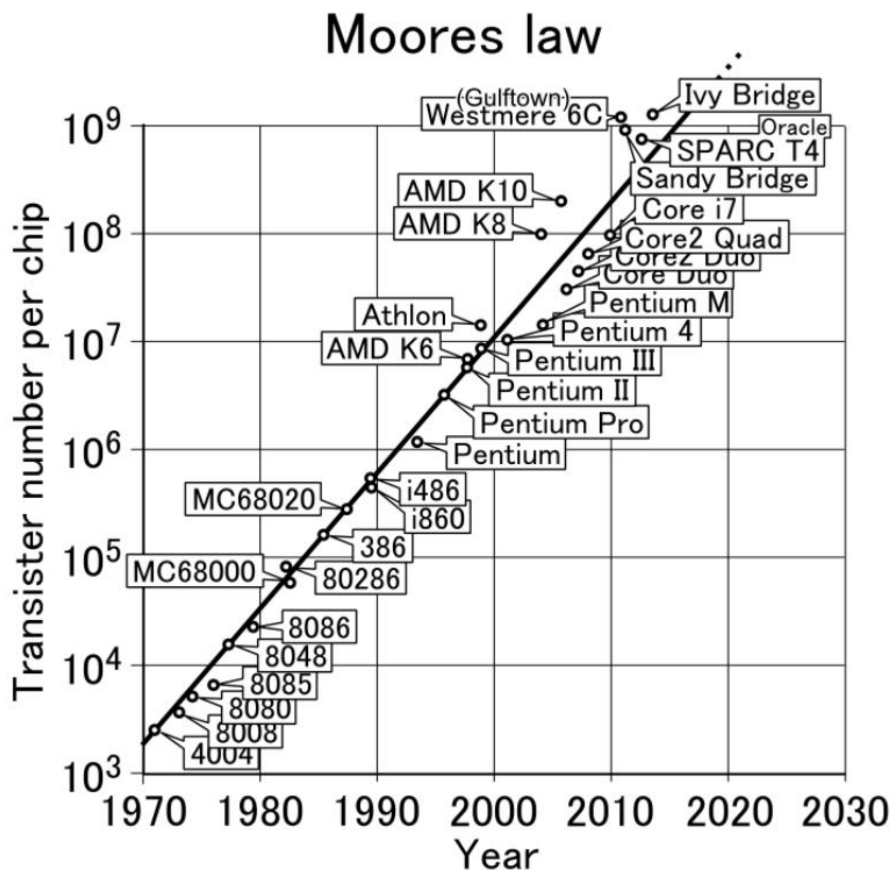

Fig. 1-1 Scaling trend of IC. MOSFET density on IC doubles about every 1.5 years [1].

1.2 Short-channel effect in conventional MOSFET

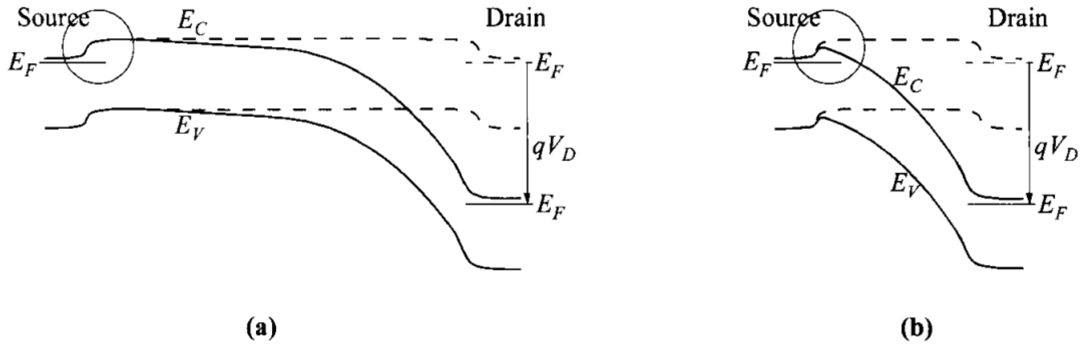

Fig. 1-2 Energy band diagram from the source to the drain at **(a)** the long-channel and **(b)** the short-channel MOSFETs. Dashed line indicates $V_D = 0$ V and solid line for $V_D > 0$ V[2].

With decreasing the channel length of MOSFET, the depletion widths of the source and drain become comparable to the channel length, thus making the device performance depart from a long-channel case. This departure, usually called a short-channel effect, comes from a two-dimension potential distribution and high electric fields in the channel region. One of the severe effects is drain-induced barrier lowering (DIBL), that the drain bias can affect the barrier at the source as shown in **Fig. 1-2**[2]. In the short-channel MOSFET, by applying V_D, the barrier at the source is lowered, which results in the threshold voltage lowering.

Because the short-channel effect complicates device operation and degrade device performance, it should be suppressed. The distribution of electrical potential in the channel region of MOSFET can be derived from the Poisson equation. Based on the Poisson equation, one of the most important parameters is the natural scaling length. Natural scaling length indicates the extension of the electrical field from the source/drain into the channel region. Natural scaling length is defined as follows[3]:

$$Natural \quad scaling \quad length = \sqrt{\frac{1}{N}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{ch} t_{ox}} \,. \tag{1-1}$$

ε_{ch} and ε_{ox} are the dielectric constants of the channel and the insulator, respectively. N

is defined as an effective gate number. N = 1 in a single-gate MOSFET and N = 2 in a double-gate MOSFET. t_{ch} and t_{ox} are the thickness of the channel and the insulator, respectively. To eliminate the effect of extension of the electrical field from the source/drain into the channel, the channel length should be 6 times larger than the natural scaling length. Thus, the simple way to eliminate the short-channel effect is to reduce the channel thickness.

1.3 2D materials

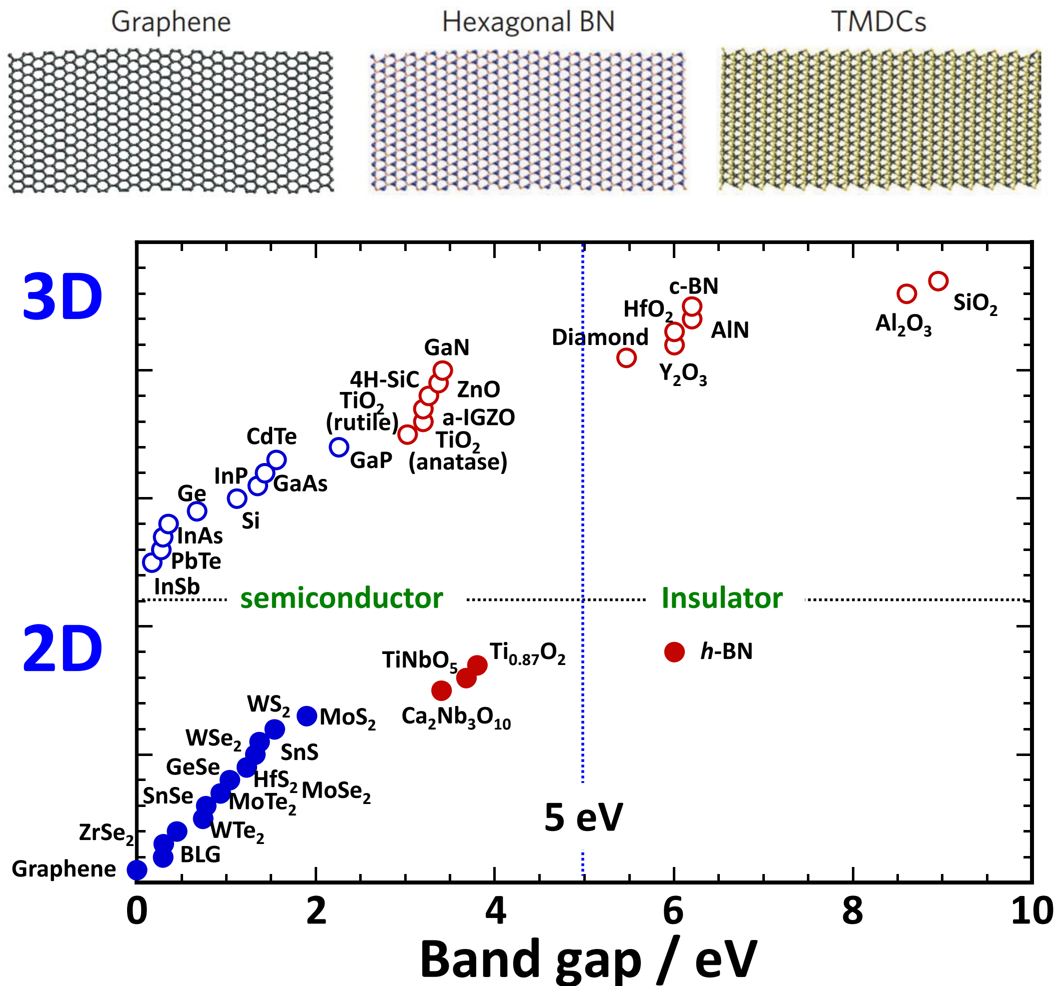

Fig. 1-3 Overview of 2D materials.

From the successful demonstration that graphene can be exfoliated by scotch tape,

two-dimensional(2D) materials have been the hot research spot because of its intriguing properties of optical, mechanical, and electrical characteristics. Strong covalent bonds are formed within the layer while weak van der Walls interaction is formed between neighboring layers in most 2D materials, which makes it possible to prepare 2D thin film by exfoliation method. Although the carrier mobility of graphene is extremely high, an absence of the energy band gap hinders its application for electron devices as shown in **Fig. 1-3**. Another group of 2D materials, transition metal dichalcogenides (TMDC), has attracted much attention in research on condensed matter physics[4-6] as well as ultimately scaled devices due to its large thickness-dependent band-gap.

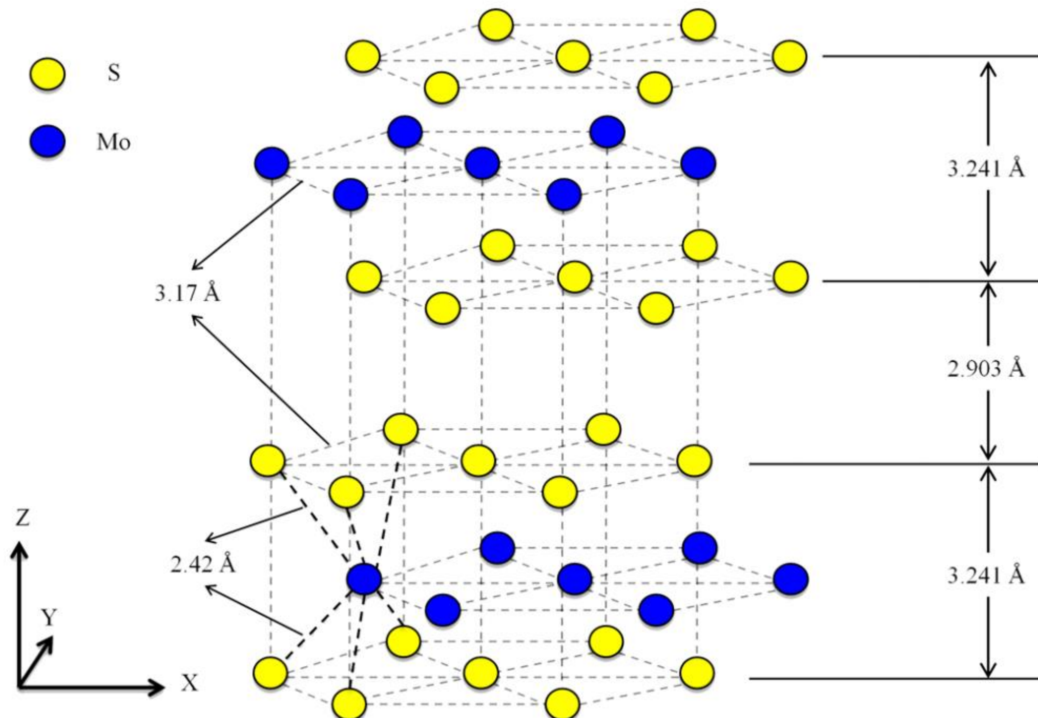

Fig. 1-4 Crystal structure of MoS_2. One MoS_2 layer consists of 2 S sheets and 1 Mo sheet.[7]

One of the typical materials in this group is MoS_2. MoS_2 has a layered hexagonal crystal structure, in which Mo atom is located at the center of a trigonal prism composed of 6 S atoms as shown in **Fig. 1-4**. Strong covalent Mo-S bonds are formed within the layer while weak van der Walls interaction is formed between neighboring MoS_2 Mo-S-Mo layers. Monolayer MoS_2 has the thickness of only 0.324 nm, which makes it

promising for suppressing the short-channel effect.

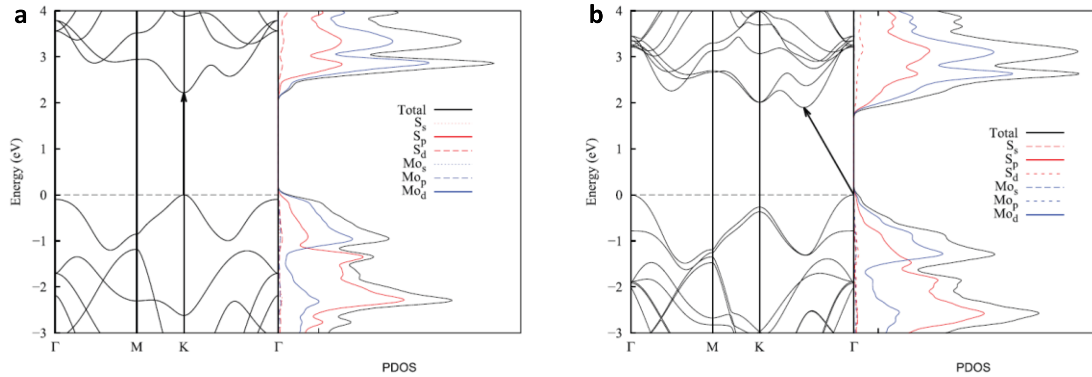

Fig. 1-5 Band structure of **(a)** monolayer and **(b)** bilayer MoS_2 based on first-principle calculation. A clear direct band-gap(K point) to indirect band-gap(Γ-K direction) transition is observed from monolayer to bilayer. [8]

First-principle calculation has demonstrated that monolayer has 1.85 eV direct band-gap while multilayer MoS_2 has 1.1 eV indirect band-gap. As shown in **Fig. 1-5**, the covalent bond of MoS_2 is mainly composed of *p* orbit of S and *d* orbit of Mo. Moreover, the added one layer from monolayer to bilayer interact with band structure, thus inducing the transition from direct band-gap at K point to indirect band-gap at Γ-K direction.

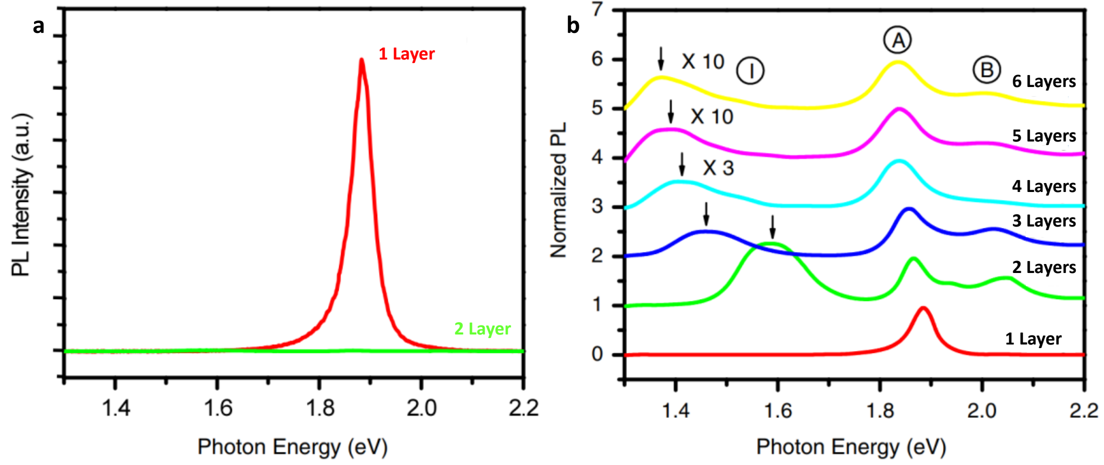

Fig. 1-6 (a) PL spectra of mono- and bilayer MoS_2. **(b)** Normalized PL spectra of MoS_2 from 1 layer to 6 layers. [9]

Photoluminescence (PL) study of MoS_2 confirms the calculation results in **Fig. 1-5**. In monolayer MoS_2 PL spectra as shown in **Fig. 1-6 (a)**, only one strong peak (A) is observed at 1.9 eV, which corresponds to direct band-gap. While in bilayer MoS_2, due to the transition from direct band-gap to indirect band-gap, PL intensity at A is seriously reduced. Moreover, a lower energy peak (I) is observed, which corresponds to indirect band-gap as shown in normalized PL in **Fig. 1-6 (b)**.

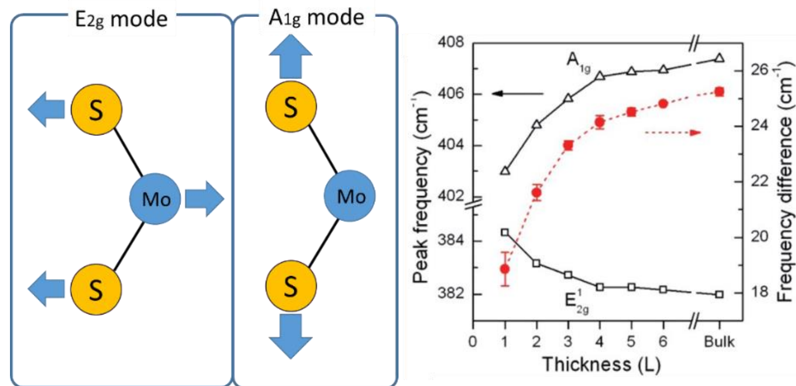

Fig. 1-7 Atomic displacements of two Raman-active modes and its frequencies in Raman spectroscopy.[10]

Raman spectroscopy shows atomic vibration information by detecting electromagnetic radiation at laser illuminated area. **Fig. 1-7** shows two active modes in Raman of MoS_2. Raman also provides a fast way to determine MoS_2 thickness because the frequency difference is sensitive to the layer number. For example, the frequency difference between these two modes equals to 19 cm^{-1} at monolayer and 21 cm^{-1} at bilayer case. This enables us to quickly distinguish layer number with the help of Raman spectroscopy.

1.4 Overcome the short-channel effect by 2D-FET

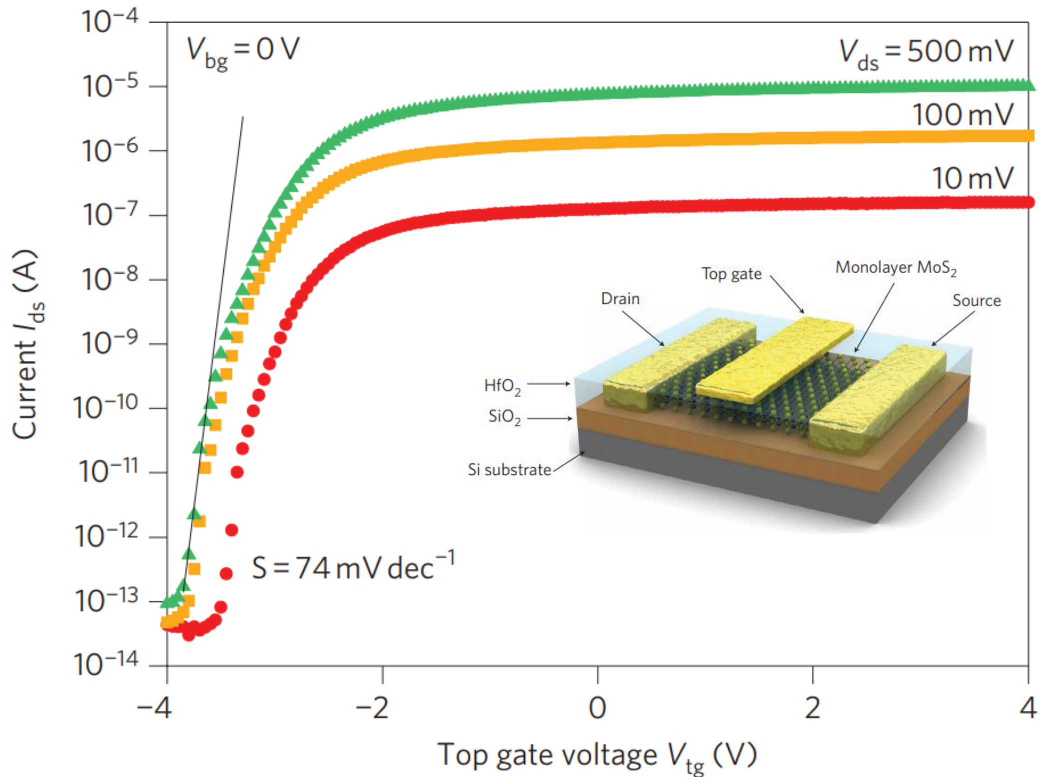

Fig. 1-8 (a) I_{DS}–V_{TG} characteristics of monolayer MoS_2 dual-gate FET at V_{DS} = 0.01, 0.1, 0.5 V, respectively. Inset shows device structure.[4]

Radisavljevic et al. firstly demonstrated high performance monolayer MoS_2 dual-gate device as shown in **Fig. 1-8**. Channel length here is several microns. It shows low subthreshold swing (*S.S.*) of 74 mV/dec and high field-effect mobility of 200 cm^2 V^{-1}

s^{-1}. Although later, this high field-effect mobility is pointed out to be overestimated due to neglecting capacitive coupling between top and bottom gate. The accurate mobility in this initial paper is ~ 10 cm^2 V^{-1} [6].

Desai et al. [11] demonstrated that bilayer MoS_2 FET can still operate well in the short-channel device due to its ultra-thin thickness. The device has the channel length of ~ 3.9 nm in the off state and ~ 1 nm in the on states, which is confined by SWCNT gate as shown in **Fig. 1-9**. *S.S.* is of 65 mV/dec and On/Off ratio of 10^6.

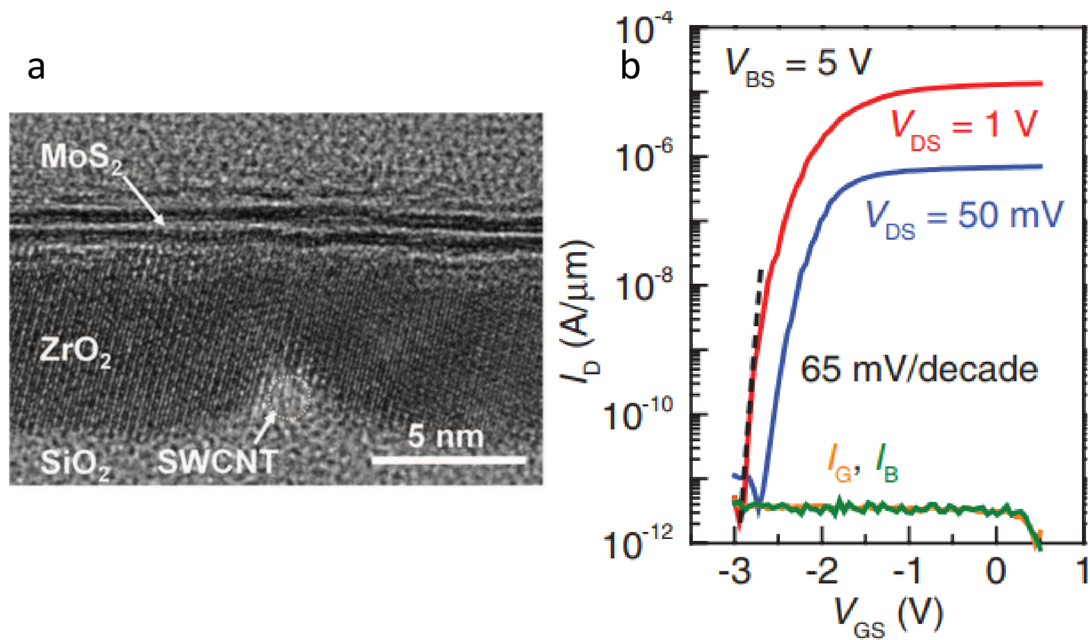

Fig. 1-9 (a) Cross-sectional TEM image of a representative sample showing the single-wall carbon nanotube (SWCNT) gate, ZrO_2 gate dielectric, and bilayer MoS_2 channel. **(b)** I_D-V_{GS} characteristics of a bilayer MoS_2 channel SWCNT gated FET.[11]

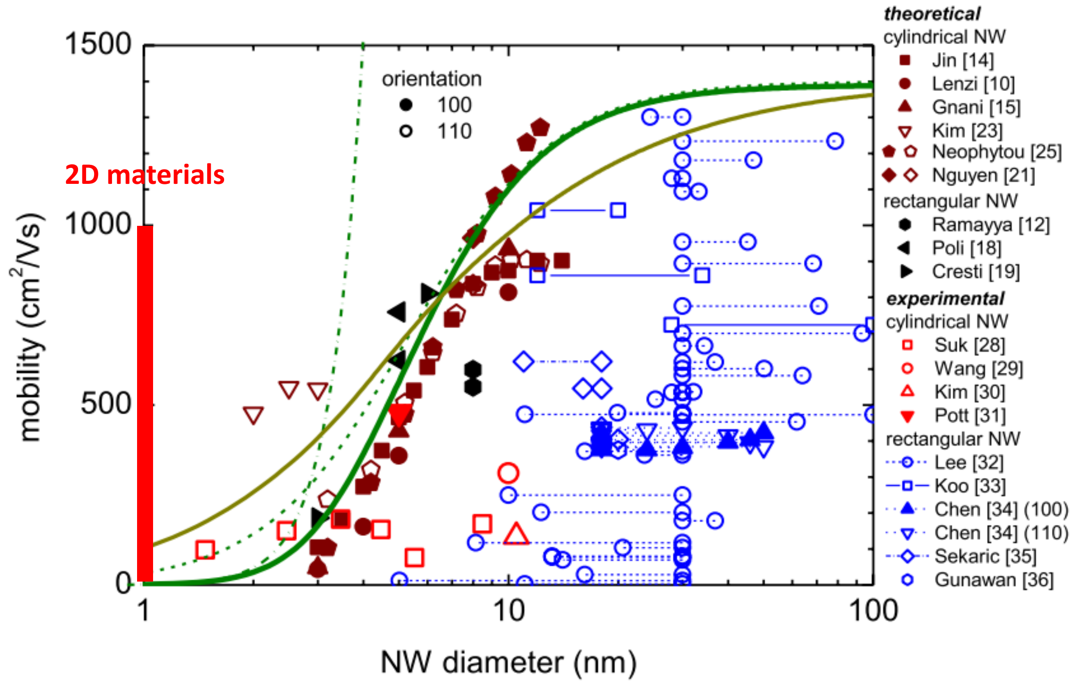

Fig. 1-10 Theoretical and experimental mobility for SiNWs. [12]

Up to now, the mobility in monolayer 2D materials can reach a high value close to 1000 $cm^2\ V^{-1}\ s^{-1}$ by optimizing interfacial properties, choosing low effective mass 2D materials and so on. Compared with the mobility of conventional semiconductor materials in nano-scale thickness, 2D - materials show higher mobility. **Fig. 1-10** shows silicon nanowire (SiNW) mobility as a function of diameter [12]. When diameter < 2 nm, mobility is severely limited by the surface roughness scattering, which is lower than 2D-materials with the same thickness.

1.5 Operation mechanism of 2D-FET

The operation mechanism of 2D-FET needs to be clarified in terms of both device physics and device performance. For example, *S.S.* is directly related with interface states. Different operation modes have different *S.S.* – interface states relations. Schottky barrier FET (SB-FET) model has been widely applied in 2D-FET. However, some studies report the device behaviors, which cannot be explained by SB-FET. These behaviors are similar to accumulation mode FET (ACCU-FET), which has been studied in silicon-on-insulator (SOI) and silicon nanowire FET. Therefore, in this subchapter, SB-FET and ACCU-FET models will be introduced.

1.5.1 SB-FET mode in 2D-FET

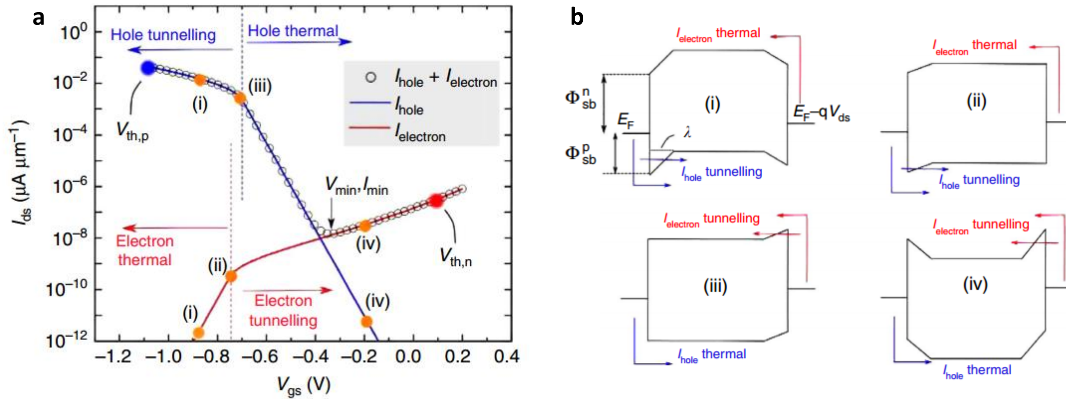

Fig. 1-11 (a) Transfer characteristic of a black phosphorus SB-FET. **(b)** Schematic of band diagram to show SB-FET operation mechanism. [17]

One of the key performance-limiting factors in 2D-FET is the 2D/metal contact [13]. Based on the historical background of similar structures for carbon nanotube [14], ultrathin silicon-on-insulator [15], and silicon nanowire [16], the Schottky barrier FET (SB-FET) model is proposed and developed by Appenzeller et al. to explain the 2D-FET operation mechanism [17-19]. Tunneling current from contact to channel is

considered to be dominant in SB-FET. Since the tunneling transport at the SB junction is dominant, studies on achieving low contact resistance by choosing metal types and inserting van der Waals materials and so on are promoted [20, 21].

One of the most important success in SB-FETs is the explanation of the ambipolar behavior. **Fig. 1-11 (a)** shows the transfer characteristic of the black phosphorus back-gate FET. It shows ambipolar behavior, which has both electron- and hole- branch. It is explained as shown in **Fig. 1-11 (b)**. By changing V_{gs}, band diagram is modulated. Electron on-state is achieved when tunneling occurs between contact metal and channel conduction band. Hole on-state is achieved when tunneling occurs between contact metal and channel valance band.

SB-FET also explains the reason why MoS_2-FET always show *n*-type behavior [18]. By changing the contact metal, I_{DS}-V_{GS} curve is affected as shown in **Fig. 1-12**. High work function metals such as Pt result in poor I_{DS}-V_{GS}. However, all of the devices still show *n*-type behavior independent of contact metal types. Based on this phenomenon, it is claimed that strong metal-MoS_2 pinning near to conduction band exists.

Although SB-FET mode explains some device behaviors in terms of metal/2D contact, it fails to explain the device behaviors in terms of 2D channel and insulator/2D interface. For example, the residual conductance observed in most multilayer 2D-FETs when over the critical thickness [22] cannot be explained by only the SB-FET mode, suggesting a 2D depletion nature. This behavior is often observed in ACCU-FET. Moreover, in conventional MOSFET, device operation behavior is understood by different electrical measurements such as capacitance measurement. However, SB-FET in 2D-FET is built only by *I-V* measurement and has not been supported by any other electrical measurement experimentally. Therefore, ACCU-FET should also be considered in 2D-FET.

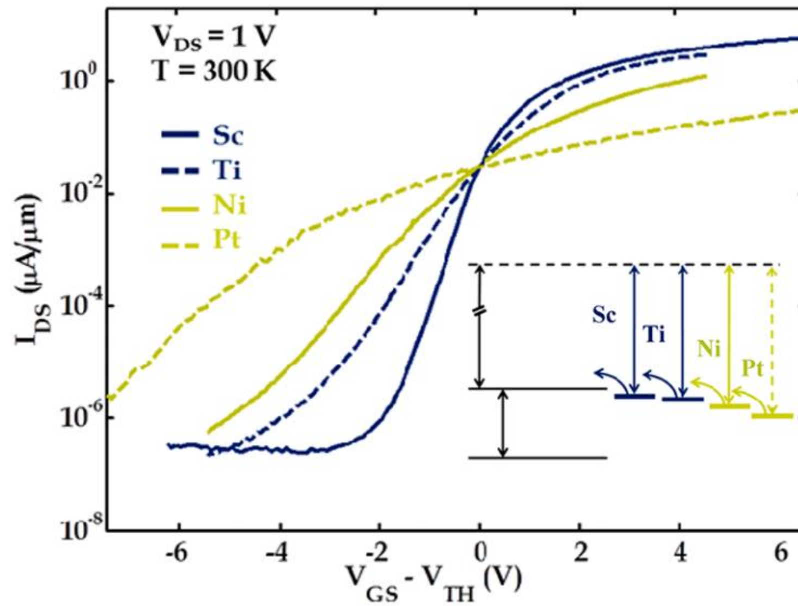

Fig. 1-12 Transfer characteristic of MoS_2 SB-FET with different contact metals. [18]

1.5.2 ACCU-FET mode in 2D-FET

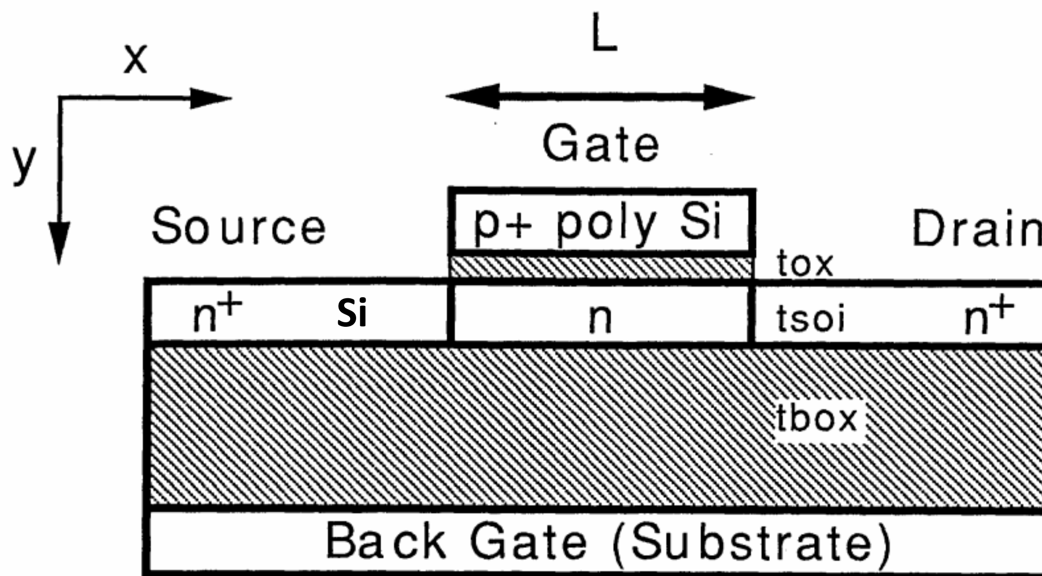

Fig. 1-13 Cross-section of accumulation-mode SOI FET. [23]

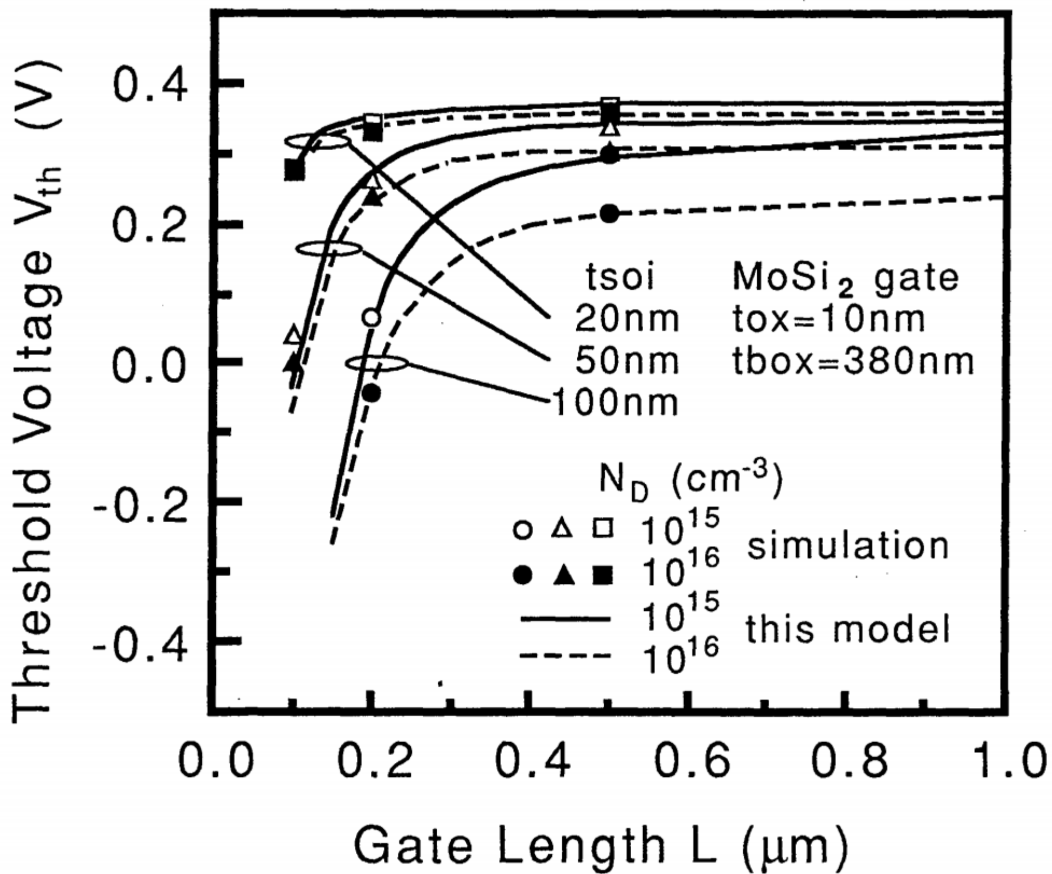

Fig. 1-14 SOI ACCU-FET threshold voltage vs gate length at different body thickness and doping concentration. [24]

ACCU-FET was firstly studied in SOI-FET [23,24]. In SOI ACCU-FET, for *n*-channel transistors, the n^+ doped source and drain regions are in contact with *n* channel as shown in **Fig. 1-13**. Fully depleted channel should be achieved to obtain well-controlled subthreshold region. Accumulation-mode FETs show similar behaviors to those of conventional inversion-mode FETs even though the transport mechanism is different. In accumulation-mode, the current comes from accumulation of majority carriers. While in inversion-mode, the current comes from the formation of inversion layer. Detailed numerical simulations of ACCU-FET based on SOI have been studied based on Poisson equation [23,24]. Short-channel effect is studied for ACCU-FET as shown in **Fig. 1-14**.Threshold voltage (V_{TH}) roll-off due to short-channel effect in SOI ACCU-FET is calculated as a function of SOI body thickness. Similar to conventional

inversion-FET, short-channel effect is suppressed by decreasing SOI body thickness.

Later, ACCU-FET model was also found in silicon nanowire FET as shown in **Fig. 1-15** [25]. The device turns on and off by modulating majority carriers below the gate. This type of top-gate ACCU-FET shows unipolar behavior. When the positive gate bias is applied, the channel below the top gate is inverted to the electrons. However, due to the formation of two *p-n* junctions at source/channel and channel/drain, electrons cannot transport through the whole channel. When the negative gate bias is applied, the channel below the top gate is accumulated and shows hole transport.

At present, although similar behaviors have been observed in 2D-FET, ACCU-FET mode has not been studied. Thus in this study, ACCU-FET mode will be systematically investigated in 2D-FET.

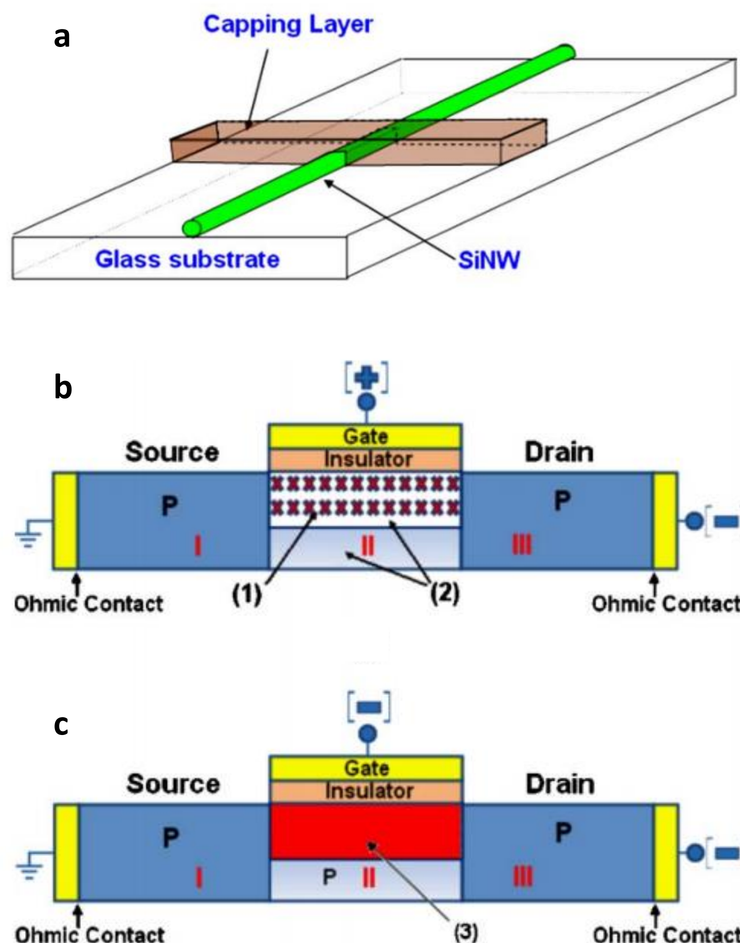

Fig. 1-15 (a) Device structure of top-gate silicon nanowire accumulation-mode FET. **(b)** Operation mechanism of this ACCU- FET at positive and negative gate bias cases.

1.6 Interface states in MoS_2

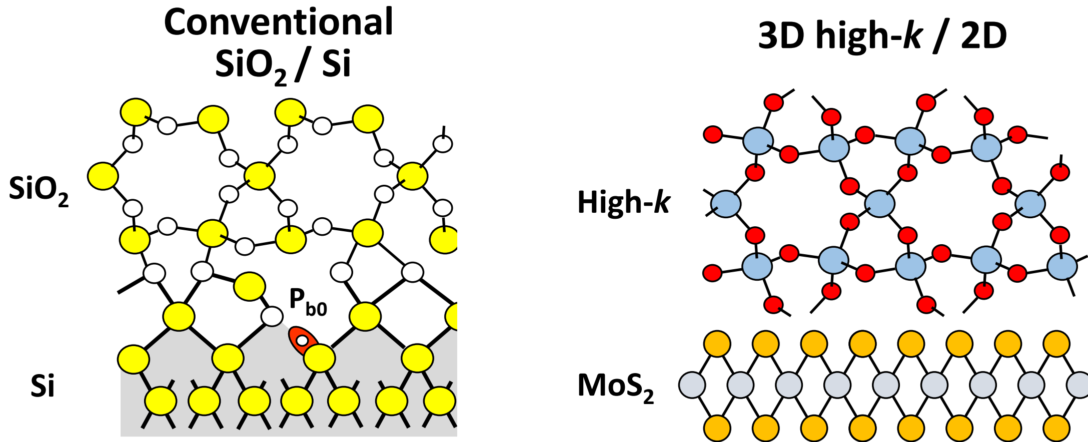

Fig. 1-16 Schematic of SiO_2/Si and high-*k*/2D interfaces, respectively.

Interface states play an important role in a very wide range of phenomena from optics to electronics. Understanding the interfacial properties is important to improve device performance. As for conventional SiO_2/Si interface, it is Si P_b center that dominates the interface states density (D_{it}) as shown in **Fig. 1-16**. As for a high-*k*/2D interface, no dangling bonds exist from MoS_2 side ideally. The origin of interface states needs to carefully investigated.

One of the origins for interface states in MoS_2 system is the defects states. Defects have been widely investigated by atomic-scale spectroscopy. **Fig. 1-17** shows images of scanning transmission electron microscope (STEM) of MoS_2 [26,27]. Many types of defects are observed, such as sulfur vacancy (Vs) and antisite defects (Mo_{S2}). Although defects type is largely dependent on the preparation method, the most frequently observed defect in mechanical exfoliated method (ME) and chemical vapor deposition (CVD) MoS_2 is Vs as shown in **Fig. 1-18**, which is due to the lowest formation energy among all types of defects. Formation of Vs will introduce defects states in the band-gap as shown in **Fig. 1-19**. Vs introduces two unoccupied defect levels ~ 0.3 eV below conduction band (CB) and one occupied defect level close to valance band (VB).

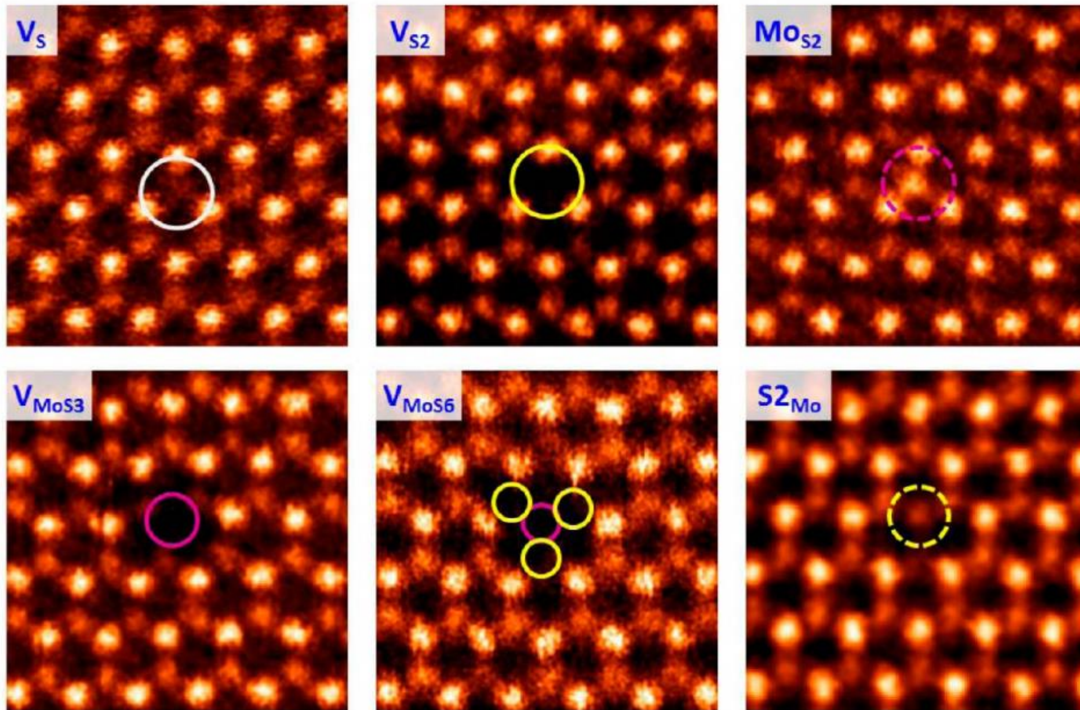

Fig. 1-17 STEM image of different types of defects in MoS_2. [26]

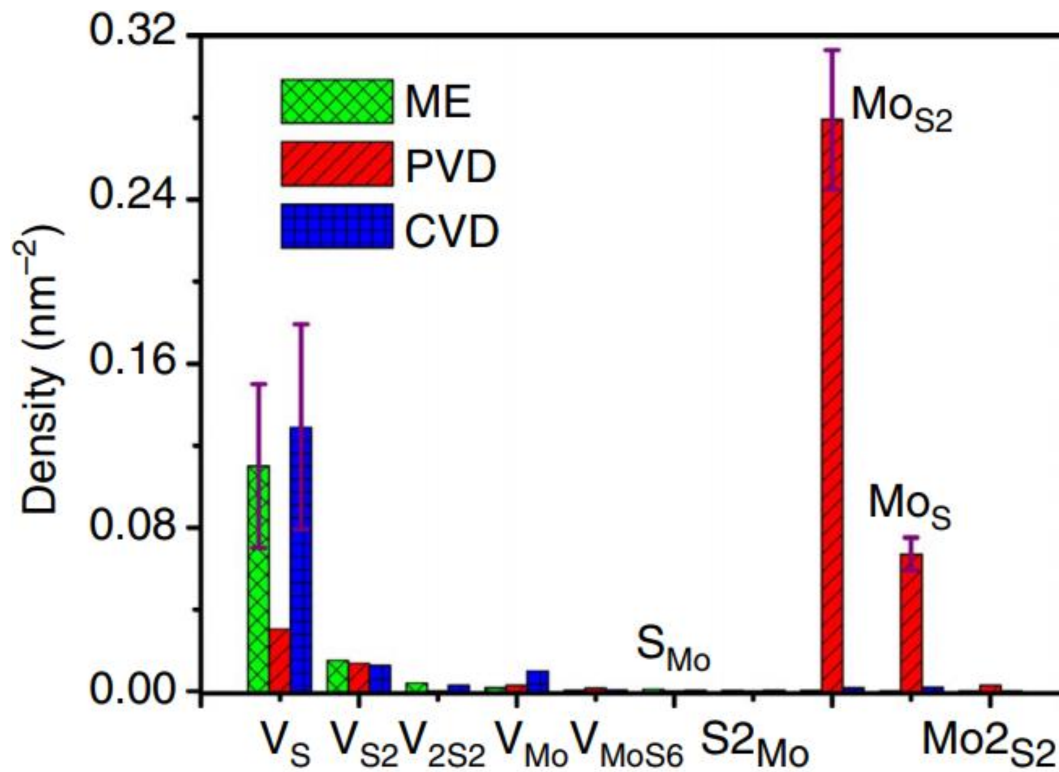

Fig. 1-18 Histogram of defects in mechanically exfoliated method, physical vapor deposition (PVD) and chemical vapor deposition method. [27]

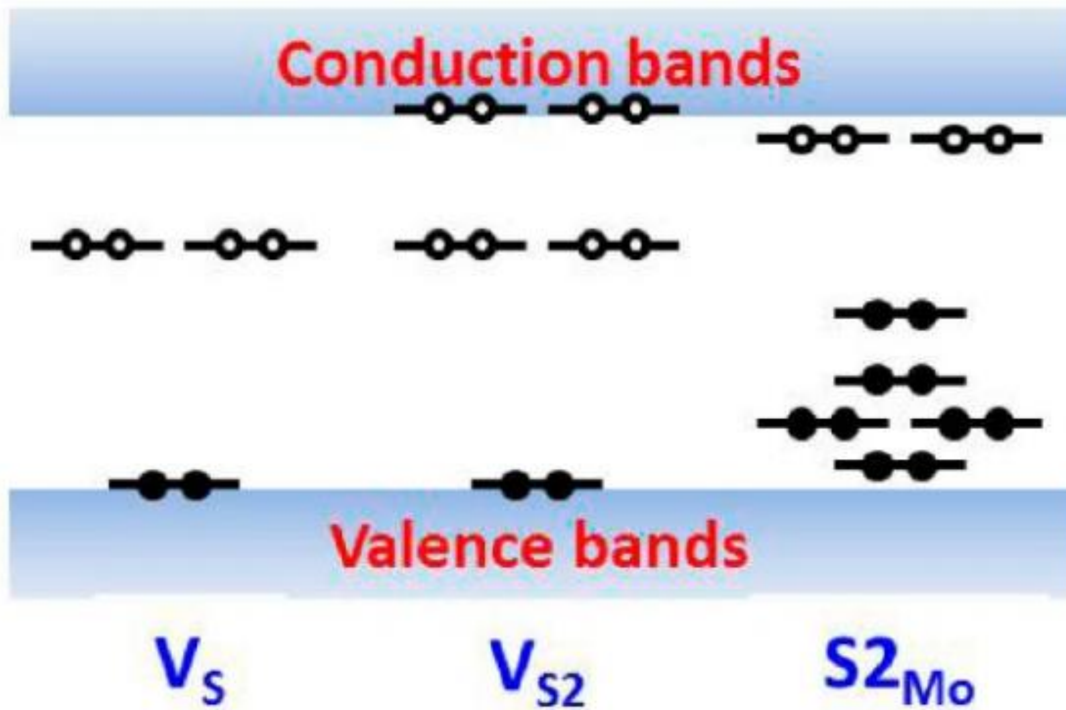

Fig. 1-19 Schematics to show defects states in MoS_2. [26]

Another origin for interface states in MoS_2 system is surface morphology induced states. 2D-materials are soft and can follow substrate surface well. However, conventional SiO_2/Si substrate is not atomic-scale flat and often introduce surface fluctuation as shown in **Fig. 1-20 (a)** [28]. MoS_2 on SiO_2/Si substrate is detected by scanning tunneling microscopy (STM). **Fig. 1-20 (b)** shows STS detected bandgap information. As we can see, on surface fluctuated substrate, MoS_2 band also fluctuates. This will introduce band-tail like interface states close to CB or VB. As a summary, MoS_2 still suffers from interface states issue even there are no dangling bonds ideally.

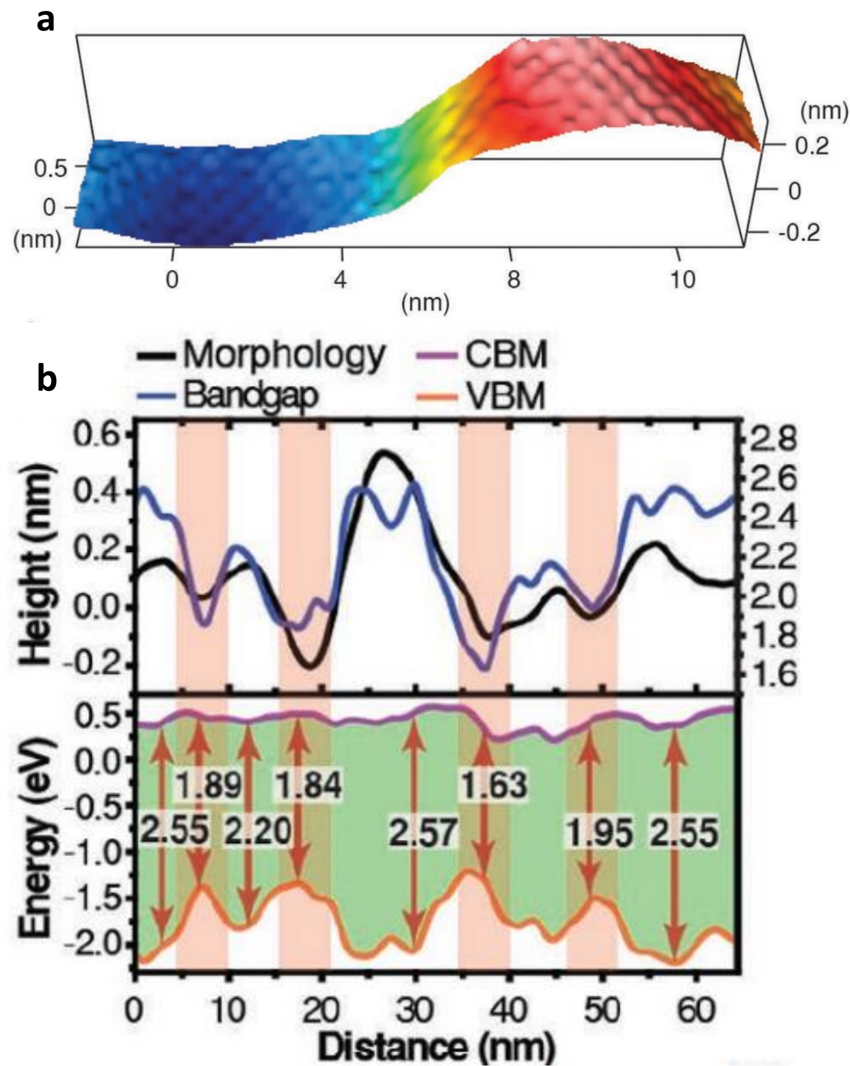

Fig. 1-20 (a) Schematics to substrate-induced surface fluctuation in MoS_2. **(b)** Line profile of height, CBM, VBM and band-gap by STS. [28]

1.7 Capacitance measurement principle relating to 2D

Electrical measurements are powerful tools to explore interfacial properties. Among them, capacitance measurement (*C*-*V*) brings many insights into interface states once the capacitance mechanism is fully understood. In this subchapter, capacitance measurement relating to 2D will be introduced.

1.7.1 Quantum capacitance

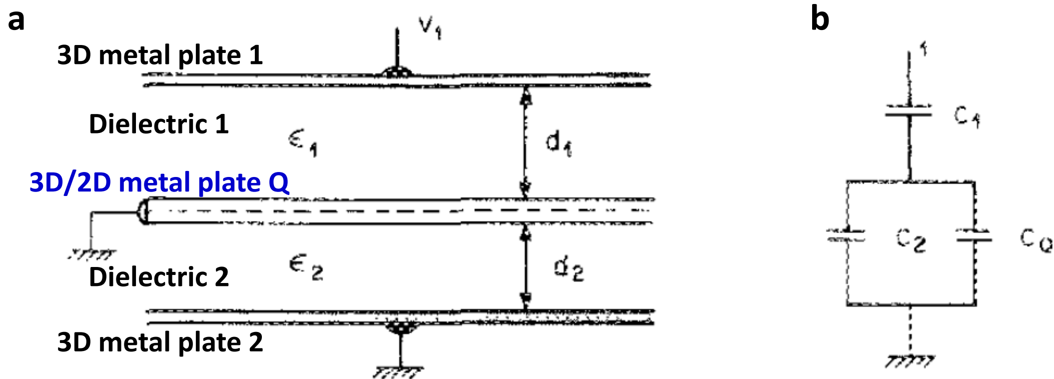

Fig. 1-21 (a) Schematics of a three-plate capacitor. Plate Q and plate 2 are grounded. **(b)** Equivalent circuit of the capacitor in **(a)**. [29]

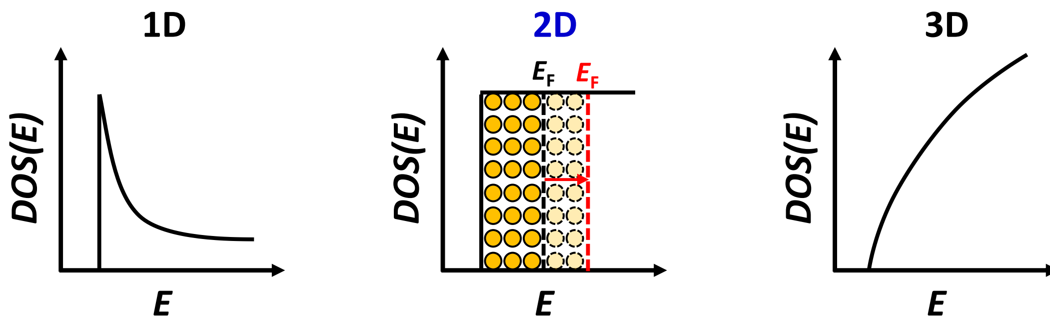

Fig. 1-22 *DOS* as a function of energy for different dimensions.

It is well known that a grounded metal plate can completely shield the electric field from one side into another. However, by reducing the dimension of the metal from 3D to 2D, the situation will be different.

Fig. 1-21 (a) shows the schematic illustration of a three-plate capacitor [29]. Two dielectrics (dielectric 1, 2) with dielectric constants of ε_1, ε_2 are separated by three metal plates (plate 1, Q, 2). Charges at plate 1, 2, Q are defined as σ_1, σ_2, and σ_Q, respectively. If the middle metal plate Q is the conventional 3D case, the applied voltage at top metal plate 1 (V_1) will induce the charges only at the top (1) and middle metal plates (Q). The electric field will also stop at plate Q. If the metal plate Q is the 2D case, the field due to the charges at plate 1 will penetrate through plate Q and induce charges on plate 2. The equivalent circuit to show this partial shielding of plate Q is shown in **Fig. 1-21**

(**b**). Here, C_1 and C_2 are the geometric capacitances:

$$C_i = \frac{\varepsilon_i}{4\pi d_i}.\ i = 1,2. \tag{1-2}$$

Quantum capacitance (C_Q) of 2D metal plate Q is related to the density of states (*DOS*). *DOS* as a function of energy (*E*) for different dimensions are shown in **Fig. 1-22**. For 2D case, $DOS_{2D} = g_v m/\pi\hbar^2$. m is the effective electron mass and g_v is the valley degeneracy factor. Based on the Pauli principle, extra energy for inducing charges is needed, which increases Fermi energy (E_F). The potential at the 2D metal is defined as V_{ch}. Based on the definition of capacitance that $C_Q = -\partial\sigma_Q / \partial V_{ch}$, the energy distribution of *DOS* (**Fig. 1-22**), and $e\partial V_{ch} = \partial E$, we can extract the C_Q as follows:

$$C_Q = e^2 \times DOS = \frac{g_v m e^2}{\pi\hbar^2}. \tag{1-3}$$

Based on the equivalent circuit as shown in **Fig. 1-21 (b)**, σ_2, and σ_Q can be shown:

$$\sigma_2 = -\sigma_1\left(\frac{C_2}{C_2 + C_Q}\right),\quad \sigma_Q = -\sigma_1\left(\frac{C_Q}{C_2 + C_Q}\right). \tag{1-4}$$

It indicates that $C_Q \gg C_2$ will result in $\sigma_Q \gg \sigma_2$, which is the conventional case of full shielding. However, when m is small, $C_Q \sim C_2$, and $\sigma_Q \sim \sigma_2$. Thus this partial shielding effect will be important in high-mobility devices.

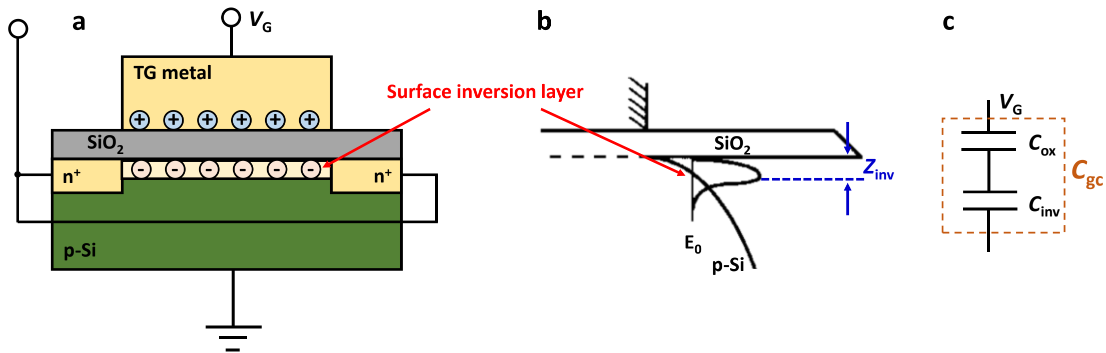

Fig. 1-23 (a) Schematic of inversion layer in MOSFET. **(b)** Band diagram of this system. **(c)** Equivalent circuit of this system. [30]

One of the most widely studied 2D metal comes from the surface strong inversion region in silicon under the MOSFET system [30, 31]. **Fig. 1-23** shows the schematic of

n-channel MOSFET. By applying the large positive gate voltage (V_G), an inversion layer will be formed at the surface, which is filled by electrons. This surface inversion layer is thin compared with p-type bulk Si. The band diagram of the inversion layer region is shown in **Fig. 1-23 (b)**. The electrons are confined in the triangle potential well caused by the strong band bending from the gate voltage. The electrons are then quantized to form subbands, which shows 2DEG (two-dimensional electron gas) behavior. The wave function of the lowest subband is shown in **Fig. 1-23 (b)**, in which most of the electrons locate. Due to quantum mechanics, the wave function has the distance from the interface. This distance between the centroid of the wave function and the interface is defined as Z_{inv}. By following **Fig. 1-21 (b)** with neglecting the back dielectric, the equivalent circuit of gate to source/drain capacitance (C_{gc}) to this system is shown as C_{ox} and C_{inv} in series as shown in **Fig. 1-23 (c)**. C_{gc} can be shown as follows,

$$\frac{1}{C_{gc}} = \frac{1}{C_{ox}} + \frac{1}{C_{inv}} = \frac{1}{C_{ox}} + \frac{1}{C_{inv}^{DOS}} + \frac{1}{C_{inv}^{thickness}}, \text{ where } \frac{1}{C_{inv}^{thickness}} = \frac{Z_{inv}}{\varepsilon_{Si}}. \quad (1\text{-}5)$$

C_{inv}^{DOS} has the same origin as C_Q in Eq. (1-3). While $C_{inv}^{thickness}$ comes from the electron distribution in the inversion layer. **Fig. 1-24** shows schematic and experimentally measured C_{inv}, which clearly shows two regions. [30] Lower region is dominated by C_{inv}^{DOS} and higher region is dominated by $C_{inv}^{thickness}$.

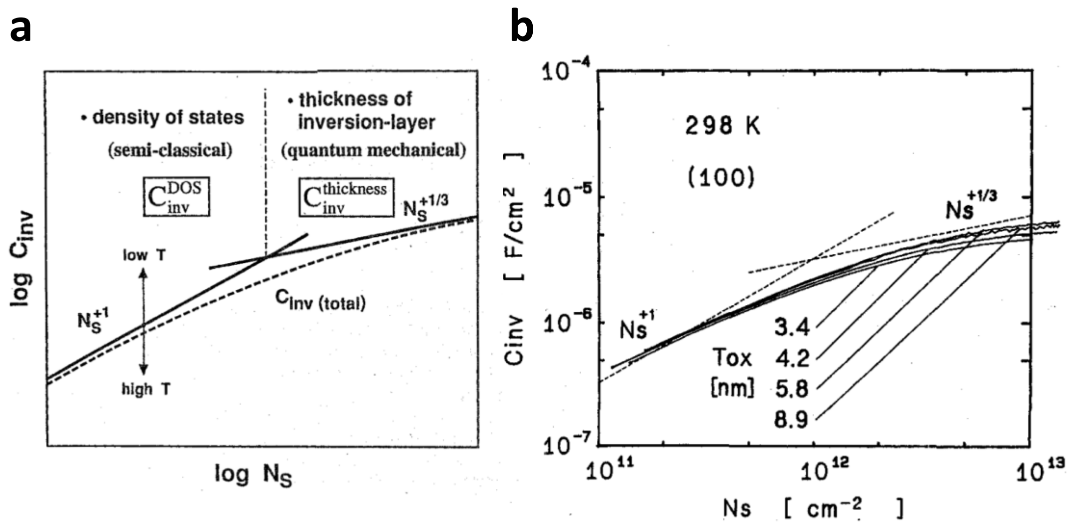

Fig. 1-24 (a) Schematic diagram of C_{inv} as a function of N_s (surface electron concentration) in MOSFET. **(b)** Experimental measured C_{inv} as a function of N_s. [30]

1.7.2 Capacitance of MOS capacitor and MOSFET

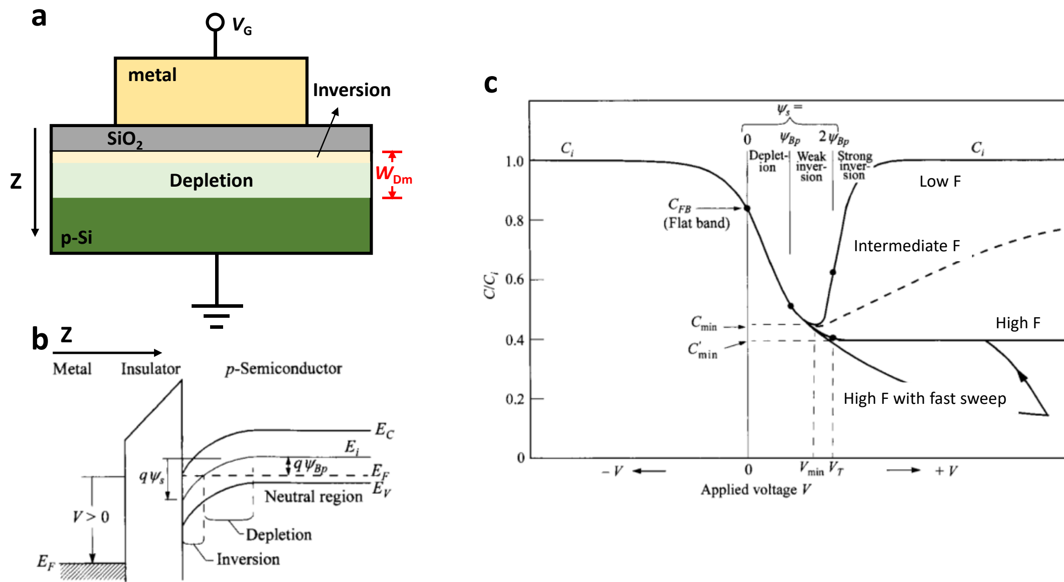

Fig. 1-25 (a) Schematic of p-Si/SiO_2 capacitor under strong inversion region. **(b)** Band diagram under strong inversion region. **(c)** Capacitor C-V curves at different frequency (F). [2]

The MOS capacitor has been widely studied in terms of capacitance measurement. The simple form is shown in **Fig. 1-25**, which has p-type Si substrate with SiO_2 dielectric. Capacitance is measured between top metal and back substrate. At low-frequency case, by applying negative V_G, Si is accumulated of holes. By applying positive V_G, Si is depleted. By applying large positive V_G, the inversion layer is formed at the surface. Depletion width maximum (W_{Dm}) is obtained in this case. The thickness of the measured Si substrate is always larger than W_{Dm}. The detailed analysis can be found in the text book[2].

Inversion capacitance has frequency dependence, which comes from the time constant of minority carriers[32]. The minority carriers in MOS capacitor structure are supplied by back contact as shown in **Fig. 1-28**. Minority carrier electron and majority carrier hole are generated through trap site at the depletion region. Electron drifts to the inversion layer while hole drifts/diffuses to the back contact. At room temperature, it is usually the generation process that determines the total time constant of minority

carriers.

The MOSFET structure is also studied in terms of capacitance measurement, which was firstly proposed by Koomen to study interface states [33]. **Fig. 1-26** shows two configurations of capacitance measurement based on *n*-channel MOSFET. Gate to channel capacitance (C_{GC}) consists of source/drain capacitance (C_{GS}+C_{GD}), which is measured in **Fig. 1-26 (a)**. C_{GC} focuses on inversion capacitance and the minority carriers are supplied by source/drain contact, which is different from MOS capacitor structure. C_{GC} directly indicates the mobile channel charge density, which was then developed to mobility measurements [34]. Gate to substrate capacitance (C_{GB}) is measured as shown in **Fig. 1-26 (b)**. C_{GB} focuses on accumulation/depletion capacitance and the majority carriers are supplied by the back substrate. **Fig. 1-26 (C)** shows measured C_{GC} and C_{GB} at low frequency. As we can see, the total capacitance of these two capacitances reproduces the *C-V* curve of MOS capacitor at low frequency as shown in **Fig. 1-25 (c).**

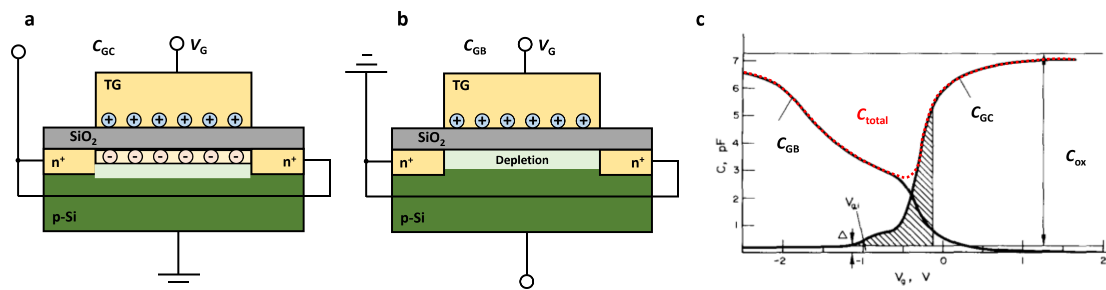

Fig. 1-26 Configuration of **(a)** C_{GC}, **(b)** C_{GB} measurement in *n*-channel MOSFET. **(c)** Experimental *C-V* curves of MOSFET at low frequency. [33]

Measured minority carriers based C_{GC} also depends on the frequency. As shown in **Fig. 1-27**, by increasing the frequency, C_{GC} decreases. The origin of inversion capacitance frequency dependence in MOSFET and MOS capacitor are different as shown in **Fig. 1-28**. In MOS capacitor structure, the dominant process is the electron/hole pair generation through the trap site. Generated carriers at the trap site usually only drift of several nanometers to reach the inversion layer. While in MOSFET

structure, electrons are supplied by the source/drain. These minority carriers have to drift for a long distance with the maximum value equals to half of the gate length, which is usually several microns. This minority carrier drift process is the dominant process in MOSFET structure to determine the minority carrier time constant. This consideration is also important in 2D-FET *C-V* analysis, which will be shown later.

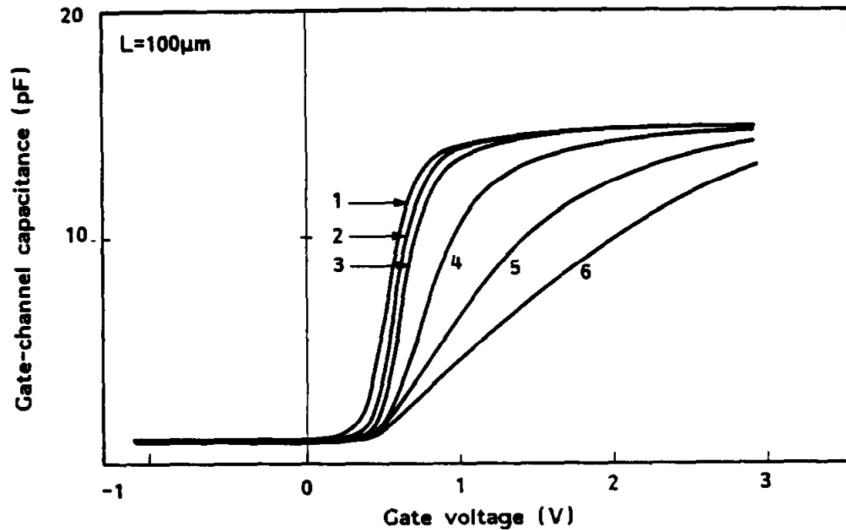

Fig. 1-27 Measured gate to channel capacitance $C_{GC} - V$ curves at frequencies of (1) 5kHz, (2) 100kHz, (3) 500kHz, (4) 2 MHz (5) 5 MHz, (6) 10 MHz, respectively. [33]

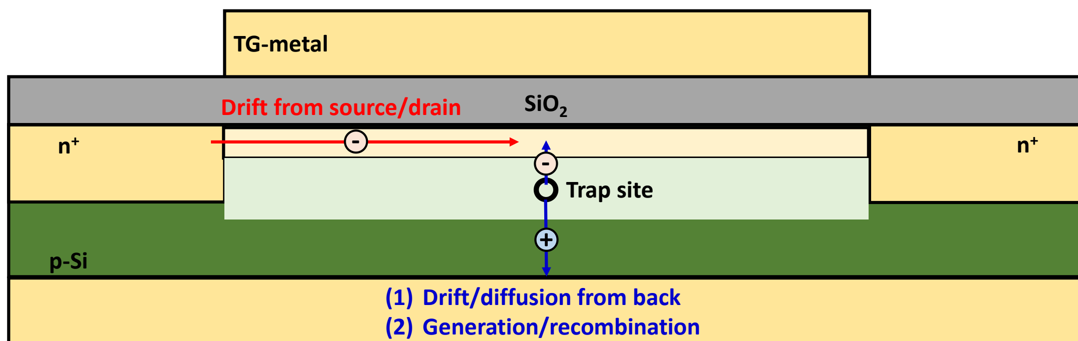

Fig. 1-28 Schematic to show the origin of minority time constant in MOSFET (red) and MOS capacitor (blue) structure, respectively.

1.7.3 Capacitance of MoS_2

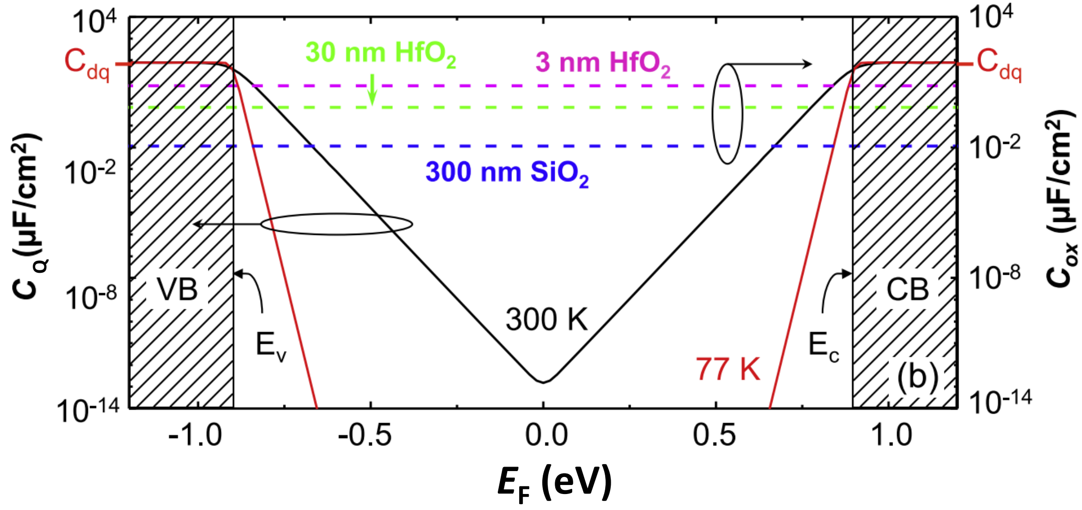

Fig. 1-29 Theoretical C_Q as a function of Fermi energy of monolayer MoS_2 channel at 77 and 300 K. [35]

In subchapter 1.7.1, the quantum capacitance of 2DEG has been introduced based on Si inversion capacitance. For monolayer MoS_2, due to the thickness confinement effect, it should show the intrinsic 2DEG property even without applying an electrical field.

Fig. 1-29 shows theoretically calculated C_Q of monolayer MoS_2 at different temperatures [35]. At 0 K, $C_Q = e^2 DOS_{2D}$ as shown in subchapter 1.7.1. While at high temperatures, C_Q will deviate from it due to the Fermi-Dirac distribution. At present, only monolayer MoS_2 C_Q has been reported. Thickness dependence of C_Q of MoS_2 has not been studied yet.

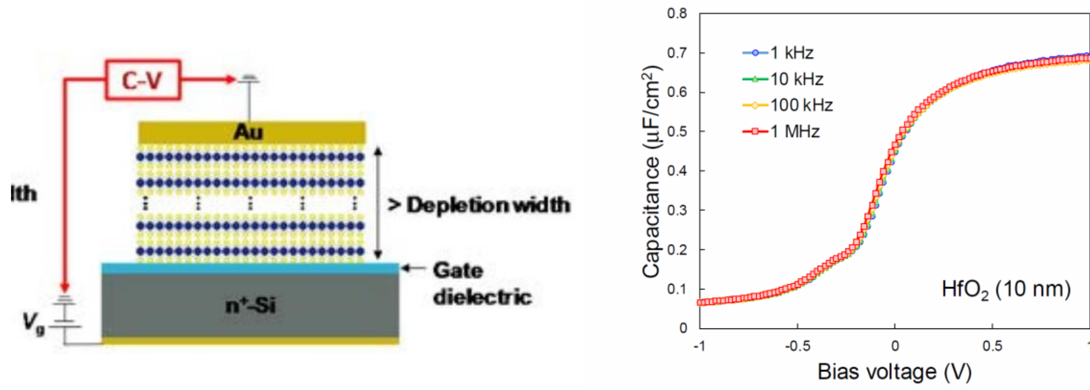

Fig. 1-30 Capacitance in bulk MoS_2/HfO_2/metal capacitor. MoS_2 thickness > W_{Dm}. [36]

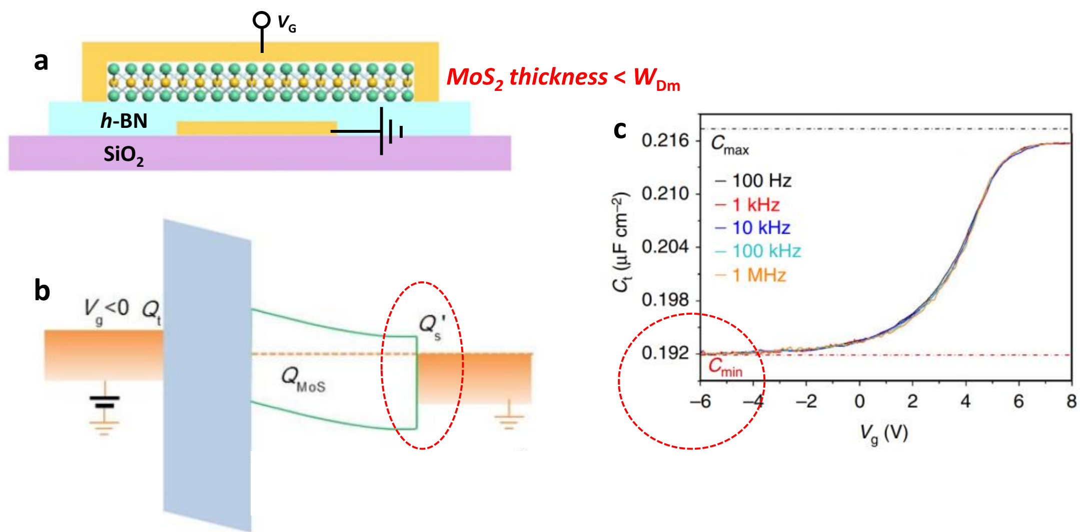

Fig. 1-31 (a) Schematic of thin MoS_2/*h*-BN/metal MOS capacitor structure. MoS_2 thickness < W_{Dm}. **(b)** Schematic band diagram of MoS_2/*h*-BN/metal at depletion region. Red circle indicates the back contact effect of channel potential distribution. **(c)** Experimental measured *C*-*V* curve. [37]

Experimentally, capacitance in MoS_2 has been measured based on both capacitor and FET structure. For capacitor structure, when MoS_2 thickness is larger than W_{Dm}, the conventional *C*-*V* curve is observed as shown in **Fig. 1-30**. [36] When MoS_2 thickness is smaller than W_{Dm}, back contact metal is important to determine the channel potential distribution as shown in **Fig. 1-31**. *C*-*V* curve shows a small modulated range with large minimum capacitance (C_{min}). In this case, the whole MoS_2 channel cannot be fully depleted due to the back metal contact. As a result, *C*-*V* curve from capacitor

structure just includes limited information excluding the full-depletion region.

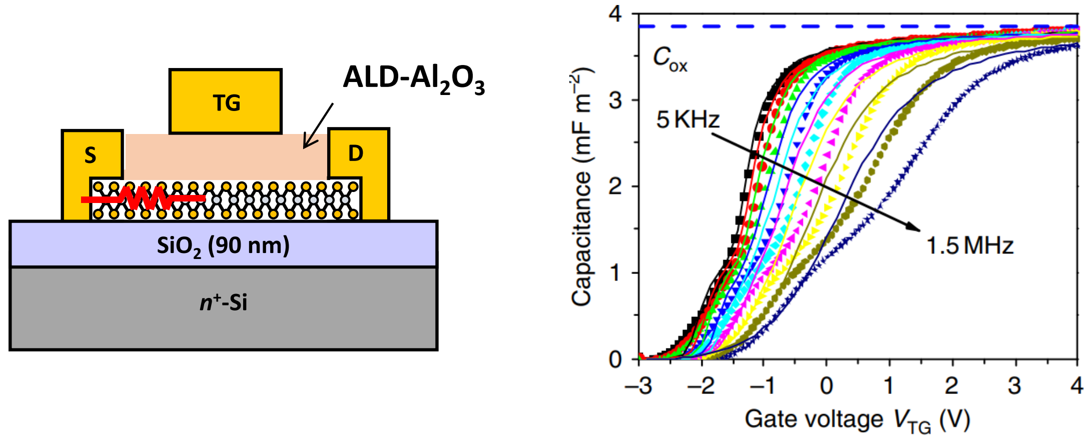

Fig. 1-32 Capacitance in monolayer MoS_2 FET structure. [39]

For FET structure, the channel can be fully depleted in ultra-thin MoS_2 [38,39]. **Fig. 1-32** shows an experimental gate to source/drain *C-V* curve in CVD monolayer MoS_2 FET structure. Compared to **Fig. 1-31 (c)**, *C-V* curve in FET structure goes to almost zero at the depletion region due to no back contact. Therefore, the capacitance in FET structure can be understood based on the theoretical calculation in **Fig. 1-29**. However, due to lack of consideration of the interface trap capacitance ($C_{it} = e^2D_{it}$) and channel resistance effects (similar consideration of minority carrier time constant of MOSFET structure in subchapter 1.7.2 & **Fig. 1-27**), C_Q in monolayer MoS_2 FET has neither been measured nor fitted well experimentally. Moreover, the large frequency dispersion is observed in **Fig. 1-32** compared with **Fig. 1-31**. This frequency dispersion could be due to the channel resistance, which is similar to the frequency dispersion in MOSFET *C-V* as shown in subchapter 1.7.2.

1.8 Measured D_{it} in MoS_2

Even though the mechanism of *C-V* of ultra-thin MoS_2 FET is still unclear, D_{it} has been extracted from *C-V* based on conventional analysis method for silicon from many reports. Extracted D_{it} from both *C-V* and *S.S.* for MoS_2 are summarized in **Fig. 1-33**.

Si(100) D_{it} is shown here for comparison[40]. At present, the only reliable D_{it} energy distribution comes from *C-V* of bulk MoS_2 capacitor by Terman method [36]. As for ultra-thin MoS_2 FET, due to lacking knowledge of C_Q, extracted D_{it} from *C-V* only shows value range but no energy distribution. Moreover, D_{it} extracted from *C-V* shows large variation and deviation, which questions the validity of the existing extraction method again. This could be due to parasitic capacitance and resistance effect. Therefore, in this study, we will build the more reliable D_{it} extraction method based on both *I-V* and *C-V* in order to study intrinsic MoS_2/high-*k* interface.

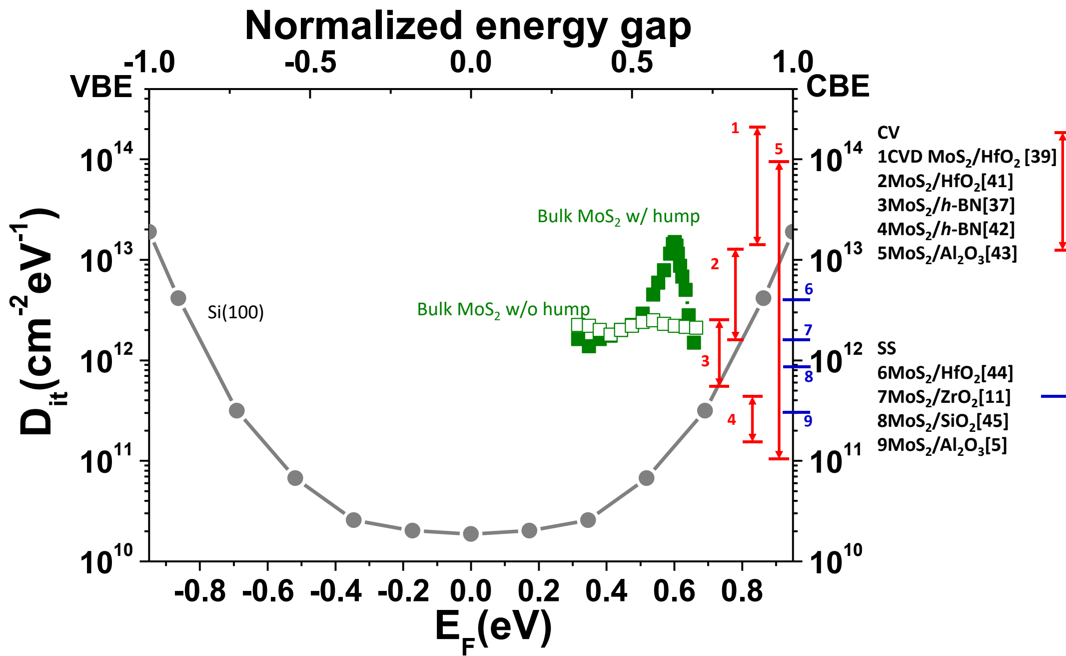

Fig. 1-33 Summarized D_{it} – energy distribution of MoS_2.

1.9 Objectives and organizations of this study

Based on the significance and current issues of 2D-FET, the objective of this study is proposed as follows:

1) To clarify the operation mechanism of MoS_2-FET.
2) To systematically investigate *C-V* characterization of MoS_2-FET structure.
3) To study full energy range of MoS_2/high-*k* interface based on both *n*-type and *p*-

type MoS_2.

4) To propose the thickness scaling rule in most of 2D-FET and summarize 2D crystal qualities.

This study are written in five chapters corresponding to the four main objectives:

In chapter 2, the key issues in device fabrication process of high-quality MoS_2 dual-gate FET are demonstrated. The operation mechanism of 2D-FET is discussed based on *I*-*V* characterization. ACCU-FET operation mechanism is proposed and developed to explain the observed behavior.

In chapter 3, *C*-*V* characterization of MoS_2 FET structure is systematically studied. Parasitic capacitance is totally removed by using insulating quartz substrate. Resistance effect is carefully checked, which is one of the main origin for observed frequency dispersion in fully-depleted region of MoS_2 FET. Quantum-mechanical effect is also investigated from monolayer to bulk MoS_2.

In chapter 4, D_{it} energy distribution is extracted at conduction band side by both *I*-*V* and *C*-*V* for *n*-type MoS_2. The origin of D_{it} is also investigated. D_{it} peaks in low quality samples for both monolayer and bulk MoS_2 are attributed to the sulfur vacancies. While band-tail shape D_{it} close to CB is attributed to Mo-S bond bending due to the strain caused by the high-*k* deposition and/or the surface roughness of the SiO_2 surface. Metal-insulator-transition (MIT) behavior is successfully explained in terms of device physics by considering temperature dependence of C_Q and band-tail shape C_{it}.

In chapter 5, D_{it} energy distribution is extracted at valance band side for Nb-doped *p*-type MoS_2. The quality of *p*-type MoS_2 crystal is confirmed by Raman and PL. Several interesting phenomena are also found. One is surface electron accumulation in *p*-type MoS_2. Another one is the asymmetry between electron and hole transport.

In chapter 6, WSe_2 FET is investigated. Thickness scaling rule for most of 2D-FET is proposed based on the findings in chapter 2-5. 2D crystal qualities are also summarized.

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2 *I-V* characterization of MoS_2 ACCU-FET

In this chapter, details of device fabrication will be presented. The key issue towards high-quality MoS_2/ high-*k* interface will be introduced. *I-V* characterization will be mainly discussed based on the fabricated dual-gate FET. Based on the observed *I-V* behaviors, accumulation-mode FET will be proposed.

2.1 Device fabrication

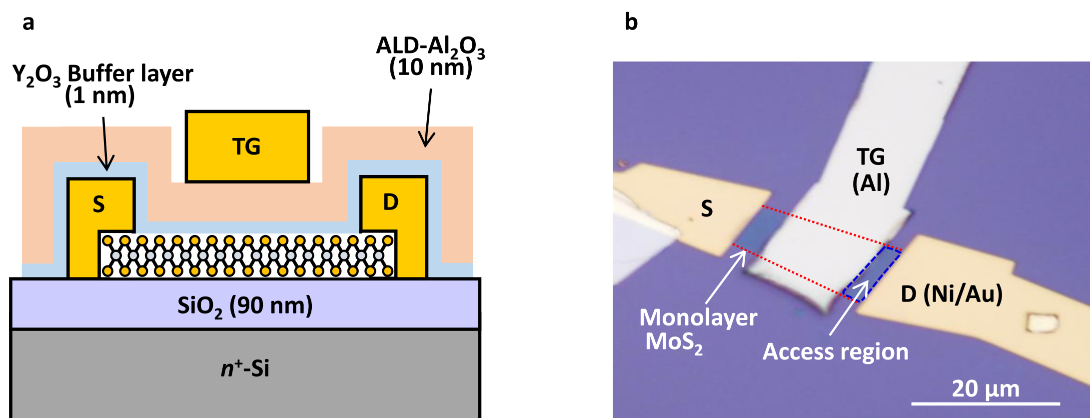

Fig. 2-1 **(a)** Schematic and **(b)** optical image of the device on n^+-Si/SiO_2 substrate. The access region refers to the channel region uncovered by the top gate electrode. S, D and TG indicate the source, drain and top gate electrodes, respectively.

The optical image of fabricated dual-gate MoS_2 FET is shown in **Fig. 2-1**. MoS_2 thin flake was mechanically exfoliated on Si/90 nm-SiO_2 substrate from natural MoS_2 crystal. Ni/Au was thermal evaporated for source/drain contact. The sample was annealing at 200 °C for 20 min. Then, 1-nm Y metal was deposited via thermal evaporation at an Ar atmosphere of 10^{-1} Pa partial pressure, followed by oxidization at atmosphere to form buffer layer. The 10-nm Al_2O_3 oxide layer was deposited by atomic layer deposition (ALD) before the Al top gate electrode formation. *I-V* and *C-V* measurement were performed in vacuum.

2.2 Buffer layer deposition & ALD

ALD is one of the widely used deposition mehtod for high-*k* on 2D materials[1-3]. However, it suffurs from nuclearation difficulties because 2D surface is usually inert. Although most TMDCs have defects inside, it is still not enough to form high-quality dielectic layer by direct ALD process. Buffer layer deposition is one of the widely used method to overcome this problem. As mentioned in the last subchapter, we used Y as buffer layer metal. There are two main reasons why we choose Y as buffer layer metal.

One reason is the easy oxidization of Y. **Fig. 2-2** shows calculated Gibbs energy for various metals. As we can see, Y has lowest Gibbs energy, which enables us to easily oxidize it at room temperature in atmosphosure.

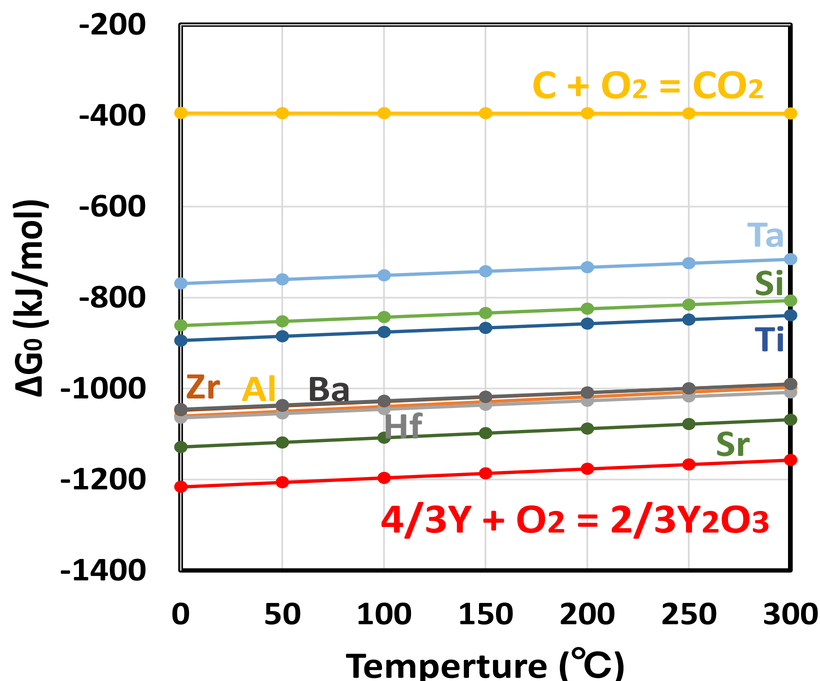

Fig. 2-2 Calculated Gibbs energy for various metals.

Another reason is the good wettability of Y. **Fig. 2-3** shows TEM images of Ti, Ni, Pd, Au, Al and Fe coating on carbon nanotubes with a thickness of 15 nm [4]. As we can see, Al clearly shows poor coating property and high discontinuity. While Ti shows uniform and continuous coating. However, the oxidization of Ti will form TiO_x, which

is conducting. Y also has good coating, which is comparable with Ti. This explains why we use Y as buffer metal.

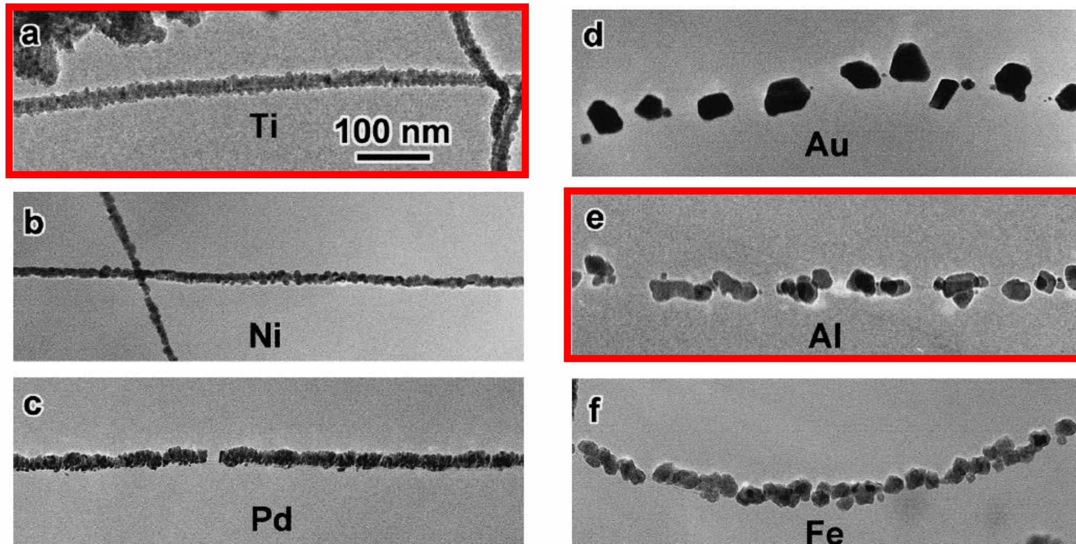

Fig. 2-3 TEM images of Ti, Ni, Pd, Au, Al and Fe coating on carbon nanotubes with a thickness of 15 nm. [4]

In order to further prevent defects formation during Y deposition process, Y was deposited at an Ar atmosphere of 10^{-1} Pa partial pressure as shown in **Fig. 2-4**. The mean free path and energy of Y atoms are reduced, which protects MoS_2 from the deposition process. Thanks to the Y deposition via thermal evaporation at an Ar atmosphere of 10^{-1} Pa partial pressure, the high-quality MoS_2 flakes are preserved during the buffer layer deposition process.

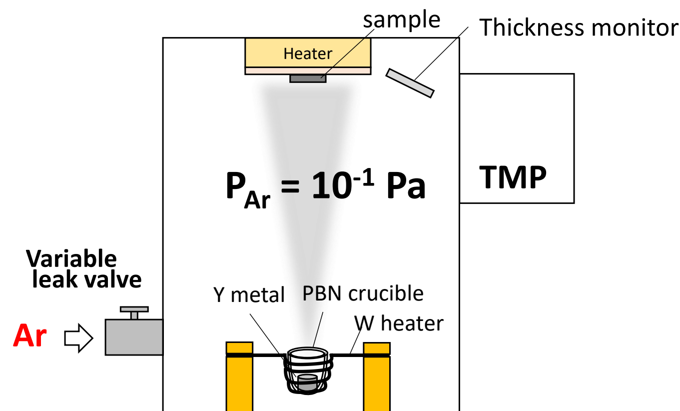

Fig. 2-4 Schematic to show Y deposition at an Ar atmosphere.

ALD is conducted for Al_2O_3 after the buffer layer deposition process. Hot wall type ALD was used. The precursor is trimethylaluminum (TMA). The growth temperature is 200 °C. The flow of one cycle of ALD is shown in **Fig. 2-5**. Firstly, the substrate is exposed to TMA. TMA reacts with surface OH- radical. The N_2 gas is then introduced into the chamber to flow away the remaining TMA molecules. Water is then introduced to react with TMA, forming OH- radical again. N_2 gas is again used to flow away water to return to the initial stage. This is called one cycle. By repeating cycles, the Al_2O_3 film is grown. 10 nm-thick Al_2O_3 needs 90 cycles and 30 nm-thick Al_2O_3 needs 300 cycles. I have to mention that no additional annealing was performed after the ALD in order to preserve high-quality MoS_2/high-*k* interface.

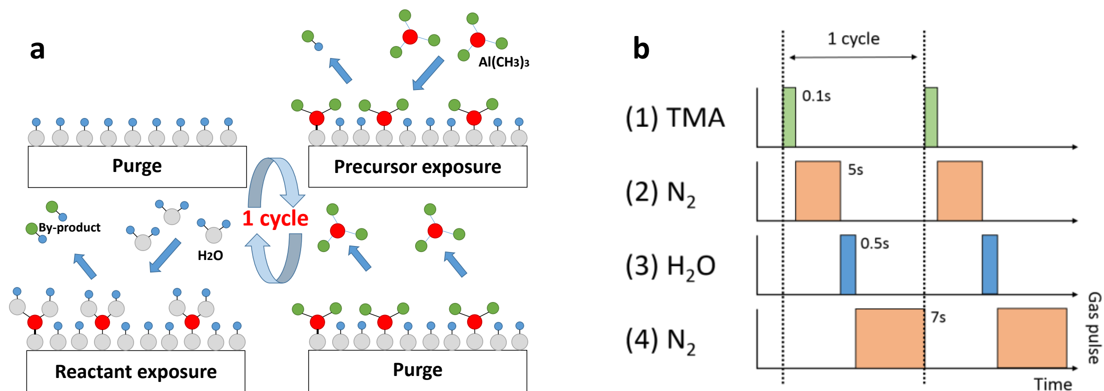

Fig. 2-5 (a) Flow of one cycle of ALD. **(b)** Parameters in one cycle.

2.3 Schottky barrier FET vs accumulation mode FET

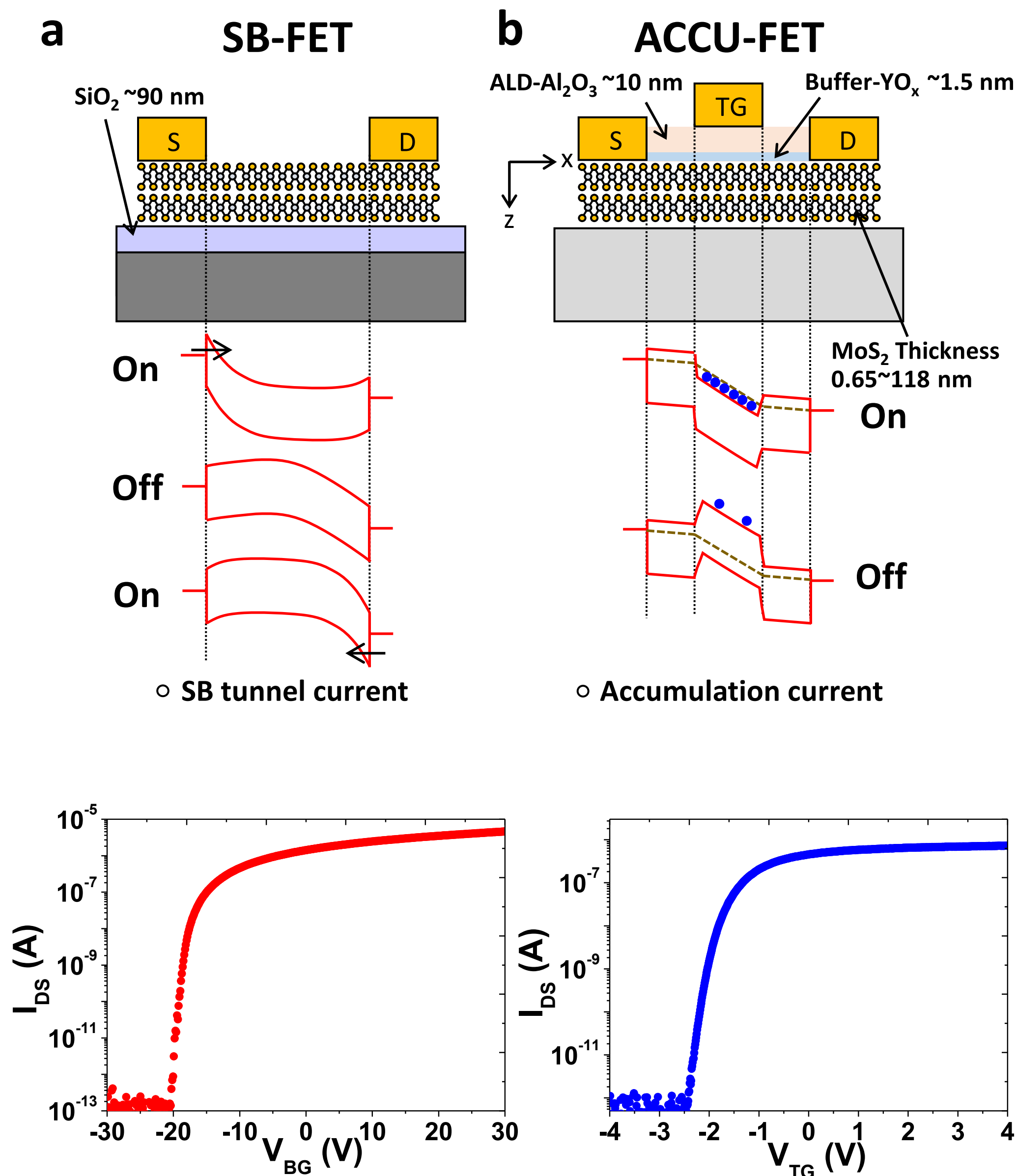

Fig. 2-6 (a) Schematic and *I*-*V* curve of a back-gate SB-FET. Band diagrams of the *n*-branch, off state, and *p*-branch are shown below. **(b)** Schematic and *I*-*V* curve of a top-gate ACCU-FET. Band diagrams of the accumulation and depletion states are shown below.

I-*V* characterization is conducted for fabricated MoS_2 FET. An accurate understanding of the operation mechanism of 2D-FETs is critical because the extraction of physical properties and the further control of the device characteristics are based on

the operation mode. Typical back-gate or fully top-gate TMDC-FET devices could possess the Schottky barrier at metal/TMDC interface, as shown in **Fig. 2-6 (a)** [5-8]. **Fig. 2-6 (b)** shows partial top-gate FETs with ohmic metallic contacts, where the 2D/metal contact is not modulated. This type of device structure is often explained by ACCU-FETs in a Si nanowire [9], where the partial gate controls the on and off states via accumulation and depletion for the majority carriers. Interestingly, the similar I_D-V_G curve is still observed even the device structure is very different. The existence of access region guarantees that I-V of top-gate MoS_2 FET can be explained by accumulation mode. The question turns to be that what is the dominant mechanism in other FETs with different structures such as back-gate case?

2.3.1 Operation mechanism study by local top-gate MoS_2 FET

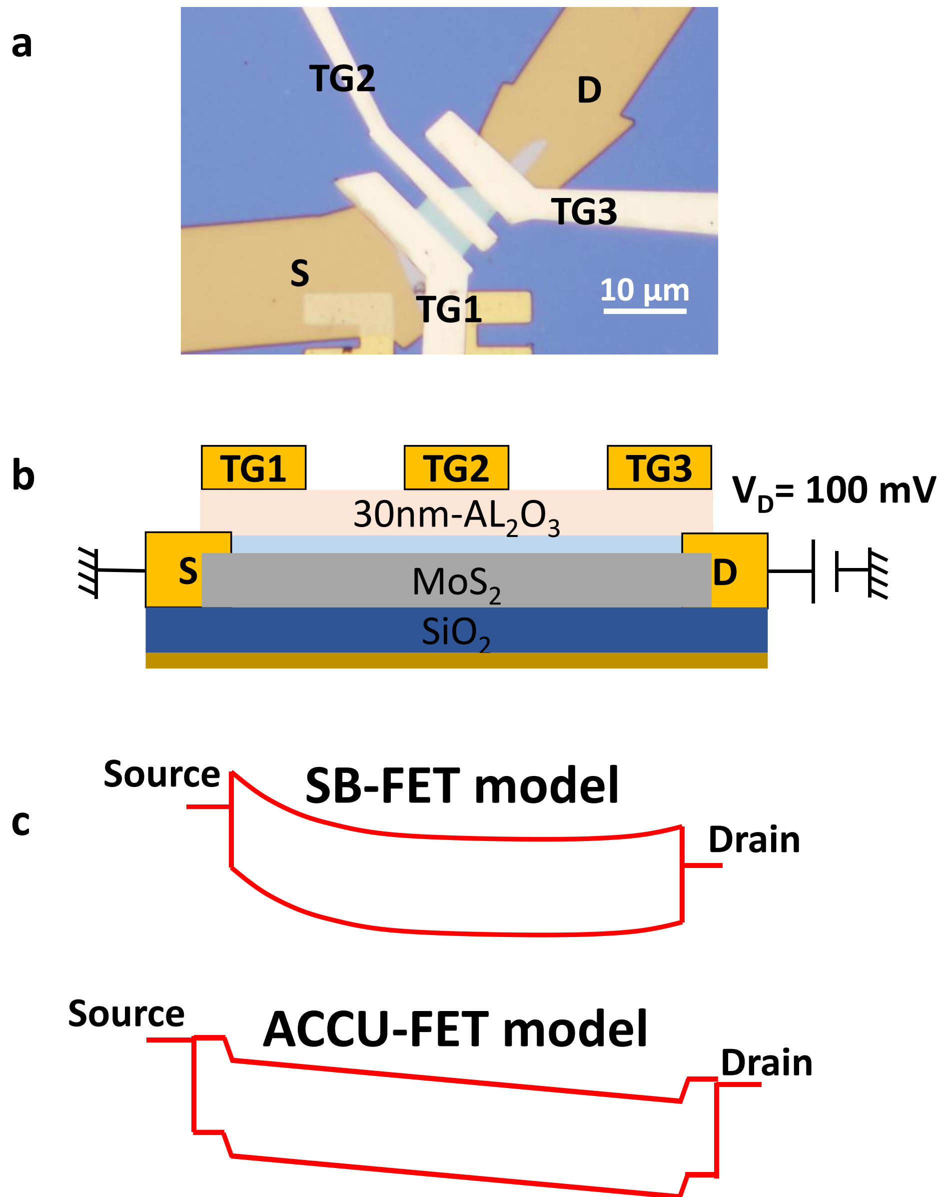

Fig. 2-7 **(a)** Optical image and **(b)** schematic of the local-gate device on n^+-Si/SiO_2 substrate. MoS_2 thickness is of ~ 10 nm. **(c)** Band diagrams of MoS_2 channel based on SB-FET model and ACCU-FET model, respectively.

In order to clarify the operation mechanism more clearly, the dual-gate MoS_2 FET with global back-gate and local top-gate was fabricated as shown in **Fig. 2-7 (a,b)**. As for back-gate, it modulates both the channel and contact region simultaneously. As for top-gate, three local-electrodes were prepared, which are defined as TG1, TG2, and

TG3, respectively. TG1 modulates the source contact and the nearby channel. TG2 only modulates the channel. TG3 modulates the drain contact and the nearby channel.

Band diagrams of MoS_2 channel based on both SB-FET model and ACCU-FET model are shown in **Fig. 2-7 (c)**. I_{DS}-V_{TG} characteristics from three different local top-gate are first discussed. As for SB-FET model, SB at source contact controls the current into the channel. It means that by modulating TG1, characteristic of SB-FET is expected. In the case of TG2, only the channel is modulated, which is not important in SB-FET model. In the case of TG3, SB at the drain is also not so important compared with that at the source. This means that characteristic from TG3, TG2 should be different from that of TG1. In a word, characteristics from three different local top-gate should be very different when SB-FET model is dominant. Expected schematic I_{DS}-V_{TG} characteristics of local top-gates based on SB-FET are shown in **Fig. 2-8 (a)**. As for ACCU-FET model, it is the channel carrier density that dominates the current. All these three local top-gates modulate channel. As a result, characteristics from three different local top-gate should be quite similar when ACCU-FET is dominant.

Experimental I_{DS}-V_{TG} characteristics of local top-gates are shown in **Fig. 2-8 (b)**. I_{DS}-V_{TG} curve from TG1 is quite similar with those from TG2, TG3, which confirms that operation mechanism is not SB-FET model but ACCU-FET model in the present structure. The slight I_{DS}-V_{TG} characteristics difference here comes from local channel interfaces difference. Another phenomenon that indicates ACCU-FET model is discussed in terms of I_{DS}-V_{BG} characteristics shown below.

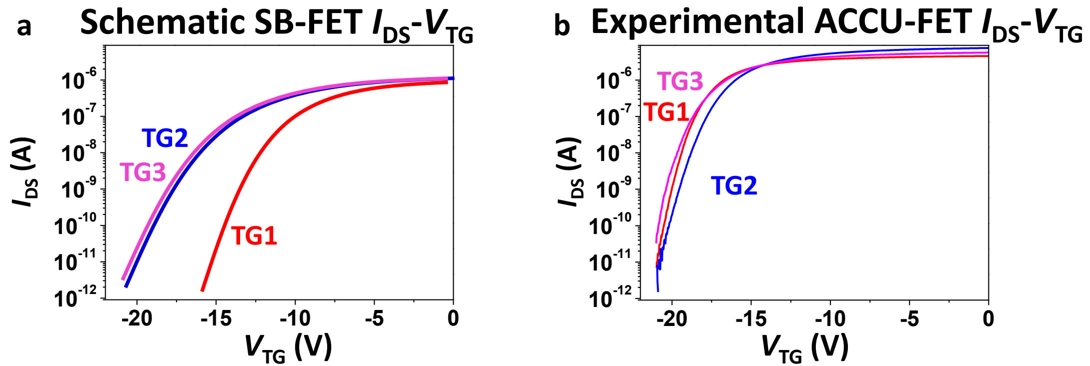

Fig. 2-8 (a) Expected schematic SB-FET model based I_{DS}-V_{TG} characteristics. **(b)** Experimental I_{DS}-V_{TG} characteristics, which shows ACCU-FET behavior.

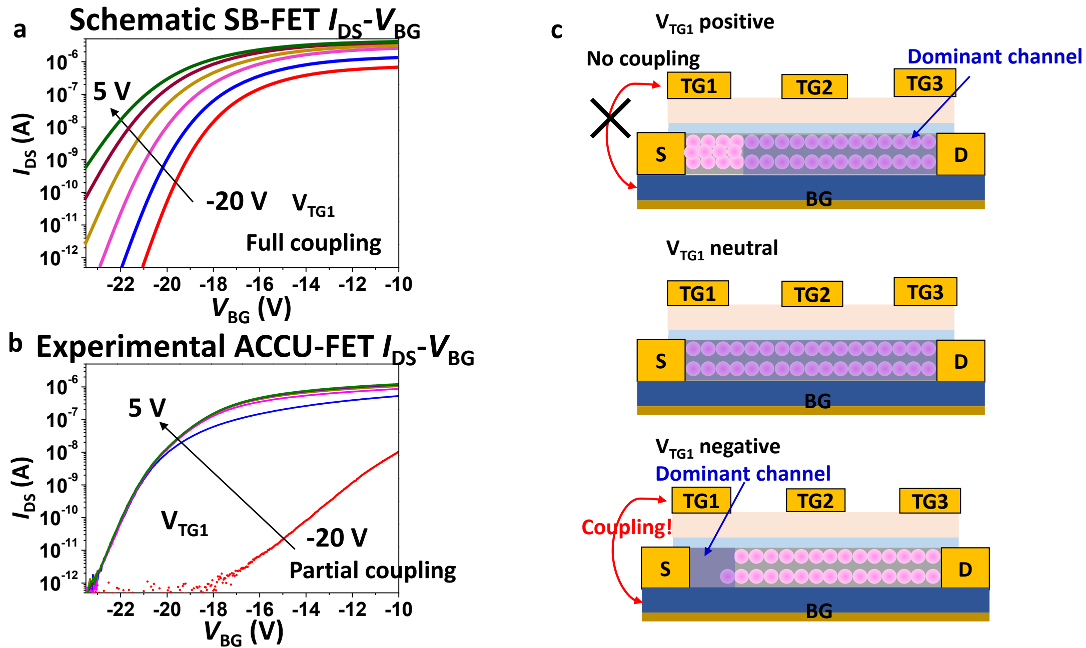

Fig. 2-9 (a) Expected schematic SB-FET model based I_{DS}-V_{BG} characteristics at different gate bias of V_{TG1}. **(b)** Experimental I_{DS}-V_{BG} characteristics at different gate bias of V_{TG1}. V_{TG1} has a range of -20 ~ 5 V with step of 5 V. **(c)** Schematic to explain partial coupling in **(b)**.

As for SB-FET, the current of I_{DS}-V_{BG} characteristics are determined by SB at source. By changing gate bias of TG1 (V_{TG1}), I_{DS}-V_{BG} curves should be modulated effectively. It should show full coupling between top-gate and back-gate as shown in **Fig. 2-9 (a)**. Experimental I_{DS}-V_{BG} characteristics at different V_{TG1} are shown in **Fig. 2-9 (b)**. V_{TG1} modulates I_{DS}-V_{BG} curves effectively only at -20 V, thus showing partial coupling behavior. This partial coupling behavior is explained in terms of ACCU-FET model as shown in **Fig. 2-9 (c)**. When V_{TG1} is positive, the local channel below TG1 is accumulated and become conductive. The total resistance from the source to drain is determined by the channel other than TG1 region. As a result, the total resistance is not modulated so much just by modulating high conductive TG1 region. When V_{TG1} is negative (-20 V), the local channel below it is depleted and become resistive. The total resistance from the source to drain is determined by the local channel at TG1 region. As a result, the total resistance is modulated effectively just by modulating high

resistive TG1 region. This partial coupling behavior again confirms the ACCU-FET model in present dual-gate MoS_2 FET.

2.3.2 Interpretation of *I-V* temperature dependence

Interpretation of temperature dependence of I_{DS}-V_G curves based on both ACCU-FET model and SB-FET model is studied in this subchapter. **Fig. 2-10** shows the temperature dependence of I_{DS}-V_{BG} curves from back-gate multilayer MoS_2 FET. I_{DS} decrease by decreasing temperatures at subthreshold region, which indicates the existence of a thermal barrier (E_B). Arrhenius plots are then drawn in **Fig. 2-10 (b)**. E_B is extracted from the slope in the region 1. In the deep subthreshold region, the temperature dependence is very large, which indicates large E_B. By increasing V_{BG}, E_B increases. This phenomenon can be explained by both SB-FET and ACCU-FET as shown in **Fig. 2-11**. As for electron transport, in SB-FET, E_B refers to the Schottky barrier between source metal and channel E_C. By applying large positive V_{BG}, the tunneling can be obtained, which results in the extremely small E_B. By applying negative V_{BG}, the E_C moves upwards, which results in the large E_B. In ACCU-FET, E_B refers to an intrinsic barrier between E_C and E_F. E_B is modulated by V_{BG} due to the modulation of E_F. Although both models can explain V_{BG} modulated E_B behavior, SB-FET cannot explain the existence of region 2 in **Fig. 2-10 (b)**. In region 2, the temperature dependence is reduced. This is widely discussed in graphene FET, which can be considered as the transition from band transport through conduction band to hopping transport through gap states [10,11]. The same scenario could also occur in MoS_2. This indicates that ACCU-FET model can be applied to the wider temperature range.

In subchapter 2.3.1, we have clarified that mechanically exfoliated MoS_2 from natural crystal shows ACCU-FET behavior in our fabricated top- and back-gate devices with Ni/Au contact. We have to emphasize that it is because our Ni contact is quite ideal, which does not restrict total resistance seriously. When large SB is formed at the contact,

it will restrict total current as shown in the schematic of **Fig. 2-12**. SB will seriously affect I_{DS}-V_G curve, especially at on-state because channel resistance is comparable with contact resistance at this region. This explains why temperature dependence of I_{DS}-V_G curve close to on-state could indicate SB height at contact [5-8]. However, SB-FET model can still not be applied to the whole current region even the contact has SB height. It is because at deep subthreshold region, channel resistance will again dominate total resistance, which results in ACCU restricted region. In a word, both SB-FET model and ACCU-FET model need to be considered when the contact is not optimized.

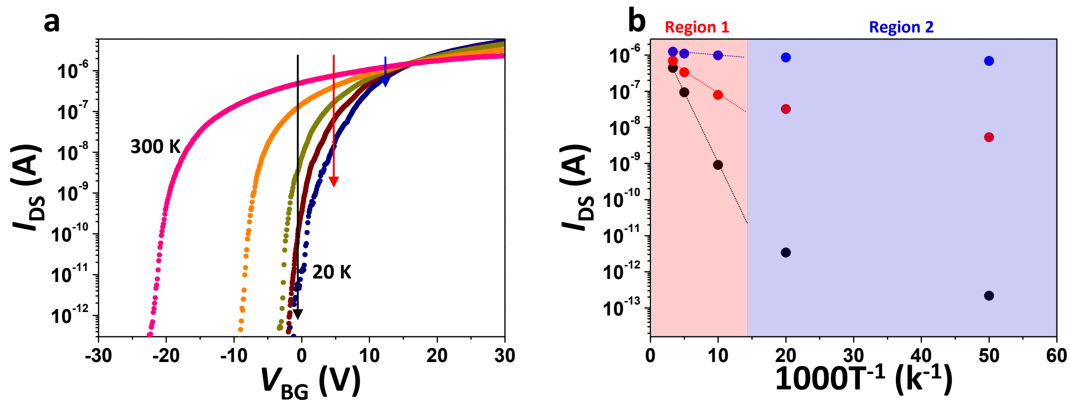

Fig. 2-10 (a) Transfer characteristics of a back-gate multilayer MoS_2 FET. Temperature steps are 300, 200, 100, 50, 20 K. V_{DS} = 0.11 V. **(b)** Arrhenius plots of I_{DS} at three different V_{BG}, which is indicated by arrows in **(a)**. Clear two regions are observed. Temperature dependence is large in region 1 and small in region 2.

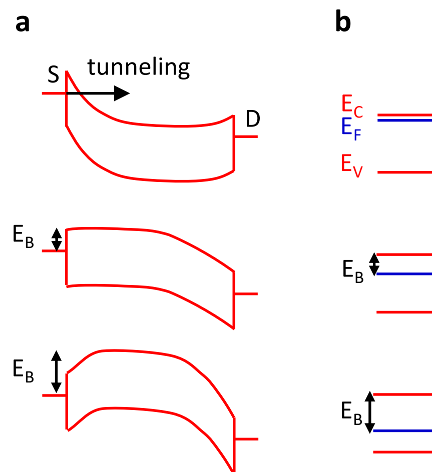

Fig. 2-11 Schematic to show V_{BG} modulated E_B in **(a)** SB-FET and **(b)** ACCU-FET.

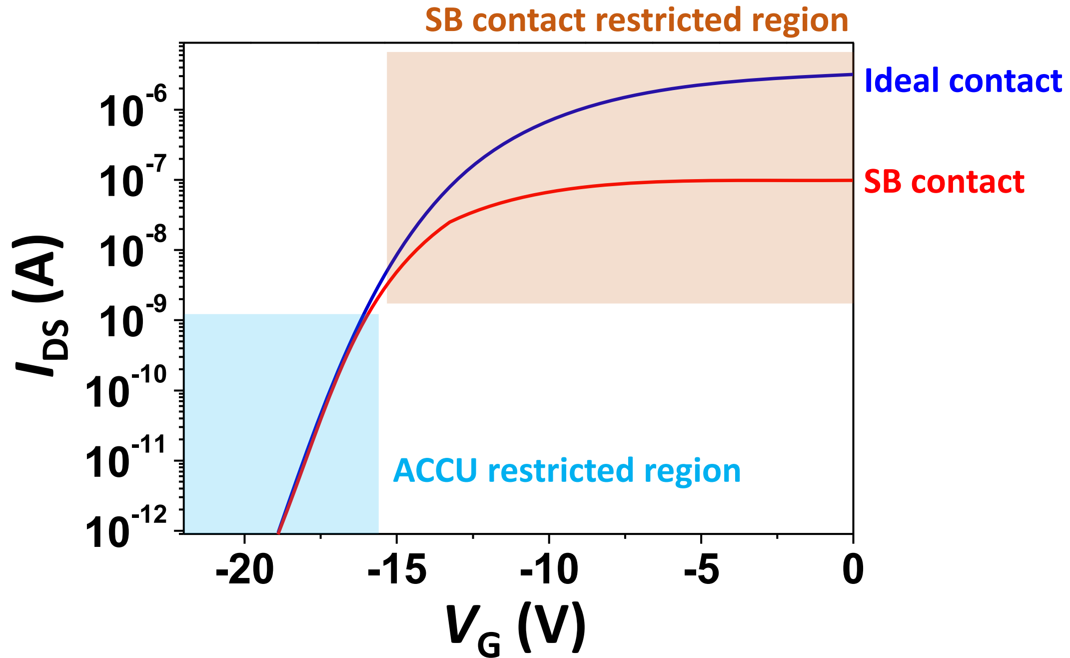

Fig. 2-12 Schematic to show how SB contact restricts I_{DS}-V_G curve.

2.3.3 Interpretation of *I-V* ambipolar behavior

Ambipolar behavior has been considered to be unique in SB-FET. However, ideally speaking, if there are no any junctions, we should obtain both *n*- and *p*-transport by modulating channel E_F. SB-FET mode just explains why SB at contact does not rectify current in the transistor structure. Since SB-FET is dominated by tunneling current from contact to channel while ACCU-FET is dominated by majority carrier transport process, it should be very different in *C-V* measurement. *C-V* mechanism is built based on carrier statistics in the channel instead of contact, which supports ACCU-FET. For example, theoretical C_Q also has both CB and VB side as shown in **Fig. 1-29**. Therefore, in the ideal ACCU-FET when no rectification occurs in the channel, *C-V* should also show ambipolar behavior. In partial top-gate ACCU-FET as shown in **Fig. 1-15** and **Fig. 2-6 (b)**, the back-to-back *p-n* junctions are formed in the channel, resulting in the unipolar behavior. However, in fabricated full dual-gate *p*-type MoS_2

FET ACCU-FET, we observed ambipolar behavior *C-V* as shown in **Fig. 2-13**. It clearly indicates that carrier density in the channel instead of tunneling current from contact that dominates *I-V* characterization. In other words, ACCU-FET can also show ambipolar behavior when no rectification occurs in the channel.

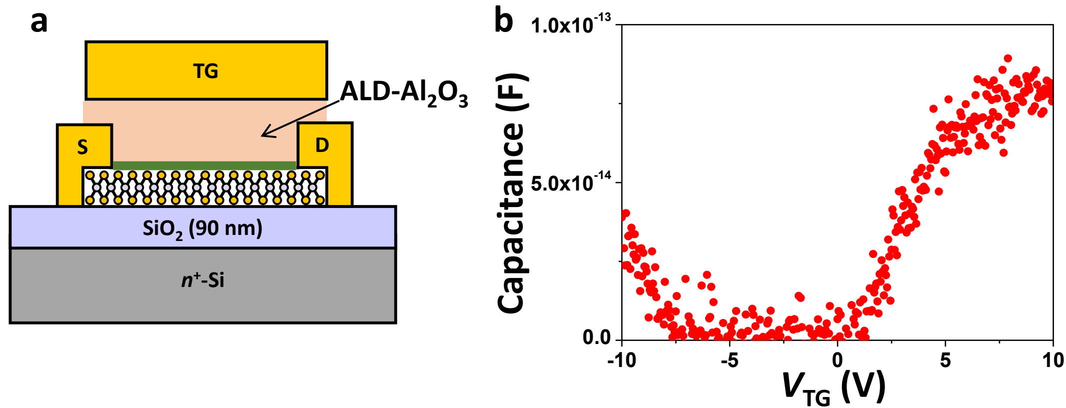

Fig. 2-13 (a) Schematic to show measured 4 nm-thick dual-gate *p*-type MoS_2 FET. *P*-type MoS_2 will be specially mentioned when used and conventional natural *n*-type MoS_2 is called MoS_2 for short. **(b)** Measured source/drain to gate capacitance in **(a)** structure shows ambipolar behavior.

2.4 Interpretation of *I-V* thickness dependence in ACCU-FET

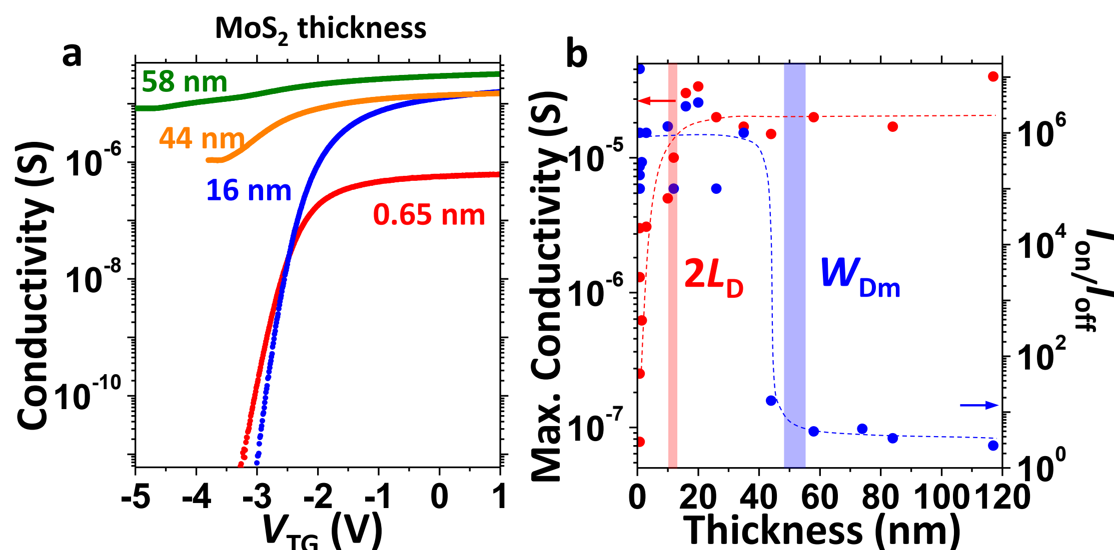

Fig.2-14 (a) σ–V_{TG} characteristics at V_{DS} = 0.1 V with MoS_2 thickness of 0.65, 16, 44, 58 nm. **(b)** Maximum conductivity and I_{ON}/I_{OFF} ratio as a function of thickness.

Thickness dependence of partial top-gate MoS_2 ACCU-FET from structure in **Fig. 3-4** is discussed in this subchapter. **Fig. 2-14** shows typical conductivity (σ) – top gate voltage V_{TG} characteristic at V_{DS} = 0.1 V with the MoS_2 thickness (t_{MoS2}) of 0.65, 16, 44, 58 nm from partial top-gate MoS_2 FET. Monolayer MoS_2 shows clear off and subthreshold region. There are two distinct features by increasing MoS_2 thickness. One is the increase in the on-state conductivity for 16 nm-thick sample and gradually saturates at thicker MoS_2 samples. The other is the abrupt increase in the residual conductance for 44 nm-thick sample.

To focus on these two features, maximum conductivity and the ratio of on-state to off-state current (I_{ON}/I_{OFF}) are shown with the range of t_{MoS2} = 0.65 ~ 118 nm in **Fig. 2-14 (b)**. It is discussed similarly with the mobility analysis in MoS_2. Coulomb scattering due to interfacial impurities is found to be dominant in scattering mechanism of ultra-thin MoS_2 [12,13]. Extrinsic Debye length (L_D) is given here for the screening length of Coulomb scattering since most of the 2D materials are intrinsically charged by

defects and impurities.

$$L_D = \sqrt{\frac{\varepsilon_{MoS2} k_B T}{e^2 N_D}} \quad . \qquad (2\text{-}1)$$

ε_{MoS2}, k_B, T, e are defined as dielectric constant of MoS_2 at the direction normal to the basal plane, Boltzmann constant, temperature, elementary charge, respectively. N_D is the density of the donors (density of acceptors N_A for p-type 2D). $2\times L_D$ is used in the following discussion to account for both top and bottom interfaces. The MoS_2 with $t_{MoS2} > 2L_D$ will be undisturbed by the interfaces and maximum conductivity saturates.

As for I_{ON}/I_{OFF}, two regions are clearly observed. The transition occurs at t_{MoS2} = ~48 - 55 nm. For ACCU-FET, the conduction comes from "body current flow", which is modulated by the depletion region in the channel. The screening length ($\lambda_{ACCU\text{-}FET}$) is determined by maximum depletion width W_{Dm} [14], which can be expressed as follows:

$$\lambda_{ACCU-FET} = W_{Dm} = \sqrt{\frac{4\varepsilon_{MoS2} k_B T \ln(N_D / n_i)}{e^2 N_D}} \quad , \qquad (2\text{-}2)$$

where n_i is intrinsic carrier density. $\lambda_{ACCU\text{-}FET}$ is independent on C_{ox}. Increase in residual conductance occurs (e.g., 44 nm-thick sample in **Fig. 2-14 (a)**) when t_{MoS2} gets close to W_{Dm} due to screening of the gate control. The present data indicates that W_{Dm} is ~48 - 55 nm. It should be noted that this W_{Dm} is roughly consistent with that in the previous data for global back gate MoS_2 FET[15,16]. It again indicates that ACCU-FEF mode dominates the device operation mechanism in widely fabricated back-gate 2D-FET. In the following discussion, we use "bulk" for MoS_2 with $t_{MoS2} > W_{Dm}$ and "multilayer" for $t_{MoS2} < W_{Dm}$ for simplicity.

2.5 C_{ox} estimation by *I-V*

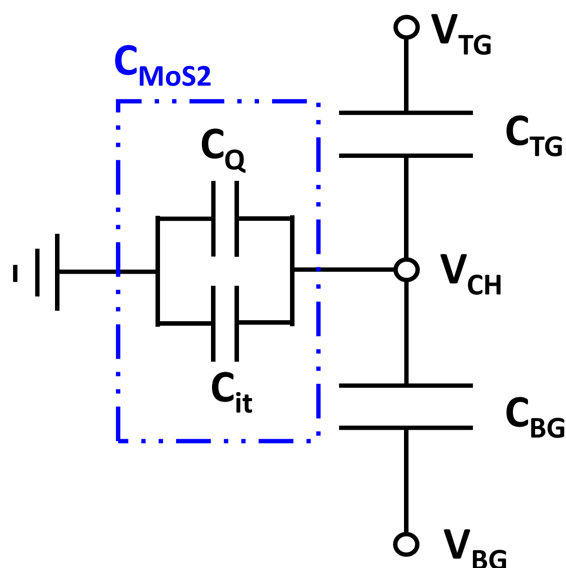

Fig. 2-15 (a) Simplified equivalent circuit of monolayer MoS_2 in monolayer dual-gate *I-V* measurement. C_{BG} and C_{TG} are the back and top gate C_{ox}, respectively. V_{CH} is the potential on the channel.

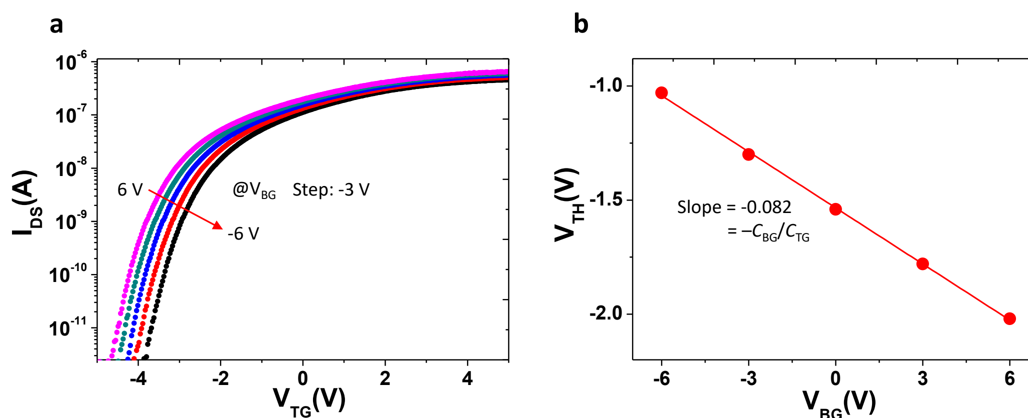

Fig. 2-16 (a) I_{DS}–V_{TG} characteristics for a monolayer MoS_2 dual-gate FET with V_{DS} = 0.1 V at different V_{BG}. V_{BG} ranges from 6~-6 V with a step of 3 V. **(b)** The trace of V_{TH} observed for the V_{TG} sweep as a function of V_{BG}. The V_{TH} position is controlled by the relative ratio of capacitive coupling between the top and back gates with a MoS_2 channel. Therefore, the slope shown in **(b)** corresponds to $-C_{BG}/C_{TG}$, Because C_{BG} is 0.038 μF/cm^2 for the 90-nm SiO_2 with k_{SiO2} = 3.9, C_{TG} can be estimated to be 0.46 μF/cm^2.

Partial coupling between top-gate and back-gate has been studied in **Fig. 2-9**, which comes from transition of dominant channel region. In this subchapter, I_{DS}–V_{TG} characteristics at different V_{BG} (**Fig. 2-16**) for a monolayer MoS_2 dual-gate FET show conventional full coupling because it is always the channel below the top gate electrode that dominates the top-gate I_{DS}–V_{TG} curves. By using this full coupling, C_{ox} of top-gate can be estimated. Based on the equivalent circuit in **Fig. 2-15**, the total charge in the channel is induced by both top gate and bottom gate.

$$V_{CH}C_{MoS2} = (V_{TG} - V_{CH})C_{TG} + (V_{BG} - V_{CH})C_{BG}, \tag{2-3}$$

where C_{MoS2} is the capacitance of MoS_2, which consists of C_Q and C_{it} in parallel. Carrier density is constant in principle when source/drain current is kept unchanged. As a result, V_{CH} and C_{MoS2} are also constant. Therefore, after the transformation,

$$Const. = V_{CH}(C_{MoS2} + C_{TG} + C_{BG}) = V_{TG}C_{TG} + V_{BG}C_{BG}. \tag{2-4}$$

By modulating top gate and bottom gate simultaneously at constant source/drain current,

$V_{BG} \to V_{BG} + \Delta V_{BG}$, $V_{TG} \to V_{TG} + \Delta V_{TG}$.

Eq. 2-4 turns to be

$$Const. = (V_{TG} + \Delta V_{TG})C_{TG} + (V_{BG} + \Delta V_{BG})C_{BG}. \tag{2-5}$$

By comparing Eq. (2-4), (2-5),

$$\Delta V_{TG}C_{TG} + \Delta V_{BG}C_{BG} = 0, \tag{2-6}$$

or

$$-C_{BG} / C_{TG} = \Delta V_{TG} / \Delta V_{BG}. \tag{2-7}$$

Because C_{BG} is 0.038 $\mu F/cm^2$ for the 90-nm SiO_2 with $k_{SiO2} = 3.9$, C_{TG} can be estimated. Experimentally, source/drain current is kept as constant below or close to the current level at V_{TH} due to high sensitivity of carrier density as a function of gate bias at subthreshold region.

C_{OX} can also be estimated by *C*-*V* in the strong accumulation region by neglecting quantum-mechanical effect, which will be shown in chapter 3. Extracted C_{ox} by *I*-*V* and *C*-*V* are consistent with each other as shown in Table 2.1.

	Monolayer Sample 1	Monolayer Sample 2	Monolayer Sample 3
Gate area (μm^2)	143	37	133
C_{ox} by IV (μF/cm^2)	0.38	0.34	0.46
C_{ox} by CV (μF/cm^2)	0.41	0.36	0.44

Table 2.1 C_{ox} of top-gate values for three samples are different because they are from different batches.

2.6 Summary

In this chapter, the device fabrication process has been demonstrated. The operation mechanism of 2D-FET has been discussed based on fabricated devices, which mainly focus on *I-V* characterization. Experimentally, contact plays an important role for killing device performance especially at on-state in terms of contact resistance. However, the contact based SB-FET mode cannot be used to fully explain the device behavior. Channel based ACCU-FET has been proposed and developed to explain the above behaviors, which is more applicable and universal in 2D-FET.

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3 *C*-*V* characterization of MoS_2 ACCU-FET

C-*V* measurement is the powerful tool to gain further insight into the device physics of 2D materials. However, only a few works report the capacitance measurement of MoS_2. The mechanism of capacitance on 2D materials is unclear. Moreover, capacitance measurement is very sensitive to parasitic capacitance and resistance effect, which is not fully considered in the previous work.

In this chapter, *C*-*V* characterization of MoS_2 FET structure will be systematically studied. Both parasitic capacitance and resistance effect will be carefully checked. Quantum-mechanical effect will also be investigated from monolayer to bulk MoS_2.

3.1 Full equivalent circuit of *C*-*V*

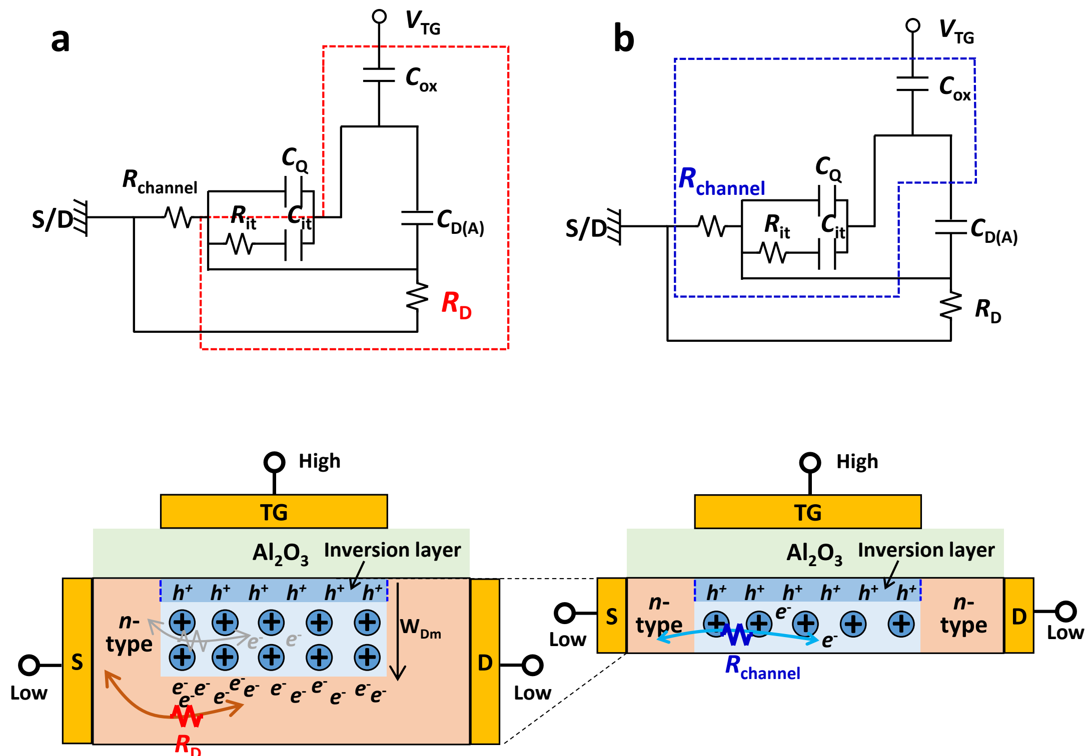


Fig. 3-1 Ideal full equivalent circuits and schematics to model MoS_2-FET *C*-*V* in **(a)** bulk and **(b)** thin MoS_2 case, respectively.

The basic understanding of equivalent circuit of 2D-FET is discussed in this subchapter. Source/drain to top-gate capacitance is always measured in *C-V* measurement for 2D-FET as shown in **Fig. 3-1**. It should be noted that MoS_2 flakes with a large area (> 30 μm^2) were selected to improve the signal-to-noise ratio in the capacitance measurement. *C-V* in Si MOSFET (discussed in subchapter 1.7) focuses on minority carriers while *C-V* in MoS_2-FET focuses on majority carriers. It is because of the lack of source/drain doping in MoS_2-FET. Although the inversion layer is still formed in MoS_2-FET by applying large negative gate bias, hole is not considered in this device structure. It is because back-to-back *p-n* junction are formed between *p*-type inversion layer and *n*-type access region. The ideal equivalent circuit is shown in **Fig. 3-1**. C_{it} and R_{it} are the interface states' capacitance and resistance, respectively, which account for carrier capture and emission processes. $C_{D(A)}$ is the depletion capacitance (accumulation capacitance) of bulk MoS_2 when $t_{MoS2} > W_{Dm}$. R_D is the resistance that models the supply of carriers to the depletion layer when $t_{MoS2} > W_{Dm}$. R_D is small due to the natural *n*-doping in bulk MoS_2. C_Q is the quantum capacitance of ultra-thin MoS_2. $R_{channel}$ is the MoS_2 channel resistance just below the top gate electrode and is modulated by the top gate bias. R_D models the supply of carriers to the depletion layer when $t_{MoS2} < W_{Dm}$. $R_{channel}$ comes from a small amount of electrons at the depletion region. As a result, $R_{channel} \ll R_D$. Strictly speaking, C_Q and $C_{D(A)}$ are not in parallel because both come from majority carrier response in MoS_2. They can be calculated by considering carriers statistics and distribution in MoS_2. However, C_Q and $C_{D(A)}$ are shown in parallel here in order to show charging path transition clearly. This is the big issue when we try to study interfacial properties and to extract C_{it}. It is because the dominant charging resistance for C_{it} may not be R_{it} but other resistance. In the bulk MoS_2 case, it is R_D that affects the charging resistance. R_D is much smaller than R_{it}, which can be neglected. This enables us to study *C-V* in the conventional way, which will be discussed in subchapter 3.6.1. While in the ultra-thin MoS_2 case, it is $R_{channel}$ that affects the charging resistance. The comparison between $R_{channel}$ and R_{it} will be made in subchapter 3.4.

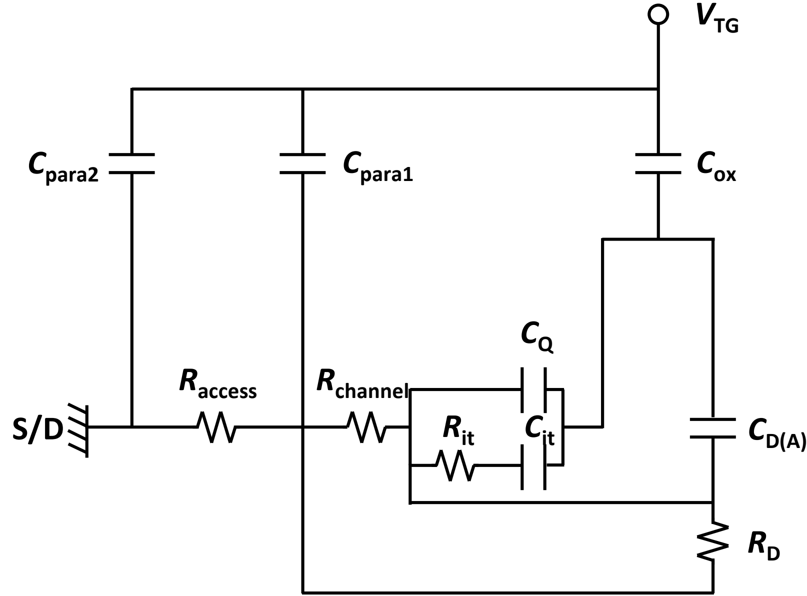


Fig. 3-2 Full equivalent circuit to model MoS_2-FET *C-V*.

By including parasitic capacitance and other resistance effects, the full equivalent circuit used to model the top gate MoS_2-FETs is shown in **Fig. 3-2**. Here, C_{para1} and C_{para2} are the two types of commonly observed parasitic capacitance. R_{access} is defined as the sum of MoS_2/metal contact resistance and MoS_2 resistance at the access region indicated in **Fig. 2-1**, which is constant. We focus on monolayer MoS_2 in subchapter 3.2-3.5 and discuss the thickness dependence of MoS_2 in subchapter 3.6.

3.2 Parasitic capacitance effect on *C-V*

Several pitfalls are first discussed for MoS_2-FET-based *C-V*. Monolayer MoS_2 *C-V* is focused here as an example. The first pitfall is the parasitic capacitance effect, which comes from the widely used n^+-Si/SiO_2 substrate. As indicated previously, in the double-gated geometry, there is capacitive coupling between the back and top gates through the large contact pad area, which induces large parasitic capacitance [1]. C_{para1} refers to the parasitic capacitance that is charged or discharged through constant R_{access}. The source is connected to low-terminal and drain is floating. While the top gate is connected to high-terminal in this case as shown in **Fig. 3-3 (b)**. This will induce large

frequency dispersion (> C_{ox}) in *C*-*V* and corresponding peaks in the conductance-frequency (G_p/ω-f) measurement as shown in **Fig. 3-3 (c, d)**. C_{para1} can be suppressed even on n^+-Si/SiO_2 substrate when both source and drain are connected to low-terminal and top gate is connected to high-terminal, which is shown in **Fig. 3-4 (c)**. C_{para2} refers to the parasitic capacitance that could shift the baseline of the *C*-*V* curve. C_{para2} cannot be neglected on n^+-Si/SiO_2 substrate. By fabricating MoS_2 FET on the quartz substrate as shown in **Fig. 3-5**, even C_{para2} can be totally suppressed as shown in **Fig. 3-4 (c)**. Monolayer MoS_2 on quartz substrate can still be distinguished by contrast in an optical microscope, which is then confirmed by Raman spectroscopy. Slight frequency change of A_{1g} peak in Raman might indicate doping effect from the substrate. Therefore, in the following *C*-*V* discussion, the quartz substrate is used to totally remove these parasitic capacitances.

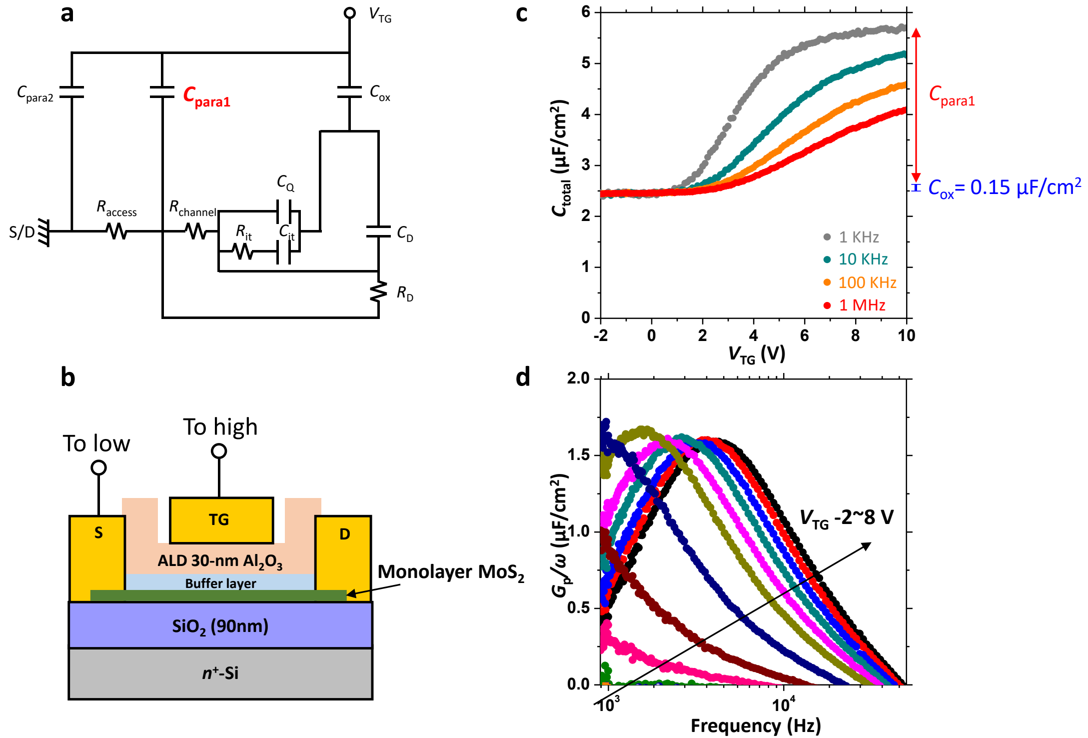


Fig. 3-3 (a) Full equivalent circuit to show C_{para1}. **(b)** The configuration of capacitance measurement. Source is connected to low-terminal and drain is floating. Top gate is

connected to high-terminal. This configuration combined with n^+-Si/SiO_2 substrate introduce large frequency dispersion ($>C_{ox}$) in **(c)** *C-V* and **(d)** corresponding peaks in conductance-frequency (G_p/ω-f) measurement. It should be noted that these peaks are not related with the interface traps.

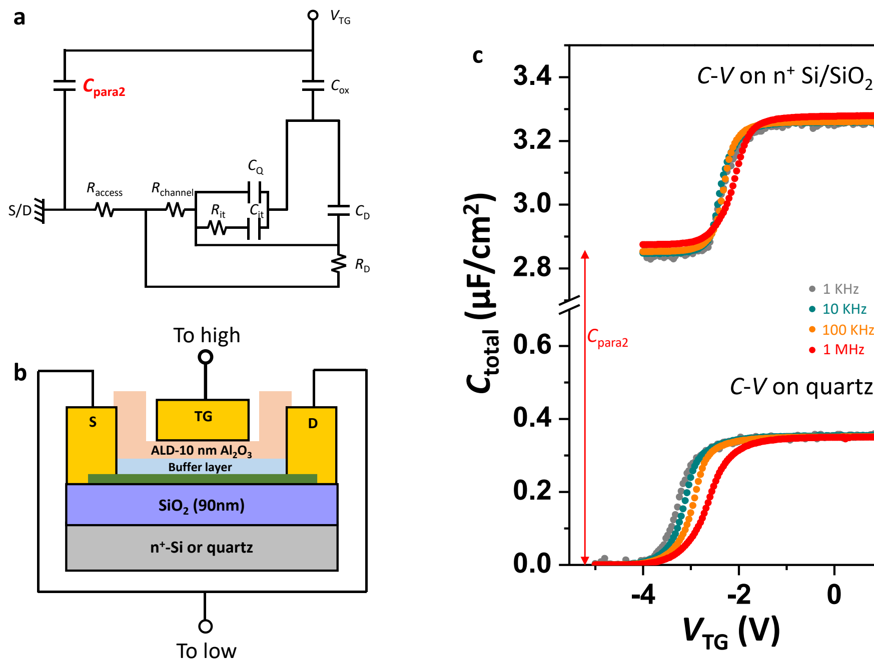


Fig. 3-4 (a) Full equivalent circuit to show C_{para2}. **(b)** The configuration of capacitance measurement. Both source and drain are connected to low-terminal and top gate is connected to high-terminal. Under this configuration, C_{para1} can be suppressed even on n^+-Si/SiO_2 substrate. However, C_{para2} still induces large baseline shift in *C-V*, which cannot be removed as shown in **(c)**. By fabricating MoS_2 FET on quartz substrate, all the parasitic capacitance is totally removed.

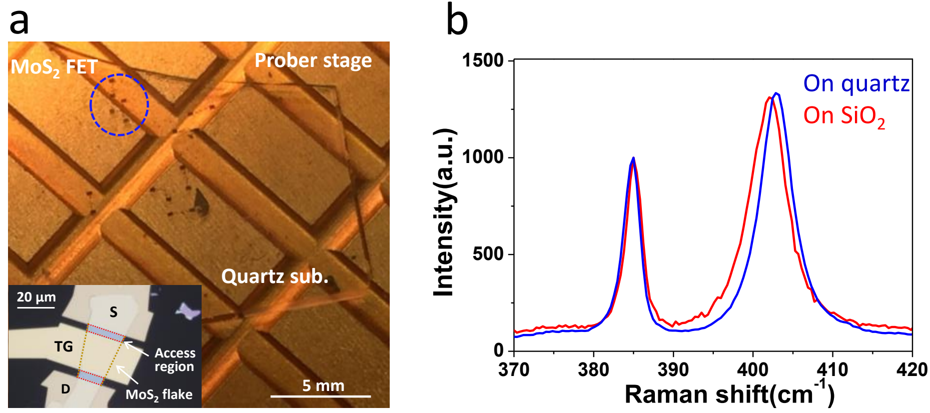


Fig. 3-5 (a) Optical image of the device on quartz substrate. The access region refers to the channel region uncovered by the top gate electrode. S, D and TG indicate the source, drain and top gate electrodes, respectively. **(b)** Raman spectroscopy of monolayer MoS_2 on both SiO_2 and quartz substrate, respectively.

3.3 Access resistance effect on *C*-*V*

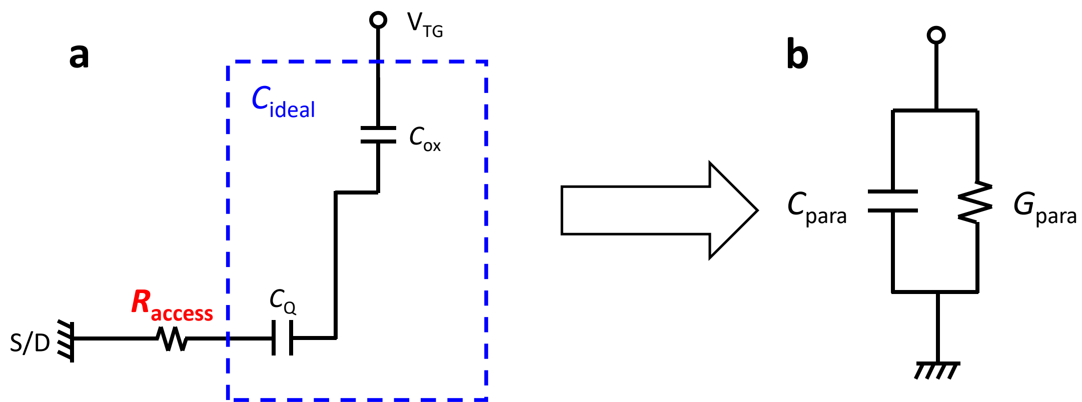


Fig. 3-6 (a) Simplified circuit of monolayer MoS_2 FET by neglecting interface states effect in order to study R_{access} effect. **(b)** Equivalent parallel circuit of **(a)**.

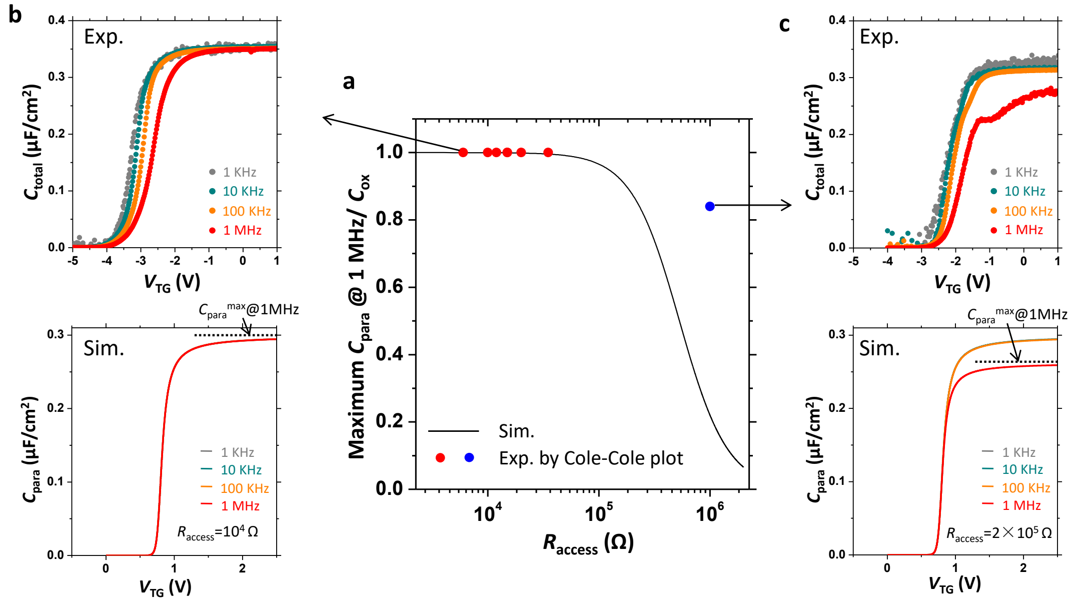


Fig. 3-7 (a) Maximum C_{para} at 1 MHz/Cox as a function of R_{access}. **(b,c)** Experimental and simulated C_{total}-V_{TG} characteristics of MoS_2 FET with different R_{access}. The decrease in Maximum C_{para} at 1 MHz is clearly observed in **(c)** due to high R_{access} ~1000 kΩ.

R_{access} can cause error in measured capacitance [2]. R_{access} effect is simulated based on equivalent parallel circuit of monolayer MoS_2 *C-V* and other resistance effect is not included in this simulation as shown in **Fig. 3-6**. Here, C_{ideal} is defined as ideal *C-V* in monolayer MoS_2 without C_{it}. Change of C_Q will not affect the conclusion in R_{access} simulation. C_{ox} is given as 0.3 μF/cm^2 with 10×10 μm^2 area. Equivalent parallel capacitance is shown as follows:

$$C_{Para} = C_{ideal} / (1 + \omega^2 C_{ideal}^2 R_{access}^2) . \quad (3\text{-}1)$$

Experimentally, access resistance can be extracted by Cole-Cole plot at accumulation region where other resistance is shunted. Maximum C_{para} at 1 MHz remains to C_{ox} when R_{access} = 10^4 Ω and decrease when R_{access} = 2×10^5 Ω. Therefore, maximum C_{para} at 1 MHz/C_{ox} is the good parameter to indicate R_{access} effect. This parameter equals to 1 when R_{access} can be neglected at measured frequency range and decrease when R_{access} limit the measured capacitance as shown in **Fig. 3-7 (a)**. The measured R_{access} is on the order of ~10 kΩ in most of the samples due to the natural n-doped property of MoS_2 and the low contact resistance with Ni. While in the rare case when R_{access} is quite high,

the large frequency dispersion occurs at the strong accumulation region of *C*-*V* both in experiments and simulations as shown in **Fig. 3-7 (c)**. As a summary, most of the fabricated samples can neglect R_{access} effect at measured frequency range, which do not show any frequency dispersion at strong accumulation region. We have to mention that R_{access} can still severely affect capacitance measurements at low temperature and for other 2D materials with higher access resistance.

Now, the equivalent circuit can be simplified as shown in **Fig. 3-8**, where the experimentally measured source/drain to gate capacitance is defined as C_{total}.

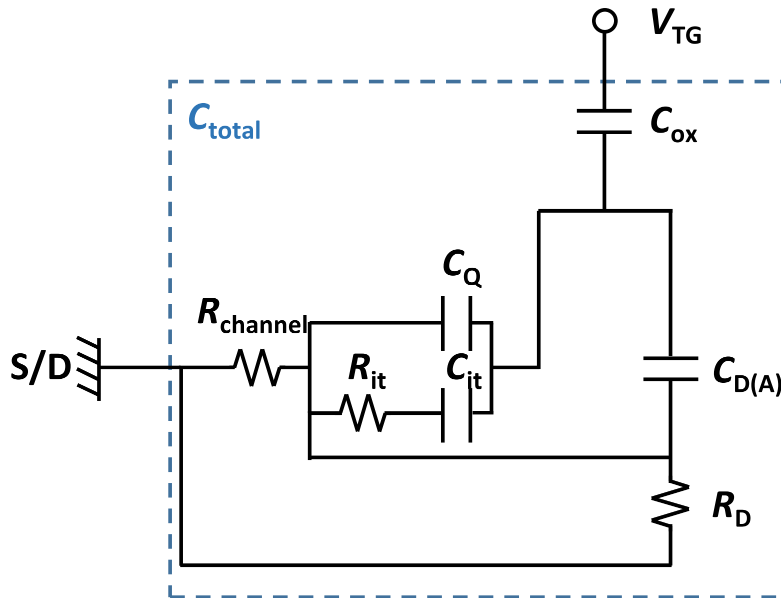


Fig. 3-8 Simplified full equivalent circuits after considering C_{para} and R_{access} effect.

3.4 Channel resistance effect on *C*-*V*

As have discussed in subchapter 3.1, channel resistance might seriously affect ultra-thin MoS_2 *C*-*V*. Thus before considering the quantum capacitance in monolayer MoS_2, $R_{channel}$ effect will be discussed in this subchapter. Shockley-Read-Hall (SRH) theory is the basis to study carrier capture and emission process by the traps [3]. Based on this theory, a series R_{it}-C_{it} network is modeled in the equivalent circuit, and experimental impedance spectroscopy always tries to capture this R_{it}-C_{it}-induced signal by excluding other capacitance or resistance effects. Large frequency dispersion is widely observed in the capacitance measurement of thin MoS_2 and other 2D-FET [4-6]. It is often treated as R_{it}-C_{it}-induced signals. However, other resistance effects could also introduce frequency-dependent signals. $R_{channel}$ is always parasitic in the FET structure, which cannot be avoided. In this subchapter, $R_{channel}$ effect will be studied quantitatively. Monolayer MoS_2 is again selected here as an example because it shows the largest frequency dispersion and the simplest C_Q expression.

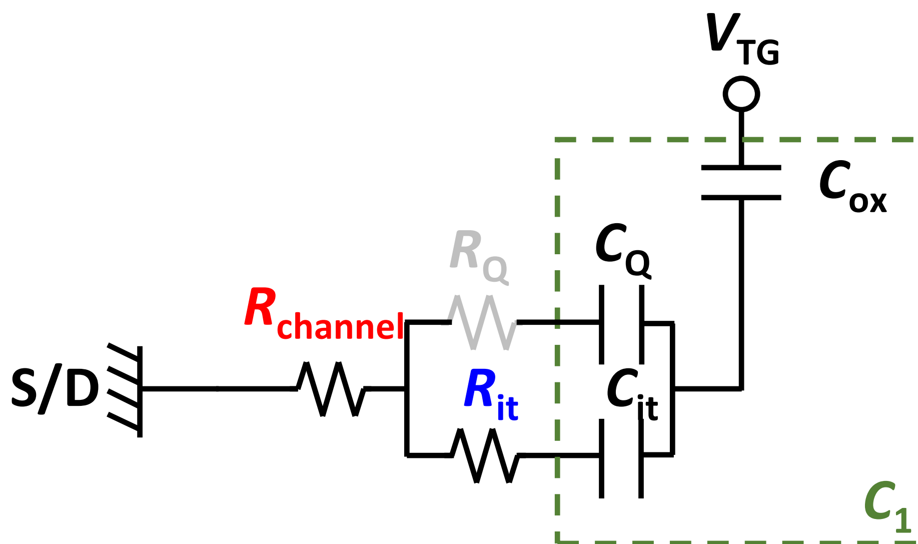


Fig. 3-9 Simplified lumped equivalent circuit to model monolayer MoS_2-FET *C*-*V*. Both $R_{channel}$ and R_{it} could limit the frequency response of the capacitance.

Fig. 3-9 shows the equivalent circuit of monolayer MoS_2 FET. C_1 is defined as

the ideal capacitance by neglecting any resistance effect, and $C_1 = \frac{(C_Q+C_{it})C_{ox}}{C_Q+C_{it}+C_{ox}}$. R_{channel} indicates the time constant of the majority carriers suppled by source/drain through drift process (similar consideration of minority carriers in Si MOSFET *C*-*V* as shown in subchapter 1.7.2). R_{it} indicates the time constant of carrier capture and emission process by the traps. R_{Q} indicates the response time (τ_{Q}) of C_{Q} when the carriers from source/drain already drift to the exact position of the channel. This response time relates to the dielectric relaxation time, which can be usually neglected for majority carriers at megahertz range. Comparison of τ_{Q} and τ_{Rch} will be shown at the end of this subchapter.

Experimentally, when resistance exists in the equivalent circuit, it will give the *R*-*C* circuit, in which the time constant (τ) is determined. C_{total} will decay from C_1 for $\omega\tau > 1$, where ω is angular frequency. τ_{Rch} and τ_{it} are defined as the time constants from R_{channel} and R_{it}, respectively.

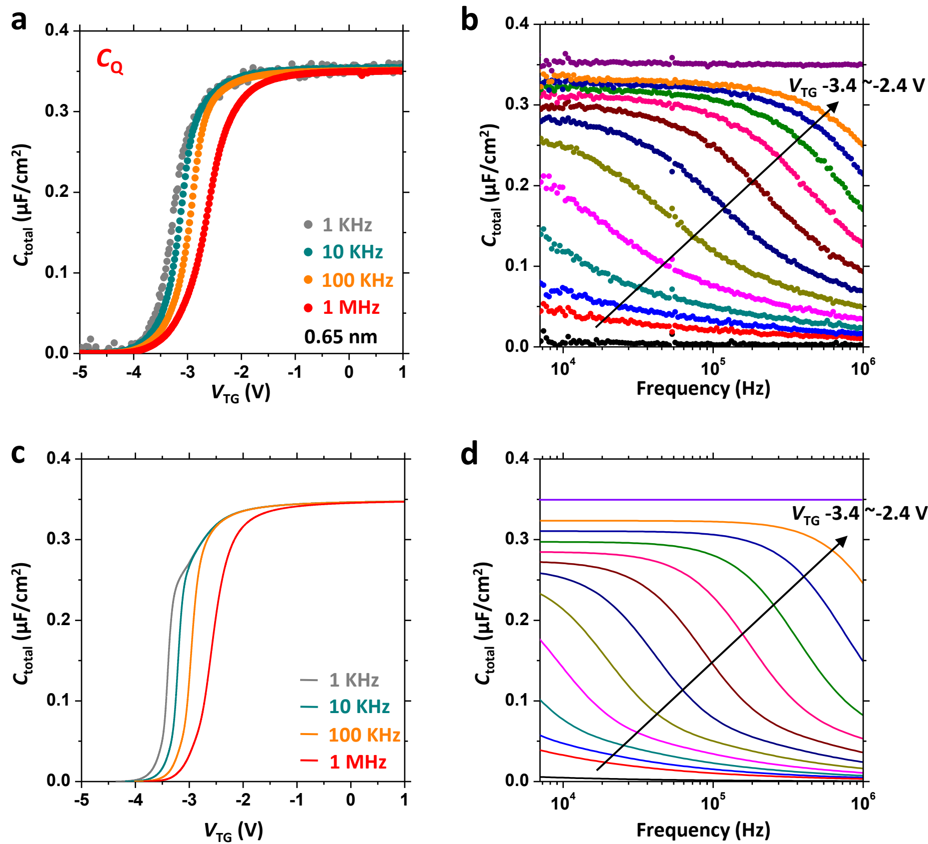


Fig. 3-10 (a) Experimental C_{total} as a function of V_{TG}. **(b)** Experimental C_{total} as a function of frequency at different V_{TG} (-3.4~-2.4 V) from monolayer MoS_2 FETs. A large frequency response is observed, which corresponds to the frequency dispersion of

C-V in **(a)**. **(c)** Calculated plot of C_{total}-V_{TG} curves. **(d)** Calculated plot of C_{total}-f curves at different V_{TG} values (-3.4~-2.4 V).

Fig. 3-10 (b) shows measured C_{total} as a function of frequency (C-f) at different V_{TG} for the monolayer device. The clear decay of C_{total} at a specific frequency indicates that the capacitance is limited by one type of resistance. Now the task is to clarify which resistance that dominates the frequency dependence here.

For τ_{Rch}, it is derived from a transmission line model [7,8] as follows (Supplementary Information Note 1):

$$\tau_{Rch} = \frac{C_1 R_{S,channel} L^2}{4}, \tag{3-2}$$

where L is the channel length and $R_{\text{S,channel}}$ is the sheet resistance of MoS_2 channel. The drift current model[9] is applied to express $R_{\text{S,channel}}$. Because the channel is on the order of micrometers in length and has homogenous bulk doping concentration from the source to drain, the diffusion current is negligible. Moreover, the drift current model reveals free carrier transport in the conduction band, which enables us to correlate C-V with I-V in the next chapter. $R_{S,channel} = \frac{1}{en_{ch}\mu}$, where n_{ch} is the channel carrier density and μ is the drift mobility. C_{it} and μ are consistent with the I-V characteristics. A higher C_{it} means that more states need to be charged, which results in a larger τ_{Rch}. On the other hand, τ_{it} is calculated based on SRH theory [10] in a 2-dimensional system as follows:

$$\tau_{it} = \frac{1}{\sigma_{capture-2D} v_{th} n_{ch}}, \tag{3-3}$$

where $\sigma_{\text{capture-2D}}$ is the capture cross section of interface states, which largely depends on the type of interface states. For point defects (e.g., sulfur vacancy), it would be close to the atom size of ~0.3 nm [11]. For substrate fluctuation induced gap states, it could be on the order of 10 nm [12]. Therefore, $\sigma_{\text{capture-2D}}$ is assumed to be in the range of 0.3~10 nm. v_{th} is thermal velocity of ~1.2×10^7 cm/s at room temperature by considering the electron effective mass of monolayer MoS_2 as $m^* = 0.6\ m_0$, where m_0 is the electron mass in a vacuum.

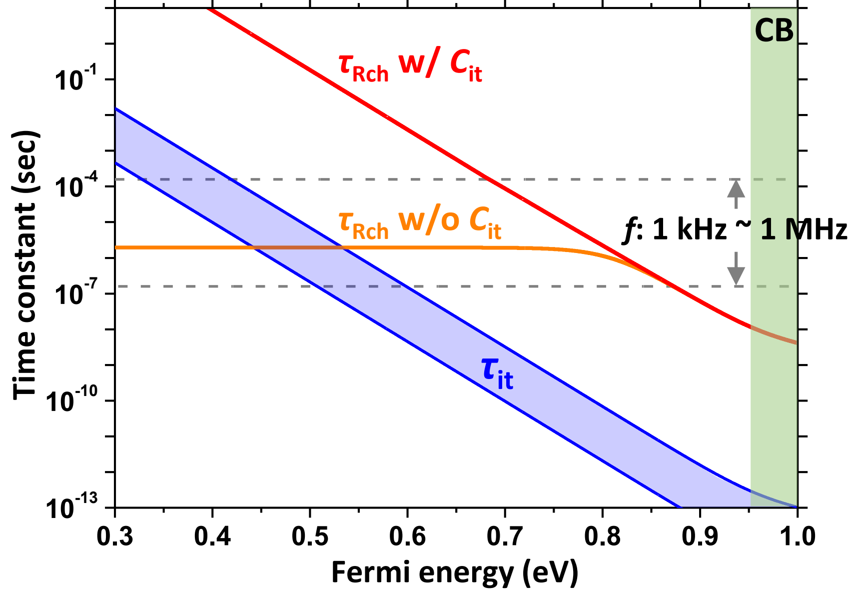


Fig. 3-11 Calculated time constant as a function of E_F. Monolayer MoS_2 is assumed to have a bandgap of 1.9 eV. E_F = 0.95 eV indicates the bottom of the CB. Dash line indicates the experimental measured frequency range by using $\tau = 1/\omega$.

The calculated time constant as a function of E_F is shown in **Fig. 3-11**. τ_{Rch} w/ C_{it} is larger than τ_{Rch} w/o C_{it}, because more states need to charged and discharged through $R_{channel}$. Used C_{it} is shown in **Fig. 4-1 (b)**. τ_{Rch} w/ C_{it} is ~3 orders of magnitude larger than τ_{it} and is distributed across the measured frequency range of 1 kHz to 1 MHz, which indicates that the time constant due to the channel charging effect is the origin of the frequency-dependent capacitance behavior in **Fig. 3-10 (a,b)**. It is noted that both τ_{it} and τ_{Rch} with C_{it} have a similar exponential E_F dependence because the parameter n_{ch} is included.

The experimental C-V and C-f curves are then reproduced by considering $R_{channel}$ instead of R_{it}. C_{total} is derived as (Supplementary Information Note 1):

$$C_{total} = C_1 \operatorname{Re}\left[\frac{\tanh \lambda}{\lambda}\right], \text{ where } \lambda = \sqrt{j\omega\tau_{Rch}}\,. \tag{3-4}$$

V_{TG} is calculated as follows:

$$V_{TG} = V_{TG,mid-gap} + \int_0^{E_F/e} (C_{Q(D)} + C_{it} + C_{ox}) / C_{ox} d(E_F / e)\,. \tag{3-5}$$

$V_{TG,mid-gap}$ is a fitting parameter to compensate the MoS_2 n-doping effect. Eq. (3-5) will

be used to correlate E_F with V_{TG}. Later, we will study multilayer MoS_2, where the surface potential ψ_S is used instead of E_F/e. C_{it} is included in Eq. (3-5) since the interface states always respond to the direct current (dc) V_{TG}. Extracted C_{it} here from *C-V* is consistent with C_{it} from *I-V* as shown in **Fig. 4-1(b)**. The simulation reproduces the experimental data quite well as shown in **Fig. 3-10 (c,d)**, suggesting that the experimentally observed frequency dispersion in *C-V* does not result from the electron capture/emission process at the interface traps but from the channel charging effect. From the above study of $R_{channel}$ effect, let us review previous work on the *C-V* study of MoS_2. The widely used high-low frequency method on 2D-FET-based *C-V*[4-6] will not reveal the true C_{it} value quantitatively because the extracted time constant is indeed τ_{Rch} instead of τ_{it}.

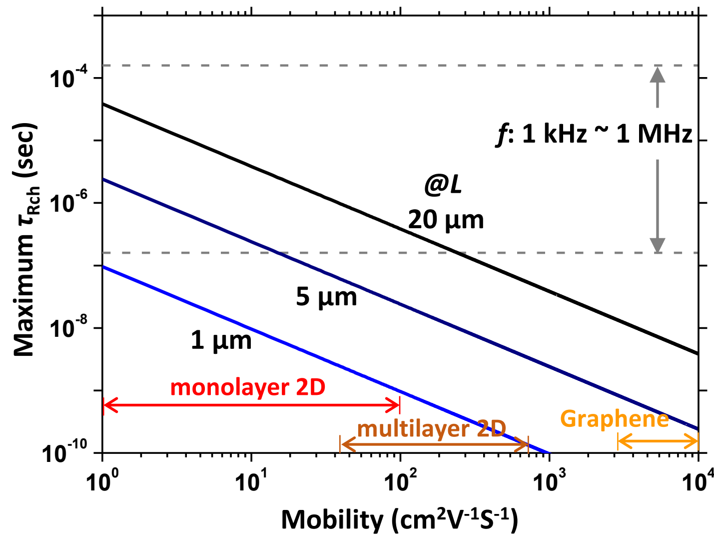


Fig. 3-12 Calculated maximum τ_{Rch} as a function of mobility at different *L*.

To provide guidance on how to avoid the channel charging effect in all 2D-FET-based *C-V* with different thicknesses from monolayer to multilayer, the universal expression is derived. The region where $C_Q << C_{ox}$ should be considered since the $R_{channel}$ effect is severe due to the low carrier density. We assume that C_{it} is smaller than C_Q, that is, attention should always be paid to improve the interface. In this case, $C_1 = C_Q$. C_Q of monolayer MoS_2 will be shown in Eq. (3-7) while C_Q of multilayer MoS_2 (full-depletion capacitance) will be shown in Eq. (3-8). Then, based on Eq. (3-2) and

the definition of $C_Q = \frac{dn_{ch}}{d\psi_s}$, $\tau_{\rm Rch}$ will have a constant maximum, which is similar to $\tau_{\rm Rch}$ without $C_{\rm it}$ in the monolayer case **(Fig. 3-11)**. This is because $n_{\rm ch}$ in both $C_{\rm Q}$ and $R_{\rm S,channel}$ cancel with each other. This constant maximum is shown as follows:

$$Maximum \quad \tau_{Rch} = \frac{L^2}{4\mu(k_B T / e)} . \tag{3-6}$$

The maximum $\tau_{\rm Rch}$ is shown as a function of μ for various L in **Fig. 3-12**. Here, μ-$n_{\rm ch}$ dependence is not considered. $\tau_{\rm Rch}$ should be smaller than the measured frequency range to avoid the channel charging effect. For L = 1 μm, the allowable μ can be as low as 1 $cm^2V^{-1}s^{-1}$. However, due to both experimental difficulty and small signal-to-noise ratio, L is usually in the range of 5 ~ 20 μm in our samples. In this case, μ is very important. μ is usually low in monolayer 2D materials, i.e., < 100 $cm^2V^{-1}s^{-1}$, at room temperature, while multilayer 2D materials have a higher μ, which has the potential to avoid the channel charging effect. This has been confirmed in our 16-nm-thick device with suppressed frequency dispersion in **Fig. 3-16**. On the other hand, for graphene-based FETs, this effect can usually be neglected due to the extremely high μ, which accounts for the recently observed frequency dispersion-free $C_{\rm it}$ in a bilayer graphene/*h*-BN/graphite heterostructure [13].

In order to derive $\tau_{\rm Rch}$ from a simple physical argument, let us consider field of one thermal unit driven by external source/drain contact is $(k_{\rm B}T)/(2eL)$. This results in nonequilibrium in the channel. Thus majority carriers must rearrange themselves to restore equilibrium. From the definition of μ under thermal field, Eq. (3-6) can be simplified as $\text{Maximum}\ \tau_{\rm Rch} = (L/2)/V_{\rm thermal}$. $V_{\rm thermal}$ is the velocity under thermal field. This equation indicates that $R_{\rm channel}$ effect on *C*-*V* measurement intrinsically come from slow response of thermal activated carriers, which are supplied from source/drain.

For $\tau_{\rm Q}$, it can also be derived in the similar way. $\tau_{\rm Q}$ can be extracted from a localized thermal fluctuation. However, this local disturbance extends over a volume of only one Debye length $L_{\rm D}$[29]. Since channel length $L/2 \gg L_{\rm D}$ in our fabricated devices, $\tau_{\rm Q}$ can be neglected.

3.5 Quantum capacitance in monolayer MoS_2

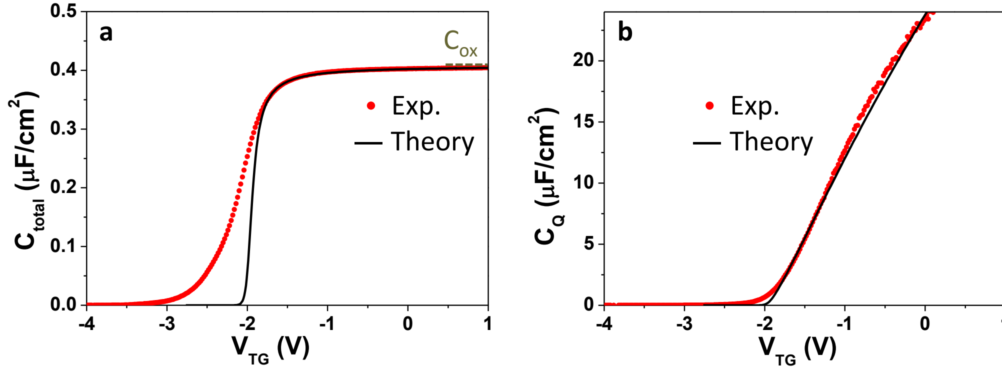


Fig. 3-13 Comparison of experiments and theory for **(a)**C_{total} and **(b)**C_Q as a function of V_{TG} from monolayer MoS_2. C_Q is experimentally extracted from the *C-V* curve at 1 MHz. The black line is the theoretical curve calculated based on Eqs. (3-5) and (3-7).

Having carefully studied both resistance and parasitic capacitance effect, now we can study underlying device physics by capacitance measurement. Quantum capacitance was originally derived from the finite *DOS* of a 2D electron gas as shown in subchapter 1.7.1[9,14]. In addition, it has been successfully extracted in graphene [15,16]. Quantum capacitance in monolayer MoS_2 is studied in this subchapter. MoS_2 thickness dependence of quantum-mechanical effect will be discussed in subchapter 3.6.2.

High-quality sample is used for this analysis. First, C_Q is extracted experimentally from the *C-V* measurements at 1 MHz in **Fig. 3-13** to observe the entire picture. At the high frequency limit of 1 MHz, the interface states are assumed to be unable to respond. Therefore, $1/C_{total} = 1/C_{ox} + 1/C_Q$ by neglecting C_{it}. C_{ox} is extracted from the saturation value at strong accumulation region. C_{ox} extracted here is consistent with that from *I-V* as shown in subchapter 2.5. Since C_{ox} has already been determined, C_Q is extracted experimentally as a function of V_{TG} in **Fig. 3-13(b)**.

Alternatively, C_Q can be calculated theoretically by considering the Fermi-Dirac distribution and *DOS* of 2D materials, and is expressed as follows[9]:

$$C_Q = e^2 g_{2D}\left[1+\frac{\exp(E_G/2k_BT)}{2\cosh(E_F/k_BT)}\right] \quad (3\text{-}7)$$

where $g_{2D} = g_s g_v m^*/2\pi\hbar^2$ is the band-edge *DOS*, and E_G is the bandgap. Here, bandgap E_G = 1.9 eV for monolayer MoS_2. g_s and g_v are the spin and valley degeneracy factors, respectively. m^* is assumed to be $0.6m_0$. The mid gap is defined to be E_F = 0 eV. Then, the conduction band edge (CBE) is located at 0.95 eV. In Eq. 3-7, C_Q is expressed as a function of E_F, and the correlation between E_F and V_{TG} is required for the comparison with the experiment. Eq. 3-5 is again used for E_F-V_{TG} correlation without including C_{it} in order to illustrate ideal case. The experimental and theoretical C_Q-V_{TG} curves are compared in **Fig. 3-13**. The C_Q-V_{TG} curve fits well with the theoretical curve over the wide range of V_{TG} (-1.8 ~ 0.1 V).

The deviations of C_Q from the theoretical curve along the transverse and vertical axes have two different origins. One, for the transverse axis, is the "stretch-out" effect [17]. Interface traps always respond to the slowly varying direct current (DC) V_{TG}, which causes the *C*-*V* curve to stretch out along the transverse V_{TG} axis as the interface trap occupancy changes with V_{TG}. The other origin, which impacts the vertical axis, is that the high-frequency limit of 1 MHz is not always satisfied since τ_{it} and τ_{Rch} are quite short near the CBE as shown in **Fig. 3-11**. Thus, the extracted C_Q from C_{total} may partially include the contribution of C_{it} in terms of the vertical axis. For both cases, interface traps cause deviations from the theoretical C_Q curve in the range of C_Q < C_{it}.

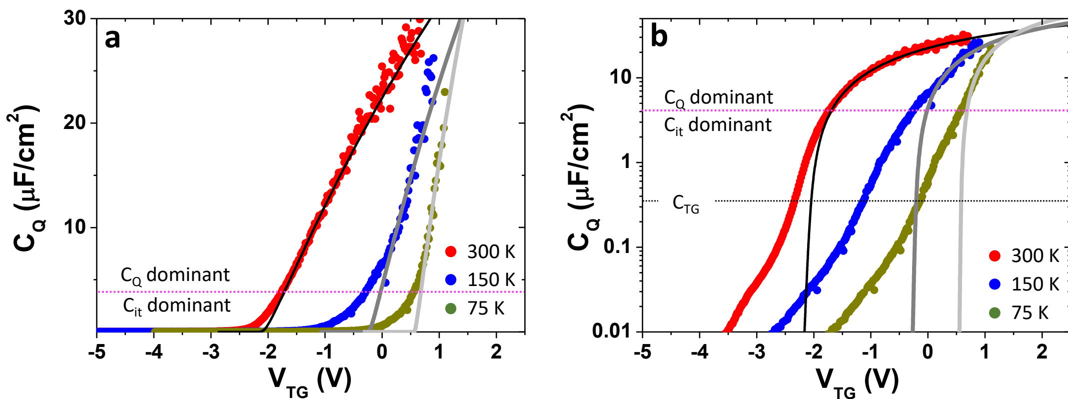


Fig. 3-14 (a) Comparison of experiments and theory for C_Q for monolayer MoS_2 FET as a function of V_{TG} at different temperatures. C_Q is experimentally extracted from the *C-V* curve at 1 MHz. The lines are the theoretical curve. **(b)** The same figure as **(a)** with the logarithmic scale.

The slope of C_Q becomes sharp at low temperatures due to the intrinsic nature of the Fermi-Dirac distribution, which provides an alternative means to confirm the validity of C_Q extraction. Based on this idea, *C-V* measurements were performed at 75, 150 and 300 K for an additionally prepared monolayer MoS_2 FET that has a relatively high quality (two-probe mobility ~ 10 cm^2 V^{-1} s^{-1}, *S.S.* = 240 mV/dec at room temperature).

C_Q is again extracted from the *C-V* curves at 1 MHz and fitted as a function of V_{TG} at different temperatures, as shown in **Fig. 3-14**. The extracted C_Q-V_{TG} curves are divided into two regions. The first region is the C_Q dominant region, with $C_Q > C_{it}$. In this region, C_Q has a clear temperature dependence and fits well with the theoretical calculation. The other region is the C_{it} dominant region, with $C_Q < C_{it}$. The C_Q-V_{TG} curve deviates from the theoretical curve and shows almost no change with decreasing temperature, which is due to C_{it} effect.

Fig. 3-15 shows experiments and theory for C_Q of monolayer MoS_2 as a function of E_F at different temperatures at full energy range. In the lower region, C_Q cannot be accurately estimated because $C_Q < C_{it}$. In the upper region, it is limited by C_{ox}. The measured C_Q range at present is still at the tail region of Fermi-Dirac distribution from CB. The larger C_{ox} is needed to directly detect two-dimensional *DOS* of ultra-thin MoS_2.

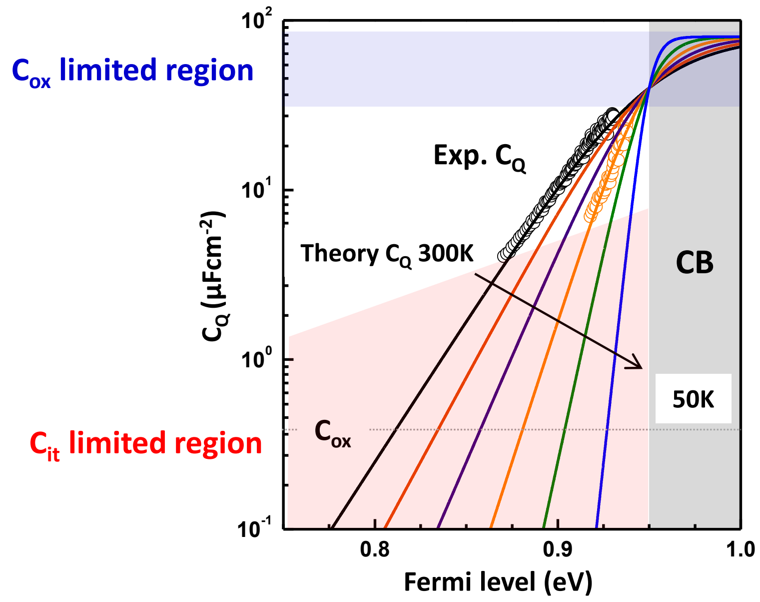


Fig. 3-15 Comparison of experiments (circle) and theory (line) for C_Q as a function of E_F at different temperatures. Temperature step is 50 K.

3.6 Thickness dependence of *C-V* characterization

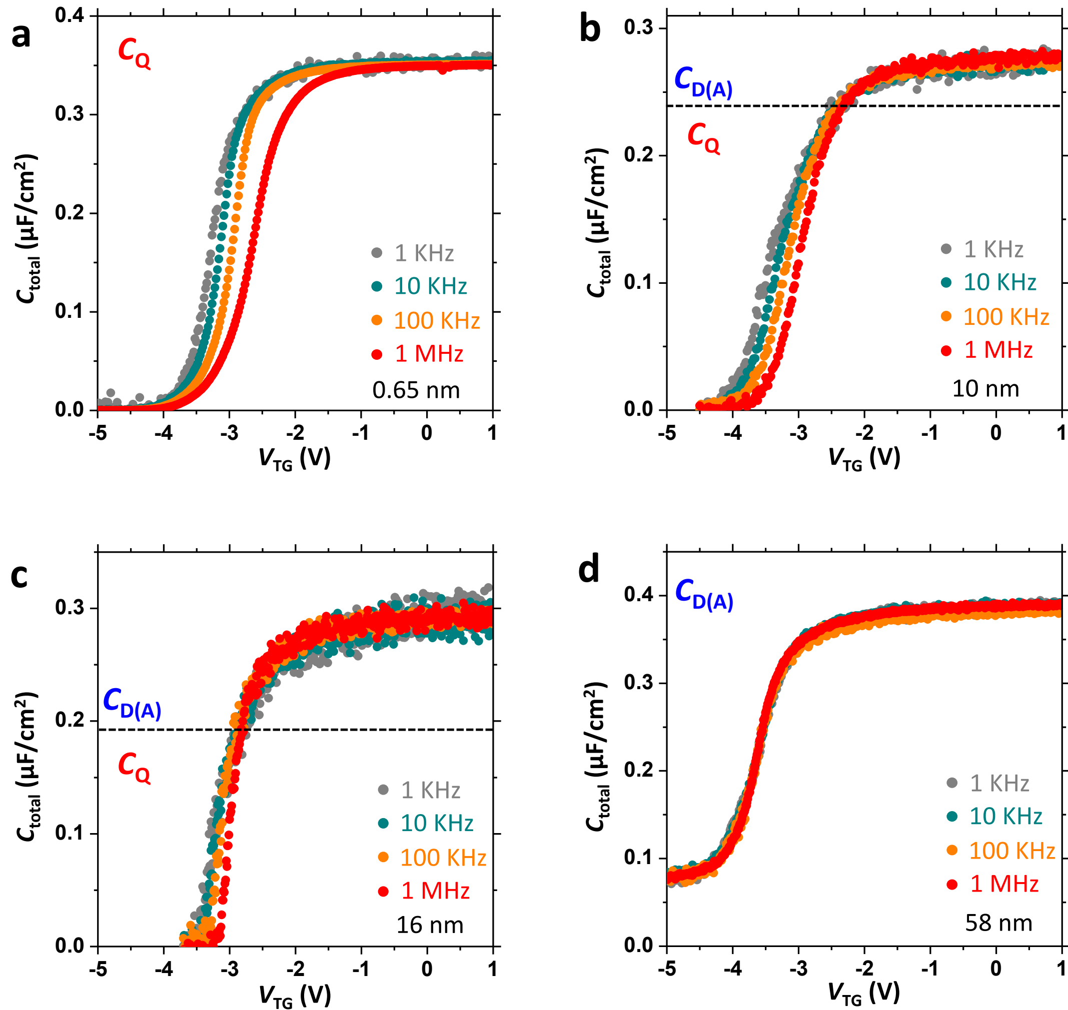


Fig. 3-16 C_{total}-V_{TG} characteristics of MoS_2 FETs with a thickness of 0.65, 10, 16, and 58 nm, respectively. Frequency ranges from 1 kHz to 1 MHz.

Thickness dependence of *C-V* is discussed in this subchapter. **Fig. 3-16** shows the experimental C_{total}-V_{TG} curves in the frequency range of 1 k - 1 MHz with t_{MoS2} = 0.65, 10, 16 and 58 nm, respectively. Since the parasitic capacitance is totally removed by using the quartz substrate, the minimum capacitance plateau observed for t_{MoS2} = 58 nm results from the contribution of C_D with W_{Dm}. That is, the inversion layer is formed, resulting in a constant depletion width. The electrical communication still passes through free electrons at the edge of the depletion region because the *p-n* junction is

formed between the inversion layer and ungated n-channel region. This *C*-*V* curve is consistent with that of a 1-μm-thick MoS_2 capacitor[18], which also supports that W_{Dm} is shorter than t_{MoS2} = 58 nm. This cannot occur in SB-FET but is unique to the depletion behavior in ACCU-FET. As a result, the undepleted MoS_2 layer will always remain, which results in residual conductance and low I_{ON}/I_{OFF} in *I*-*V*. On the other hand, for monolayer MoS_2, C_Q contributes to C_{total}, instead of C_D. It originates from the partially occupied *DOS* of CB modulated by the Fermi energy (E_F) in the Fermi-Dirac distribution as shown in subchapter 3.5. Distinct from C_D, one of the main behaviors of C_Q is that it follows an exponential decrease with respect to E_F when E_F is modulated in the band-gap. Due to the large band-gap of MoS_2, C_Q can reach a small value, which results in an extremely low carrier density. This will be experimentally observed as a decrease to almost zero in *C*-*V* and a clear subthreshold/off region in *I*-*V*. *C*-*V* of 10, 16-nm-thick MoS_2 FET also show similar C_Q behavior at fully depleted region. So the capacitance here is defined as C_{FULL-D}, which is similar to C_Q numerically. Thickness dependence of capacitance at depletion region will be discussed in the next subchapter firstly.

3.6.1 Thickness dependence of capacitance at depletion region

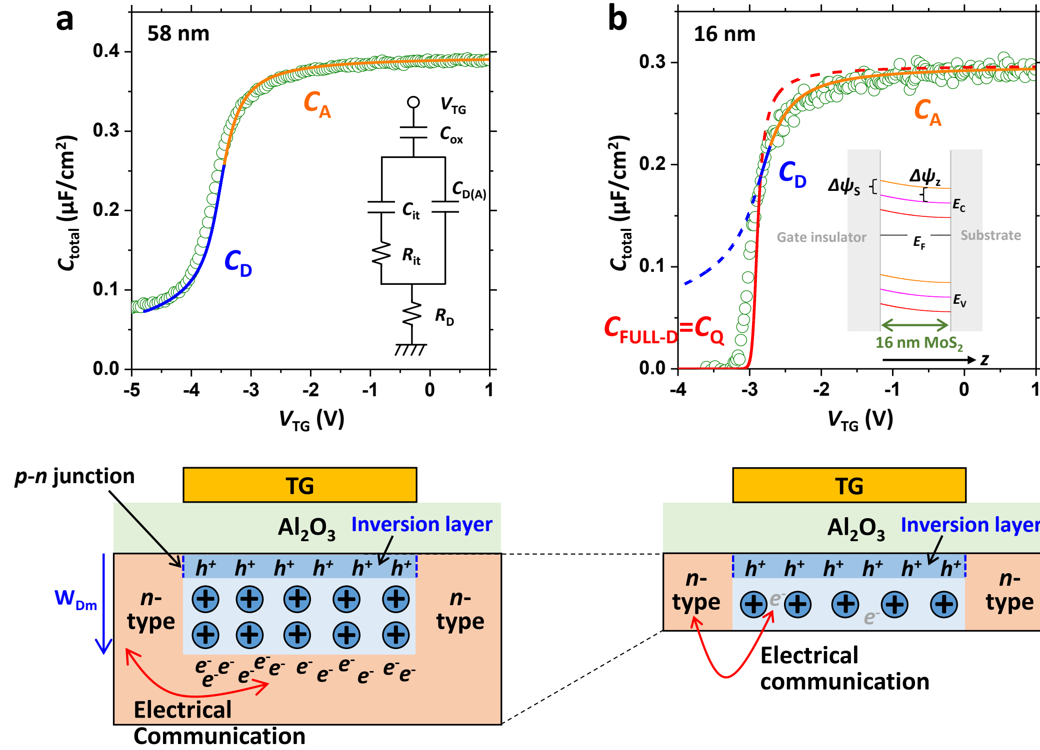


Fig. 3-17 (a) Depletion capacitance (accumulation capacitance) of a 58-nm-thick MoS_2 FET. The green circle is the experimental C_{total}-V_{TG} curve at 1 MHz from **Fig. 3-16**. The blue and orange solid lines are the theoretical fitting curve based on C_D and C_A ($C_{total} = \frac{C_{D(A)}C_{ox}}{C_{D(A)}+C_{ox}}$), respectively. The inset is the simplified lumped equivalent circuit to model bulk MoS_2-FET *C*-*V*. The bottom schematic shows the situation for $V_{TG} << 0$ V. **(b)** C_D-$C_{FULL\text{-}D(Q)}$ transition in a 16-nm-thick MoS_2 FET. The green circle is the experimental C_{total}-V_{TG} curve at 1 MHz from **Fig. 3-16**. The blue, orange and red solid lines are the theoretical plots based on C_D, C_A and $C_{FULL\text{-}D}$ ($C_{total} = \frac{C_{FULL-D}C_{ox}}{C_{FULL-D}+C_{ox}}$), respectively. The inset shows the potential distribution calculated as a function of MoS_2 thickness (z direction) at different values of ψ_s. The bottom schematic shows the situation for V_{TG} $<< 0$ V.

Now let us consider the thickness dependence of capacitance at the depletion region. Most of the measured MoS_2 FETs with t_{MoS2} > 55 nm show depletion capacitance (accumulation capacitance)-dominant *C*-*V* without thickness dependence as shown in **Fig. 3-17**. C_D and C_A are separated by flat-band voltage (V_{FB}). Moreover, channel resistance-induced frequency dispersion is totally suppressed because $R_{channel}$ is shunted by the unmodulated conductive MoS_2 region, which results in a low charging resistance R_D. Thus, the equivalent circuit can be simplified as a lumped circuit, and conventional $C_{D(A)}$ analysis method can be applied. This enables us to extract parameters such as N_D and ε_{MoS2} of bulk MoS_2. The minimum C_D is given as $Minimum\ C_D = \frac{\epsilon_{MoS2}}{W_{Dm}}$. By considering that W_{Dm} is 48~55 nm and the minimum C_D is ~ 0.1 μF/cm^2, bulk ε_{MoS2} is extracted as 6.3. This is roughly consistent with the calculated bulk ε_{MoS2} in the z direction [19]. N_D is determined to be $2\text{~}3\times10^{17}$ cm^{-3}. With these parameters, by using conventional C_D expression (Eq. s1-10 in Supplementary Information Note 2) and Eq.3-5 without C_{it}, the *C*-*V* of 58-nm-thick MoS_2 is fitted as shown in **Fig. 3-17 (a)**. The simulated *C*-*V* fits well with the experimental data. The slight deviation is due to C_{it}-induced distortion and the stretch-out effect.

C_D-$C_{FULL\text{-}D}$ transition always occurs at full depletion region for multilayer MoS_2 FET-based *C*-*V*. Firstly, free electrons at the edge of the depletion region still communicate electrically with S/D through the ungated *n*-channel region. By modulating V_{TG} negatively, the depletion width will reach t_{MoS2} (16 nm). As a result, the electrical communication in *C*-*V* occurs between S/D and the quite small density of free electrons in the "depletion region". Based on this scenario, when the depletion width reaches t_{MoS2}, it can be considered that the C_D-$C_{FULL\text{-}D}$ transition occurs, since the carrier density in the "depletion region" can be controlled by $C_{FULL\text{-}D}$. Therefore, the *C*-*V* curve goes to zero even for the multilayer. After the whole channel is depleted, the surface potential will be continuously increased by further decreasing V_{TG}. Finally, the inversion layer will be formed. However, inversion capacitance corresponding with the *p*-branch in *I*-*V* cannot be observed because of the *p*-*n* junctions, as schematically illustrated in **Fig. 3-17 (b)**.

Now, let us reproduce the *C-V* curve for t_{MoS2} = 16 nm by simple analytical calculation. Since the expression for $C_{D(A)}$ is already obtained, the surface potential (ψ_s) is calculated in order to obtain the expression for C_{FULL-D} of multilayer MoS_2. The boundary condition of electric field = 0 at z = t_{MoS2} is used for the solution of the one-dimensional Poisson equation. This is the intrinsic condition for the present 2D-FET structure, where the channel is always surrounded by the insulator or other insulating environment [20]. The calculated potential distribution is shown in the inset in **Fig. 3-17 (b)**. By modulating the surface potential with the change of $\Delta\psi_s$, the potential in the channel changes everywhere ($\Delta\psi_z$) with the same value, that is, $\Delta\psi_z = \Delta\psi_s$, indicating that the whole channel can be fully controlled by ψ_s and ψ_s has a similar function as E_F in monolayer C_Q to modulate n_{ch}. By following the similar expression in monolayer MoS_2, C_{FULL-D} is also represented as C_Q. With the calculated potential distribution, C_{FULL-D} is shown below (Supplementary Information Note 2):

$$C_{FULL-D} = C_Q = N_Q \exp(\frac{e\psi_S}{k_B T}), \quad (3\text{-}8)$$

where N_Q is a constant independent of ψ_s. It is not surprising to see that C_Q in the multilayer has a similar formula as that in the monolayer case with the same exponential e/k_BT dependence. Then, using C_Q and $C_{D(A)}$ without C_{it}, the experimental data are well fitted. The cross point indicates the transition from C_D to C_Q at $t_{MoS2} = W_D$. The slight deviation from the analytical C_Q comes from the contribution of C_{it}. In **Fig. 3-16 (b,c)**, the transition from C_D to C_Q is clearly seen with decreasing MoS_2 thickness. Moreover, it is interesting that the frequency dispersion is observed only in the C_Q-dominant region. This is because the charging resistance R_D is low enough for the $C_{D(A)}$-dominant region, while $R_{channel}$ is quite high for the C_{FULL-D} dominant region.

3.6.2 Thickness dependence of capacitance at accumulation region

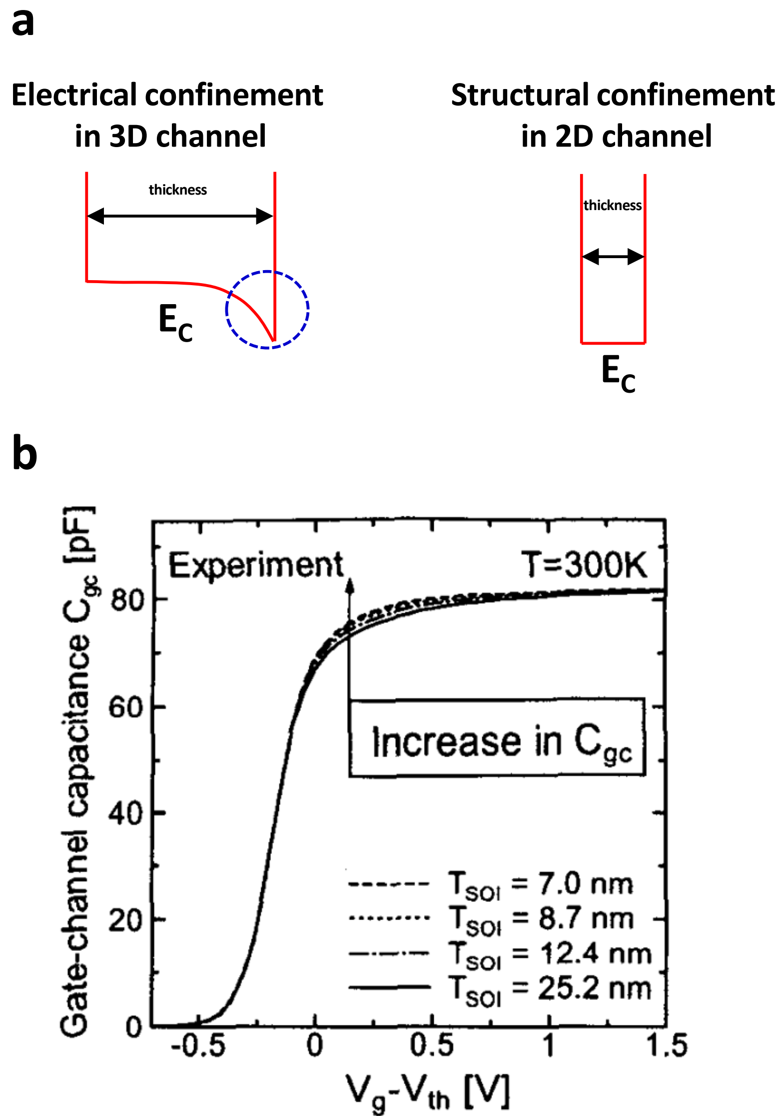


Fig. 3-18 (a) Schematic to show electrical confinement effect in bulk 3D channel and structure confinement in 2D channel. **(b)** Gate-channel capacitance as a function of V_G-V_{TH} for SOI FET with different SOI thickness [23].

In the last subchapter, capacitance thickness dependence was discussed at depletion region. In this subchapter, quantum-mechanical effect will be studied at accumulation region. In conventional Si/SOI MOSFET structure, quantum-mechanical effect is focused on the inversion region where device works at the on-state [21-23].

Large band bending will be introduced at the surface as shown in **Fig. 3-18**, which results in the strong electrical confinement effect. As a result, 2DEG channel is formed at the surface of 3D bulk materials. By decreasing the thickness of SOI to 7 nm, slight increase of C_{GC} is observed, which is due to the structure confinement effect. While in recent 2D-materials, channel thickness can be reduced to below 1 nm, which should show much stronger quantum-mechanical effect than that in SOI case. Since quantum capacitance of monolayer MoS_2 has been clarified in subchapter 3.5, it will be extended to multilayer MoS_2 case in this subchapter in terms of quantum-mechanical effect.

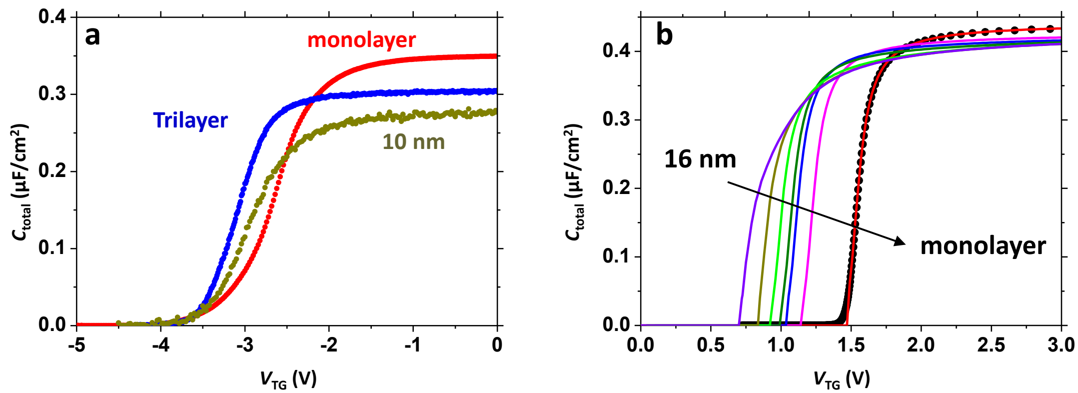


Fig. 3-19 (a) Experimental C_{total}-V_{TG} characteristics at 1 MHz of MoS_2 FETs with a thickness of mono-, tri-layer and 10 nm, respectively. **(b)** Simulated C_{total}-V_{TG} characteristics of MoS_2 FETs with a thickness of mono-, bi-, tri-layer, 2.6 nm, 5nm, 10 nm and 16nm, respectively. Black dot is the quantum capacitance of 2D-limit, which has been discussed in subchapter 3.5.

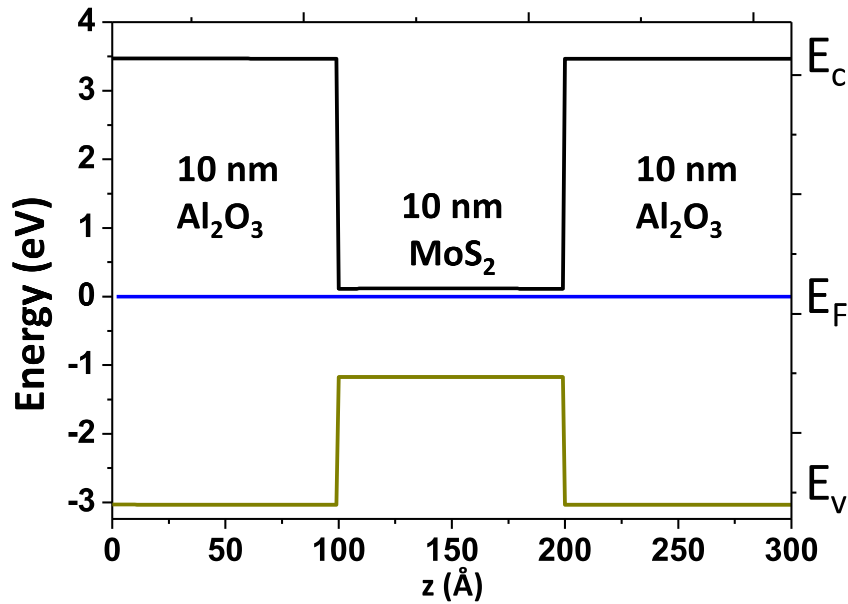


Fig. 3-20 Energy band diagrams of 10-nm Al_2O_3/10-nm MoS_2/10-nm Al_2O_3 structure at almost flat band voltage case at thickness direction. Gate voltage will be applied on left side insulator. Right side insulator will be used as substrate. The type of substrate insulator will not affect the simulation results.

Fig. 3-19 shows the experimental C_{total}-V_{TG} curves in the frequency of 1 MHz with t_{MoS2} = mono-, tri-layer, and 10 nm, respectively. Monolayer *C-V* shows highest saturation capacitance and sharpest change at accumulation region. Trilayer *C-V* still shows sharp change but saturation capacitance decreases. While 10-nm-thick MoS_2 *C-V* shows lowest saturation capacitance and slowest change to accumulation region. Compared with SOI in **Fig. 3-18(b)**, strong thickness dependent *C-V* curves due to quantum-mechanical effect have been observed in 2D materials. This thickness dependence of this *C-V* curve is reproduced by solving Poisson equation and Schrödinger equation self-consistently [21]. The Schrödinger equation is solved in the effective mass approximation using a freely available tool by incorporating material properties specific to the device [24]. The energy band diagrams at almost flat band voltage for 10-nm Al_2O_3/10-nm MoS_2/10-nm Al_2O_3 are shown in **Fig. 3-20**. By changing the thickness of MoS_2 from monolayer to 16 nm at different gate bias, **Fig. 3-**

19 (b) is reproduced. Van der Waals energy gap is not considered in our model. **Fig. 3-21(a)** shows the effective electric field (E_{eff}) under external electric field (E_{ext}) for different layer numbers of MoS_2 when Van der Waals energy gap is considered [25]. By increasing the layer number of MoS_2, E_{eff} is reduced. Since ε_{MoS2} is determined by the ratio of the external and internal fields, ε_{MoS2} will have the layer number dependence, which is calculated in **Fig. 3-21 (b)**. Thicker MoS_2 has smaller ε_{MoS2}. Although we have not considered the Van der Waals energy gap in our model, we used layer number dependent ε_{MoS2} from the reports of first-principle calculation [26, 27]. The parameters of MoS_2 used in the simulation is shown in **Table 3.1.**

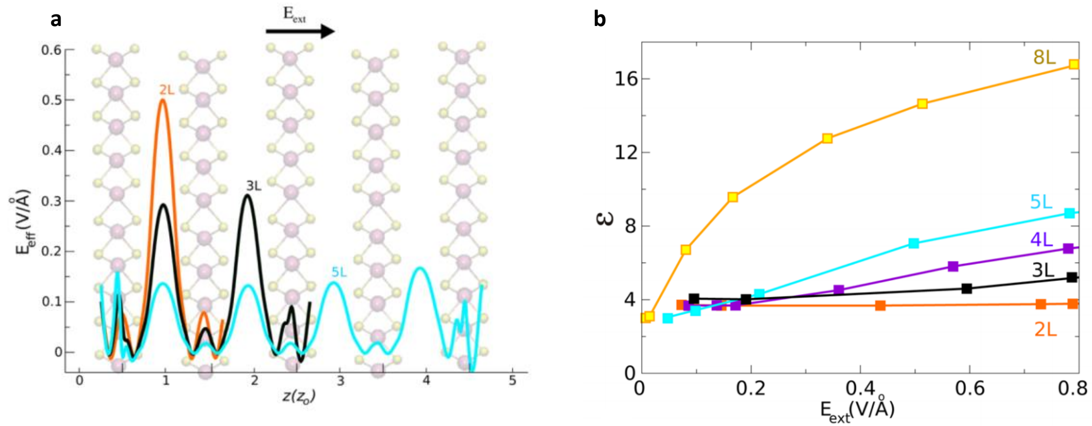


Fig. 3-21 (a) E_{eff} as a function of z direction for 2L, 3L, 5L MoS_2, respectively. The black arrow indicates the direction of constant E_{ext}. **(b)** Calculated dielectric constant as a function of E_{ext} for 2L-8L MoS_2, respectively. [25]

	Dielectric constant	Effective mass	N_D (cm^{-3})
monolayer	3.0	0.73	3×10^{17}
bilayer	4.2	0.73	3×10^{17}
bulk	6.3	0.73	3×10^{17}

Table 3.1 MoS_2 Parameters used in the simulation. [26, 27]

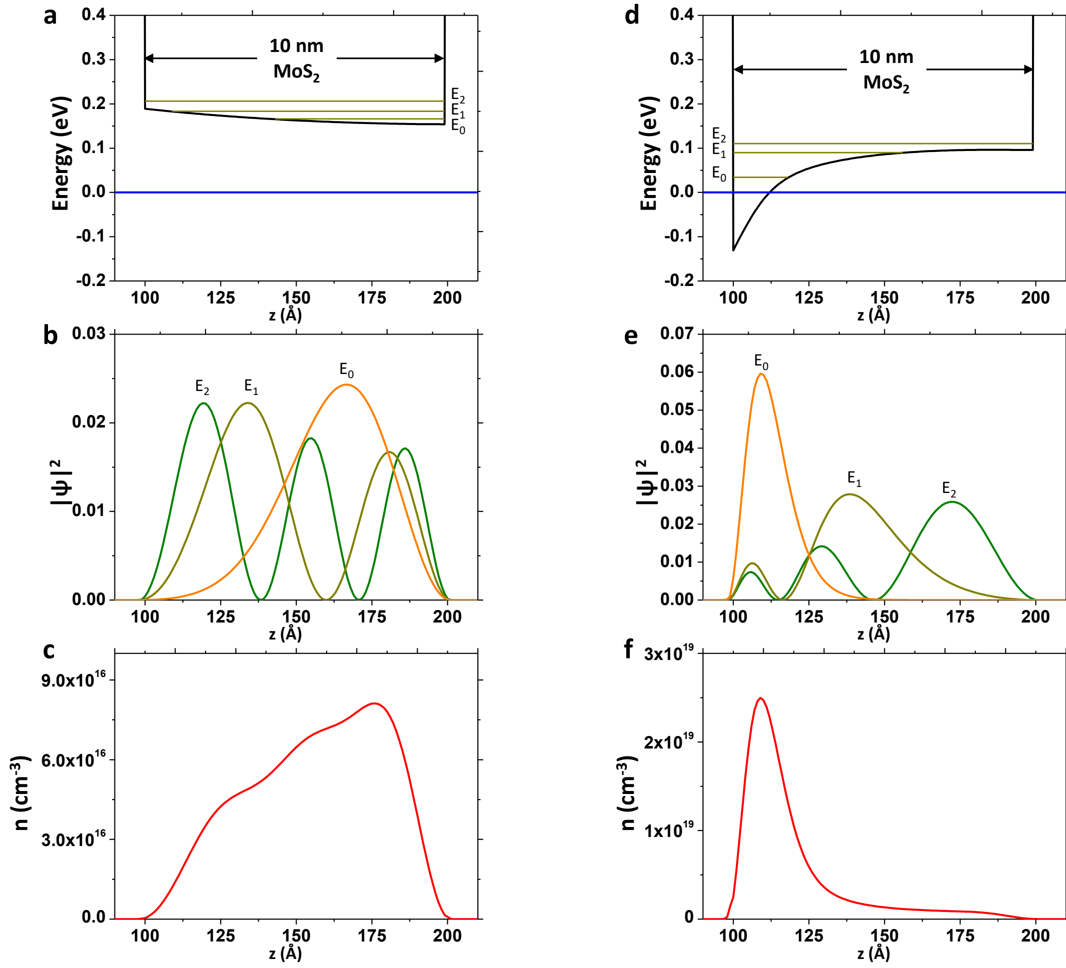


Fig. 3-22 **(a)** Energy band diagrams of 10-nm Al_2O_3/10-nm MoS_2/10-nm Al_2O_3 structure at weak depletion region. Gate voltage is applied on left side insulator. E_0, E_1 and E_2 indicate eigenvalues of three lowest subbands. **(b)** Square modulus of wave function of each subband. **(c)** Electron density thickness distribution. The strong accumulation case is shown in **(d, e, f)**.

Fig. 3-22 (a, b) shows calculated three lowest subband energy and square modulus of each subband when t_{MoS2} = 10 nm. Energy difference between the subband is smaller than k_BT, which makes all these subbands occupied. As a result, channel electron density (n) is distributed in the whole channel region as shown in **Fig. 3-22 (c)**. By applying positive gate bias, the strong accumulation can be obtained. Energy difference between E_0 and E_1 is increased due to triangle potential confinement effect at the surface as shown in **Fig. 3-22 (d)**. As a result, most of electrons only locate in lowest energy

subband E_0 and wave function of E_0 is confined in this triangle potential well. This makes centroid of electron distribution to be ~ 1-2 nm from surface.

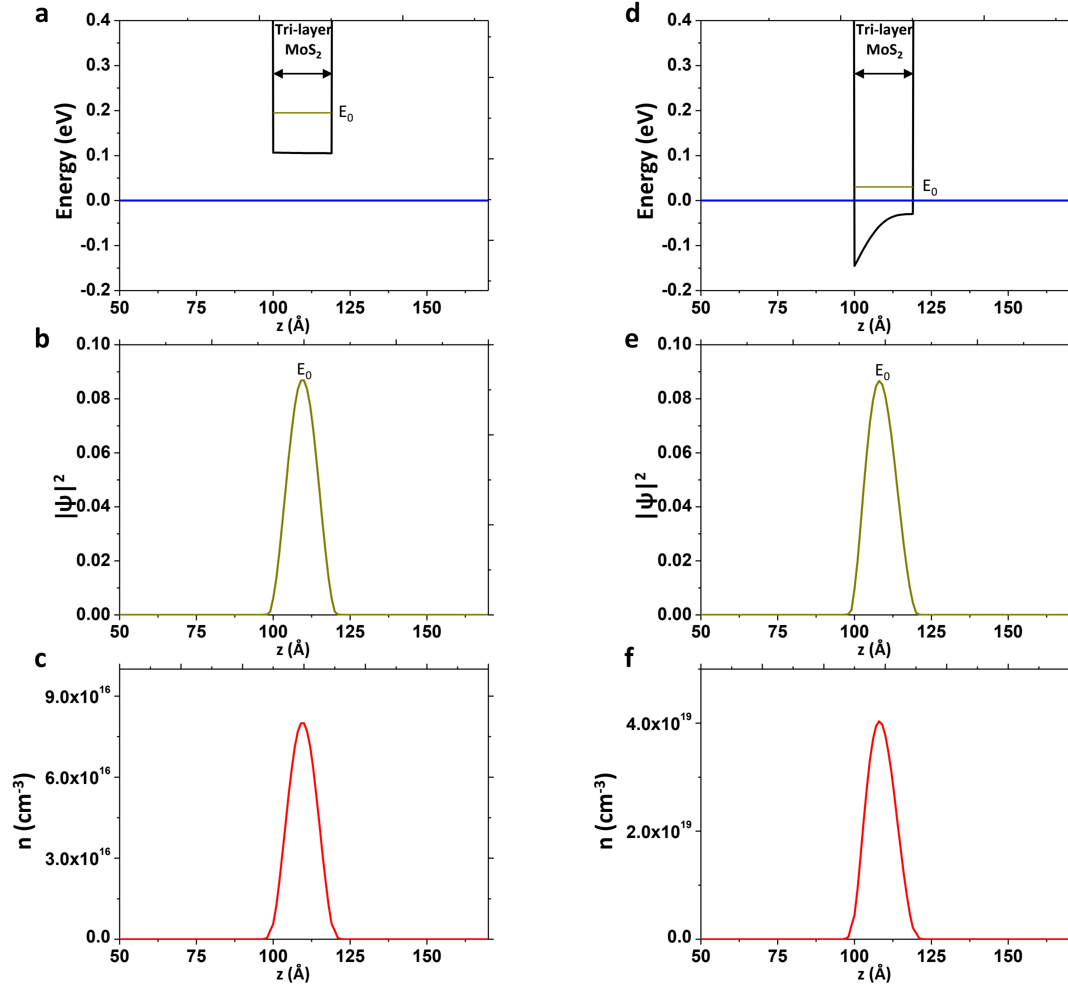


Fig. 3-23 **(a)** Energy band diagrams of 10-nm Al_2O_3/tri-layer MoS_2/10-nm Al_2O_3 structure at weak depletion region. Gate voltage is applied on left side insulator. E_0 indicates eigenvalue of lowest subband. **(b)** Square modulus of the subband. **(c)** Electron density thickness distribution. The strong accumulation case is shown in **(d, e, f)**.

Fig. 3-23 shows the trilayer MoS_2 situation. Most of the electrons only occupy E_0 subband even at weak depletion case as shown in **Fig. 3-23 (a-c)**. Electron distribution is confined into ~2 nm channel. By applying positive gate bias, the channel is accumulated. Thus E_F gets close to E_0 and band bending also occurs. However, the band

bending will not affect electron distribution much. As a result, subband E_0 dominates the carrier modulation from depletion to accumulation, which indicates the intrinsic 2D electron gas (2DEG) channel due to the ultra-thin thickness confinement effect. It is different from 2DEG in conventional inversion region of Si MOSFET, which is introduced by the electrical field. The simple way to estimate how thin is needed to form intrinsic 2DEG can be done as follows.

$$E_n = \frac{\hbar^2 \pi^2 n^2}{2m_{n-mos2} t_{mos2}^2} \tag{3-9}$$

Eq. 3-9 shows energy eigenvalues of a quantum well. When the energy difference between n=1 and 2 is larger than $3k_B T$, we can consider that only lowest subband is occupied. The intrinsic 2DEG channel also explains why trilayer and monolayer *C-V* changes more quickly than in the thick 10-nm-thickness case. As for atomically thin MoS_2, applied gate voltage will directly modulate E_F of the lowest subband, which is same as C_Q in monolayer case. While for thick MoS_2 case, electrons distribute along the whole 3D channel at the weak accumulation and depletion region. As a result, gate electrical field will be partially screened by the channel at *z*-direction, which results in degraded capacitance modulation by the gate voltage.

The next task is to explain why saturation capacitance drastically increases in monolayer MoS_2 case. **Fig. 3-24** shows square modulus of the wave function of lowest subband with different MoS_2 thickness at strong accumulation region. As we can see, in 10 nm-thick MoS_2 case, the centroid of wave function is confined by band bending induced potential well instead of its body thickness. The distance between centroid wave function and gate insulator interface (t_{accu}) is ~ 1 nm. By decreasing MoS_2 thickness, the centroid gets close to interface due to the confined channel. In the monolayer case, t_{accu} is ~ 0.2 nm.

This t_{accu} thickness dependence will severely affect accumulation capacitance. Accumulation capacitance can be shown as Eq. 3-10.

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{Q(DOS)}} + \frac{t_{accu}}{\varepsilon_{mos2}}. \tag{3-10}$$

In subchapter 3.5, C_Q of monolayer MoS_2 has been studied. t_{accu} is not considered

in C_Q of monolayer MoS_2 because t_{accu} is only ~ 0.2 nm. This explains why only C_Q is enough to explain *C-V* in monolayer MoS_2. While in thick MoS_2, t_{accu} is ~ 1 nm. This will severely degrade C_{total}. At strong accumulation region, saturation capacitance is obtained due to very large $C_{Q(DOS)}$. As a result, Eq. 3-10 can be simplified as $1/C_{total} = 1/C_{ox} + t_{accu} / \varepsilon_{mos2}$. t_{accu} thickness dependence explains the reason why saturation capacitance decrease by increasing MoS_2 thickness.

Eq. 3-10 indicates that measured C_{total} at strong accumulation region will be smaller than C_{ox} due to quantum mechanical effect. **Fig. 3-25 (a)** shows how C_{total} deviates from C_{ox}. When EOT = 7.8 nm, the loss of capacitance is only 8 % in multilayer case. While when EOT = 1 nm, the loss of capacitance is as high as 20 %. The use of monolayer MoS_2 will definitely increase accumulation capacitance, especially for thin EOT case. This has been experimentally confirmed by *C-V* measurement as shown in **Fig. 3-25 (b)**. Although the variation is observed from sample to sample, monolayer MoS_2 saturation capacitance is unambiguously larger than that of thicker MoS_2. The above study indicates that the use of monolayer 2D materials will obviously increase carrier injection efficiency in the channel by field-effect.

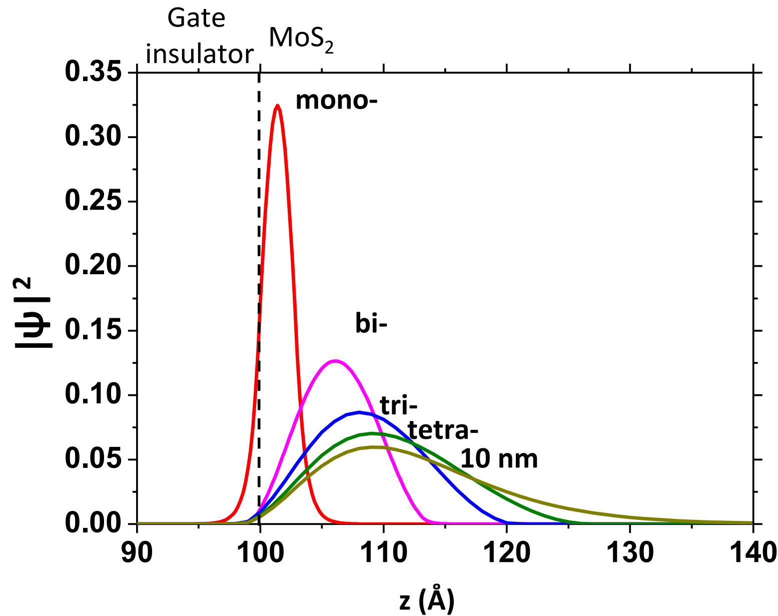


Fig. 3-24 Square modulus of wave function of lowest subband with MoS_2 thickness ~ mono, bi, tri, tetra-layer, 10nm at strong accumulation region, respectively.

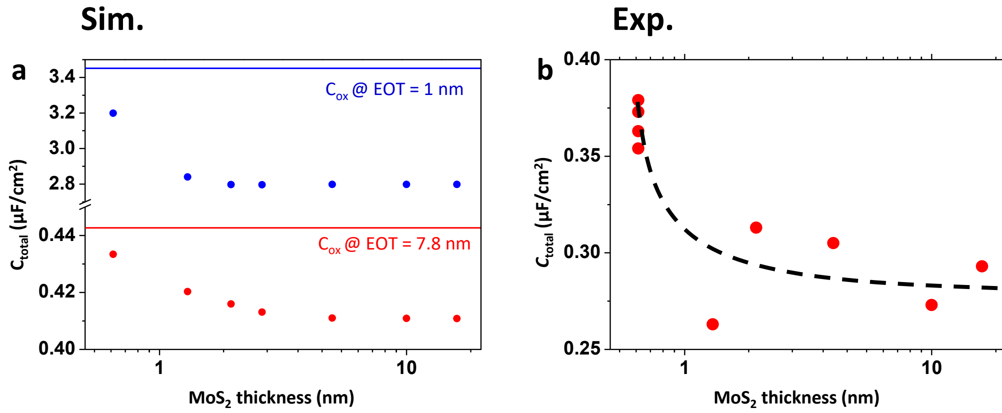


Fig. 3-25 (a)Simulated C_{total} and (b) experimental C_{total} at strong accumulation region with difference MoS_2 thickness.

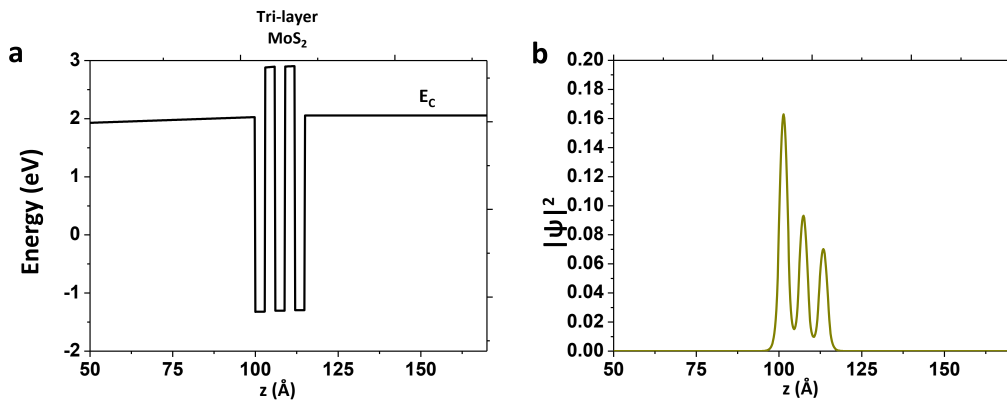


Fig. 3-26 (a) Energy band diagrams of 10-nm Al_2O_3/tri-layer MoS_2/10-nm Al_2O_3 structure at accumulation region by including Van der Waals energy gap. Gate voltage is applied on left side insulator. **(b)** Square modulus of the lowest subband.

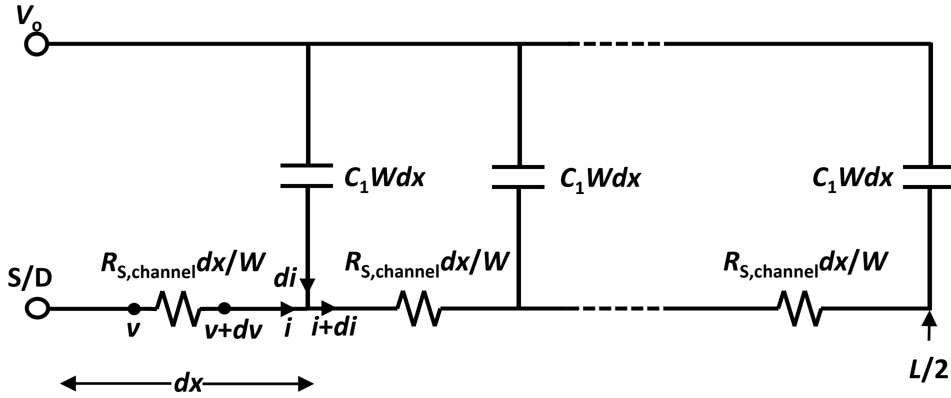
Van der Waals energy gap is not considered in the previous simulation. In **Fig. 3-26**, we show the simulation of tri-layer MoS_2 with including Van der Waals energy gap. By including the Van der Waals energy gap, the Square modulus of subband shows three peaks, which corresponds to three layers, respectively. The detailed analysis of Van der Waals energy gap is needed for further study.

3.7 Summary

In this chapter, *C-V* characterization of MoS_2 FET structure has been systematically studied. Parasitic capacitance was totally removed by using the insulating quartz substrate. Resistance effect was carefully checked, which is one of the main origins for the observed frequency dispersion in fully-depleted region of MoS_2 FET. Quantum-mechanical effect was also investigated from monolayer to bulk MoS_2.

Supplementary Information

Note 1. MoS_2 Channel resistance effect on capacitance measurement.



Supplementary Fig. 1 Transmission line equivalent circuit of MoS_2 FET. This equivalent circuit is valid when the whole channel of MoS_2 is depleted.

Transmission line model has been applied to study channel resistance effect on *C-V* for Si MOSFET[7,8]. Here, transmission line model will also be used in MoS_2 FET to model $R_{channel}$ effect as shown in **Supplementary Fig. 1**. Notice that substrate is insulating in MoS_2 FET, which simplifies the mathematical expressions of equivalent circuit by neglecting charge supply from the substrate. Assume that all variables are in phasor quantities. v_0 refers to small ac variation. $R_{S,channel}$ refers to sheet resistance of $R_{channel}$. i refers to current from one side (source or drain) of the electrode. So the total current from both sides $i_{D,S}$ is $2\times i$.

Firstly,

$$\frac{dv}{dx} = -\frac{R_{S,channel}}{W} i , \quad \text{(S-1)}$$

$$\frac{di}{dx} = j\omega C_1 W (v_0 - v) . \quad \text{(S-2)}$$

Differentiating Eq. S-1 with respect to *x* and substituting it into Eq. S-2,

$$\frac{dv^2}{dx^2} = -j\omega C_1 R_{S,channel}(v_0 - v) \tag{S-3}$$

Assume $u = v - v_0$, we have:

$$\frac{du^2}{dx^2} = \gamma^2 u \quad , \tag{S-4}$$

where $\gamma = \sqrt{R_{S,channel} j\omega C_1}$.

The solution of this Eq. S-4 is

$$u = Ae^{-\gamma x} + Be^{\gamma x} \tag{S-5}$$

Based on the boundary conditions,

$v = 0$ when $x = 0$ and $\frac{dv}{dx} = 0$ when $x = \frac{L}{2}$, we have:

$$A = \frac{v_0}{e^{-\gamma L} + 1}, \quad B = -\frac{e^{-\gamma L} v_0}{e^{-\gamma L} + 1}. \tag{S-6}$$

Based on Eq. S-1 at $x = 0$, source/drain current:

$$i_{DS} = 2i = -\frac{2W}{R_{S,channel}} \frac{dv}{dx} = LWj\omega C_1 v_0 \frac{\tanh \frac{L\gamma}{2}}{\frac{L\gamma}{2}} \tag{S-7}$$

The propagation constant λ and channel resistance limited time constant τ_{Rch} are given as below:

$$\lambda = \frac{L\gamma}{2} = \sqrt{j\omega\tau_{Rch}}, \quad \tau_{Rch} = \frac{C_1 R_{S,channel} L^2}{4}. \tag{S-8}$$

So the experimental measured equivalent parallel capacitance and conductance C_{total} and G_{total} are:

$$C_{total} = C_1 \operatorname{Re}\left[\frac{\tanh\lambda}{\lambda}\right], \quad \frac{G_{total}}{\omega} = -C_1 \operatorname{Im}\left[\frac{\tanh\lambda}{\lambda}\right] \tag{S-9}$$

Note 2. $C_{FULL\text{-}D(Q)}$-C_D transition at depletion region.

Classical depletion capacitance (accumulation capacitance) expression of MoS_2 is given below by neglecting holes[28],

$$C_{D(A)} = \frac{\varepsilon_{MoS2}}{\sqrt{2}L_D} \frac{\left| \exp(\frac{e\psi_S}{k_B T}) - 1 \right|}{\sqrt{\exp(\frac{e\psi_S}{k_B T}) - \frac{e\psi_S}{k_B T} - 1}} . \quad \text{(S-10)}$$

Notice that often used E_F in monolayer MoS_2 discussion is unsuitable in multilayer and bulk MoS_2 since potential ψ changes from surface to body. Instead, surface potential ψ_S is used.

By neglecting free carriers in the depletion region, the depletion layer width is shown as:

$$W_D = \sqrt{\frac{2\varepsilon_{MoS2}\psi_S}{eN_D}} . \quad \text{(S-11)}$$

As for bulk MoS_2 (Thickness > 55 nm), W_{Dm} is obtained when ψ_S saturates at strong inversion region. While for multilayer MoS_2 (Thickness < 35 nm), transition from depletion capacitance to full depletion capacitance (quantum capacitance) occurs when W_D reaches MoS_2 body thickness. Transition condition of ψ_S is given as below:

$$\psi_{S(D\to Q)} = \frac{eN_D t_{MoS2}^2}{2\varepsilon_{MoS2}} . \quad \text{(S-12)}$$

Thickness of MoS_2 is defined as t_{MoS2}. Quantum capacitance is calculated based on Poisson equation and boundary conditions.

The potential distribution is firstly calculated. Parabolic function is used due to Poisson equation as shown:

$$\psi_X = C_0 + C_1 z + C_2 z^2 . \quad \text{(S-13)}$$

One dimension Poisson equation is given as below:

$$\frac{d^2\psi_z}{dz} = \frac{-eN_D}{\varepsilon_{MoS2}} = A . \quad \text{(S-14)}$$

Two boundary conditions are given below:

(1) Potential at surface (z=0) is ψ_S.

$$\psi_z\big|_{z=0} = \psi_S \,. \tag{S-15}$$

(2) The electric field at $z=t_{MoS2}$ is approximately zero, which is due to insulating quartz substrate.[5]

$$\left.\frac{d\psi_z}{dz}\right|_{z=t_{MoS2}} = 0 \,. \tag{S-16}$$

This condition is the intrinsic condition for present 2D-FET structure, where channel is always surrounded by the insulator or environment and is important for obtaining C_Q dominant region. Either additional making metal contact to MoS_2 such as capacitor structure or $t_{MoS2}>W_{Dm}$ will degrade this condition to conventionally used one, that is ψ_∞=0.

Using from Eq. S-13 to eq. S-16, potential distribution is obtained as

$$\psi_z = \frac{Az^2}{2} - At_{MoS2}z + \psi_S = f(z) + \psi_S \,. \tag{S-17}$$

Then free electron statistics is calculated. Free electron density per unit volume at position z is written as

$$n(z) = N_D \exp\left(\frac{e\psi_z}{k_B T}\right) . \tag{S-18}$$

By integrating Eq. S-18 with z from 0 to t_{MoS2}, and replacing ψ_z with Eq. S-17, we get total channel free electron per unit area as:

$$n_{ch} = N_D \exp\left(\frac{e\psi_S}{k_B T}\right)\int_0^{t_{MoS2}} \exp\left(\frac{ef(z)}{k_B T}\right) d_z \,. \tag{S-19}$$

Quantum capacitance is calculated from the definition $C_Q = \frac{dn_{ch}}{d\psi_S}$, which is given as below:

$$C_Q = \frac{en_{ch}}{k_B T} = N_Q \exp\left(\frac{e\psi_S}{k_B T}\right)$$,where constant

$$N_Q = \frac{eN_D \int_0^{t_{MoS2}} \exp\left(\frac{ef(z)}{k_B T}\right) d_z}{k_B T} \,. \tag{S-20}$$

To simplify the calculation of N_Q, capacitance continuity condition is finally used. That is

$$C_D = C_Q \left| \psi_S = \psi_{S(D \to Q)} \right. . \tag{S-21}$$

Capacitance in multilayer MoS_2 (C_{MoS2}) is given by two piece-wise functions combined with Eq. S-10,12,20,21,

$$C_{MoS2} = \begin{cases} C_D, \psi_S > \psi_{S(D \to Q)} \\ C_Q, \psi_S < \psi_{S(D \to Q)} \end{cases} . \tag{S-22}$$

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4 MoS_2/high-*k* interfacial properties

I-*V* and *C*-*V* mechanism have been systematically studied in the last two chapters. It comes to the stage to study MoS_2/high-*k* interfacial properties in this chapter based on these two methods.

In this chapter, D_{it} will be extracted by both *I*-*V* and *C*-*V* from monolayer to bulk MoS_2. The origin of D_{it} will be investigated, which will be supported by photoconductivity measurement. Finally, MIT behavior will be explained in terms of C_Q and C_{it}.

4.1 D_{it} extraction method

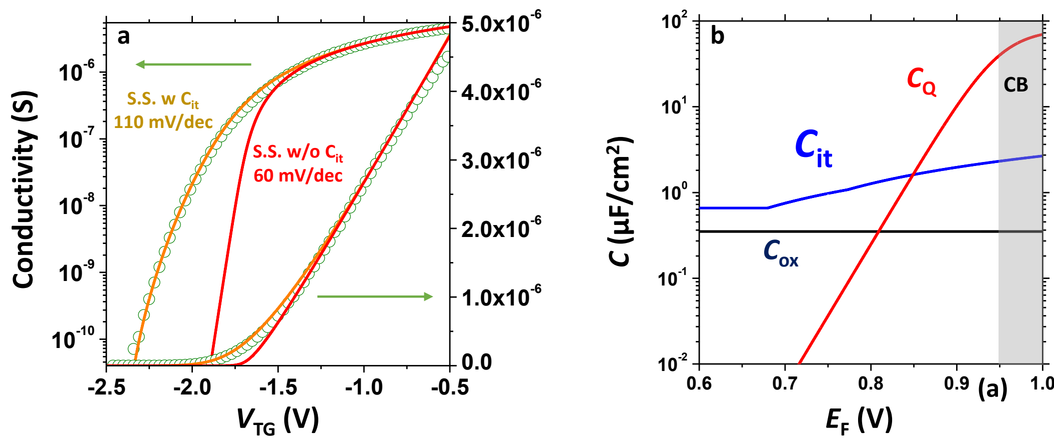

Fig. 4-1 (a) Transfer characteristics of a 0.65-nm-thick MoS_2 ACCU-FET. The green circuit is the experimental σ-V_{TG} curve. The red solid lines are the theoretical fitting curves without C_{it} and orange lines are the theoretical fitting curves with C_{it}. **(b)** Extracted C_{it} from *I*-*V*.

I-V and C-V have been studied in the last two chapters. In this chapter, MoS_2/high-k interfacial properties will be studied by these two methods.

As for the bulk sample, Terman method is suitable for D_{it} estimation [1]. As we can see in **Fig. 3-17 (a)**, the Experimental C-V curve in 58 nm sample (>W_{Dm}) slightly deviates from simulation due to C_{it}-induced distortion and stretch-out effect, which enables us to extract D_{it} based on Terman method.

As for ultra-thin sample, especially for monolayer sample, conventional high-low frequency method or Terman method is not suitable for extracting D_{it} due to channel charging effect. The reliable D_{it} estimation method for the thin sample should include channel charging effect, which will be shown below.

D_{it} is firstly extracted from I-V. As for vertical axis, based on the drift current model, conductivity $\sigma = en_{ch}\mu$. n_{ch} is estimated by C_Q in monolayer, which has been confirmed in subchapter 3.5. μ is assumed to be constant, which is experimentally extracted from the linear region of I-V. As for horizontal axis, the existence of D_{it} degrades the V_G-E_F relation based on Eq. 3-5. Since both C_Q and C_{ox} are experimentally confirmed by capacitance measurement, the only unknown parameter in Eq. 3-5 is C_{it}. The simulation results of monolayer sample are shown in **Fig. 4-1**. Ideal $S.S.$ of ~60 mV/dec can be obtained without C_{it} effect, which comes from the thermal limitation in C_Q. Experimental I-V from off to linear region is then fully reproduced by including C_{it} as shown in **Fig. 4-1(b)**. Clear band-tail shape C_{it} close to CB is observed. $S.S.$ degrade as well as the gradual transition from linear to the subthreshold region in the linear region. In the ACCU-FET, the equation to describe $S.S.$ is given equivalently with the conventional MOSFET as:

$$S.S. = \ln 10 \frac{k_B T}{e} \frac{C_{ox} + C_{it}}{C_{ox}}. \quad (4\text{-}1)$$

This equation is valid from the monolayer to multilayer when $t_{MoS2} \ll W_{Dm}$. $S.S.$ will be degraded when t_{MoS2} get close to or larger than W_{Dm} due to losing the gate control of the whole channel. D_{it} extracted from on-region of I_D-V_G should be avoided in this method.

The extracted C_{it} in **Fig. 4-1(b)** is further confirmed by C-V as shown in subchapter

3.4. When C_{it} is not included in transmission line model as shown in Supplementary Information Note 1, channel charging effect induced frequency dispersion in **Fig. 4-2** is totally different from experimental results as shown in **Fig. 3-10**. Simulation results in **Fig. 3-10 (c,d)** reproduce experimental *C*-*V* and *C*-*f* curves well by including the band-tail shape C_{it} as shown in **Fig. 4-1 (b)**. As a summary, C_{it} in monolayer MoS_2 is successfully extracted by *I*-*V*, which is further confirmed by *C*-*V*. Since C_{it} can be directly extracted from *I*-*V*, *I*-*V* will be focused in the following part to study MoS_2/high-*k* interface.

Several low-quality samples from the monolayer to bulk MoS_2 show humps in both *I*-*V* and *C*-*V* as shown in **Fig. 4-3**. The humps here indicates D_{it} peaks.

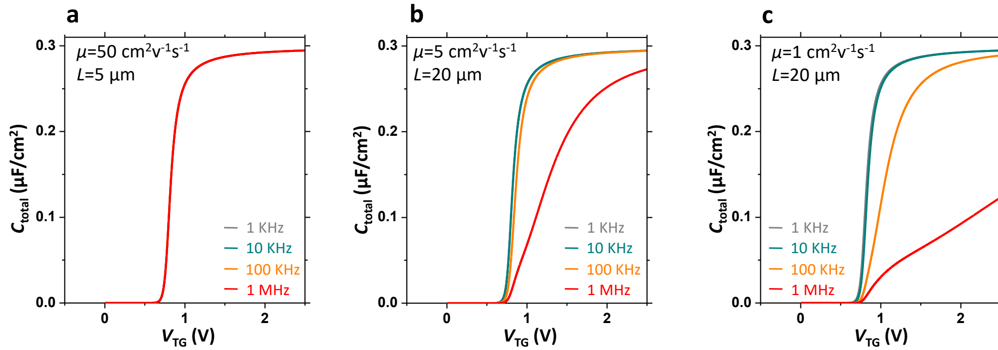

Fig. 4-2 (a,b,c) Calculated plot of C_{total}-V_{TG} curves at different μ and *L* but without C_{it}. Although frequency dispersion is observed, experimental C_{total}-V_{TG} curves in **Fig. 3-10(a)** cannot be reproduced.

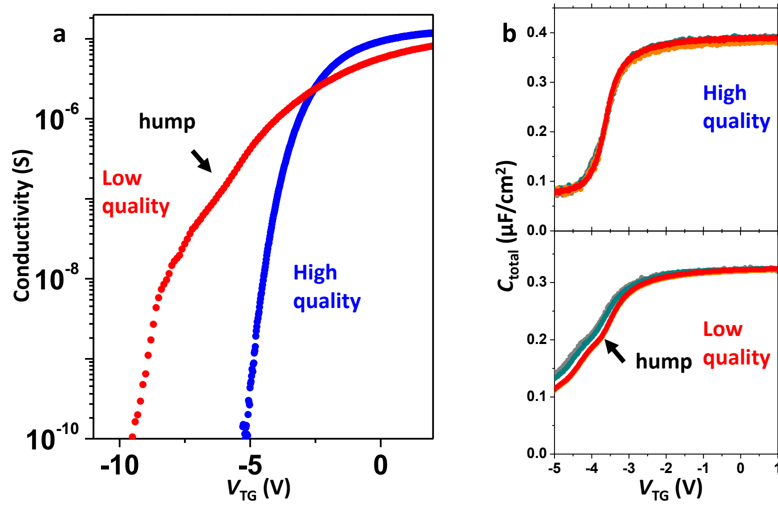

Fig. 4-3 (a) σ–V_{TG} characteristics at V_{DS} = 0.1 V of monolayer MoS_2 with high quality and low quality, respectively. **(b)** C_{total}-V_{TG} characteristics of two bulk MoS_2 FETs with a thickness > W_{Dm}. Frequency ranges from 1 kHz to 1 MHz.

4.2 MoS_2/high-*k* interfacial properties

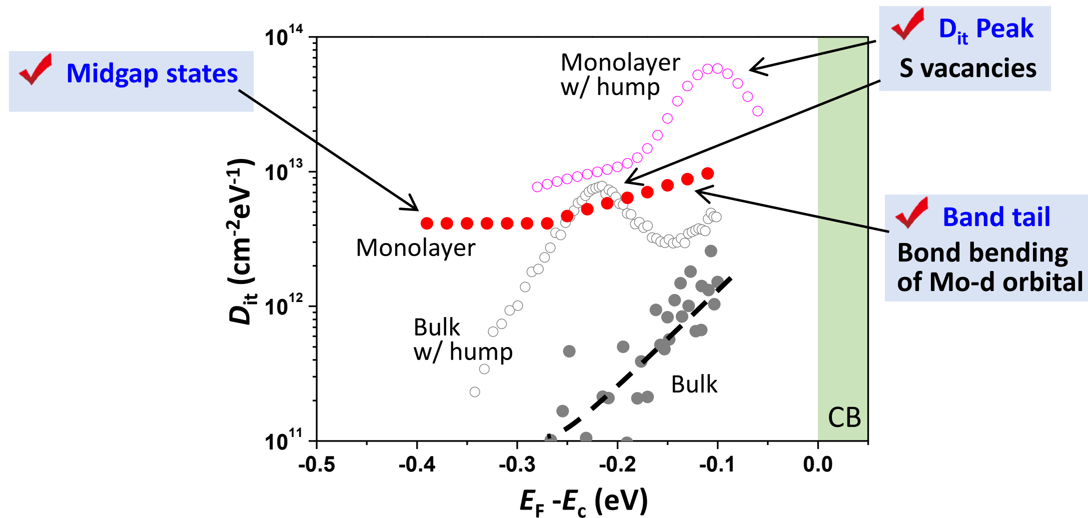

Fig. 4-4 Extracted D_{it} energy distribution for monolayer and bulk MoS_2/high-*k* interface with different interface qualities as shown in **Fig. 4-3**. Midgap states are clearly observed for monolayer MoS_2.

Fig. 4-4 shows extracted D_{it} from both *I-V* and *C-V* method for bulk and monolayer MoS_2 with different sample quality. D_{it} peaks in low-quality samples for both monolayer and bulk MoS_2 are attributed to sulfur vacancies. While, clear band-tail shape D_{it} close to CB is observed. The band-tail shape D_{it} increase by decreasing MoS_2 thickness with ~10^{13} $cm^{-2}eV^{-1}$ in monolayer and ~10^{12} $cm^{-2}eV^{-1}$ in bulk. Since the conduction and valence bands of MoS_2 are mainly composed of the energy splitting of the Mo *d* orbital [2,3], the Mo-S bond bending due to the strain caused by lattice mismatch at the MoS_2/high-*k* interface [4,5] and/or the surface roughness/potential fluctuation f of the SiO_2 surface is suggested to be the origin as shown in **Fig. 4-5**. Moreover, midgap states are clearly observed for monolayer MoS_2.

By increasing MoS_2 thickness, band-tail D_{it} should be reduced and close to the bulk case because bulk MoS_2 is robust to substrate surface roughness and strain effect. This has been clearly seen in *S.S.*-thickness relation, as shown in **Fig. 4-6 (c)**. *S.S.* is extracted for the I_{DS} range of 10^{-12}~10^{-10} A, which corresponds to mid-gap D_{it} range. A clear decrease in *S.S.* also indicates that traps in high-*k* is unlikely the main origin for extracted D_{it} since high-*k* quality is assumed to be the same in principle without MoS_2 thickness dependence.

In order to further decrease bond bending of Mo *d* orbits even in monolayer MoS_2, the heterostructure was designed by S. Toyoda in our lab [6]. Back-gate graphite/*h*-BN/monolayer MoS_2 heterostructure FET was fabricated and shows extremely small *S.S.* of ~ 75 mV/dec as shown in **Fig. 4-6 (a,b)**. This reduced *S.S.* is due to the suppressed bond bending of Mo *d* orbits.

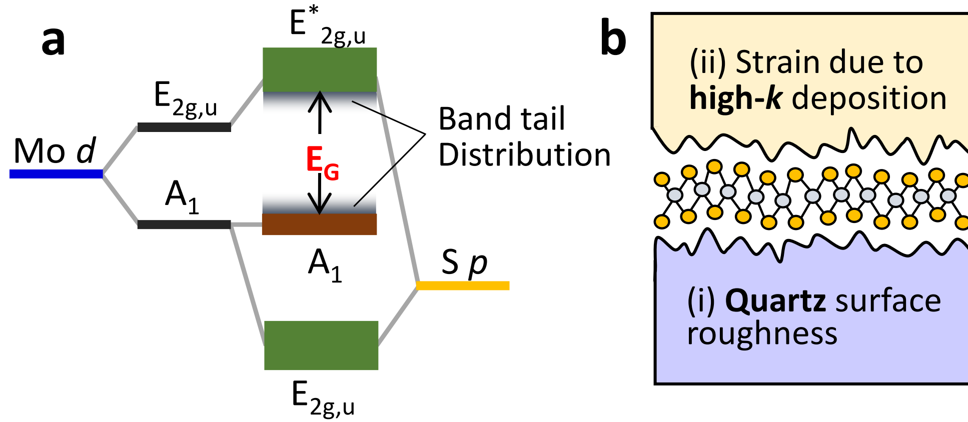

Fig. 4-5 (a) Ligand field theory to understand the origin for MoS_2 conduction band. **(b)** Two possible origins of D_{it} in MoS_2/high-*k* interface.

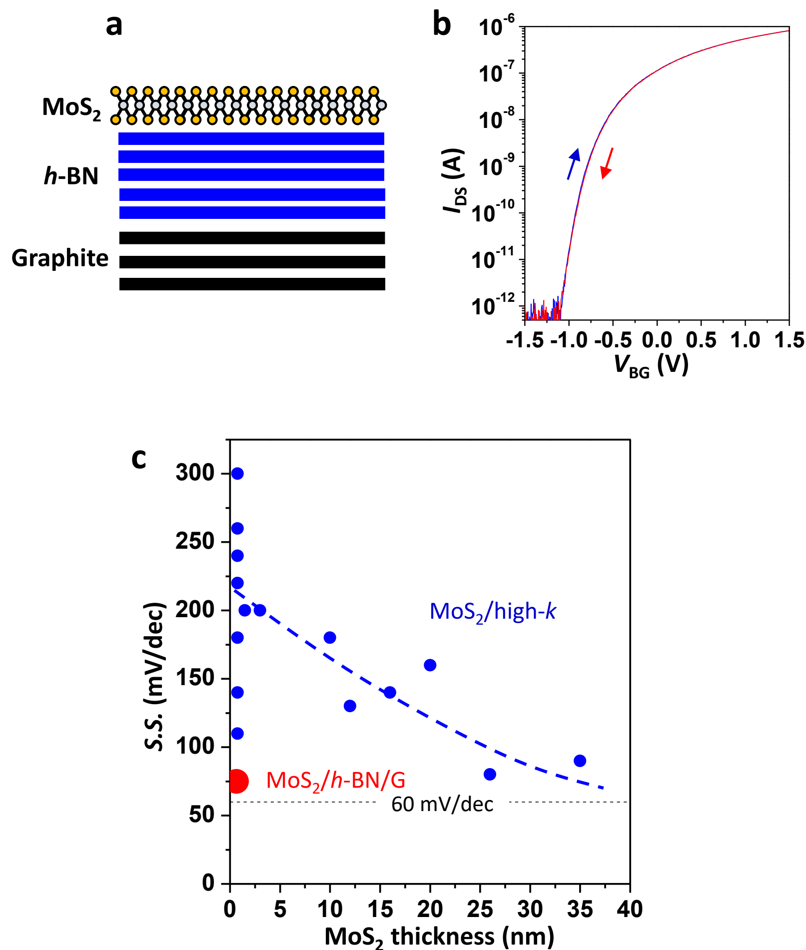

Fig. 4-6 (a) Schematic MoS_2/*h*-BN/graphite heterostructure by Toyoda [6]. **(b)** I_{DS}-V_{BG} curve of monolayer MoS_2/*h*-BN/graphite heterostructure FET [6]. **(c)** Extracted *S.S.* as a function of MoS_2 thickness for MoS_2/high-*k* and MoS_2/*h*-BN/graphite interfaces, respectively.

4.3 Support from Photoconductivity

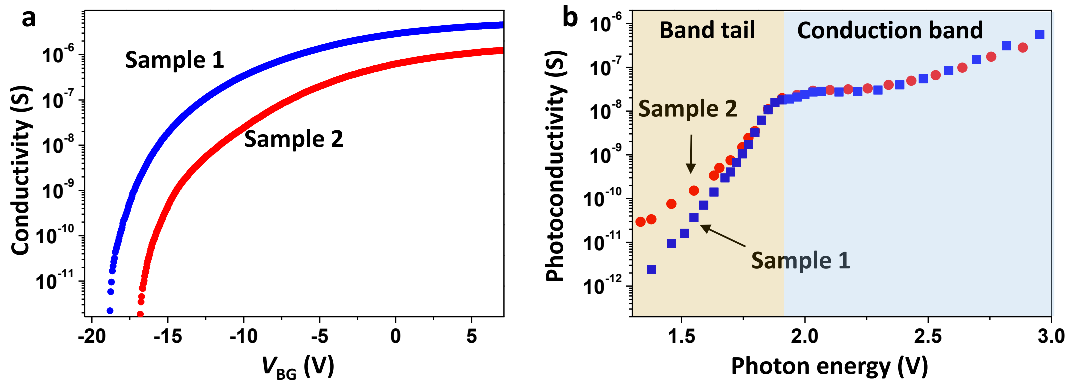

Fig. 4-7 (a) Measured transfer characteristics of two different monolayer MoS_2 samples. **(b)** Measured photoconductivity as a function of photon energy for these two different samples.

Photoconductivity measurement is used to directly measure band-tail shape D_{it}. Two back-gate monolayer MoS_2 FETs encapsulated by 5-nm Al_2O_3 dielectric layer are prepared for photoconductivity measurement. Sample 1 has sharper *S.S.* than that of sample 2, which indicates lower band-tail shape D_{it} as shown in **Fig. 4-7(a)**. **Fig. 4-7(b)** shows measured photoconductivity as a function of photon energy of these two samples. Band-gap of monolayer MoS_2 is confirmed to be~ 1.8 eV, which shows a small difference. While photoconductivity < 1.7 eV shows a large difference. Sample 2 has much higher photoconductivity than that of sample 1, which comes from large band-tail shape D_{it}. This is consistent with *S.S.* analysis.

4.4 Interpretation of metal-insulator transition by interface states

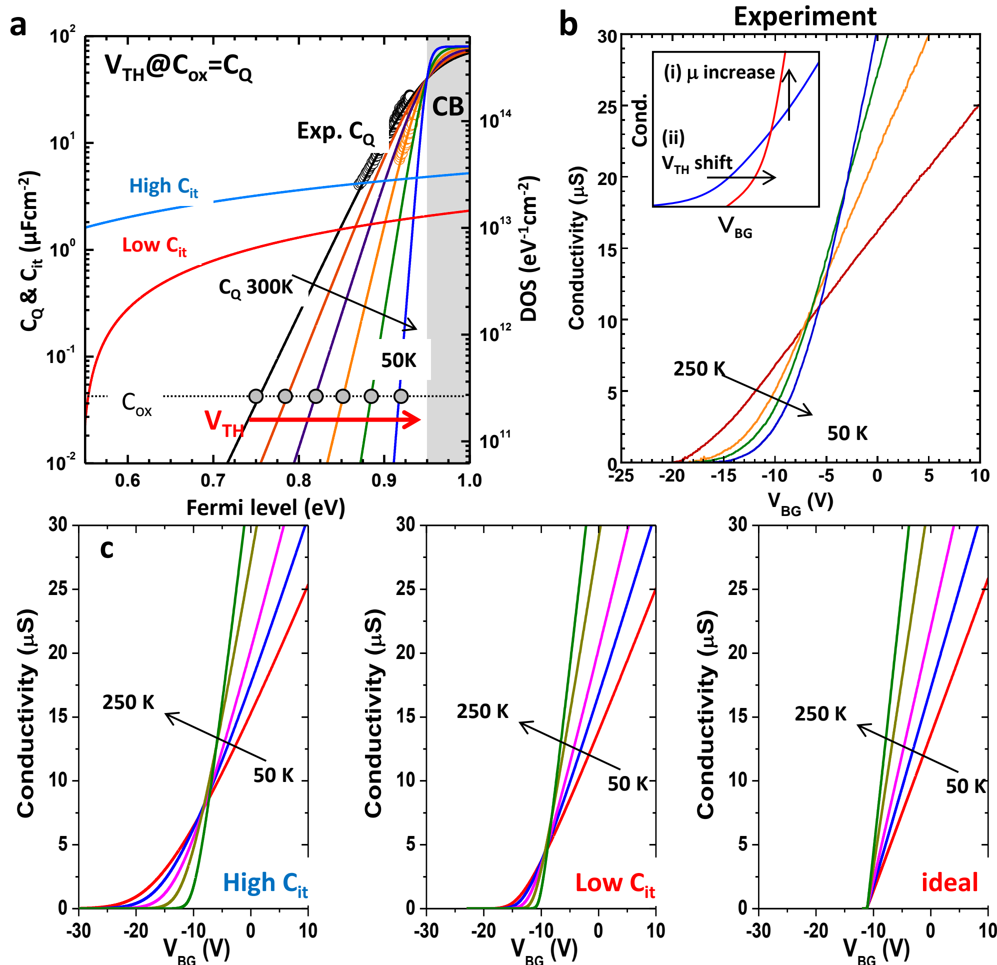

Fig. 4-8 (a) C_{it} and C_Q at different temperatures. High and low C_{it} lines are used for the simulation. **(b)** Experimental 4P conductivity at 50~250 K. **(c)** Simulated σ-V_{BG} curves with different C_{it}.

Cross-over point in temperature dependent *I-V* is often understood as "MIT" behavior [7-10]. However, the origin of MIT in 2D-FET is still unclear. This subchapter explains MIT in terms of C_Q temperature dependence and C_{it} as shown in **Fig. 4-8 (a)**. **Fig. 4-8 (b)** shows experimental conductivity-V_{BG} characteristics from four-probe back-gate device, which clearly shows MIT. Experimental σ-V_{BG} characteristics is simulated with three different C_{it} levels (high, low and no C_{it}) and plotted in **Fig. 4-8(c)**.

MIT can be observed intuitively by the combination of (i) the increase in the mobility and (ii) positive V_{TH} shift with decreasing the temperature. The mobility is assumed to increase with decreasing temperature due to suppression of phonon scattering [11,12]. Therefore, the dominant key factor for MIT is a positive V_{TH} shift with decreasing temperature. This occurs because E_F at V_{TH} approaches the conduction band edge at lower temperature since V_{TH} is defined by V_{BG} at $C_Q = C_{ox}$, which is shown in **Fig. 4-8 (a)**. Thus, a larger amount of C_{it} needs to be filled by electrons before reaching V_{TH} at lower temperature, resulting in the V_{TH} shift. By decreasing the C_{it} level, the crossover points of the MIT get close to V_{TH} and finally enter the subthreshold region for the case with no C_{it}, which is the ideal V_{TH} shift.

Recently, no MIT has been reported for an *h*-BN-encapsulated monolayer CVD-MoS_2 FET, suggesting a quite low C_{it} due to superior 2D/2D interface properties [13]. The present model indicates that C_{it}-induced positive V_{TH} shift is one of the main origins for "extrinsic" MIT. It should be noted that C_D has a much smaller temperature dependence than C_Q, which indicates that threshold voltage shift with temperature is only prominent at ultra-thin 2D materials.

4.5 Summary

In this chapter, D_{it} energy distribution has been successfully extracted by both *I-V* and *C-V* from monolayer to bulk MoS_2. The origin of D_{it} has been investigated. D_{it} peaks in low-quality samples for both monolayer and bulk MoS_2 are attributed to the sulfur vacancies. While, band-tail shape D_{it} close to CB is attributed to Mo-S bond bending due to the strain caused by the high-*k* deposition and/or the surface roughness of the SiO_2 surface. Finally, MIT behavior has been explained in terms of device physics by considering temperature dependence of C_Q and C_{it}.

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5 Nb-doped *p*-MoS_2/SiO_2 interfacial properties

We have studied natural *n*-type MoS_2 FET in the previous chapters. However, stable *p*-type FET is always needed in terms of traditional semiconductor technologies. Moreover, the interface states of MoS_2 at valance band side is still unclear. Therefore, in this chapter, *p*-MoS_2 will be investigated.

5.1 Crystal quality of *p*-MoS_2

P-MoS_2 crystal was bought from HQ graphene [1]. It was grown by chemical vapor transport (CVT) method [2,3]. Here, niobium (Nb) was introduced for submission of Mo atoms. **Fig. 5-1** shows schematic of Nb-doped MoS_2. It has been predicted by first principle calculation that Nb has one less electron than Mo, which is the most suitable substitutional acceptor [4]. **Fig. 5-2** shows the calculated *DOS* of Nb, Zr, and Y substitution, respectively. Nb-doped MoS_2 will show strong *p* behavior. Moreover, Nb induced defects states is at the valance band side, which is more delocalized than that in Zr, Y. As a result, Nb-doped MoS_2 should have higher hole mobility compared with Zr, Y-doped MoS_2.

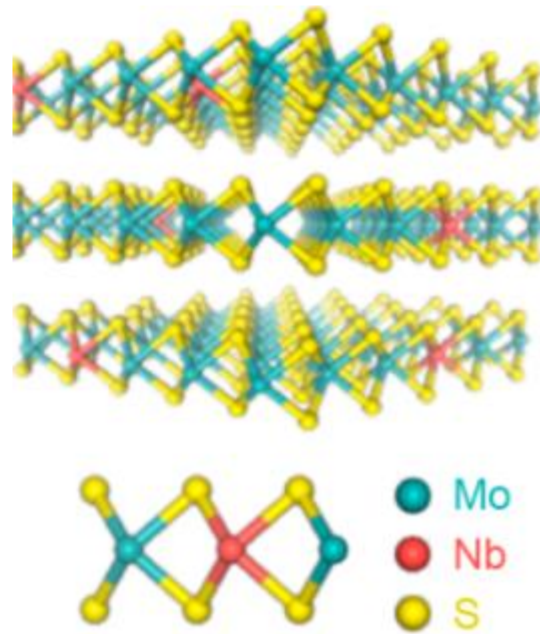

Fig. 5-1 Cross-sectional illustration of Nb-doped MoS_2. [2]

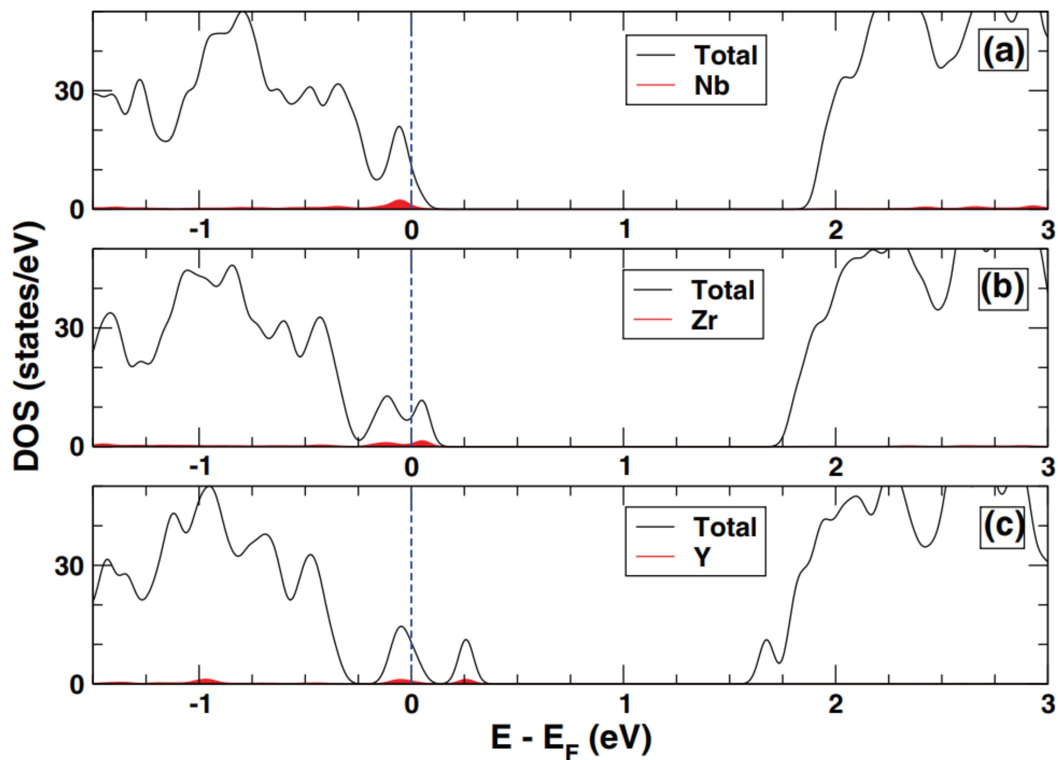

Fig. 5-2 Calculated *DOS* for monolayer MoS_2 in which one Mo atom is replaced by **(a)** Nb, **(b)** Zr and **(c)** Y. The blue dashed line shows the Fermi energy and the colored areas show *DOS* of dopants. [4]

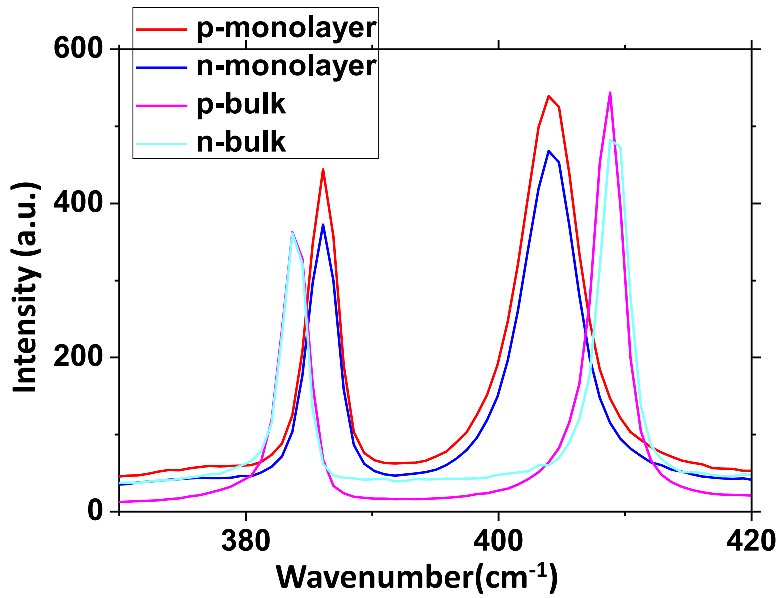

Fig. 5-3 Raman spectra of *p*-MoS_2 and *n*-MoS_2, respectively.

Fig. 5-3 shows measured Raman spectra of *p*-MoS_2 and *n*-MoS_2, respectively. There is no distinct difference between *p*- and *n*-MoS_2 from the monolayer to bulk, which indicates that Nb-doping does not affect lattice phonon much. However, PL spectra in **Fig. 5-4** shows a clear difference between monolayer *n*- and *p*-MoS_2. The lower energy peak in *p*-MoS_2 might be attributed to Nb induced defects states.

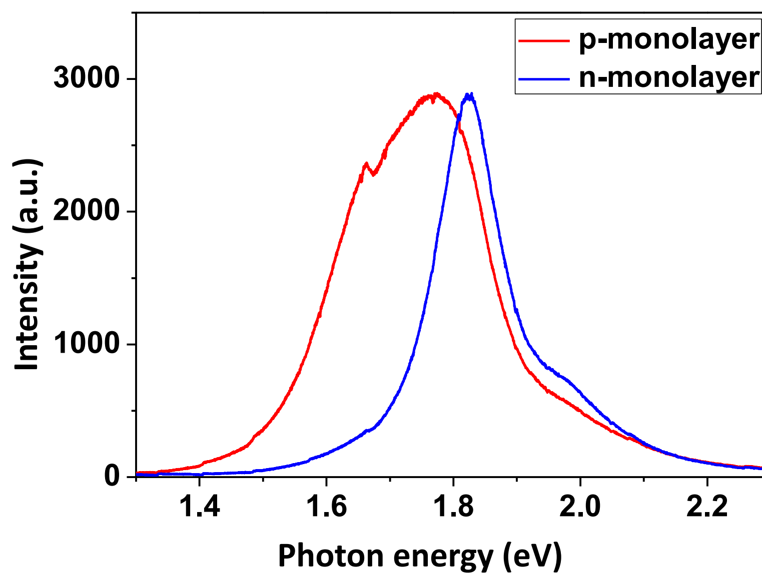

Fig. 5-4 PL spectra of monolayer *p*-MoS_2 and *n*-MoS_2, respectively.

5.2 *P*-MoS_2/SiO_2/Si FET characterization

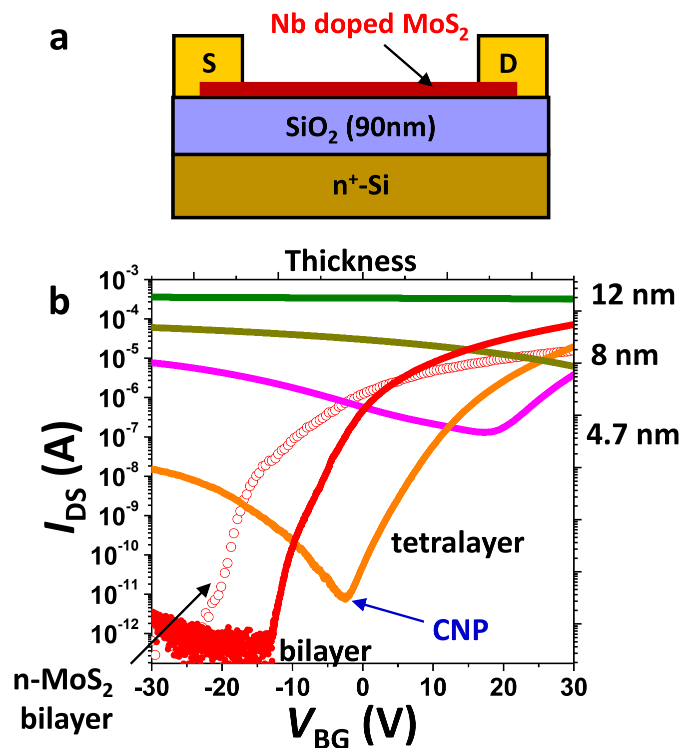

Fig. 5-5 **(a)** Schematic diagram of *p*-type MoS_2 back-gate device. **(b)** Transfer characteristics of *p*-type MoS_2 back-gate FET with different channel thickness. V_{DS} = 1 V. Red circle indicates bilayer *n*-type MoS_2 back-gate FET transfer characteristics.

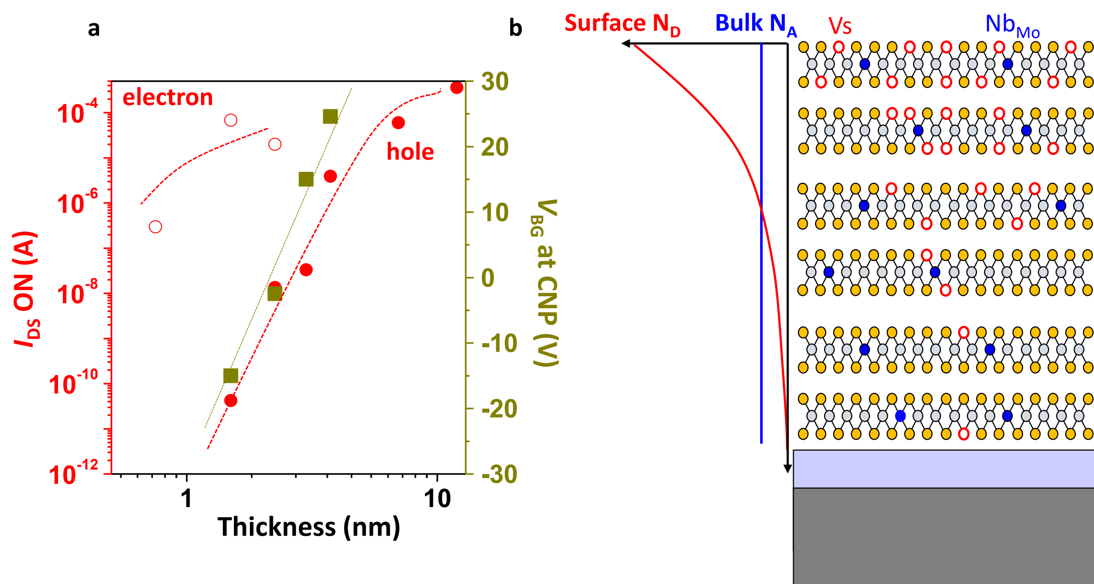

Fig. 5-6 **(a)** I_{DS} ON of hole, electron and V_{BG} at CNP as a function of *p*-MoS_2 thickness. **(b)** Schematic to show the origin of surface electron accumulation in *p*-type MoS_2.

Back-gate p-MoS_2/SiO_2/Si FET was then fabricated by following the same process as n-MoS_2. I_D-V_{BG} curves with different MoS_2 thickness are shown in **Fig. 5-5**. Unlike n-MoS_2, it shows unipolar p-type behavior when thick and ambipolar behavior when becomes thin. By decreasing thickness, off current is dramatically decreased, which indicates the value of W_{DM} is ~ 7 nm. It indicates that N_A is of ~ $2*10^{19}$ cm^{-3}.

There are two main interesting phenomena by decreasing thickness. One is the transition from p-type to n-type FET. Another one is the asymmetry between electron and hole transport. In order to focus on these two phenomena, on-current of both electron, hole (I_{DS} ON) and V_{BG} at charge neutral point are shown as a function of p-MoS_2 thickness (**Fig. 5-6**).

As for the transition from p-type to n-type FET, it can be understood as a surface electron accumulation effect. Charge neutral point (CNP) is defined as the point to change from n- to p-behavior at ambipolar behavior. Experimentally, CNP is always shifted at V_{BG} scale ($V_{BG\text{-}CNP}$) whose doping carrier density can be shown as $V_{BG\text{-}NP}*C_{ox}$. Doping carrier density at CNP is determined by both surface donor ($N_{D\text{-}2D}$) and bulk acceptor (N_A*t_{MoS2}). It is found that $V_{BG\text{-}NP}$ at CNP is almost linear to the thickness as shown in **Fig. 5-6**. Thus, it can be shown as follows.

$$V_{BG-CNP}C_{ox} = -N_{D-2D} + N_A t_{mos2} \tag{5-1}$$

Fitted $N_{D\text{-}2D} = 8.5*10^{12}$ cm^{-2} and $N_A = 2.7*10^{19}$ cm^{-3}. Estimated N_A here is close to N_A from W_{Dm}, which confirms the validity of the fitting. The simple fitting gives us several important information. N_A ~ $2.7*10^{19}$ cm^{-3} is an extremely high doping level even in conventional semiconductor materials. However, if we consider the monolayer case, N_A is normalized by monolayer MoS_2 thickness ($N_{A\text{-}2D}$) and $N_{A\text{-}2D}$ is only ~ $1.8*10^{12}$ cm^{-2}. This doping concentration is not enough to achieve p-type transport in nanoscale thickness device compared with $N_{D\text{-}2D}$. As a result, it is the surface doping effect that dominates the transport type at the atomically thin channel. This explains that although bulk transport is totally different between n- and p-MoS_2, it shows a slight difference in the bilayer case as shown in **Fig. 5-5**. Bilayer n-MoS_2 I_D-V_{BG} curve just shifts negatively with ~ 8 V compared with curve from bilayer p-MoS_2. This V_{BG} shift

is also consistent with estimated V_{BG} shift based on bulk N_A and N_D difference between p-MoS_2 and n-MoS_2 of ~ 12 V.

The dominant surface electron doping effect mainly comes from sulfur vacancies formation at the surface, which has been confirmed in chemical vapor transport (CVT) MoS_2 [5]. Moreover, the observed surface sulfur vacancy density by STEM is ~ 10^{13} cm^{-2}, which is close to the extracted value of $N_{D\text{-}2D}$. Based on the above analysis, the schematic to show surface electron accumulation is shown in **Fig. 5-6 (b)**.

Another interesting point is the asymmetry between electron and hole transport. Compared to electron transport, hole transport degrade severely with decreasing thickness. In order to further investigate this phenomenon, the temperature dependent I_{DS}-V_{BG} curve is shown in **Fig. 5-7**. Hole side shows larger temperature dependence compared with electron side. I also checked I_{DS}-V_{DS} curves since the contact effect could also result in a similar behavior. I_{DS}-V_{DS} curves in **Fig. 5-8** at both electron and hole on-region show almost linear behavior. In SB-FET, when I_{DS}-V_{DS} shows linear behavior, it means no energy barrier. As a result, I_{DS}-V_{BG} curve should show negligible temperature dependence at both electron and hole on-region. However, this is not the case in **Fig. 5-7**, which means that the metal/MoS_2 contact is not the main origin for the observed asymmetry between electron and hole transport. While in ACCU-FET, the linear of I_{DS}-V_{DS} does not relate to the energy barrier between CB/VB and Fermi level. Therefore, this linear I_{DS}-V_{DS} and large temperature dependent I_{DS}-V_{BG} curves can be explained by ACCU-FET. It is reasonable to conclude that hole transport in p-MoS_2 is worse than electron transport.

The origin of the degraded hole transport is the shallow defects states at VB side as shown in **Fig. 5-9**. Although both V_s or Nb_{Mo} could introduce defects states at VB side, the density of V_s (~ 10^{13} cm^{-2}) is much larger than that of Nb_{Mo} (~ $1.8*10^{12}$) in monolayer MoS_2, which indicates that sulfur vacancy is the dominant origin for the degraded hole transport.

Defects-states related transport is more easily observed at VB side compared with CB side. It has been found that in mechanically exfoliated monolayer MoS_2 ionic-liquid gated FET, defects-states related transport is observed at valance band side [7] as shown

in **Fig. 5-10 (a)**. We also observed defects-states related transport at valance band side in 4.7 nm-thick back-gate MoS_2 FET as shown in **Fig. 5-10 (b),** which again indicates that hole transport is worse compared to electron transport.

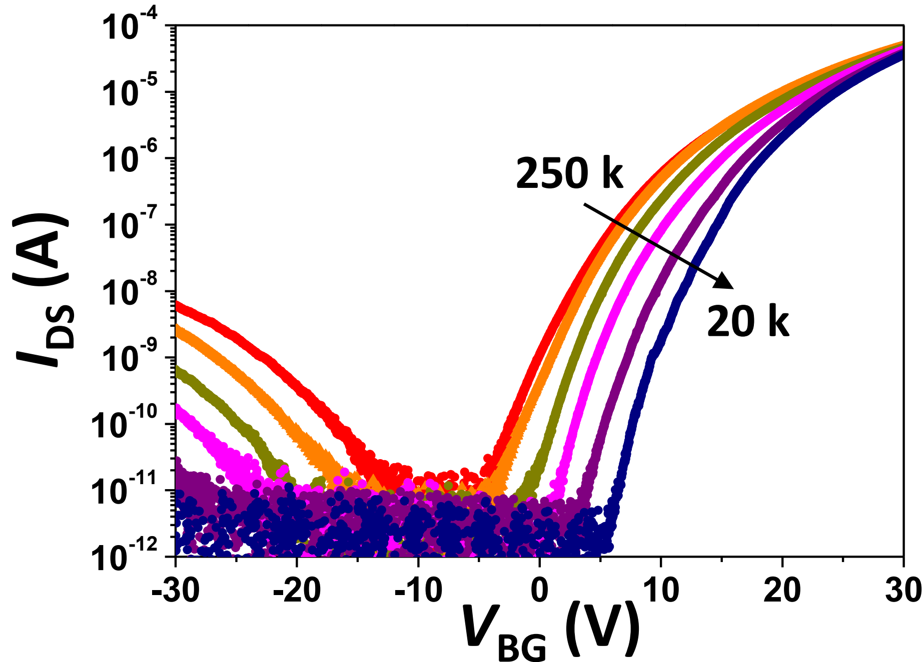

Fig. 5-7 Transfer characteristics of back-gate tetralayer MoS_2 FET. Temperature steps are 250, 200, 150, 100, 50, 20 K. V_{DS} = 1 V.

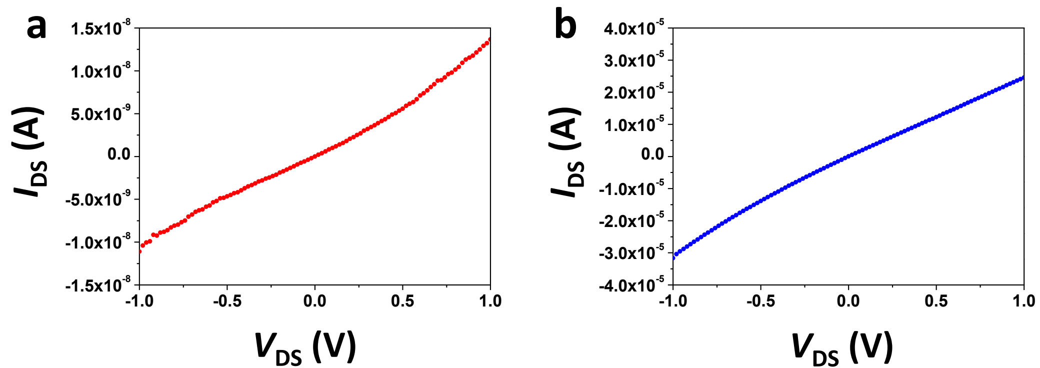

Fig. 5-8 I_{DS}-V_{DS} curves at (a) V_{BG} = -30 V and (b)V_{BG} = 30 V, respectively.

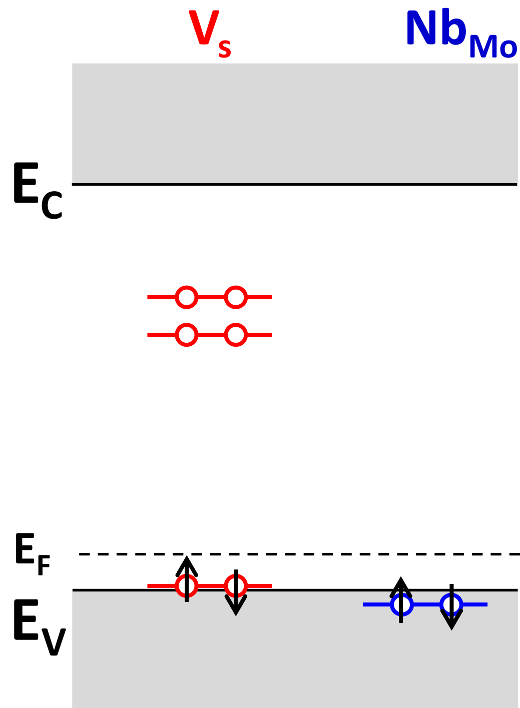

Fig. 5-9 Schematic to show defects states of V_s and Nb_{Mo}.

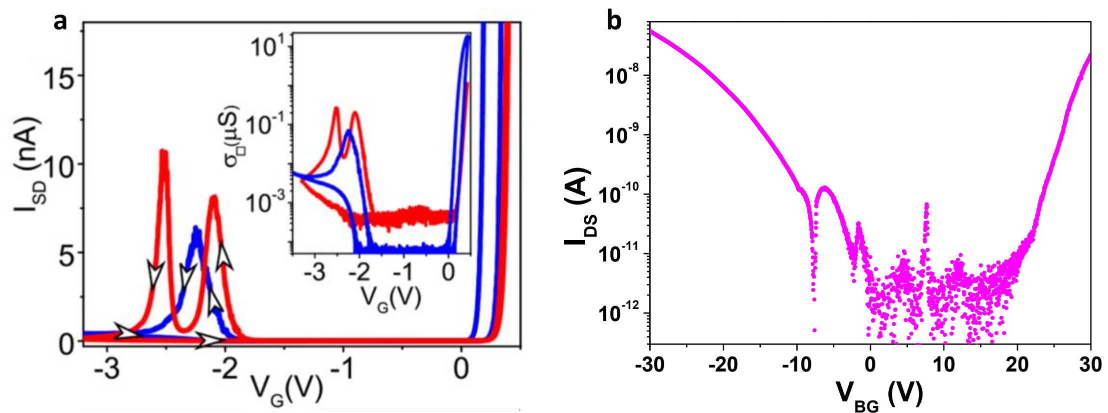

Fig. 5-10 (a) Transfer characteristics of ionic-liquid gated FET based on monolayer mechanical exfoliated MoS_2 [7], **(b)** back-gate 4.7 nm-thick back-gate MoS_2 FET at 50 K. V_{DS} = 1 V.

5.3 P-MoS_2/h-BN/graphite FET characterization

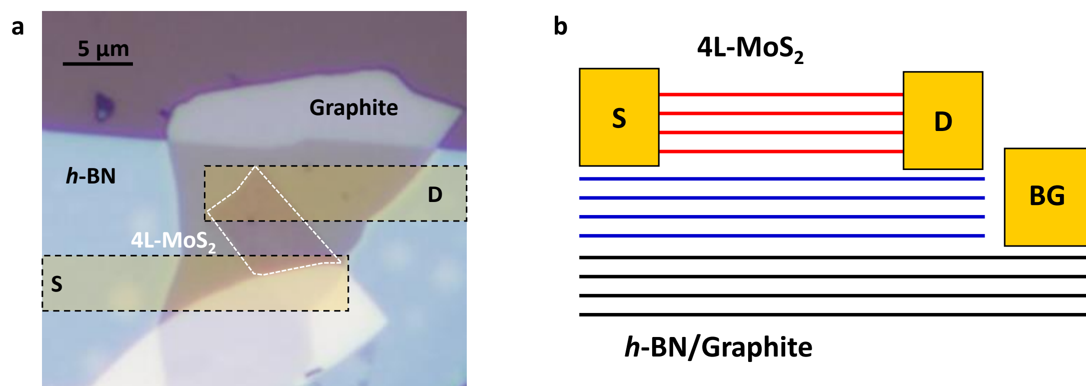

Fig. 5-11 (a) Optical image and **(b)** schematic of the p-MoS_2/h-BN/graphite hetero-FET with atomically flat surface.

The main origin of D_{it} at CB side is the Mo-S bond bending due to the strain caused by the high-k deposition and/or the surface roughness of the SiO_2 surface, which has been discussed in chapter 4. By fabricating p-MoS_2/h-BN/graphite hetero-FET, the atomically flat substrate and no strain from high-k deposition are expected. Thus the interfacial properties should be improved. This scenario has been confirmed in natural n-type MoS_2 as shown in **Fig. 4-6** [8]. I also followed this device structure to investigate the origin of interface degradation at VB side. The experimental details are shown as follows. First, h-BN and p-MoS_2 flakes were mechanically exfoliated on a polydimethylsiloxane (PDMS) sheet separately. These flakes were then transferred on graphite bulk flakes on the SiO_2/Si substrate by using the alignment system. The Ni/Au electrodes were then formed using the electron beam lithography. The fabricated p-MoS_2/h-BN/graphite hetero-FET image is shown in **Fig. 5-11**.

The I_{DS}-V_{BG} curve of tetralayer p-MoS_2/h-BN/graphite hetero-FET is shown in **Fig. 5-12**. *S.S.* is of ~ 160 mV/dec for electron and 590 mV/dec for hole. It indicates that interfacial properties at CB side are improved due to the atomically flat surface of h-BN/graphite and no high-k deposition. While interfacial properties at VB side is still poor. The I_{DS}-V_{BG} curve is then fitted by the method discussed in chapter 4. The full energy range D_{it} is summarized in **Fig. 5-13** by including D_{it} extracted from **Fig. 4-4**

and D_{it} from monolayer n-MoS_2/h-BN/graphite hetero-FET [8]. D_{it} at CB side of monolayer MoS_2 is reduced from ~10^{12} $cm^{-2}eV^{-1}$ to ~10^{11} $cm^{-2}eV^{-1}$ by using h-BN/graphite heterostructure. However, D_{it} at VB side of tetralayer MoS_2 still stays high of ~10^{13} $cm^{-2}eV^{-1}$. It indicates that the high D_{it} at VB side is not due to the surface flatness but the sulfur vacancies in MoS_2 itself. The reason why sulfur vacancies degrade more seriously at VB side is that sulfur vacancy induced states at VB side is shallow (**Fig. 5-9**).These shallow defects states can easily communicate with holes, which works as strong trap sites. In a word, it is the defects in the p-MoS_2 that degrades the interfacial properties at VB side, which cannot be improved by just designing dielectric layer environment.

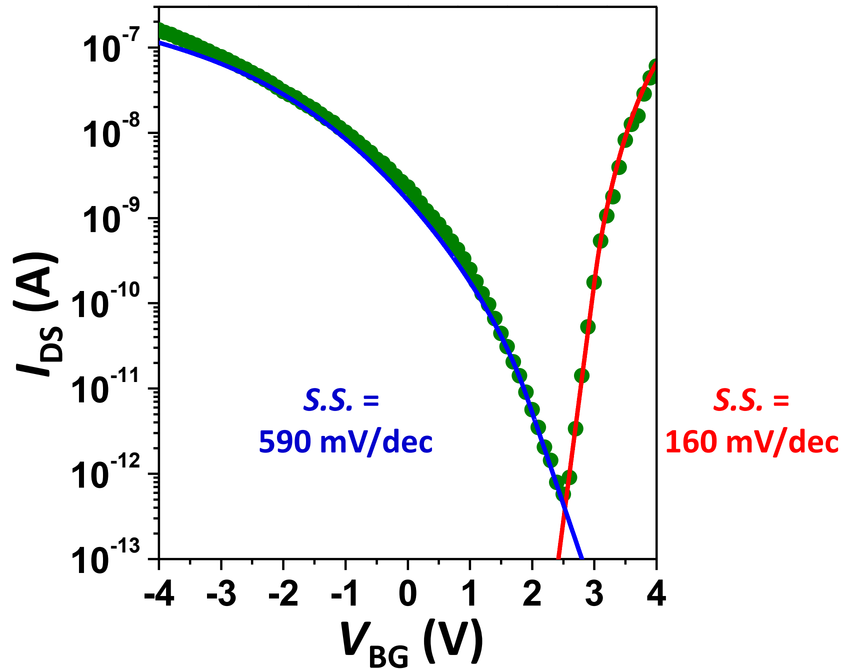

Fig. 5-12 Transfer characteristics of tetralayer p-MoS_2/h-BN/graphite hetero-FET. Temperature is 300 K. V_{DS} = 1 V. Blue and red lines are simulations as discussed in chapter 4.

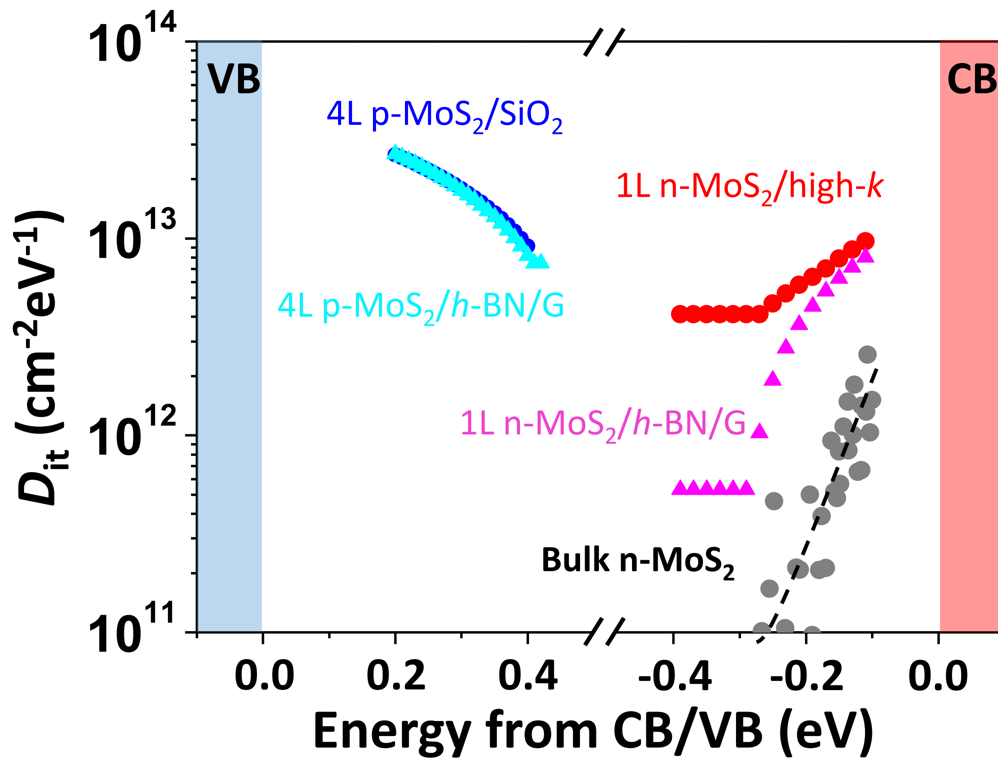

Fig. 5-13 Extracted D_{it} energy distribution for both CB and VB side of MoS_2. D_{it} of VB side was studied from *p*-MoS_2 while D_{it} of CB side was studied from *n*-MoS_2.

5.4 Summary

In this chapter, Nb-doped *p*-type MoS_2 has been investigated. Raman and PL confirms the quality of *p*-type MoS_2 crystal. Several interesting phenomena have been found. One is the surface electron accumulation in *p*-type MoS_2, which prevents the fabrication of ultra-thin *p*-FET even from *p*-MoS_2 crystals. Another one is the asymmetry between electron and hole transport. Both of them are due to surface sulfur vacancies formation in MoS_2. Full range D_{it} - energy distribution is obtained based on *n*-MoS_2 and *p*-MoS_2.

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6 Other TMDC interfacial properties

6.1 WSe_2/SiO_2 interfacial properties

In order to further extend the above analysis to most 2D materials and summarize universal rule, I also study WSe_2 in this chapter. WSe_2 crystal was bought from HQ graphene. Back-gate WSe_2/SiO_2 FET was then fabricated by following the same process as MoS_2. I_D-V_{BG} curves with different WSe_2 thickness are shown in **Fig. 6-1**. Unlike p-MoS_2, it shows ambipolar behavior for the whole thickness range. No clear surface accumulation/depletion effect is observed. By decreasing thickness from 20 nm to 10 nm, off current is dramatically decreased, which indicates W_{DM} is close to this range. Moreover, *S.S.* degradation by decreasing thickness is more severe in WSe_2 than that in MoS_2. For example, *S.S.* of a 2 nm-thick sample is ~ 6 V/dec, which corresponds to mid-gap D_{it} of ~$2*10^{13}$ $cm^{-2}eV^{-1}$. While mid-gap D_{it} of 2nm-thick n-MoS_2 is ~ $3*10^{12}$ $cm^{-2}eV^{-1}$, which is one order smaller than WSe_2.

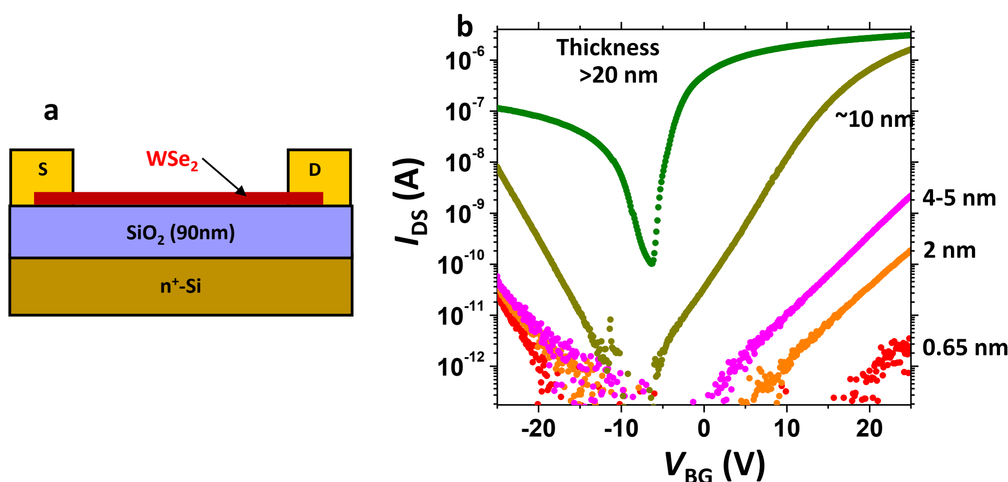

Fig. 6-1 (a) Schematic diagram of WSe_2 back-gate device. **(b)** Transfer characteristics of back-gate WSe_2 FET with different channel thickness. V_{DS} = 0.1 V.

6.2 Photoconductivity of WSe_2

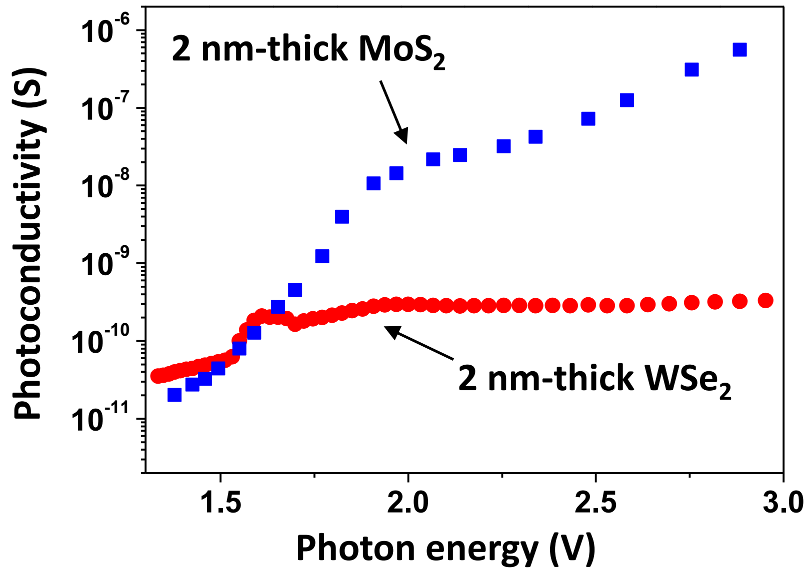

Fig. 6-2 Photoconductivity as a function of photon energy for 2 nm-thick MoS_2 and 2 nm-thick WSe_2 sample, respectively.

Photoconductivity measurement is again studied to show how the different 2D materials with different interfacial properties could affect photon behavior. **Fig. 6-2** shows photoconductivity for the 2 nm-thick MoS_2 and 2 nm-thick WSe_2 samples, respectively. Photoconductivity in WSe_2 is more than 3 orders smaller than that in MoS_2. Moreover, the slow photon energy dependence at energy range 1.3 ~ 1.6 eV indicates much higher D_{it} in WSe_2 than that in MoS_2. In order to explain why photoconductivity in WSe_2 is more than 3 orders smaller than that in MoS_2, photoconductivity equation is shown below [1].

$$\Delta\sigma = e\mu_n \Delta n + e\mu_p \Delta p \qquad (6\text{-}1)$$

Photoconductivity is determined by mobility and photon-induced electron-hole pair density. Although mobility in thin WSe_2 is smaller than that in MoS_2, it could not be the main origin. Thus, the electron-hole pair in WSe_2 should be also less than that in MoS_2. This is understandable because mid-gap states extracted in 2 nm-thick WSe_2 is

one order of magnitude larger than that in MoS_2. The high-level mid-gap states in WSe_2 will introduce a recombination path for generated electron-hole pairs [2]. Thus, generated electron-hole pairs will quickly recombine, which results in low electron-hole density. This has been confirmed by the dynamics of photoconductivity as shown in **Fig. 6-4**. Time constant in WSe_2 is < 1 s while > 400 s in MoS_2. This indicates that defects engineering is important for optics in 2D-FET.

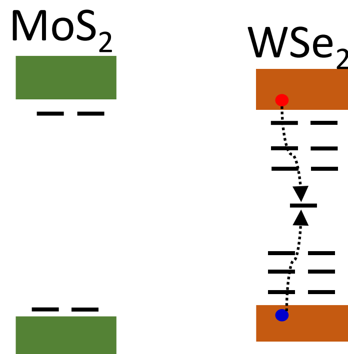

Fig. 6-3 Schematic to show how mid-gap state introduces the electron-hole pair recombination path in WSe_2.

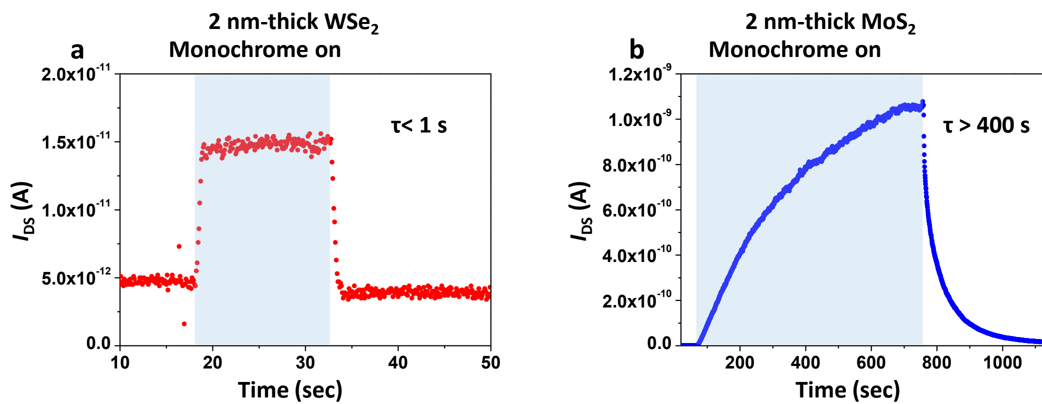

Fig. 6-4 I_{DS}-time characteristics to show electron-hole dynamics of (**a**)2 nm-thick WSe_2, (**b**)2 nm-thick MoS_2, respectively.

6.3 Thickness scaling rule of 2D-FET

Having demonstrated the transport and crystal qualities of MoS_2, p-MoS_2 and WSe_2, it is time now to summarize other 2D materials. The bulk doping concentration can be estimated in terms of W_{Dm} by I-V thickness dependence (chapter 2). First, MoS_2 is demonstrated as an example. The transport mechanism is divided into three regions as a function of t_{MoS2}. When $t_{MoS2} > W_{Dm}$, the channel is only partially controlled by the gate and shows band transport. The existence of residual conductance is the sign of this region. When $2L_D < t_{MoS2} < W_{Dm}$, the channel is fully controlled with optimized mobility because of screening of interfacial Coulomb scattering. Band transport also dominates in this region. When $t_{MoS2} < 2L_D$, band transport is still dominant at room temperature, but it often suffers from mobility degradation due to prominent interfacial Coulomb scattering. In the subthreshold region at low temperature, the localized states induced transport such as hopping will become dominant [3-5]. It should be noted that both W_{Dm} and $2L_D$ are independent of C_{ox}, which enables us to propose the thickness scaling rule of transport properties for various 2D materials as a function of N_D (N_A). The summarized 2D materials here have a band-gap of 1~2 eV and a similar dielectric constant. As mentioned before, transport properties for the present top gate MoS_2 FET are consistent with that from global back gate MoS_2 devices. Therefore, almost all of the data on W_{Dm} and L_D in **Fig. 6-5** are obtained from global back-gate devices in the previous literature. At high N_D (N_A) region (>10^{19} cm^{-3}), W_{Dm} will decrease substantially, resulting in a small thickness window for "fully controlled band transport", that is, fully depleted. In fact, full control of channel will be lost when the 2D thickness becomes greater than W_{Dm}. Moreover, it will be more degraded by considering a heavy doping effect such as band gap narrowing [6]. This explains why well-controlled FETs with high I_{ON}/I_{OFF} are difficult to achieve in recent heavily doped 2D materials such as PtS_2, $PtSe_2$, SnS, and SnSe. Meanwhile, $2L_D$ is scaled down to just several atomic layers of thickness. This strong electrostatic confinement effect combined with increased N_D (N_A) will introduce strong scattering. Band transport is difficult to achieve in atomically thin flake of these heavily doped 2D materials, and the Anderson localization phenomenon

is suggested to be observed [7]. Moreover, in terms of 2D/metal contact, heavily doped 2D materials generally show low contact resistance because of the thin Schottky barrier width.

In silicon, the bulk doping concentration can be controlled by the technology such as ion implantation. However, in 2D materials, the bulk doping concentration comes from the most thermally stable defects, which indicates the crystal qualities of 2D materials itself. For example, the crystal quality of MoS_2 or WS_2 is much better than that of SnS. From the above analysis, well controlled doping approaches on 2D crystals are in great demand for improving the performance of 2D ACCU-FET.

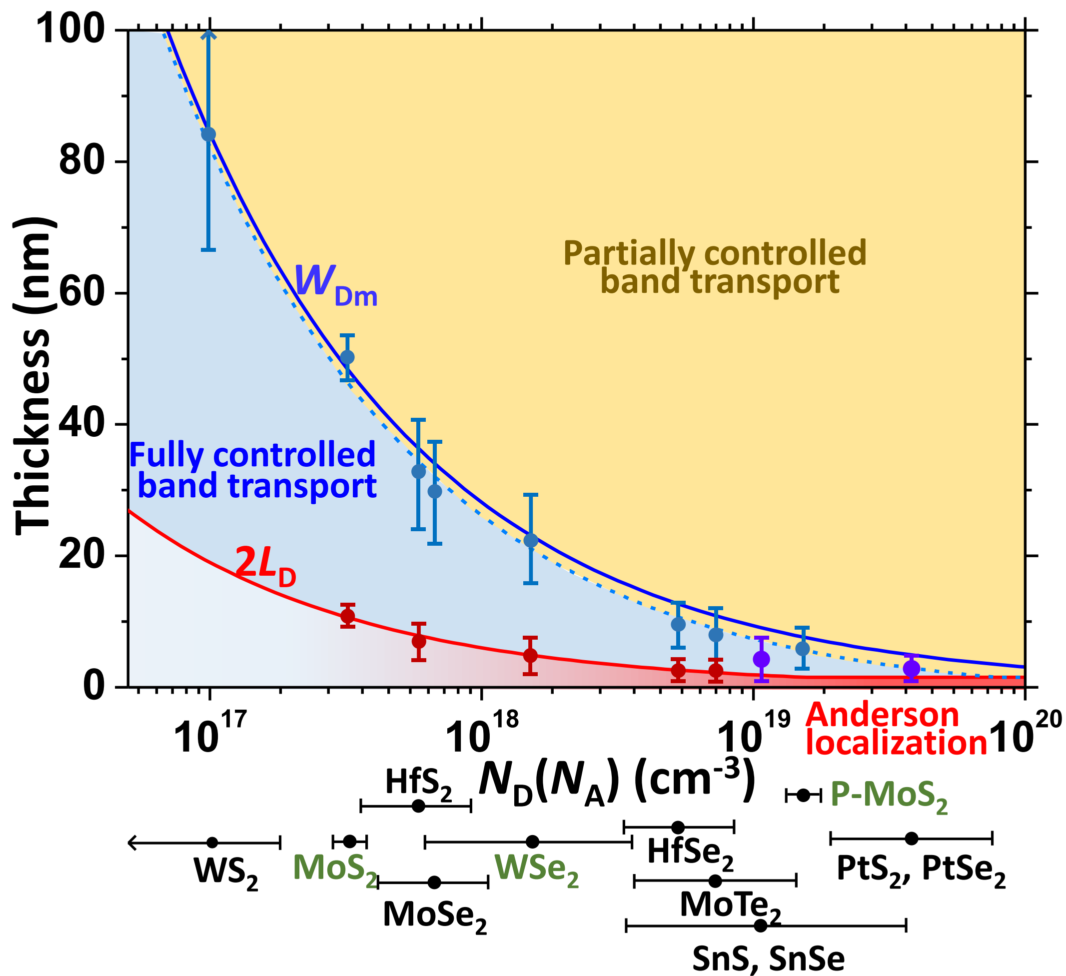

Fig. 6-5 Thickness scaling rule of a 2D ACCU-FET. Baselines of W_{Dm} and $2L_D$ are calculated from the parameters of bulk MoS_2. Band-gap = 1.29 eV and ε = 6.3. Studied materials in this work are marked in green. Parameters of other 2D materials are extracted from previous reports [8-19].

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7 Summary and outlook

7.1 Summary

TMDC, one type of two-dimensional materials, has attracted much attention in research on ultimately scaled 2D-FET due to its large tunable band-gap and ultra-thin body thickness. To further investigate the underlying device physics and improving the device performance, it is required to fully understand the operation mechanism of 2D-FET by *I-V* and *C-V*.

Firstly, the key issues in the device fabrication process of high-quality MoS_2 dual-gate FET were demonstrated. Buffer layer deposition process was optimized by depositing Y metal at an Ar atmosphere of 10^{-1} Pa partial pressure in order to prevent defects formation in MoS_2. The operation mechanism of 2D-FET was discussed. *I-V* temperature dependence, *I-V* thickness dependence, and *C-V* cannot be fully explained by only SB-FET. Thus, ACCU-FET mode was proposed and developed to explain the observed behavior, which is more applicable and universal in 2D-FET.

Then, *C-V* characterization of MoS_2 FET structure was systematically studied. Parasitic capacitance was totally removed by using an insulating quartz substrate. Resistance effect was carefully checked, which is one of the main origins for observed frequency dispersion in the fully depleted region of MoS_2 FET. Quantum-mechanical effect was investigated from the monolayer to bulk MoS_2, which is important in terms of device physics and application prospect.

Based on the achievements in *I-V* and *C-V* characterization, full range D_{it} - energy distribution was successfully extracted. The origin of D_{it} was investigated. For CB side, D_{it} peaks in low-quality samples were attributed to the sulfur vacancies. While band-tail shape D_{it} close to CB was attributed to Mo-S bond bending due to the strain caused by the high-*k* deposition and/or the surface roughness of the SiO_2 surface. For VB side, high D_{it} level was attributed to sulfur vacancies.

Finally, crystal qualities of most of 2D materials were evaluated based on the bulk doping concentration. Thickness scaling rule for most of 2D-FET was proposed.

From the above summary, I would like to point out the specific new points that this study contributes to the research field of two-dimensional materials:

1) The interpretation of *C-V* characterization in MoS_2-FET. Widely observed frequency dispersion was due to the channel resistance effect. Quantum-mechanical effect was studied from the monolayer to thick MoS_2. Depletion width maximum in two-dimensional materials was precisely measured.
2) The development of ACCU-FET in two-dimensional materials. The D_{it} – energy extraction method from *I-V* characterization was built. Bulk doping concentration extraction method from *I-V* characterization was built. Most of two-dimensional materials crystal qualities were evaluated in terms of bulk doping concentration.
3) The systematical study of MoS_2/high-*k* interface. Full range D_{it} - energy distribution was extracted. For CB side, the origin for band-tail shape D_{it} was found to be Mo-S bond bending due to the strain caused by the high-*k* deposition and/or the surface roughness of the SiO_2 surface. For VB side, high D_{it} level was attributed to sulfur vacancies.

7.2 Outlook

This study solved commonly encountered problems in MoS_2-FET *C*-*V* measurement and built the platform of *C*-*V* measurement for most 2D-FET, which finally leads to the development of understanding in *I*-*V* and MoS_2/high-*k* interface. In this study, we mainly focused on MoS_2, which is the most conventional materials in TMDC. By applying *C*-*V* measurement to other 2D-FET with new channels or new structure, we can achieve more interesting physics. For example, 1T-TaS_2 usually shows the phase transition by changing temperatures. The accurate measurement of capacitance to trace this transition would give much physics behind, which is invisible by just *I*-*V*.

As for MoS_2/high-*k* interface, it is still far from perfect due to band tail D_{it}, which is attributed to Mo-S bond bending caused by substrate roughness or strain from high-*k*. In order to suppress surface roughness, atomically flat substrate and high-*k* deposition with reduced strain are always needed. For example, the interface dedicated device fabrication process is highly demanded to realize the MoS_2 FET without the aid of *h*-BN.

PUBLICATIONS

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(7) **Fang, N.** & Nagashio, K. Quantum-mechanical effects on accumulation capacitance of two-dimensional field-effect-transistor. (In preparation)

(8) **Fang, N.**, Toyoda, S., Taniguchi T., Watanabe K. & Nagashio, K. Systematical study of interfacial properties of n-type and p-type MoS_2. (In preparation)

AWARDS

(1) Young researcher award, 47th International Conference on SSDM, 2015.

(2) Young scientist presentation award, 43th Spring Meeting of JSAP, 2017.

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