博士論文(要約)

Study on optical modulator and switch based on the III-V/Si hybrid MOS optical phase shifter

(III-V/Si ハイブリッド MOS 光位相シフタに基づく光変調器および光スイッチに関する研究)

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Abstract

With the continuous huge research effort and investment by academic institutes and industry respectively, Si photonics has rapidly grown into a mature and established platform promising large bandwidth, low cost and high-level integration with the traditional electronic devices, by leveraging the complementary metal-oxide-semiconductor (CMOS) manufacturing facilities. In optical communication and networking systems, optical modulator and switch are two critical building blocks for both of which an optical phase shifter is an indispensable component. On Si photonics platform, most optical phase shifters are either based on the thermo-optic effect or carrier dispersion effect, which suffer from large power consumption, low modulation efficiency, or severe absorption loss. To address these challenges, a III-V/Si hybrid MOS optical phase shifter is proposed and demonstrated. The III-V/Si hybrid MOS optical phase shifter was formed by bonding a n-type III-V layer on a p-type Si waveguide using a high-*k* dielectric layer as the bonding interface. With a positive gate voltage applied between the Si and III-V layer, holes and electrons are accumulated on the MOS interface, modifying the local refractive index and changing the phase of the optical mode. Owning to the small effective mass of electrons in the III-V material, the free-carrier plasma dispersion effect is enhanced leading to higher modulation efficiency. Furthermore, the high electron mobility enables smaller resistance resulting into larger modulation bandwidth. The III-V/Si hybrid MOS optical modulator has demonstrated a low $V_{\pi}L$ of 0.047 Vcm and low absorption loss of 0.23 dB at π phase shift. Compared with its Si counterparts, the modulation efficiency was increased by 5 times while the absorption loss was reduced by 10 times.

Although the III-V/Si hybrid MOS optical phase shifter has exhibited excellent performance, there is still plenty of room for improvement. In this dissertation, we have improved the III-V/Si hybrid MOS optical phase shifter in terms of modulation efficiency and modulation bandwidth, integrated it on a Si 2×2 optical switch and a Si racetrack resonator, and proposed a new modulation scheme to break the inherent trade-off relationship between modulation efficiency and modulation bandwidth.

Firstly, the performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter was numerically studied systematically. The influence of doping concentration and layer thickness of III-V and Si layers, and equivalent oxide thickness (EOT) of the oxide layer inserted between III-V and Si layers was analyzed. It was found that the modulation efficiency was able to be increased by improving the overlap between optical mode and accumulated free carriers on the MOS interfaces. EOT scaling is effective to increase the modulation efficiency. However, when Al_2O_3 is used as the bonding interface, the EOT is difficult to be scaled below 5 nm due to the generation of nano-scale voids in the bonding interface. By employing HfO_2/Al_2O_3 stack for wafer bonding, an EOT as small as 3.5 nm was successfully achieved, which is expected to produce a low $V_{\pi}L$ of 0.035 Vcm. The modulation bandwidth was increased by removing the parasitic capacitance. After introducing an isolation trench on the one side of the Si slab waveguide, 86% parasitic capacitance was successfully eliminated. To fully eliminate all the parasitic effect, a SiO_2 filling process followed by a chemical mechanical planarization (CMP) process was proposed. Preliminary wafer bonding test was conducted and verified the feasibility of the proposed methods.

In addition, a 2×2 Si Mach-Zehnder interferometer (MZI) optical switch based on III-V/Si hybrid MOS optical phase shifter was demonstrated. Owing to the negligible gate

leakage current in the hybrid MOS capacitor, the power consumption required for switching is 0.18 nW, approximately one million times smaller than that of a Si thermo-optic phase shifter. A switching time of less than 20 ns was also achieved, which is 1000 times faster than a Si thermo-optic phase shifter. A 4×4 optical switch is now under development, which is a prototype for large scale optical switch fabrics or photonics circuit used for deep learning applications. Next, the III-V/Si hybrid MOS optical phase shifter was successfully integrated on a Si racetrack resonator. The Si racetrack resonator was well designed to achieve the critical coupling condition that lowers the driving voltage swing or capacitance for optical intensity modulation. Compared with a MZI optical modulator with the same phase shifter, the demonstrated racetrack resonator only need halved driving voltage and one quarter energy for 10-dB optical modulation.

For all the MOS-type optical modulators based on carrier accumulation, the trade-off relationship between modulation efficiency and modulation bandwidth is a challenging issue. To break this limitation, an efficient optical modulator by reverse-biased III-V/Si hybrid MOS capacitor was proposed and demonstrated. It was found that, by carefully engineering the wavelength detuning and doping concentration of III-V and Si layers, a high modulation efficiency could be achieved by combing the Franz-Keldysh effect and carrier depletion. Moreover, the small capacitance under the depletion mode enhanced the relationship between modulation bandwidth and energy per bit. A III-V/Si hybrid MOS optical modulator working under reverse bias has been experimentally demonstrated with a low $V_{\pi}L$ of 0.12 Vcm. Compared with forward biased case, the reverse biased optical modulator required halved capacitance, which improved modulation bandwidth and energy consumption, simultaneously.

In summary, the III-V/Si hybrid MOS optical phase shifter has been improved and

successfully applied on the optical modulator and optical switch, which are very attractive for high-speed data communication and large-scale optical networking.

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Chapter 1
Introduction

Due to the rapid development in mobile device, cloud service, internet of things (IoT) and dada centers, the thirst for high-data-rate and high-bandwidth optical data communication is surging. Silicon (Si) photonics is a promising platform to address this requirement. However, a major disadvantage of Si photonics is that it lacks integrated light source. Therefore, III-V/Si heterogenous integration is attractive because it enables compact integration of lasers on Si photonics circuits along with more efficient light modulation and detection. In this chapter, the applications for high-speed optical data communication was reviewed. Then, the Si photonics and III-V/Si hybrid photonics platform were introduced. Finally, the research objective and outlines of this dissertation were summarized.

1.1 Demand for high-bandwidth optical interconnect

The global Internet Protocol (IP) data traffic is surging exponentially. According to Cisco, the global IP data traffic will increase 3-fold from 2017 to 2022. By 2022, the monthly global IP data traffic will be 400 exabytes, as shown in Fig. 1.1 [1]. The explosive increase is mainly driven by mobile and wireless device, IoT, video and gaming data. With the upcoming wide deployment of 5G technology that enables unprecedently larger capacity and lower latency, the 5G devices and connections will be over 3 percent of global mobile devices and connections by 2022, which generate nearly 12 percent of global mobile traffic.

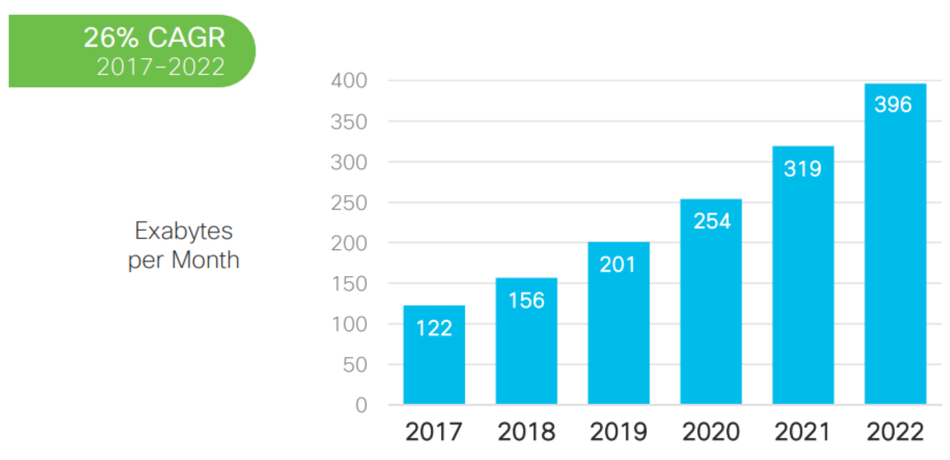

Fig. 1.1. Global IP traffic growth predicted by Cisco [1].

Under this circumstance, data centers are playing an increasingly critical role because they are at the center of providing web service, storage, communication and networking for individual and enterprise customers. By 2021, the east-west traffic, which is the traffic within data centers and traffic between data centers, will account for 85 percent of total traffic associated with data center, while the north-south traffic, which is the traffic exiting the data center to Internet or WAN, is only 15 percent, as shown in Fig. 1.2 [2]. The rapid growth in data center traffic is promoted mainly by cloud traffic. As anticipated, 94 percent

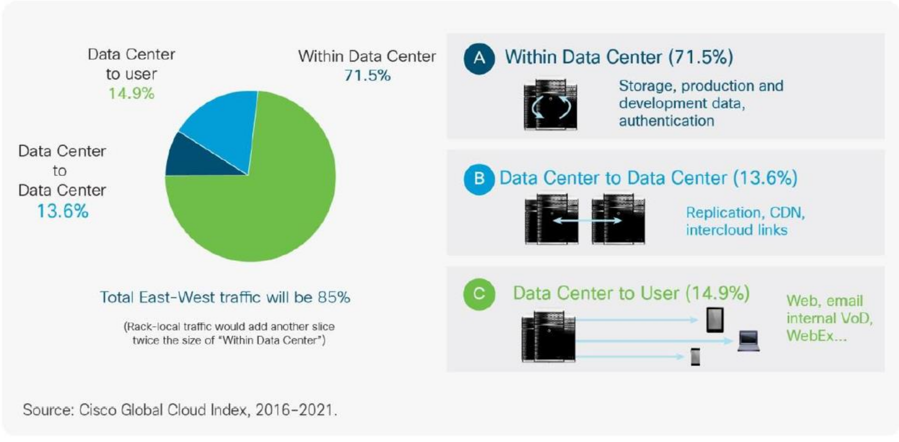

Fig. 1.2. Global data center traffic by destination by 2021 predicted by Cisco [2].

of all workloads and compute instances will be processed in the cloud.

1.2 Hyperscale data centers

To address the need for cloud service and big data storage, traditional small data centers owned and operated by small enterprises are being replaced by more and more hyperscale data centers that are being built and maintained by large operators such as Google, Microsoft, Amazon, Facebook, Apple, Alibaba and others. Figure 1.3 shows the images of hyperscale data centers operated by Google, Microsoft, Amazon and Facebook. Compared with traditional enterprise data centers, hyperscale data centers are larger in physical size and more complex in terms of computing architecture. Although there is no clear definition of hyperscale data center, a hyperscale data center usually has a minimum of 5000 servers and at least 10000 sq ft. in size [3]. For instance, one of the largest hyperscale data centers is in Chicago owned by Microsoft, which occupies 700000 sq. ft. and consumes 198 MW power [4]. The number of hyperscale data center will grow from 338 at the end of 2016 to 628 by 2021, representing 53 percent of all installed data centers

Fig. 1.3. Hyperscale data centers operated by Google, Microsoft, Amazon and Facebook.

by 2021[2].

As distance and data rate increase, the electrical interconnect based on copper becomes challenging because it cannot scale with data rate largely due to frequency dependent loss. For example, copper links have 20 dB loss at data rate higher than 10 Gbps. In contrast, optical interconnect has low loss of around 0.2 dB per kilometer which is independent of data rate [5]. When the bandwidth-distance product has exceeded ~100Gb/s-m, optical interconnection can offer bandwidth, cost and energy advantages as against to electrical interconnection, which is preferable for modern hyperscale data centers where long interconnection distance and high bandwidth are required [6]. In this application scene, Si photonics is progressively replacing Vertical Cavity Surface Emitting Lasers (VCSELs) as a result of increasing distance and bandwidth in hyperscale data centers. Actually, data center interconnection is the largest market for Si photonics. For optical interconnection supporting a distance of 500 m and above, Si photonics product accounts for about 25% of the market [7].

1.3 Si photonics platform

After decades of research and development efforts dedicated by academic community as well as industrial companies, Si photonics has been developed into a mature and competitive technology platform, providing optical interconnect solutions for a wide range of applications. In particular, owning to the compatibility with CMOS technology, Si photonics can be manufactured at wafer scale by leveraging existing CMOS fabrication

infrastructure, process, as well as co-designing with electronics.

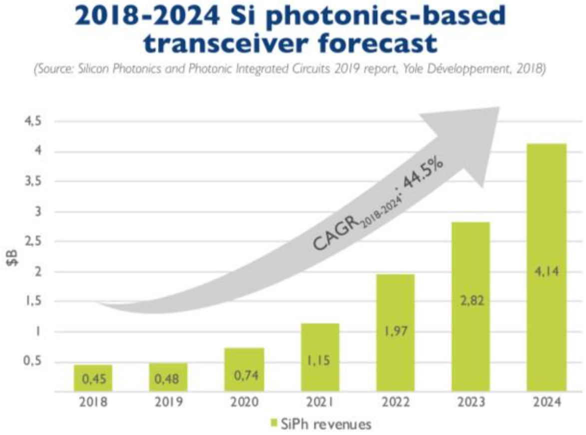

Fig. 1.4. Forecast of revenues from Si photonic-based transceivers [8].

According to a new report by Yole Developpement in 2018, Si photonics will grow from US$ 455 million in 2018 to around US$ 4 billion in 2024, as shown in Fig. 1.4 [8]. Major players, such as Intel, Luxtera, and Acacia, are shipping transceivers to data center market in large volume, while numerous companies, including GLOBALFOUNDRIES, IMEC, STMicroelectronics, and others, are providing foundry service with process design

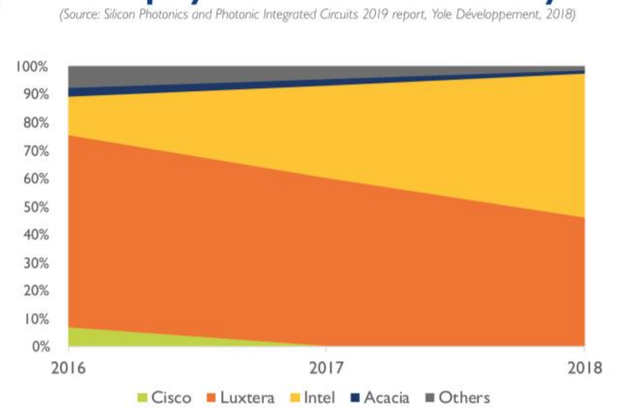

Fig. 1.5. Market share of Si photonics players [8].

kit (PDK).

As shown in Fig. 1.5, the current Si photonics market is almost equally shared by two major players: Luxtera and Intel. Luxtera was founded in 2001 and is a pioneer in the commercialization of Si photonics. It is the first company that introduced a Si-photonics-based transceiver on the market [9]. In their products, Si photonic circuits are fabricated on a photonic die. Then, an electronic die and a packaged Laser are attached to the photonic die, as depicted in Fig. 1.6(a) [10]. The hybrid integration enables independent optimization of photonic and electronic components, allowing for design flexibility and better performance. Since 2017, Luxtera has partnered with TSMC to develop Si photonic transceiver. By leveraging the TSMC's world-class Si process technology, Luxtera has achieved record-breaking optical performance. The grating coupler has under 1 dB loss. The 3-dB bandwidth of phase modulator is over 50 GHz. The germanium photodetector features a high responsivity over 1 A/W and a 3-dB bandwidth higher than 45 GHz [11].

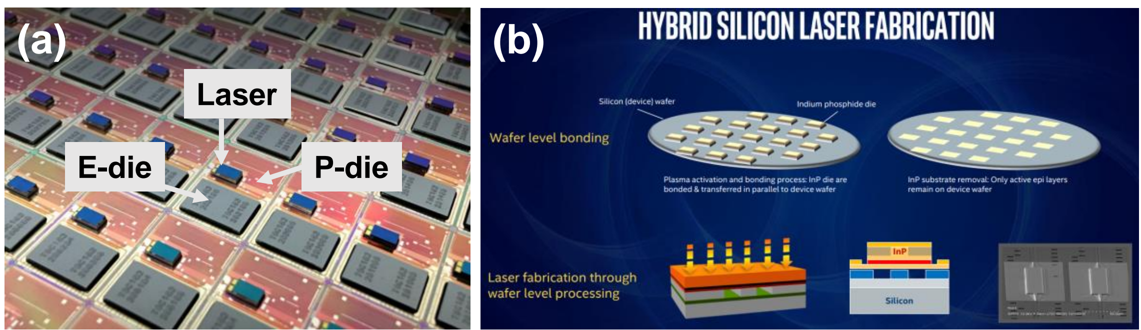

Fig. 1.6. (a) Photonic die with electronic die and laser module bonded from Luxtera [10], and (b) fabrication process of hybrid Si laser from Intel [15].

Intel is a traditional processor supplier for computer systems. In 2016, it introduced a Si photonic transceiver that support 100 Gbps optical interconnection [12]. In contrast to Luxtera that integrate packaged lasers on Si photonic chip, Intel chooses a more compact

scheme by utilizing a hybrid Si laser [13-15]. The fabrication process flow of hybrid Si laser is shown in Fig. 1.6(b) [16]. An indium phosphide (InP) die is bonded on a Si wafer with waveguide pre-defined via oxygen plasma wafer bonding. After removing the InP substrate with only active epitaxial layer remained, wafer-scale process is carried out to fabricate the hybrid laser. The adoption of hybrid Si laser brings a lot of advantages. Firstly, the hybrid Si lasers are created directly on the Si wafer, enabling compact size and dense integration. In addition, the wafer bonding process does not need fine alignment, which allows for high-volume and low-cost manufacturing. Hundreds of lasers can be made by one single bonding step. Furthermore, the hybrid Si laser is compatible with wavelength multiplexing technology. The lasing wavelength can be changed by modifying the Si waveguides property without the need to adjust the InP material, which multiplies the data rate easily. With the arrival of 5G, Intel is expanding the application of its Si photonic transceivers to the fronthaul of 5G network architectures [17].

With the market being occupied by major players, some industrial companies and research institutes, such as GLOBAL FUNDRY [18], STMicroelectronics [19, 20], IMEC [21-23], UCB [24], and so on, are actively providing Si photonics foundry service. Along with the process platform, a PDK compatible with standard EDA tools is provided allowing a co-design environment with comprehensive electronic and photonic libraries.

1.4 Optical phase shifters on Si photonics platform

Figure 1.7 shows a diagram of an optical interconnection and networking system. The emitted light from lasers is input into the optical modulators. Driven by external electrical circuits, optical modulators encode the electrical signals into optical signals. The encoded

optical signals propagate in Si waveguides. The optical switches perform path routing for optical signals in the Si waveguide circuits. At the end of optical interconnect, optical detectors convert the optical signals back into electrical signals which can be further processed by the traditional electrical circuits. Therefore, it is obvious that optical modulator and switch are two fundamental building blocks for optical interconnection and networking system.

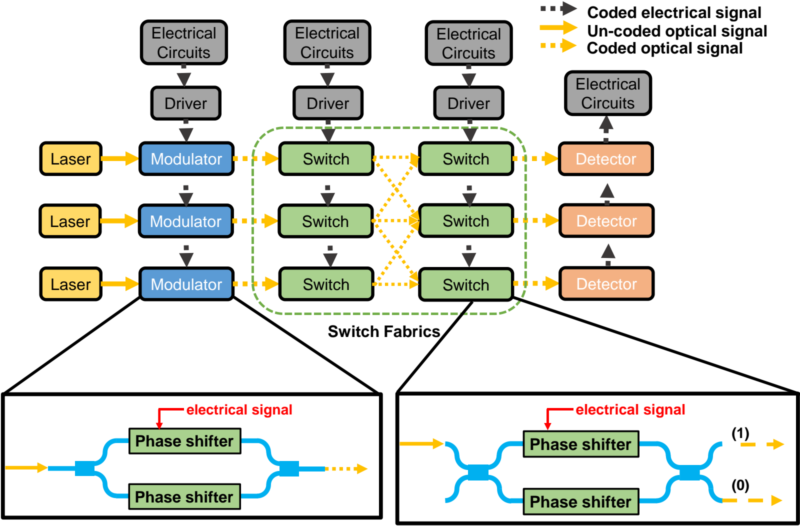

Fig. 1.7. A diagram of an optical networking system on Si photonics platform.

This dissertation focuses on the optical modulator and switch relying on embedded phase shifters, as shown in the insets of Fig. 1.7, for their capability of complex modulation format and optically broadband operation. For this configuration, optical phase shifter is an indispensable part for both optical modulator and optical switch. There are several types of optical phase shifter on Si photonics platform, which is based either on thermo-optic effect or free-carrier plasma dispersion effect, as shown in Table 1.1.

Table 1.1. Optical phase shifters on Si photonic platform

Type		Efficiency	Speed	Energy	Loss
Thermo-optic	SiO_2 Au Si	Low	Ultra-low	High	Ultra-low
Carrier-injection	SiO_2 p i n	High	Low	High	High
Carrier-depletion	SiO_2 p+ p n n+	Low	Ultra-fast	Low	Ultra-high
Carrier-accumulation	SiO_2 n p	High	Fast	Ultra-low	Medium

Thermo-optic effect is the change of refractive index by temperature variation. The great advantage of thermo-optic phase shifter is its ultra-low optical loss. Hence it is widely used in optical switch fabrics where tens of phase shifters are cascaded on the optical path [25, 26]. Another application area of thermo-optic phase shifter is for phase tuning and correction in ring resonator or optical switch [27, 28]. Thermo-optic phase shifter has micro-second (μs) transition time [29, 30], making it unsuitable for high-speed application. The milliwatt power consumption of thermo-optical phase shifter also strain the overall power budget in large-scale integration case.

Free-carrier plasma dispersion effect is the change of refractive index by the variation of free carrier density. The free carrier density can be manipulated by different methods, including carrier injection through a p-i-n junction, carrier depletion through a p-n junction, and carrier accumulation through a semiconductor-insulator-semiconductor capacitor. The carrier-injection optical phase shifter is easy for fabrication and can realize very high modulation efficiency owing to the large density of injected free carriers [31]. Like thermo-optic phase shifter, the carrier-injection optical phase shifter is also limited by milliwatt

power consumption due to the large injection current, and low modulation speed because of the relative long minority carrier lifetime [32, 33]. The optical modulator based upon carrier depletion is capable of ultra-fast modulation. High data rates of 40~60 Gb/s have been demonstrated on this modulator structure [34-36]. One challenging issue of carrier-depletion effect is the balance between optical modulation and insertion loss. The high modulation efficiency calls for high doping concentration that inevitably cause larger free carrier-induced absorption loss.

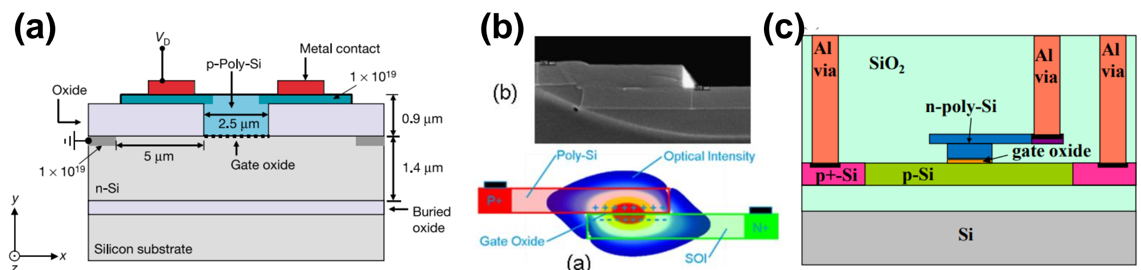

Fig. 1.8. Si MOS-type optical modulator demonstrated by (a) Intel [37], (b) Cisco [41], and (c) PETRA [42].

In 2004, the research group from Intel demonstrated the first Si photonic optical modulator with over 1 GHz modulation bandwidth, as shown in Fig. 1.8(a) [37]. The optical modulation is realized by inducing carrier accumulation in the capacitor formed by p-poly-Si/oxide/n-Si, which is also called MOS capacitor or SIS capacitor. Since the concentration of accumulated carriers is independent on the doping concentration in the semiconductor layer, this type of optical phase shifter can provide relatively higher modulation efficiency even with low doping concentration in the modulation region [38-40].

To fabricate such a MOS structure, a thin oxide layer is firstly formed on the bottom Si layer, followed by the deposition of an amorphous Si layer, as shown in Fig. 1.8 (b) and (c) [41, 42]. After that, post-deposition annealing is carried out to enable the phase change from amorphous Si to poly-Si for lower absorption loss and higher doping concertation. However, the abundant grain boundaries and lattice defects in poly-Si material still cause significant intrinsic absorption loss around 5 dB/mm [43-45]. Another drawback of poly-Si layer is that its low doping efficiency makes it difficult to realize low resistance required for large modulation bandwidth. Many efforts have been put to optimize the amorphous silicon deposition process and post-deposition annealing process to reduce the absorption loss and resistivity from poly-Si layer, as shown in Fig. 1.9(a) and (b) [42, 46, 47]. It is also

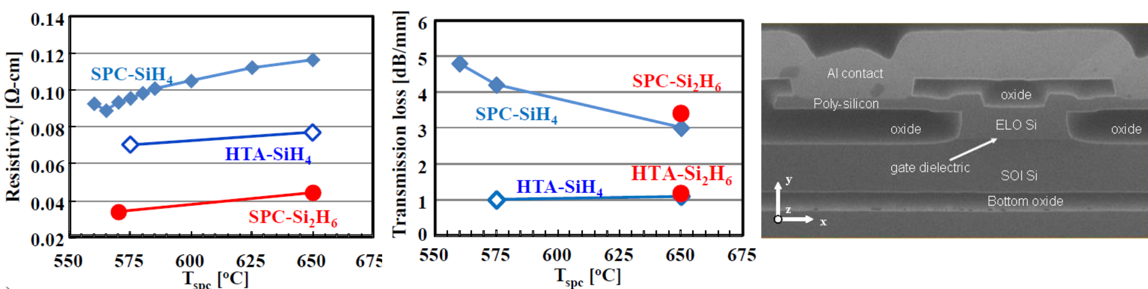

Fig. 1.9. (a) Resistivity and (b) transmission loss dependence on T_{spc} in the case of solid-phase-crystallization (SPC) of SiH4- and Si2H6-based poly-Si and SPC of SiH4-based poly Si with high-temperature annealing (HTA). (c) A transmission electron microscopy (TEM) image of a MOS Si optical layer with the top Si layer grown by epitaxial lateral overgrowth (ELO)

possible to replay the poly-Si layer with epitaxial Si layer but at the cost of process complexity, as shown in Fig.1.9(c) [48].

In addition to the issue of poly-Si, there is an intrinsic and challenging balance for all

the MOS type optical phase shifters, which is the trade-off between modulation efficiency and modulation bandwidth. The MOS type optical phase shifter relies on a semiconductor-insulator-semiconductor capacitor for phase change. The high modulation efficiency necessitates a large capacitance which will in turn limit the RC limited modulation bandwidth.

In order to break this relationship, a III-V/Si hybrid MOS optical phase shifter was proposed, as shown in Fig. 1.10 [49, 50]. III-V materials feature small electron effective mass and high electron mobility. The small electron effective mass enhanced the free-carrier plasma dispersion effect, while the high electron mobility enables low resistance

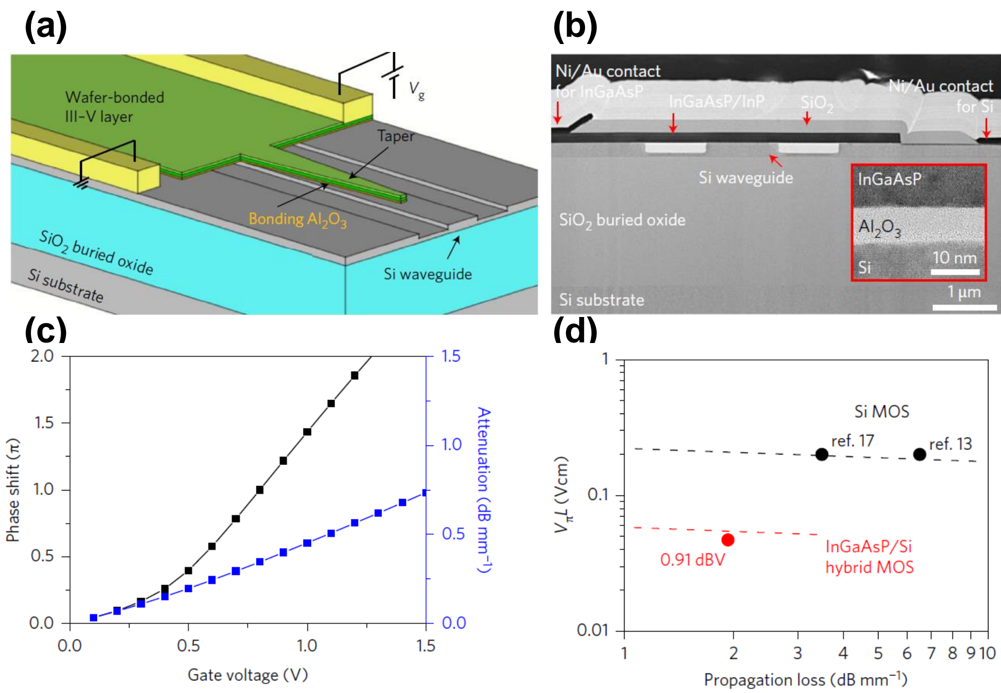

Fig. 1.10. (a) Three-dimensional view of the InGaAsP /Si hybrid MOS optical modulator, (b) scanning electron microscope (SEM) image of the fabricated device, (c) calculated phase shift and attenuation of an InGaAsP/Si hybrid MOS optical modulator and (d) relationship between $V_\pi L$ and propagation loss, from [50].

which is preferable for high speed modulation. For optical phase shifters, $V_\pi L$, the product of phase shifter length and voltage required for π phase shift, is commonly adopted as a figure of merit. The III-V/Si hybrid MOS optical phase shifter demonstrated extremely high modulation efficiency with a $V_\pi L$ of 0.047 Vcm. Owning to the low absorption in III-V layer, the loss at π phase shift is only 0.23 dB. Compared with its Si counterparts, the III-V/Si hybrid MOS optical phase shifter has increased modulation efficiency by 5 times and reduced the absorption loss by a factor of 10, simultaneously.

1.5 Research objectives

Even though the III-V/Si hybrid MOS optical phase shifter has exhibited extraordinary performance, there is still a lot of worthwhile work. Firstly, the performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter has not been fully understood. Higher modulation efficiency is achievable by enhancing the interaction between optical mode and free carriers through structure modification. It is also necessary to remove parasitic capacitances which are limiting the modulation bandwidth of the current optical modulator. Equivalent oxide thickness (EOT) scaling is another way to effectively increase the modulation efficiency, which has not been demonstrated yet. In addition, the modulation bandwidth of the III-V/Si hybrid MOS phase shifter is limited by Resistance-Capacitance (RC) constant. Removing all the parasitic capacitances is necessary to achieve high modulation operation. In addition to being used in a MZI optical modulator, there are a variety of devices that can benefit from the integration of III-V/Si hybrid MOS optical phase shifter, such as optical switch, ring resonator and so on.

1.6 Thesis outline

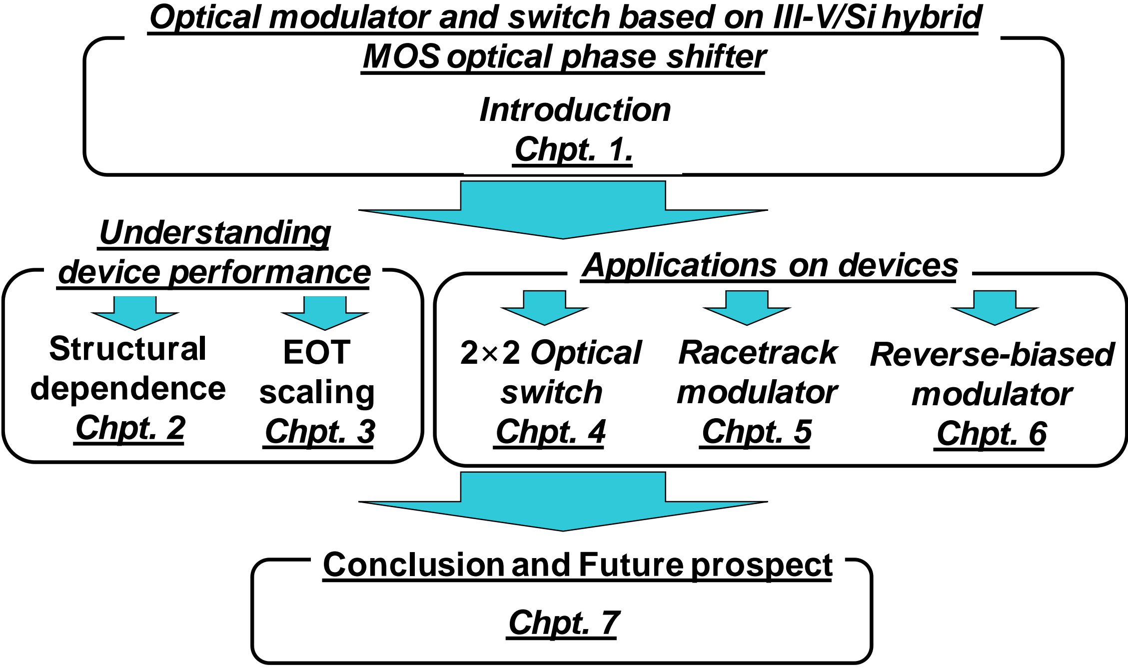

Fig. 1.11. Overview of this dissertation.

Figure 1.11 shows the organization of this dissertation, which focuses on the understanding as well as the application of III-V/Si hybrid MOS optical phase shifter.

In chapter 2, the performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter was studied through numerical simulations, which deepens our understanding on the device. The structure of III-V/Si hybrid MOS optical phase shifter has been improved by introducing an isolation trench and using Si waveguide embedded in SiO_2 to completely remove all the parasitic capacitances for high-speed operation. In chapter 3, the EOT scaling was successfully demonstrated by introducing HfO_2 into the Al_2O_3 bonding layer, which enables even higher modulation efficiency. In chapter 4 and 5, we presented the application of III-V/Si hybrid MOS optical phase shifter in a 2×2 optical switch and a racetrack resonator, respectively. In chapter 6, in order to further improve the

trade-off relationship between modulation efficiency and modulation bandwidth, an efficient III-V/Si hybrid MOS optical phase shifter by combing the FK effect and carrier depletion was proposed and demonstrated. Finally, chapter 7 present the conclusion of the dissertation and possible future works.

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Chapter 2
Performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter

In our previous study, we have demonstrated an optical modulator based on III-V/Si hybrid MOS optical phase shifter, exhibiting high modulation efficiency with a $V_{\pi}L$ around 0.05 Vcm. However, the performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter has not been fully studied which means there is still large room for improvement. In this chapter, we carried out a systematic study on the structure-dependent performance of III-V/Si hybrid MOS optical phase shifter. In addition, the parasitic capacitance was removed by introducing an isolation trench on one side of the Si waveguide or using Si waveguide embedded in SiO_2 layer.

2.1. Introduction

In order to break the inherent trade-off relationship between modulation efficiency and modulation bandwidth in Si metal-oxide-semiconductor (MOS)-type optical modulators, we have proposed a III-V/Si hybrid MOS optical modulator by using direct wafer bonding [1, 2]. Owing to large change in refractive index induced by the electrons in III-V material near the MOS interface, the hybrid MOS optical modulator showed extremely high modulation efficiency with a $V_{\pi}L$ of 0.047 Vcm, which is 5 times smaller than that of its Si counterparts. Furthermore, the optical absorption loss at π phase shift is

only 0.23 dB, which is 10 times smaller than Si MOS-type optical modulators. Therefore, the III-V/Si hybrid MOS optical modulator is promising for high-efficiency and low-loss optical modulation.

Despite the amazing performance demonstrated by the III-V/Si hybrid MOS optical modulator, there is plenty of room for further improvement. Firstly, the optical confinement factor in the III-V layer is low because the Si layer is almost twice thick as the III-V layer. Secondly, the modulation bandwidth is limited by the large resistance-capacitance (RC) constant which is dominated by parasitic effect. The parasitic capacitance is 8 times larger than the intrinsic capacitance. In this chapter, a comprehensive simulation study was conducted to understand the performance dependence on the device structure. Additional processes were also proposed to remove the parasitic capacitance.

2.2. Performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter

2.2.1. Modeling of III-V/Si hybrid MOS optical phase shifter

Fig. 2.1 shows the structure of III-V/Si hybrid MOS optical phase shifter used in

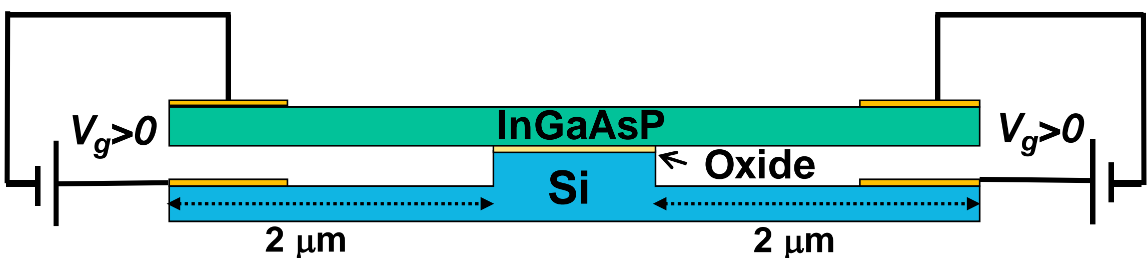

Fig. 2.1. The structure of III-V/Si hybrid MOS optical phase shifter used in simulation.

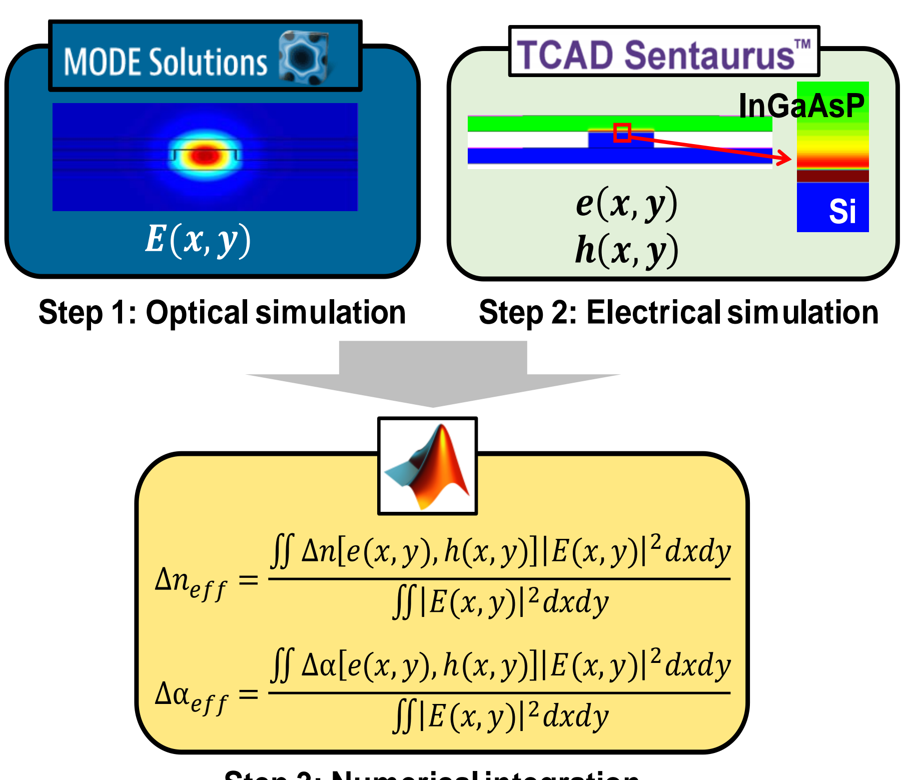

Fig. 2.2. The simulation flow adopted in this study.

simulations. Indium gallium arsenide phosphide (InGaAsP) lattice-matched to indium phosphide (InP) with bandgap energy of 0.91 eV (bandwidth wavelength λ_g=1.37 μm) was used as the III-V material to maximize the free-carrier plasma dispersion effect.

Fig. 2.2 shows the simulation flow adopted in this study. Firstly, optical simulation was conducted using Lumerical MODE Solutions to obtain the fundamental transverse electric (TE) mode. The electric filed intensity of the TE mode as a function of space ($E(x,y)$) was extracted. Then, electrical simulation was conducted using Sentaurus TCAD tools. The distribution of electrons and holes across the cross-section of III-V/Si hybrid MOS optical phase shifter ($e(x,y)$ and $h(x,y)$) was obtained. In the final step, the results from optical and electrical simulations were combined in a numerical integration over the whole cross-section. The presence of electrons and holes in the phase shifter induced

changes in refractive index ($\Delta n[e(x,y),h(x,y)]$) and absorption coefficient $\Delta\alpha(e(x,y),h(x,y))$. In Si layer, only free-carrier plasma dispersion effect was considered [3, 4]. In III-V layer, band-filling effect and bandgap shrinkage effect were also taken into consideration in addition to free-carrier plasma dispersion effect [2]. The change in the effective refractive index (Δn_{eff}) and absorption coefficient ($\Delta\alpha_{eff}$) were calculated by the integration as shown in Fig. 2.2 [5]. Δn_{eff}can be converted to the change in optical phase ($\Delta\varphi$) by $\Delta\varphi = 2\pi\Delta n_{eff}L_{ps}/\lambda$ where L_{ps} is the length of phase shifter.

2.2.2. Dependence of modulation efficiency on the doping concentration in InGaAsP layer

When a positive gate voltage (V_g) was applied on the III-V/Si hybrid MOS optical phase shifter, both electrons in III-V layer and holes in Si layer accumulated on the MOS interfaces, modulating optical phase. However, the optical phase shift induced by the electrons in III-V layer is much greater than that induced by the holes in Si layer because

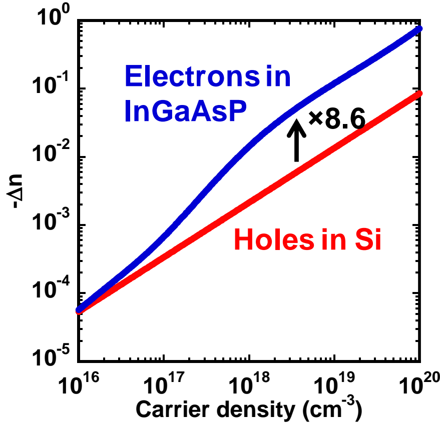

Fig. 2.3. Change in refractive index induced by electrons in InGaAsP (blue) and holes in Si (red).

III-V material has a lighter electron refractive mass. Figure 2.3 shows the change in refractive index induced by the electrons in InGaAsP and holes in Si. When the carrier density was higher than 3×10^{18} cm^{-3}, the refractive index change induced by the electrons in InGaAsP was more than 8.6 times larger than that induced by the holes in Si. Hence, the optical phase modulation was dominated by the electron-induced effect in the InGaAsP layer. It is necessary to examine the influence of doping concentration in InGaAsP layer on the modulation efficiency of III-V/Si hybrid MOS optical phase shifter.

The dependence of modulation efficiency on the doping concentration in InGaAsP layer (N_d-InGaAsP) was studied by simulations as shown Fig. 2.2. The doping concentration in Si layer (N_a-Si) was fixed as 1×10^{17} cm^{-3}. Figure 2.4 shows the change of $V_\pi L$ with N_d-InGaAsP. With N_d-InGaAsP varying from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}, the change of $V_\pi L$ was within 0.002 Vcm, indicating that the modulation efficiency was weakly dependent on N_d-InGaAsP. It is because that high concentration of free carriers can accumulate on the MOS interfaces irrespectively of the doping concentration in III-V and Si layers. Hence, high modulation efficiency is achievable by using semiconductor layers with comparatively lower doping concentration, avoiding the severe free-carrier-induced

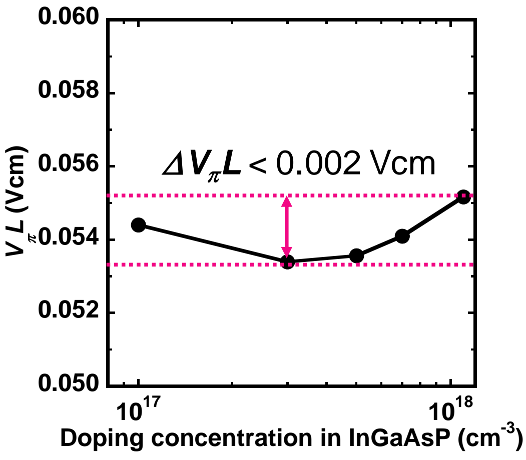

Fig. 3.4. $V_\pi L$ as a **function** of N_d-InGaAsP with N_a-Si was fixed as 1×10^{17} cm^{-3}.

loss as the case in the optical modulators based on carrier depletion. However, a minimum amount of doping concentration is required to ensure large modulation bandwidth.

The variation of $V_\pi L$ with N_d-InGaAsP was due to the change of distribution profile of accumulated carriers on the MOS interfaces. Fig. 2.5 shows the distribution profiles of accumulated electrons near the MOS interface at 1-V bias with different N_d-InGaAsP. With higher N_d-InGaAsP, the peak density of accumulated electrons increased while the thickness of accumulation layer which can be described as Debye length decreased. Higher density of accumulated electrons near the MOS interface induced larger change in the refractive index. On the other hand, thinner accumulation layer degraded the overlap between optical mode and accumulated electrons. These two opposite effects lead to the variation of $V_\pi L$ with N_d-InGaAsP.

2.2.3. Dependence of modulation efficiency on the thickness ratio between InGaAsP and Si layers

In the previous demonstration, a 110-nm-thick InGaAsP layer and a 220-nm-thick Si

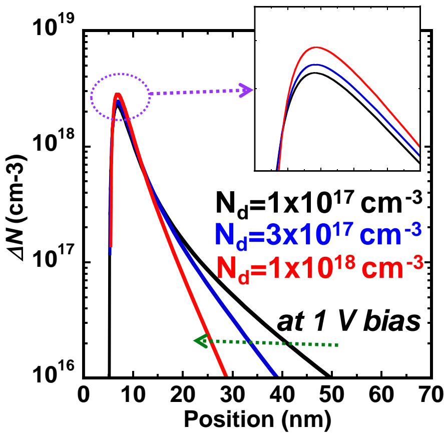

Fig. 4.5. Distribution profile of accumulated electrons on the MOS interface with different N_d-InGaAsP.

layer was adopted for the fabrication of III-V/Si hybrid MOS optical phase shifter. However, the optical confinement factor in the InGaAsP layer was only 22.7%. It was due to that the Si layer was two times thick as InGaAsP layer. The optical mode distributed almost equally in InGaAsP and Si layers since their refractive indexes are very close (n_{Si}=3.48, $n_{InGaAsP}$=3.44). Hence, better overlap between optical mode and accumulated free carriers can be obtained by adjusting the thickness ratio between InGaAsP and Si layer, leading to enhanced modulation efficiency.

The thickness ratio was defined as $t_{InGaAsP}/t_{Si}$. The total thickness was kept same as last demonstration (330 nm) while the thickness ratio was changed from 0.5 to 1.54. Fig. 2.6 shows the change of $V_\pi L$ as a function of thickness ratio. With the thickness ratio increasing from 0.5 to 1, the $V_\pi L$ was reduced from 0.054 Vcm to 0.046 Vcm. When the thickness ratio was 1, the modulation efficiency was maximized indicating enhanced interaction between optical mode and accumulated free carriers.

Fig. 2.7(a) and (b) shows the fundamental TE mode of III-V/Si hybrid MOS optical phase shifter with thickness ratio of 0.5 and 1.0, respectively. Fig. 2.7(c) and (d) shows the distribution of normalized optical intensity ($|E|^2$) and free carriers of III-V/Si hybrid MOS

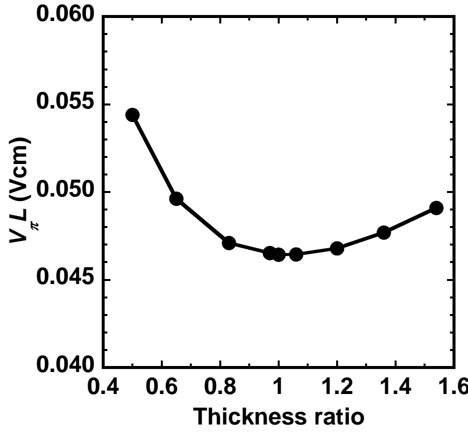

Fig. 5.6. $V_\pi L$ as a function of thickness ratio between InGaAsP and Si layer.

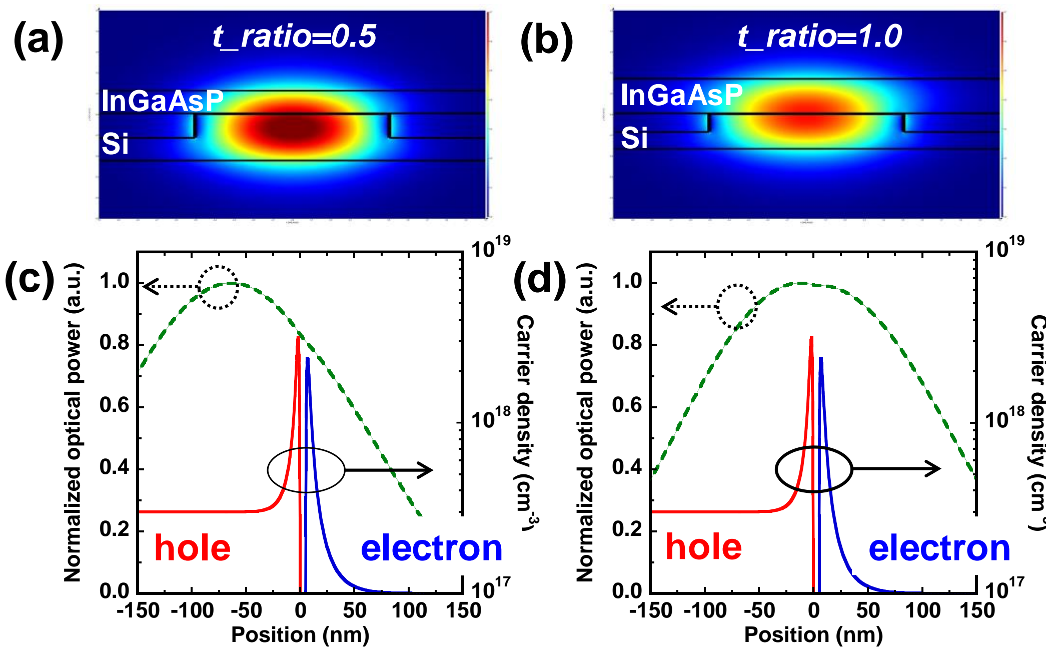

Fig. 6.7. Fundamental TE mode of III-V/Si hybrid MOS optical phase shifter with thickness ratio of (a) 0.5 and (b) 1.0. Distribution of normalized optical power and free carriers in III-V/Si hybrid MOS optical phase shifters with thickness ratio of (c) 0.5 and

optical phase shifter with thickness ratio of 0.5 and 1.0, respectively. The optical intensity was obtained by normalizing the electric files strength to the largest value and squared ($|E/E_{max}|^2$). When the thickness ratio was 0.5, the peak of optical intensity was inside Si

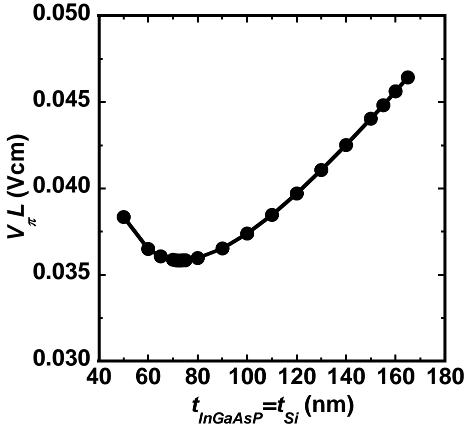

Fig. 7.8. $V_{\pi}L$ as a function of thickness of InGaAsP (Si) layer.

layer and far wary from the MOS interfaces where the free carriers accumulated. When the thickness ratio was 1.0, the peak of optical intensity resides on the MOS interfaces, leading to better overlap between optical mode and accumulated free carriers, and enhanced optical modulation.

2.2.4. Dependence of modulation efficiency on the total thickness of InGaAsP and Si layers

In this section, the dependence of modulation efficiency on the total thickness of InGaAsP and Si layers was explored. The thickness of InGaAsP and Si layers ($t_{InGaAsP}$, t_{Si}) was fix as same to align the peak of optical intensity with the accumulated free carriers.

Fig. 2.8 shows the change of $V_{\pi}L$ as a function of $t_{InGaAsP}$ (t_{Si}). When $t_{InGaAsP}$ (t_{Si}) was reduced from 165 nm to 72 nm, $V_{\pi}L$ was also reduced. When $t_{InGaAsP}$ (t_{Si}) was below 72 nm, $V_{\pi}L$ was enlarged. The dependence of $V_{\pi}L$ on $t_{InGaAsP}$ (t_{Si}) is associated with the optical

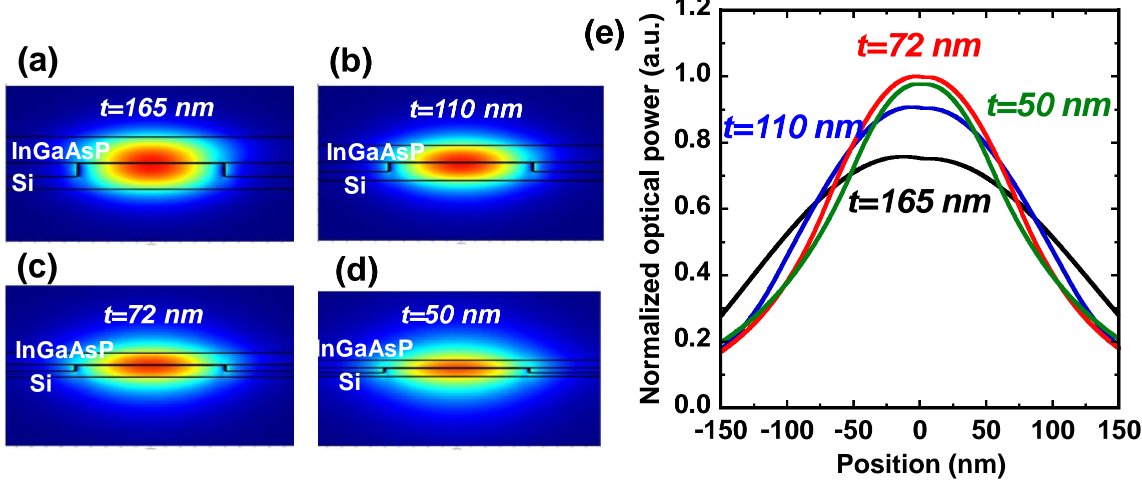

Fig. 8.9. (a)~(d) Fundamental TE mode and distribution of normalized optical power of III-V/Si hybrid MOS optical phase shifter with different thickness of InGaAsP and Si layers.

mode profile and the normalized optical intensity as shown in Fig. 2.9.

The optical intensity was normalized to the value of optical power integrated over the cross-section of the III-V/Si hybrid MOS optical phase shifter with 72-nm-thick InGaAsP and Si layers. With $t_{InGaAsP}$ (t_{Si}) decreasing from 165 nm to 72 nm, the peak of optical intensity increased because the optical mode was more effectively confined. With $t_{InGaAsP}$ (t_{Si}) smaller than 72 nm, the optical mode was leaking outside of the III-V/Si hybrid MOS optical phase shifter, resulting into reduced modulation efficiency and increased $V_{\pi}L$.

To sum up, the peak of optical intensity can be aligned with accumulated free carriers by using InGaAsP and Si layers with the same thickness. The intensity of optical mode can be maximized by thinning the thickness of InGaAsP and Si layer to 72 nm. Fig. 2.10 shows the performance of two kinds of III-V/Si hybrid MOS optical phase shifter. The length of the phase shifter was assumed as 1 mm. The blue line is for III-V/Si hybrid MOS optical phase shifter with 110-nm-thick InGaAsP layer and 220-nm-thick Si layer, which is the structure adopted in the previous demonstration, while the red line is for III-V/Si hybrid MOS optical phase shifter with 72-nm-thick InGaAsP and Si layer, which is optimized for

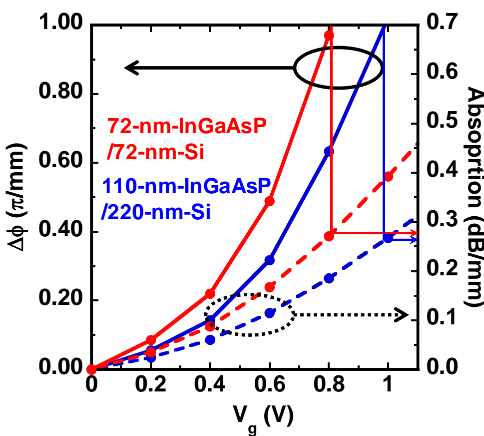

Fig. 9.10. Optical phase shift and absorption as a function of V_g.

high modulation efficiency. Comparing with the previous demonstration, the new structure has improved the modulation efficiency by reducing $V_{\pi}L$ to 0.0358 Vcm. Unfortunately, the absorption was increased by 0.0136 dB/mm due to the enhanced interaction between optical mode and accumulated free carriers.

2.3. Parasitic capacitance removal for high-speed operation.

In addition to the modulation efficiency, there is also room for improving the modulation bandwidth. In the previous demonstration, the modulation bandwidth was 100 MHz, which is limited mainly by the parasitic capacitance and contact resistance. The large contact resistance could be easily reduced by inclusion of a heavily-doped area in the metal contact region. In this section, parasitic capacitances have been removed firstly by introducing an isolation trench on one side of Si waveguide, and then by using Si waveguide embedded in SiO_2.

2.3.1 Proposals to remove parasitic capacitances

Figure 2.11(a) shows the equivalent circuit of III-V/Si hybrid MOS optical phase shifter in the previous demonstration. There are two parasitic capacitances residing on both left and right sides of the intrinsic capacitance that realizes the optical phase modulation. The parasitic capacitance was 8 times in total larger than the intrinsic one, significantly limiting the achievable modulation bandwidth. In the first solution shown in Fig. 2.11(b), an isolation trench was introduced on the right side of the Si rib waveguide, to electrically isolate the parasitic capacitance on the right side, which is 6 times larger than the intrinsic

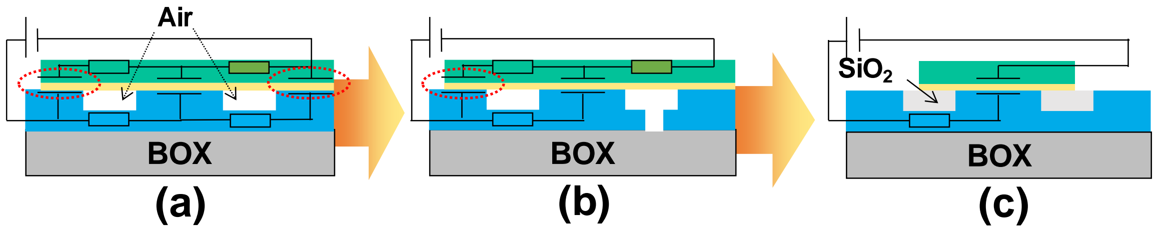

Fig. 2.11. (a) Equivalent circuit of III-V/Si hybrid MOS optical phase shifter in previous demonstration, (b) introduction of an isolation trench on one side of Si waveguide, and (c) using Si waveguide embedded in SiO_2.

capacitance. In Fig. 2.11(c), we also proposed to fill the air gaps with SiO_2 followed by a chemical mechanical polishing (CMP) process, which can completely eliminate the parasitic capacitance on the left terrace.

2.3.2 Introduction of an isolation trench on Si waveguide to isolate parasitic capacitance

In order to ensure robust wafer bonding as well as enough space for metal contact to III-V layer, a large area of III-V layer is bonded on the right Si terrace, as shown in Fig. 2.12(a). The width of the parasitic III-V/Si hybrid MOS capacitor on the right terrace is 6 μm, contributing to the largest part of parasitic capacitance. Figure 2.12(b) shows a *C-V* curve of a III-V/Si hybrid MOS optical phase shifter before any reduction of parasitic capacitances with an inset showing the distribution of parasitic capacitances. The length of the phase shifter is 250 μm. The intrinsic capacitance is 1.69 pF, indicating an EOT of 5.1 nm. However, the parasitic capacitance on the right is 10.12 pF that is 6 times larger than the intrinsic capacitance and account for the 86% of the total parasitic capacitance. In the

next demonstration, an isolation trench was successfully introduced on the right side of the Si rib waveguide, electrically removing the largest parasitic capacitance.

Figure 2.12(c) shows a TEM image of a III-V/Si hybrid MOS optical phase shifter with an isolation trench, in which the III-V and Si layer as well as an isolation trench are clearly shown. Figure 2.12(d) shows the C-V curve of a III-V/Si hybrid MOS optical phase

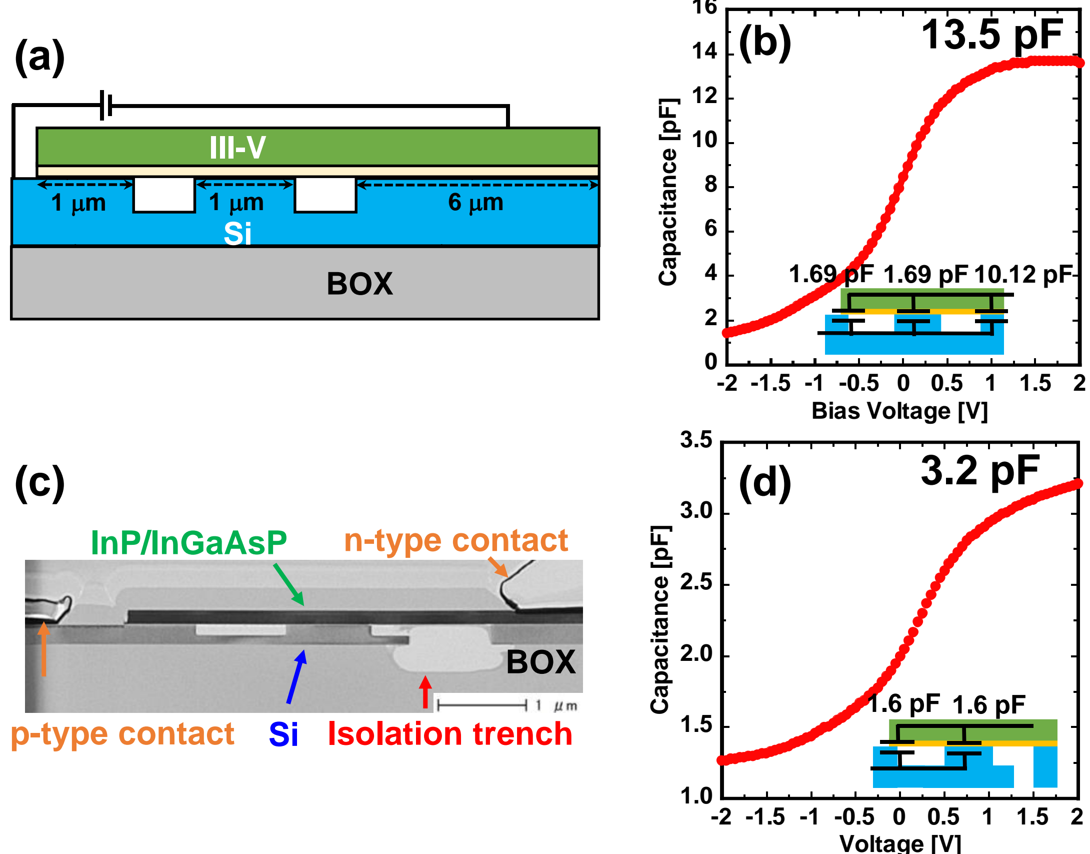

Fig. 2.12. (a) A cross-sectional schematic of the III-V/Si hybrid MOS optical phase shifter, (b) The *C-V* curve of a III-V/Si hybrid MOS optical phase shifter without reduction of parasitic capacitance, (c) a TEM image of a III-V/Si hybrid MOS optical phase shifter with an isolation trench, and (d) The *C-V* curve of a III-V/Si hybrid MOS optical phase shifter with an isolation trench.

shifter with an isolation trench. The intrinsic capacitance is 1.6 pF, corresponding to an EOT of 5.4 nm. With the largest parasitic capacitance being removed, the total capacitance was reduced to 3.2 pF. Therefore, the introduction of an isolation trench has effectively reduced the parasitic capacitance by 86%.

2.3.3 III-V/Si hybrid MOS optical phase shifter with Si waveguide embedded in SiO_2

In order to completely remove all the parasitic capacitances, a SiO_2 filling process followed by a CMP process is necessary, as proposed in Fig. 2.11(c). Figure 2.13(a) shows the proposed process flow. A wafer bonding test was conducted to verify the feasibility of

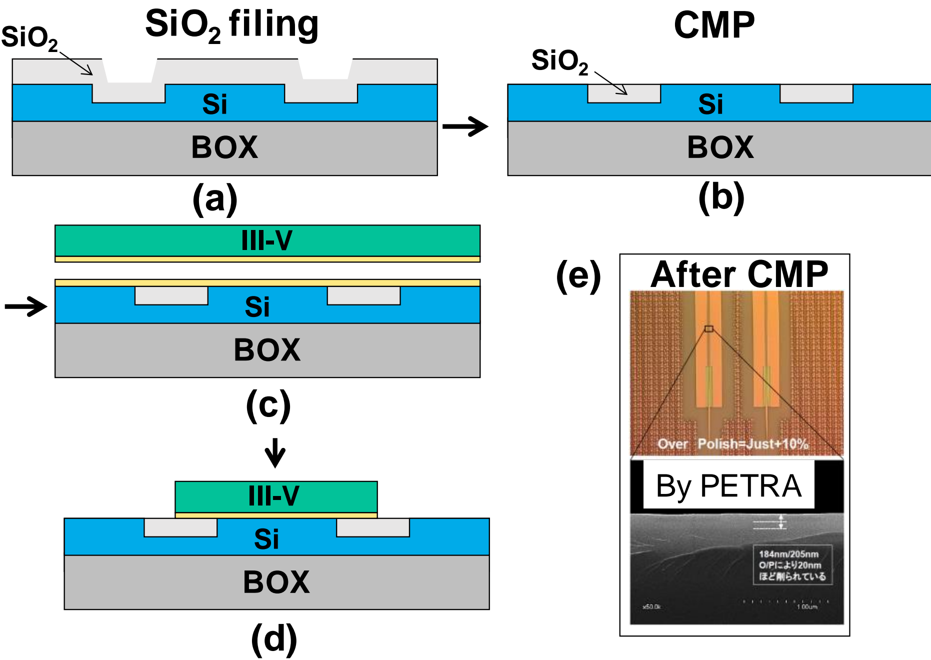

Fig. 2.13. (a)~(d) Process flow of SiO_2 filling followed by CMP, and (e). a photo image and a TEM image of the processed Si wafer.

bonding III-V wafer on uneven SiO_2 surface. Figure 2.14 shows a photo image of a Si wafer with III-V layer bonded. In spite of the surface fluctuation, III-V layer was well-bonded on the processed Si wafer, which lay the foundation for the further experimental demonstration of a III-V/Si hybrid MOS optical phase shifter without any parasitic capacitance.

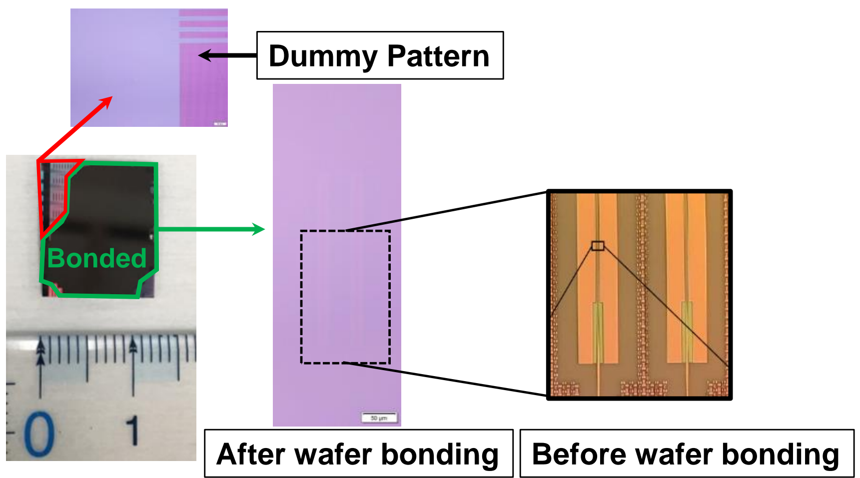

Fig. 2.14. Photo images of a processed Si wafer with III-V layer bonded on the surface.

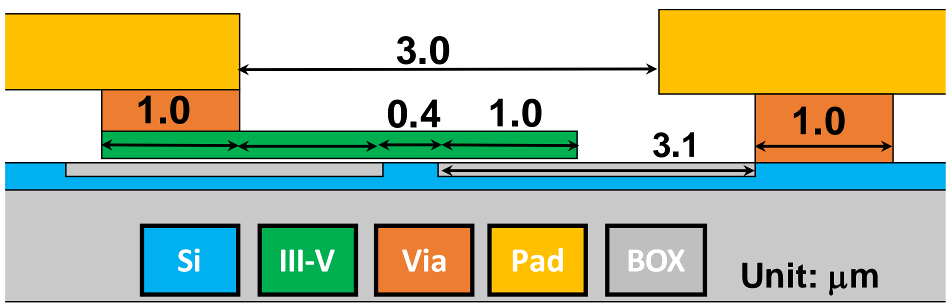

Fig. 2.15. Design of III-V/Si hybrid MOS optical phase shifter using Si waveguide embedded in SiO_2.

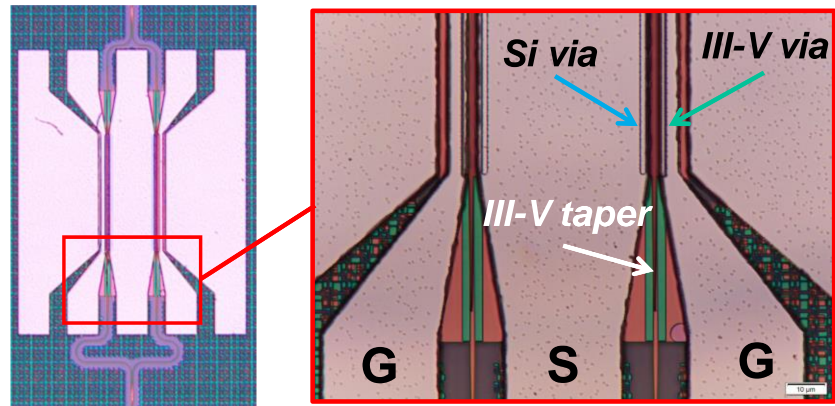

Fig. 2.16. A photo image of III-V/Si hybrid MOS optical phase shifter designed for removing parasitic capacitance.

Fig. 2.15 shows the design of III-V/Si hybrid MOS optical phase shifter without parasitic capacitance. By using a Si waveguide embedded in SiO_2, the bonding region of III-V on Si is able to be confined near the Si waveguide avoiding its overlap with Si terrace. The optical modulator was aimed to operate in O band (1260 nm ~ 1360 nm). Thus, InGaAsP lattice matched to InP substrate with bandgap wavelength of 1.19 μm was used in the III-V/Si hybrid MOS optical phase shifter.

The optical modulator with this design has been successfully fabricated. Fig. 2.16 shows a photo image of the device. In the zoomed-in photo, the Si via, III-V via and III-V taper were clearly shown. EOT extracted from a p^+-Si/Al_2O_3/III-V hybrid MOS capacitor was 7.2 nm. The capacitance of a phase shifter can be calculated from the EOT value and the size of III-V/Si bonding region. The capacitance was calculated as 0.46 pF.

Fig. 2.17(a) shows a capacitance-voltage (*C*-*V*) curve of III-V/Si hybrid MOS optical phase shifter measured with 1 MHz. The measured accumulation capacitance was 0.66 pF, which is larger than the calculated value. However, it was caused by large leakage current rather than design. Fig. 2.17(b) shows the *C*-*V* curves of the same phase shifter measured

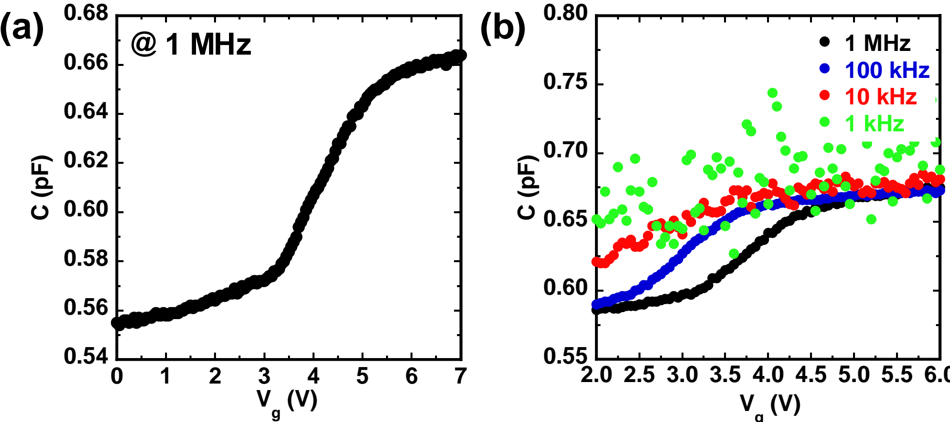

Fig. 2.17. (a) *C-V* curve of III-V/Si hybrid MOS optical phase shifter measured with 1 MHz, and (b) *C-V* curves of III-V/Si hybrid MOS optical phase shifter measured with different frequencies.

at four different frequencies: 1 MHz, 100 kHz, 10 kHz and 1 kHz. A severely large frequency dispersion was observed and no well-behaved *C-V* curves were obtained at lower frequencies, indicating high density of interface traps and large leakage current.

Fig. 2.18 shows the ratio of parasitic capacitance to the total capacitance for different

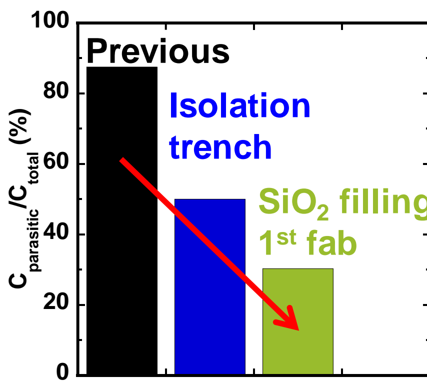

Fig. 2.18. Ratio of parasitic capacitance to the total capacitance for different design of III-V/Si hybrid MOS optical phase shifter.

designs of III-V/Si hybrid MOS optical phase shifter. In the previous demonstration, the ratio of parasitic capacitance to the total capacitance was over 87.5%. By introducing an isolation trench on one side of Si waveguide, the ratio was reduced to 50%. In the final design, the measured capacitance was 1.30 times larger than the intrinsic capacitance. By

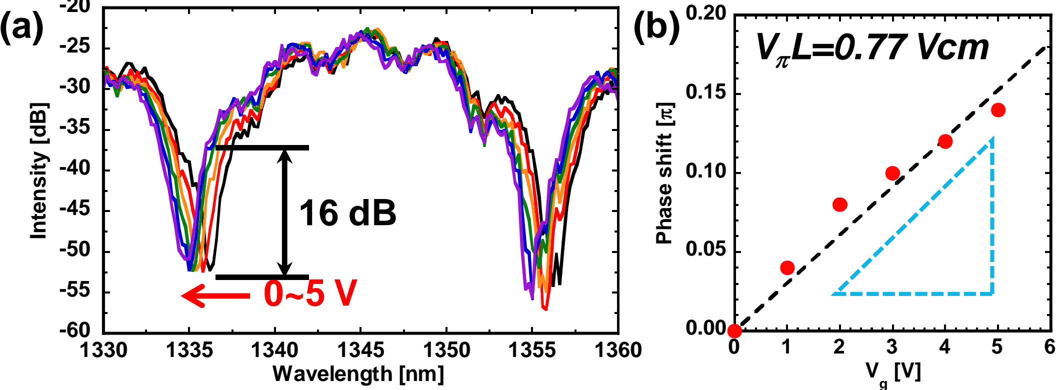

Fig. 2.19. (a) Measured transmission spectra of III-V/Si hybrid MOS optical modulator with varied V_g and (b) phase shift as a function of V_g.

improving the interfacial quality of the III-V/Si hybrid MOS capacitor, all the parasitic capacitance is expected to be removed completely.

Fig. 2.19(a) shows measured transmission spectra of the III-V/Si hybrid MOS optical modulator with various V_g. The length of the phase shifter was 240 μm. The optical phase shift was calculated as $\Delta\varphi = 2\pi\Delta\lambda/FSR$, where $\Delta\lambda$ is the change of resonating peak near 1335 nm and FSR is the free-spectral-range. Fig. 2.19(b) shows the phase shift as a function of V_g. $V_\pi L$ was calculated from the slope of the fitting in Fig. 2.19(b) as $V_\pi L = \frac{FSR \cdot L_{PS}}{2\left(\frac{\Delta\varphi}{\Delta V}\right)}$, where L_{PS} was phase shifter length. The $V_\pi L$ was calculated as 0.77 Vcm. In 2017, we have demonstrated a $V_\pi L$ of 0.097 Vcm with 6.0-nm EOT and similar III-V material in 1310-nm band [6]. The degradation of $V_\pi L$ compared with previous result was due to the large

density of interfacial traps and defects probably caused by the over-polishing in the CMP process. In the future, the Si waveguide embedded in SiO_2 without over-polishing will be used, which means there will be a thin SiO_2 layer remaining on top of Si waveguide. The interfacial quality of SiO_2/Si interface will be examined by *C-V* measurement. Once good interfacial quality is confirmed, III-V/Si hybrid MOS optical modulator without parasitic capacitance can be fabricated and high-speed operation is expected.

2.4 Conclusion

In this chapter, the performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter was explored. Due to the similar refractive index of InGaAsP and Si, the peak of optical intensity centers in III-V/Si hybrid structure, while the free carriers accumulates on the MOS interfaces. By using InGaAsP and Si layers with same thickness, the peak of optical intensity can be aligned with accumulated free carriers, leading to improved overlap between optical mode and free carriers. Furthermore, by thinning the InGaAsP and Si layers used in the III-V/Si hybrid MOS optical phase shifter, the optical power intensifies in the center of III-V/Si hybrid structure, enhancing the interaction between optical mode and free carriers. The parasitic capacitances were removed for the realization of high-speed operation. Three methods were suggested to remove the parasitic capacitance step by step. By introducing an isolation trench on the one side of Si rib waveguide, 86% of parasitic capacitance was removed, which has been successfully demonstrated experimentally. To completely remove all the parasitic capacitance, a SiO_2 filling process followed by a CMP process has been proposed. It has been confirmed that the surface fluctuation caused by the CMP process has no significant influence on the

following wafer bonding process. The final demonstration of a high-efficiency and high-speed III-V/Si hybrid MOS optical modulator is expected in the near future.

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Chapter 3
EOT scaling of III-V/Si hybrid MOS capacitor

Optical phase shifter is an indispensable part for not only optical modulator but also for optical switch. However, they have distinct requirements for the phase shifter. For optical modulator, both high modulation efficiency and high modulation speed are essential figures of merit for practical usage. The currently deployed transceivers support 100 Gb/s operation using 4 × 25 Gb/s on-off keying (OOK) modulation format. The recent IEEE P802.3bs has selected the pulse amplitude modulation with four levels (PAM-4) as the modulation format for the next generation 400 Gb/s Ethernet, which means a maximum speed above 100 Gb/s per single wavelength is required for optical modulators [1, 2]. In contrast, the large bandwidth in optical switch is realized by high-port count, rather than fast operation. Usually, nano-second level reconfiguration time is sufficient for optical switch. For optical switch, high modulation efficiency, low insertion loss, low power consumption and high-port count are more critical figures of merit. In this chapter, the modulation efficiency of III-V/Si hybrid MOS optical phase shifter is improved via EOT scaling, which inevitably induces large capacitance and lower modulation bandwidth. This study is targeted for optical switch application that prefers high modulation efficiency over GHz operation.

3.1 Introduction

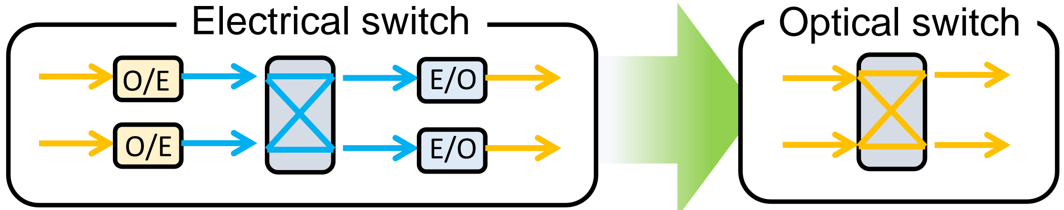


Fig. 3.1. Optical switch can remove O/E/O conversion.

As predicted by Cisco, the East-West Internet Protocol (IP) data traffic, which means the traffic within the dace center and traffic between data centers, will present 86 percent of the total traffic associated with data centers [3]. As the data traffic surging in data centers, the switching capacity of conventional electrical switches cannot scale up accordingly due to the limitations in power consumption and pin count [4, 5]. Optical switches are considered as a promising alternative because they promise lower power consumption by eliminating the optical/electrical/optical (O/E/O) conversion, as indicated by the Fig. 3.1, and larger bandwidth by eliminating the pin. Furthermore, as opposed to electrical switches, optical switches are inherently compatible to wavelength division multiplexing (WDM), which further extends modulation bandwidth, and reduces cost and system complexity [6].

As introduced in Chapter 1, Si photonics has been considered as a promising technology to realize high-speed and low-cost optical interconnection for short-reach distance. On Si photonic platform, the commonly used phase shifters for optical switch are based on thermo-optic effect and carrier injection through a p-i-n junction [7, 8]. However, both of them need milli-watt (mW) level power consumption, limiting their potential application in large-scale integrated case. As mentioned before, our III-V/Si hybrid MOS optical phase shifter has demonstrated extremely high modulation efficiency with low

absorption loss, making it very attractive for the application in optical switch. Because high modulation efficiency means low driving voltage and short device length, enabling high-density integration with low overall power consumption, while low absorption loss ensures low insertion loss and large crosstalk, which is also preferable for large-scale integration since the insertion loss and crosstalk will accumulate across layers of a switching fabric.

It is desirable for optical switches to have a high modulation efficiency, which means lower $V_{\pi}L$. The MOS-type optical phase shifter relies on a semiconductor-insulator-semiconductor capacitor to change carrier density and realize optical phase modulation [9], as shown in Fig. 3.2(a). The modulation efficiency of MOS-type optical phase shifter could be effectively improved by EOT scaling, as has been done in traditional CMOS devices for performance enhancement as the technology node advances [10, 11]. Generally speaking, the modulation efficiency is linearly proportional to the capacitance, which is determined by the EOT, as presented in Fig. 3.2(b). Even though an extremely high modulation efficiency with a $V_{\pi}L$ around 0.05 Vcm has already been demonstrated by the III-V/Si

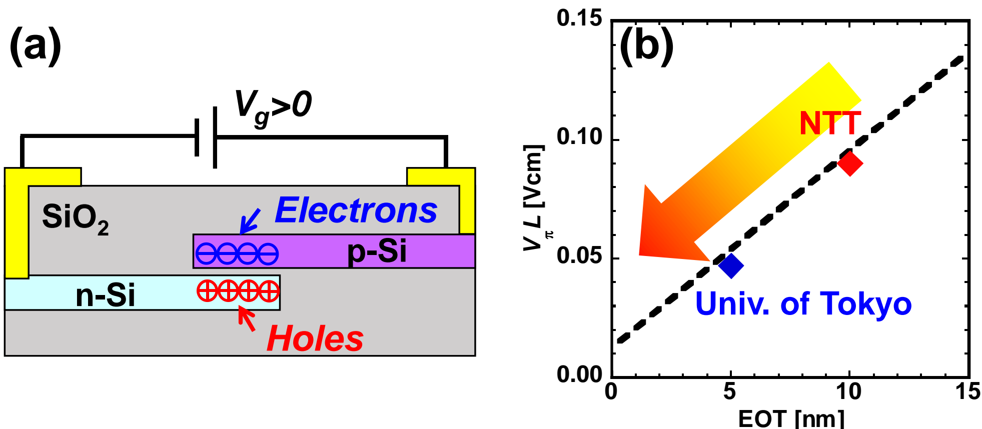


Fig. 3.2. (a) A cross-sectional schematic of a Si MOS-type optical phase shifter, and (b) the relationship between $V_{\pi}L$ and EOT values.

hybrid MOS optical phase shifter, there is still room to achieve higher modulation efficiency by using III-V/Si hybrid MOS capacitors with thinner EOT value. In this chapter, the EOT scaling of III-V/Si hybrid MOS capacitor using high-k material was investigated, which is useful to enhance the modulation efficiency of III-V/Si hybrid MOS optical phase shifter for optical switching application.

3.2 EOT scaling issue

In the previous demonstrations, Al_2O_3 is used as the bonding interface for III-V and Si wafer bonding because it provides large surface energy and strong bonding strength. By thinning the thickness of Al_2O_3 layer deposited, smaller EOT is expected. However, in our previous study, we found that the EOT stops scaling with the physical thickness of the Al_2O_3 layer and saturated above 5 nm [12]. It was suspected that the generation of nano-scale tiny voids on the bonding interface due to the degassing of water from Al_2O_3 layer

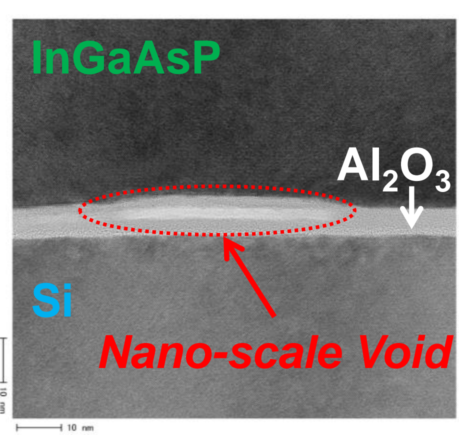
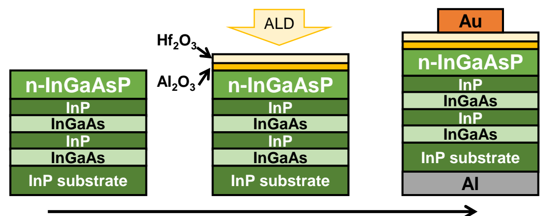


Fig. 3.3. A cross-sectional TEM image of a III-V/Si hybrid MOS capacitor with Al_2O_3 as bonding interface.

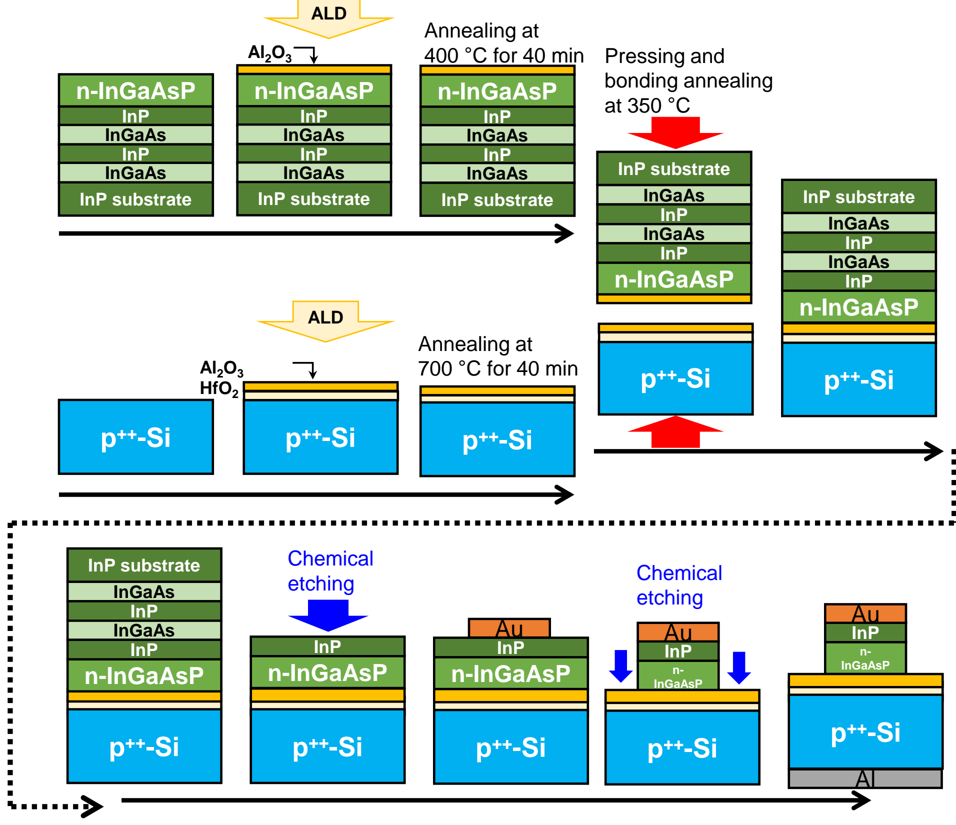
may be the reason. Figure 3.3 shows a TEM image of the wafer bonded III-V/Si hybrid MOS capacitor. A void is clearly shown in the bonding interface layer. In another study, it was confirmed that the introduction of HfO_2 into the bonding interfacial layers is effective to suppress the void generation on the bonding interface [13]. Another benefit we can take advantages of is that HfO_2 is a high-*k* material with a *k* value around 25 which is much larger than that of Al_2O_3 whose *k* value is around 9. In the following study, we have invested the effect of HfO_2/Al_2O_3 bonding stack to enhance the salability of the EOT of III-V/Si hybrid MOS capacitor.

3.3 Fabrication process of III-V MOS capacitor

Both conventional and wafer-bonded hybrid MOS capacitors were fabricated. Figure 3.4 shows the fabrication pross flows of a conventional metal/high-*k*/III-V MOS capacitor and a wafer-bonded III-V/high-*k*/Si MOS capacitor. For a conventional metal/high-k/III-V MOS capacitor, firstly, the III-V wafer was pre-cleaned using acetone, ammonium hydroxide and ammonium sulfide in sequence. Then, the HfO_2/Al_2O_3 high-*k* stack was deposited on the III-V wafer. Trimethylaluminium (TMA) and H_2O were used as the precursors of Al_2O_3, while tetrakis(ethylmethylamino)-hafnium (TEMAf) and H_2O were used as the precursors of HfO_2. Next, Au and Al pad was thermally evaporated on the front and back surface of the III-V wafer as front and back contact, respectively. For a wafer-bonded III-V/high-*k*/Si MOS capacitor, the III-V and Si wafers were firstly precleaned separately. The Si wafer is heavily doped with an acceptor concentration over 1×10^{20} cm^{-3} so as to act as a gate electrode. Al_2O_3 layer was deposited on the III-V wafer, while Al_2O_3 and HfO_2 layers were deposited on the Si wafer in sequence. Then, the III-V and Si wafer



(a) Conventional Metal/high-k/III-V MOS capacitor



(b) Wafer bonded III-V/high-k/Si MOS capacitor

Fig. 3.4. The fabrication process flow of (a) a conventional metal/high-*k*/III-V MOS capacitor and (b) a wafer-bonded III-V/high-k/Si MOS capacitor.

were annealed at 400 °C and 700 °C, respectively, for 40 min. This step is before the wafer bonding process and thus called pre-bonding annealing. The purpose of pre-bonding annealing is to remove the H_2O inside the high-k dielectric layers as much as possible to suppress the void generation on the bonding interface. Then, after being cleaned using DI-

water with megasonic, the III-V and Si wafers were firstly bonded manually and then pressed with 500 N pressure in conjunction with 350-℃ annealing for 1 hour. After the wafers were successfully bonded together, the InP substrate and three etch-stop layers were removed by selective chemical etching. The thickness of remaining III-V layers is 220 nm to accommodate the depletion width. Next, Au was evaporated on the III-V layer surface through a hard mask. III-V mesas were formed by selective chemical etching to electrically isolate capacitors with each other. Finally, Al was evaporated on the Si surface to form back contact.

3.4 *C-V* curves of III-V MOS capacitors

Firstly, two III-V MOS capacitors, a conventional Au/HfO_2/Al_2O_3/III-V MOS capacitor and a wafer-bonded Au/III-V/ HfO_2/Al_2O_3/Si MOS capacitor, were fabricated and compared. Table 1 sows the thickness of HfO_2 and Al_2O_3 layers used in these two capacitors.

Table 1. The thickness of high-k dielectric layers used in the capacitors

	k	Conventional	Wafer-bonded
Al_2O_3	~9	7.0 nm	5.3 nm
HfO_2	~25	3.5 nm	4.0 nm

From Table 1, the HfO_2 thickness in the conventional and wafer-bonded MOS capacitors are similar. However, the Al_2O_3 thickness in the conventional MOS capacitor is 1.7 nm thicker than that of the wafer-bonded MOS capacitor. Considering that the k value

of HfO_2 is much larger than that of Al_2O_3, the EOT of conventional MOS capacitor is expected to be larger than that of wafer bonded MOS capacitor. For the conventional MOS capacitor, the EOT calculated from the physical thickness and dielectric constant k, is 3.6 nm.

Figure 3.5 (a) and (b) shows the C-V curves of a conventional Au/HfO_2/Al_2O_3/III-V MOS capacitor and a wafer-bonded Au/III-V/HfO_2/Al_2O_3/Si MOS capacitor, respectively. We characterized the capacitance equivalent oxide thickness (CET) from the measured oxide capacitance at 1 MHz and 2-V bias. The unsaturated capacitance in the accumulation region was due to leakage current. The difference between CET and EOT is negligible when CET is larger than 3 nm. From Fig. 3.8(a), the CET of the conventional capacitor is 3.7 nm, which is very close to the value calculated from the physical thickness and dielectric constant. The *C-V* curve shown in Fig. 3.8(b) indicates a CET of 5.4 nm, which is much thicker than that of the conventional capacitor. Therefore, it is confirmed that the wafer bonding process tends to enlarge the CET of the hybrid MOS capacitor. It is worth

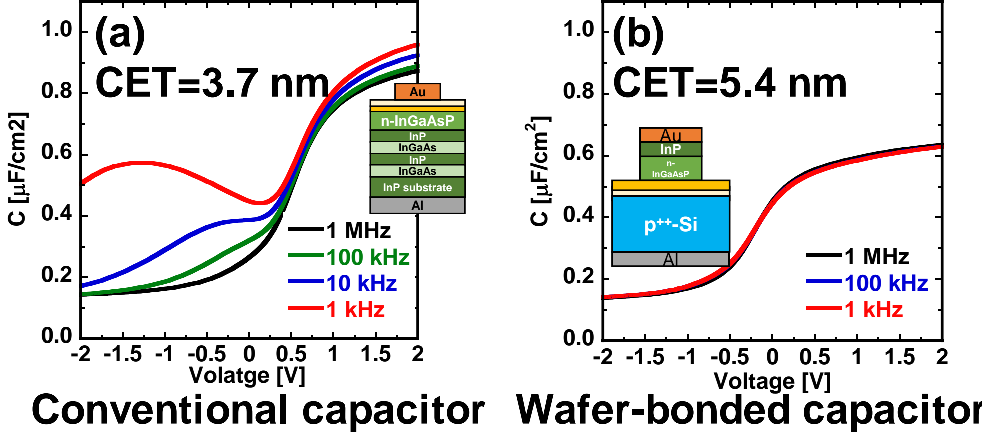


Fig. 3.5. *C-V* curves of (a) a conventional Au/HfO_2/Al_2O_3/III-V MOS capacitor and (b) a wafer-bonded Au/III-V/ HfO_2/Al_2O_3/Si MOS capacitor.

noting that, compared with the wafer-bonded MOS capacitor, the conventional MOS capacitor has large frequency dispersion in both accumulation region and depletion region, indicating large density of border trap and interface state. We suspect that, while the post-bonding annealing process enhances the bonding strength, it also improved the interfacial quality as commonly practiced in III-V MOS capacitors [14, 15].

Table 2. The thickness of high-*k* dielectric layers used in the capacitors

	p^+-Si		n-III-V
Material	**HfO_2**	**Al_2O_3**	**Al_2O_3**
(a)	**2.6 nm**	**1.3 nm**	**1.5 nm**
(b)	**2.0 nm**	**1.3 nm**	**1.5 nm**
(c)	**2.6 nm**	**1.3 nm**	**1.1 nm**

In order to realize a EOT below 5 nm, three wafer-bonded Au/III-V/HfO_2/Al_2O_3/Si MOS capacitors (sample (a)~(c)) were fabricated. Table 2 shows the thickness of HfO_2 and Al_2O_3 layers of each sample. Figure 3.9(a) to (c) shows the corresponding *C-V* curves of sample (a) to (c). For sample (a), a CET of 4 nm was successfully achieved by using 2.6-nm HfO_2 and 2.8-nm Al_2O_3 layer as bonding interface. In sample (b), only the thickness of HfO_2 layer was reduced to 2.0 nm aiming to further reduce the achievable CET. However, the obtained CET is still 4.0 nm. Since the thickness of HfO_2 and Al_2O_3 layer is similar, the CET is dominated by the thickness of Al_2O_3 because the dielectric constant of Al_2O_3 is much smaller than that of HfO_2. In sample (c), compared with sample (a), the thickness of Al_2O_3 layer deposited on the III-V wafer was reduced by 0.4 nm with other layer unchanged. The CET was reduced to 3.5 nm accordingly. Therefore, thinning the Al_2O_3 layer is

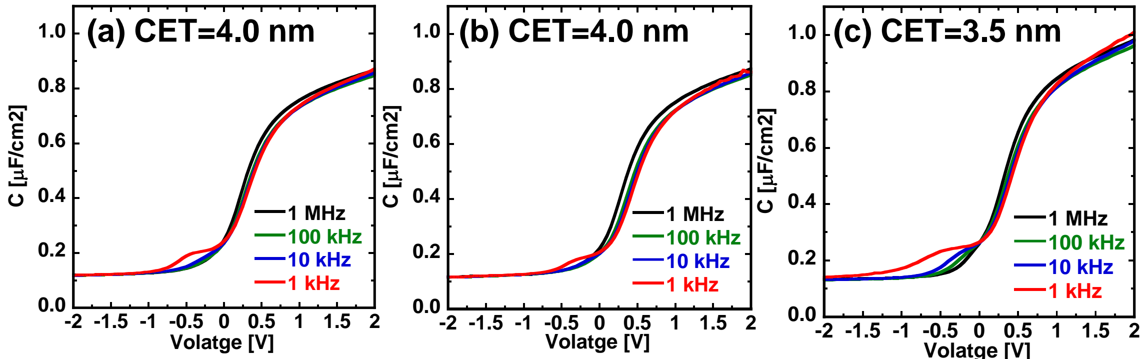


Fig. 3.9. The *C-V* curves of wafer-bonded Au/III-V/HfO_2/Al_2O_3/Si MOS capacitors with different high-k dielectric thickness.

effective to scale down the CET of Au/III-V/HfO_2/Al_2O_3/Si MOS capacitor. Even smaller CET is possible by continually thinning the Al_2O_3 layer as long as the dielectric layer stack is thick enough to suppress the leakage current and ensure strong bonding strength.

Figure 3.10 presents the relationship between gate leakage current density and the CET of wafer-bonded Au/III-V/HfO_2/Al_2O_3/Si MOS capacitors. For the capacitor with 3.5-nm CET, the gate leakage current density is 1.36×10^{-4}A/cm^2 at V_g=V_{fb}+ 1 V (V_{fb}: flat-band

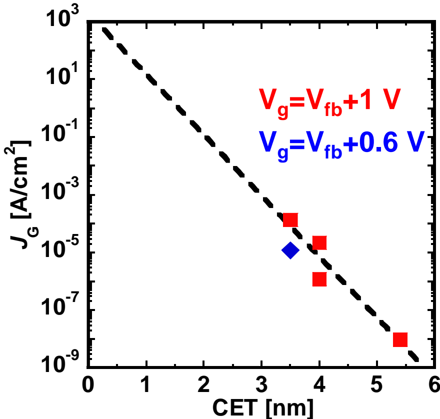


Fig. 3.10. The relationship between gate leakage current density and the CET of wafer-bonded Au/III-V/HfO_2/Al_2O_3/Si MOS capacitors.

voltage). As discussed above, the scaling down of CET will enhance the modulation efficiency of III-V/Si hybrid MOS optical phase shifter, which enables smaller driving voltage and smaller leakage current density. For instance, the leakage current density is 1.19×10^{-5}A/cm^2 at V_g=V_{fb} + 0.6 V, which is one order of magnitude smaller than the case with 1-V driving voltage.

3.5 Simulation study of the effect of EOT scaling

We investigated the effect of the EOT scaling demonstrated in the last section through numerical simulations. The simulation method is exactly same with that used in Chapter 2.

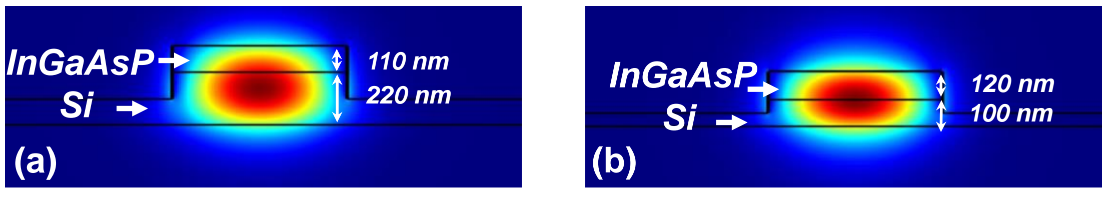


Fig. 3.11. The TE fundamental mode of III-V/Si hybrid MOS optical phase shifter with varying thickness of InGaAsP and Si layer.

Figure 3.11 shows the TE fundamental mode of III-V/Si hybrid MOS optical phase shifter with different structures. In Fig. 3.11(a), the thickness of InGaAsP and Si layer is 110 nm and 220 nm, respectively, while in Fig. 3.11(b), the thickness of InGaAsP and Si layer is 120 nm and 100 nm, respectively. The structure in Fig. 3.11(a) corresponds to the design demonstrated in [16], and the structure in Fig. 3.11(b) is the optimized design presented in Chapter 2.2. The length of the phase shifter is assumed to be 500 μm.

Figure 3.12 shows the relationship between $V_\pi L$ and EOT values. For both structures in Fig. 3.11, the $V_\pi L$ is linearly proportional to the EOT value. Compared with the

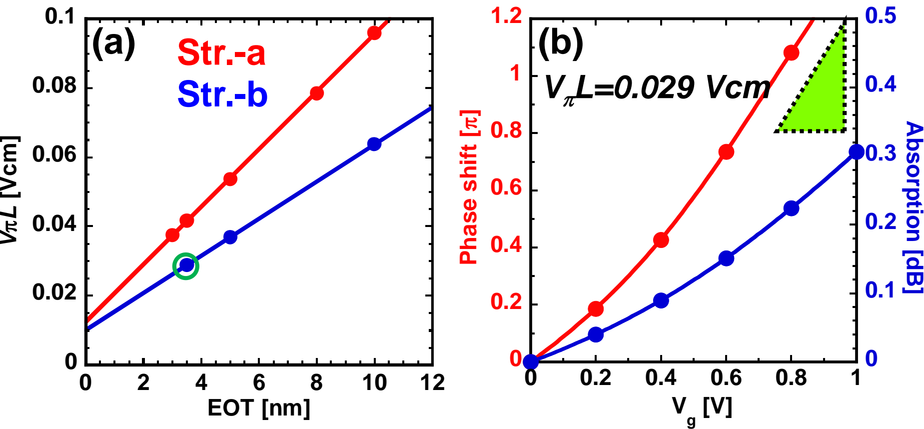


Fig. 3.12. (a) the relationship between $V_\pi L$ and EOT value, and (b) the phase shift (red) and absorption (blue) as a function of gate voltage.

unoptimized structure, the optimized case showed smaller $V_\pi L$ due to the improved overlap between optical mode and accumulated electrons, which agrees well with the conclusion in Chapter 2.2. With a 3.5-nm EOT, the III-V/Si hybrid MOS optical phase shifter with optimized structure demonstrated a $V_\pi L$ of 0.029 Vcm, as indicated by the green circle in Fig. 3.12(a). Figure 3.12(b) shows the performance of the III-V/Si hybrid MOS optical phase shifter with optimized structure and 3.5-nm EOT. From the slope of phase shift induced by the V_g, the modulation efficiency is extracted as 0.029 Vcm. The absorption at π phase shift is 0.21 dB, owing to the small absorption in InGaAsP layer.

In the future, the EOT scaling should be continued firstly by thinning the HfO_2 and Al_2O_3 layer until they are too thin to suppress large leakage current or to ensure reliable wafer bonding. For instance, a 1.08-nm CET Au/HfO_2 (2 nm)/Al_2O_3 (0.2 nm)/InGaAs capacitor has been demonstrated in the other study [17]. Utilizing other high-*k* material is another promising choice. For instance, ZrO2 features a high dielectric constant of 35~53 [18, 19]. In a recent study, a 1-nm CET has been achieved by using ZrO_2/Al_2O_3 stack on

InGaAs MOS capacitor [20]. In sum, 1-nm CET for III-V/Si hybrid MOS optical phase shifter is achievable given proper thickness reduction in bonding interface or choice of suitable high-*k* material.

3.6 Conclusion

EOT scaling is an effective way to enhance the modulation efficiency of III-V/Si hybrid MOS optical phase shifter. However, it is difficult to scale down the EOT of III-V/Si hybrid MOS capacitor to below 5 nm using only Al_2O_3 as bonding interface due to the generation of nano-sacle voids. On the other hand, HfO_2 can suppress the void generation on the bonding interface. Moreover, its high dielectric constant also enables effective EOT scaling. In this chapter, conventional III-V MOS capacitor and wafer-bonded hybrid III-V capacitor were fabricated and compared. Compared with the conventional III-V MOS capacitor, the wafer-bonded hybrid MOS capacitor tends to have larger CET. By thinning both the HfO_2 and Al_2O_3 layer thickness, a small CET of 3.5 nm was successfully demonstrated. Simulation study predicted that, with a 3.5-nm CET, a low $V_{\pi}L$ of 0.029 Vcm is expected.

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Chapter 4

2×2 Si Mach–Zehnder interferometer optical switch based on III-V/Si hybrid MOS phase shifter

In the previous study, we have successfully demonstrated a MZI optical modulator based on III-V/Si hybrid MOS optical phase shifter. The high efficiency and low absorption loss make the III-V/Si hybrid MOS optical phase shifter also suitable for optical switching, which has not been demonstrated yet. In this chapter, the dependence of switching crosstalk on the absorption loss induced by phase shifter was analyzed. By using III-V/Si hybrid MOS optical phase shifter, a low crosstalk of -38 dB was predicted. Next a 2×2 Si MZI optical switch with III-V/Si hybrid MOS optical phase shifter was demonstrated with ultra-low power consumption and high switching speed.

4.1 Introduction

Recent years have witnessed the dramatic explosion of global internet data traffic, particularly driven by the rapid growth of cloud services, resulting in the need for a higher bandwidth and data rate in optical networks for hyperscale data centers [1, 2]. Silicon (Si) photonics is a competitive technology for realizing short-reach optical interconnects to deliver high data rates beyond 100 Gb/s [3-5]. Optical switches are expected to be critical components for optical network systems because they enable optical path routing in space [6-8]. A Si photonic integrated circuit (PIC) integrated with numerous optical switches can

also be used for quantum computing [9, 10], deep learning [11] and data communication [12, 13]. Si optical switches based on the thermo-optic (TO) effect, the free-carrier plasma dispersion effect, and micro-electro-mechanical-systems (MEMS) technology have been well developed in recent years. MEMS optical switch fabrics have high port counts but are limited by their microsecond switching time [14-16]. TO switches have low crosstalk but require milliwatt-level power consumption [17, 18]. Their slow switching speed may limit applications. Optical switches with p-i-n junctions utilize the carrier-induced refractive index change and are capable of nanosecond switching. However, they require milliwatt power consumption [19-22]. In addition, the coexisting free-carrier absorption effect causes a severe optical power imbalance between Mach–Zehnder interferometer (MZI) arms [23], degrading the crosstalk.

In our previous study, we have demonstrated that a III-V/Si hybrid metal-oxide-semiconductor (MOS) phase shifter enables efficient optical phase modulation with low optical absorption loss [24, 25]. An optical modulator based on the III-V/Si hybrid MOS phase shifter exhibited a modulation efficiency of 0.047 Vcm and low optical attenuation of 0.23 dB at π phase shift owing to the large electron-induced refractive index change in InGaAsP. In this paper, we present a 2×2 Si MZI optical switch with III-V/Si hybrid MOS phase shifters. The power consumption was suppressed to below 1 nW owing to the negligible leakage current of the hybrid MOS capacitor. Broadband and symmetric optical switching characteristics were obtained with an extinction ratio of less than -23 dB. A high switching speed of below 20 ns was also achieved.

4.2 Dependence of switching crosstalk on the absorption loss

For optical switching applications, especially large-scale integrated optical switching fabrics, low crosstalk is a desired property, because the crosstalk will accumulate stage by stage when the optical signal travels along the switching fabrics.

To evaluate the crosstalk, we numerically analyzed the switching characteristics of MZI optical switch by using the transfer matrix method. The transfer matrix of a 3-dB coupler is given by

$$C = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} \quad (1)$$

The transfer matrix of the phase shifter can be expressed by

$$P = \begin{bmatrix} 1 & 0 \\ 0 & e^{-j\Delta\beta_1 L} \end{bmatrix} \quad (2)$$

with $\Delta\beta_1$ being the change in the propagation constant of one of the phase shifters, and L being the length of the phase shifter. The change of propagation constant is

$$\Delta\beta_1 = \frac{2\pi}{\lambda}\Delta n - j\frac{\Delta\alpha}{2} \quad (3)$$

where Δn and $\Delta\alpha$ are the change in effective refractive index and absorption coefficient induced by the accumulated carriers, respectively. The total transfer matrix of the MZI optical switch is

$$T = CPC = \frac{1}{2}\begin{bmatrix} 1 - e^{-j\Delta\beta_1 L} & j\left(1 + e^{-j\Delta\beta_1 L}\right) \\ j\left(1 + e^{-j\Delta\beta_1 L}\right) & -1 + e^{-j\Delta\beta_1 L} \end{bmatrix} \quad (4)$$

We first numerically estimated the electron-induced effects in InGaAsP. Figure 4.1 exhibits the relationship between the electron-induced changes in refractive index and absorption coefficient in Si and InGaAsP. Since InGaAsP has significantly greater refractive index change than Si, for the same change of refractive index, the increase in

absorption coefficient in InGaAsP is 10~30 times smaller than that in Si.

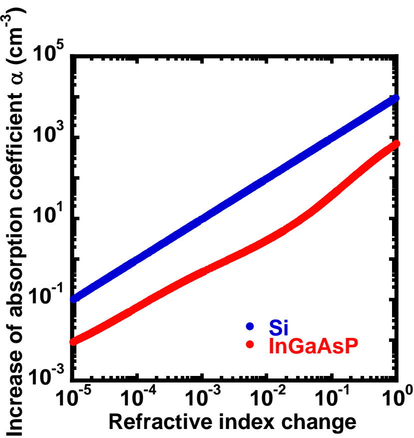

Fig. 4.1. Relationship between the changes in refractive index and absorption coefficient in Si and InGaAsP.

Figure 4.2 illustrates the relationship between the carrier-induced absorption loss at π phase shift and the minimal achievable crosstalk obtained by using the transfer matrix. It is apparent that the minimal achievable crosstalk is limited by the carrier-induced absorption loss, because it causes the optical power imbalance between the two arms of the MZI. For the Si phase shifter based on a Si MOS structure demonstrated by CISCO [26], a loss of 2.4 dB was reported at π phase shift, which means the crosstalk will be limited above -20 dB. In comparison, the ultra-low carrier-induced absorption loss of 0.23 dB at π phase shift is expected in the InGaAsP/Si hybrid MOS optical phase shifter when the phase shifter length is assumed to be 500 μm, enabling a crosstalk of -37.6 dB.

The switching characteristics of the MZI optical switch based on the InGaAsP/Si hybrid MOS optical phase shifter is plotted in Fig. 4.3. The EOT of the gate oxide was assumed to be 5 nm. By applying the gate voltage, the accumulated electrons at the InGaAsP MOS interface induces the large change in the refractive index, resulting in

switching from the cross state to the bar state. The switching voltage was predicted to be 0.86 V. Since the gate leakage current is negligible, the switching power could be dramatically reduced as compared with a thermo-optic switch.

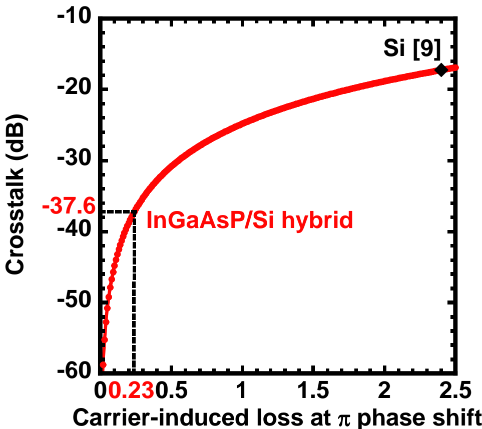

Fig. 4.2. Relationship between the carrier-induced absorption loss at π phase shift and the crosstalk of the optical switch.

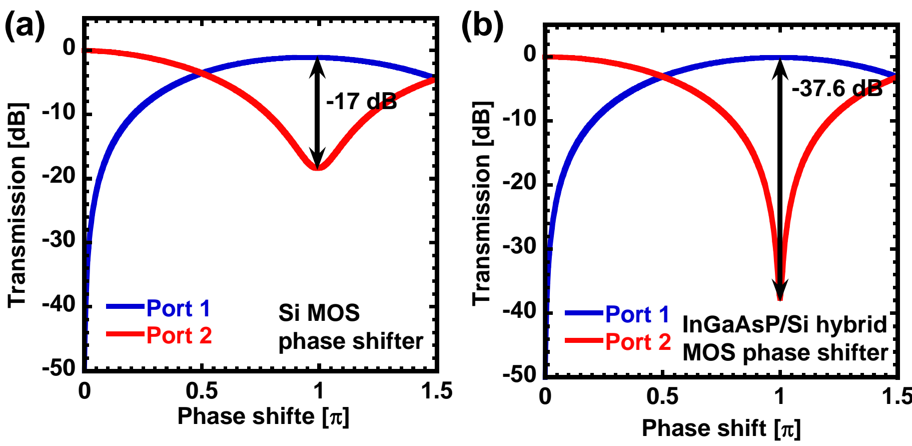

Fig. 4.3. The switching characteristics of a MZI optical switch based on (a) Si MOS optical phase shifter and (b) III-V/Si hybrid MOS optical phase shifter.

4.2 Design of the 2×2 Si MZI optical switch

A schematic of the 2×2 Si MZI optical switch with III-V/Si hybrid MOS phase shifters is shown in Fig. 4.4(a). The optical switch consists of two 2×2 multimode interferometer (MMI) couplers based on Si rib waveguides and two III-V/Si hybrid MOS phase shifters. Figure 4.4(b) shows a cross-sectional schematic of the phase shifter, in which an n-type III-V layer is bonded on a p-type Si waveguide with a 5-nm-thick Al2O3 layer as the bonding interface. We use a III-V membrane consisting of a 110-nm-thick InGaAsP layer and a 50-nm-thick InP etch-stop layer. The bandgap wavelength of InGaAsP lattice-matched to InP is designed to be 1.37 μm to maximize the electron-induced refractive index change while avoiding optical absorption of the propagating optical mode at a 1.55 μm wavelength [25]. The thin III-V membrane allows us to use a standard Si-on-insulator (SOI) wafer with a 220-nm-thick Si layer. The width of the Si rib waveguide in the phase

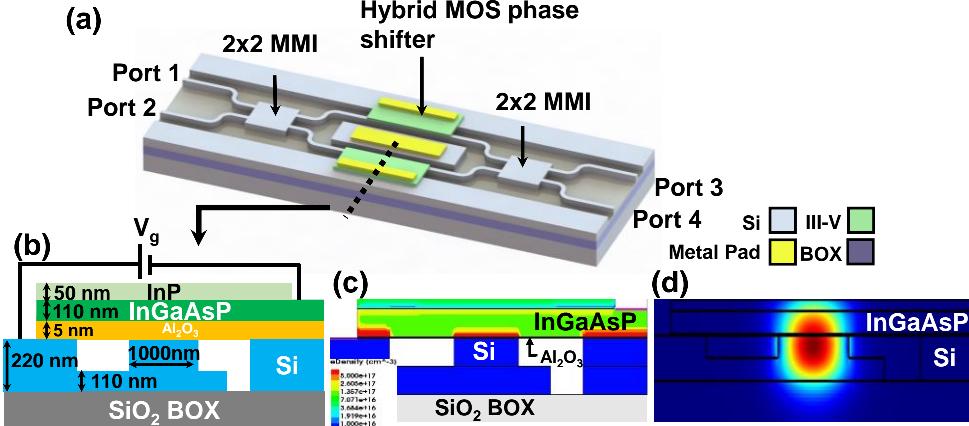

Fig. 4.4. (a) Schematic of 2×2 Si optical switch with III-V/Si hybrid MOS phase shifters. (b) Schematic cross-section of III-V/Si hybrid MOS phase shifter. (c) Electron distribution in the accumulation state with V_g of 1.6 V. (d) Fundamental TE optical mode of III-V/Si hybrid MOS phase shifter.

shifter region is designed to be 1000 nm to achieve a large fabrication tolerance, although a narrower single-mode Si waveguide, which is used in the passive region, may be adopted. An isolation trench is introduced on one side of the Si rib waveguide to electrically isolate the parasitic capacitance between the III-V contact and Si terrace. The free-carrier distribution under a bias voltage was simulated using Sentaurus TCAD tools. When a positive gate voltage (V_g) is applied between the Si and III-V layers, electrons accumulate at the III-V MOS interface as shown in Fig. 4.4(c), modulating the local refractive index and thus the phase of the fundamental transverse electric (TE) optical mode at a wavelength of 1.55 μm, as shown in Fig. 4.4(d) which was obtained by Lumerical MODE Solution.

To obtain a broadband switching characteristic, we designed a 3-dB 2×2 MMI coupler with tapered input and output ports [26, 27]. Figure 4.5(a) shows the layout structure of the MMI coupler. The width and height of the Si rib waveguide are 0.55 μm and 0.22 μm, respectively. The etching depth of the Si rib is assumed to be 0.11 μm. By three-

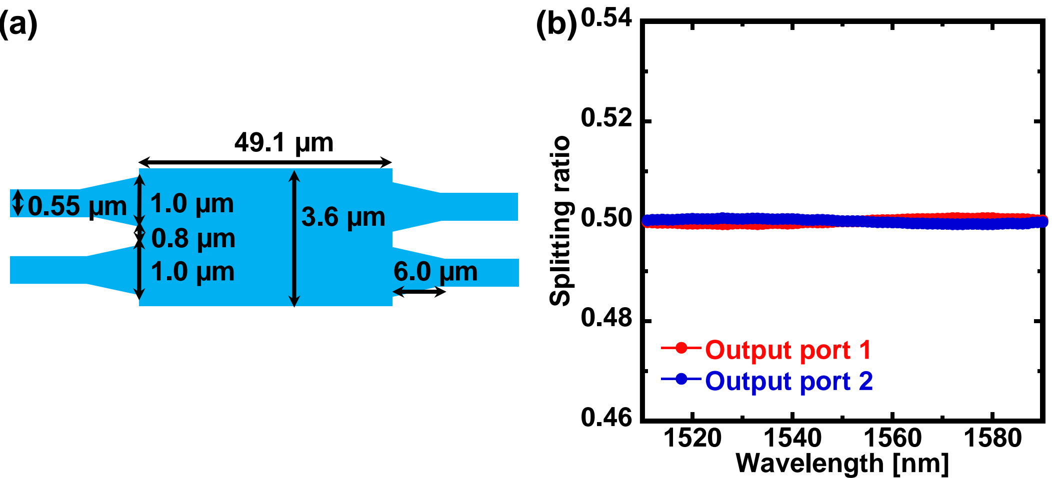

Fig. 4.5. (a) Layout and (b) simulated splitting ratio of 3-dB 2×2 MMI coupler with tapered input and output ports based on Si rib waveguides.

dimensional (3D) finite-difference time-domain (FDTD) simulation using Lumerical FDTD Solutions, the width and length of the MMI coupler are designed to be 3.6 μm and 49.1 μm, respectively. The linear tapers in the input and output waveguides of the MMI coupler contribute to the broadband transmission and low insertion loss. The taper width and length are 1.0 μm and 6.0 μm, respectively. Figure 4.5(b) shows the splitting ratio of a 2×2 MMI coupler calculated by 3D-FDTD simulation. The splitting ratio of the 2×2 MMI coupler is defined as $P_{out1\ or\ 2}/P_{in}$, where $P_{out\ 1\ or\ 2}$ is the output power from either one of the output ports and Pin is the input power into one of the input ports. The optimized 2×2 MMI coupler exhibited an almost constant splitting ratio of 0.5 from 1510 nm to 1590 nm, in which transmission spectra, the transmission difference between the two output ports was below 0.1 dB.

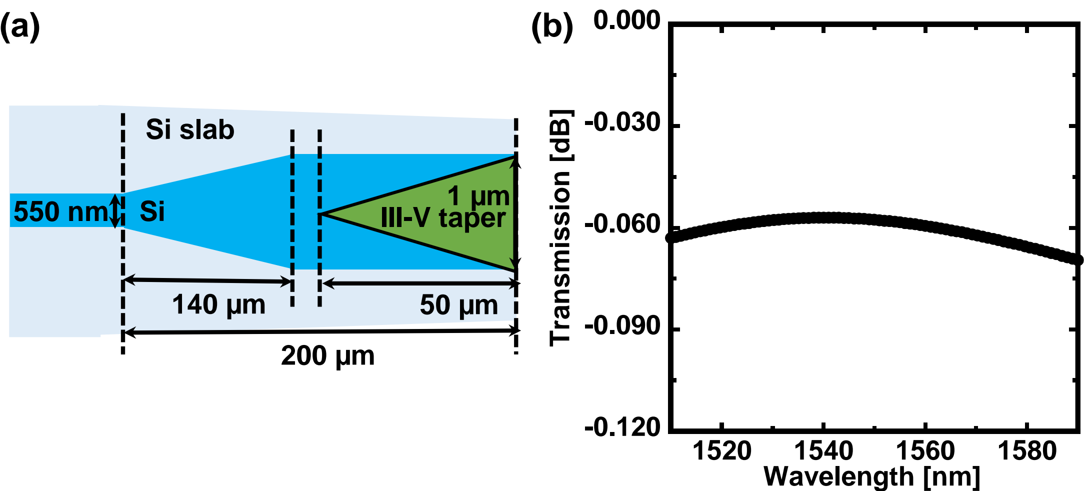

Fig. 4.6. Layout of Si and III-V tapers between Si waveguide and III-V/Si hybrid MOS phase shifter.

A double-layer taper design was also employed to ensure a smooth optical mode transition between the Si rib waveguide and III-V/Si hybrid MOS phase shifter, as shown

in Fig. 4.6. The taper consists of a 140-µm-long silicon taper and a 50-µm-long III-V taper. The transmission of the hybrid taper is defined as P_{PS}/P_{Si}, where P_{PS} and P_{Si} are the power of the fundamental optical modes in III-V/Si hybrid phase shifter and Si single-mode waveguide, respectively. A 3D-FDTD simulation shows a low insertion loss of below 0.07 dB from 1510 nm to 1590 nm.

4.3 Fabrication of the 2×2 Si MZI optical switch

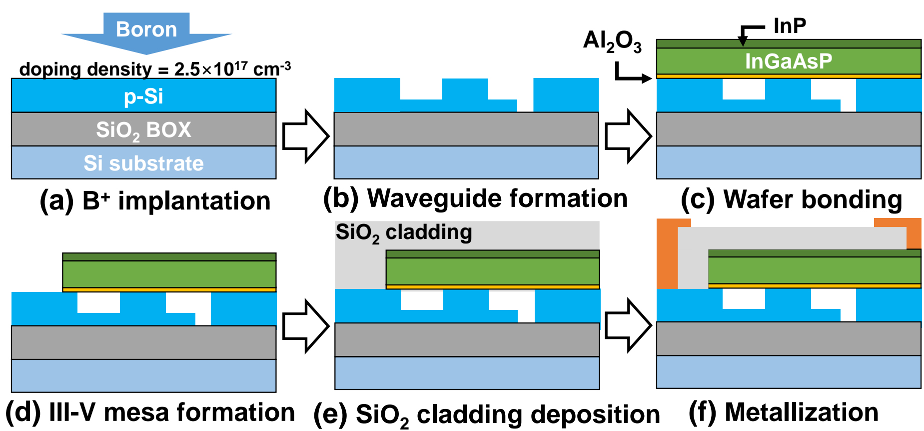

Fig. 4.7. Fabrication procedure of the 2×2 Si MZI optical switch with III-V/Si hybrid MOS phase shifters.

The fabrication procedure of the 2×2 Si MZI optical switch with the III-V/Si hybrid MOS phase shifters is shown in Fig. 4.4. The procedure started with boron (B) implantation of an SOI wafer with a 220-nm-thick Si layer and a 2-µm-thick SiO_2 buried oxide (BOX) layer, as shown in Fig. 4.7(a). The implantation dose and energy were 1×10^{13} cm^{-2} and 25 keV, respectively. After activation annealing, the resistivity was 0.11 Ωcm, indicating a hole density of 2.5×10^{17} cm^{-3}. As depicted in Fig. 4.7(b), the Si passive photonic

components were defined by electron-beam (EB) lithography and inductively coupled plasma (ICP) etching. A fully etched trench was introduced on one side of the Si rib waveguide in the phase shifter region to electrically isolate the parasitic capacitance. Then, Al_2O_3 was deposited on Si and InP wafers by atomic layer deposition (ALD). Pre-bonding annealing was then carrier out on Si and InP wafers at 700 °C and 400 °C, respectively, for 40 min in order to reduce the voids generated by the degassing of water from Al_2O_3 layer during wafer bonding [28]. The reason for annealing InP wafer at 400 °C is to avoid the thermal degradation of III-V material property. Next, both wafers were cleaned using ultrasonic water and bonded with 500 N pressure at 300 °C for 1 h, as illustrated in Fig. 4.7(c). The InP substrate was firstly removed by HCl. The etch-stop layers (InGaAs/InP/InGaAs) were chemically removed by wet etching in sequence at room temperature. The InGaAs layer was etched using H_3PO_4:H_2O_2:H_2O=1:1:7, while the InP layer was etched using HCl:H_3PO_4 =1:4. The 50-nm-thick InP layer on top of InGaAsP layer can protect InGaAsP from being chemically etched. The doping concentrations of the n-type InGaAsP and InP layers were approximately 1×10^{17} cm^{-3} and their thickness were 110 nm and 50 nm, respectively. A III-V mesa was formed by EB lithography and reactive ion etching (RIE). Then, a 250-nm-thick SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) as a cladding layer, as portrayed in Figs. 4.5(d) and 4.7(e). After contact via formation, a Ni/Ti/Pt metal stack was sputtered and Al was thermally evaporated on the device. Finally, as shown in Fig. 4.7(f), the metal stack was lifted off to form contact pads.

Figure 4.8(a) presents a plan-view microscope image of the fabricated optical switch. The length of the phase shifter was 500 μm. The III-V taper on top of the Si waveguide is clearly shown in the scanning electron microscope (SEM) image in Fig. 4.8(b). A cross-

sectional transmission electron microscope (TEM) image is shown in Fig. 4.8(c). Both the III-V membrane bonded on the Si rib waveguide and the isolation trench can be clearly observed.

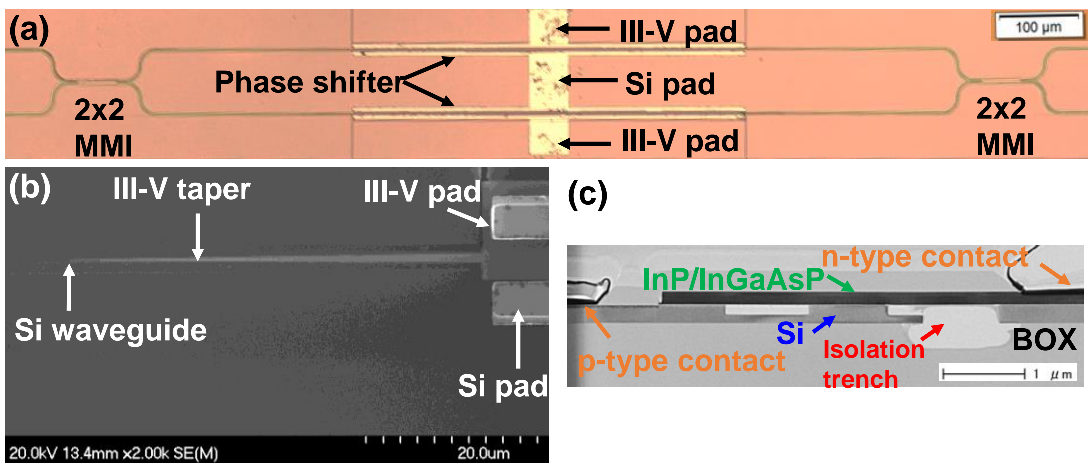

Fig. 4.8. (a) Plan-view microscope image of 2×2 Si MZI optical switch, (b) SEM image of III-V taper on top of Si waveguide, and (c) cross-sectional TEM image of III-V/Si hybrid MOS phase shifter.

4.4 Characterization of the 2×2 Si MZI optical switch

The *C-V* property of the III-V/Si hybrid MOS phase shifter measured at 1 MHz is shown in Fig. 4.9. When the gate voltage V_g was applied between the Si and III-V layers, as shown in Fig. 4.4(b), and swept from -2 to 2 V, the capacitance increased owing to the transition from carrier depletion to accumulation in the MOS capacitor. The capacitance in the accumulation state was approximately 3.2 pF. The distribution of the capacitances is shown in the inset. By introducing the electrical isolation trench on one side of the Si rib

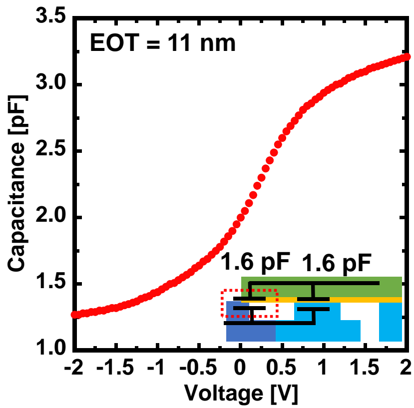

Fig. 4.9. C-V curve of III-V/Si hybrid MOS phase shifter.

waveguide, the parasitic capacitance under the III-V contact was completely removed.

From the C-V measurement, the EOT of the gate oxide was estimated to be approximately 11 nm. Compared with our previous design [25], the parasitic capacitance was reduced by 86%. The elimination of parasitic capacitance has no effect on the modulation efficiency since it has no overlap with the optical mode. The remaining parasitic capacitance of 1.6 pF (red dot box in the inset of Fig. 4.9) is due to the partial overlay of III-V layer anchored on the left terrace of the Si rib waveguide. It can be eliminated by proton implantation into the overlapped III-V layer or by filling the void above the half-etched Si with SiO_2 and terminating the III-V layer on it.

To evaluate the phase modulation efficiency of the phase shifter, an asymmetric MZI with a 500-µm-long III-V/Si hybrid MOS phase shifter was measured at the C-band. The input light from a Santec TSL-510 tunable laser source was coupled to the cleaved input waveguide through a lens fiber. The polarization of the input light was adjusted to the TE mode of the Si waveguide. The output signal was coupled again into a single-mode fiber by an objective lens. The output power was evaluated by an Agilent 81618A InGaAs power

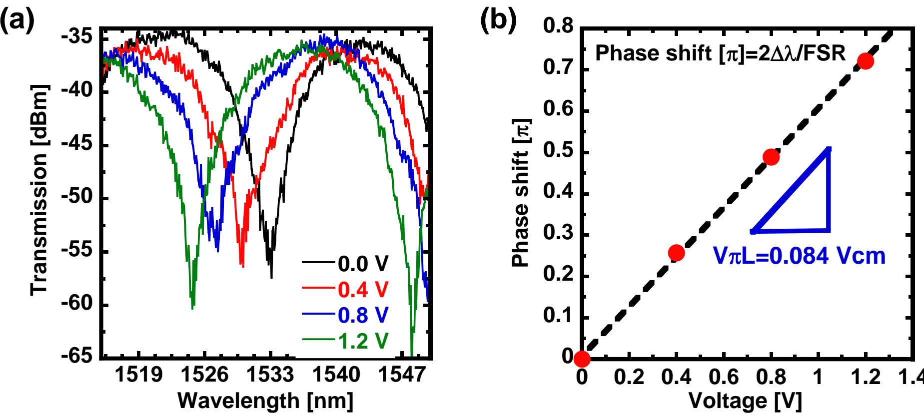

Fig. 4.10. Transmission spectra of asymmetric MZI at different V_g, and (b) phase shift as a function of V_g.

meter.

Figure 4.10(a) shows the transmission spectra for various V_g. The transmission spectrum subjected to periodic interference was shifted by applying V_g owing to the electron-induced change in the refractive index of InGaAsP. The phase shift was calculated from the wavelength shift associated with V_g and the free spectral range (FSR) and is shown in Fig. 4.10(b). The modulation efficiency ($V_\pi L$) was 0.084 Vcm which was extracted from the gradient in Fig. 4.10(b). Compared with previous result [25], the increase in $V_\pi L$ was due to comparatively higher EOT value.

The measured switching characteristics of the 2×2 Si MZI optical switch at a wavelength of 1527 nm are shown in Fig. 4.8(a). Owing to the unavoidable initial phase error induced by imperfect fabrication, the 2×2 Si MZI optical switch was not in the cross state at V_g of 0 V. Therefore, the initial phase error was compensated by applying V_g to the upper MZI arm. It can be seen in Fig. 4.11(a) that the input light from port 1 was switched from port 4 (cross port) to port 3 (bar port). We obtained a similar switching characteristic

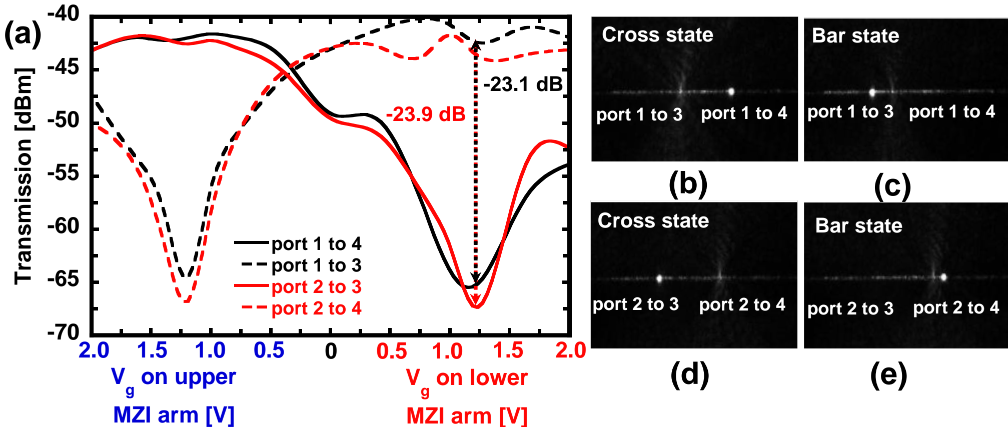

Fig. 4.11. Switching characteristics of 2×2 Si MZI optical switch with III-V/Si hybrid MOS phase shifters. (b) to (e) IR camera images of output ports in cross and bar states when the optical signal is injected to port 1 or port 2.

when the optical signal was injected to port 2. Thus, we successfully obtained 2×2 optical switching. The crosstalk in the bar state was smaller than -23 dB. The switching between the cross and bar states was also clearly observed in the infrared (IR) camera images of the output ports in Figs. 11(b) to 11(e).

The measured transmission spectra of the 2×2 Si MZI optical switch in the cross and bar states with light input from Port 1 and Port 2 are shown in Figs. 4.12(a) and 4.12(b), respectively. Owing to the almost constant splitting ratio of 0.5 of the MMI coupler from 1510 nm to 1590 nm wavelength, as discussed for Fig. 4.5(b), broadband switching was obtained. Although fluctuations due to the imperfect fabrication were observed in the transmission spectra, more uniform switching can be obtained by improving the fabrication procedure.

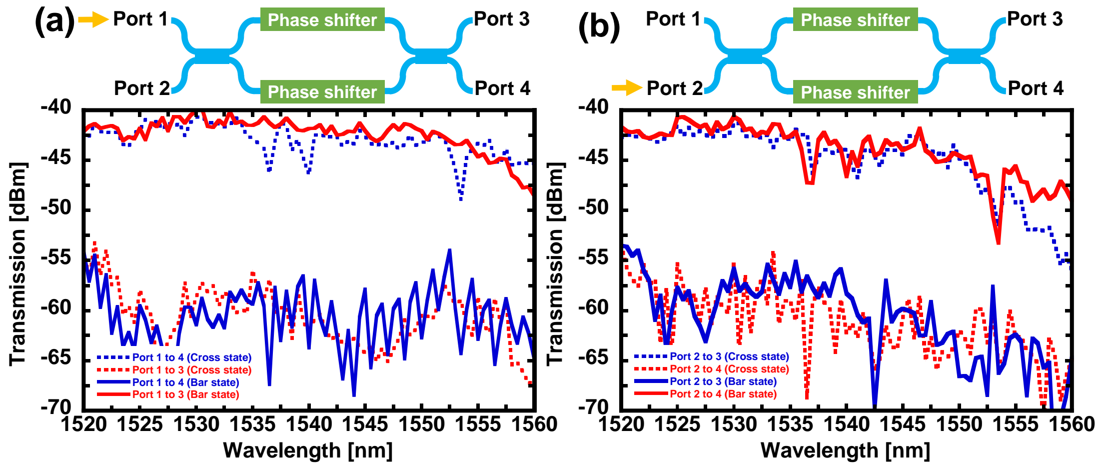

Fig. 4.12. Measured transmission spectra of 2×2 Si MZI optical switch in the cross and bar states with the optical signal input from (a) port 1 and (b) port 2.

Unlike optical modulators where high-speed modulation is necessary, optical switch need to hold one switching state for a long time. Hence, the static power consumption is very critical. The static power consumption of the optical switch is dominated by the gate leakage current of the hybrid MOS capacitor. The size of III-V/Si hybrid MOS capacitor

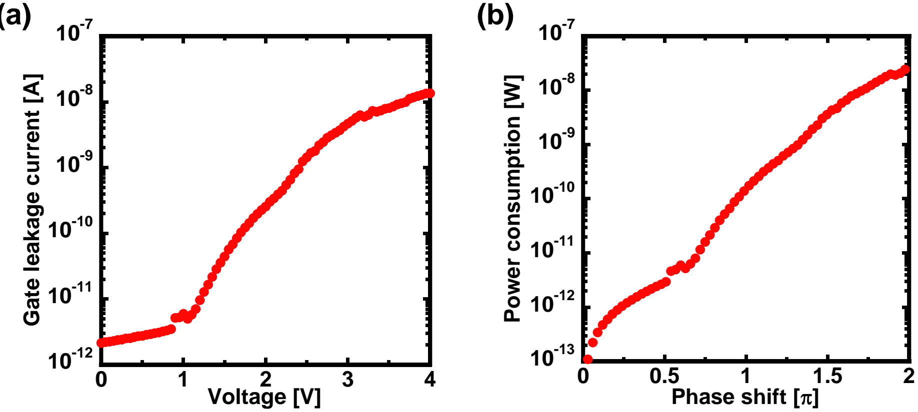

Fig. 4.13. I–V curve of the III-V/Si hybrid MOS capacitor and (b) relationship between power consumption and phase shift of the III-V/Si hybrid MOS phase shifter.

including parasitic part is 2000 μm^2. Figure 4.13(a) shows the current–voltage (I–V) curve of the III-V/Si hybrid MOS phase shifter. For V_g smaller than 2 V, the leakage current was below 1 nA. The relationship between the power consumption and the phase shift obtained from the measurement of the asymmetric MZI is plotted in Fig. 4.13(b). The power consumption for π phase shift was 0.18 nW, which is approximately 10^7 times smaller than that of a TO phase shifter.

Finally, we characterized the dynamic switching properties of the 2×2 Si MZI optical switch. A pseudorandom electrical signal generated by an Agilent 33500B function generator was applied to the III-V/Si hybrid MOS phase shifter. The optical output from one of the output ports of the 2×2 Si MZI optical switch was fed into a Thorlabs DET10D/M InGaAs optical detector and characterized with an Agilent DSO5014A oscilloscope. Figure 4.14(a) indicates that the optical output faithfully responded to the varying electrical driving signal. The zoomed plot of rising and falling edges are shown in Figs. 4.14(b) and 4.14(c), respectively. The measured rising and falling times were 18.6 ns

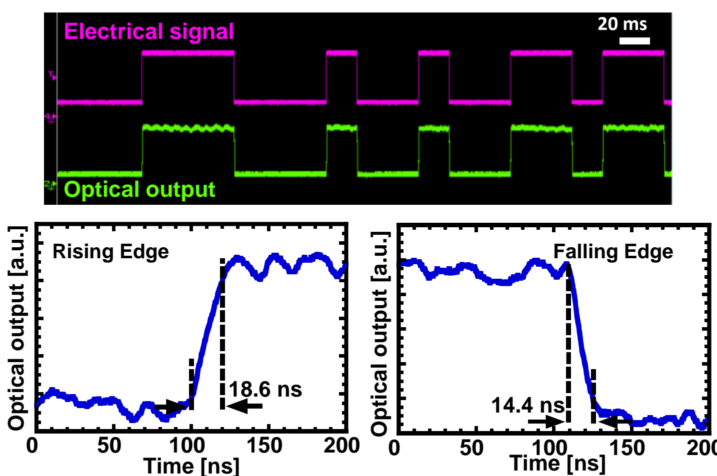

Fig. 4.14. (a) Pseudorandom driving electrical signal and optical output waveform, (b) rising and (c) falling edge of the 2×2 Si MZI optical switch.

and 14.4 ns, respectively, which are currently limited by the measurement setup. By introducing a high-speed measurement setup, the III-V/Si hybrid MOS phase shifter is expected to have a switching time below 10 ns.

4.5 Conclusion

In this study, we successfully demonstrated a 2×2 Si MZI optical switch with III-V/Si hybrid MOS phase shifters. In conjunction with an MMI coupler with tapered input and output ports, broadband and low-crosstalk switching was achieved owing to the electron-induced change in the refractive index of InGaAsP. Since the static switching power was dominated only by the gate leakage current of the hybrid MOS capacitor, the demonstrated optical switch consumed 0.18 nW for switching, approximately 10^7 times smaller than that of a Si TO phase shifter. We also obtained a switching time of < 20 ns, which is approximately 1000 times shorter than that of a TO phase shifter. By optimizing the design and fabrication process, a switching time below 10 ns is potentially achievable. Hence, the III-V/Si hybrid MOS optical phase shifter can be applied to various Si PICs that require efficient, low-power, and high-speed optical phase control.

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Chapter 5

Si racetrack modulator with III-V/Si hybrid MOS optical phase shifter

In the previous chapters, all the devices demonstrated are all based on MZI structure. A MZI structure is consisting of two 3-dB couplers splitting and combining the light beam, and a pair of phase shifters integrated on the waveguides between these two 3-dB couplers. It has several advantages, such as large fabrication tolerance, low sensitivity to temperature variation. However, the length of phase shifter in MZI modulators is several-hundred-μm long [1]. In contrast, the typical radius of a ring resonator for optical modulation is within ten μm [2-4]. Thus, it is easier to realize large-scale integration by adopting ring-type (ring or racetrack) resonators. Furthermore, ring-type resonators have a looped optical path coupled with a straight bus waveguide. When the optical phase shift around one loop equals an integer times 2π, the optical field inside the resonator interferes constructively, strengthening the interaction between optical mode and phase shifter and leading to enhanced optical intensity modulation without increasing the physical capacitance. In this chapter, the integration of a III-V/Si hybrid MOS optical phase shifter on a racetrack resonator was reported. Compared with a MZI optical modulator, the demonstrated racetrack resonator with a III-V/Si hybrid MOS optical phase shifter has successfully reduced the driving voltage and energy consumption.

5.1 Introduction

Among Si optical phase shifters employing the plasma dispersion effect, a metal-oxide-semiconductor (MOS) optical phase shifter is promising in terms of high modulation efficiency. In particular, we have demonstrated a Mach-Zehnder interferometer (MZI) optical modulator with III-V/Si hybrid MOS optical phase shifter which was enabled by wafer bonding technology [5, 6]. Compared with a Si MOS optical modulator, a hybrid MOS optical modulator exhibited a 5-times larger modulation efficiency but with 10-times smaller absorption at π phase shift owing to the electron accumulation at the III-V MOS interface. This makes it promising for efficient, low-loss and low-power optical modulation with advanced modulation format.

In MOS-type optical modulators, the modulation bandwidth and energy consumption are in a trade-off relationship, as shown by the black line in Fig. 5.1. A small capacitance in a MOS junction is demanded for high modulation bandwidth, which limits the modulation efficiency and increases the voltage swing, resulting in high energy

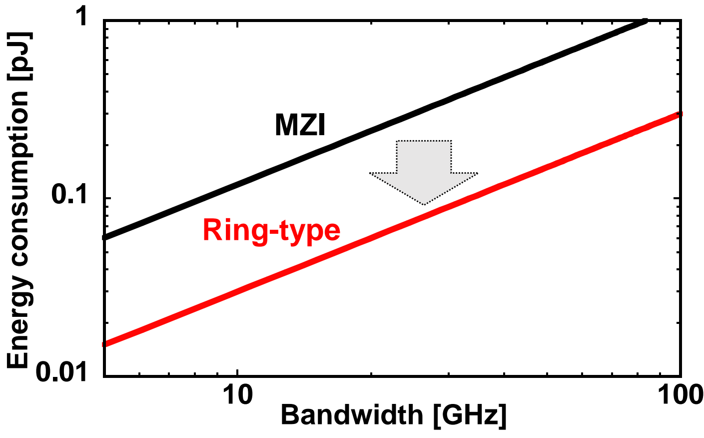

Fig. 5.1. The relationship between the modulation bandwidth and the energy consumption of a MZI modulator (black line) and a ring-type resonator (red line).

consumption. In order to improve this trade-off relationship, it is promising to integrate a hybrid MOS optical phase shifter with a microring resonator, enabling low-energy modulation with smaller voltage swing as the red line shown in Fig. 5.1. However, a 45-μm-long III-V taper is required for transition from a Si waveguide to a hybrid waveguide, a simple ring resonator cannot be integrated with a hybrid MOS optical phase shifter.

In this study, we presented a Si racetrack modulator that enables us to integrate it with a III-V/Si hybrid MOS optical phase shifter. By designing a proper Q factor of a racetrack resonator for efficient and high-speed modulation, the voltage swing of a racetrack modulator with a hybrid MOS optical phase shifter was approximately half of a MZI modulator, reducing the energy consumption by a factor of four.

5.2 Design of a Si Racetrack Modulator with III-V/Si Hybrid MOS Optical Phase Shifter

A cross-sectional schematic of a hybrid MOS optical phase shifter is shown in Fig. 5.2. A thin n-type InGaAsP layer is bonded on a p-type Si waveguide with Al_2O_3 gate oxide. In order to integrate the III-V/Si hybrid MOS optical phase shifter on a Si waveguide, it is necessary to include 45-μm-long III-V tapers for smooth optical mode transition as shown in Fig. 5.2(a). Therefore, a racetrack resonator design is adopted rather than a ring resonator to accommodate the III-V tapers at both the input and output ends of the hybrid phase shifter, as shown in Fig. 5.2(b).

The passive Si components were fabricated on a SOI wafer with a 220-nm-thick Si layer. The width and etching depth of the Si rib waveguide were designed to be 550 nm and 110 nm, respectively. The lengths of the III-V taper and the III-V/Si hybrid MOS phase

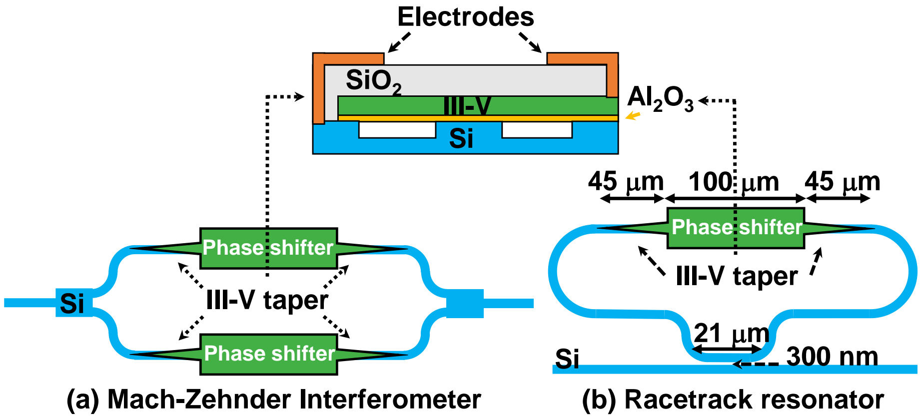

Fig. 5.2. Schematics of (a) a Mach-Zehnder interferometer modulator and (b) a racetrack resonator with III-V/Si hybrid MOS optical phase shifter.

shifter were 45 μm and 100 μm, respectively. The gap between the Si racetrack and the Si waveguide was set to be 300 nm for easy fabrication. The bend radius was assumed to be 5 μm. The length of the coupling region was carefully designed to achieve the critical coupling condition.

The total loaded quality factor (Q_L) of the racetrack resonator is expresses as $Q_L^{-1} = Q_0^{-1} + Q_c^{-1}$, where the Q_0 and Q_c are the intrinsic quality factor and coupling quality factor, respectively [7]. Q_0 can be estimated from the loss of the racetrack by $Q_0 = \frac{2\pi n_g}{\alpha\lambda_0}$, where n_g is the group index, λ_0 is the resonance wavelength, and α is the loss per unit length. In the loss term, the optical loss from the straight waveguide, bent waveguide and the insertion loss of the hybrid phase shifter were taken into consideration. Q_c is related to the coupling length Z_0 via $Q_c = -\frac{\pi n_g L}{\lambda_0 ln[cos(\Delta\beta Z_0/2)]}$, where L is the total length of the racetrack resonator and Δβ is the difference between the propagation constants of the supermodes of the directional coupler structure, which was obtained by simulations using Lumerical MODE

Solutions.

The relationship between Q factors of Q_0, Q_c and Q_L, and coupling length is shown in Fig. 5.3. When $Q_c > Q_0$, the resonator is in under critical coupling condition where the resonance is too weak to be used. When $Q_c < Q_0$, the resonator is in over critical-coupling condition which is only desired for low loss all-pass filter and coupled-resonator filter [8-10]. When $Q_0 = Q_c$, the critical coupling condition is achieved, which has the maximized filed enhancement is desired for efficient optical modulation. Thus, the coupling length for critical coupling condition was found to be 22.74 μm. When a 300-nm gap was assumed in the coupling region, the FDTD simulation showed that the contribution of two waveguide bends to the coupling length was equal to a 2.16-μm-long straight waveguide. Therefore, the length of the directional coupler was determined to be 21 μm. The expected loaded Q factor was 1824, which enables a high photon-lifetime limited bandwidth of over 100 GHz.

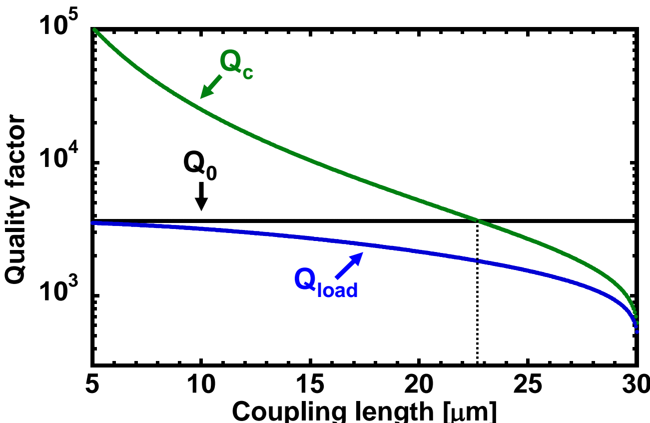

Fig. 5.3. The intrinsic quality factor (Q_0), coupling quality factor (Q_c) and loaded quality factor (Q_L) as a function of coupling length.

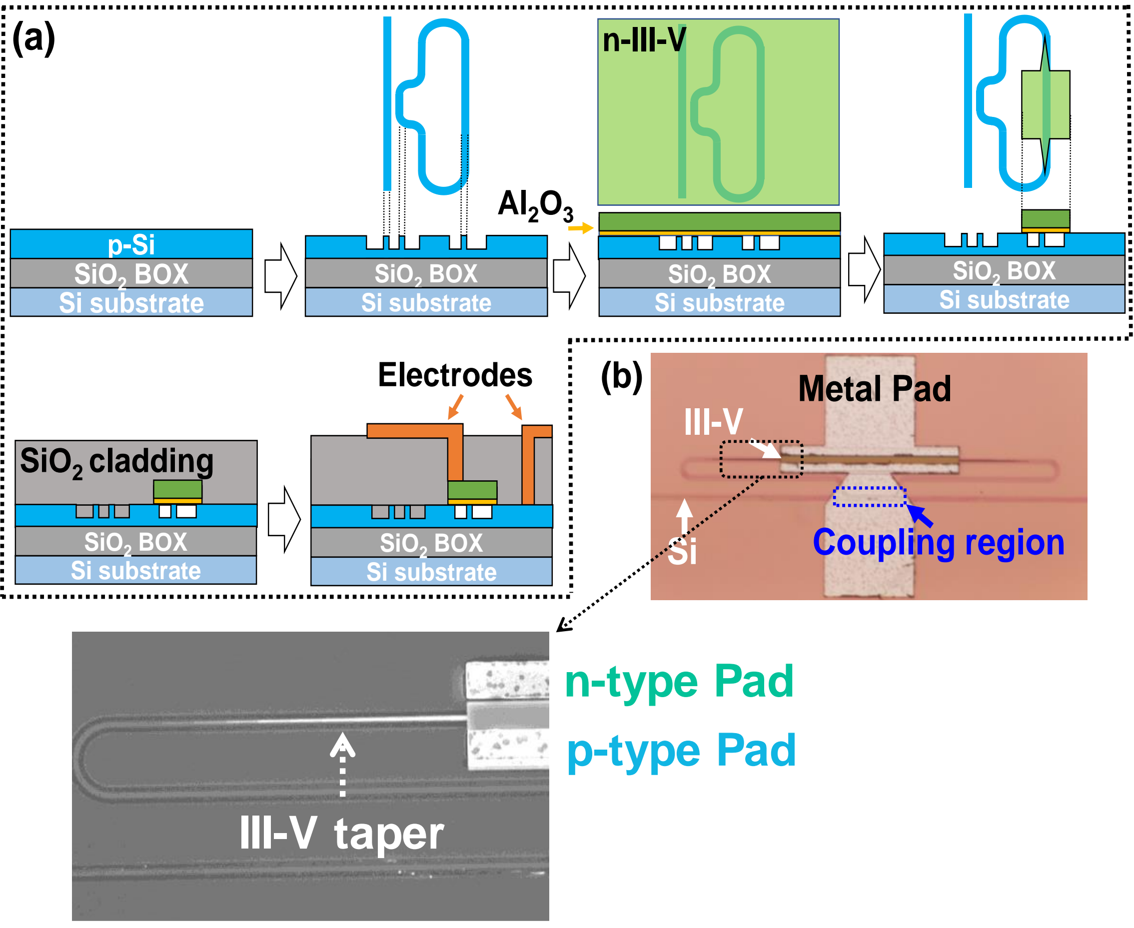

Fig. 5.4. (a) Fabrication procedure and (b) plan-view photo of Si racetrack modulator

5.3 Fabrication of a Si Racetrack Modulator with III-V/Si Hybrid MOS Optical Phase Shifter

The device fabrication process flow is shown in Fig. 5.4(a). The Si passive components, including waveguide and racetrack resonator, were defined by EB lithography and ICP etching on a 220-nm p-type SOI wafer. Then, an InP wafer containing a n-type 200-nm-thick InGaAsP (λ_g=1.37 μm) layer was bonded on a Si waveguide with a 5-nm-thick Al_2O_3 layer as bonding interface. After wafer bonding, the InP substrate and etch-stop layers were selectively removed by wet chemical etching. The thickness of the remaining

III-V layer was 220 nm. A III-V mesa was formed by EB lithography and RIE etching. Then, a 300-nm-thick SiO2 cladding layer was deposited by PECVD. After contact via formation, a Ni/Ti/Pt metal stack was sputtered, and Al was thermally evaporated on the device. Finally, the metal stack was lifted off to form the contact pads. A photo image of the fabricated device was shown in Fig. 5.4(b).

5.4 Characterization of a Si Racetrack Modulator with III-V/Si Hybrid MOS Optical Phase Shifter

The optical transmission spectra with varied gate voltages applied to the III-V/Si hybrid MOS phase shifter are shown in Fig. 5.5. The measured Q was 2607. The extinction ratio was over 25 dB. With the increasing applied voltage, the resonance peak of the racetrack resonator was blue shifted. From the wavelength shift associated with the applied voltage, the modulation efficiency $V_{\pi}L$ was found to be 0.064 Vcm.

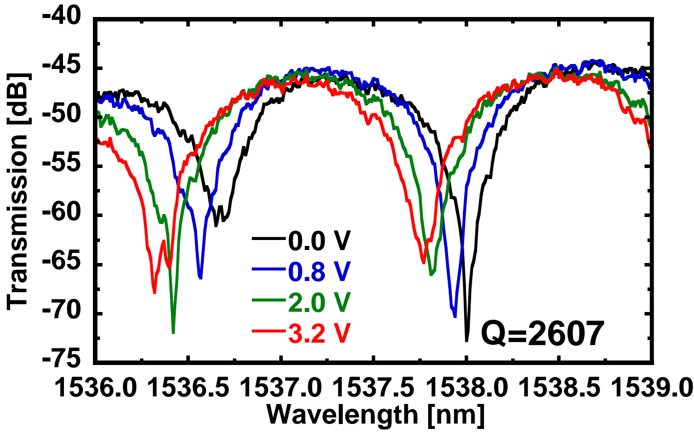

Fig. 5.5. The transmission spectra of the fabricated Si racetrack resonator under the different gate voltages.

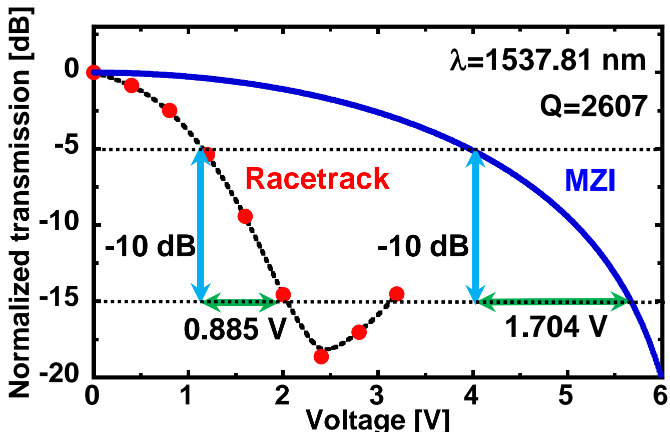

Fig. 5.6. The optical modulation characteristics by the fabricated Si racetrack resonator and a MZI modulator with the same phase shifter.

The optical modulation characteristics at a 1537.81 nm wavelength is shown in Fig. 5.6. The voltage swing for 10-dB (from -5 dB to -15 dB) modulation was 0.885 V, which was corresponding to a phase shift of 0.138π. The simulated optical modulation by a MZI modulator with the same phase shifter is also presented in Fig. 5.6. The 10-dB modulation by a MZI modulator required a voltage swing of 1.704 V. Thus, when we assumed to use the same hybrid MOS phase shifter, the voltage swing of the racetrack resonator for 10-dB modulation was reduced by half, which means the energy consumption was reduced by approximately 4 times. If we use the same voltage swing as a MZI modulator, we can increase a gate oxide thickness double. Thus, the MOS capacitance can be reduced by half, which will double the RC-constant limited modulation bandwidth and reduce the energy consumption by half, simultaneously.

Figure 5.7 shows the calculated energy consumption ratio of a racetrack modulator to a MZI modulator with the same phase shifter, which agreed well with the experimental result. The photon-lifetime limited bandwidth is also plot in Fig. 5.7.

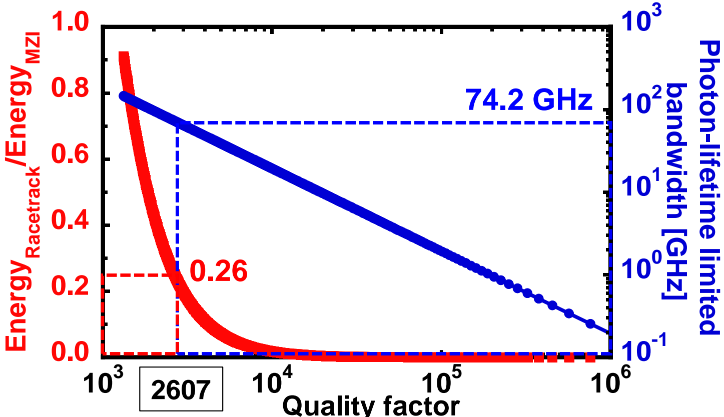

Fig. 5.7. The energy consumption ratio of a racetrack resonator to a MZI modulator (red) and the photon-lifetime limited bandwidth (blue) as a function of Q.

The photon-lifetime limited bandwidth is expressed as $f_{photon} = \frac{c}{\lambda Q}$, with c being the light speed in vacuum. As shown in Fig. 5.7, the Q value of 2607 supports a high photon-lifetime limited bandwidth of 74.2 GHz.

Figure 5.8 shows the benchmark of Si ring/racetrack modulators with respect to 3-dB

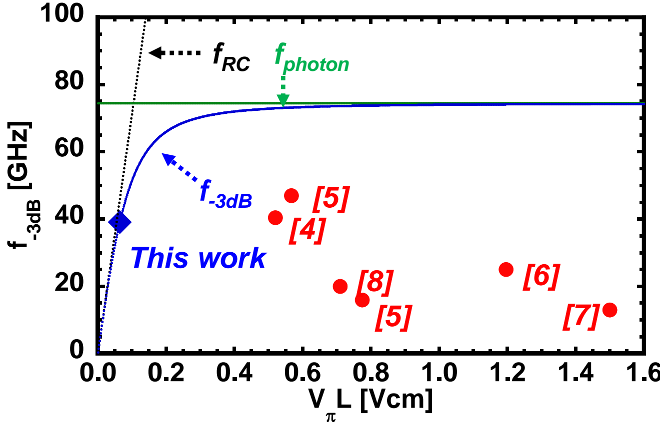

Fig. 5.8. Benchmark of Si ring/racetrack modulators based on the free-carrier plasma dispersion effect.

bandwidth and $V_{\pi}L$ [4, 11-14]. The 3-dB modulation bandwidth is determined by both the RC constant and the photon lifetime, as expressed by $\frac{1}{f_{-3dB}^2} = \frac{1}{f_{RC}^2} + \frac{1}{f_{photon}^2} = \frac{1}{(2\pi RC)^2} + \left(\frac{\lambda Q}{c}\right)^2$ [4]. When the photon-lifetime limited bandwidth was over 74 GHz, the 3-dB bandwidth of the modulator was limited by the RC constant.

5.5 Conclusion

We have demonstrated a Si racetrack modulator with a III-V/Si hybrid MOS optical phase shifter. Compared with a MZI modulator with the same phase shifter, the racetrack resonator successfully reduced the voltage swing by 48% for 10-dB optical intensity modulation, leading to 3.7 times smaller energy consumption. The racetrack resonator exhibited the Q of 2607 which did not limit the 3dB modulation bandwidth dominated by the RC constant. Thus, the integration of the III-V/Si hybrid MOS optical phase shifter into the racetrack resonator successfully improved the energy-and-bandwidth trade-off relationship in MOS optical modulator and is promising for high-speed and low-power optical interconnection.

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Chapter 7

7.1 Thesis summary

In this dissertation, we focus on the understanding, improvement and applications of III-V/Si hybrid MOS optical phase shifter This study can be summarized as below:

1. The performance dependence on the structure of III-V/Si hybrid MOS optical phase shifter was studied through numerical simulations. The influence of doping concentration of III-V layer, thickness of III-V and Si layers, EOT on the modulation efficiency was analyzed. By using III-V and Si layers of the same thickness, the peak of optical intensity can be aligned with accumulated free carriers. In addition, the optical power at the center of III-V/Si hybrid optical phase shifter can be intensified by using 72-nm-thick III-V and Si layers with the width of phase shifter fixed as 1 μm. By using this structure, a low $V_{\pi}L$ of 0.0358 Vcm was predicted with 5-nm EOT.

2. To realize high-speed operation, parasitic capacitances were removed by introducing an isolation trench on one side of Si rib waveguide and using Si waveguide embedded in SiO_2. The ratio of parasitic capacitance to the total capacitance has been reduced from 87.5% to 30.3%. In the future, all the parasitic capacitance is able to be completely removed by improving the interfacial quality of Si waveguide embedded in SiO_2 and high-speed operation is expected.

3. The modulation efficiency of III-V/Si hybrid MOS optical phase shifter is linearly proportional to the EOT value of the III-V/Si hybrid MOS capacitor. Reducing the EOT value is effective to enhance the modulation efficiency, which is attractive for the applications in optical switch. In the previous study, an EOT scaling issue was identified.

It was found that the EOT value saturates above 5 nm regardless of the physical thickness of the Al_2O_3 used for wafer bonding. It was suspected that the EOT scaling issue is due to the generation of nano-scale tiny voids on the bonding interface which can be attributed to the degassing of H_2O from Al_2O_3 layer. It was also found in the previous study that introducing HfO_2 into the Al_2O_3 bonding interface is effective to suppress the void generation. Furthermore, the high dielectric constant of HfO_2 enables more efficient EOT scaling than Al_2O_3. In this chapter, by utilizing the HfO_2/Al_2O_3 bilayer bonding stack, the void generation on the bonding interface was suppressed. EOT scaling was successfully carried out. A CET as small as 3.5 nm was obtained by thinning both the HfO_2 and Al_2O_3 layer. Simulations predicted that a III-V/Si hybrid MOS optical phase shifter with a CET of 3.5 nm is able to deliver high modulation efficiency with a $V_{\pi}L$ of 0.029 Vcm.

4. Optical switch is a promising alternative to replace electrical switch in data center application because optical switch enables lower power consumption, mainly by eliminating the optical/electrical/optical conversion, and larger bandwidth owning to the elimination of the electrical pin and the compatibility with wavelength multiplexing technology. In chapter 4, a 2×2 Si MZI optical switch with III-V/Si hybrid MOS optical phase shifter was successfully demonstrated. A 2×2 MMI coupler was designed to enable broadband and equal optical splitting which contributes to the broadband and low crosstalk optical switching. A Si/III-V double layer taper was designed and employed to allow for low insertion loss. The 2×2 Si MZI optical switch was fabricated, exhibiting broadband 2×2 optical switching. The crosstalk was below -23 dB due to the low absorption in III-V layer. The power consumption for switching is only 0.18 nW, which is dedicated by the leakage current of the III-V/Si hybrid MOS capacitor. The switching speed was measured below 20 ns, which is currently limited by the measurement setup. The 2×2 Si MZI optical

switch with ultra-low power consumption and high-speed optical switching is promising for applications in data centers or various PIC.

5. For MOS-type MZI optical modulator, there is an intrinsic trade-off relationship between modulation efficiency and modulation bandwidth. High modulation efficiency necessitates a large capacitance that limits the modulation bandwidth. However, for ring-type optical modulator, the looped optical path results into a high quality factor leading to steep change of optical intensity near the resonance wavelength. In chapter 5, the III-V/Si hybrid MOS optical phase shifter was successfully integrated on a racetrack resonator and demonstrated reduced voltage swing for 10-dB optical intensity modulation than that of a MZI optical modulator. A racetrack design is adopted in replace of a ring structure to accommodate III-V tapers on both input and output ends of the III-V/Si hybrid MOS optical phase shifter. The coupling length was carefully designed to achieve critical coupling condition for efficient optical intensity modulation. The gap between the racetrack and Si waveguide is 300 nm. The coupling length was determined as 21 μm. The Si racetrack modulator integrated with III-V/Si hybrid MOS optical phase shifter was demonstrated with a Q of 2607. Compared with a MZI modulator with the same phase shifter, the voltage swing of the racetrack modulator for 10-dB modulation was reduced by half, which means the energy consumption was reduced by a factor of 4. On the other hand, with the driving voltage being fixed, the capacitance required by the racetrack modulator is halved than that of a MZI modulator, which will double the RC-constant limited modulation bandwidth and reduce the energy consumption by half.

6. A MOS-type optical modulator driven by a forward gate voltage induces a large oxide capacitance limiting the modulation bandwidth. In order to remove this intrinsic trade-off relationship, an efficient optical modulator by reverse-biased III-V/Si hybrid

MOS capacitor was proposed. With reverse bias, F-K effect and carrier depletion are combined together to contribute to high modulation efficiency. Compared with the forward biased case, the reverse bias induces a small capacitance, which expands the modulation bandwidth. In chapter 6, the wavelength detuning and doping concentration of III-V and Si layers were optimized for high modulation efficiency and large modulation bandwidth. The proposed modulator was successfully fabricated and characterized. The optical modulator showed a $V_{\pi}L$ of 0.12 Vcm, which agrees well with the theoretical calculation and confirms the feasibility of the proposal. Compared with forward biased case for the same modulation efficiency, the reverse biased optical modulator showed halved capacitance, which is expected to enable high-speed and low-power optical interconnection beyond 100 GHz.

Figure 7.1 shows comparison of the performance of III-V/Si hybrid MOS optical phase shifter working under accumulation mode, depletion mode and integrated on a Si

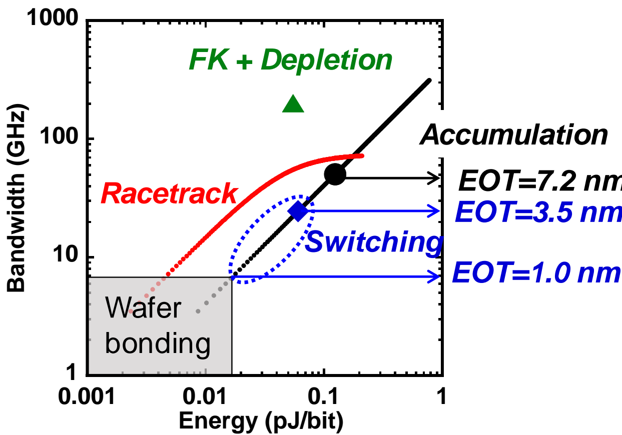

Fig. 7.1. Comparison of the performance of III-V/Si hybrid MOS optical phase shifter working under accumulation mode, depletion mode and integrated on a Si racetrack modulator.

racetrack modulator. Regarding the optical modulation application, the combination of F-K effect and carrier depletion, as indicated by the green triangle is the most promising in terms of the balance between modulation bandwidth and energy consumption. It can achieve a high modulation bandwidth (>200 GHz) with small energy consumption (<0.06 pJ/bit), but with higher optical absorption than the accumulation mode. The III-V/Si hybrid MOS optical modulator working in accumulation mode, as indicated by the black line, is capable of large modulation bandwidth by EOT scaling with low optical absorption. For example, to realize 100 Gb/s data transmission, it is safe to have a 50-GHz modulation bandwidth [1], which requires a EOT of 7.2 nm. The energy consumption would be around 0.1 pJ/bit. By integrating a III-V/Si hybrid MOS optical phase shifter on a Si racetrack modulator, high modulation bandwidth and low energy consumption is enabled. Besides, the footprint of racetrack modulator was smaller than that of a MZI modulator. However, the modulation bandwidth of a racetrack modulator is limited by photon lifetime in addition to the RC constant. Moreover, racetrack resonator features narrower optical bandwidth and is sensitive to temperature variation as other ring-type resonators.

Regarding optical switching applications, a modulation bandwidth larger than 0.1 GHz is sufficient because the reconfiguration process of an optical switch takes time of more than 10 ns [2]. In addition, high-speed data transmission is realized by high port counts in an optical switch rather than by low switching time. Since the modulation bandwidth of III-V/Si hybrid MOS optical phase shifter can easily reach tens of GHz with several-nm EOT, the reduction of energy consumption is more attractive for an optical switch. The energy consumption scales linearly with capacitance which is determined by EOT. In chapter 3, we have realized an EOT of 3.5 nm leading to energy per bit of 0.06 pJ/bit. With thinner EOT, lower energy consumption is obtainable. The scaling is limited

by the EOT that can be realized by the III-V/Si wafer bonding technology.

This study has explored various applications of III-V/Si hybrid MOS optical phase shifter, which is promising for efficient, low-loss and high-speed optical phase modulation. There are both advantages and disadvantages for each specific case. However, we have provided several possibilities to choose from basing on specific requirements.

7.2 Prospect and possible works

In this dissertation, although many studies have been demonstrated experimentally, there remained some work only investigated by simulations. In some part of the dissertation, preliminary verifications of necessary process have been finished and final demonstrations are waiting to be done. Additionally, there are many possibilities and applications in which the employment of III-V/Si hybrid optical MOS phase shifter has great potential. All these topics are summarized and discussed as below.

1. In chapter 2, the enhancement of modulation efficiency by adjusting III-V and Si layer thickness has been investigated by simulation. The results indicate that, by using 100-nm-thick Si layer and 120-nm-thick InGaAsP layer, a low $V_{\pi}L$ of 0.038 Vcm is expected. The fabrication process flow of such a device has no significant difference with previous demonstrations except that it required a SOI wafer with 100-nm-thick Si layer that is not commonly used for Si photonics. In order to address this issue, a combination of surface oxidation and chemical etching process should be added before the established process flow to thin the commonly used 220-nm SOI wafer. After that, the demonstration of a higher modulation efficiency could be easily done.
2. The EOT scaling of III-V/Si hybrid MOS capacitor has been explored. The CET of

III-V/Si hybrid MOS capacitor has been successfully scaled down to 3.5 nm. By combing the EOT scaling and structure optimization mentioned above, a low $V_{\pi}L$ of 0.029 Vcm is expected. The experimental demonstration of this conclusion is meaningful to break the modulation efficiency record set by the demonstration in [3]. In the future, a thinner CET as small as 1 nm may be obtained by utilizing ZrO_2/Al_2O_3 stack for wafer bonding, which is meaningful to explore the ultimate potential of III-V/Si hybrid MOS optical phase shifter.

3. To realize high-speed operation, several ways to remove parasitic capacitance have been proposed in this dissertation. The 86% parasitic capacitance has already been removed by introducing an isolation trench. The complete removal of all the parasitic capacitance requires a SiO_2 filling process followed by a CMP process. The preliminary experiments have been conducted to verify the feasibility of bonding a III-V on a process Si wafer. Since the proposed process is outsourced to a Si photonics foundry service, the remaining issue to be resolved is the process integration of inhouse process and standard Si photonics process. For instance, our inhouse process use electron beam (EB) lithography for its fine linewidth, while the Si photonics foundry use KrF photo lithography out of the consideration of process maturity and cost. It is important to ensure that the mark pattern required by the EB process is accurately fabricated in the photo lithography step and can be easily recognized in the EB alignment procedure.

4. A 2×2 Si MZI optical switch with III-V/Si hybrid MOS optical phase shifter was demonstrated with ultra-low power consumption and high-speed reconfiguration. However, high-port count is an important figure of merit for optical switch to be deployed in practical application. Therefore, the demonstration of 4×4 or 8×8 optical switch is critical to act as a prototype to verify the scalability of the optical switch fabrics based on the III-V/Si hybrid MOS optical phase shifters. To this end, the uniformity of III-V/Si wafer bonding should

be confirmed to allow for the fabrication of several phase shifter with similar performance by one-step wafer bonding.

5. In addition to optical modulator and switch, there are a variety of areas where the employment of III-V/Si hybrid MOS optical phase shifter can bring competitive advantages, such as photonic neuron network [4, 5] and optical phase array (POA) for LiDAR application [6]. A Si PIC with plenty of 2×2 optical switches meshed together is capable of performing arbitrary linear operation on the input matrix, which can be utilized for implementing deep learning algorithms [7, 8]. The low power consumption of the 2×2 Si optical switches demonstrated before in conjunction with the low absorption loss in the III-V material makes the III-V/Si hybrid MOS optical phase shifter is advantageous in the application of photonic neural network that require excellent scalability. In order to ensure safe driving and rapid response, autonomous cars need to acquire information from constantly changing environment via plenty of sensors, among which the light detection and ranging (LiDAR) sensor is a crucial one. Beam steering is one key functionality in LiDAR. In a recent study, a LiDAR sensor by integrating III-V phase shifters on Si photonic platform has been demonstrated. In this work, a III-V multiple quantum-well (MQW) with both n-type and p-type doping is bonded on Si waveguide. It is necessary to make both n-type and p-type metal contacts on III-V layer. For such kind of configuration, usually one contact is made on the top of MQW with thick (1~2 μm) III-V cladding layer to avoid severe optical absorption loss, which results into a small optical confinement factor, less efficient phase modulation [9]. In addition, the III-V phase shifter in this integration scheme is impossible to act as an active grating emitter since the metal contact will absorb all the light. In our design, a n-type thin (~200 nm) III-V layer is used for the modulation in conjunction with p-type Si layer, which contributes to a larger optical confinement factor.

Metal contact is made away from the hybrid capacitor, enabling the light emission through the III-V gratings. By controlling the gate voltage applied between the III-V and Si layers, the free carriers are accumulated or depleted near the MOS interface, modulating the refractive index and changing the light emission angle. With the active optical beam steering in both longitudinal and lateral axis, the scanning range is broadened, enabling more compact beam steerer.

7.3 Reference

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List of publication

1. Publication as the first author

A. Journals

[1]. Q. Li, J.-H. Han, C.P. Ho, S. Takagi, and M. Takenaka, "Ultra-power-efficient 2x2 Mach-Zehnder Interferometer Optical Switch based on III-V/Si hybrid MOS Phase Shifter," *Opt. Express*, vol. 26, 35003, 2018.

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[2]. (Oral presentation) Q. Li, C.P. Ho, S. Takagi, and M. Takenaka, "Efficient Optical Modulator by Reverse-biased III-V/Si Hybrid MOS Capacitor based on FK Effect and Carrier Depletion," *Optical Fiber and Communication Conference (OFC2019)*, p. M4A.2, San Diego, March 2019.

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2. Publication as non-first author

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