博士論文

Development of Nonlinear Interface Circuits for Electret Kinetic Energy Harvester

(力学的エレクトレット環境発電器のための非線形電源管理回路の開発)

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Abstract

In the scenario of the Internet of Things (IoT), wireless sensor nodes play a fundamental role for sensing and communication. Currently, most nodes are battery-powered. However, with the proliferation of sensor nodes, the choice of battery becomes unfavorable considering its inevitable maintenance and environmental burden. On the other hand, energy harvesting, which exploits ambient energy to generate electricity, has emerged a promising alternative solution in place of batteries. So far, the main task for small-scale energy harvesting is to enhance the output power to support a wider range of low-power electronics.

This thesis focuses on electret-based in-plane kinetic energy harvester which has been demonstrated to be MEMS compatible, low in profile and to harvest more power in sub-100 Hz frequency range compared electromagnetic counterparts. However, its output power is severely constrained by the shunting effect of parasitic capacitance due to its lower internal capacitance. Structural designs have been attempted to reduce the parasitic capacitance. On the other hand, the shunting effect can be compensated by nonlinear power management circuits such as SSHI (Synchronous Switch Harvesting on Inductor). However, as electret-based energy harvester exhibits low output current and low internal capacitance, high-voltage small-signal components should be selected to minimize introduced capacitance and leakage current. Therefore, there has been no existing study focusing on nonlinear circuits for electret-based energy harvester. The present study attempts to develop nonlinear circuits for electret-based energy harvester, aiming at enhancing its output power. The objective of the present study is to present new approaches to optimize energy conversion from kinetic energy (human motion) using rotational electret energy harvester and to describe the most important parameters in circuit design. Meanwhile, in terms of wearable application, the height of the proposed circuit should not exceed that of the low-profile electret energy harvester itself. Therefore, the applicability of the proposed circuits to integrated circuit (IC) technology is also investigated in the present study, aiming at realizing a practically-attractive low-profile circuit.

In the present study, the electromechanical transduction mechanism of electret in-plane energy harvester is elucidated analytically for the first time, which confirms the applicability of nonlinear circuits on electret kinetic energy harvester. The proposed model also enables a comparison of output characteristics between electret-based and

piezoelectric energy harvester, which specifies challenges of implementing nonlinear circuits on electret-based energy harvesters, which are much more susceptible to parasitic capacitance than piezoelectric ones.

Development of SSHI for electret-based rotational energy harvester is presented in the present study. The theoretical performance of SSHI on electret EH is derived and verified by simulation with LTspice, showing a power enhancing ratio of 6.7 against the standard case, where a conventional full-bridge rectifier is employed. Circuit design of parallel SSHI is then proposed using a resistive voltage divider as the low-voltage signal generator. Based on this voltage-divider SSHI design, experimental validation based on a test bench of electret-based energy harvester is carried out using discrete components. In the external-powered SSHI where the control block is powered by external DC supply, a power enhancing ratio of 2.47 is experimentally achieved at a rotating speed of 1 rps. In addition, simulated results are in accordance with experimental results, which makes it possible to analyze SSHI circuit based on simulation. As a result, the inversion ratio, which is the benchmark of SSHI performance, is highly related to the parallel resistance of the inductor due to the low shunt capacitance of electret energy harvester. Since the serial resistance of the inductor is not important in determining SSHI performance, it is valid to utilize thinner wires for reducing the height of the inductor which dominates the height of the whole circuit. According to the circuit efficiency analysis, the voltage-divider and the diodes in rectifier turned out to be quite lossy in the high voltage range where the performance of SSHI increases. Consequently, the efficiency of SSHI drops from over 80% @ 30V to below 30% @ 200V.

In this regard, a novel dual-stage electrode design is proposed to achieve efficient operation of SSHI. The proposed dual-stage electrode aims to reduce power loss by removing the lossy voltage divider. Instead of the voltage-divider, a minority of area in the stator serves as a control stage to provide low-voltage signal for the control block; whilst a power stage with major area is in charge of power generation. Thanks to this isolated control stage, the switch action is also immune to voltage drops led by subsequent converter operation. Consequently, a power enhancing ratio of 4 is achieved, which is 1.56 times of the power harvested with the voltage-divider SSHI. The efficiency of SSHI is thus enhanced. Self-powered SSHI is then examined with a dual-polarity converter to supply the control block, making the system energetically closed. However, the power enhancing ratio reduces to 1.4 in the self-powered SSHI due to 1)

the low voltage rating (50V) of the dual-polarity DC/DC converter, where the power enhancing ratio of SSHI is merely 2.8; 2) the low efficiency 50% of the dual-polarity converter. Dual-stage SSHI is successfully implemented on a fully-integrated electret EH, instead of test bench, with cold-start and self-powering ability confirmed under random excitation.

Since the proposed parallel SSHI suffers from the low efficiency of dual-polarity rectifier and requires high voltage (input voltage>200V) DC/DC converter, which is difficult to realize efficiently, a novel dual-stage SECE (Synchronous Electric Charge Extraction) circuit for electret-based energy harvesters is presented. Compared with SSHI, SECE is free of dual-polarity rectifier, and should harvest more power in a lower load voltage range. Therefore, a higher overall power enhancing performance is expected with SECE, especially in the low voltage range at DC load side. The theoretical performance of SECE on electret EH is derived and then verified by simulation with LTspice. Circuit design of SECE is then proposed, featuring a novel switch control scheme adaptive to arbitrary internal capacitance and the external inductor. Test-bench-based experimental validation is carried out with the control block externally powered. Consequently, a power enhancing ratio of 2.77 against full-bridge rectifier is experimentally achieved at a rotating speed of 1 rps. Notably, a power enhancing ratio of 2 at a low load voltage of 5 V is achieved with current SECE design, which confirmed that additional DC/DC converter is not required. Based on the simulation, the end to end efficiency of the proposed SECE circuit reaches 80% at a DC load voltage of 10V, which is superior to that in SSHI. Meanwhile, the voltage stress at generator output in SECE is approximately twice of the open circuit voltage in standard DC case, which is also several times lower than the optimal voltage in SSHI, making it easier to miniature SECE circuit. Self-powering and cold-start of the proposed SECE can be achieved by utilizing the charges accumulated in the control stage. Moreover, simulation result shows that the inductor in SECE could be lower than 100 μH without severely reducing the power enhancing performance, which is also in favor of the circuit miniaturization. Based on the efficiency analysis, reducing the forward voltage drop of the freewheel diode, which consumes substantial power in the freewheeling phase due to the large current amplitude, is crucial to improve the SECE performance in low load voltage range.

The IC-compatibility of the proposed circuits is investigated. It is found that except the inductor, components in the proposed nonlinear circuits can be integrated on chip

by utilizing high-voltage BCD process. The inductor, on the other hand, could be tailored to be low-profile in our case according to the discussion above. With the aid of IC technology, the power consumption of the control blocks in nonlinear circuits should be further reduced. In this regard, tri-stage SSHI circuit is proposed to remove the low-efficiency dual-polarity converter. Instead, the control block is powered by a third stage which outputs dual-polarity voltage with limited power. In this way, the converter in the power stage could be a classic unipolarity converter which exhibits higher efficiency. For SECE, with reduced power consumption of control block using IC, it becomes feasible to power the control block by the DC-side storage capacitor of the control stage, thereby achieving self-powering and cold-start. Therefore, low-profile nonlinear circuits is achievable for electret energy harvester with the aid of IC technology.

To summarize, the present study presents the development of nonlinear circuits (SSHI, SECE) for electret kinetic energy harvester for the first time. Detailed circuit design of the nonlinear circuits is proposed, simulated, experimentally validated and analyzed. SSHI is developed for its higher theoretical output power at generator output over SECE, but it needs high-voltage DC/DC converter which currently suffers from low efficiency and low voltage rating. In this regard, SECE is developed for its higher output power at low-voltage DC load side over current SSHI. A novel dual-stage electrode design is proposed to address the high output voltage of the electret energy harvester, thereby enabling efficient operation of SSHI and innovative design of control block in SECE. Consequently, the effectiveness of the proposed dual-stage design is experimentally confirmed. In regard to battery-less operation of the circuits, self-powering and cold-start schemes for nonlinear circuits are proposed. The ability of cold-start and self-powering under random excitation is experimentally confirmed for the proposed dual-stage SSHI. Circuit analysis based on simulation is carried out to provide guidance for improving the performance of the proposed nonlinear circuits and for selecting a proper inductor which usually dominates the height of the circuit. Based on the efficiency analysis, the lossy components in the proposed circuits are located and methods to reduce their power consumption are indicated. By analyzing how the inductance, series resistance and parallel resistance of the inductor influence the power enhancing performance, it is found that the inductor in both circuits could be scaling down to be low profile, without severely destroying the power enhancing performance. It is also found that except the inductor, components in the proposed nonlinear circuits

can be integrated on chip by utilizing high-voltage IC process. Therefore, low-profile nonlinear circuits, which intend for wearable application, is feasible for electret energy harvester.

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Nomenclature

0.0.0.1 Roman symbols

R_L Load resistor

C_p Parasitic Capacitance

F_{PE} Restoring force to the piezoelectric disk

K_{PE} Short-circuit stiffness of the piezoelectric disk

u Displacement of piezoelectric disk/collector electrode

V Generator output voltage

I Generator output current

I_s Source current in the generator

C_0 Internal capacitance of generator

F_e Electrical restoring force

x_1 Relative displacement of collector electrode

w Width of electrode

E Electric field

0.0.0.2 Greek symbols

α Force factor

ε Permittivity

σ Surface charge density

0.0.0.3 Subscripts and superscripts

^{TM} Trade Mark

$_{PE}$ Piezoelectric energy harvester

$_{EE}$ Electret energy harvester

0.0.0.4 Abbreviations

IoT	Internet of Things
WSN	Wireless Sensor node
MCU	Micro-Controller Unit
RF	Radio Frequency
VDRG	Velocity-Damped Resonant Generator
ECM	Electret Condenser Microphone
MEMS	Micro-Electro-Mechanical Systems
PCB	Print Circuit Board
PFC	Power Factor Correction
rpm	revolutions per minute
AC	Alternative Current
DC	Direct Current
IC	Integrated Circuit
SSHI	Synchronized Switch Harvesting on Inductor
SSHC	Synchronized Switch Harvesting on Capacitor
DSSH	Double Synchronized Switch Harvesting
SSHI-MR	Synchronized Switch Harvesting on Inductor with Magnetic Rectifier
SECE.	Synchronous Electric Charge Extraction
OSECE	Optimized Synchronous Electric Charge Extraction
ASIC	Application-Specific Integrated Circuit
MPPT	Maximum Power Point Tracking

Chapter 1 Introduction

1. 1. Energy Harvesting

1. 1. 1. Internet of Things

In the scenario of the IoT [1] (Figure 1-1), WSNs play a fundamental role for sensing and communication. A typical WSN (Figure 1-2) contains three parts: a sensor, a wireless MCU and their power supply. Currently, most WSNs are battery-powered. However, with the proliferation of sensor nodes, the choice of battery becomes unfavorable considering its inevitable maintenance and environmental burden. In this regard, researchers are exploring alternative solutions in place of batteries.

On the other hand, thanks to the rapid development of electronic industry, the power consumption of the components in a WSN has been reduced substantially (Figure 1-3). For example, the wireless MCU CC2650 [2] exhibits a standby power dissipation as low as 1.8 μW. Meanwhile, the sensor in a WSN usually consumes power ranging from sub-10 μW to tens of milliwatts, according to its specific function. As a result, the average power consumption of a WSN operating in an intermittent mode can be restrained in μW level, which alleviates the stress on its power supply.

1. 1. 2. Small-scale Energy Harvesting

Energy harvesting is an emerging technology which exploits ambient 'waste' energy to generate electricity, aiming to provide a local maintenance-free power supply for WSN in place of battery [3] (Figure 1-4).

The ambient energy includes vibration, light, heat, radiation and so on. The term 'waste' means that this unconfined energy will otherwise be wasted if not captured by the energy harvesting device. Therefore, the energy sources (light, heat, radiation, etc.) for energy harvesting are usually weak and loose, which is different from those for macroscale power generation. This is a major feature of energy harvesting which differs from conventional power generation. The power densities of energy sources for energy harvesting is given in Table 1-1.

Table 1-1 Characteristics of various energy sources available in the ambient and harvested power [4].

Source	Source power	Harvested power
Ambient light		
Indoor	0.1 mW/cm^2	10 μW/cm^2
Outdoor	100 mW/cm^2	10 mW/cm^2
Vibration/motion		
Human	0.5 m @1 Hz 1 m/s^2 @50 Hz	4 μW/cm^2
Industrial	1 m @5 Hz 10 m/s^2 @1 kHz	100 μW/cm^2
Thermal energy		
Human	20 mW/cm^2	30 μW/cm^2
Industrial	100 mW/cm^2	1-10 mW/cm^2
RF		
Cell phone	0.3 μW/cm^2	0.1 μW/cm^2

On the other hand, since the energy harvester is intended for replacing small batteries, it should be miniaturized. In this regard, small-scale (dimensions in cm-scale or less) energy harvesters attract much attention[5][6]. Small-scale energy harvesters usually generate up to hundreds of microwatts [4], which exceeds the power consumption of a WSN in a cyclic mode. But the bottleneck is still the limited output power.

1. 1. 3. Kinetic Energy Harvesters

Kinetic energy harvester is extensively studied as motion is ubiquitous in ambient environment [7]. Figure 1-5 shows a motion-powered quartz watch: Seiko Kinetic [8], which is an example of successfully commercialized product based on kinetic energy harvesting.

The kinetic energy source includes human and machine motion. Human motion is usually around 1 Hz, featuring multiaxial motion with large amplitude; whilst machine motion is usually sub-100 Hz linear vibration with limited amplitude. In other words, the mechanical excitation in energy harvesting scenes is usually weak, intermittent and low in frequency [9]. As a result, new challenges, which do not exist or stand out in macro-scale power generation, arise in kinetic energy harvesting field, such as designing a miniaturized energy harvester with high effectiveness [10], developing new

mechanisms to achieve broadband energy harvesting [11] and introducing innovative energy-efficient power conditioning circuits to optimize output power [12].

Three popular transduction principle are studied: electrostatic[13]–[15], piezoelectric[16]–[18] and electromagnetic [19]–[21]. Figure 1-6 shows a comparison of effectiveness between different types of linear vibration energy harvesters which is suitable for capture machine motion. It reveals that electrostatic energy harvesters show higher effectiveness at lower frequency, if compared with piezoelectric or electromagnetic counterparts.

Recently, rotational kinetic energy harvester is gaining attention for its potential to harvest energy from human motion. As human motion features large-amplitude multi-axis movement, rotational structure should be more suitable than linear-motion-driven ones. In addition, there is no upper limit of displacement for rotational devices, thereby the power generation limit of VDRG can be overcome [22]. Romero et al. presented an integrated electromagnetic rotational energy harvester (Figure 1-7a), harvesting 10 μW from elbow motion at 1.56 m/s walking speed [23]. Xue et al. fabricated a wrist-worn piezoelectric rotational energy harvester generating 40 μW at 1 rps rotational speed [24]. Recently, Miyoshi et al. successfully fabricated a wrist-worn low-profile (3.3 mm) electret (electrostatic) rotational energy harvester which outputs 80 μW at 1.45 m/s walking speed [25].

1. 2. Electret-based kinetic energy harvester

Electret is a dielectric material which is capable of storing charges quasi-permanently[26]. It was firstly introduced by Eguchi in 1920 [27]. Later, Sessler [28] in Bell Laboratories made a major breakthrough by applying electret into microphone, known as ECM which is widely used in tape recorders, stereos, telephones, cordless and cellular phones and hearing aids now [29].

The application of electret in power generation dates back to 1970s, when Jefimenko reported the first electret generator (152 mm in diameter, Figure 1-8a) [30], later improved and refined by Tada (90 mm in diameter, Figure 1-8b) [31], [32]. Electret generator is a special type of electrostatic generator where a pre-charged electret where a pre-charged electret serves as a quasi-permanent charge source, so it is free of external circuitry to provide bias voltage or charge. In their generators, the charge on the counter electrode, induced by the charged electret, changes due to in-plane motion of electret, resulting in an alternative current in external circuit (**Figure 1-9**). Their pioneer work

demonstrated the feasibility of electret generator, but no further application was followed because electret generator has no distinct advantages upon electromagnetic ones in macro scale.

In 2003, Boland et al presented a micro-scale electret generator (8 mm in diameter) based MEMS technology [33]. It obtained 25 μW when rotating at 4170 rpm. In the meantime, Genda et al explored the possibility of using electret generator in micro-machined gas turbines[34]. Electret generator gains attention in micro scale because it is compatible with semiconductor fabrication technology. Their work reveals that it is necessary to enhance the output power of electret generator. Two major ways to do so is to develop high-performance (high surface potential and long-term stability) electret material and to evolve mechanical fabrication method (e.g. gap control, increasing poles).

As for the high-performance electret, Kashiwagi et al developed nano-cluster-enhanced high-performance perfluoro-polymer electrets, known as CYTOP EGG™, exhibiting both high surface charge density and excellent long-term charge stability (Figure 1-10) [35]. In addition, Hagiwara et al proposed soft-X ray charging (Figure 1-11) in place of conventional corona charging, which enables uniform charging electret after package [36]. As for the fabrication evolution, progress are made in [14], [37]–[39] by increasing the number of poles, introducing reliable spring and packaging.

These fundamental progress made electret generator interesting in kinetic energy harvesting field in that: (1) frequency up-conversion, which is crucial in enhancing the output power of energy harvester in low-frequency operation [40][41][42], is easily achievable in electret generators by increasing the number of poles; (2) electrostatic(electret) generators are compatible with semiconductor fabrication technology, hence it is possible to integrated electrostatic energy harvester and other low-power electronics in a WSN together. (3) Compared other types of electrostatic generator [43][44], electret generator is free of external circuitry for providing bias voltage or charge, which makes the generator simple and reliable.

As a result, Masaki et al reported a fully-integrated linear-vibration electret energy harvester (**Figure 1-12**), harvesting 100 μW under 30Hz, 0.15 g. excitation[45]. Recently, Miyoshi et al reported a wrist-worn rotational electret energy harvester(**Figure 1-7**c) for human motion, harvesting 80 μW at a walking speed of 1.45 m/s [38].

Besides the aforementioned in-plane overlapping-area-change type of electrostatic(electret) (Figure 1-13a), there is another type called gap-closing (Figure 1-13b) [46]–[50]. In the overlapping-area-change type, the relative movement between electret and its counter electrode, due to in-plane motion, directly leads to the variation of induced charges on the counter electrode and hence an external current. In the gap-closing type, the change of gap distance, driven by either in-plane or out-of-plane motion, leads to capacitance change of the air layer, which initiates a charge redistribution between the electret layer and the air layer, resulting in an external current. This thesis focuses on the in-plane overlapping-area-change type which has been demonstrated to be MEMS compatible, low in profile and to harvest more power in sub-100 Hz frequency range if compared with its electromagnetic contour parts. Therefore, the electret generator mentioned henceforth refers to in-plane type.

The research object of this research is the rotational electret energy harvester, as an example of electret energy harvesters [51]. Figure 1-14 schematically depicts the low-profile rotational electret energy harvester using PCB. PCB technology is employed for its low parasitic capacitance, low cost and ease of fabrication.

On the rotor substrate, radial interdigital electrodes are formed as the base and the guard electrodes, on which the electret material is uniformly coated. On the stator substrate, same numbers of interdigital electrodes are formed for extracting the induced charges to the external circuit. Note that only electret on the base electrode is charged, whilst electret on the guard electret is not charged. When the rotor is driven by human motion, the relative displacement between rotor and stator changes and so do the induced charges on the collector electrode, resulting in an alternative current through external load R_L.

1. 3. Parasitic capacitance

1. 3. 1. Influence on output power

Parasitic capacitance, which locates parallelly between the generator and load (Figure **1-15**), usually contains the stray capacitance of the generator itself and the introduced capacitance from subsequent power management circuits and/or measurement setup.

Despite that parasitic capacitance is usually in pF range for electret energy harvesters, it restrains the output power of electret energy harvester severely, as illustrated in

Figure 1-16 [52]. Intuitively, parasitic capacitance shunts the charges generated by the generator, thereby a portion of the charges cannot be delivered to the load. In electrical engineering, the power consumed by this parasitic capacitance is defined as reactive power. Although reactive power does no work, the current associated with reactive power still must be supplied by the power source. Since electret generators have quite weak current generation ability (<10 μA), it is sensitive to parasitic capacitance. From a electromechanical point of view, the parasitic capacitance acts as an electrical spring which weakens the electromechanical coupling. Therefore, reducing parasitic capacitance is an effective way to enhance the output power (effectiveness) of electret energy harvesters.

1. 3. 2. Attempts to tackle with parasitic capacitance

Several attempts have been made to reduce parasitic capacitance by structural design. Since parasitic capacitance mainly exists between interdigitated electrodes (Figure 1-17), Masaki et al. developed concave electrodes (Figure 1-18a) to increase the creepy distance between electrodes and hence reduce the parasitic capacitance from 25pF to 17pF. Consequently, the output power (Figure 1-18b) was increased from 40 μW to 100 μW [45]. Chen et al. developed suspended electrodes (Figure 1-19a) to reduce the equivalent permittivity beneath electrodes and hence reduce parasitic capacitance by 36%, resulting in a 35% increase (Figure 1-19b) in the output power [53].

On the other hand, parasitic capacitance can be compensated by an inductor, according to the well-known PFC theory. In this regard, Genda et al. proposed passive LC resonant circuit (Figure 1-20) for electret generator in high-frequency (1 Mrpm) operation. Simulated results (Figure 1-21) showed 80~90% of the theoretical output power (without parasitic capacitance) was recovered with this circuit at resonant frequency [34]. However, this passive approach cannot apply to energy harvesting field where excitation frequency is low and broadly distributed. Firstly, to adapt the resonant frequency of LC circuit to a low frequency, the inductor (value and volume) should be impractically large, as the parasitic capacitance is in pF-range. Secondly, the performance of passive LC circuit deteriorates sharply at off-resonant frequencies, which is unfavorable in energy harvesting application where excitation is broadly distributed in frequency. Therefore, a new design of power management circuit, aiming to compensate parasitic capacitance, is bound to be developed for electret energy harvester.

1. 4. Power management circuits for kinetic energy harvesters

Power management circuit, or interface circuit, is usually inserted between the energy harvester and the load. As shown in Figure 1-22, power management circuit may have two functions: (1) voltage regulation. In electret energy harvester case, it converts the AC fluctuant high voltage to DC stable low voltage for subsequent electronics; (2) conjugate impedance matching. Impedance matching is usually implemented for maximal power transfer, but without conjugate impedance matching, the maximal power is still constrained by parasitic capacitance. Conjugate impedance matching employs an inductive component to compensate parasitic capacitance, thereby booming the maximal achievable power.

The present work focuses on developing a power management circuit which achieves conjugate impedance matching, also known as nonlinear interface circuit, for electret energy harvesters. To distinguish it from conventional power management circuit aiming at voltage regulation, the circuit to be developed here is called interface circuit in this thesis.

Here a literature review of nonlinear interface circuits for other kinetic energy harvesters, mainly piezoelectric ones, is presented first, to get an overview of progress in nonlinear circuit field. Afterwards, a literature review of power management circuits for electret (electrostatic) is presented, to confirm nonlinear circuits have not been explored for electret energy harvesters.

1. 4. 1. Nonlinear interface circuits for piezoelectric energy harvesters

As explained in early section, passive compensation is not practical in energy harvesting field. Therefore, active compensation is explored first in piezoelectric energy harvesting field. The term ‘active’ means it needs additional active components such as switch, which requires additional power, for the compensation.

In 2001, Taylor et al. proposed a concept called switched resonant-power conversion (**Figure 1-23**) for piezoelectric ocean/river power generator [54], which turns out to be the first trial of active compensation in energy harvesting field. It employs an intelligent active switch and an inductor to reverse the voltage across the clamped capacitance synchronously with the voltage source V_{oc}, thereby compensating the shunt capacitance (clamped capacitance in this case). They performed theoretical derivation and simulation. Later in 2005, Guyomar et al proposed a nonlinear interface circuit (Figure 1-24) called SSHI for piezoelectric energy harvester, with rigorous theory and

experimental validation [55]. In a narrow sense, the term ‘nonlinear’ refers to a nonlinear processing achieved by a synchronized switch, which makes the output voltage of piezoelectric disk nonlinear (Figure 1-25). It is called parallel SSHI where a switch-inductor branch is parallelly inserted between generator and load. The switching actions make sure that output voltage and the source current (velocity) always have the same sign. Consequently, their product, the output power is enhanced by several hundred percent (Figure 1-26). This method is especially effective for weakly-coupled piezoelectric energy harvesters since it enhances the electromechanical coupling (effectiveness) of piezoelectric energy harvester significantly.

Following this concept, numerous researches has been conducted to make SSHI more practically attractive, efficient and compact. Lallart et al. reported an envelope-detector-based (free of external displacement sensor) simple low-cost electronic switch (Figure 1-27) to achieve an autonomous switching in a self-powering manner [56]. Krihely et al. proposed a self-contained SSHI-based rectifier (Figure 1-28) to reduce components counts and power consumption in switch control circuitry [57].

In integrated circuit community, SSHI is also called bias-flip circuit. Ramadass et al. reported an efficient bias-flip circuit (Figure 1-29) implemented in a 0.35 μm CMOS process. As a result, 4x power gain was achieved. Recently, Du et al. proposed synchronized switch harvesting on capacitor (SSHC) (Figure 1-30) to replace inductor with an array of capacitors, aiming at making bias-flip circuit fully integrated [58].

Besides aforementioned technical progress, principles of SSHI circuit is also abundantly investigated, including modelling [59][60], performance evaluation [61][62], switching delay effects [63] and choice of switch in main circuit [64]. These papers provide generic knowledge for understanding and improving SSHI performance, which is valuable reference for developing SSHI for electret energy harvester.

In addition to parallel SSHI, other derivative topologies such series-SSHI [65], DSSH (SSHI with buck converter) [66], SSHI-MR [67], pre-biasing[68] are also explored, each of which tackles with a particular problem. All of the nonlinear circuits mentioned above feature in synchronously inverting the voltage across the shunt capacitance. In addition, in these approaches the generator is directly connected to the load/storage stage, hence the harvested power is usually load dependent. If the switch is not placed in the main power transferring path, self-powering is usually easier to achieve, by using the stored energy in the parallel SSHI. However, in real-world sensor

node application, the load is usually time-varying (sleep mode, RF transmission, etc.). Therefore, it is interesting to develop load-independent interface circuits.

In this regard, another group of load-decoupling nonlinear circuits are also investigated. The load-decoupling is usually realized by using an inductor as an energy intermediate between the generator and the storage capacitor. Lefeuvre et al. proposed SECE circuit (Figure 1-31) in 2005 [69]. As shown in Figure 1-31, the synchronized switch is turned on at displacement extremums of the piezoelectric cantilever, converting the electrostatic energy stored in the internal capacitor into magnetic energy in the coil. The switch is then turned off at voltage zero-crossing points. Afterwards, the magnetic energy in that coil is freewheeled to the load. In this way, the shunting effect is weakened (Figure 1-32). Theoretically, it achieves 4x power enhancement regardless of load resistance (Figure 1-33).

Actually, SECE can be viewed as a conventional flyback converter [70] where the switch is synchronized with the behavior of the generator at input. Therefore, it simultaneously achieves both voltage regulation and conjugate impedance matching. Potentially, SECE may have fewer components (inductors) if compared with SSHI, because SSHI requires additional DC/DC converter.

Later in 2008, Wu et al. proposed SSCDI circuit (Figure 1-34). Compared with SECE, the topology of SSDCI is a buck converter instead of a flyback converter. Therefore, the transformer in original SECE is not required. The working principle of SSDCI is almost the same as SECE. Therefore, the power enhancing ratio of SSDCI retains 4 in the ideal case. When the losses in the circuit (especially the loss in LC resonator) are considered, the power enhancing performance is shown in Figure 1-35. Below a critical load voltage, the performance shows load independence like SECE. The load dependence in very low load voltage is caused by the circuit loss. Above the critical voltage, the discharging of the internal capacitor is not sufficient because the load voltage is high.

Despite the merits mentioned above, the switch control of SECE/SSDCI is more complex than SSHI [71], especially for turning off the switch at voltage zero-crossing points. Although discharging of the internal capacitor is naturally cut off by the rectifier, the switch still needs to be turned off at voltage zero-crossings, to avoid short circuit during the next charging phase. The difficulty of switching off lies in the detection of voltage zero-crossing points bidirectionally. Since the voltage shall cross zero in both directions (positive to negative, or vice versa), a threshold voltage with either polarity

(say, -5 mV) for zero-crossing detection will lose accuracy for the next detection when the voltage drops in the other direction (say, negative to positive). A conventional single-polarity zero-crossing detector usually led to imperfect voltage waveforms which deteriorates the power enhancing performance, as shown in [72].

In early implementations with discreet components, the switch drive signals are generated by external sensors[69][73], which is unfavorable for miniature devices. In 2013, Wu et al. proposed optimized synchronous electric charge extraction (OSECE), which achieves better power enhancing performance than SECE, with simplified switch control strategy (as simple as that in SSHI), but 3 coupled coils are required in practical implementation [74]. Recently, Morel et al. developed a dual-mode comparator, which addressed the switching-off issue by dynamically changing the polarity of the threshold voltage in the zero-crossing comparator[75]. But this IC-based method is a little bit complex to realize. For reliability, fixed on-duration switch is also employed [76], but it is not adaptive to internal capacitance and external inductors, and hence loses accuracy with device aging.

In addition, self-powering and cold-start of SECE are also not straightforward as those in parallel SSHI, because the generator and the load is separated by a normally-off switch. Therefore, an additional generator-to-storage branch (Figure 1-36) is usually inserted parallelly with SECE main circuit for start-up [77][78]. For SSDCI which features buck converter topology, at least one floating switch is necessary to make the load have the same ground with the switch [75][73]. It is difficult to make this switch energy-efficient when the generator outputs high voltage, like in the electret generator case. Photo-coupled floating switch is utilized in [73], but it usually consumes mW-level power. For OSECE, the switch unit is forwardly powered by the generator, therefore self-powering is achieved without using the energy storage at load end. Self-powered OSECE is reported in [79].

Most of the SECE-based circuits mentioned above are intended for piezoelectric energy harvesters outputting low voltage (<10V). Surprisingly, Gasnier et al. developed Multi-Shot SECE to handle very high voltages (>100V) in piezoelectric energy harvesters, with a fully autonomous IC circuit and off-chip components [77]. The discharging phase is spilt into several shots for efficient energy conversion from the internal capacitor with high voltage to the coil. This pioneer work provides valuable reference for electret-based energy harvesters which also features high output voltage.

Recently, Short-Circuit SECE [80] and N-SECE [81]strategy are proposed to optimize the output power and bandwidth and of highly-coupled piezoelectric energy harvesters. Although it is interesting to include the electromechanical coupling of the generator in the discussion of nonlinear circuits [82][83], it is out of the scope of this thesis. Because the mechanical behavior of rotational electret energy harvester is still under investigation [84]. The present work mainly focuses on the power enhancing prospective under fixed displacement/rotational speed condition.

Generally, both SECE and SSHI features in synchronized switch. But the function of the inductor in each case is different. In SSHI, the inductor serves just for inverting the charges across the shunt capacitor, without holding the main power generated by energy harvester. In SECE, however, the inductor acts as an energy intermediate; it converts the electrostatic energy stored in shunt capacitor into electromagnetic energy and stores the energy before releasing to load. Thanks to this decoupling inductor, the performance of SECE is load independent. Meanwhile, SSHI exhibits higher power enhancing ability in a load dependent manner. From a perspective of electrical engineering, SSHI is an active power factor correction approach; whilst SECE is a synchronous flyback/buck converter. Both of them enhance the electromechanical coupling of the energy harvester by weakening shunt effect of the internal capacitance, thereby achieving significant output power increase for weakly-coupled energy harvesters. Technically, they differ in the switch control scheme and self-powering strategies. More detailed comparison between these interface circuits is carried out in [71][85][86](Figure 1-37). To summarize, both SSHI and SECE are valuable candidates for enhancing the power output of electret-based energy harvesters.

1. 4. 2. Power management circuits for electret/electrostatic energy harvesters

So far, circuit design for electret-based EHs has not been explored as much as that for piezoelectric ones. In early applications, full-bridge rectifier was employed for its simplicity and reliability[45]. Later, High-efficiency (85%) ASIC buck converters with high input voltage (60V) were developed in [87][88], with MPPT algorithm to achieve maximal power transfer. But the switch inside their buck converter are not synchronized with generator motion, therefore their circuits do not serve the purpose of conjugate impedance matching for enhancing output power (Figure 1-38).

In gap-closing electrostatic generators, the converter circuit needs to extract the charges stored in the internal capacitor at voltage maximums to the inductor. In this

sense, the converter in gap-closing electrostatic energy harvesters behaves like SECE. Therefore, the knowledge earned in this aspect should provide value reference for developing SECE for electret generator, because both types of generator feature low internal capacitance and high output voltage. In 2006, Stark et al. shed insights on circuit design, semiconductor device selection and analysis of parasitics for micro power gap-closing electrostatic energy harvester [89]. In their case, the generator generates pulses of 250V on a 10-pF capacitor. The circuit needs to convet this energy to a low voltage. They found that the effects of leakage and parasitic stored charges are important. Recently, Perez et al. developed SECE circuit for a electret-based gap-closing energy harvester [90][76], reporting a 50% conversion efficiency.

In a broader sense, triboelectric energy harvesters are also based on electrostatic induction. Therefore, the circuit design for triboelectric generators is also reviewed here. Park et al. developed dual-input buck converter with 70V voltage toleration and 70% end-to-end efficiency[91][92]. Figure 1-39 shows a comparison of high voltage ASICs intended for electrostatic/triboelectric energy harvesters. It reveals that even though electret/electrostatic/triboelectric generators exhibit high voltages, it might still be compatible with IC by utilizing high voltage process. With discrete components, Zhang et al. reported a buck converter which handles 450V peak voltage of the triboelectric generator [93]. This high-voltage toleration is achieved by using a mechanical switch, instead of electronic switch, in the buck converter. Moreover, the turning-on of this switch is achieved by point discharge instead of contact. As a result, the efficiency is around 30% for this energy transfer.

Nonlinear circuits for triboelectric generators are reported lately. In 2019, Li et al. proposed a SSHI rectifier for triboelectric gap-closing energy harvester[94], reporting a 242.86% power increase over full-bridge rectifier. In 2019, Cao et al. proposed a SECE-like circuit for in-plane triboelectric energy harvester [95]. In 2019, Xu et al. proposed SSHI-based circuits for in-plane triboelectric generators[96]. These papers proved that nonlinear circuit could be applicable on triboelectric generators experimentally, but their circuit design is not close to practical application in terms of in-situ switch control and self-powering issues.

To summarize, synchronized-switch-based nonlinear circuits are still not explored for electret-based in-plane energy harvesters. Experiences in the circuit design of other electrostatic/triboelectric energy harvesters have provided important knowledge in

dealing with low current, low internal capacitance and high output voltage, but there is still much room to further explore new understandings about it.

1. 5. Objective

1. 5. 1. Objective and approaches

The present study attempts to develop nonlinear circuits for electret-based energy harvester, aiming at enhancing its output power. The objective of the present study is to present new approaches to optimize energy conversion from kinetic energy (human motion) using rotational electret energy harvester and to describe the most important parameters in circuit design. Circuit analysis of the proposed circuits is to be carried out to provide guidance for improving the performance

In addition, the present study also aims to develop a low-profile circuit which is favor of wearable applications. Since the rotational electret energy harvester [38] is only 3.3 mm thick, the height of the proposed circuit should not be higher. Usually, the inductor employed in the circuit such as SSHI dominates the height, and relatively-large inductance is necessary for high power enhancement. Therefore, there will be a trade-off between the size of inductor and the power enhancement of the proposed circuit. Therefore, circuit analysis is also to be conducted to optimize the volume of the selected inductor. Moreover, the compatibility of the proposed circuits to IC technology is also to be investigated in the present study, aiming at minimizing the area of the proposed circuit.

The approaches employed in the present study include mathematical modelling, SPICE-based circuit simulation, MEMS fabrication and experimental validation with discrete components.

1. 5. 2. Outline

Contents in this thesis are arranged as follows:

In Chapter 1, previous studies on electret-based in-plane energy harvesting and nonlinear circuits have been reviewed, respectively. It reveals that there has been no existing study focusing on nonlinear circuits for electret-based in-plane energy harvester. The objective of this thesis has been presented.

In Chapter 2, a generator model is proposed based on the 1-dimentional model of electret-based in-plane energy harvester. It reveals that electret energy harvester behaves similar to the piezoelectric energy harvester, which confirms the applicability

of nonlinear power management circuits on electret-based energy harvester. A circuit-model-based comparison between electret and piezoelectric EHs is presented to identify challenges of implementing nonlinear circuits on electret EH.

In Chapter 3, development of SSHI for rotational electret energy harvester is presented. Firstly, the theoretical performance of SSHI on electret EH is derived and then verified by simulation with LTspice. Circuit design of parallel SSHI is then proposed using a resistive voltage divider as low-voltage signal generator. Based on this voltage-divider SSHI design, experimental validation based on a test bench of electret-based energy harvester is carried out using discrete components. In this case, the control block is powered by external supply. Since the simulated results are in accordance with experimental results, SSHI performance evaluation, in terms of voltage inversion ratio and circuit efficiency, is carried out based on simulation. As a result, the voltage-divider and diodes in rectifier turned out to be quite lossy at high voltage range where better SSHI performance locates.

In Chapter 4, a novel dual-stage electrode design is proposed to achieve efficient SSHI. The proposed dual-stage electrode aims to reduce power loss by replacing the lossy voltage divider. Experimental validation of dual-stage SSHI is carried out. Self-powered SSHI is then examined with a dual-polarity converter to make the system energetically closed. However, the power enhancing ratio reduces to 1.4 in self-powered SSHI, due to the low voltage rating and low efficiency of this converter. In addition, implementation of dual-stage SSHI on a fully-integrated electret EH, instead of test bench, is presented. It confirms the cold-start and self-powering ability of the proposed dual-stage SSHI circuit under random excitation.

In Chapter 5, development of dual-stage SECE for rotational electret energy harvester is presented. Compared with SSHI, SECE is free of dual-polarity rectifier and harvests more power in a lower load-voltage range. Therefore, a higher overall power enhancing performance is expected with SECE. Firstly, the theoretical performance of SECE on electret EH is derived and then verified by simulation with LTspice. Circuit design of SECE is then proposed featuring a switch control scheme which is adaptive to arbitrary internal capacitance and external inductor. Test-bench-based experimental validation is carried out with control block externally powered. In addition, a performance evaluation of SECE based on simulation is carried out.

In Chapter 6, a PCB-based compact circuit design of dual-stage SECE is presented. The IC compatibility of the proposed SSHI/SECE circuits are investigated. In addition,

an IC-friendly self-powered SSHI with tri-stage design is proposed. These preliminary investigations indicate the direction of future work towards low-profile IC-friendly nonlinear circuits.

The conclusions are given in Chapter 7.

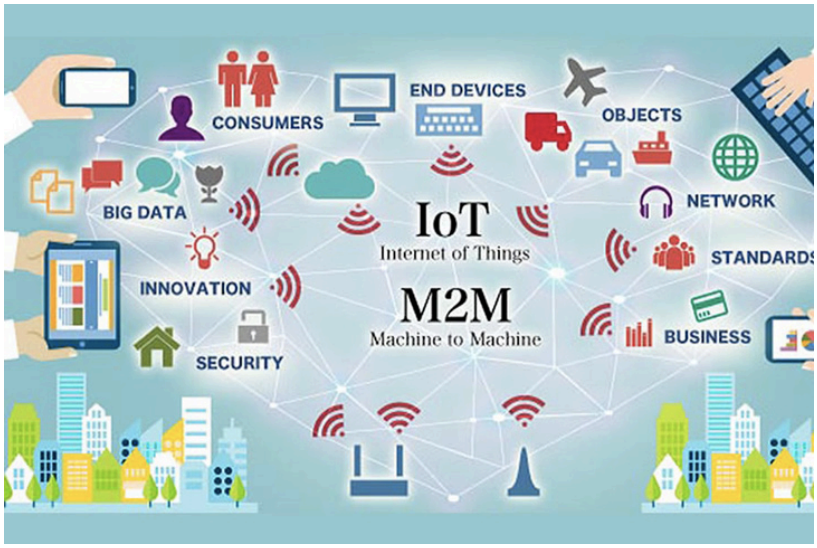


Figure 1-1 Internet of things [1].

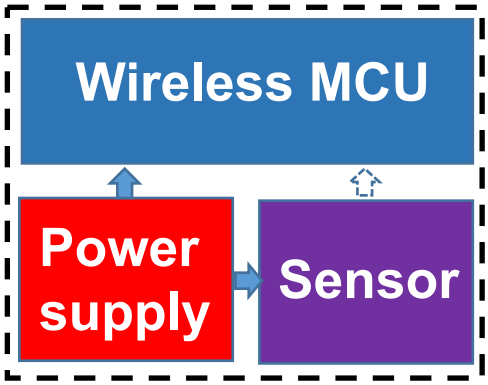


Figure 1-2 Wireless sensor node.

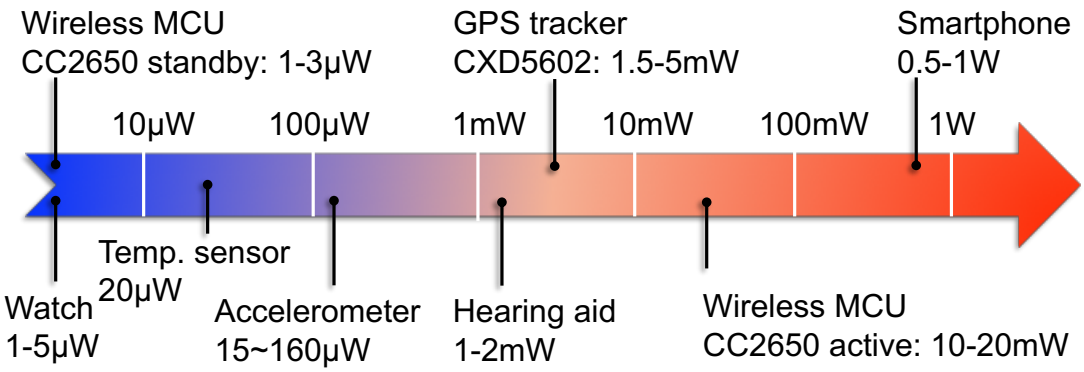


Figure 1-3 Typical power consumption of each component in a WSN.

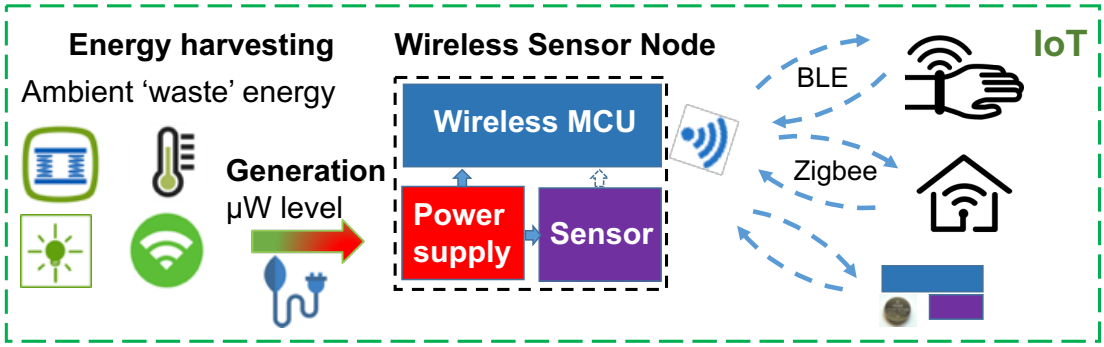


Figure 1-4 Energy harvesting for wireless sensor nodes in IoT.

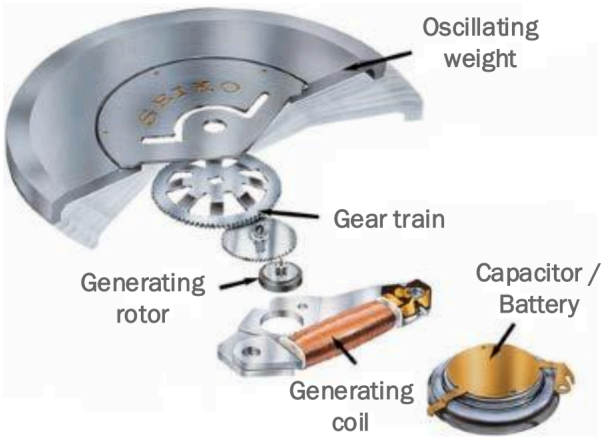


Figure 1-5 Seiko kinetic watch [8].

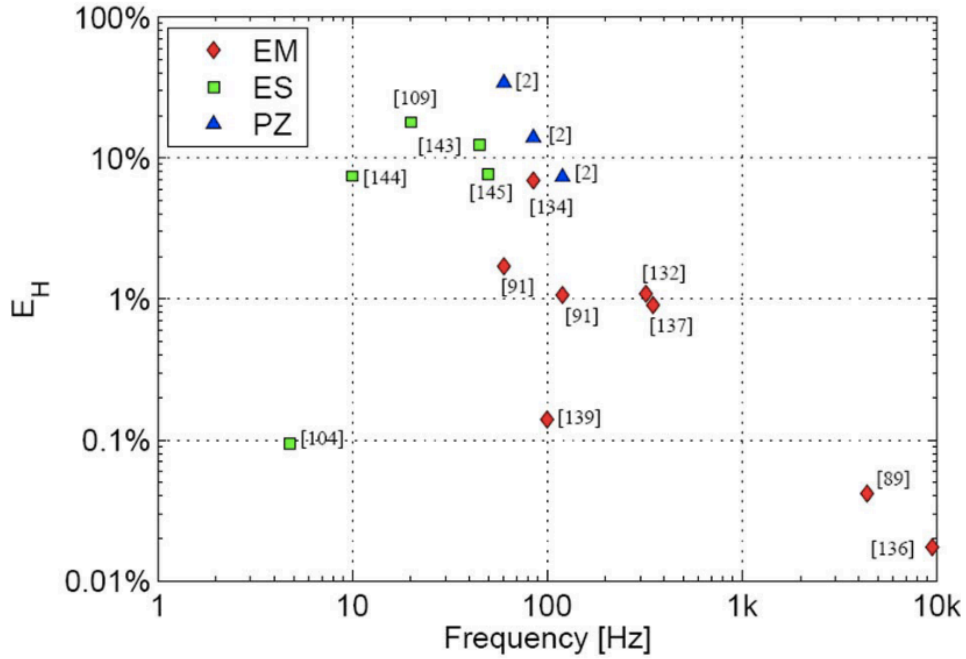
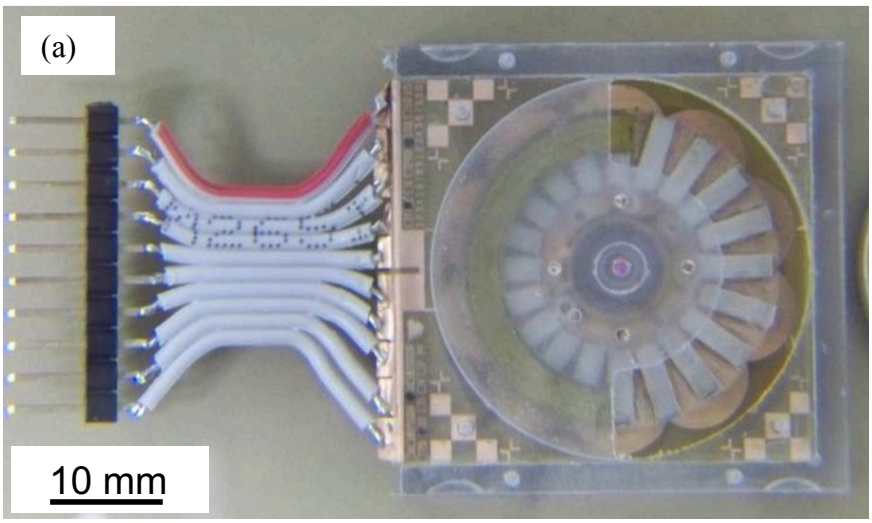


Figure 1-6 Harvester effectiveness of reported devices versus operating frequency [9].



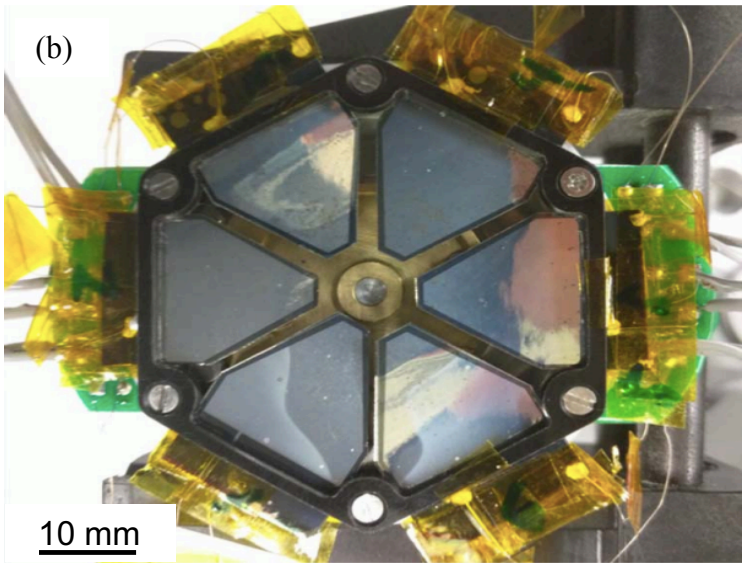


Figure 1-7 Rotational energy harvesters for human motion. (a) Electromagnetic [23], (b) Piezoelectric [24], (c) Electrostatic (electret) [25].

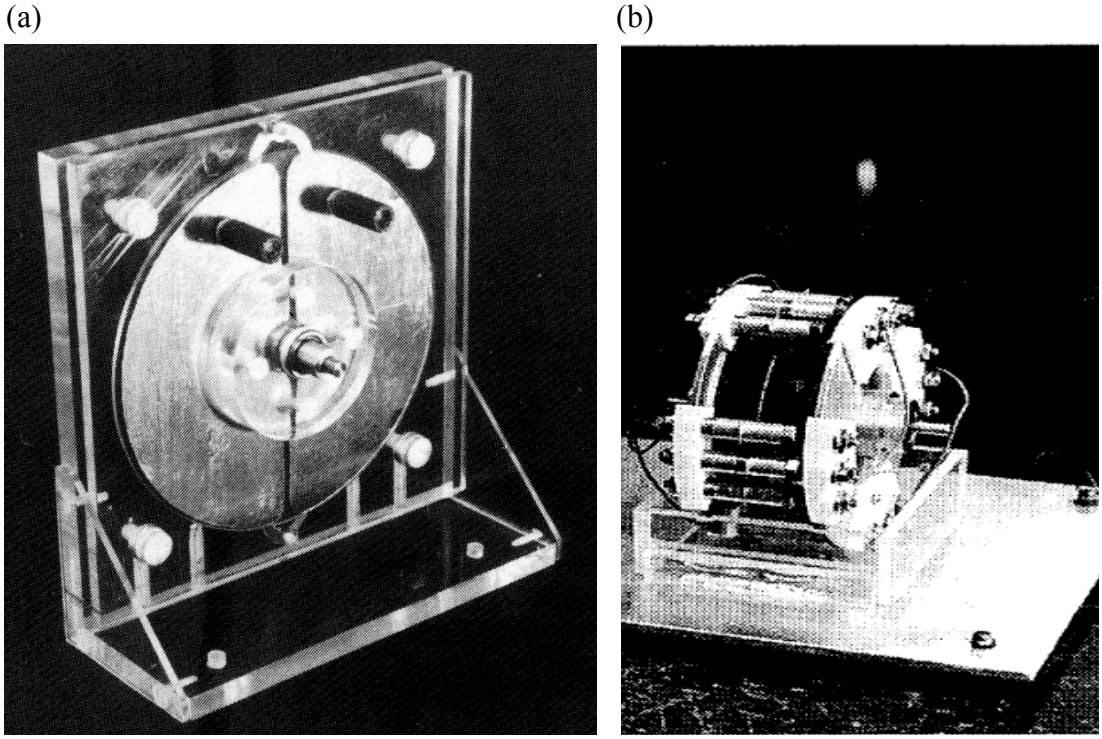


Figure 1-8 The first-generation electret generators by (a) Jefimenko et al. [30] and (b) Tada [31].

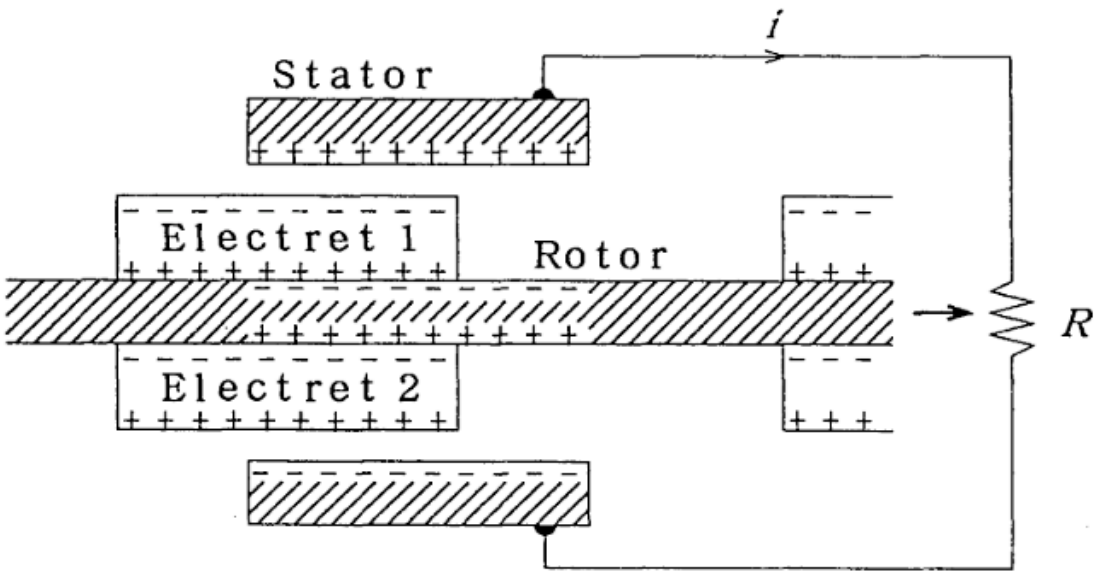


Figure 1-9 Model of an electret generator [31].

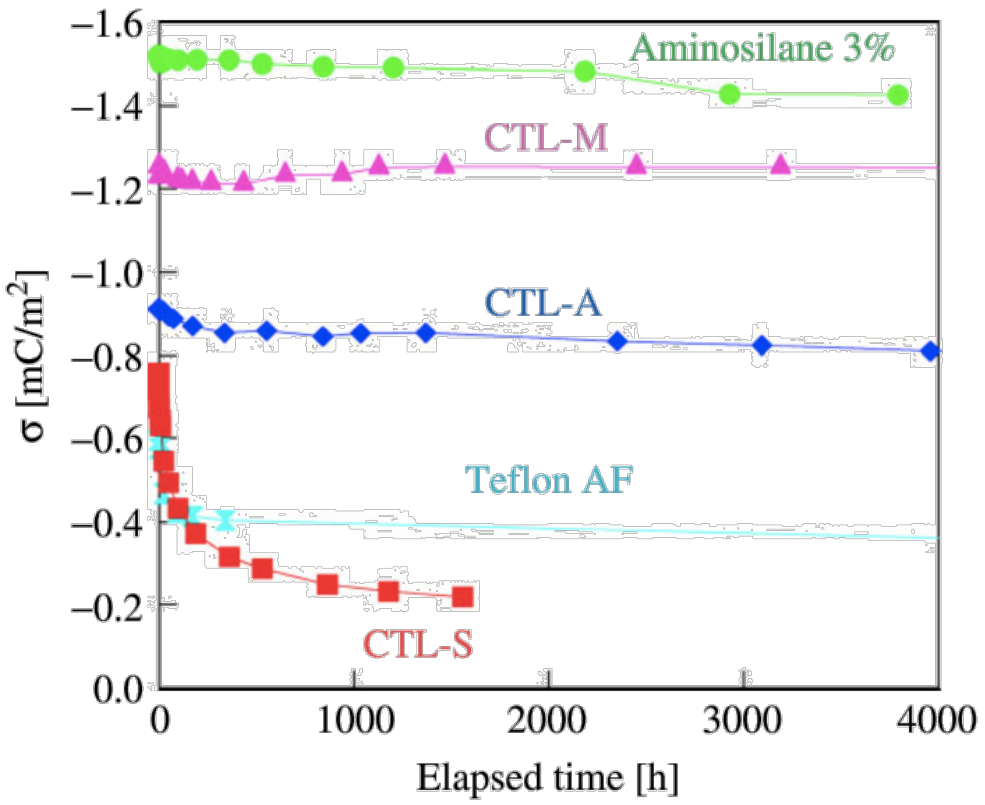


Figure 1-10 Surface charge density vs elapsed time for electret materials [35].

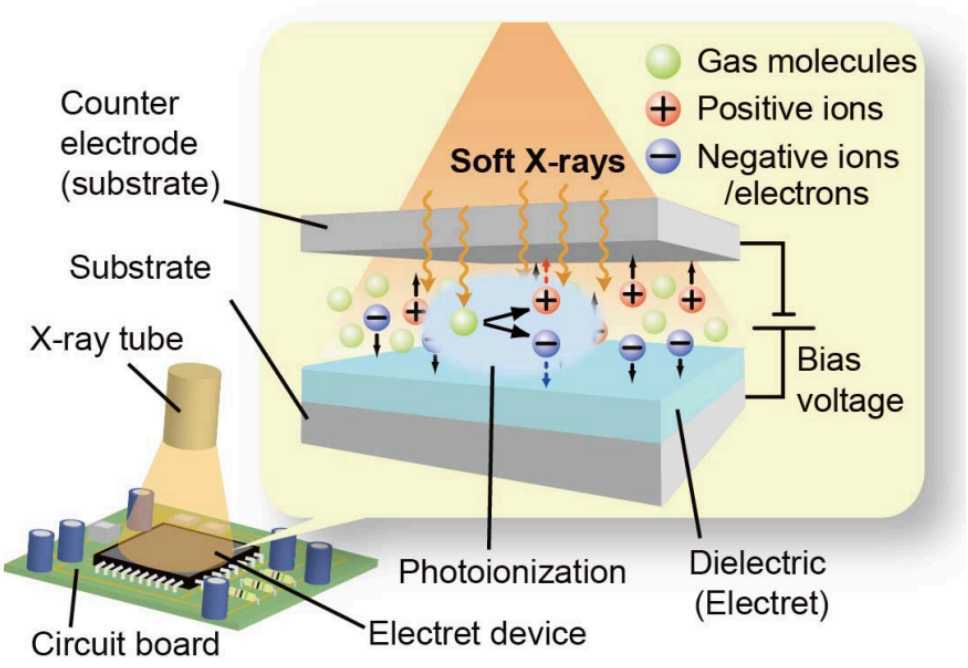


Figure 1-11 Soft X-ray charging of electrets embedded in MEMS devices[36].

Figure 1-12 A fully-integrated linear-vibration electret energy harvester [45].

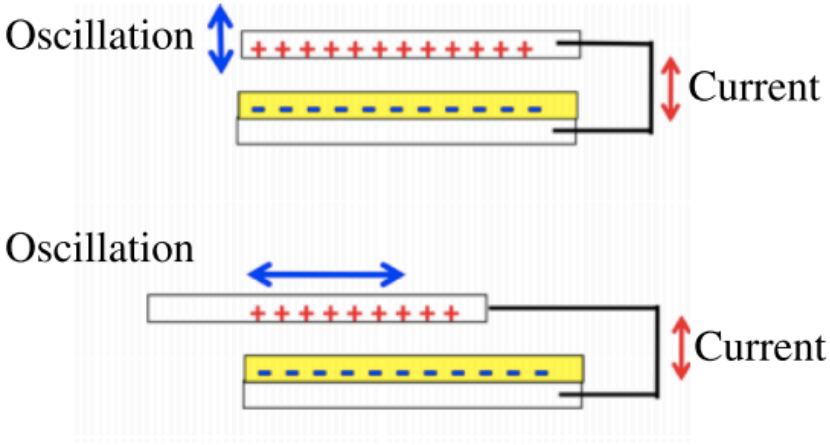


Figure 1-13 Different types of electret-based energy harvesters [97]. (a) gap-closing, (b) in-plane overlapping-area-change.

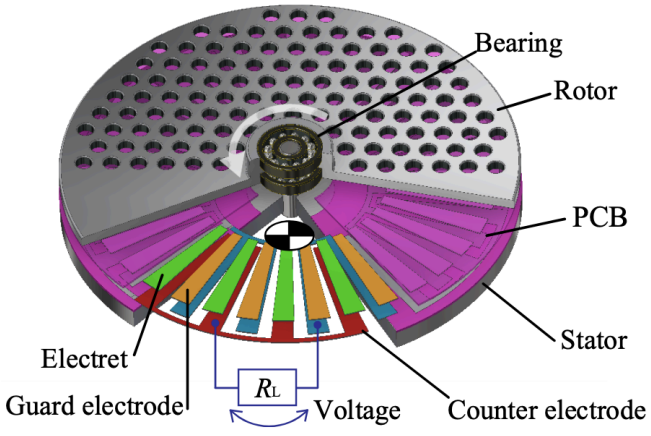


Figure 1-14 Schematic of rotational electret energy harvester [51] .

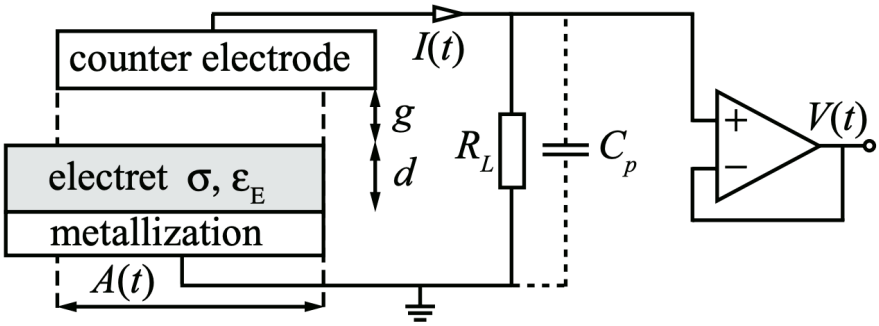


Figure 1-15 Parasitic capacitance in parallel with electret-based energy harvester [52].

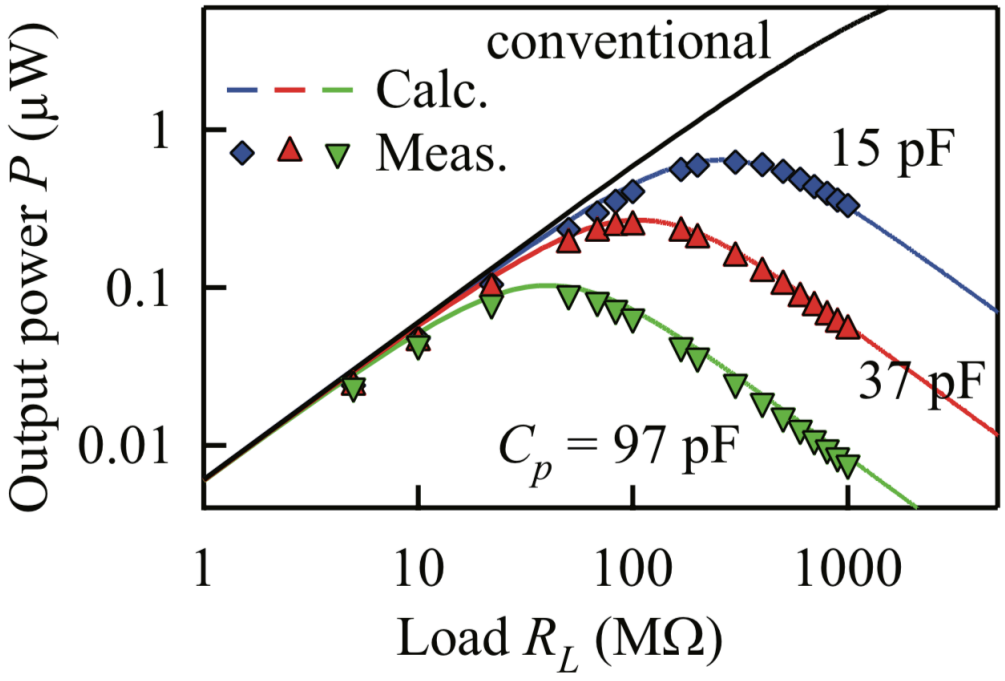


Figure 1-16 Influence of parasitic capacitance on output power[52].

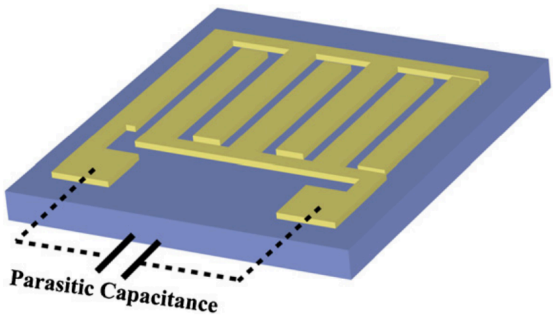


Figure 1-17 Parasitic capacitance between interdigital electrodes[53].

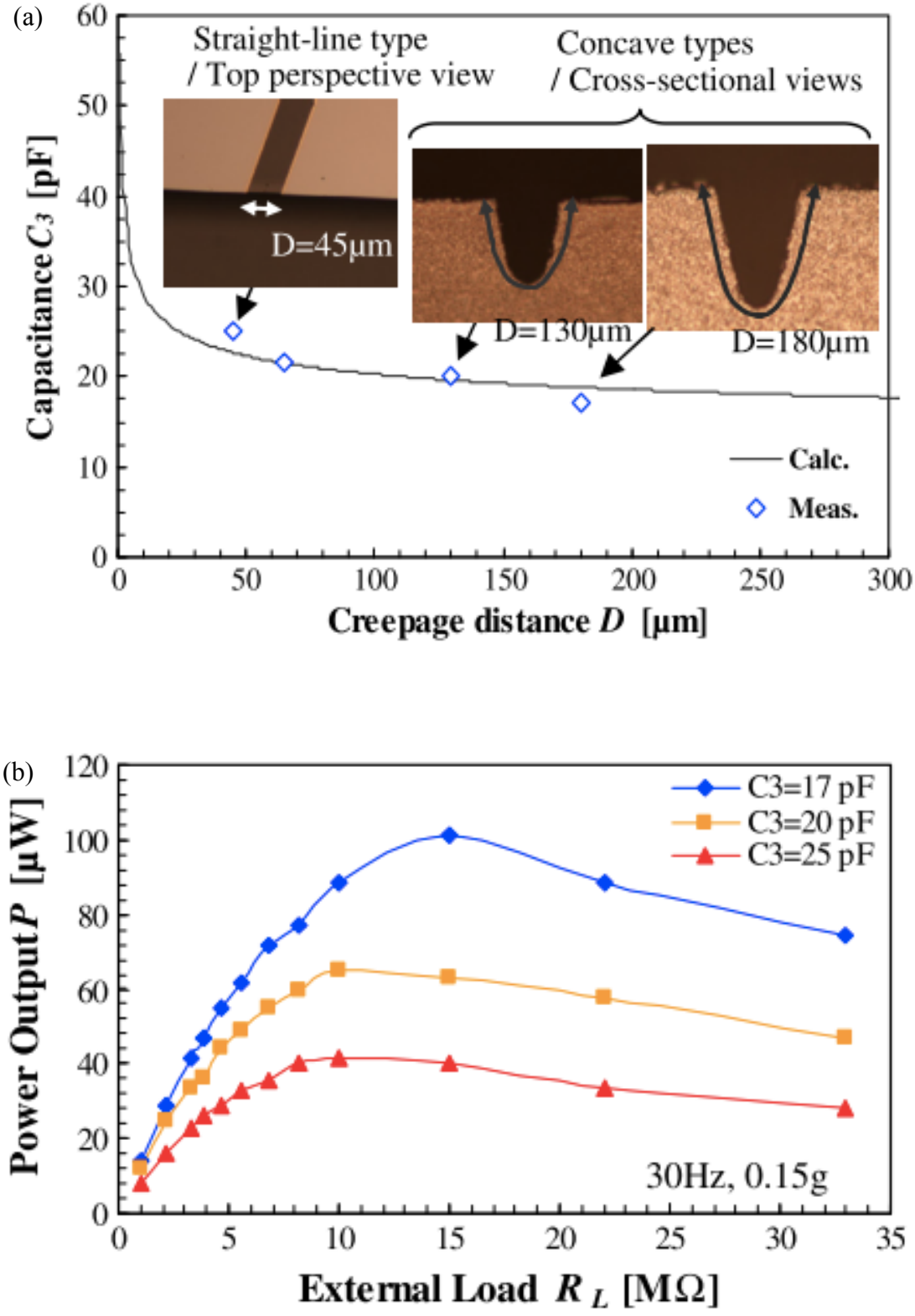


Figure 1-18 Trench between electrodes to reduce parasitic capacitance, (a) trench between electrodes (b) output power of electret energy harvester with reduced parasitic capacitance [45].

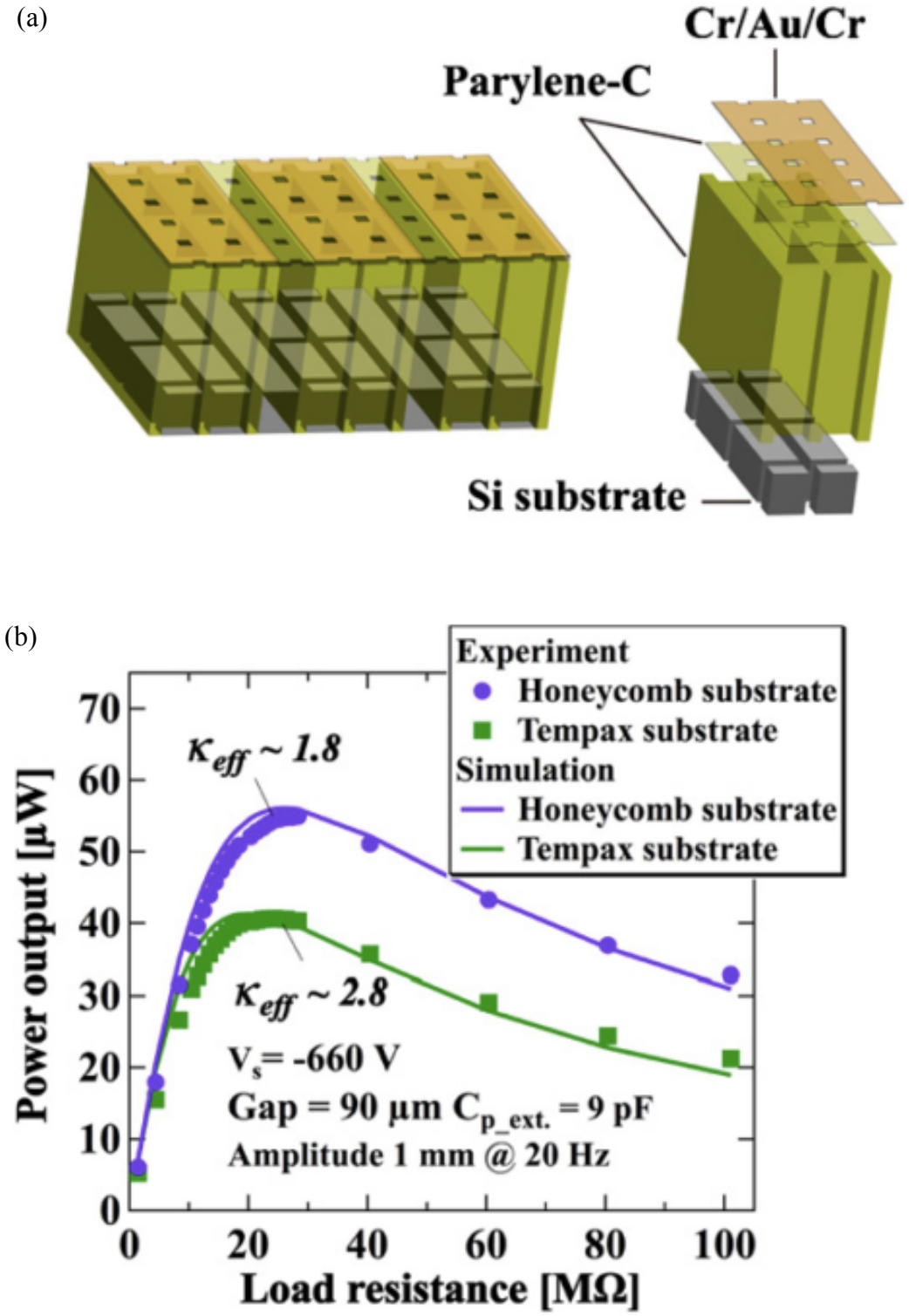


Figure 1-19 Suspended electrodes to reduce parasitic capacitance, (a) suspended electrode design, (b) output power with reduced capacitance [53].

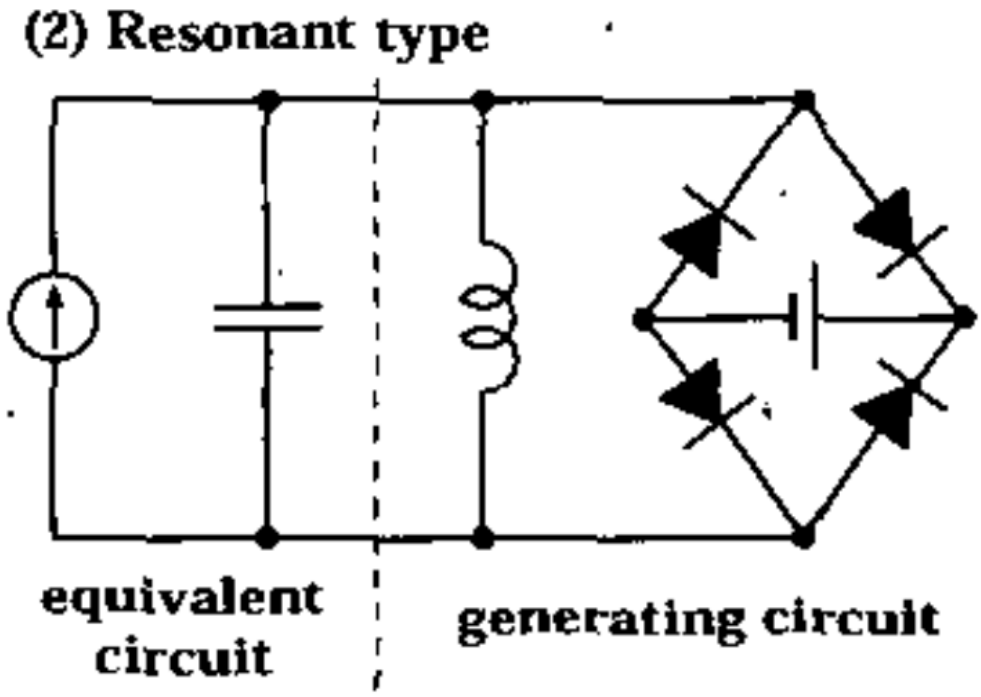


Figure 1-20 Electret-based high-frequency generator with passive LC resonant circuit [34].

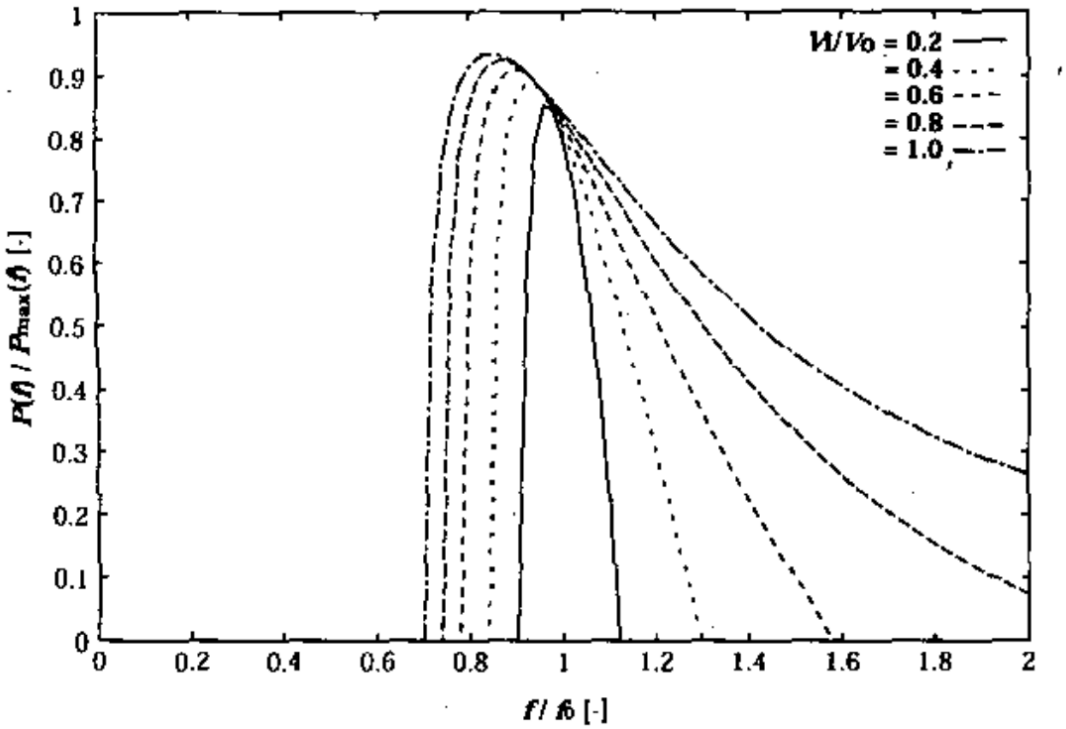


Figure 1-21 Output power vs frequency with passive LC circuit[34].

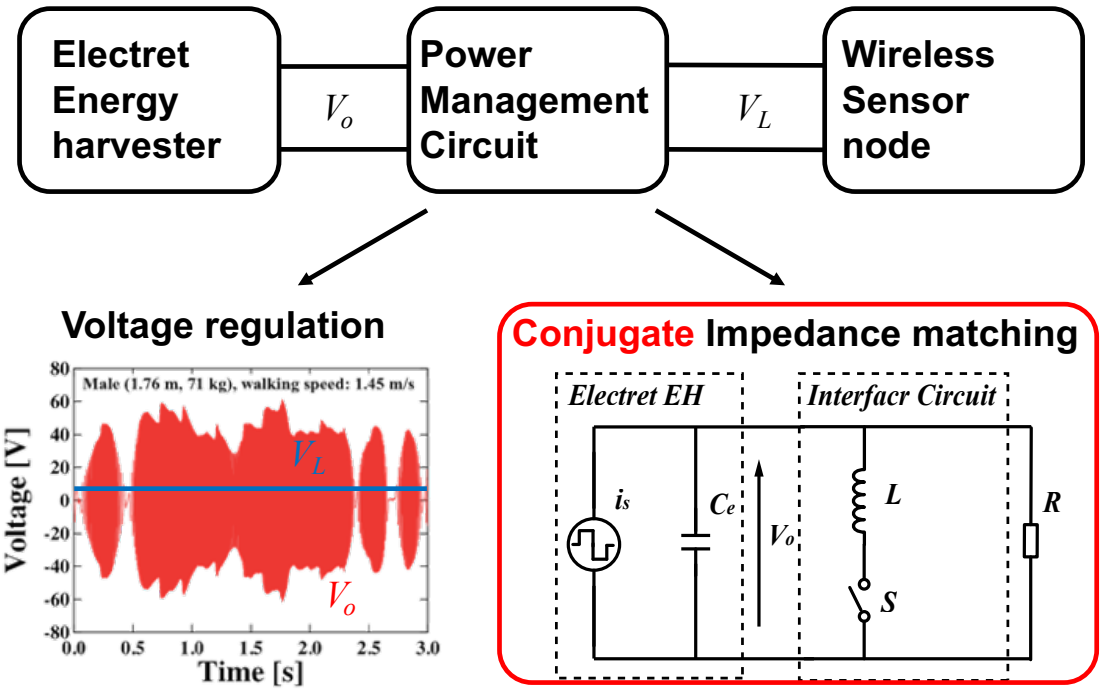


Figure 1-22 Power management circuit and its functions.

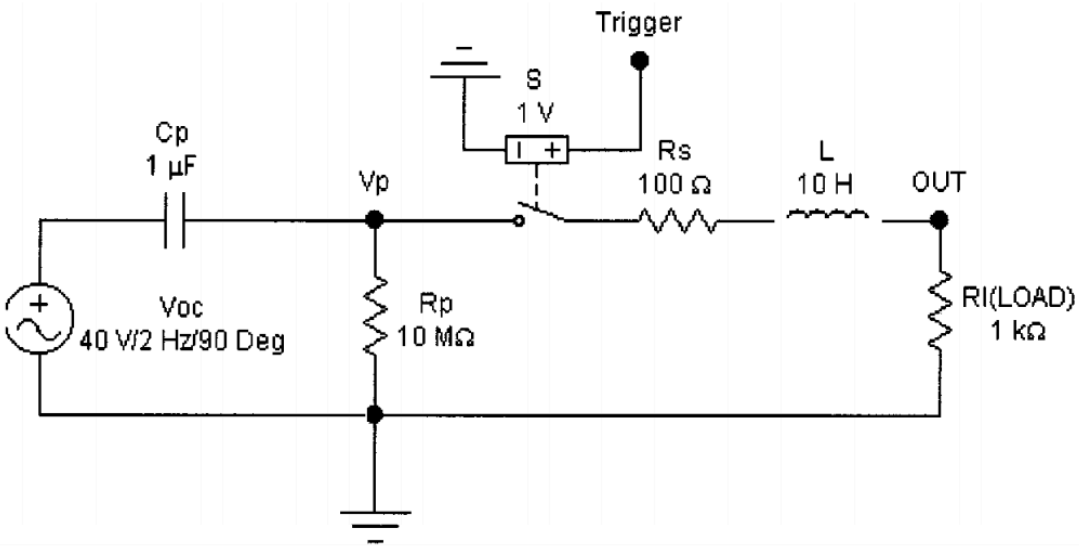


Figure 1-23 Switched resonant-power converter [54].

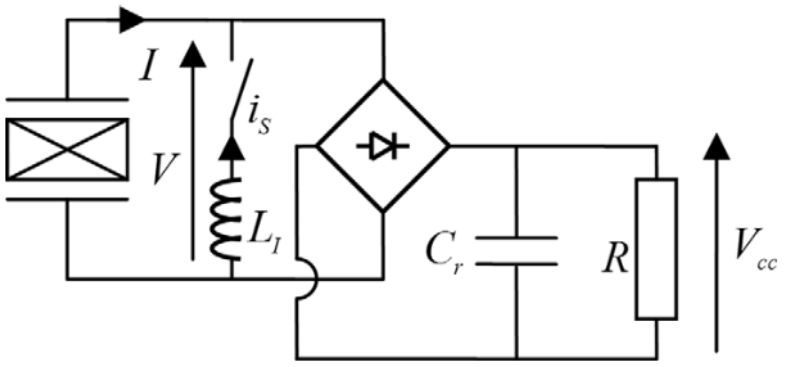


Figure 1-24 Parallel SSHI for piezoelectric energy harvester [55].

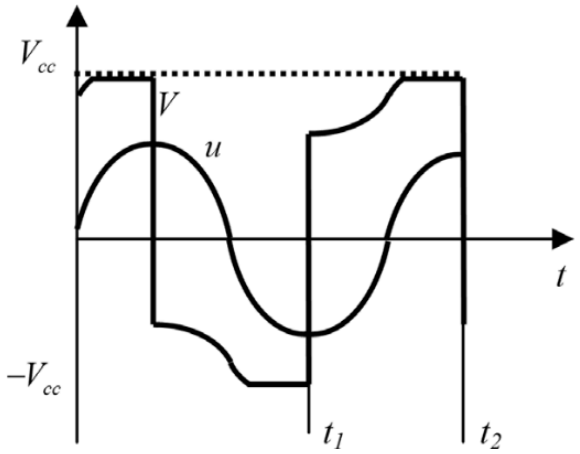


Figure 1-25 Typical voltage and displacement waveforms in SSHI [55].

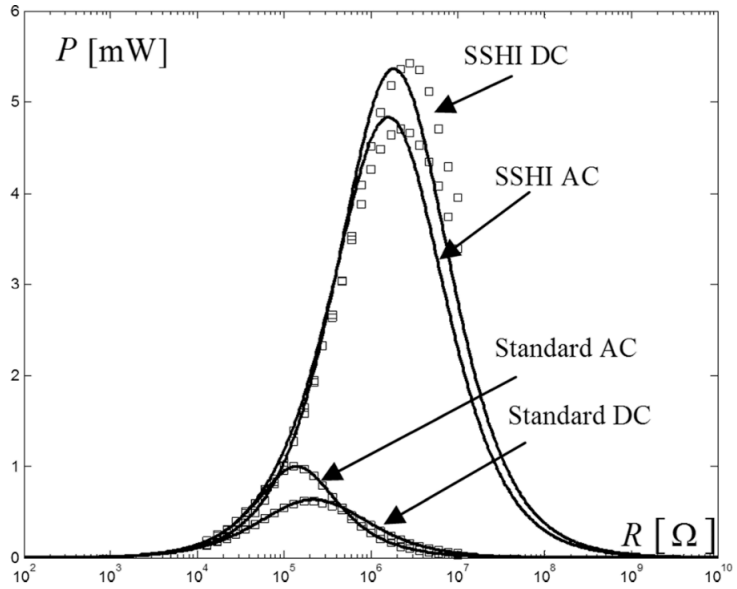


Figure 1-26 Output power of piezoelectric generator as a function of load [55].

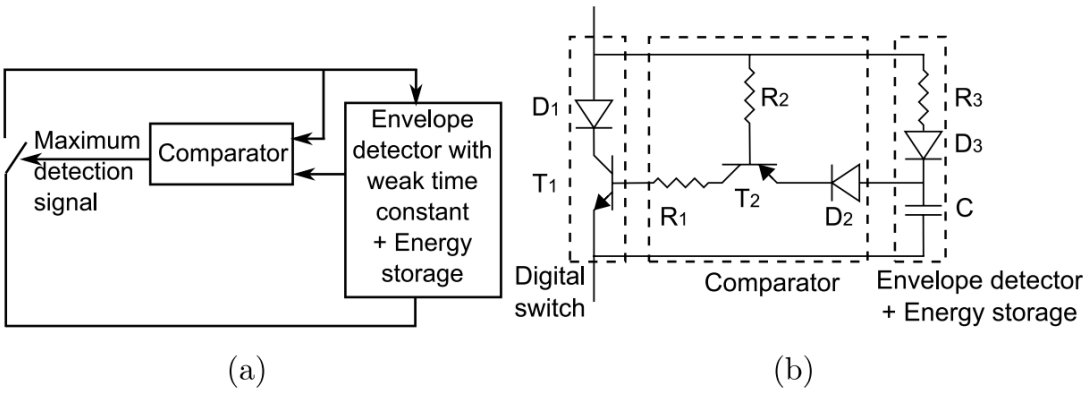


Figure 1-27 Electronic switch for self-powered operation of SSHI [98].

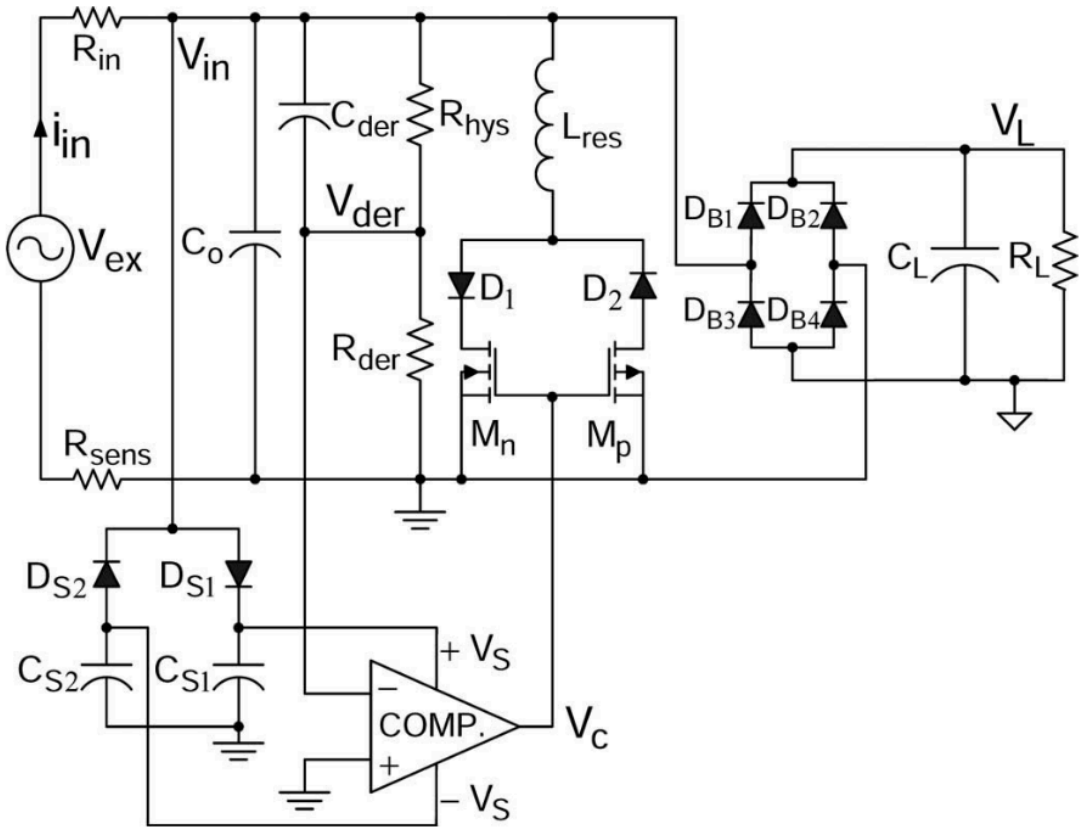


Figure 1-28 Self-contained SSHI circuit [57].

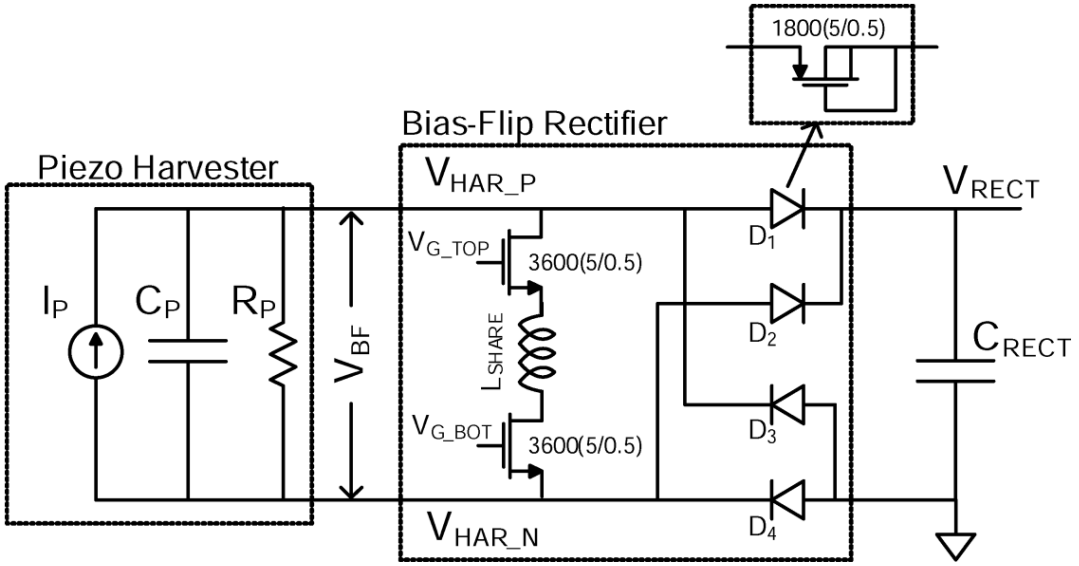


Figure 1-29 Bias-flip rectifier [99].

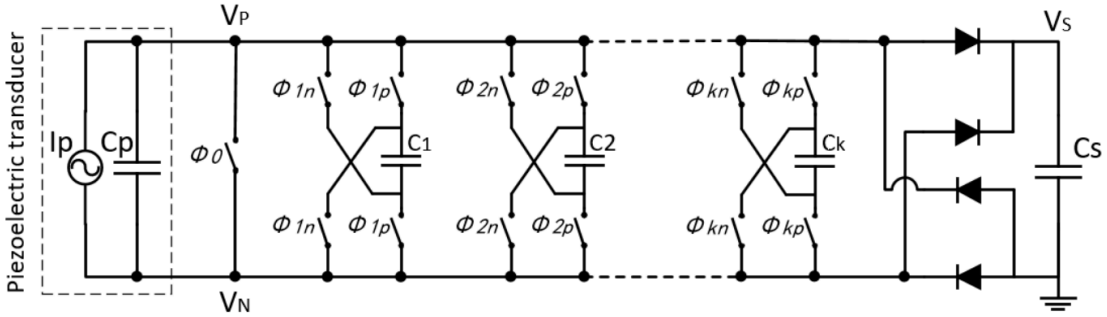


Figure 1-30 SSHC circuit to release the dependence on inductor [58].

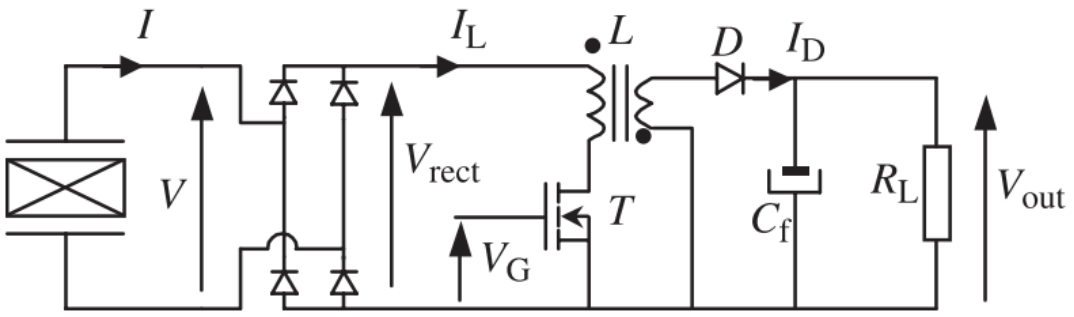


Figure 1-31 Synchronous electric charge extraction [69].

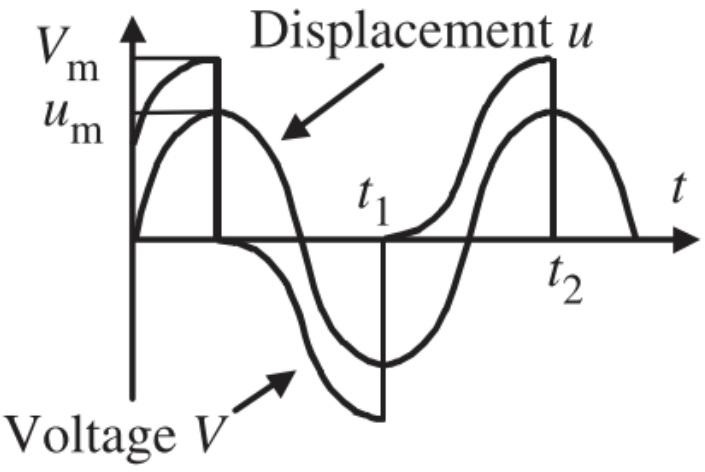


Figure 1-32 Typical waveforms in SECE [69].

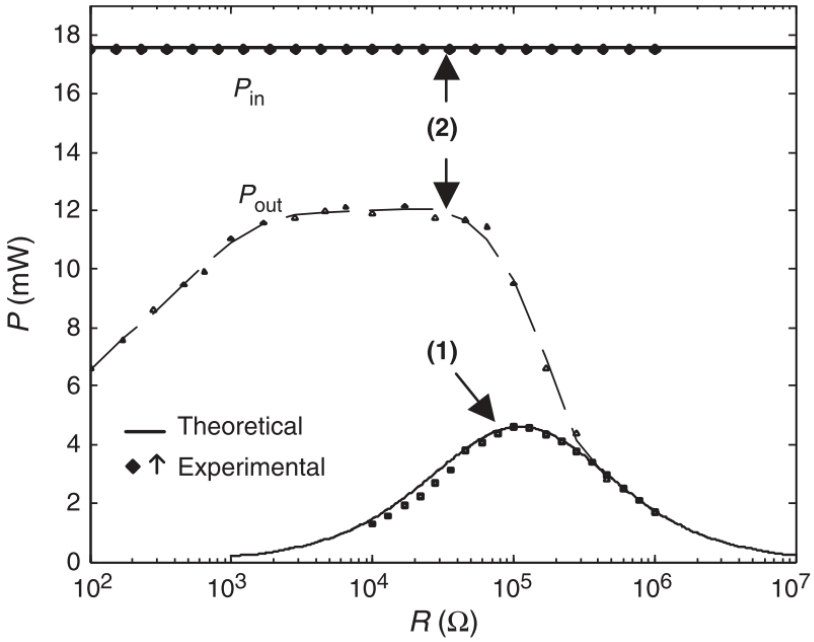


Figure 1-33 Output power vs load in (1) standard and (2) SECE (P_{in}: generator output, P_{out}: output of DC/DC converter) [69].

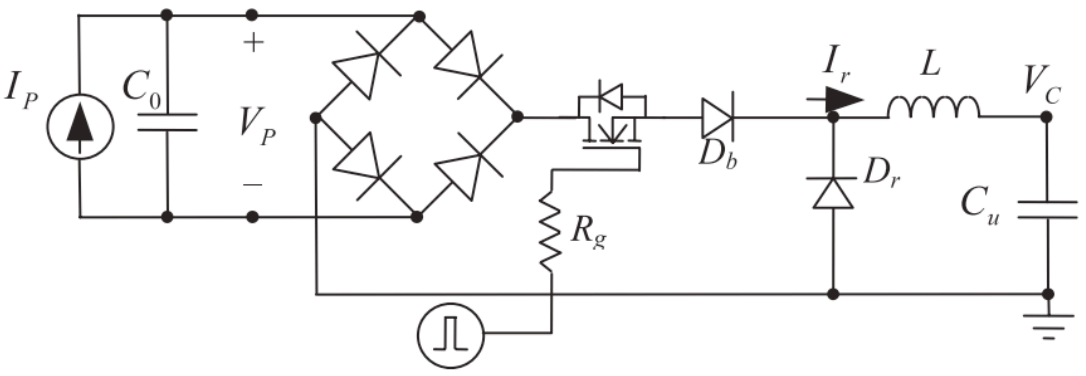


Figure 1-34 SSDCI circuit diagram[73].

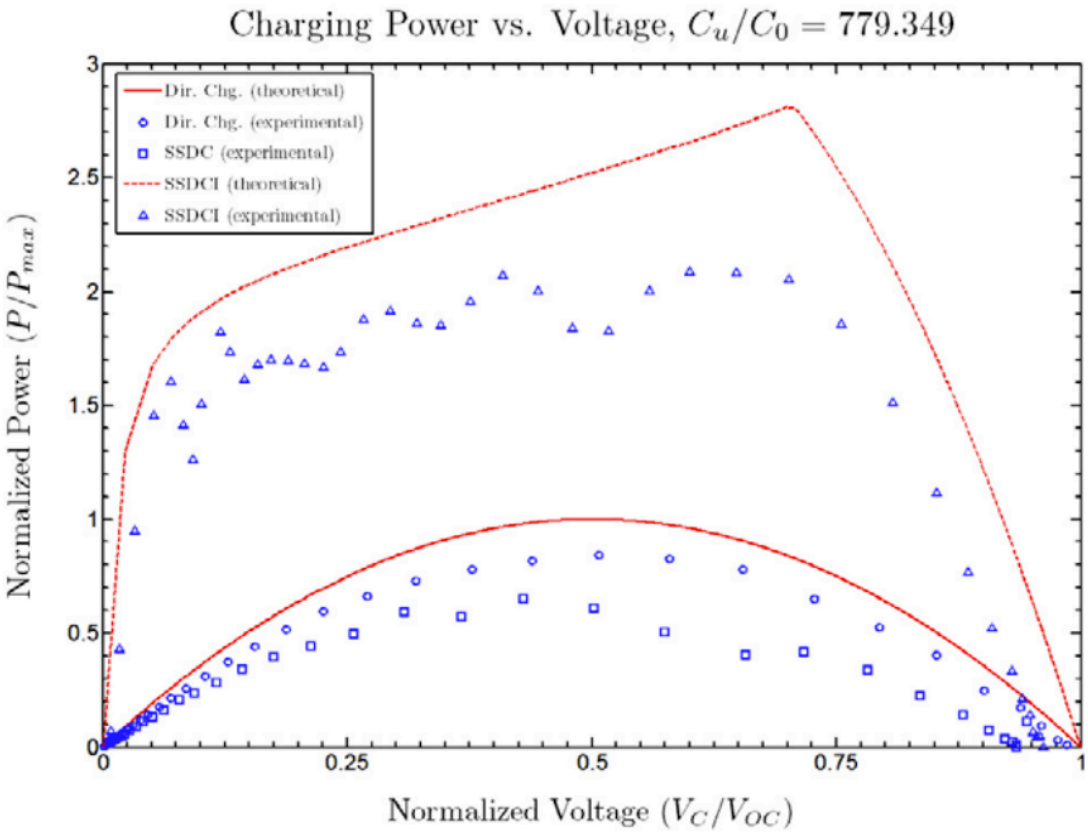


Figure 1-35 Charging power versus voltage in SSDCI case (Q=2.6) [73].

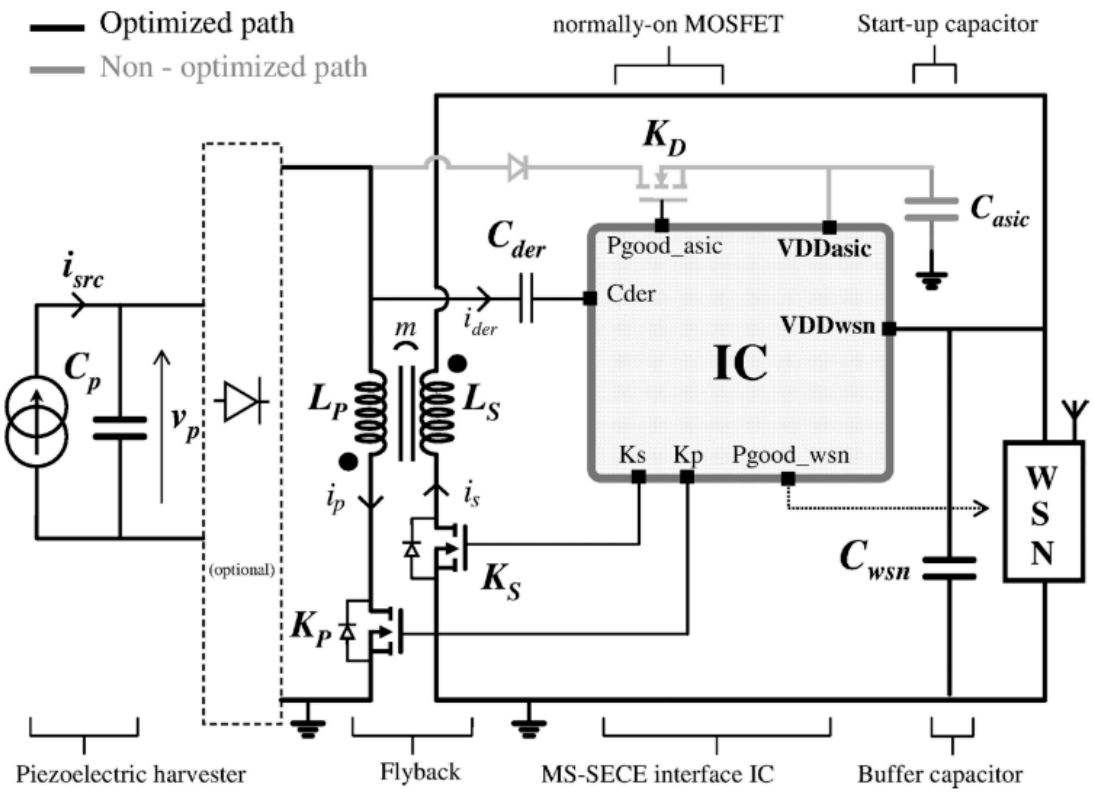


Figure 1-36 Schematic of piezoelectric energy harvesting system with MS-SECE[77].

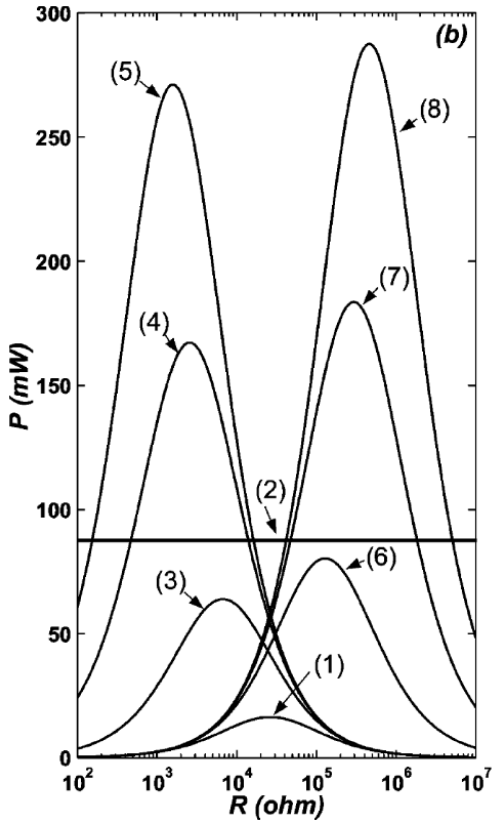


Figure 1-37 Comparison between (1) Standard interface; (2) SECE; (3)-(5) Series SSHI; (6)-(8) Parallel SSHI [85].

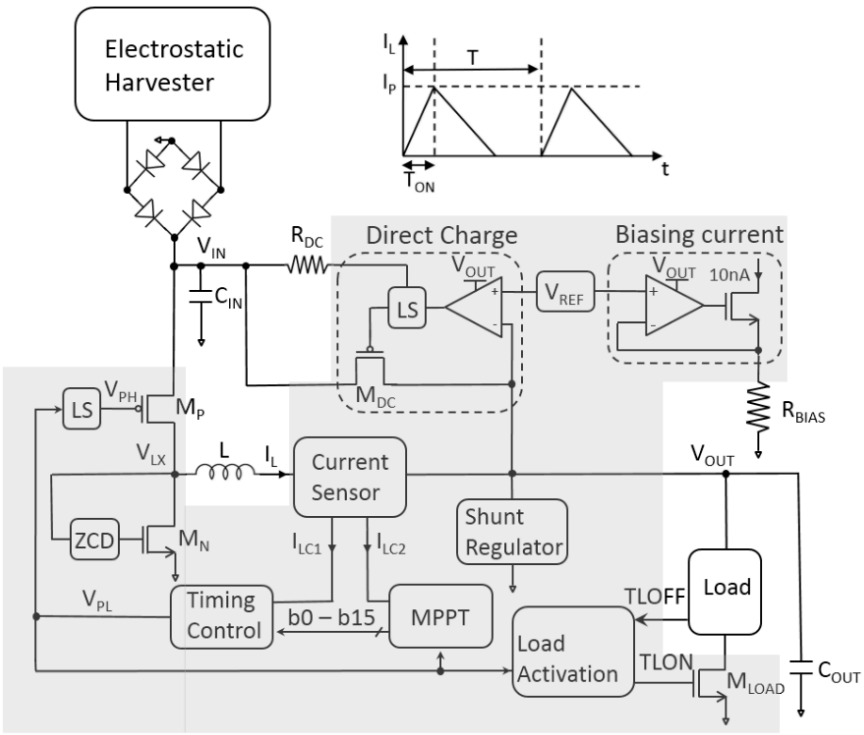


Figure 1-38 An integrated electrostatic energy harvester interface with 60V maximal input voltage [88].

	This work	ISSCC 2018 [1]	ISSCC 2015 [3]	ISSCC 2013 [4]
Process	0.18-µm BCD	0.18-µm BCD	0.25-µm BCD	0.25-µm BCD
Harvester type	Triboelectric	Triboelectric	Electrostatic	Electrostatic
Converter topology	Dual–input buck (bidirectional)	Dual–input buck (unidirectional)	Single–input buck	Single–input buck
MPPT method	FOCV	FOCV	Digital	Analog
MPPT integration	Yes	No	Yes	Yes
Input power	8.62–19.8µW	4.53–16.3µW	1µW–1mW	25µW–1.6mW
Input voltage	<70V	<70V	<60V	<60V
Output voltage	3–5V	1–5V	1–5V	1–5V
Maximum end-to-end efficiency @ input power	70.72% @ 20.70µW (V_{IN} = 30V)	49.57% @ 16.3µW (V_{IN} = 30V)	85%* @ 13.20µW** (V_{IN} = 4.862V)	89%* @ 100µW** (V_{IN} = 7.071V)

* Measured with electrical model of energy harvesters
** Estimated

Figure 1-39 Comparison between high-voltage interface circuits for electrostatic/triboelectric energy harvesting systems [91].

Chapter 2 Generator model

2. 1. Introduction

To verify the applicability of SSHI, a generator model of electret-based energy harvester ought to be built. This model, which links the mechanical domain (force, displacement) and the electrical domain (voltage, current), has not been clearly classified so far. Numerous researches have been focused on reliable prediction of output power, including modeling of parasitic capacitance and/or fringe effects [33], [100], [101]. Minor attention was drawn on the electromechanical model which is important in dynamic analysis [84], electromechanical-coupled optimal design[102] and synchronized circuit design in the present study. Specifically, this model consists of two parts: (1) a circuit model which links the output current to the mechanical displacement; (2) a dynamic model which defines the electrical restoring force applied back to the mechanical structure due to power generation.

For the circuit model, Bartsch et al. proposed a square-wave voltage source in series with an internal resistor (Figure 2-1), which served their aim of output power prediction [52]. However, this model loses accuracy to predict the phase difference between source current i_{ges} and output voltage $V(t)$, because actually the internal resistor in this model should be an internal capacitor.

As for the electrical restoring force, Miki et al. carried out numerical simulation and proved that electrical restoring force is strongly dependent on the nonlinearity of external circuit [103]. Crovetto et al. pointed out the electrical restoring force is more related to the output voltage [104]. Murotani et al. derived a rigorous electromechanical model in which an analytical form of electrical restoring force is presented, and introduced time-delay model to address the phase lag between output voltage and velocity of the mass [105]. But the conversion from equivalent circuit model to linearized circuit model is obscure. The time-delay model does not fully disclose the physics which caused the phase lag between output voltage and velocity.

In this paper, an analytical generator model for electret in-plane energy harvester is presented. In this model, a circuit model which is compatible with spice simulation will be presented, and an analytical expression of electrical restoring force is given. In addition, physical meaning of each term will be clearly classified to reach a comprehensive understanding on electromechanical behaviors of electret in-plane EH.

2. 2. Electromechanical transduction

The generator model of piezoelectric energy harvester is introduced first before looking into that of electret ones. **Figure 2-2** shows the equivalent model of piezoelectric vibration energy harvester [55]. The piezoelectric equations describe its electromechanical transduction as

$$\begin{cases} \boldsymbol{F_{PE} = K_{PE}u + \alpha_{PE}V} \\ \boldsymbol{I = \alpha_P \dot{u} - C_{PE}\dot{V}} \end{cases} \quad (2\text{-}1)$$

It links mechanical parameters (displacement u, restoring force F_P) with electrical ones (output current I, output voltage V). K_{PE} is the short-circuit stiffness of the piezoelectric disk, C_{PE} is the clamped capacitance and α_{PE} is the force factor [55]. It reveals that the restoring force F_{PE} is the sum of a mechanical elastic force from the piezoelectric material and an electrical force $F_{ePE}=\boldsymbol{\alpha_{PE}V}$ proportional to output voltage. On the other hand, as a generator, piezoelectric EH can be modelled as a current source $I_{sPE} = \alpha_P \dot{u}$ in parallel with its shunt capacitance.

However, the electromechanical transduction equations of electret in-plane EH has not been clearly addressed. Figure 2-3 shows the model of electret-based in-plane EH assuming a one-dimensional electrostatic field [97].

The guard electrode and the base electrode are formed on movable structure; whilst the collector electrode and the ground electrode are formed on fixed structure to collect induced charges. Electret material is evenly coated on guard and ground electrodes, but only the electret on the base electrode is charged. The load resistor R is connected between collector electrode and ground electrode. The ground electrode, base electrode, and guard electrode are grounded. The parasitic capacitance C_p, which located between interdigital collector and ground electrodes, is assumed to be constant with time. x_1 represents the relative displacement of the collector electrode with respect to the charged electret film. The horizontal gap between electrodes are neglected, hence $x_1 + x_2 = w$, where w is the width of electrode.

Applying Gauss's law at the electret surface, we get

$$\begin{cases} \boldsymbol{\varepsilon_1 E_1 - \varepsilon_2 E_2 = \sigma_e} \\ \boldsymbol{\varepsilon_1 E_3 - \varepsilon_2 E_4 = 0} \end{cases} \quad (2\text{-}2)$$

where E_1, E_3 are the electric fields in the air gap (permittivity: ε_1); E_2, E_4 are the electret fields in the electret film (permittivity: ε_2), respectively. $\sigma_e = \frac{\varepsilon_2 V_S}{d}$ is the surface

charge density, where V_s is the surface potential and d is the thickness of electret film. Using Kirchhoff's law, we obtain:

$$\begin{cases} \boldsymbol{V + gE_1 + dE_2 = 0} \\ \boldsymbol{V + gE_3 + dE_4 = 0} \end{cases} \tag{2-3}$$

where V is the output voltage across load and g is the height of air gap. The output current I is given by the conservation of charges:

$$\boldsymbol{I = -\frac{\partial(\sigma_1 x_1 L + \sigma_2 x_2 L)}{\partial t} - C_p \frac{\partial V}{\partial t}} \tag{2-4}$$

where L is the inward length of the electrode, $\sigma_1 = -\varepsilon_1 E_1$ and $\sigma_2 = -\varepsilon_1 E_3$ are the surface charge densities on the collector electrode. Combining (2-2)- (2-4) yields

$$\boldsymbol{I = \frac{C_i V_s}{w}\frac{\partial x_1}{\partial t} - (C_i + C_p)\frac{\partial V}{\partial t}} \tag{2-5}$$

where $C_i = \frac{\varepsilon_2 wL}{d+\frac{\varepsilon_2}{\varepsilon_1}g}$ is the internal capacitance between collector electrode and its counter electrode, $\frac{\partial x_1}{\partial t}$ is the relative velocity between rotor and stator.

The terms on the RHS of Eq. (2-5) can be viewed as, 1) the induced current $I_s = \frac{C_i V_s}{w}\frac{\partial x_1}{\partial t}$, which corresponds to the change of induced charges on the collector electrode, and 2) the charging current of the internal capacitor C_i and the parasitic capacitance C_p. Therefore, a circuit model is derived as Figure 2-4. Since C_i is usually smaller than C_p, electret-based EHs are susceptible to C_p and the matched impedance is determined in $C_e = C_i + C_p$. Previous studies often failed to recognize the internal capacitance C_i which leads to additional phase lag between velocity and output voltage besides parasitic capacitance.

On the other hand, to calculate the electrical restoring force F_e, the energy conservation law is considered. For a given period of time, the change of electrical energy E_{elec} should be equal to the work done by electrical restoring force F_e in lateral direction since the structure is fixed vertically, namely

$$\boldsymbol{\dot{E}_{elec} = F_e \dot{x}} \tag{2-6}$$

where E_{elec} is the sum of internal electrostatic energy E_{in} and the external energy E_{ex} which is consumed by C_p and R:

$$\boldsymbol{E_{elec} = E_{in} + E_{ex} = \sum_{k=1}^{6} \frac{1}{2} C_{ik} V_k^2 + \int \frac{V^2}{R} dt + \frac{1}{2} C_p V^2} \tag{2-7}$$

where C_{ik} and V_k are the capacitances and voltages across the dielectric layers corresponding to electric field E_1 to E_6, respectively. By applying gauss's in each layer, E_{in} can be rewritten as

$$\boldsymbol{E_{in} = \sum_{k=1}^{6} \frac{1}{2} C_{ik} V_k^2 = \frac{1}{2} C_i V^2 + \frac{1}{2} \frac{\varepsilon_2 g}{\varepsilon_1 d} C_i V_s^2} \tag{2-8}$$

Combining (2-5)- (2-8) and considering $I = V/R$ yields

$$\boldsymbol{F_e = \frac{C_i V_s}{w} V} \tag{2-9}$$

Eq. (2-9) reveals that the electrical restoring force F_e is proportional to the output voltage V. Due to the phase lag led by C_i and C_p, in-plane electret EH cannot be viewed as velocity-damped resonant generator (VDRG) in which F_e is proportional to velocity $\dot{x}$.

Finally, combining (2-5) and (2-9) yields the electromechanical transduction equations for in-plane electret EH:

$$\begin{cases} \boldsymbol{F_e = \alpha_e V} \\ \boldsymbol{I = \alpha_e \dot{u} - C_e \dot{V}} \end{cases} \tag{2-10}$$

Here the force factor of electret-based in-plane energy harvester is defined as

$$\boldsymbol{\alpha_e = \frac{C_i V_s}{w} = \frac{n \varepsilon_2 L V_s}{d + \frac{\varepsilon_2}{\varepsilon_1} g}} \tag{2-11}$$

The shunt capacitance C_e in electret EH is the sum of internal capacitance C_i and parasitic capacitance C_p:

$$\boldsymbol{C_e = C_i + C_p} \tag{2-12}$$

Comparing Eq. (2-1) with Eq. (2-10), it is found that electret-based in-plane EH behaves like piezoelectric EH, except that 1) electret-based in-plane has no intrinsic stiffness like K_{PE} in piezoelectric EH; 2) the force factor of electret-based EH is tunable (by n, V_s and g) for a given dimension and material (L, ε_2, ε_1 and d fixed), whilst the force factor of piezoelectric EH is a quantity of material type if the dimension is fixed.

Table 2-1 shows a comparison between electret and piezoelectric EHs. Electret EH is much more susceptible to parasitic capacitance due to its low internal capacitance which results from relatively large vertical air gap (100 μm). On the other hand, the low shunt capacitance C_e leads to high output voltage in spite of low source current.

Table 2-1 Comparison between electret and piezoelectric EH based on circuit model

	Electret EH	Piezoelectric EH [81]
V(mm^3)	Φ40*1.2	10*5*0.5
I_s (μA)	7.9@1 Hz	>100@100Hz
C_i (pF)	41	1400
C_p (pF)	128	Neglected
C_e (pF)	169	1400
V_{oc} (V)	107	<10@0.3 $m \cdot s^{-2}$
P_o (μW)	~200	7.2

For weakly-coupled electret EHs, increasing I_s and reducing C_p are two fundamental ways to enhance the output power of electret EH. Note that both methods will inevitably increase output voltage, which draws challenge for subsequent voltage converter design.

2. 3. Electromechanical model of linear vibration generator

Figure 2-5 shows an equivalent model of electret-based in-plane linear vibrational energy harvester. F is the excitation force applied on a mass M mounted on moveable part, D_m is the mechanical damping coefficient and K_e is the system stiffness. The dynamic equation is

$$\boldsymbol{F = M\ddot{u} + D_m\dot{u} + K_E u + \alpha_e V} \tag{2-13}$$

Similar to that in piezoelectric EH, the squared electromechanical coupling coefficient k_e^2 of electret EH can be defined as

$$\boldsymbol{k_e^2 = \frac{\alpha_e^2}{K_E C_e + \alpha_e^2}} \tag{2-14}$$

This coefficient is crucial to evaluate a kinetic energy harvester because it defines the effectiveness of the generator. In other words, it defines the percentage of energy from the motion into work done against the electrostatic force.

In piezoelectric energy harvester (Figure 2-2), the dynamic equation gives

$$\boldsymbol{F = M\ddot{u} + D\,\dot{u} + (K_{PE} + K_s)u + \alpha_p V} \tag{2-15}$$

Both the coupling coefficient of piezoelectric disk k_m^2 and the global coupling coefficient of the EH k_p^2 are defined as

$$\boldsymbol{k_m^2 = \frac{\alpha_p^2}{K_{PE}C_{PE} + \alpha_p^2}} \tag{2-16}$$

$$\boldsymbol{k_p^2 = \frac{\alpha_p^2}{(K_{PE} + K_s)C_p + \alpha_p^2}} \tag{2-17}$$

where $K_{PE} = \frac{c_{33}^E A}{d} = \frac{\varepsilon_{33}}{c_{33}^E}\alpha_p$ is the short-circuit stiffness of piezoelectric disk, $K_s$is the structure stiffness, $\alpha_p = \frac{\varepsilon_{33} A}{d}$ is the force factor. ε_{33} is piezoelectric coefficient and c_{33}^E is the short-circuit elastic rigidity [55].

Based on a generic model of electret and piezoelectric EHs shown in Figure 2-6, a comparison of the electromechanical coefficient is presented in Table 2-3. A highly coupled piezoelectric generator composed of two single crystal PZT-PT plates is chosen for a fair comparison [81]. On the other hand, a compact electret generator with reduced parasitic capacitance and a low-elastic-coefficient external spring is chosen for its potential high coupling[45]. The parameters are listed in Table 2-2.

As shown in Table 2-3, the force factor of electret EH is much smaller than piezoelectric ones because the limited charge stored in electret and the relatively large air gap. Consequently, the induced current of electret EH is usually lower than piezoelectric ones. However, thanks to the much lower shunt capacitance and the absence of material stiffness K_{PE}, the electret EH shows superior effectiveness over the selected highly coupled piezoelectric EH.

Figure 2-7, Figure 2-8 and Figure 2-9 show the influence of surface potential, parasitic capacitance and overall stiffness on electromechanical coupling coefficient, respectively. It reveals that system stiffness, which can be tuned by designing an external spring, draws a strongest impact on coupling. In the meantime, reducing parasitic capacitance is an effective way to achieve higher coupling. The coupling improvement led by solely increasing surface potential saturates in a region where system stiffness plays a more important role.

Table 2-2 Parameters in an electret-based in-plane linear vibration EH [45].

Parameters	Definition	Value (typical)
ε_e	Permittivity of electret	$2.1\varepsilon_0$
L	Length of electrode	20 mm
Vs	Surface potential	0~1000V (700V)
d	Thickness of electret	15μm
g	Vertical gap	70μm
K_s	System stiffness	0~100N/m (30N/m)[1]
C_{in}	Internal capacitance	5-8pF (6pF)
C_p	Parasitic capacitance	17-25pF (25pF)
n	Electrode pairs	≈22

[1] estimated from [106].

Table 2-3 Comparison of electromechanical coupling between electret and piezoelectric EHs.

Parameters	**Piezoelectric EH**[81]	**Electret EH**[45]
α (mN/V)	90	0.035
C_e (pF)	1400	25
K_{PE} (N/m)	7350	0
k_m^2 (-)	0.8	1
K_s(N/m)	7.36×10^6	30
$P(\mu W)$	7.2 @97.5 Hz, 0.3m·s^{-2}	100@30 Hz, 1.47 m·s^{-2}
$M(g)$	19.6	<3.7
k^2 (-)	0.44	0.57

2. 4. Circuit model validation

As the main purpose of the present work is to develop nonlinear circuit to electret EH, the circuit model is validated as follows.

2. 4. 1. Fabrication process

The rotor and stator are fabricated based on MEMS technology. In the rotor part (Figure 2-10), a 360-nm-thick Cr/Au/Cr layer is first coated on Tempax (glass) wafer. Tempax wafer is chosen for its good transparency and resistance to thermal deformation. Afterwards, 109 poles are patterned by photolithography. The horizontal distance between electrodes at the innermost edge is chosen as 50 μm [37]. Afterwards, 17-μm-thick electret material CYTOP EGG [35] is spun-on the patterned electrodes. Only the CYTOP film above the base electrode is charged with soft X-ray [36].**Figure 2-12** shows a magnified view of the rotor. In the stator part (Figure 2-11), the same number of poles are formed without electret coated.

2. 4. 2. Experimental setup

The difficulty in validating the theoretical analyses mainly lies in the accurate inspection of the vertical gap between rotor and stator. In this regard, a test bench as Figure 2-13 is developed to accurately control the vertical gap distance. At first, the rotor is attached to a rotational stage (DDR100/M, Thorlabs) by thermal glue. The rotational stage is driven to rotate at 1rps by PC. On the other hand, the stator is attached onto a metal frame via a vacuum absorber. The metal frame is connected a 5-axis stage which enables adjusting the position and inclination of the stator. This allows alignment of center and parallelism between rotor and stator using a laser displacement meter (LT-9500, Keyence). A stepping motor (DS102, Suruga Seiki) is employed to adjust the gap distance accurately.

In the measuring part, An I/V converter (CA5350, NF) is placed in series with load resistor to measure the generator output current in sub-10μA range. Then the output power for a give load is calculated. The validation of circuit model is carried out in standard AC case. In this case, the rotational EH is connected to a resistive load.

Figure 2-14 shows the simulation setup in LTspice. Based on the circuit model in Figure 2-4, assuming x_1=0 at t=0 (Figure 2-3),the source current I_s of a rotational electret EH rotating at f_r rps is a square wave as

$$I_s = \begin{cases} 2C_i V_s n f_r, & t \in \left[kT, \left(k+\frac{1}{2}\right)T\right) \\ -2C_i V_s n f_r, & t \in \left[\left(k+\frac{1}{2}\right)T, (k+1)T\right) \end{cases} \quad k = 0, 1, 2 \ldots \tag{2-18}$$

where $C_i = \frac{\varepsilon_2 A}{d+\frac{\varepsilon_2}{\varepsilon_1}g}$. The generator parameters are listed in Table 2-4.

2. 4. 3. Results

Figure 2-15 and Figure 2-16 show a comparison of output voltage and output power between simulation and experiment, respectively. In terms of output power, the experimental results are in accordance with simulation. In figure 12(a), the output voltage in experiment (red dots) is not as nonlinear as that in simulation. This is because the fringe electric field and horizontal gap between electrodes are not considered in simulation.

2. 5. Summary

The contents of this chapter are summarized as follows:

(1) An analytical generator model, including a circuit model and a dynamic model, is proposed for the first time. It reveals that electret in-plane EH behaves like piezoelectric ones. Namely, electret EH can be modelled as a current source in parallel with its internal capacitance and parasitic capacitance, which confirms the applicability of nonlinear circuits (SSHI/SECE). According to the dynamic model, the electrical

Table 2-4 Parameters in electret-based rotational EH

f_r	Rotational frequency	1 Hz
n	Number of electrode pairs	109
A	Maximum overlapping area	5 cm^2
V_s	Surface potential of electret	886 V
ε_2	Permittivity of electret	2.1ε_1
ε_1	Permittivity of air	8.85×10^{-12} F/m
d	Thickness of electret	17 μm
g	Air gap	100 μm
C_p	Measured parasitic capacitance	128 pF
C_i	Calculated internal capacitance	41 pF

restoring force is proportional to the output voltage, which agrees with previous experimental studies. The scale factor between the electrical restoring force and the output voltage, known as the force factor in piezoelectric transducers, is hence defined for electret energy harvester for the first time.

(2) An electromechanical model of in-plane electret linear vibration energy harvester is derived. Thanks to the absence of intrinsic stiffness, electret energy harvester presented stronger electromechanical coupling based on the case study.

(3) Based on the circuit model, electret EH is susceptible to parasitic capacitance due to its low internal capacitance (<50 pF). On the other hand, despite that electret generator generates much lower current (< 10 μA), the output voltage is still much higher (10s~100s V) than that of piezoelectric ones, owing to its much lower shunt capacitance (<200 pF). Therefore, electret energy harvester is sensitive to leakage current and introduced capacitance which may led by the nonlinear circuit.

(4) In addition, the circuit model is experimentally validated using a test bench of rotational energy harvester.

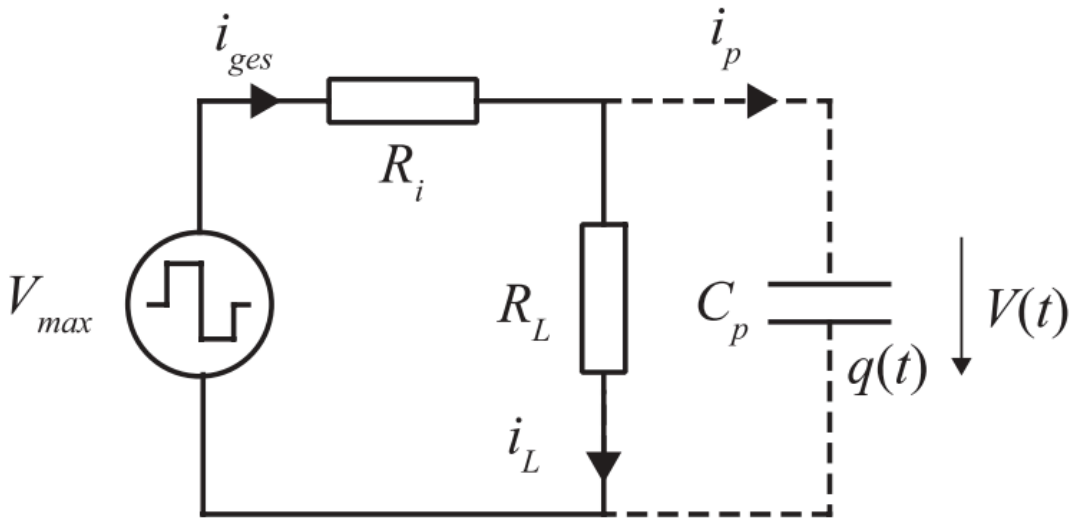


Figure 2-1 Equivalent circuit representation of electret generator with square voltage and internal resistor R_i [52].

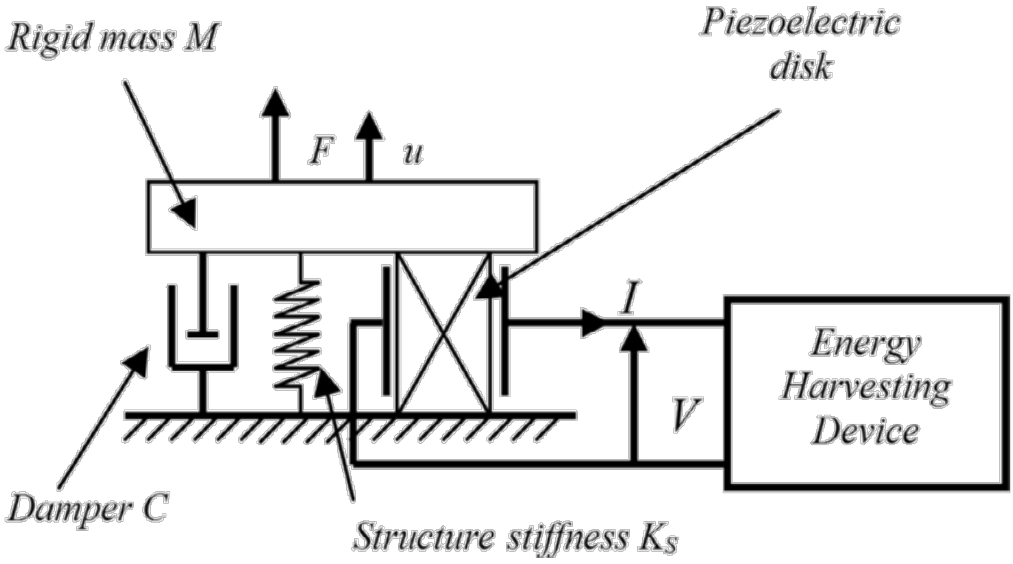


Figure 2-2 Equivalent model of piezoelectric vibration energy harvester [55].

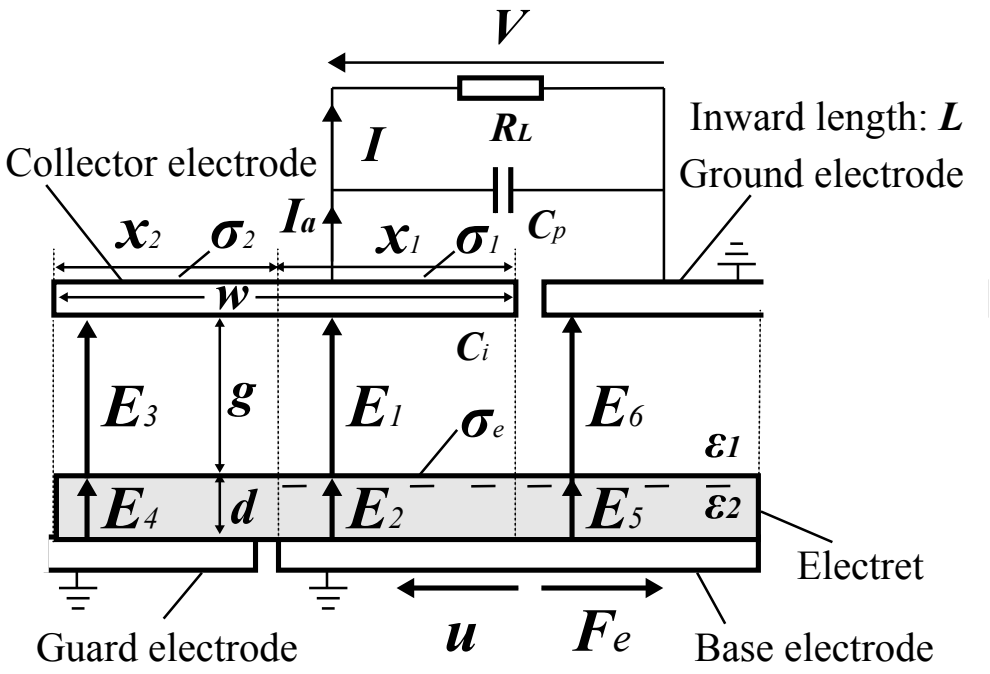


Figure 2-3 1-dimensional model of electret-based in-plane energy harvester with CYTOP evenly coated on guard and base electrodes.

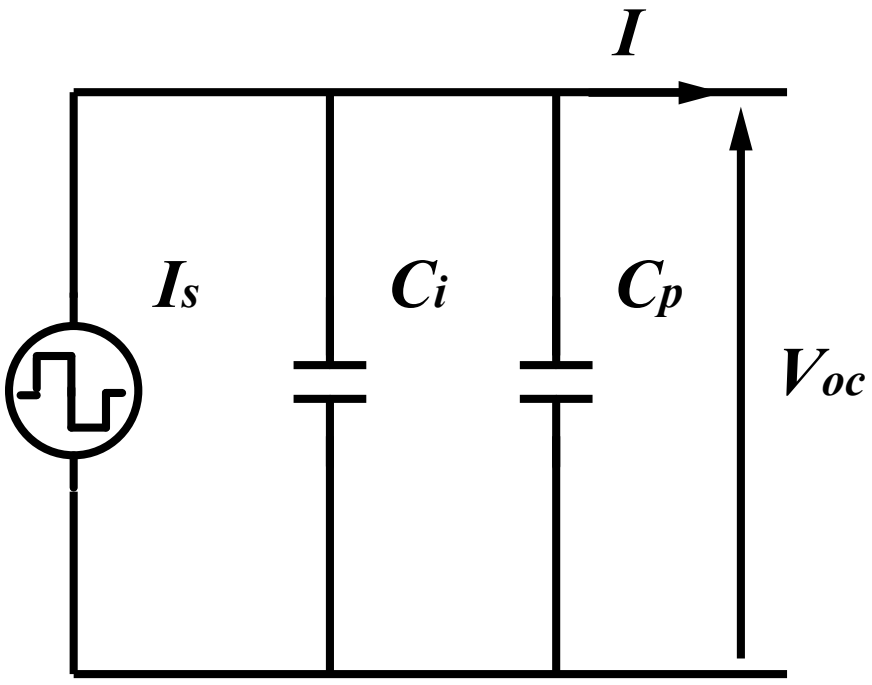


Figure 2-4 Circuit model of electret-based in-plane EH.

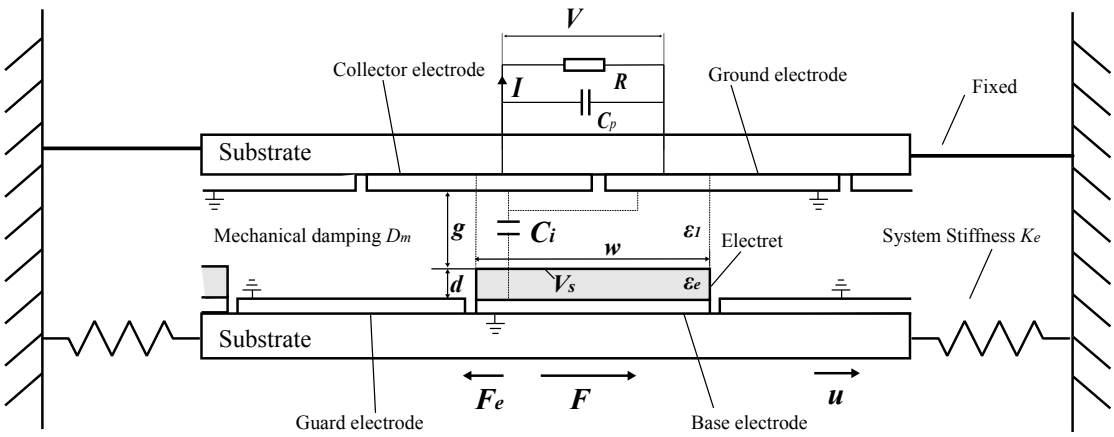


Figure 2-5 Equivalent model of electret-based in-plane linear vibration energy harvester.

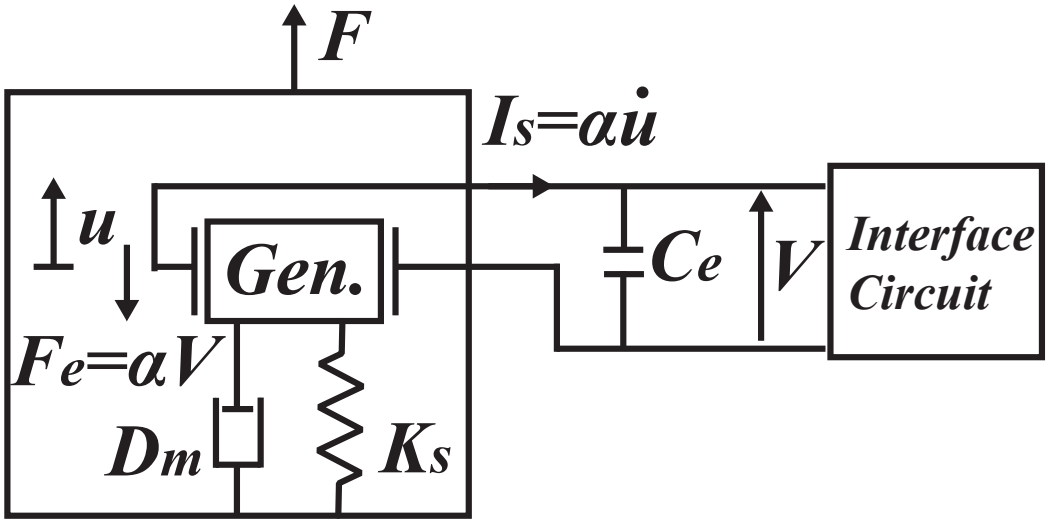


Figure 2-6 Generic model of electret and piezoelectric energy harvester.

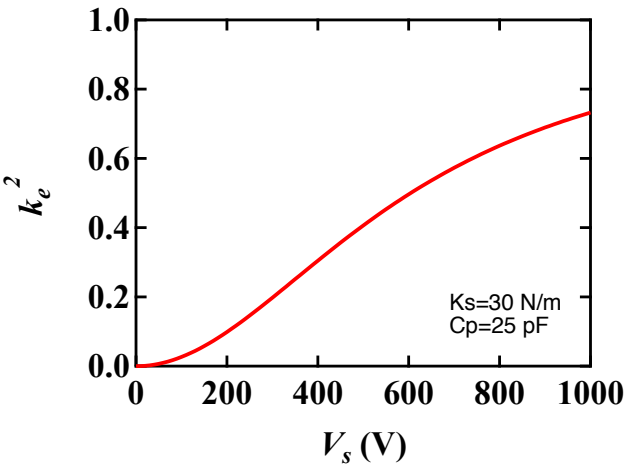


Figure 2-7 Generator coupling coefficient k_e^2 as a function of surface potential V_s.

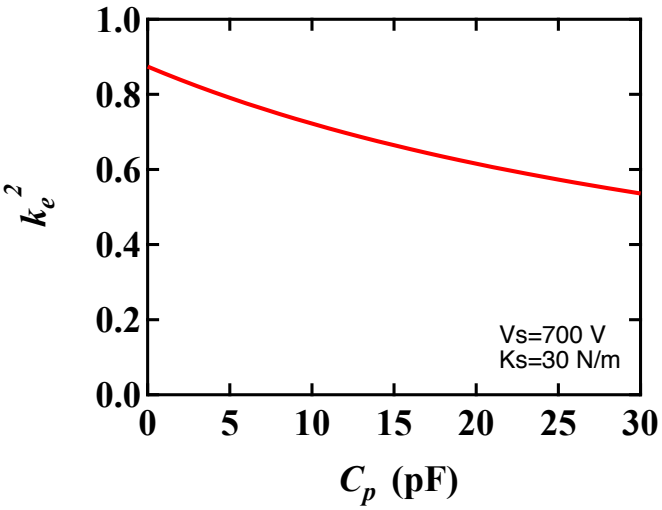


Figure 2-8 Generator coupling coefficient k_e^2 as a function of parasitic capacitance C_p.

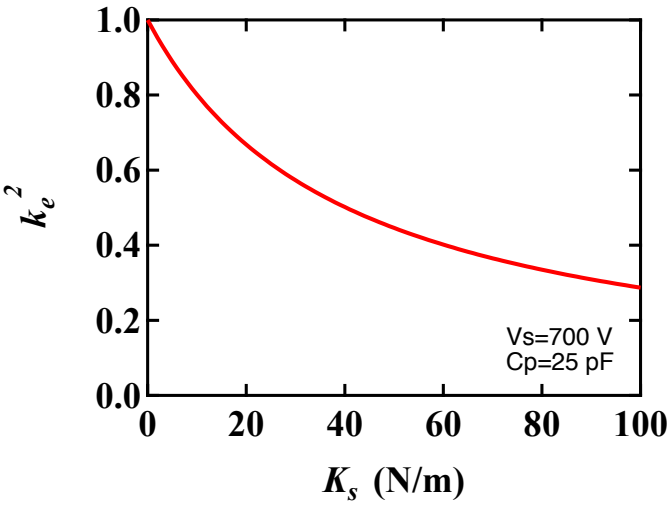


Figure 2-9 Generator coupling coefficient k_e^2 as a function of overall stiffness K_s.

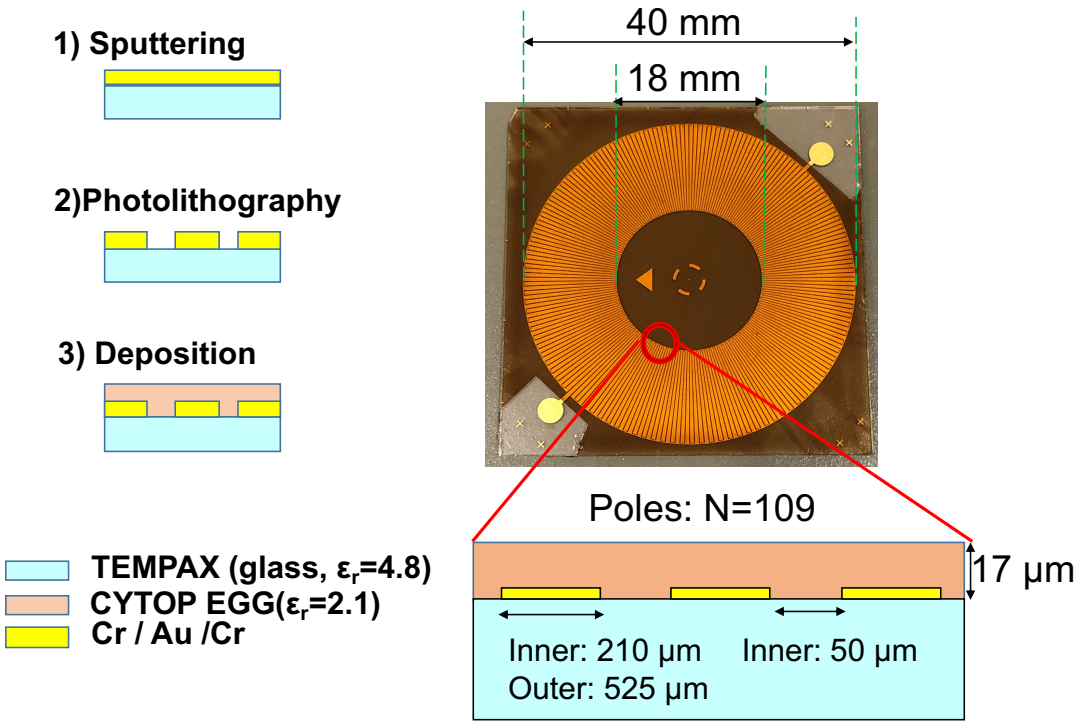


Figure 2-10 Rotor fabrication using Tempax wafer.

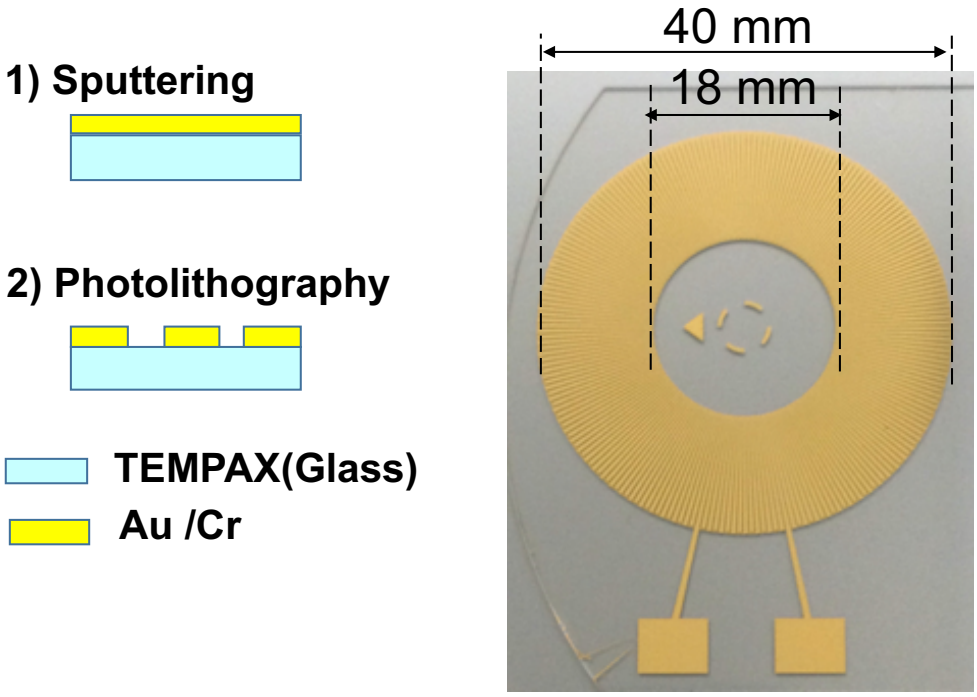


Figure 2-11 Stator fabrication using Tempax wafer.

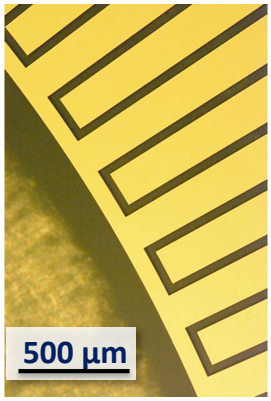


Figure 2-12 Magnified view of rotor.

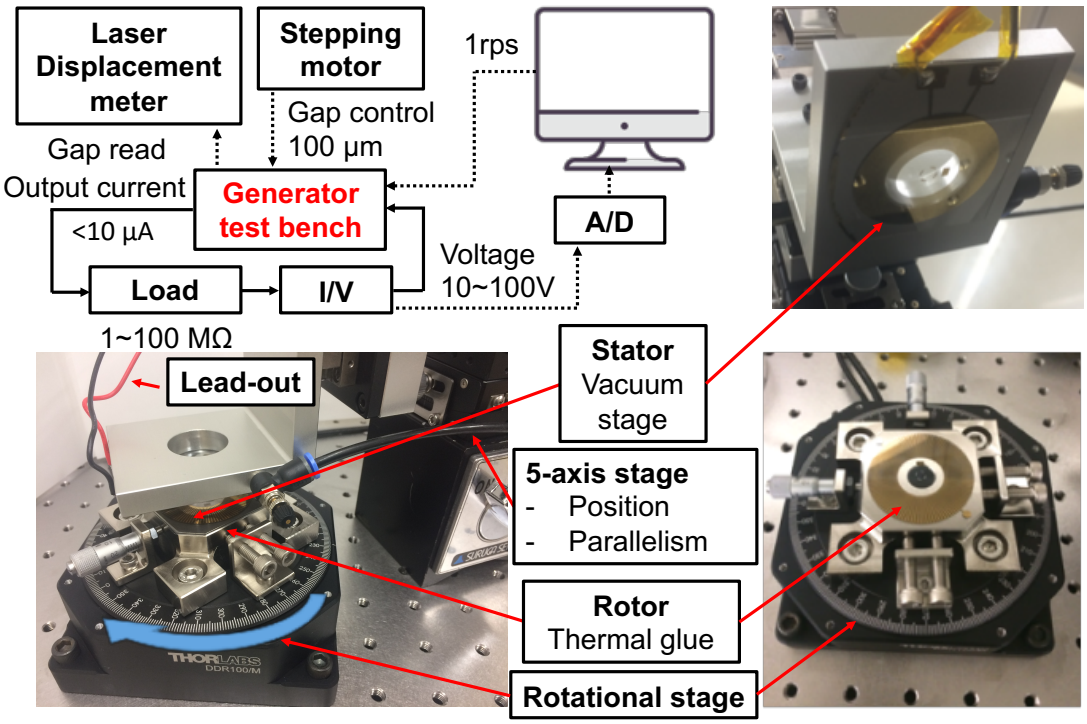


Figure 2-13 Test bench of electret-based in-plane EH.

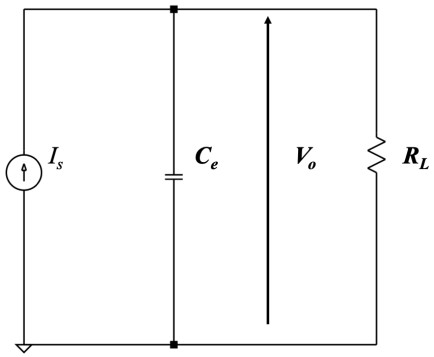


Figure 2-14 Simulation setup in LTspice (standard AC)

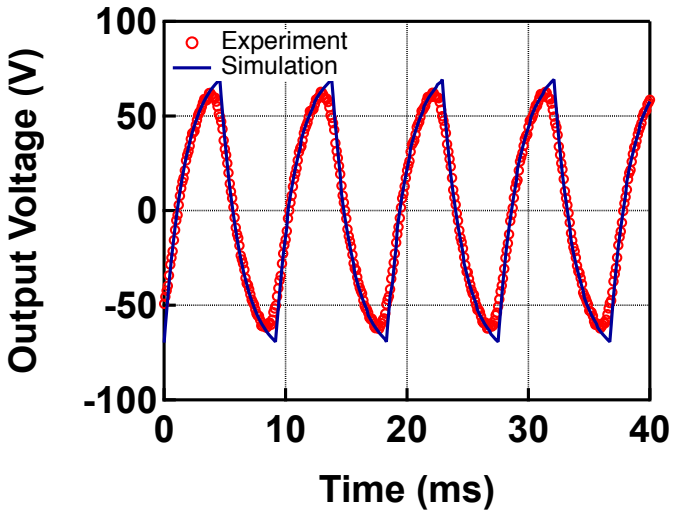


Figure 2-15 Simulated and measured output voltages of electret EH.

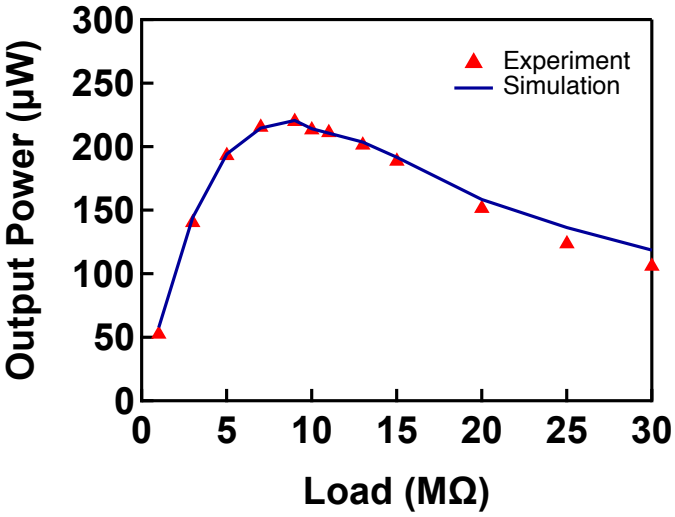


Figure 2-16 Simulated and measured output power of electret EH.

Chapter 3 Synchronized Switch Harvesting on Inductor

3. 1. Output power of rotational electret EH with SSHI

3. 1. 1. Standard DC

Figure 3-1 shows the standard DC case where rotational electret EH is connected to a full-bridge rectifier. At steady state, the DC voltage across storage capacitor C_s is V_{rec}. The generator output voltage V_o is shown as $V_{standard}$ in Figure 3-4. The charge conservation law in half a period gives

$$\frac{\boldsymbol{I_s T}}{\boldsymbol{2}} = \boldsymbol{2C_e V_{rec}} + \frac{\boldsymbol{V_{rec} T}}{\boldsymbol{2R}} \tag{3-1}$$

Therefore, the output power is

$$\boldsymbol{P_o} = \frac{\boldsymbol{V_{rec}^2}}{\boldsymbol{R}} = \boldsymbol{I_s V_{rec}} - \boldsymbol{4C_e f_s V_{rec}^2} \tag{3-2}$$

where $I_s = 2Q_e f_s = 2C_i V_s n f_r$ based on Eq. (2-18), Q_e is defined as inducible charge in a rotational electret EH. The optimal voltage and maximal power are given as

$$\boldsymbol{V_{opt}} = \frac{\boldsymbol{C_i V_s}}{\boldsymbol{4C_e}} \tag{3-3}$$

$$\boldsymbol{P_{max}} = \frac{\boldsymbol{C_i^2 V_s^2 n f_r}}{\boldsymbol{4C_e}} \tag{3-4}$$

Based on Eq.(3-3), it is found that V_{opt} is independent of rotational frequency. On the other hand, if there is no parasitic capacitance, then C_e=C_i, thereby the optimal voltage $V_{opt} = \frac{1}{4} V_s$. Since the surface potential Vs is usually in 0.3~2 kV range, stepping down the high output voltage is a fundamental challenge in terms of circuit design for electret EH.

3. 1. 2. Parallel SSHI

Figure 3-2 shows a parallel SSHI interface circuit where a L-S branch is inserted parallelly between generator and full-bridge rectifier. The switch is turned on at zero-crossings of the source current to initiate a L-C_e oscillating process. This process is then stopped after half-period of the LC resonator, resulting in a voltage inversion across C_e. Usually the period of LC resonator is set to be much smaller than that of the current source ($T_s = \frac{1}{n f_s}$), hence the voltage inversion is completed instantly, as V_{sshi} shown in

Figure 3-4. Due to the resistance in the LC loop, the amplitude of voltage -V_{inv} after inversion cannot be equal to V_{rec}. Here we define an inversion ratio as

$$\boldsymbol{\gamma = \frac{V_{inv}}{V_{rec}}} \tag{3-5}$$

where

$$\boldsymbol{\gamma = e^{-\frac{\pi}{2Q_I}}} \tag{3-6}$$

is determined by the quality factor of the LC loop $Q_I = \frac{1}{r}\sqrt{\frac{L}{C_e}}$ [55]. Based on this equation, Q_I for electret generators should be higher than that in piezoelectric ones for a given inductor (inductance L and series resistance r defined), because the shunt capacitance C_e is usually much lower in electret generators.

As shown in Figure 3-4, it is clear that the switch actions make sure that I_s and V_o always have the same sign in SSHI case, indicating more power extracted from mechanical structure than that in standard case. On the other hand, the load voltage V_{rec} in SSHI case exceeds that in standard case, indicating more power harvested on load. The charge conservation law during half a period gives

$$\boldsymbol{\frac{I_s T}{2} = C_e(1-\gamma)V_{rec} + \frac{V_{rec}T}{2R}} \tag{3-7}$$

Therefore, the output power in parallel SSHI case is

$$\boldsymbol{P_o = \frac{V_{rec}^2}{R} = I_s V_{rec} - 2(1-\gamma)C_0 f_s V_{rec}^2} \tag{3-8}$$

The optimal voltage and maximal power are given as

$$\boldsymbol{V_{opt} = \frac{C_i V_s}{2(1-\gamma)C_e}} \tag{3-9}$$

$$\boldsymbol{P_{max} = \frac{C_i^2 V_s^2 n f_r}{2(1-\gamma)C_e}} \tag{3-10}$$

By comparing Eq. (3-2) and Eq. (3-8), it is found that the effect of parallel SSHI is to equivalently reduce the shunt capacitance from C_e to $\frac{(1-\gamma)}{2}C_e$, thereby leading to power enhancing ratio of $\frac{2}{1-\gamma}$, theoretically. Note that the optimal voltage of parallel SSHI is also $\frac{2}{1-\gamma}$ higher than that of standard DC case.

3. 1. 3. Series SSHI

Figure 3-3 shows a series SSHI interface circuit where a L-S branch is inserted between generator and full-bridge rectifier in series. Series SSHI is considered because it has the same optimal impedance as that in the standard case, which is much lower than that in parallel SSHI case [65]. In other words, the optimal voltage in series SSHI should be lower than that in parallel SSHI case, which is favorable for subsequent voltage stepping down. Similar to parallel SSHI, the switch *S* is controlled to flip the voltage across the shunt capacitance C_e at zero-crossings of the current source. The charge conservation law during half a period gives

$$\frac{\boldsymbol{I_s T}}{\boldsymbol{2}} = \boldsymbol{C_e(1-\gamma)V_{rec}} + \frac{\boldsymbol{V_{rec}T}}{\boldsymbol{2R}}\boldsymbol{(xx)} \tag{3-11}$$

Therefore, the output power in series SSHI case is

$$\boldsymbol{P_o} = \frac{\boldsymbol{1+\gamma}}{\boldsymbol{1-\gamma}}\boldsymbol{(I_s V_{rec} - 4C_0 f_s V_{rec}^2)} \tag{3-12}$$

The optimal voltage and maximal power are given as

$$\boldsymbol{V_{opt}} = \frac{\boldsymbol{C_i V_s}}{\boldsymbol{4C_e}} \tag{3-13}$$

$$P_{max} = \frac{(1+\gamma)C_i^2 V_s^2 n f_r}{4(1-\gamma)C_e} \tag{3-14}$$

By comparing Eq.(3-3) and Eq.(3-13), it is found that the optimal voltage at DC side is the same as that in standard case. The output power is enhanced by a ratio of $\frac{1+\gamma}{1-\gamma}$ by comparing Eq. (3-4) and Eq. (3-14).

Figure 3-5 shows a comparison of theoretical performance between series SSHI and parallel SSHI. In series SSHI case, the generator output voltage V_o is very high especially for low rectified voltage V_{rec}, which leads to very high voltage stress on the switch *S* during cold-start where V_{rec} increases from 0. Moreover, it needs additional circuitry for cold-start as the switch S is in series with full-bridge rectifier. In view of these practical issues, parallel SSHI is chosen for the first attempt.

3. 1. 4. Ideal SSHI

To verify the theoretical analysis in standard and parallel SSHI cases, numerical simulation is carried out using LTspice. Figure 3-6 shows the simulation setup of ideal SSHI using LTspice. The term 'ideal' means that the action of switch *S* is perfectly

Table 3-1 Parameters in ideal SSHI simulation setup.

Parameters	Definition	Value
I_s	Generator source current	7.9 μA
C_e	Generator shunt capacitance	169 pF
L	Inductance	5.6 mH
r	Series resistance of the inductor	1.37 kΩ
C_s	Storage capacitance	0.1 μF

synchronized with the current source I_s. This is achieved by the voltage-controlled switch S provided by LTspice and its supervisor V_m which is set to be synchronized with I_s. The parameters in the circuit is shown in Table 3-1. The generator parameters are calculated based on Table 2-4. Note that the series resistance r of the inductor L is tuned to achieve a realistic inversion ratio γ=0.7. In the standard DC case, the S, V_m and L are excluded.

Figure 3-7 shows the simulated and calculated results of output power as a function of rectified voltage V_{rec}, which verifies the equations derived in the theoretical analysis. Consequently, a power enhancing ratio of 6.7 is obtained at V_{rec}=350 V, with an output power of 1.2 mW. Despite the attractive power enhancing performance, the high V_{rec} required for optimal performance draws significant challenges for practical circuit design.

3. 2. Circuit design

The challenges of circuit implementation are resulted from the features of electret EH: 1) low source current makes the generator sensitive to leakage current; 2) low internal capacitance make the generator susceptible to parasitic capacitance introduced by nonlinear circuit. In view of these two features, electric components for small signal application should be chosen. 3) High output voltage makes it challenging for the control block which requires low input voltage and low DC voltage (<5V) supply.

Figure 3-8 shows a block diagram of SSHI circuit design for electret EHs. The main circuit, which consists of the switch unit and the dual-polarity rectifier, operates at high voltage (50~240 V) for transferring power from generator to load. On the other hand,

the peak detector serves as a control block to trigger and drive the switch for SSHI operation. Here a voltage divider is employed to convert the output voltage to a low one as the input to the peak detector. The peak detector is powered by the low-voltage DC output of the rectifier, thereby achieving an energetically closed system. Figure 3-9 shows a detailed circuit design of voltage-divider-based SSHI. It is explained in detail as follows.

3. 2. 1. Switch unit

Figure 3-10 shows the switch configurations of the L-S branch utilized in piezoelectric SSHI.

In the N-P configuration (Figure 3-10b), a pair of paralleled MOSFETs (M_n: N-channel MOSFET; M_p: P-channel MOSFET) switches are employed [57][107]. Since electret EH is modeled as current source in parallel with capacitance, the zero-crossing points of source current correspond to the extremes of the output voltage V_{max}. When the output voltage reaches its positive maximum, namely V_o=+V_{max}, Mn is turned on (by V_n>V_{thn}, V_{thn} is the threshold voltage of M_n) to enable a charge flipping of C_e via *L*-D_n-M_n. This process is stopped by D_n when the loop current tends to reverse, which indicates the completion of voltage inversion. Similarly, when V_o=-V_{max}, M_p is turned on (by V_p<-V_{thp}, V_{thp} is the amplitude of M_p threshold voltage) and a charge flipping of C_e is initiated via *L*-D_p-M_p. The latter is stopped by D_p. Note that the pulse generated for V_p and V_n has to be dual-polarity with respect to ground.

In the N-N configuration (Figure 3-10c), a pair of N-channel MOSFETs (M_{n1}, M_{n2}) switches are employed [60] [108]. The source of M_{n1} is connected to ground and the source of M_{n2} is connected to the output voltage, respectively. The working principle is similar to N-P configuration.

The N-N configuration is popular in piezoelectric application because 1) NMOS has lower on-resistance and volume; 2) N-N configuration doesn't require dual-polarity pulse for V_{n1} and V_{n2}. However, it is unfavorable if the generator output voltage is high, like that in the electret EH case. The reason is explained as follows. To turn on M_{n2} without breaking it, -V_{max}+V_{gs_max}>V_{n2}>-V_{max}+V_{thn2} should be held. V_{gs_max} is the maximal gate-to-source voltage and V_{thn2} is the turn-on threshold voltage. When V_{max} is large, a level-shifter is necessary to convert low-voltage pulse signal to high-voltage switch drive signal V_{n2} [108].

However, in the case of electret EH, an over-100V level-shifter is hard to realize in an efficient way considering an overall power budget of μW level. On the other hand, a local electronic breaker at high side could be another option[60]. However, the discharge of the capacitor in the envelop detector is tricky, because a proper gate resistor for discharging will introduce a significant leakage current to the generator. Moreover, the local electronic breakers introduce much parasitic capacitance to the generator.

Therefore, the N-P configuration is chosen for electret EH despite a dual-polarity pulse is required.

3. 2. 2. Peak detector

As illustrated above, a peak detector to detect the extremes of the generator voltage is needed for trigger the switch. It is achieved by calculating the derivative of the output voltage [56]. In Figure 3-11, assuming $V_o=V_{max}$ at $t=0$, the input signal V_r to the inverting input of the comparator is

$$\boldsymbol{V_r = V_o - V_c = V_o - V_o e^{-\frac{t}{R_{ed}C_{ed}}} = \left(1 - e^{-\frac{t}{R_{ed}C_{ed}}}\right) V_o} \qquad (3\text{-}15)$$

Therefore, V_r is the difference between current V_o and a previous V_o, which is preserved on C_{ed}, of a moment ($\tau=R_{ed}C_{ed}$) before. In other words, V_r indicates the time derivative of the output voltage. After a time period τ from the $V_o=V_{max}$, V_r turns negative and hence $V_g=V_{cc}$, thereby turning on M_n to initiate the voltage inversion from positive to negative. The process at $V_o=-V_{max}$ is similar. The comparator in this case can be a BJT [56], a MOSFET [64]or an IC [57]. In this way, the peak detection is achieved.

3. 2. 3. Dual-polarity rectifier

Since the peak detector in this case requires dual-polarity voltage supply, a dual-polarity rectifier is proposed for achieving self-powering. It is based on a unipolarity rectifier.

Figure 3-12 shows a unipolarity rectifier developed by OWL Co.[109]. The working principle is explained as follows. In Figure 3-13, when the voltage V_{rec} across the primary capacitor C_1 exceeds the threshold voltage of the Zener diode, it breaks down and hence the IC is powered to turn on the switch S which enables power transfer from generator to load. Figure 3-14 shows the measured results of converter efficiency as a function of generator source current which is derived based on the circuit model. It

reveals over an efficiency of over 70% was obtained at a very low sub-10 μA. By selecting an appropriate Zener diode, the average rectified voltage V_{rec} can be maintained at optimal voltage V_{opt} in Eq. (3-3), thus achieving maximal power transfer.

Figure 3-15 shows a detailed schematic of the dual-polarity rectifier. The dual-polarity rectifier consists of two half-wave bridge rectifiers flowed by a positive converter and a negative converter, respectively. In the positive converter, the buck converter is identical to that in unipolarity converter. The negative converter has a mirrored configuration compared with the positive converter. In this way, the AC input high voltage is rectified and converted to low-voltage dual-polarity output voltages ($+V_s$ and $-V_s$) with respect to the ground at AC side.

3. 3. Simulation results

Figure 3-16 shows the simulation setup of voltage-divider SSHI. Since the main scope of this work is the SSHI nonlinear circuit, so the dual-polarity rectifier is replaced by a full-bridge rectifier with a storage capacitor C_s and load R_L, to exclude the influence led by dual-polarity rectifier. In this case, the comparator is externally powered by DC voltage supply (V_s=3 V). Table 3-2 shows the parameters used in the simulation. The generator parameters are fitted from a test-bench-based electret EH device based on its output power in standard case. The components, which are also used in experimental validation, are characterized in detail.

The inductor is characterized using an impedance analyzer, with its inductance L, series resistance r_{series} and parallel resistance $r_{parallel}$ specified. The MOSFETs are intended for high-voltage small-signal application. Here the MOSFETs of the highest voltage-rating (M_n: BSP89, 240V; M_p: BSP92P, -250V) are selected, where the parameters from their datasheets are applied into simulation. Note that the upper limit of generator output voltage is then constrained at 240V considering the withstand voltage of the n-channel MOSFET. 250V-tolerable diodes BAV21 are characterized using a multimeter (U1282A, Keysight), with forward voltage drop V_F=0.6 V and reverse resistance $r_{reverse}$ measured. The $r_{reverse}$ of D_1, D_2, D_3, D_4, D_n, D_p are 370 MΩ, 233 MΩ, 216 MΩ, 285 MΩ, 376 MΩ, 421 MΩ, respectively. A 0.1 μF multi-layer ceramic capacitor is chosen for the storage capacitor C_s for its ultralow dielectric loss, which is negligible because the resistance of C_s is out of the range of the multimeter.

Table 3-2 Parameters in VD-SSHI simulation and experiment.

Definition	Value	Definition	Value
I_s	7.32 μA@109 Hz	M_n	BSP89 [110]
C_e	147 pF	M_p	BSP92p [111]
R_{d1}	100 MΩ	C_s	0.1 μF (MLCC)
R_{d2}	4.8 MΩ	Comparator	LTC1540
L	5.6 mH	C_{ed}	100 pF
r_{series} of L	10.22 Ω	R_{ed}	50 kΩ
$r_{parallel}$ of L	130 kΩ	D_n, D_p, D_1-D_4	BAV21
C_{par} of L	5 pF	$r_{reverse}$ of D	233~421 MΩ

Figure 3-19 shows the simulated output voltage which shows an inversion ratio as high as 0.8. Figure 3-20 shows the simulated output power as a function of rectified voltage. A power enhancing ratio of 2.45 is obtained at V_{rec}=140 V.

3. 4. Experimental results

3. 4. 1. Measurement setup

Figure 3-17 shows a schematic of measurement setup in standard DC and external-powered SSHI cases. In standard DC case, the inductor L, switch S and its peripheral circuits are not included. In external-powered SSHI case, the term 'external-powered' refers to the comparator in peak detector is powered by DC supply externally. As aforementioned, each component is characterized.

The AC-side voltage is measured by an oscilloscope (DSO6014A, Agilent) via a high-input-impedance (1GΩ, 5pF) voltage probe (HV-P60A). The power harvested on load at DC side is calculated by $P_o = I^2 R_L$. The load current I is derived by measuring the voltage across a sampling resistor R_s (100 kΩ) using a digital multimeter (U1282A, Keysight). The voltage probe is detached during output power measurement. Figure 3-18 shows the experimental setup of self-powered SSHI circuit which is made up of discrete components. Note that dual-polarity rectifier is excluded in external-powered SSHI case.

3. 4. 2. External-powered SSHI

Figure 3-19 shows the measured output voltage in external-powered SSHI case, with R_L=9 MΩ. An inversion ratio of 0.74 was observed. Consequently, a power enhancing ratio of 2.47 is obtained with SSHI experimentally (Figure 3-20). In addition, experimental and simulated results show good consistency, which enables an analysis of SSHI circuit efficiency based on simulation. By the way, the measured power consumption of comparator is 6 μW, indicating a self-powered operation is feasible.

3. 4. 3. Self-powered SSHI

In self-powered SSHI, 3 cases are investigated: standard, bi-standard and self-powered SSHI, as shown in Figure 3-21.

In standard case (Figure 3-21a), a unipolarity converter (Figure 3-12) is connected to the generator. In bi-standard case (Figure 3-21b), dual-polarity converter (Figure 3-15) is connected to the generator. In self-powered SSHI case (Figure 3-21c), SSHI circuit are inserted into bi-standard case.

Considering the high optimal voltage in SSHI case (Figure 3-20), dual-polarity converter rated at V_{rec}=50V (the highest voltage rating so far) is employed to achieve higher output power in SSHI. Since dual-polarity converter outputs V_p and V_n, the load voltage is defined as $V_L = \frac{V_p - V_n}{2}$. Figure 3-18 shows a view of the experimental setup.

Figure 3-22 shows the power generation results. By comparing bi-standard and self-powered SSHI case, we can observe the power enhancing effect of SSHI without the influence of converters. Consequently, 1.82x power gain was obtained in self-powered SSHI case against bi-standard case.

By comparing standard and bi-standard cases, the efficiency difference of unipolarity converter and dual-polarity converter are revealed. Unfortunately, for a given input power around 200 μW, the conversion efficiency of dual-polarity converter was 50%, approximately 30% lower than the unipolarity converter.

Finally, the overall performance of self-powered SSHI case is evaluated by comparing standard and self-powered SSHI cases. A moderate 1.22x power gain is achieved in self-powered SSHI case. The limited performance is mainly resulted from low efficiency and low voltage rating (50V) of dual-polarity converter.

Figure 3-23 depicts the measured voltage waveforms during cold-start process of self-powered SSHI in unloaded cases. At 1 rps rotational speed, it takes 10s to start the SSHI operation when the load voltage reaches 1.5V. SSHI voltage waveform with high inversion ratio was observed when load voltage exceeds 2V, which is the lower limit of supply voltage for normal operation of the comparator LTC1540. The upper limit of load voltage is 3.3V, owing to a protection circuitry inside the rectifier. It also reveals that after SSHI is initiated, more power was harvested on load.

3. 5. Discussion

3. 5. 1. Inversion ratio

The inversion ratio γ is an important benchmark to evaluate the performance of SSHI. Based on Eq. (3-6) and the inductor parameters in Table 3-2 , the theoretical inversion should be

$$\boldsymbol{\gamma_{ser} = e^{-\frac{\pi}{2Q_I}} = e^{-\frac{\pi}{2}*10.22*\sqrt{\frac{147*10^{-12}}{5.6*10^{-3}}}} = 0.997} \qquad (3\text{-}16)$$

However, γ in simulation and experiment is merely 0.74. Based on Eq. (3-6), γ=0.7 corresponds to a series resistance of 1.37 kΩ in the LC loop, which is unrealistic in the case that M_n and D_n are turned on. Therefore, the inversion ratio in Electret EH cannot be simply estimated by Eq. (3-6) which corresponds to a series RLC circuit.

To disclose this problem, a detailed circuit model of the L-C loop is built in Figure 3-24, taking the positive voltage conversion as an example. In the model, the series resistance R_{ser}, the parallel resistance R_{par} and the parasitic capacitance C_{par} of the inductor are considered; R_{on_d} and R_{on_n} denote the on-state resistances of D_n and M_n. Note that D_p and M_p are bypassed by D_n and M_n, hence their reverse resistance and parasitic capacitance are not considered. The value of parameters above is list in Table 3-3.

Table 3-3 Parameters in the detailed model of LC loop.

Parameters	Definition	Value
C_e	Generator shunt capacitance	147 pF
L	Inductance	5.6 mH
R_{ser}	Series resistance of the inductor	10.22 Ω
R_{par}	Parallel resistance of the inductor	130 kΩ
C_{par}	Parasitic capacitance of the inductor	5 pF
R_{on_d}	On-state resistance of diode D_n	5 Ω
R_{on_n}	On-state resistance of resistance M_n	6 Ω

The influence led by the parasitic capacitance of inductor can be neglected as it is much smaller than C_e. However, the shunt current led by R_{par} cannot be ignored as it is comparable to the impedance of C_e. Here we propose a simplified model (Figure 3-25), where R_{par} is included. Note that R_s is the sum of R_{ser}, R_{on_d} and R_{on_n}.

Figure 3-26, Figure 3-27, Figure 3-28 show the simulated inversion ratio as a function of R_{par}, R_{par} and L in SSHI (Figure 3-16) and the proposed simplified model, respectively. Compared with Eq.(3-6), the proposed model shows an improved consistence with SSHI simulation by considering R_{par}. The over-estimation by the proposed model might be caused by the transient resistance of MOSFET which is not considered.

Specifically, Figure 3-26 shows that parallel resistance (usually 10s~100s kΩ) draws a significant influence on inversion ratio. Figure 3-27 reveals that series resistance does not influence the inversion ratio in its usual range (<100 Ω). In Figure 3-28, the blue line depicts the inversion ratio in positive-to-negative voltage inversion and the green one corresponds to negative-to-positive inversion. To attain an average inversion ratio of 0.8, 1mH inductor should be enough, which is much smaller than the currently-employed 5.6 mH one.

The new findings above lead to new criteria for selecting an inductor which, as the only off-chip component, dominates the circuit volume. First, since series resistance is not important, hence the wire in the coil can be thinner, thereby reducing its volume at the cost of higher series resistance. Second, a 680- 1000 μH inductor is sufficient to guarantee an inversion ratio above 0.65, which could effectively reduce the turns of the inductor. Third, even though parallel resistance influences the inversion ratio to a large degree, it exhibits a saturation if R_{par}>100 kΩ, which means it is unnecessary to increase R_{par} further beyond 100s kΩ. These criteria are quite different from those in piezoelectric EH case which are based on Eq.(3-6).

To understand this abnormal phenomenon, the following is considered. Actually, Eq.(3-6) is based on the series RLC model. The series RLC circuit model, where R_{ser}, L and C_e share the source voltage, is not suitable for electret EH case, because the voltage across R_{ser} cannot be comparable to that across C_e, considering the low resistance R_{ser} the high impedance of C_e.

Instead, a parallel RLC circuit (Figure 3-29), where R_{par}, L and C_e share the source current, is more suitable to estimate the inversion ratio in electret EH case, because the

impedance of R_{par} and C_e are comparable. In this case, the quality factor and inversion ratio are given by

$$\boldsymbol{Q_I = R_{par}\sqrt{\frac{C_e}{L}}} \tag{3-17}$$

$$\boldsymbol{\gamma = e^{-\frac{\pi}{2Q_I}} = e^{-\frac{\pi}{2*21}} = 0.928} \tag{3-18}$$

Although the inversion ratio yield from parallel RLC circuit gives a closer result to the experimental case, it is not accurate enough. Therefore, it is better to employed the enhanced model to estimate the inversion ratio.

3. 5. 2. Efficiency analysis

Since the simulated output voltage and output power show good consistence with experimental results, an efficiency analysis of SSHI circuit is carried out based on simulation.

Figure 3-30 shows the power dissipation of each component in the voltage-divider SSHI circuit. Based on current design, voltage divider and diodes consume substantial power with increasing output voltage, followed by the inductor. For the voltage divider of 104.8 MΩ, its power consumption is proportional to V_o^2, resulting in a approximate power dissipation of 400 μW at V_{rec}=200 V. For the diodes in the rectifier, their reverse resistances are between 200-400 MΩ, which corresponds to a 100-200 MΩ parallel resistance to the generator, resulting in substantial power loss.

Consequently, the efficiency of SSHI decreases from over 80% @ 30V to below 30% @ 200V. If we consider the efficiency of 50% for the 50V-rated dual-polarity converter, the overall circuit efficiency of self-powered SSHI is merely 25%. Therefore, there is much room to enhance the performance of voltage-divider based SSHI to attain much higher absolute output power, by selecting diodes with higher reverse resistance, increasing the efficiency of dual-polarity rectifier and seeking alternative solution in place of voltage divider.

3. 6. Summary

In this chapter, a nonlinear circuit, known as SSHI, has been developed for electret energy harvester for the first time. Moreover, The simulated and experimental results of SSHI show good consistence, which allows a circuit analysis is based on simulation. The following results are obtained:

(1) A parallel-SSHI-based circuit design was proposed, simulated and experimentally validated. As a result, a power enhancing ratio of 2.47 has been obtained in SSHI case against conventional full-bridge rectifier experimentally, with control block externally powered.

(2) In self-powered SSHI, the ratio reduced to 1.2 due to the limited efficiency and voltage rating of the proposed dual-polarity converter.

(3) The inversion ratio, which is a benchmark to indicate power enhancing performance of SSHI, shows a dependence on the parallel resistance of the inductor. On the other hand, the series resistance of the inductor doesn't influence the inversion ratio in a certain range. This phenomenon, which is not observed in piezoelectric case, might be resulted from low internal capacitance of electret energy harvester. This knowledge shed new criteria in selecting inductors: smaller inductor with higher series inductance is acceptable in electret case.

(4) The presented voltage-divider-based SSHI (externally powered) circuit shows merely an efficiency of 50% at optimal voltage. It is found that the main power loss lies in the lossy voltage divider and rectification diodes. In addition, this efficiency reduces to 25% in self-powered SSHI, owing to the low efficiency of the proposed dual-polarity rectifier.

Therefore, future work should be done to achieve efficient operation of SSHI.

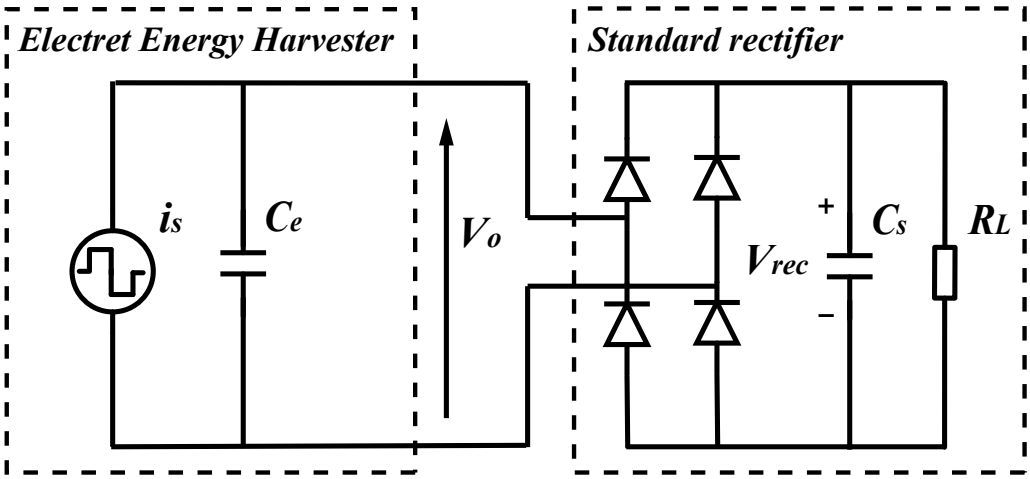


Figure 3-1 Standard DC: rotational electret EH with a full-bridge rectifier.

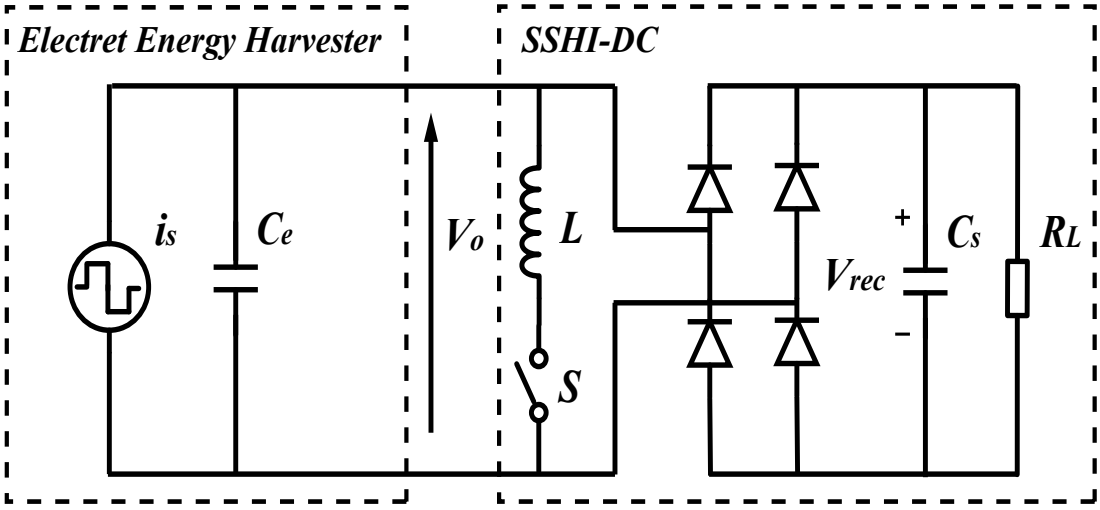


Figure 3-2 Parallel SSHI: rotational electret EH with parallel SSHI interface.

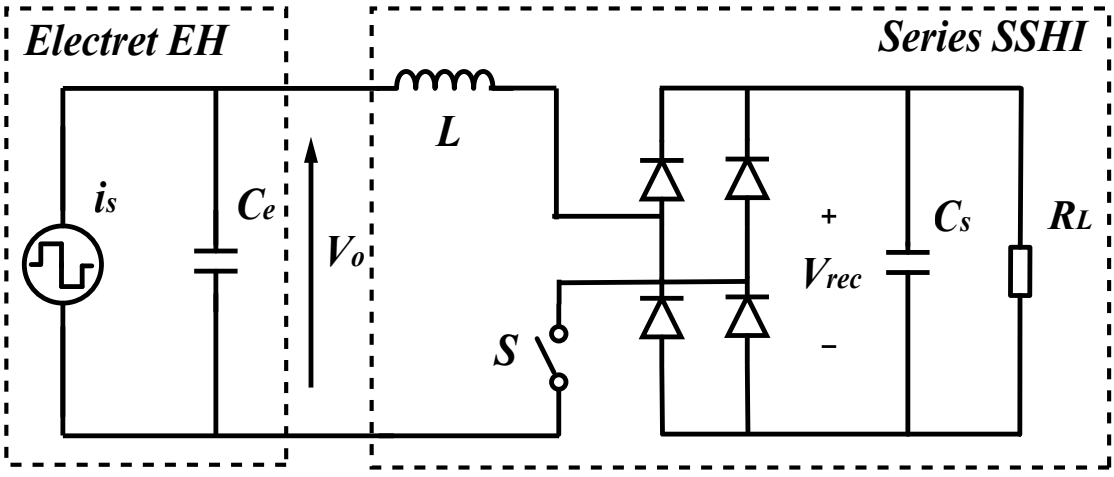


Figure 3-3 Series SSHI: rotational electret EH with series SSHI interface.

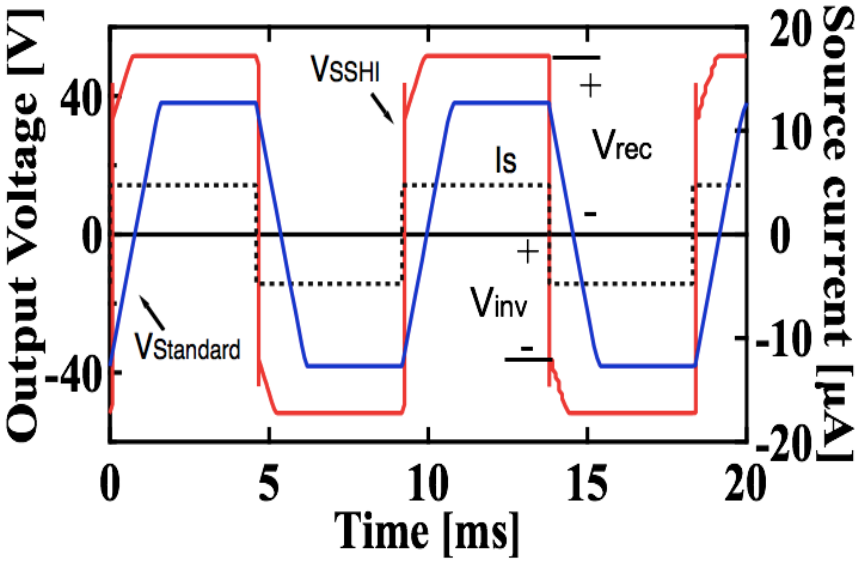


Figure 3-4 Typical waveforms in Standard and Parallel SSHI cases.

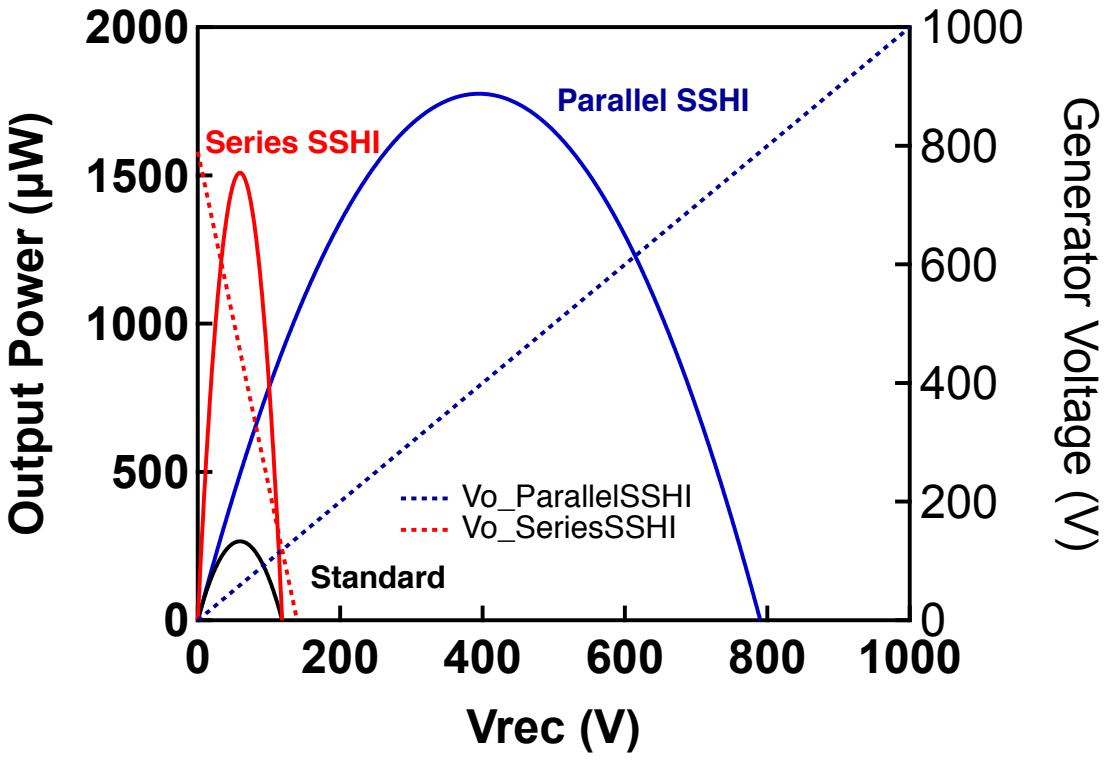


Figure 3-5 Theoretical performance of series SSHI and parallel SSHI on electret EH.

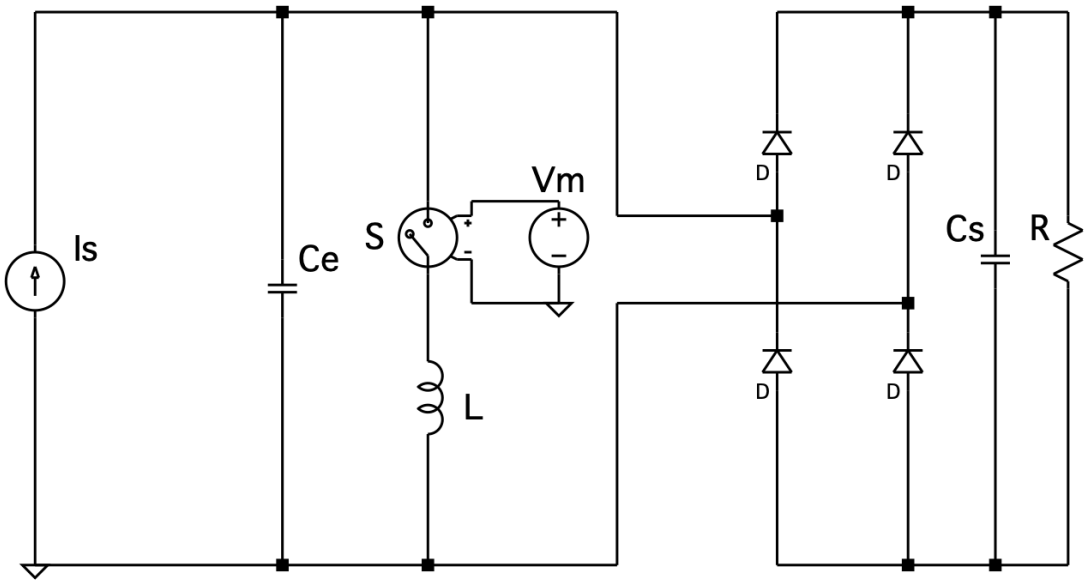


Figure 3-6 Simulation setup of ideal SSHI in LTspice.

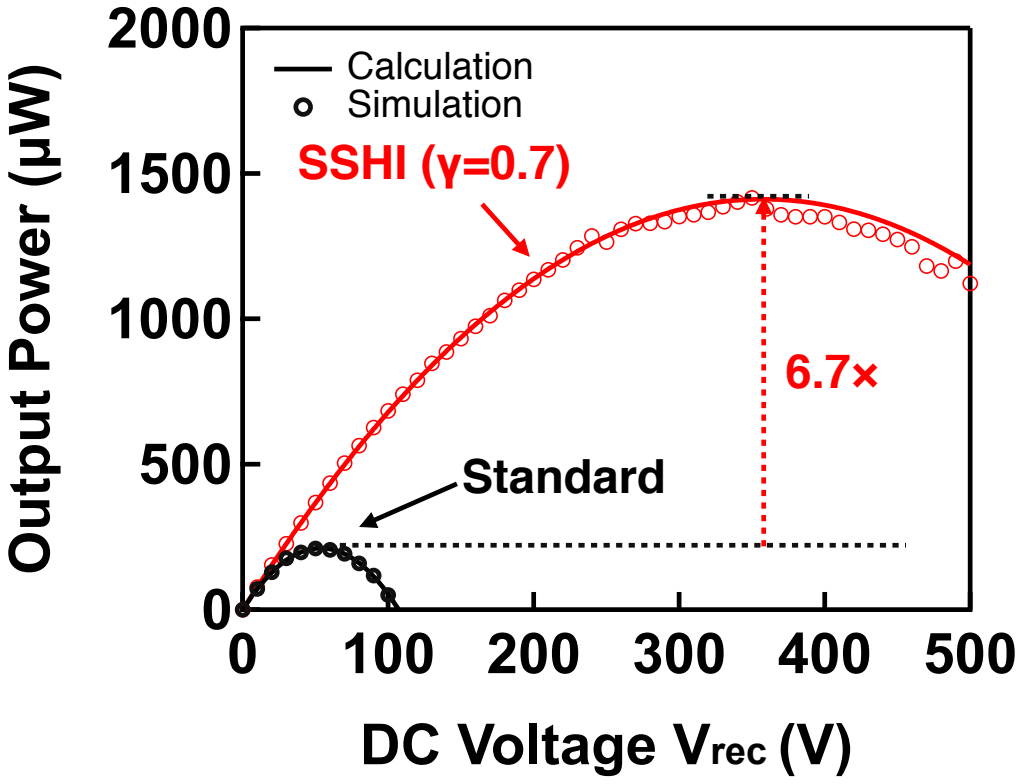


Figure 3-7 Output power as a function of rectified voltage in ideal SSHI case.

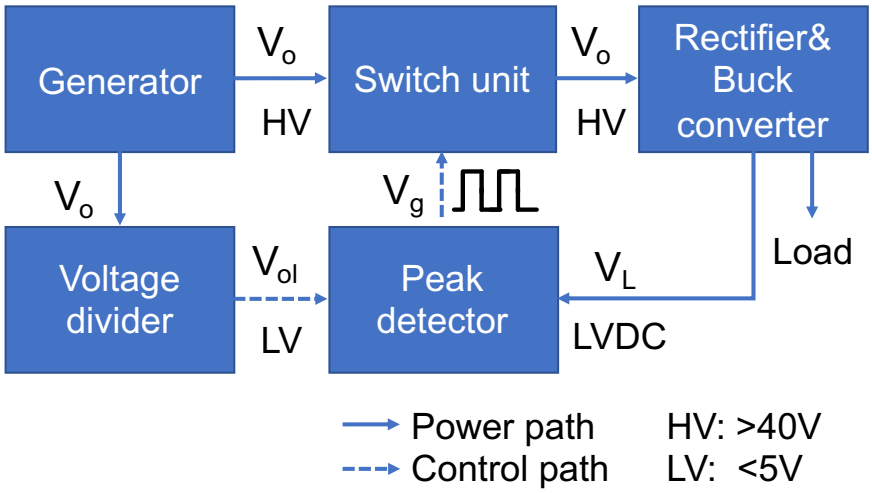


Figure 3-8 System design of SSHI for electret EH.

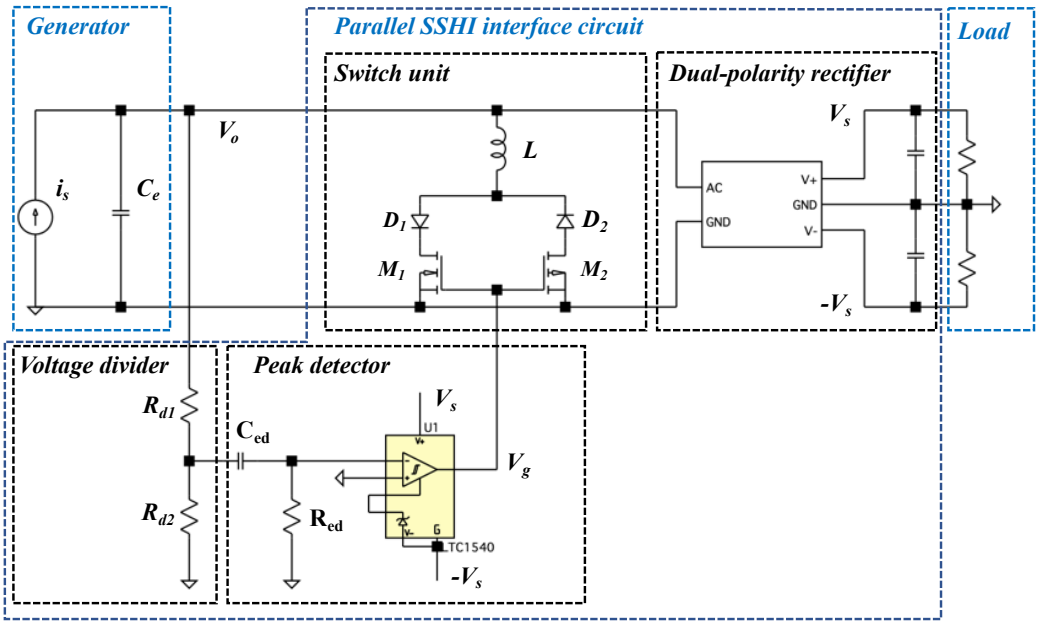


Figure 3-9 Circuit design of SSHI for electret EH.

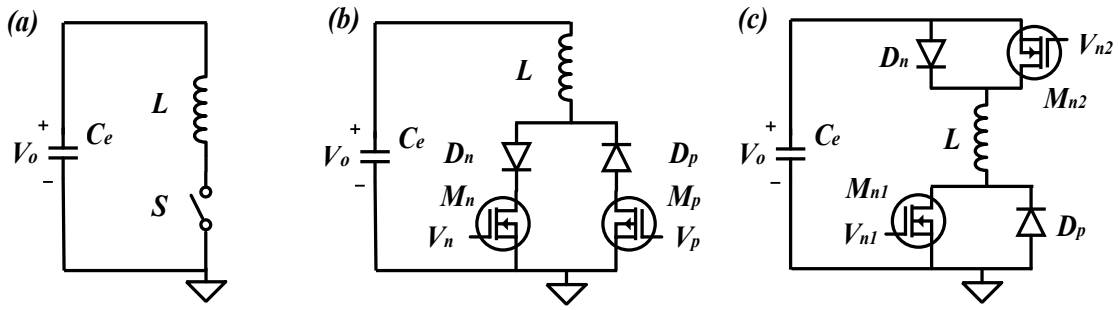


Figure 3-10 Switch configurations in SSHI: (a) schematic, (b) N-P configuration and (c) N-N configuration.

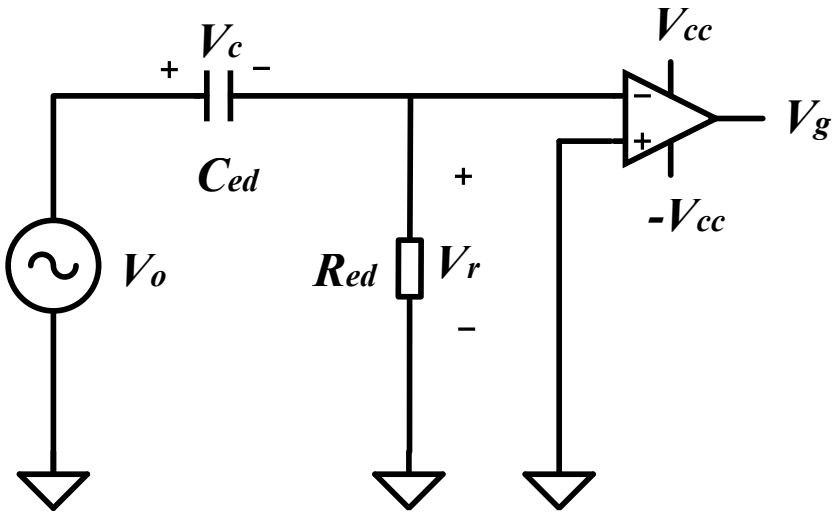


Figure 3-11 Peak detector for generating pulse V_g to the MOSFET switches.

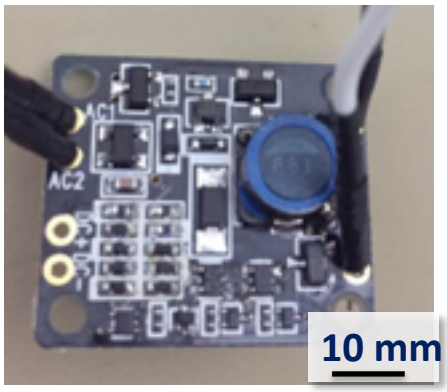


Figure 3-12 Unipolarity rectifier developed by OWL Co [109].

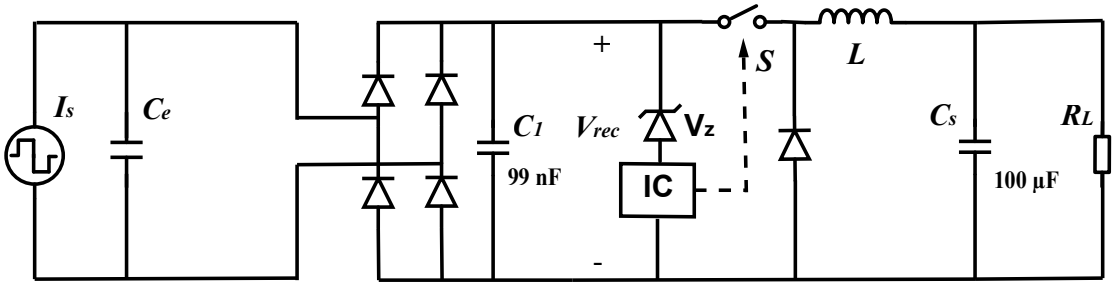


Figure 3-13 Schematic of the unipolarity rectifier circuit design.

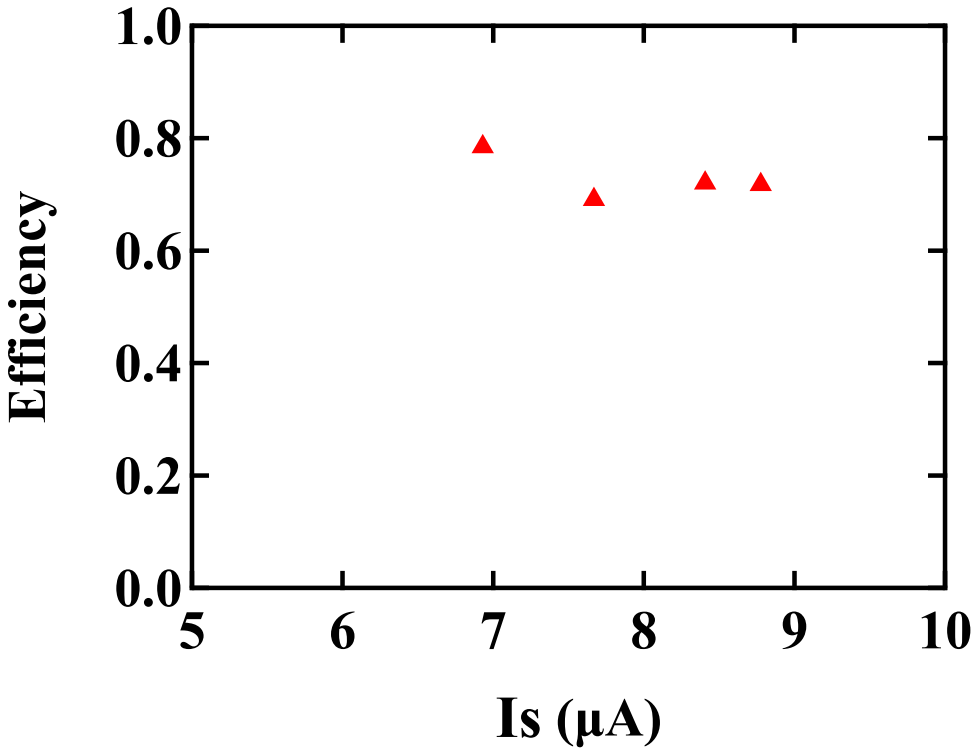


Figure 3-14 Measured results of converter efficiency as a function of generator source current I_s.

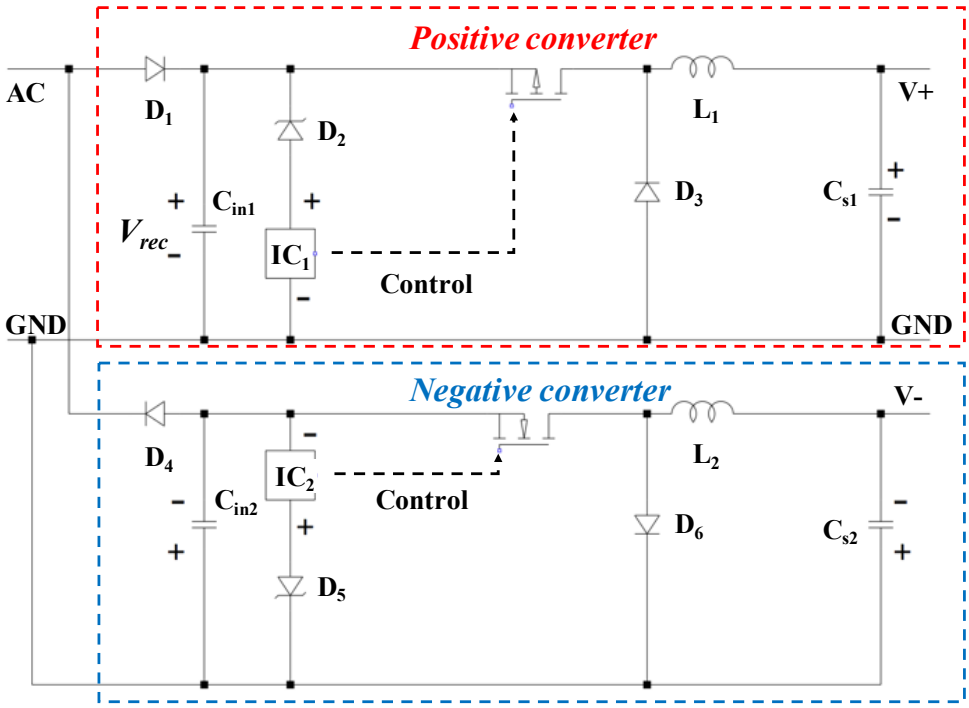


Figure 3-15 Circuit schematic of dual-polarity rectifier.

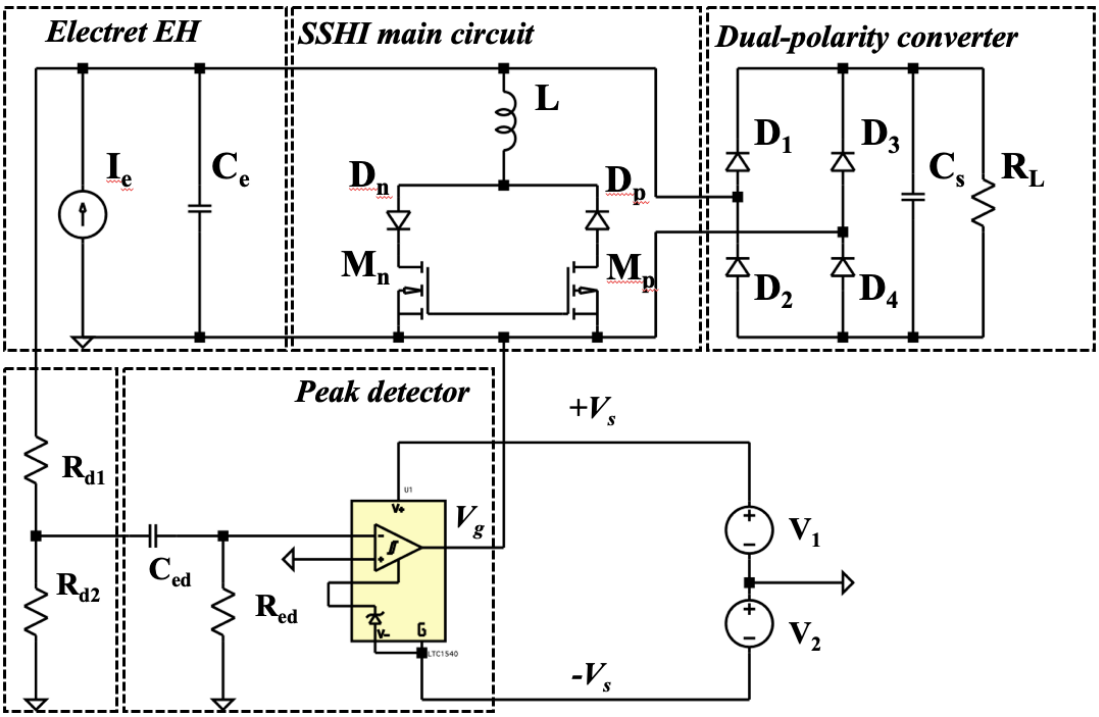


Figure 3-16 Simulation setup for voltage-divider SSHI (comparator externally powered).

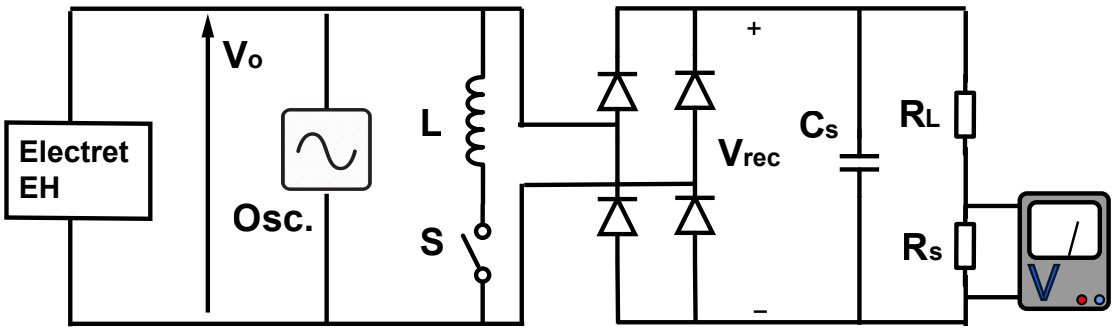


Figure 3-17 Schematic of measurement setup in Standard DC (*L*, *S* excluded) and SSHI cases.

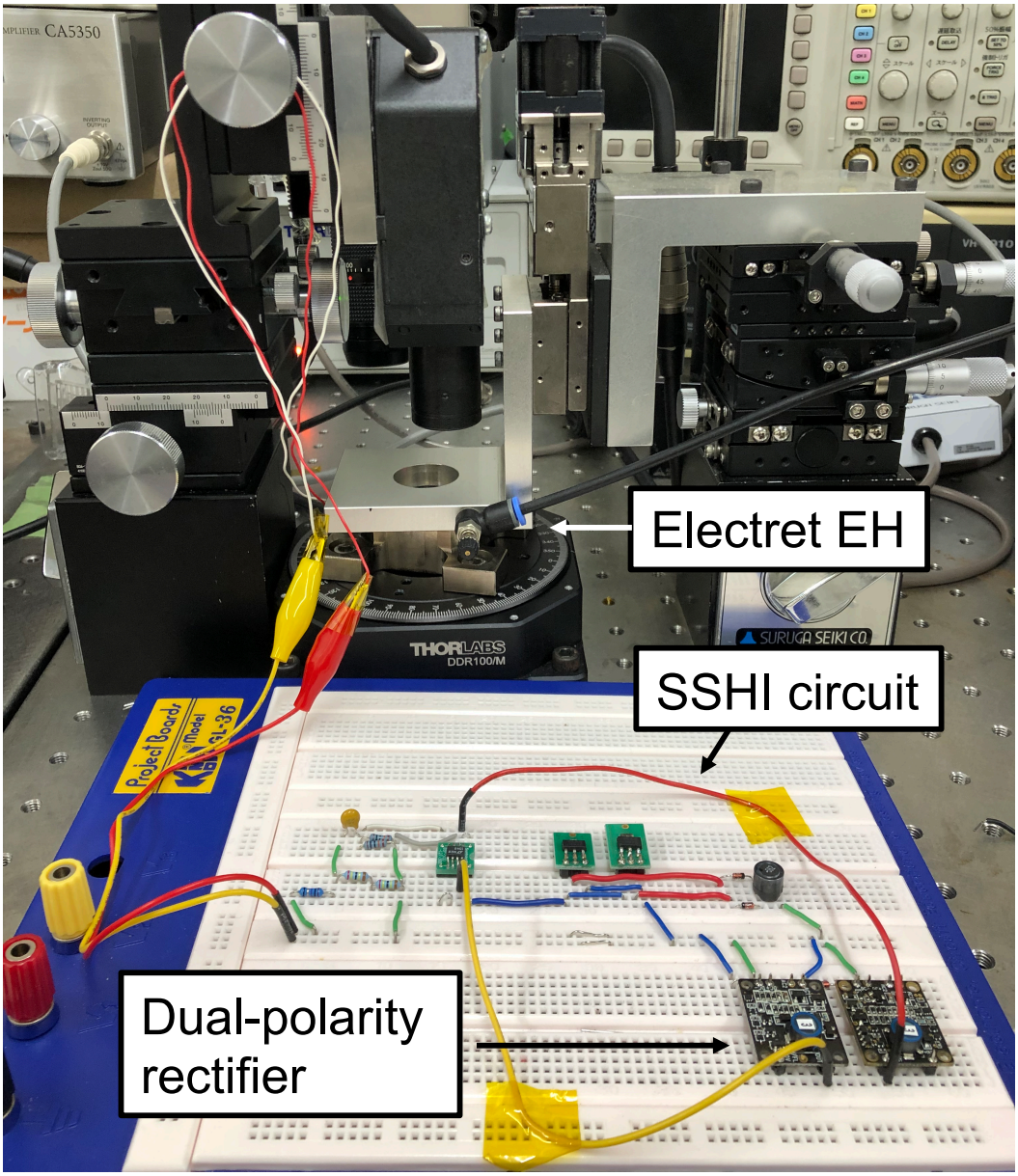


Figure 3-18 Experimental setup (dual-polarity rectifier excluded in external-powered SSHI)

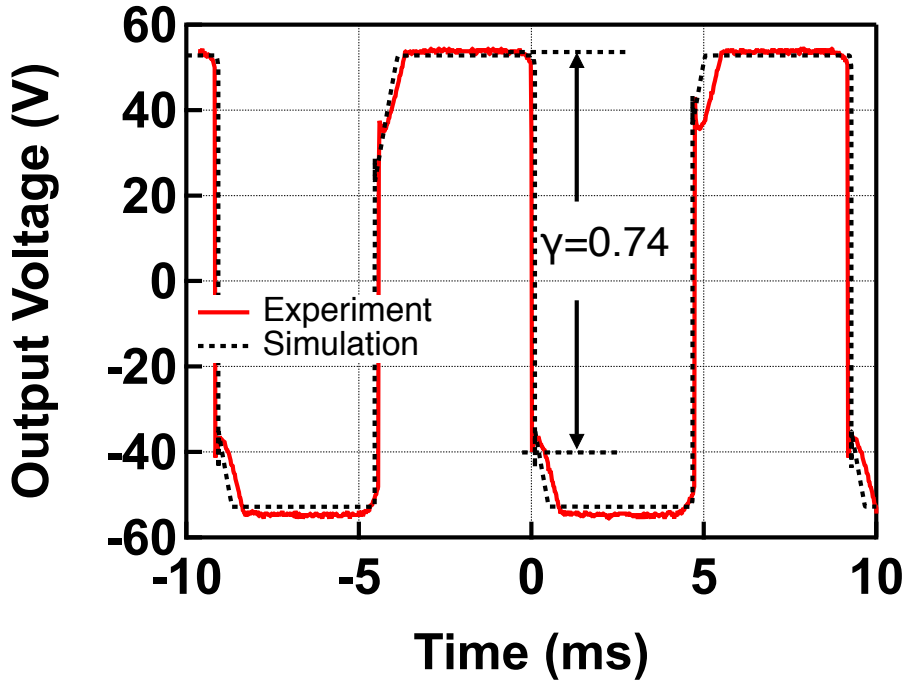


Figure 3-19 Simulated and measured output voltage with R_L=9 MΩ.

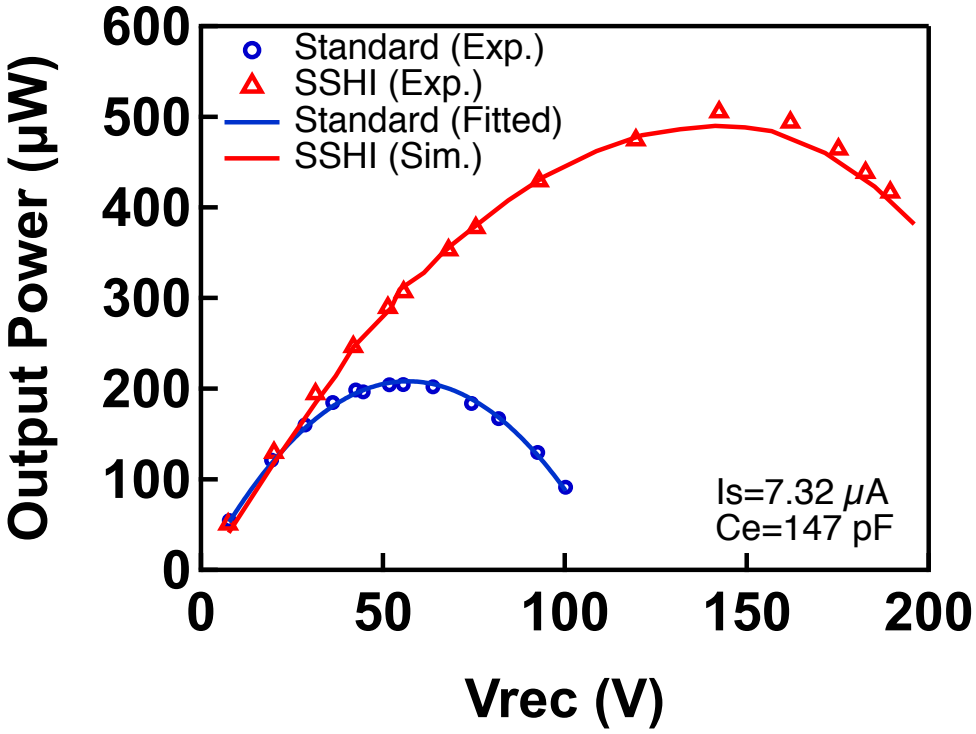


Figure 3-20 Simulated and measured output power as function of rectified voltage.

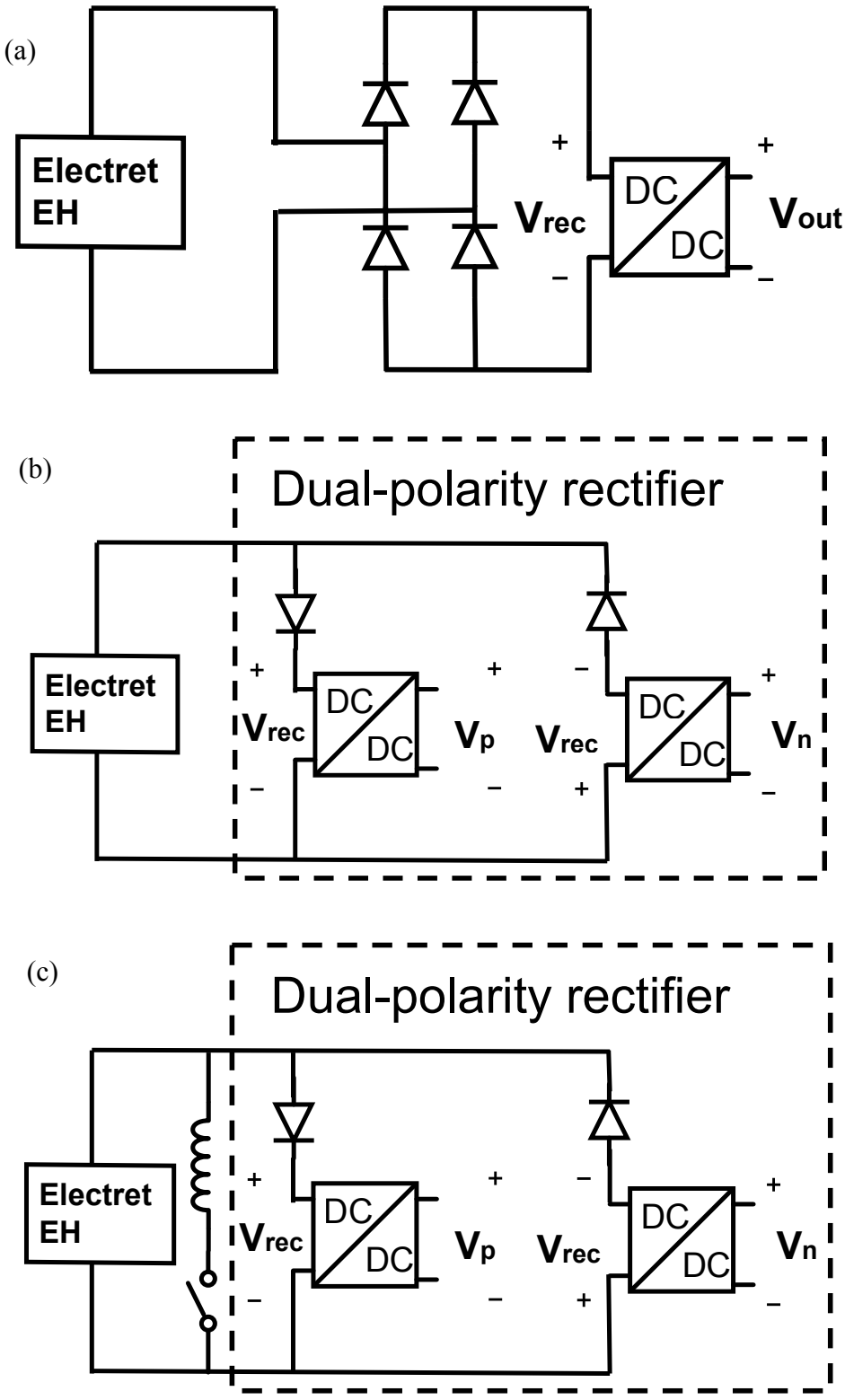


Figure 3-21 Cases studied for Self-powered SSHI: a) Standard case, b) Bi-standard case, c) Self-powered SSHI case.

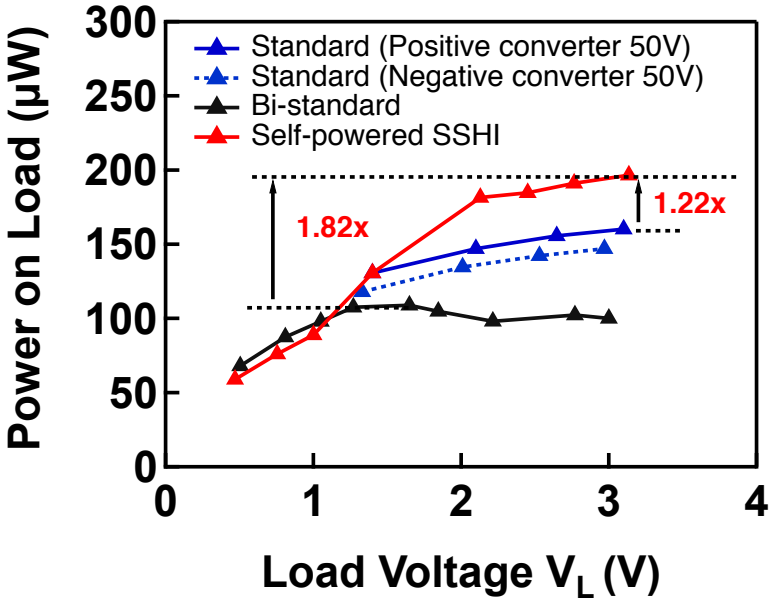


Figure 3-22 Power on load as a function of load voltage in self-powered SSHI.

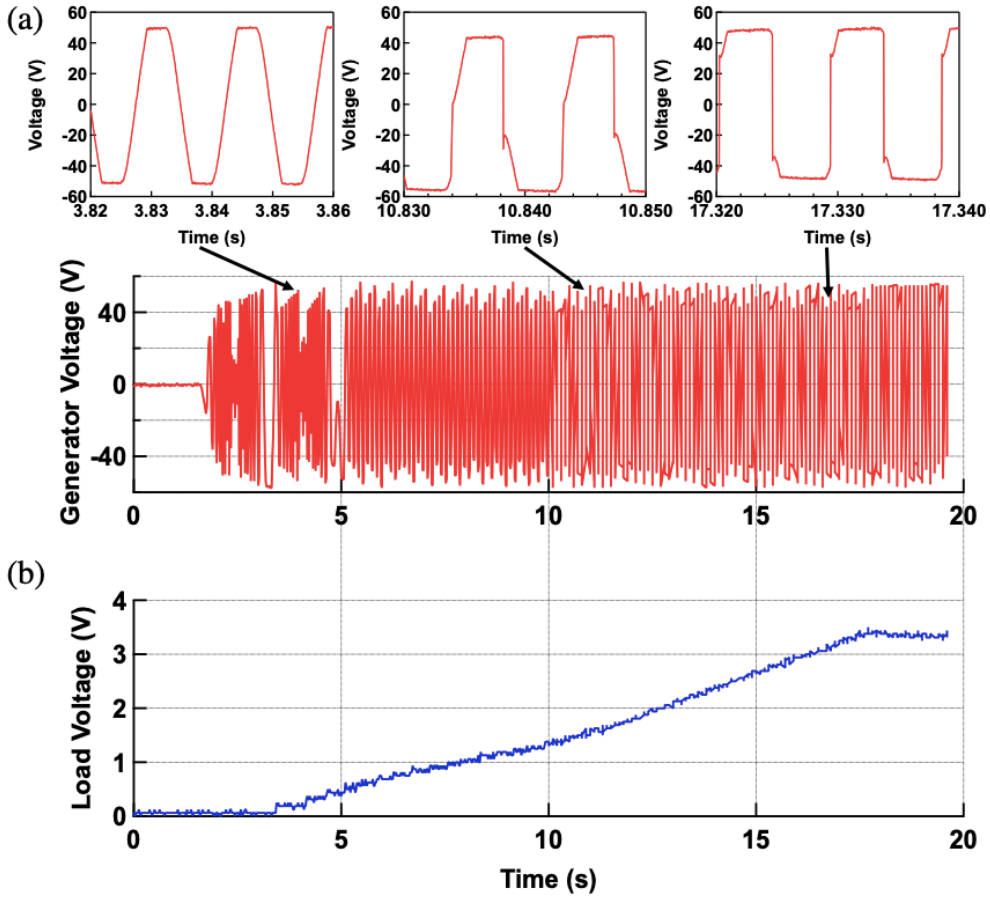


Figure 3-23 Cold-start of self-powered SSHI. a) Output voltage of rotational electret EH, b) Load voltage across the storage capacitor ($+V_s$).

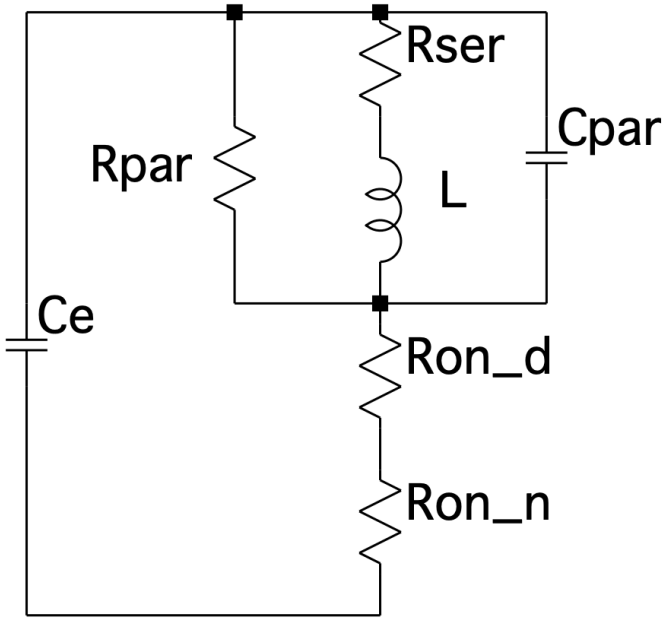


Figure 3-24 Circuit model of the LC resonant loop when switch is closed.

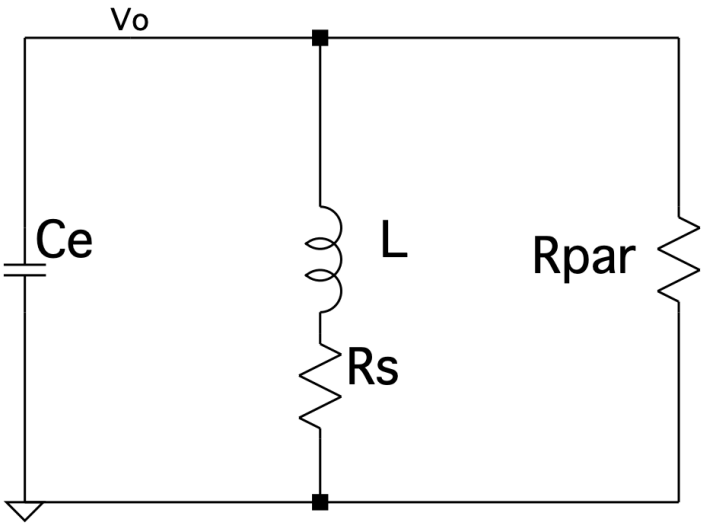


Figure 3-25 Simplified model of the LC resonant loop including R_{par}.

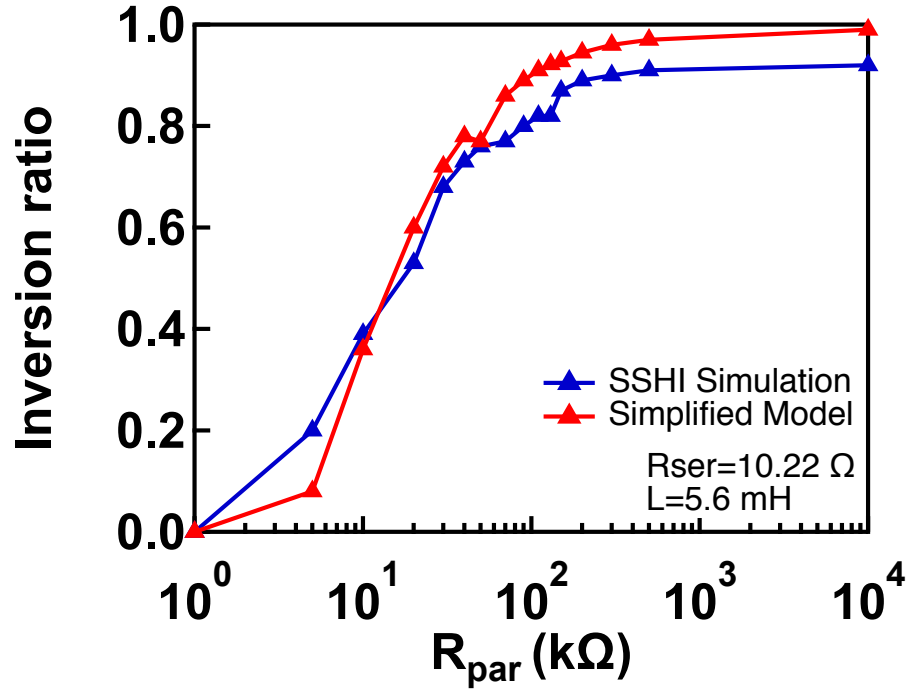


Figure 3-26 Inversion ratio as a function of the parallel resistance of inductor R_{par}.

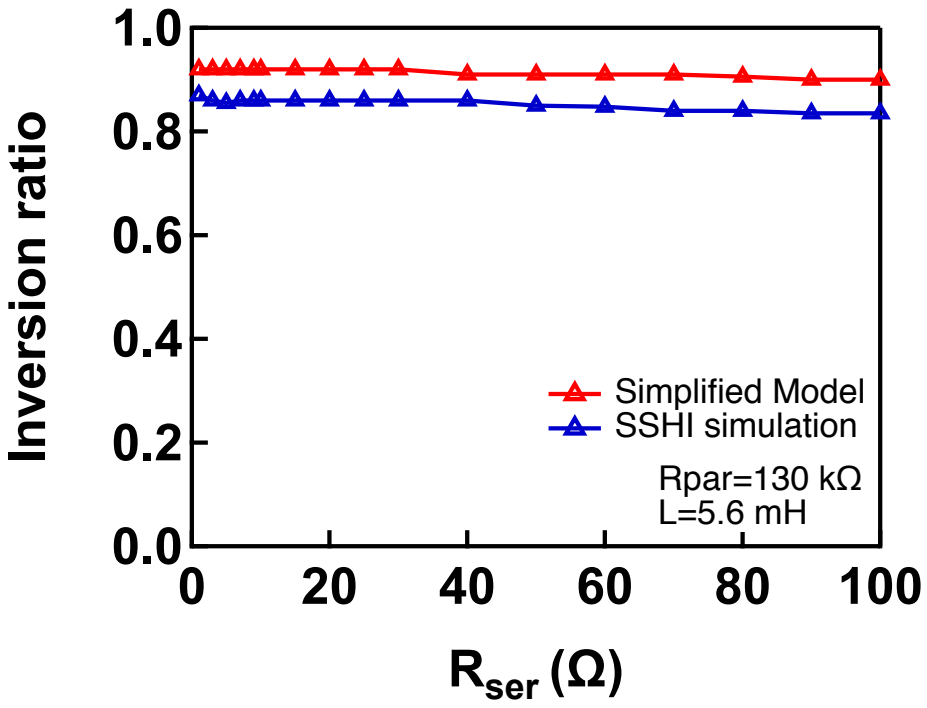


Figure 3-27 Inversion ratio as a function of the series resistance of inductor R_{ser}.

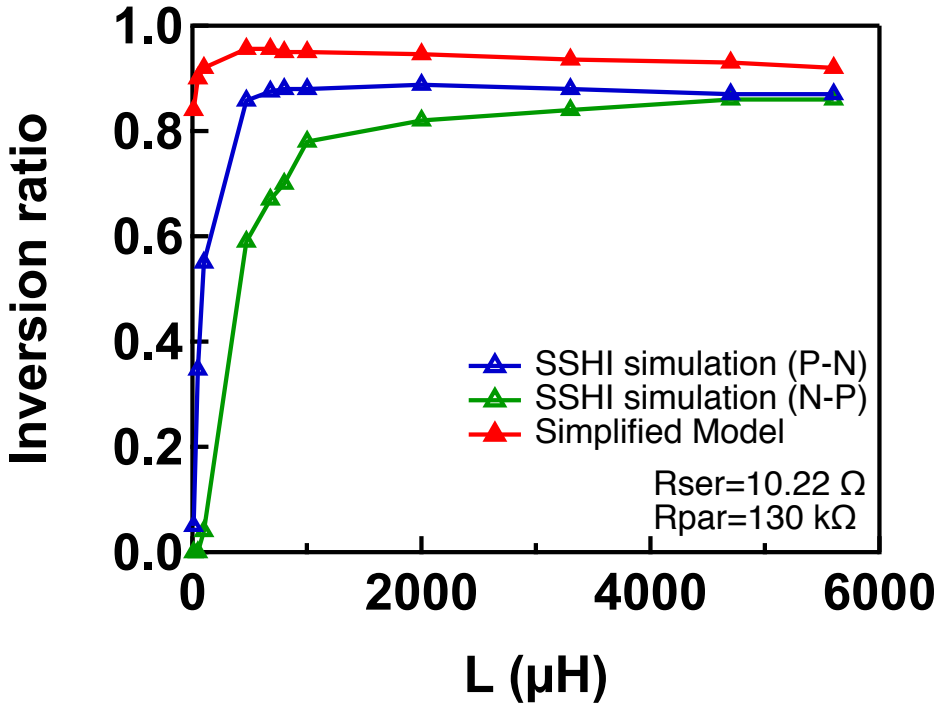


Figure 3-28 Inversion ratio as a function of the inductance of inductor *L*.

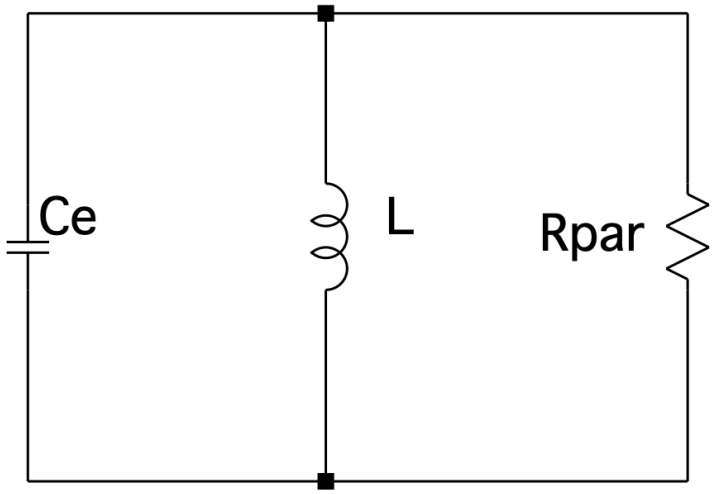


Figure 3-29 Parallel RLC circuit.

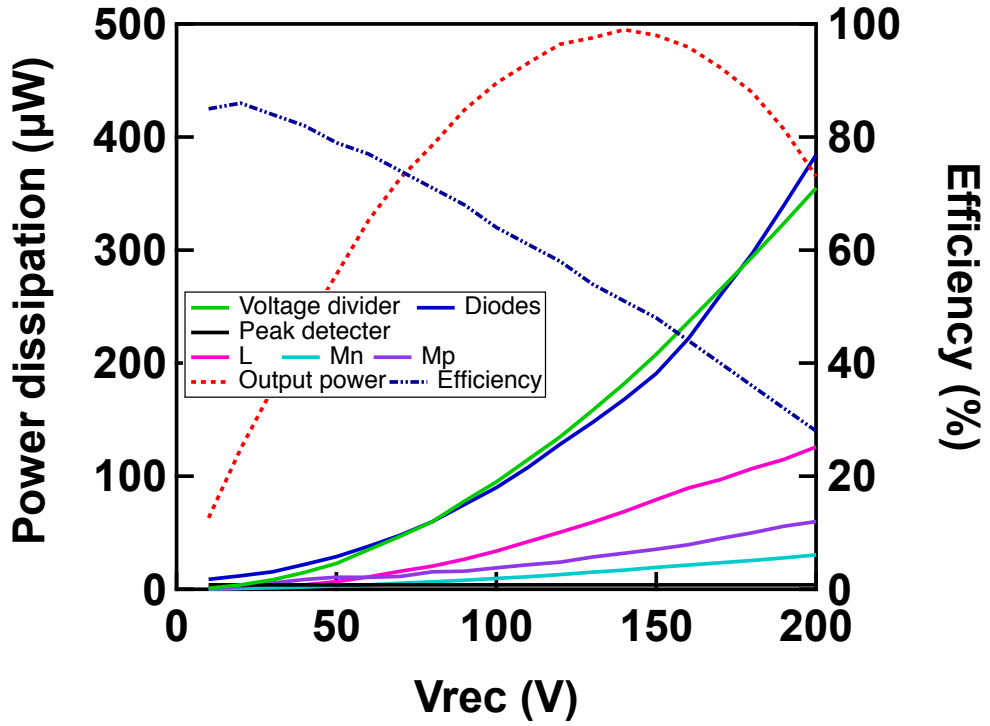


Figure 3-30 Power dissipation of components in voltage-divider SSHI.

Chapter 4 Dual-stage Synchronized Switch Harvesting on Inductor

In chapter 3, it is found that the voltage divider employed in SSHI design is one of the main bottlenecks to achieve efficient operation of SSHI. In this chapter, a dual-stage electrode design, in place of voltage divider, is proposed to achieve a more efficient SSHI operation.

4. 1. Dual-stage electrode design

Two types of dual-stage electrode design are proposed: radius-based and pole-number-based. Figure 4-1 shows a schematic of radius-based dual-stage design. It consists of a control stage (V_{ct}, V_{cg}) and a power stage (V_{po}, V_{pg}). The power stage, which occupies the majority of the total area, operates at high voltage for power generation. Meanwhile, the control stage, which occupies the minority of the total area, operates at low voltage for the control circuitry. Note that the current generated by the control stage is inherently in phase with that generated by the power stage, hence it is suitable to trigger the synchronized switch. Figure 4-2 shows a schematic of pole-number-based dual-stage design. In this case, a minority of poles constitutes the control stage; whilst a majority of poles constitutes the power stage. Figure 4-3 shows an enhanced SSHI circuit based on dual-stage electrode design. Compared with the voltage-divider SSHI, the control stage, instead of voltage divider, provides a low-voltage, isolated signal of generator output voltage to the peak detector.

The pole-number-based design has advantages upon radius-based design in a larger effective area, lower inter-capacitance between control and power stage and ease of lead-out. On the other hand, the radius-based design could lead to lower parasitic capacitance in the power stage, which is in favor of power generation. Since the distribution of parasitic capacitance in radial direction is not even, the inner part contributes the majority of parasitic capacitance. Therefore, the parasitic capacitance of power stage is equivalently reduced by making the inner part as control stage, if compared with the conventional uni-stage design.

4. 2. Comparison between dual stage and voltage divider

Table 4-1 shows a comparison between dual-stage SSHI and voltage-divider SSHI in terms of efficiency and reliability. The power loss led by control stage is lower than the voltage divider, and the switch action in dual-stage SSHI is immune to subsequent

Table 4-1 Comparison between dual stage and voltage divider in SSHI operation

	Voltage-divider SSHI	Dual-stage SSHI
Power loss	high	low
Interference with converter	Yes	No
High voltage spike on comparator	Yes	No
Efficiency	low	high
Reliability	low	high

converter operations. Therefore, dual-stage SSHI should be more efficient than voltage-divider SSHI. On the other hand, due to the isolation feature, control will not lead to high voltage spikes on comparator as the voltage divider do, resulting in higher reliability. These features will be elaborate as follows.

4. 2. 1. Power loss

Figure 4-4 shows a schematic of voltage-divider SSHI (Figure 4-4a) and dual-stage SSHI (Figure 4-4b). The power dissipated by the voltage divider P_{vd} is

$$\boldsymbol{P_{vd} = \frac{V_o^2}{R}} \tag{4-1}$$

where R is the resistance of the voltage divider, V_o is the output voltage of generator. On the other hand, since control stage is not utilized for power generation, the equivalent power loss is

$$\boldsymbol{P_{ds} = I_{ct} V_o} \tag{4-2}$$

Where I_{ct} is the generated current by control stage, V_o is the output voltage of power stage. Figure 4-5 shows a comparison of power loss between P_{vd} and P_{ds}, based on the parameters given in Figure 4-4. It reveals that dual-stage design can effectively reduce the power loss at high voltage.

Honestly speaking, this comparison may not be fair because it is based on a pair of instances of voltage divider and dual stage. In other words, it is possible to increase the resistance of voltage divider to achieve lower power dissipation in voltage divider case. In the meantime, it is also to possible to reduce the power loss of control stage by reducing r_{ct} in radius-based design or by reducing n_{ct} in pole-number-based design. a fair comparison can be carried out if we know the maximal limits of both designs in

practical implementation. However, this kind of experiment is not so interesting. Therefore, the comparison here aims to provide a generic trend.

4. 2. 2. Interference with subsequent converter

Figure 4-6 shows the measured output voltage in voltage-divider-based self-powered SSHI case. It is observed that the switch is triggered at some undesired points which do not correspond to the current zero-crossings of the generator. Actually, it is caused by the voltage drop due to power transfer from generator to load. Specifically, when the rectified voltage V_{rec} exceeds the rated voltage of the DC/DC converter, the switch in the converter is turned on to initial power transfer from C_1 to C_s (Figure 3-13), which leads to a voltage drop of V_{rec}. This voltage drop, which can be viewed a local peak, is detected by the peak detector via voltage divider and hence triggers the switch mistakenly. This undesired switch could lead to significant power loss as the generator needs to recover the voltage amplitude in several attempts afterwards.

Figure 4-7 shows the measured output voltage in dual-stage-based self-powered SSHI case. Thanks to the control stage isolated from the rectifier, the voltage drop in power stage will not conducted to control stage. Therefore, undesired switch actions have not been observed in dual-stage-based self-powered SSHI case. Therefore, dual-stage SSHI is more efficient in the self-powered operation than voltage-divider SSHI.

4. 3. Results

4. 3. 1. Simulation results

Figure 4-3 shows the simulation setup for dual-stage SSHI. the dual-stage rectifier is replaced by a storage capacitor in parallel with a load resistor.The generator parameters in dual-stage and voltage-divider SSHI cases are listed in Figure 4-4. The output current and shunt capacitance of each stage are calculated based on the proposed model. The circuit parameters are identical in both cases. Note that R_{ed}=2.4 MΩ in this case.

Figure 4-8 shows the simulated output power in standard, voltage-divider SSHI and dual-stage SSHI cases. It is clear that dual-stage SSHI harvests more power with the rectified voltage increasing.

4. 3. 2. Experimental results

The radius-based design is chosen for SSHI for the first attempt. Figure 4-9 shows the fabricated dual-stage electrode. Since control stage and power stage in SSHI share a common ground, it has three terminals including a common ground. The large portion of the electrode in the outer part (10 mm < r <20 mm) constitutes power stage. On the other hand, the smaller inner part (9 mm < r < 10 mm) constitutes control stage.

Figure 4-10 shows the experimental setup for dual-stage SSHI which is quite similar to that for voltage-divider SSHI, except that voltage divider is replaced by control stage. The measurement setup is identical with that in voltage-divider SSHI case. Figure 4-11 shows the measured output voltage in external-powered SSHI case. An inversion ratio of 0.8 was obtained. **Figure 4-12** shows the output power versus load. With the present SSHI circuit, 582 μW has been obtained for a rectified voltage Vrec=230 V, which is 4.2 times higher than with the standard full-bridge rectifier where conventional electrode design is employed. Moreover, power harvested in the present dual-stage case is 1.56 times higher than that in the voltage-divider case, indicating a more efficient SSHI by using the present dual-stage strategy.

Figure 4-13 shows the power generation results. By comparing bi-standard and self-powered SSHI case, we can observe the power enhancing effect of SSHI without the influence of converters. Consequently, 2x power gain was obtained in self-powered SSHI case against bi-standard case.

Finally, the overall performance of self-powered SSHI case is evaluated by comparing standard and self-powered SSHI cases. A moderate 1.41x power gain is achieved in self-powered SSHI case. The limited performance is mainly resulted from low efficiency and low voltage rating (50V) of dual-polarity converter.

4. 4. Implementation on the integrated rotational electret EH

4. 4. 1. Energy harvester fabrication

It would be more interesting if the proposed dual-stage SSHI could effective with the generator excited by real-world random excitation. In this regard, dual-stage SSHI is implemented on a fully-integrated rotational electret EH.

In this generator, print circuit boards (PCBs) are used for the electret and electrode substrates. To reduce the parasitic capacitance between the adjacent electrodes, 170 μm-thick PCB with low permittivity (ε=2.4) is used as the stator substrate for the

current collector electrodes (Figure 4-14a). The outer/inner diameters are 38 mm and 18 mm, respectively. Number of poles for the control stage is 115 while 4 poles serve as the control stage. The parasitic capacitance of the power stage is 110 pF. On the other hand, 105 μm-thick glass-fiber-reinforced PCB is employed for the electret substrate (Figure 4-14b) in order to minimize deformation during the thermal curing process of the electret material. The minimum electrode width is 185 μm, and the gap between comb electrodes are chosen as 50 μm. Both PCBs have backside electric contact for charging/ extracting power. 15 μm-thick CYTOP EGG is spun-on the rotor PCB with patterned electrodes. Only the CYTOP film above the base electrode is charged with soft X-ray. Then, the rotor is assembled with the stator and the high-precision ball bearing as shown in Figure 4-15. The assembled rotational EH has the air gap of 300 μm. Surface voltage of electret is -807 V. Note that the mechanical damping of the bearing is as low as 20 % of the estimated electrostatic damping.

4. 4. 2. External-powered SSHI results

In order to evaluate the effectiveness of proposed SSHI with dual-stage electrode design, power generation experiments are carried out using the assembled generator and discrete electronic components listed in Table 4-2. In the present experiment, the rectifier and buck converter are replaced by a resistor, corresponding to the SSHI-AC case. In this case, the comparator is externally powered by a DC power source, but its power consumption is below 6 μW. In the standard case, the resistive load is directly connected to generator output. In the voltage-divider SSHI case, the voltage divider is employed to generate low-voltage signal. In dual-stage SSHI case, control stage generates low-voltage signal. Note that in standard and voltage-divider SSHI cases, V_{po} and V_{ct} are connected to employ all 119 poles for power generation.

Table 4-2 Parameters in circuit design of dual-stage SSHI for PCB-based electret EH

Definition	Value	Definition	Value
I_{po}	8.61 μA	M_1	BSP89
I_{ct}	0.38 μA	M_2	BSP92p
C_{po}	110 pF	D_1, D_2	BAV21
C_{ct}	4 pF	Comparator	LTC1540
L(r)	5.6mH(4.9Ω)	C_{ed}	100pF
Rectifier	Dual-polarity	R_{ed}	2.4MΩ

In the present study, the generator is driven by hand motion. Since it has 120 (including 1 void) poles, a rotational speed of 1 rps should correspond to a 120 Hz output voltage. In view of the high load resistance (up to 100 MΩ), the power is calculated from the measured load current rather than the load voltage. By measuring the voltage across a 100 kΩ sampling resistor in series with load, the load current is calculated.

Figure 4-16 shows the measured output voltage of rotational electret EH with the dual-stage SSHI. The load resistance is chosen as 100 MΩ. An inversion ratio γ as high as 0.8 is obtained. Figure 4-17 shows the power generation results. 143 μW has been obtained on load with the proposed dual-stage SSHI, which is 2.6 times and 1.33 times more power than the standard case and the voltage-divider case, respectively.

4. 4. 3. Self-powered SSHI results

The aim of this section is to validate the cold-start and self-powering ability of the proposed SSHI circuit under random excitation. The power enhancing performance is difficult to quantitatively define, because it is hard to maintain the rotor motion in a fixed manner using the fully-integrated electret EH, which can be achieved using test bench.

Figure 4-18 shows the experimental setup for validating the cold-start and self-powering ability of the proposed SSHI circuit under random excitation. Voltage-divider SSHI is chosen because it has similar performance with dual-stage SSHI at V_{rec}=40V, which is the input voltage rating of the dual-polarity converter.

Figure 4-19 show the generator output voltage and load voltage during the cold-start process under unloaded condition. When the load voltage is null, the circuit works in standard DC mode (Figure 4-20) to charge the storage capacitor. When the load voltage across the storage capacitor exceeds the lower limit of the comparator's supply voltage (1.6V), SSHI is activated (Figure 4-21). With the load voltage increasing, the supply voltage for the control block increases, which lead to higher inversion ratios in SSHI (Figure 4-22). Note that the upper limit of load voltage is 3.3 V due to the output protection of the converter.

4. 5. Summary

In this chapter, a novel dual-stage electrode design is proposed for efficient SSHI by removing the lossy voltage divider. The following results are obtained:

(1) A power enhancing ratio of 4 upon standard case is experimentally achieved in dual-stage SSHI (externally powered), which is 1.56 times of the power harvested with the voltage-divider SSHI. Therefore, the efficiency of SSHI is enhanced by dual-stage design. However, the power enhancing ratio reduces to 1.4 in the self-powered SSHI, indicating an overall efficiency of 25%, due to the low voltage rating and low efficiency of the dual-polarity converter.

(2) The proposed dual-stage SSHI is successfully implemented to a fully-integrated rotational electret energy harvester, with power enhancing performance confirmed. Moreover, the self-start and self-powering ability of dual-stage SSHI under random excitation is also confirmed using this fully-integrated generator.

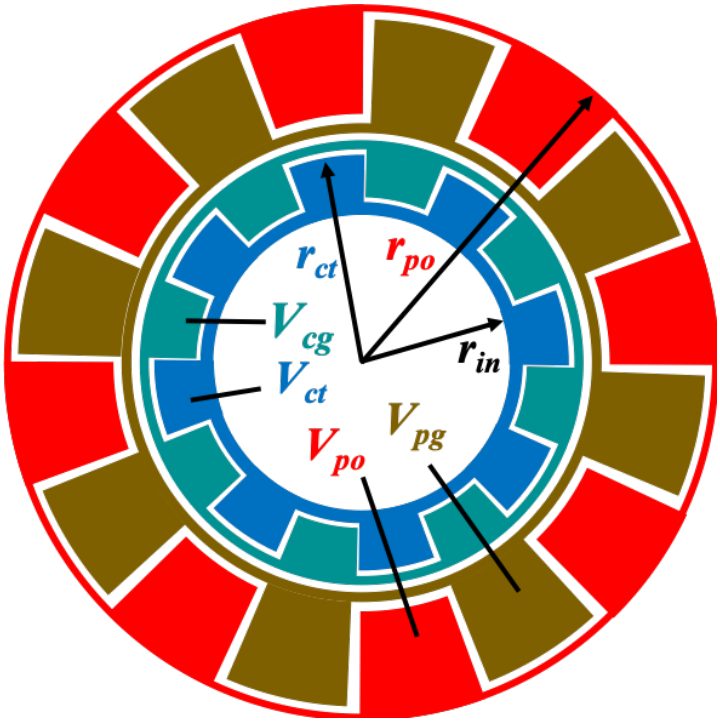


Figure 4-1 Schematic of radius-based dual-stage design.

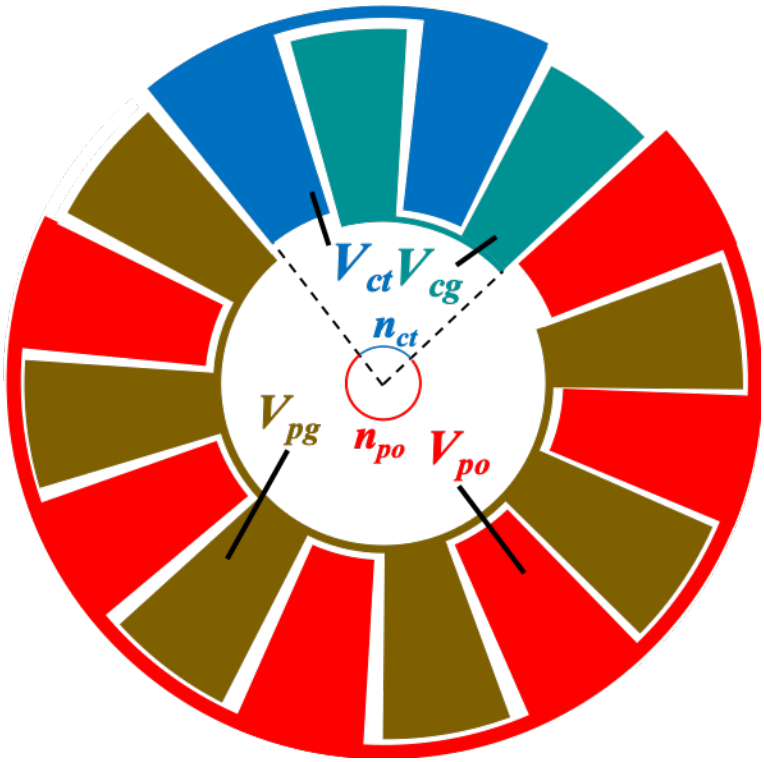


Figure 4-2 Schematic of pole-number-based dual-stage design

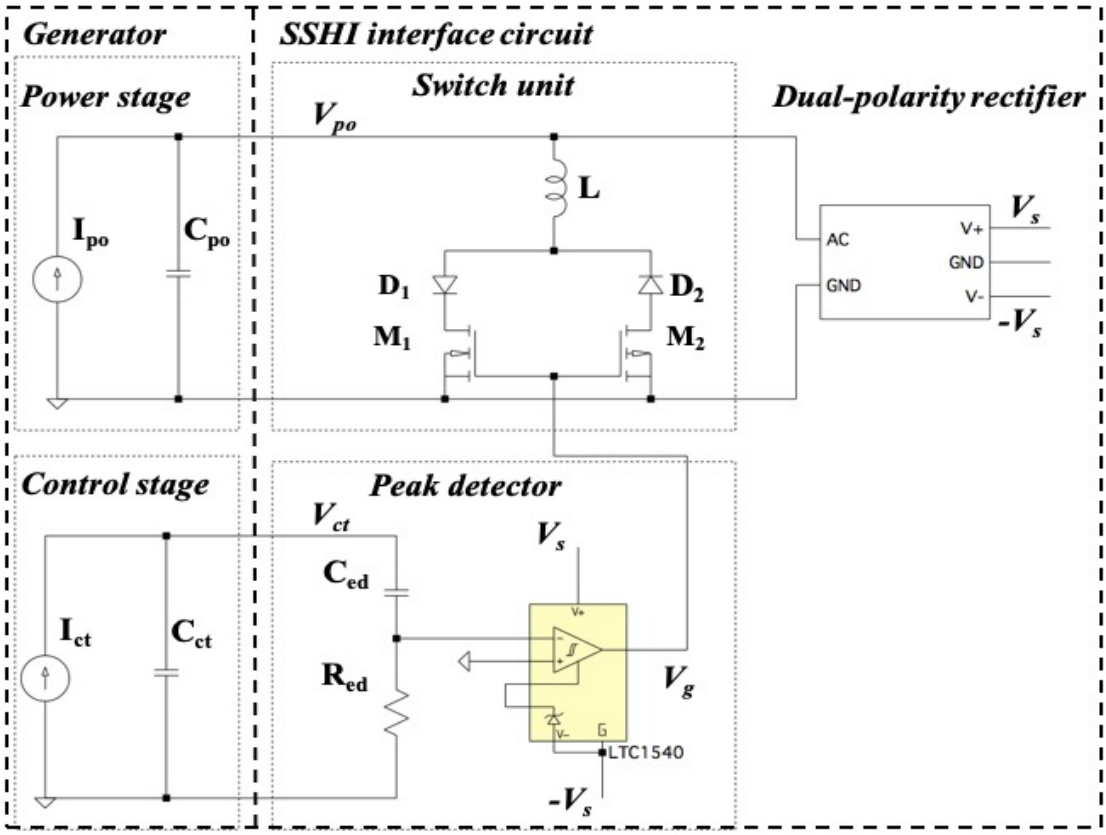


Figure 4-3 Dual-stage SSHI circuit design.

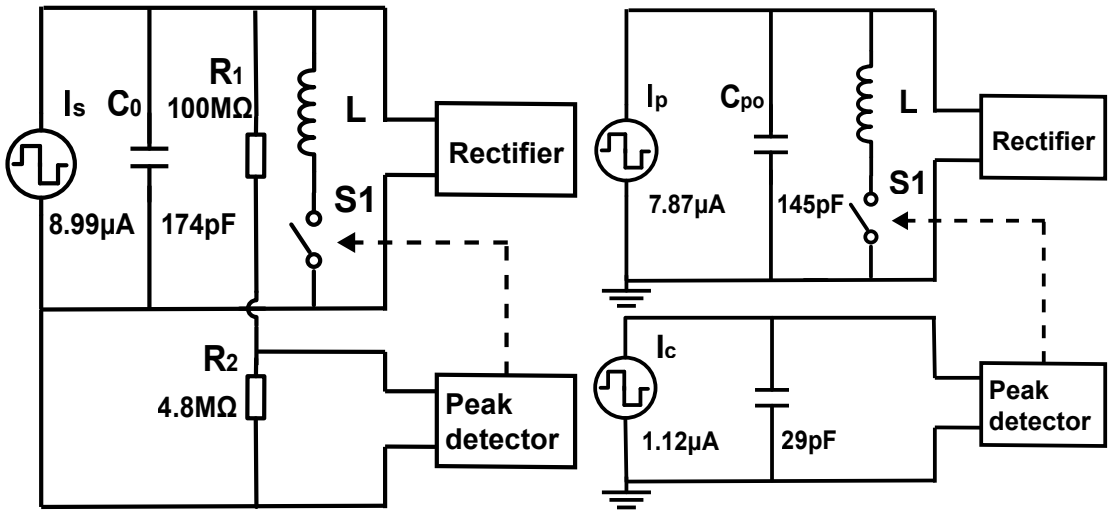


Figure 4-4 Schematic of (a) voltage-divider SSHI and (b) Dual-stage SSHI for loss comparison.

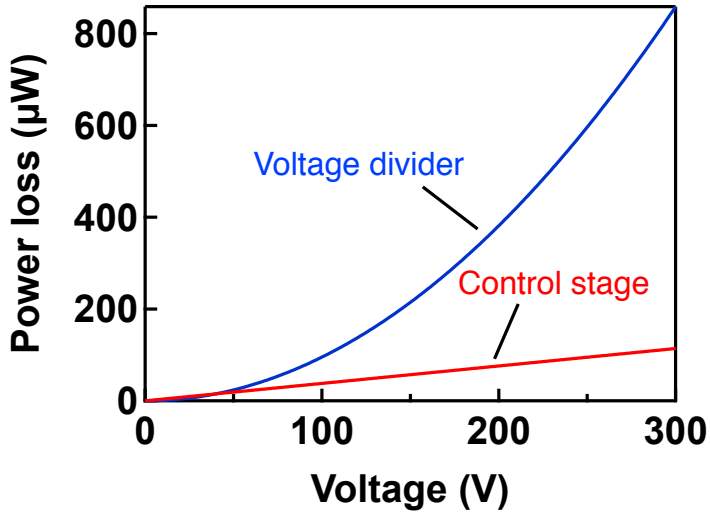


Figure 4-5 Power loss of the voltage divider and the control stage as a function of applied voltage.

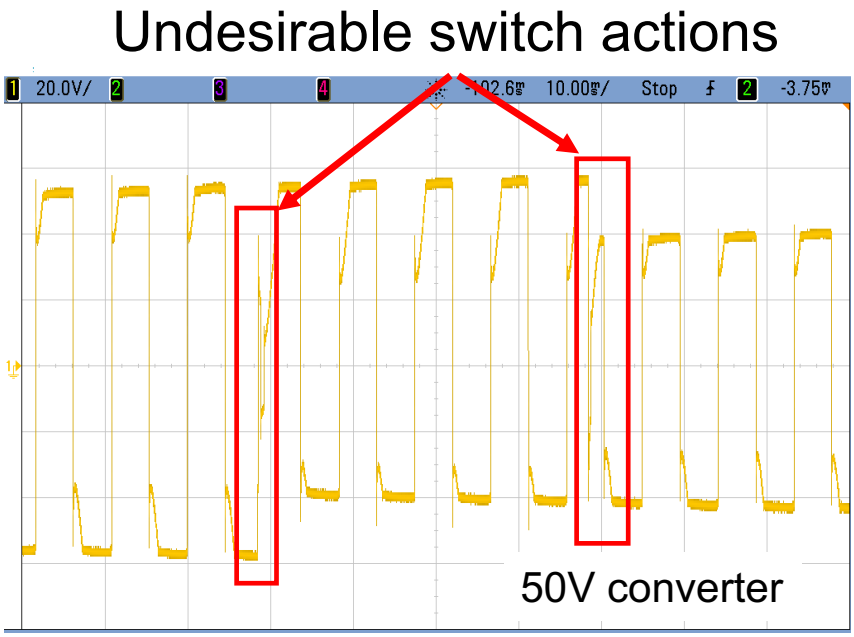


Figure 4-6 Output voltage in voltage-divider self-powered SSHI case.

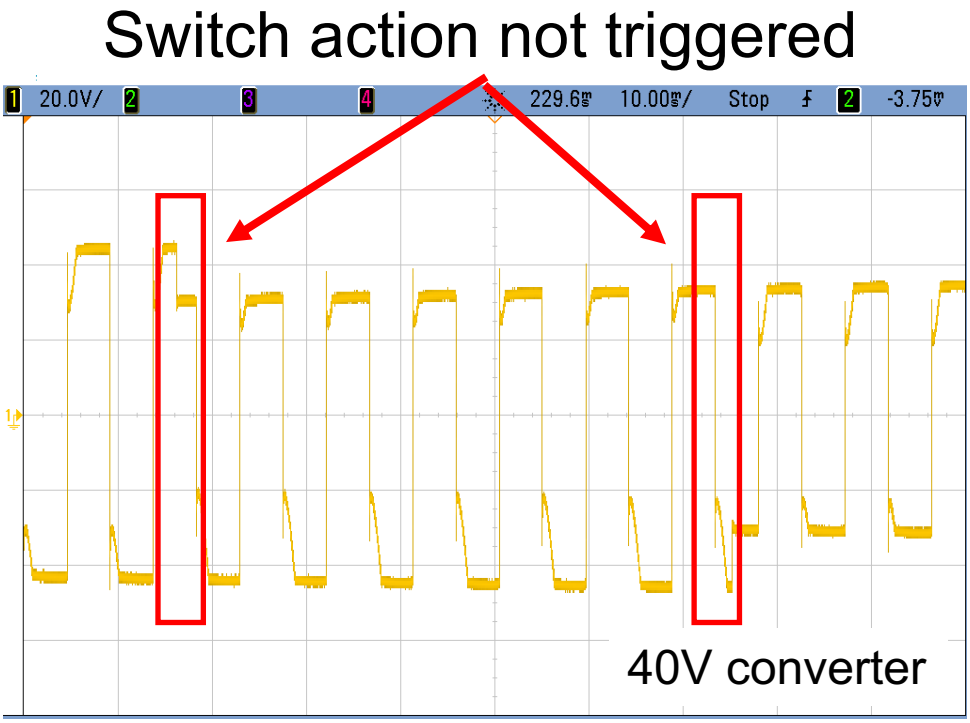


Figure 4-7 Output voltage in dual-stage self-powered SSHI case.

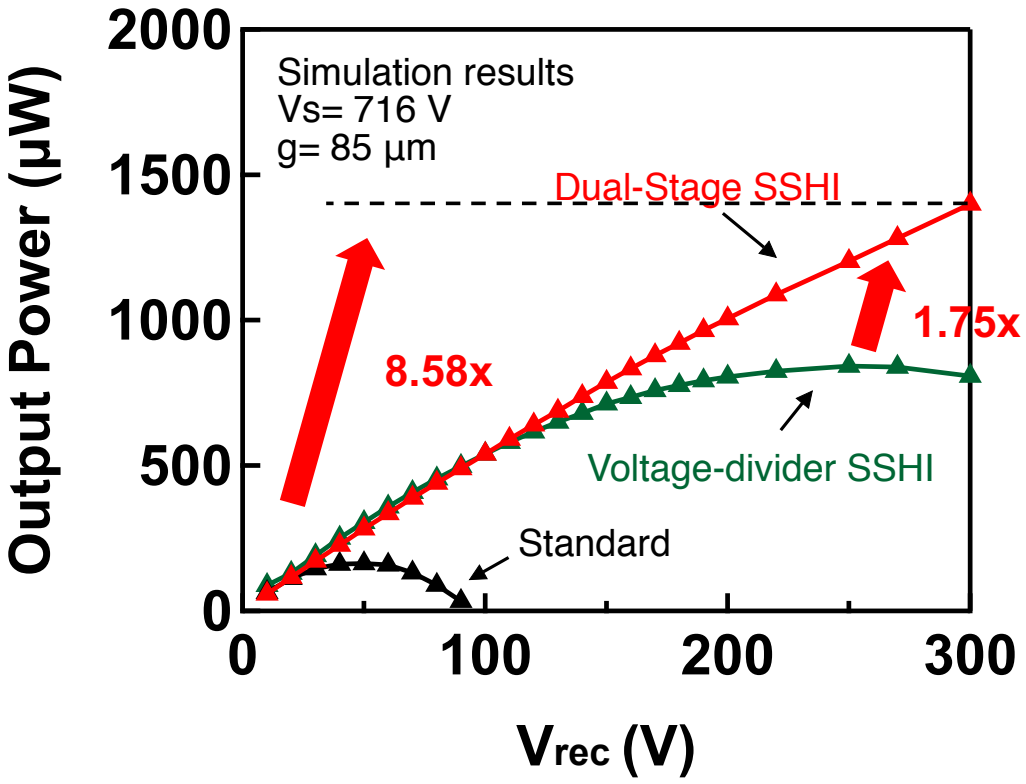


Figure 4-8 Simulated output power as function of rectified voltage in standard, voltage-divider SSHI and dual-stage SSHI cases.

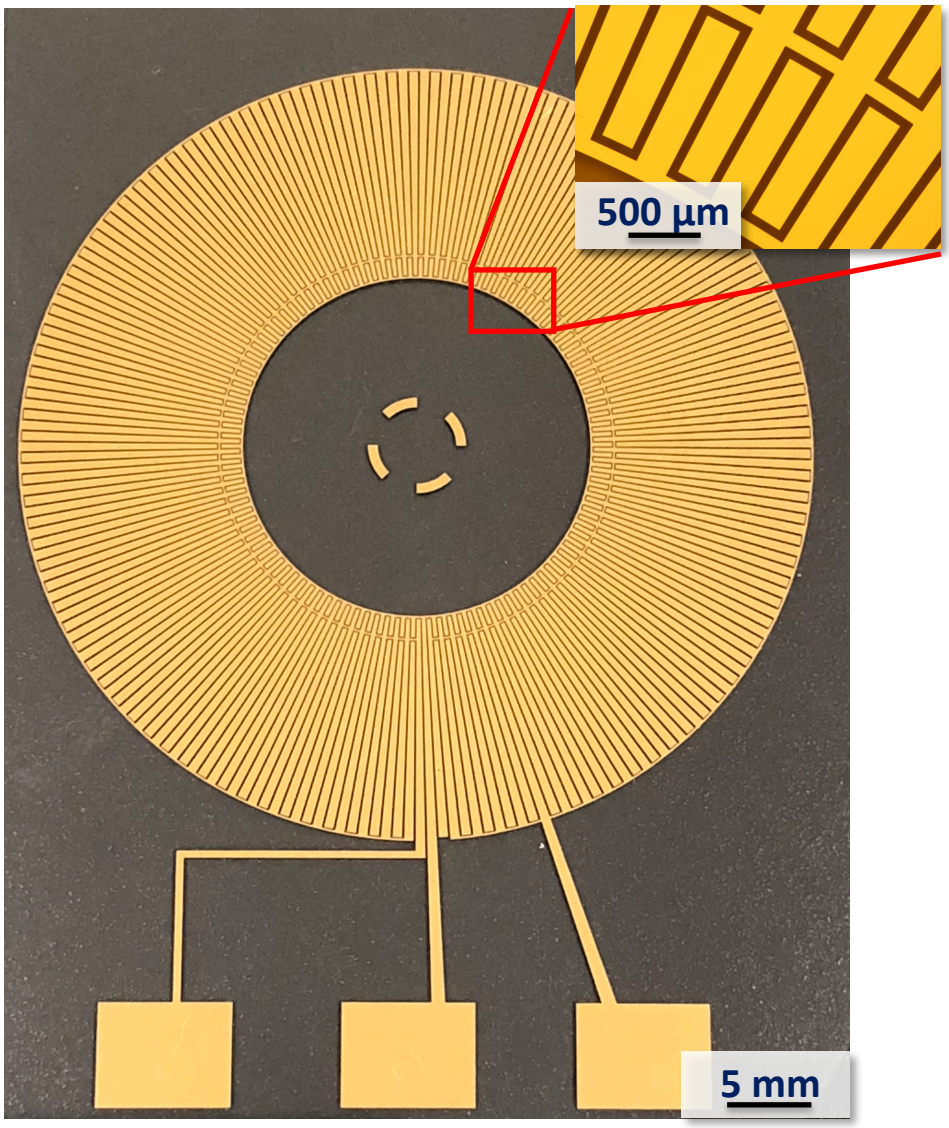


Figure 4-9 Radius-based dual-stage electrode (control stage :9 mm< *r*<10 mm; power stage (10 mm< *r* < 20 mm).

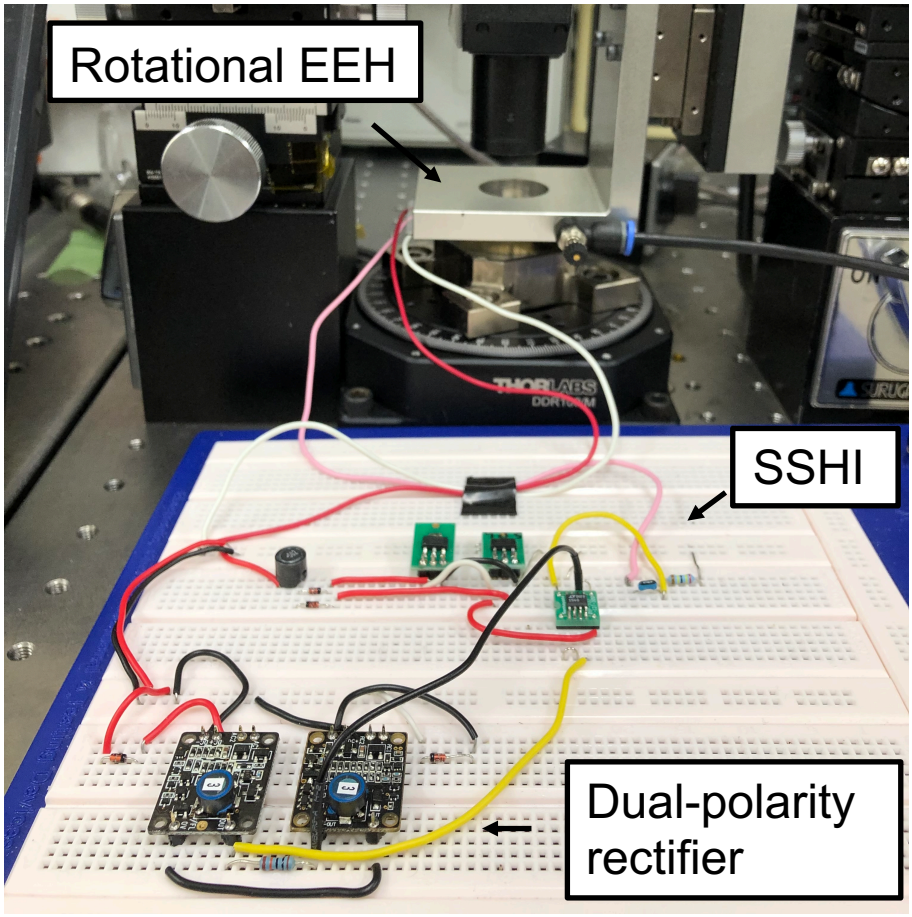


Figure 4-10 Experimental setup of dual-stage SSHI.

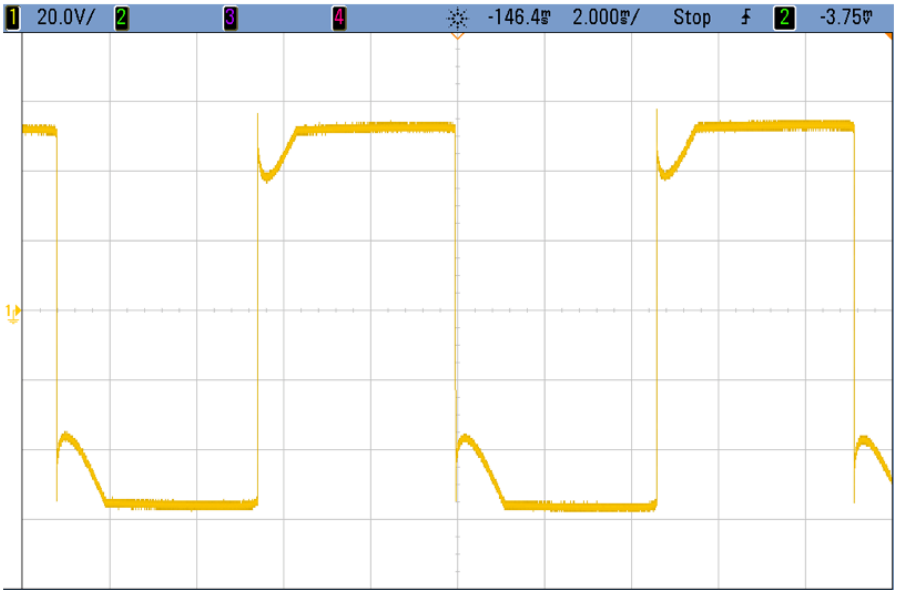


Figure 4-11 Measured generator output voltage with dual-stage SSHI (R_L=9 MΩ).

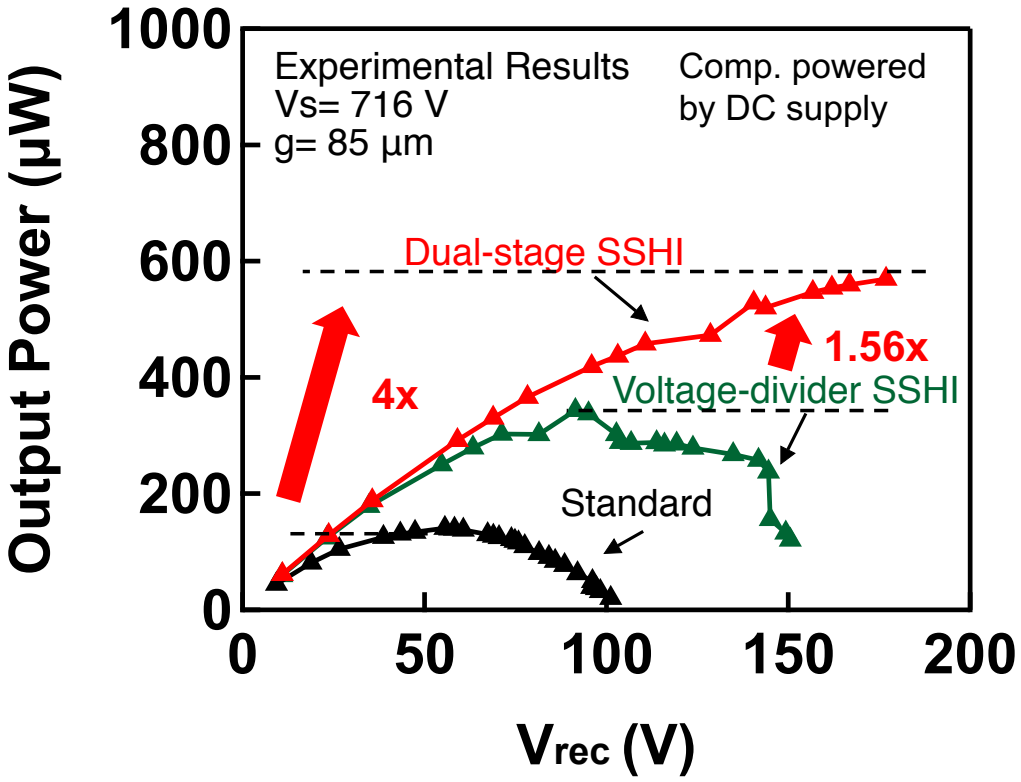


Figure 4-12 Measured output power as a function of rectified voltage in standard, voltage-divider SSHI and dual-stage SSHI cases (control block externally powered).

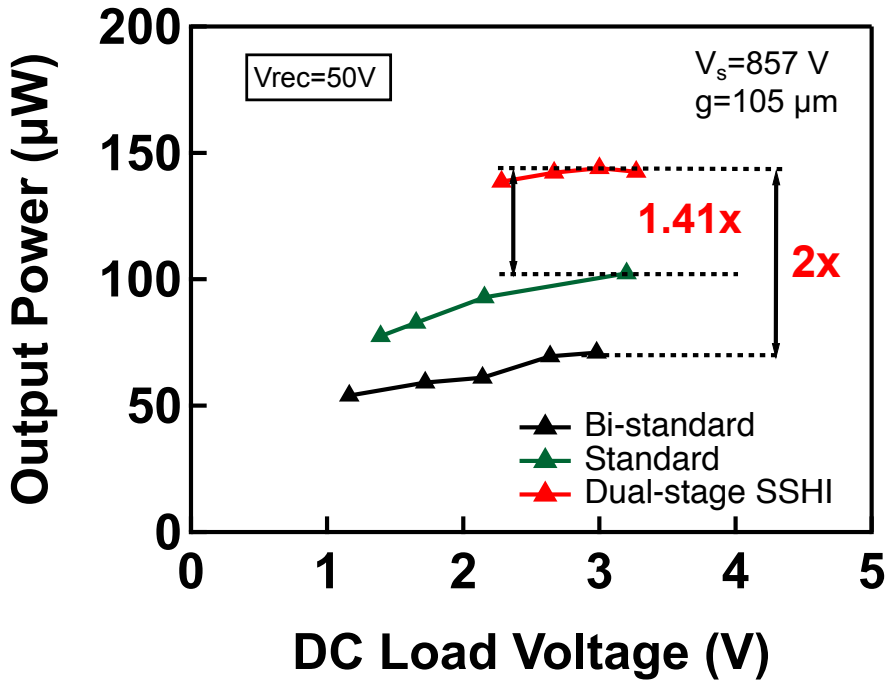


Figure 4-13 Measured output power as a function of DC load voltage in standard, bi-standard and self-powered dual-stage SSHI cases.

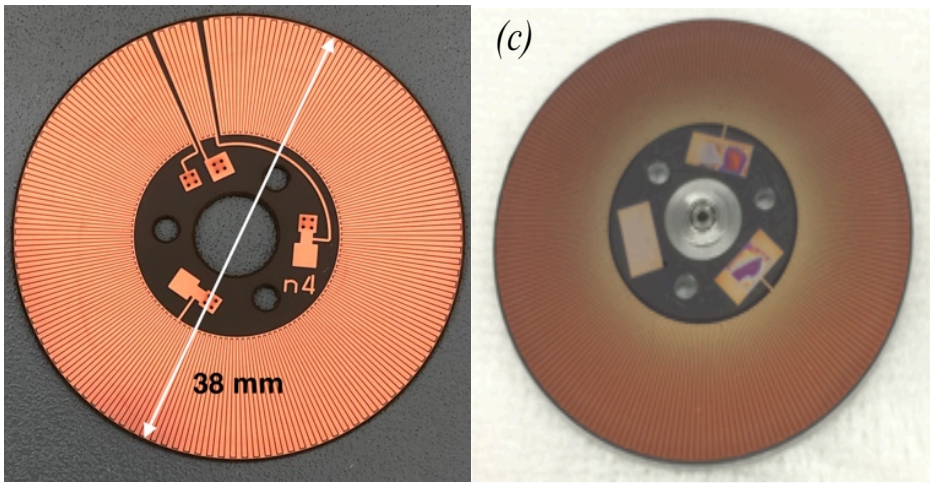


Figure 4-14 Prototype of (a) pole-number-based dual-stage stator and (b) rotor based on PCB technology.

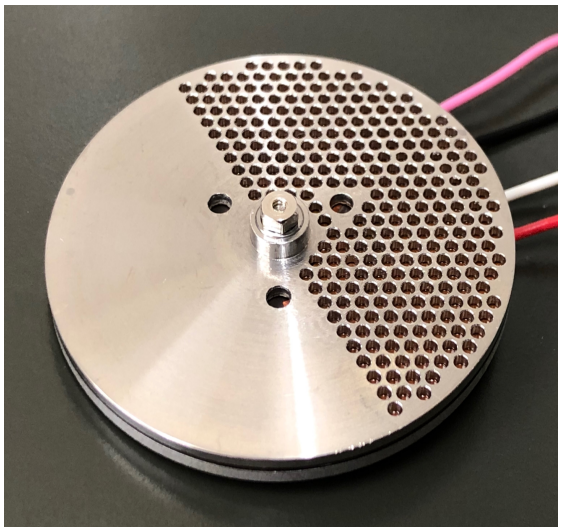


Figure 4-15 Assembled fully-integrated rotational electret EH with dual-stage stator.

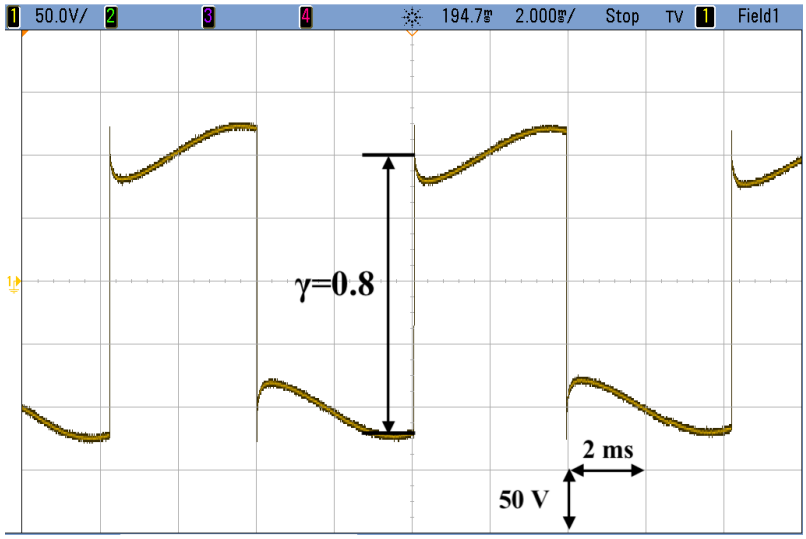


Figure 4-16 Measured output voltage of electret EH with dual-stage SSHI.

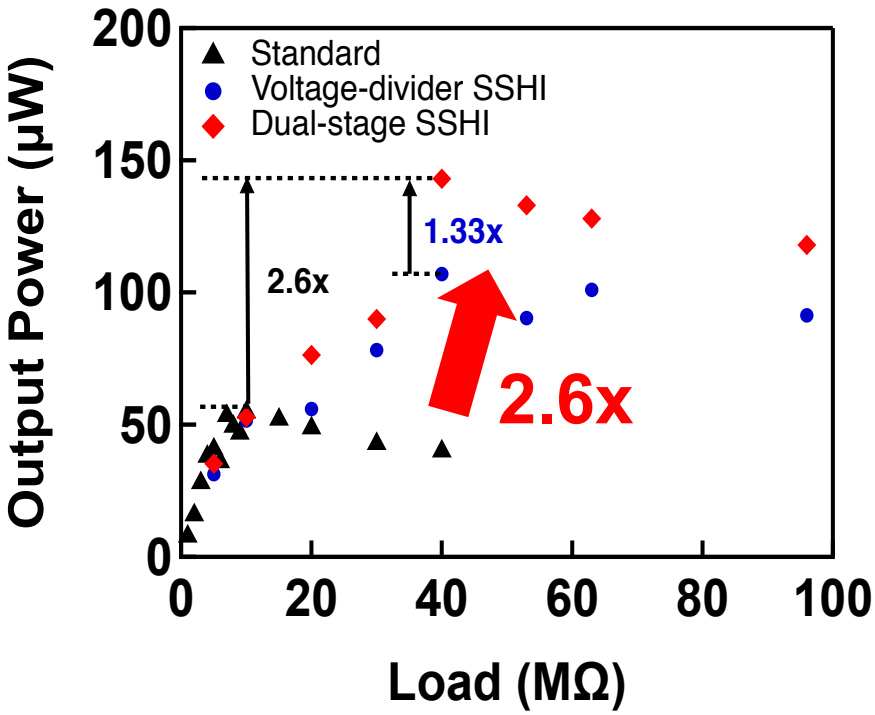


Figure 4-17 Measured output power of electret EH as a function of load resistance in standard AC, voltage-divider SSHI and dual-stage SSHI cases.

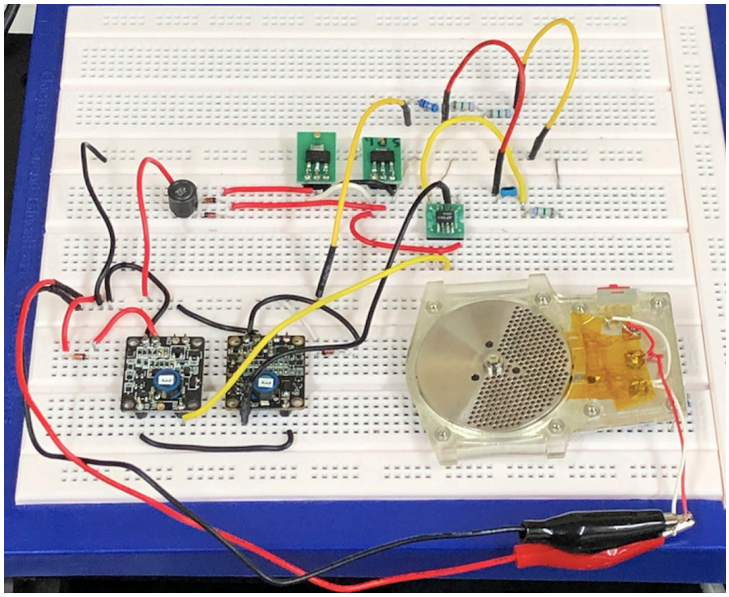


Figure 4-18 Experimental setup for validating cold-start and self-powering ability of voltage-divider SSHI circuit under random excitation.

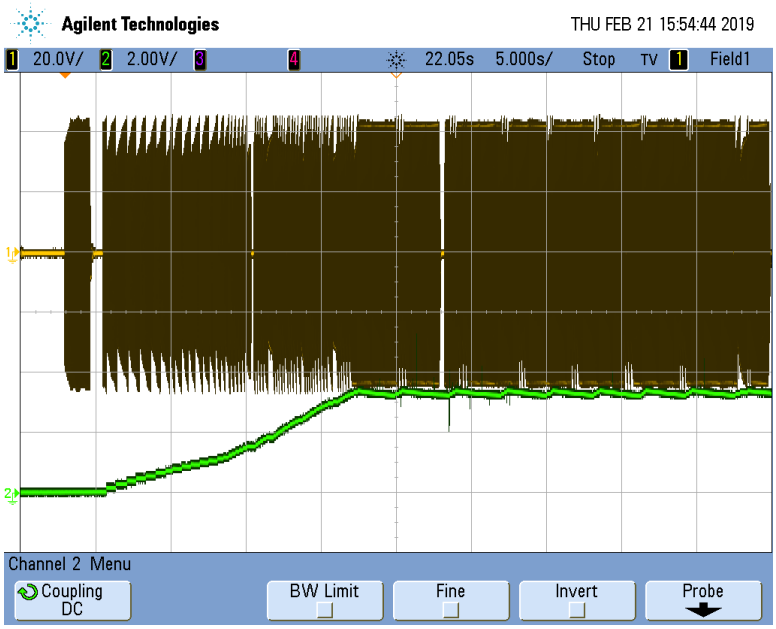


Figure 4-19 Output and load voltage of rotational electret energy harvester during start-up process.

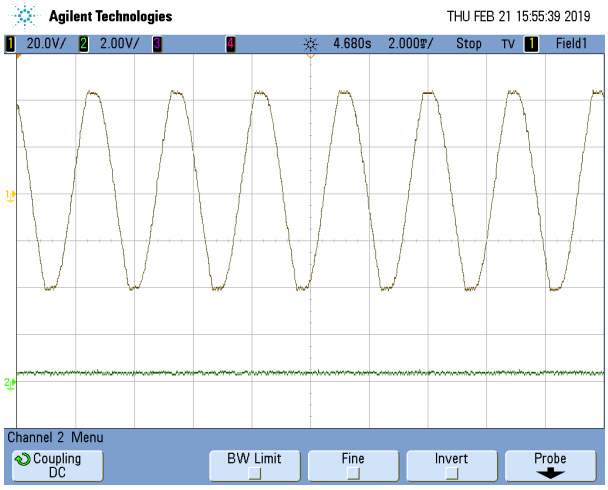


Figure 4-20 Magnified voltage waveforms when SSHI is not activated.

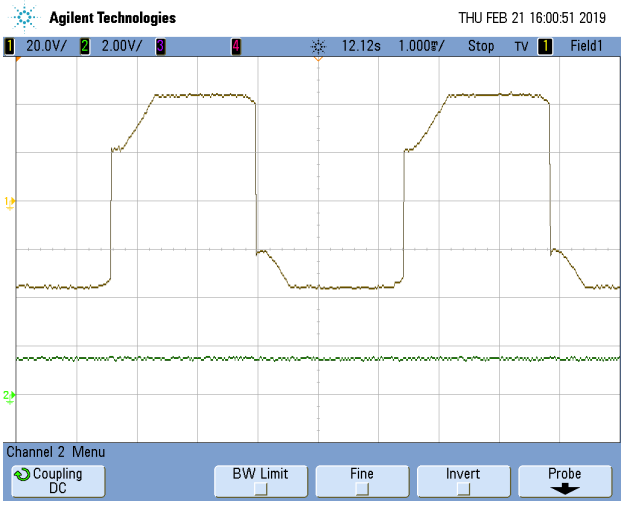


Figure 4-21 Magnified voltage waveforms when SSHI is started.

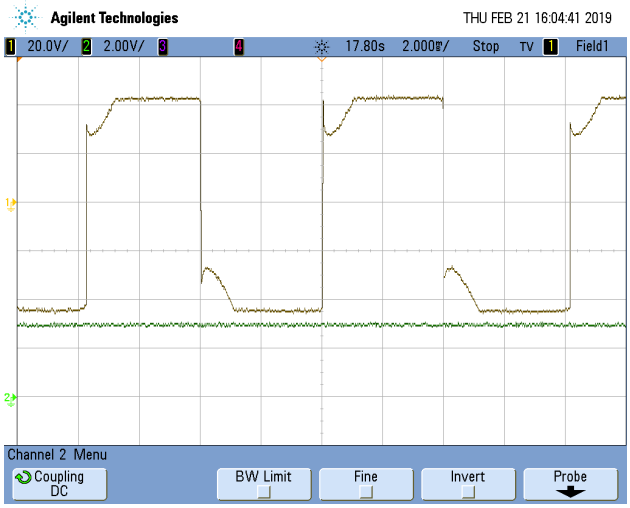


Figure 4-22 Magnified voltage waveforms during stable SSHI operation

Chapter 5 Dual-stage Synchronized Electric Charge Extraction

In parallel SSHI, two major challenges remain: (1) SSHI has better performance at high voltage (>200V) range, which make it difficult to step-down the high voltage to sub-5 V efficiently based on current DC/DC converter technology. (2) Dual-polarity converter, which suffers from lower (<50%) conversion efficiency than classic uni-polarity converter, is required for self-powering. Therefore, a novel circuit, which addresses these challenges, is to be developed. This chapter introduces the development of such a circuit, which is based on the concept of SECE in piezoelectric case, for electret EH.

5. 1. Theoretical analysis of SECE

5. 1. 1. Output power of electret EH with SECE

Figure 5-1 shows a circuit diagram of SECE for electret EH. The topology is similar to SECE [69] or SSDCI [73] for piezoelectric EHs.

The working principle is explained as follows. Assuming V_o=0 at initial state and the switch S is turned off, hence the current source I_s starts to charge its shunt capacitance C_e from null. After half a period, the accumulated electrostatic energy E_c in C_e reaches its maximum, in ahead of I_s alters its direction. The E_c at this instant is given by

$$\boldsymbol{E_c = \frac{1}{2} C_e V_m^2 = \frac{1}{2} C_e \left(\frac{I_s T}{2C_e}\right)^2 = \frac{C_i^2 V_s^2}{2C_e}} \quad (5\text{-}1)$$

At this voltage peak V_m, the switch S is turned on to transfer E_c to the inductor L. Assuming $C_s >> C_e$ and V_L =0, after ¼ of the LC period, when V_o becomes null, E_c is totally converted to magnetic energy in L. At this instant, the switch is turned off again. Afterwards, the current source charges C_e to the opposite polarity; whilst the magnetic energy in L is transferred to load through the freewheel diode D. In this way, E_c is extracted every half a period. The output power in SECE case is then given by

$$\boldsymbol{P_o = \frac{E_c}{0.5T} = \frac{1}{2} C_e \left(\frac{I_s T}{2C_e}\right)^2 * 2f_s = \frac{I_s^2 T}{4C_e} = \frac{C_i^2 V_s^2 f_s}{C_e}} \quad (5\text{-}2)$$

Comparing with the maximal power in standard case in Eq. (3-4), it is found that a power enhancing ratio of 4 is achieved with SECE, regardless of the load impedance.

5. 1. 2. Influence of load voltage on SECE

In fact, Eq. (5-2) maintains its accuracy in case that $V_L << V_o$. In SECE implementation, an impedance converter, in this case a fly-back transformer, is inserted between load and the output of rectifier to scale down V_{out} viewed by the transducer (Figure 5-2), which functions like maintaining $V_L << V_o$ in Figure 5-1. Therefore, it is claimed that the harvested power in SECE is load independent [69], as shown in Figure 5-3.

In the case that the transformer is not employed, Eq.(5-2) loses its accuracy as the storage capacitor charges. Since the difference between V_L and V_m decreases as C_s charges, the discharging of C_e becomes insufficient, reducing the energy extracted from transducer, as well as the effectiveness of weakening the shunting effect. Simulation is carried out to illustrate this case.

Figure 5-4 shows the simulation setup for ideal SECE in electret EH. The switch S is perfectly triggered with Is and keeps an on-state duration of ¼ LC period. The inductor L has no series resistance. The diodes have infinite reverse resistance and zero forward voltage drop. A DC voltage source is employed to emulate the load in the steady state. The output power in this case is measured by power consumption of the DC voltage source. The parameters are listed in **Table 5-1**. To keep consistency, generator parameters (I_s, C_e) and the inductance of the inductor L are identical to those in ideal SSHI simulation.

Figure 5-5 shows the simulated transducer voltage V_o waveforms for V_L=1V and V_L=50V, respectively. First, V_o ramps to V_L instead of 0 in ¼ LC period, therefore, with V_L increasing, the discharge of C_e becomes less sufficient, indicating less power

Table 5-1 Parameters in ideal SECE simulation.

Parameters	Definition	Value
I_s	Generator source current	7.9 μA
C_e	Generator shunt capacitance	169 pF
L	Inductance	5.6 mH
C_s	Storage capacitance	0.1 μF

extracted from C_e to load. On the other hand, as the residual voltage across C_e after discharging is V_L instead of 0, the transducer needs to discharge it first. In this regard, the shunt effect of Ce is less effectively weakened with V_L increasing. Therefore, the Vo peak in V_L=50V case is much lower than that in V_L=1V case, indicating less power extracted from mechanical structure. Therefore, if the on-state duration of S is fixed at ¼ LC period, both generator output power and power on load decrease with VL increasing. Actually, if the on-state duration of S is tuned to make V_o ramps to 0 during discharge, instead of fixing at ¼ LC period, the output power can be less dependent on load voltage (Figure 5-6), which is discussed in detail in [73].

In the fixed on-state duration case, for a given load voltage V_L, the charge conservation law gives

$$\boldsymbol{C_e(V_L + V_m) = \frac{I_s T}{2}} \tag{5-3}$$

where V_m is the amplitude of V_o. The extracted power from transducer as a function of V_L is then given by

$$P_o = \frac{\frac{1}{2}C_e(V_m^2 - V_L^2)}{\frac{T}{2}} = -I_s V_L + \frac{I_s^2 T}{4C_e} \tag{5-4}$$

Note that Eq.(5-4) reduces Eq. (5-2) if V_L=0. Figure 5-10 shows the simulated and calculated generator output power as a function of load voltage V_L. In standard case, V_L refers to the rectified voltage V_{rec}. Figure 5-7a shows that a power enhancing ratio of 4 with SECE is obtained at very low load voltages V_L<10V (Figure 5-7b). Note that high voltage still exists at generator output of which the peak is $2V_{oc}$. V_{oc} is the open-circuit voltage in standard case.

To summarize, the major merit of SECE is that it has superior performance at low V_L range. It is also found that if switch S is fixed to close for ¼ LC period, SECE exhibits load dependency. In this regard, it is better to optimize the on-state duration of switch S in circuit implementation to ensure Vo discharge to 0.

5. 1. 3. Theoretical comparison with SSHI

Table 5-2 shows a comparison of SECE (**Figure 5-8**b) and SSHI (**Figure 5-8**a) for a rotational electret EH (I_s=7.9 μA, C_e=169 pF). $V_{oc} = \frac{I_s}{4C_e f_s}$ denotes the open-circuit voltage in standard case.

Theoretically, SSHI is able to present higher power enhancing performance at generator output than SECE, at cost of several times higher generator output voltage than that in SECE for optimal operation. However, a DC/DC converter is necessary to convert this high voltage to sub-3V for electronic devices in a sensor node. Currently, the efficiency of unipolarity DC/DC converter has an efficiency of 80% at input voltages of 40~60V. To achieve self-powering of SSHI, a dual-polarity converter is required. Unfortunately, the efficiency of the dual-polarity converter efficiency drops to 50% at 50V. Since the power enhancing ratio of dual-stage SSHI at V_{rec}=50 is around 2.2, the overall power enhancing ratio at load end V_L becomes merely 1.4.

On the other hand, SECE performs a power enhancing of 4 at generator output with much lower voltage, which is twice of the open-circuit voltage in standard case, than that is SSHI. Since SECE circuit itself serves as a DC/DC converter, no additional DC/DC converter like that in SSHI case is needed. In piezoelectric case, the efficiency of power transfer is around 60% in [77]. In electret case, it is still unknown. Assuming an efficiency of 60% in electret case, the overall power enhancing performance is 2.4 at DC low-voltage end. Moreover, the switch in SECE doesn't require dual-polarity supply, so dual-polarity rectifier is not required in this case. In this regard, the power enhancing ratio may keep in self-powered case. Therefore, an overall power enhancing ratio of 2.4 can be expected with SECE, which is higher than that in SECE.

In addition, due to the absence of additional (dual-polarity) DC/DC converter, SECE should have fewer components count than SSHI. Therefore, it is interesting to develop SECE circuit for electret EH for a better overall performance than SSHI.

5. 2. Circuit design

Figure 5-9 shows a block diagram of self-powered SECE system design. The generator is divided into power stage and control stage. Similar to dual-stage SSHI, the power stage, which occupies majority of poles on the stator, outputs high voltage V_o to the SECE main circuit for transferring power. On the other hand, the control stage, which occupies minority of poles, outputs low voltage V_{ct} to the control block which generates V_g to drive the switch action in SECE main circuit. As SECE functions DC/DC conversion itself, the output voltage of SECE circuit V_L is DC low voltage V_L readily for the load. Note that the control block in this case is expected to be powered by the control stage itself, as will be explained later, for self-powering.

Table 5-2 Theoretical comparison between SECE and parallel SSHI on rotational electret EH.

	Parallel SSHI	**SECE**
Generator power (compared with standard)	4~10x ($\frac{2}{1-\gamma}$, γ=0.5~0.8)	4x
Generator output voltage V_o	432~1080V(optimal) ($\frac{2}{1-\gamma}V_{oc}$, γ=0.5~0.8)	216V ($2V_{oc}$)
Additional DC/DC converter?	Yes	No
Requirements for converter	Dual-polarity High input voltage	--
DC/DC converter efficiency	50% (dual-polarity converter)	60% (SECE itself, Piezo)
Load power	1.4x (γ=0.7, V_o=60V)	2.4x (Expected)

Figure 5-10 shows a detailed circuit design of dual-stage SECE. The working principle is explained as follows.

5. 2. 1. Dual-stage electrode design

Figure 5-11 shows the pole-number-based dual-stage electrode design for SECE. the number of poles n_{ct} for control stage and control stage is 9 and 100, respectively. As shown in Figure 5-10, the power stage outputs V_p and V_n; whilst the control stage outputs V_{pc} and V_{nc}. Note that the ground in SECE is on DC side, therefore V_n and V_{nc} are not connected as that in SSHI case. The currents generated by the power stage and the control stage are I_{po} and I_{ct}, respectively. The shunt capacitances of the power stage and the control stage are C_{po} and C_{ct}, respectively. Note that the source current and shunt capacitance of each stage is proportional to its poles. The inter-terminal parasitic capacitance is useful for discharging, as will be explained in later section.

5. 2. 2. SECE main circuit

Figure 5-12 shows 3 possible topologies of SECE main circuit. In **Figure 5-12**a, the inductor L and storage capacitance are connected in parallel [72], which allows V_{rec} ramps to 0 during discharging phase, regardless of the load voltage V_L. This is a favorable feature for SECE operation. However, if the on-state duration of the switch is not precisely tuned to the ¼ period of L-Ce period, which often happens in view of the extradentary short L-Ce period [72], there will be voltage residual (On-duration too short) after the discharging phase. In this case, both the effectiveness of weakening the shunt effect and the stored energy in coil will be reduced. Therefore, the requirement of high precision on switch on-duration limits a robust operation of SECE. In addition, the ground of V_L is not the ground of the switch S. Therefore, a fly-back transformer [69][90] or a pair of exclusive switches [75] is usually employed to convert the ground of V_L for self-powering. However, a fly-back transformer could be bulky and the exclusive switches include a high-side switch which is difficult to realize in electret EH case because V_{rec} is high.

In **Figure 5-12**b, a high-side switch is employed to release the constraint of ground conversion. However, the high-side switch itself becomes quite lossy under high voltage. A photocoupler was employed to drive the high-side switch in [73], but it consumes mW-level power, which is unfavorable for small scale energy harvesting.

In the present study, the topology in **Figure 5-12**c is employed. It features a low-side switch and a series connection of L and C_s. Due to the series connection, the current flowing in L is bound to charge C_s. Even if the on-duration of the switch is much longer than ¼ of L-C_e period, C_s will be charged continuously during the overlong L-C_e oscillation, because C_s, which locates in DC side, is in series with L. In a parallel L-Cs configuration as in **Figure 5-12**a, if the on-duration of the switch is overlong, the energy stored in L will be lost in L-Ce oscillation, instead of charging Cs, because Cs is bypassed by L. Therefore, the on-duration of the switch in this case can be longer than ideal, as long as it is still much smaller than the period of the source, thus achieving a more robust operation of SECE, comparing with parallel L-Cs configuration. Note that the load voltage V_L in this case is also floating, but it does not matter if an alternative way to achieve self-powering, instead of using V_L, is achievable, which will be illustrated later.

5. 2. 3. Control block

The control block consists of a full-bridge rectifier, a storage capacitor C_r, two comparators and an AND gate. The input signals to the control block are the AC output voltages of the control stage (V_{pc} and V_{nc}). The output signal of the control block V_g drives the NMOS switch. The control block detects the peak and zero-crossing of V_{po} to turn on and turn off the switch, respectively.

Figure 5-13 illustrates the waveforms during SECE operation. Assuming I_s>0, V_s>0 since $t=0^+$, hence $V_{pc}=V_s+V_D$, $V_{nc}=-V_D$. V_D is the forward voltage drop of the diode in the rectifier. As shown in Figure 5-10, the condition for V_g outputting high is V_{pc}>0 and V_{nc}>0. Therefore, V_g=0 since $t=0+$.

At $t=t_1$, I_{po} alters its direction to $-I_s$ and so does I_{ct}. Therefore, V_{nc} starts increasing from $-V_D$ toward 0; whilst V_{pc} is still positive but starts decreasing from V_s+V_D towards 0. At $t=t_2$, V_{nc} exceeds 0, which satisfies the condition for Vg outputting high, thereby activating the discharging phase. Note that $\Delta t=t_2-t_1$ is the switch delay in this case. From $t=t_2$ and $t=t_3$, V_{po} quickly ramps to 0 and so does V_{pc}, owing to the parasitic capacitance between them. At $t=t_3$, V_{nc} drops below 0 making Vg output low, thereby terminating the discharging phase. After $t=t_3$, another charging cycle initiates and the stored energy in the inductor will freewheel to the load. In this way, the control block governs the switch action, adapting to arbitrary internal capacitance and external inductor. Actually, the on-duration of the switch is extradentary short (sub-3 μs) comparing with the source period (~10 ms), hence the discharge phase happens instantly.

Table 5-3 shows a comparison of several control schemes in SECE implementation. It is clear that the proposed diode-based switch control method is simple, adaptive and IC-compatible.

Table 5-3 Comparison of switch control schemes in SECE

	Fixed time [77]	Dual-mode comparator[112]	Sensor-based [69][73]	Diode-based [This work]
Merits	-Reliable -Easy to realize	-Adaptive	-Adaptive -Easy to realize	-Adaptive -Easy to achieve
Drawbacks	Not adaptive	Complex	Bulky	--

5. 2. 4. Self-powering

Most SECE implementations utilize the power harvested on load to power the control block of SECE in a feedback manner. It usually requires a fly-back transformer or a high-side switch, both of which are unfavorable in electret EH case. In dual-stage SECE, the energy accumulated in the storage capacitor of the control stage C_r can be used to power the control block, because it shares the same ground with the control circuitry. The critical challenge here is whether the control stage is able to generate enough power for the control stage, which will be discussed in next chapter.

5. 3. Simulation results

Figure 5-14 shows the simulation setup of dual-stage SECE. The parameters are listed in

Table 5-4. The generator parameters are calculated based on the circuit model, using the output power of an electret EH in standard case. The components, which are also used in experimental validation, are characterized in detail for a more realistic simulation. The inductor is characterized using an impedance analyzer, with its inductance L, series resistance r_{series} and parallel resistance $r_{parallel}$ specified. The MOSFET series is intended for high-voltage small-signal application. Here the MOSFET of the highest voltage-rating (M_n: BSP89, 240V) is selected, where the parameters from their datasheets are applied into simulation. Note that the upper limit of generator output voltage is then constrained at 240V considering the withstand voltage of the n-channel MOSFET. 250V-tolerable diodes BAV21 are characterized using a multimeter (U1282A, Keysight), with forward voltage drop V_F=0.6 V and reverse resistance $r_{reverse}$ measured. A 0.1 μF electrolytic capacitor is chosen for the storage capacitor C_s of the resistance is out of the range of the multimeter. C_1 is the

Table 5-4 Parameters in dual-stage SECE simulation and experiment

Definition	Value	Definition	Value
I_{po}	5.78 μA@109 Hz	M_n	BSP89 [110]
C_{po}	145 pF	C_s	0.1 μF
I_{ct}	0.52 μA@109 Hz	Comparator	LTC1540
C_{ct}	13 pF	Diodes	BAV21
L	5.6 mH	C_1	8 pF
r_{series} of L	10.22 Ω	C_2	8 pF
$r_{parallel}$ of L	130 kΩ	AND gate	SN74HC11N
C_{par} of L	5 pF	DC supply	3 V

measured parasitic capacitance between V_p and V_{pc}; whilst C_2 is the measured parasitic capacitance between V_n and V_{nc}. The control block is powered by a DC supply externally. The DC side of the control stage V_s is also connected to the DC supply.

Figure 5-17 shows the simulated rectified voltage in SECE case. It is clear the switch is turned on at voltage peak and then turned off at the zero-crossing point of the voltage. Afterwards, the energy in the coil is transferred to the load via the freewheel diode D_2. The current in L is null, D2 recovers to reversed state with high-frequency oscillation. The plateau indicates that the generator needs some time to charge the internal capacitor to V_L after the switch S is turned off. The simulated on-duration is actually around 50 μs, much longer than ¼ of L-C_e period. This will cause some charge loss but not much, because 50 μs is much shorter than 5 ms, which is ½ of the source period. Figure 5-19 shows the simulated load power as a function of load voltage. A power enhancing ratio of 2.77 is obtained at a load voltage of 60V. Note that a remarkable power enhancing ratio of 2 is obtained at load voltage of 5V, which is an end-to-end power enhancing performance.

5. 4. Experimental results

5. 4. 1. Experimental setup

Figure 5-15 shows a photo of fabricated dual-stage electrode. It has four lead-outs, namely V_p, V_n, V_{pc} and V_{nc}. The number of poles for control stage and power stage is 9 and 100, respectively. Figure 5-16 shows the SECE circuit using discreet components. The control block and the DC side of control stage are connected to a 3V DC supply. The detailed information of the generator and the components are listed in

Table **5-4**.

The AC-side voltage is measured by an oscilloscope (DSO6014A, Agilent) via a 100:1 (100 MΩ, 5pF) voltage probe. The power harvested on load at DC side is calculated by $P_o = I^2 R_L$. The load current I is derived by measuring the DC voltage across a sampling resistor R_s using a digital multimeter (U1282A, Keysight). The voltage probe is detached during load power measurement.

5. 4. 2. External-powered SECE

Figure 5-17 shows the measured rectified voltage of generator output in external-powered SECE case, with R_L=2 MΩ. It shares the same shape with the simulated result.

But the voltage amplitude of experimental result is lower than that of simulated one. One possible reason for this is that the impedance of the probe (100 MΩ) is not high enough, it shunts a portion of charges during the open-circuit charging phase, which results in lower amplitude of experimental results. This reason might be true because the power generation results with R_L=2 MΩ (Figure 5-19), where the probe is detached, do not show much difference between simulation and experiment. A second reason is that the on-duration of the switch in experiment is longer than that in simulation, because unexpected switching on is observed in experiment (Figure 5-18). This undesired jitter might be caused by the environmental noise to the discrete components.

Figure 5-19 shows the power generation results in standard, voltage-divider SSHI and SECE cases. The control block in SSHI and SECE are externally powered. The load voltage in standard and SSHI cases refers to the input voltage to the DC/DC converter or primary storage capacitor; whilst the load voltage in SECE case refers to the load voltage across the storage capacitor, which could be DC low voltage without using DC/DC converter. Consequently, a power enhancing ratio of 2.77 is obtained with SECE. More importantly, a power enhancing ratio of 2 is achieved at a load voltage as low as 5V. In addition, experimental and simulated results show good consistency until V_L=70V, which enables an analysis of SECE circuit based on simulation. The reason for the difference between experiment and simulation in over-70V range remains to be disclosed.

5. 5. Discussion

5. 5. 1. On-state duration of the switch

It is observed that both in simulation and experiment, the on-duration of the switch is much longer than ¼ of L-C_e period, but the power enhancing performance is still remarkable. Specifically, the calculated ¼ of L-C_e period is around 1.5 μs, but the on-duration in simulation is 50 μs (Figure 5-20) and that in experiment is 40 μs (without jitter) and 190 μs (with jitter). Therefore, it is interesting to look into the power transfer process.

Figure 5-20 shows the power transfer process in SECE. It can be divided into three phases: discharge, free wheel and neutralization. In the discharge phase, V_g goes high at the peak of V_{po} to turn on the switch, thereby activating discharging C_e to the inductor L. This phase stops when V_{po} ramps to 0, because the LC oscillation is blocked by the

rectifier. Note that the discharging phase stops even if V_g does not go low to turn off the switch. In the next freewheel phase, the inductor current freewheels to load through D_F (see I_{DF}), thereby converting magnetic energy stored in L to the storage capacitor C_s. This phase stops when I_L ramps to 0. In the next neutralization phase, the diode DF oscillates to reversed state, so that the voltage across the inductor oscillates to 0 and V_{rec} oscillates to V_L.

By analyzing the power transfer process, the followings are found. First, the on-duration is bound to be larger than ¼ of LC period to ensure that V_{po} ramps to 0. As shown in Figure 5-20, it takes 5 μs for V_{po} to ramp to 0. Second, the overlong on-duration does not jeopardize transferring energy from C_{po} to C_s, because the LC oscillation is naturally blocked by the rectifier at V_{po}=0. Third, the overlong on-duration does not hinder the re-charge of C_e by I_s reversely, as long as the amplitude of V_{po} is no larger than V_L. The extreme of V_{po}, which is less than $2V_{oc}$, might be caused by the introduced impedance of the SECE circuit, instead of overlong on-duration time.

Therefore, even though the on-duration of the switch is longer than expected, it does not hinder harvesting and transferring power in a typical SECE manner, as long as the on-duration is not long enough to make $|V_{po}|$ exceed V_L.

5. 5. 2. Inductor selection

The inductor size is another concern because it dominates the volume of the circuit. Since the inductor also acts as an energy intermediate in SECE, the quality factor $Q_I = \frac{1}{R_{ser}}\sqrt{\frac{L}{C_e}}$ may also influence the performance, especially in low load voltage cases where the voltage difference between generator and load is high. Therefore, the influence of inductance L, series resistance R_{ser} and parallel resistance R_{par} is investigated base on simulation, with load voltage V_L=5V.

Figure 5-21 shows the power harvested on load as a function of the inductance. It clearly reveals that the inductance has a significant influence on load power, if the inductance is lower than 100 μH. However, the improvement led by increased inductance saturates when the inductance exceeds around 100 μH. Therefore, replacing the 5.6 mH inductor employed in current SECE by a 100 μH one will not severely damage the power enhancing performance. But it can effectively reduce the height of the inductor because the turns of the coil are reduced to a large degree.

Figure 5-22 shows the power harvested on load as a function of the parallel resistance of the inductor. If the parallel resistance is over 100 kΩ, which is usually satisfied for practical components, it will not influence the load power significantly.

Figure 5-23 shows the power harvested on load as a function of the parallel resistance of the inductor. It reveals that the load power is dependent on the series resistance in a quasi-linear manner, but the ramp is not high. If the series resistance increases from 1 Ω to 50 Ω, the load power just decreases by 10%. Therefore, there is a trade-off between power performance and coil diameter in choosing the series resistance.

5. 5. 3. Efficiency analysis

Figure 5-24 shows the power consumption of each component in SECE as a function of load voltage. It reveals that the freewheel diode consumes substantial power at low load voltage. This is because the current amplitude of the inductor is high when the voltage difference between generator and load is large. Therefore, the power consumption of the freewheel diode, which is the product of inductor current and forward voltage drop, is significant at low load voltage. Since a larger inductance is not preferred in our case, an effective method to address this issue is to choose a freewheel diode with lower forward voltage drop (currently 0.5V).

The efficiency of SECE circuit exceeds 80% even at sub-10V load voltage range, which is remarkable compared with that of SSHI for electret EH. This is because the quality factor is high, thanks to the ultralow shunt capacitance C_e.

A comparison between dual-stage SSHI and dual-stage SECE with experimental results is given in Table 5-5.

5. 6. Summary

In this chapter, a dual-stage SECE circuit is proposed to achieve a higher overall power enhancing performance over SSHI. As a result, the followings are obtained:

(1) A novel SECE circuit design for electret energy harvester is proposed for the first time. Thanks to its buck converter topology, the proposed dual-stage SECE also achieves voltage-stepping-down function. Moreover, thanks to the DC side switch, dual-stage SECE is free of the dual-polarity converter needed in SSHI. In addition, The

Table 5-5 Comparison between dual-stage SSHI and dual-stage SECE with experimental results.

	Parallel SSHI	**SECE**
Generator power (Theoretical) (compared with standard)	4~10x ($\frac{2}{1-\gamma}$, γ=0.5~0.8)	4x
Generator power (Experimental) (externally powered)	4x @ V_{rec}=180V	2.85x (V_{rec}=160V)
Additional DC/DC converter?	Yes	No
DC/DC conversion efficiency (Experimental)	50% (Dual-polarity)	80%
Load power (Experimental)	1.4x @ 5V (γ=0.7, V_o=60V)	2.3x @5V
Self-powering	Experimentally confirmed	Proposed
Random Excitation Applicable?	Experimentally confirmed	To be confirmed
Circuit Volume	Large (3 coils)	Small (1 coil)

proposed control block is adaptive to arbitrary internal capacitor and external inductor, thus enabling a robust operation against generator/components aging.

(2) Experimentally, a power enhancing ratio of 2.77 is obtained in SECE, with control block externally powered. More importantly, a power enhancing ratio of 2 is achieved at a load voltage as low as 5V, which means no additional DC/DC converter is needed. The voltage stress at generator output is twice of the open circuit voltage in standard case, which is much lower than that in SSHI case. Self-powering schemes is also proposed by using the charges accumulated in the storage capacitor of the control stage.

(3) Based on the simulation, the efficiency of proposed SECE circuit is above 80%, thanks to the high LC quality factor led by the ultralow internal capacitance of the generator.

(4) The inductor in SECE could be lower than 100 μH without severely reducing the power enhancing performance, which is in favor of the circuit miniaturization. Reducing the forward voltage drop of the freewheel diode is crucial to improve the SECE performance in low load voltage range.

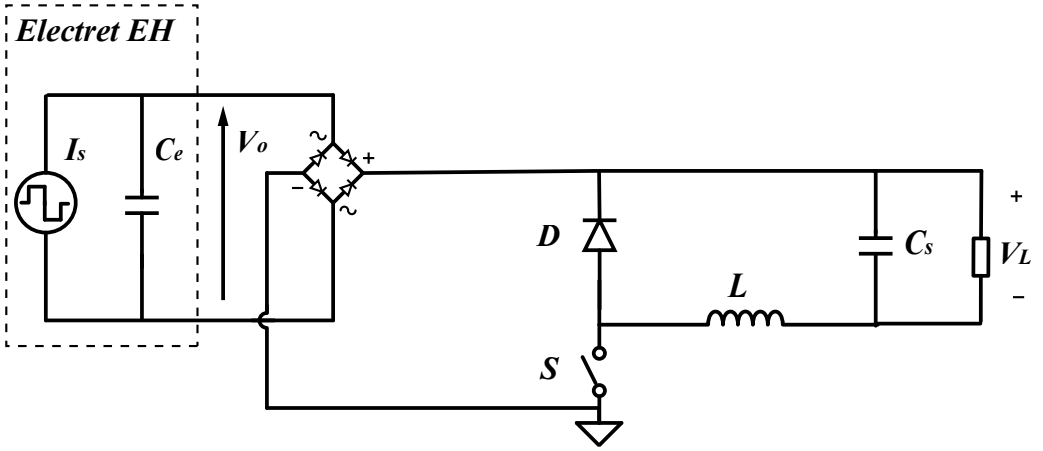


Figure 5-1 Schematic of SECE for electret energy harvester.

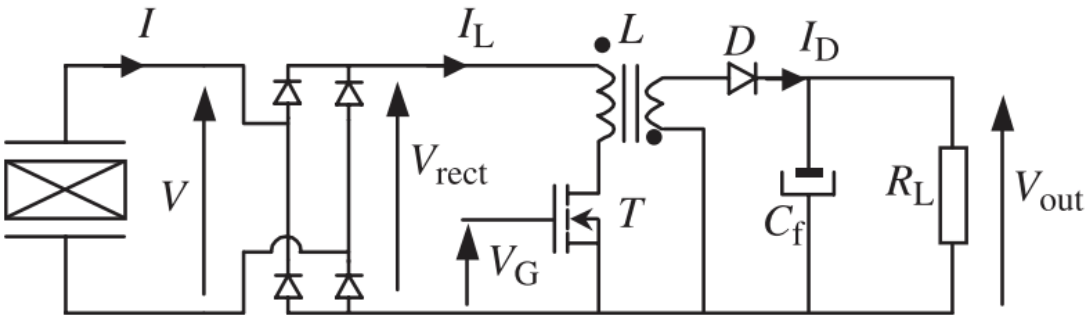


Figure 5-2 Experimental circuit with flyback transformer to perform SECE in piezoelectric case [69].

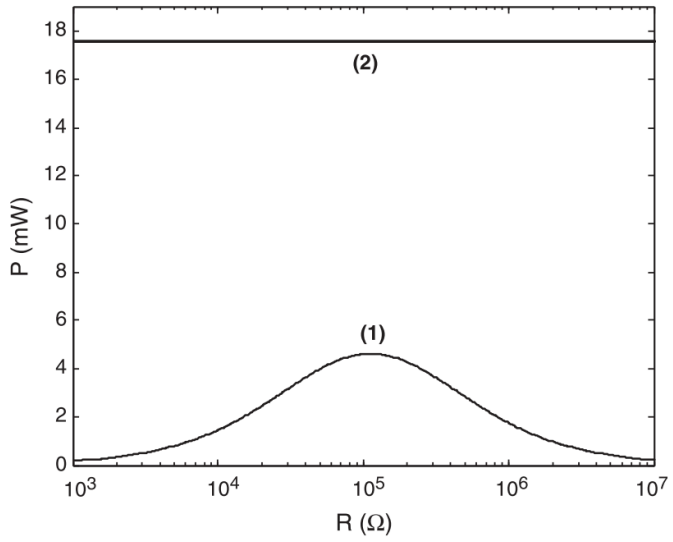


Figure 5-3 Theoretical output power of piezoelectric EH in (1) standard DC and (2) SECE cases [69].

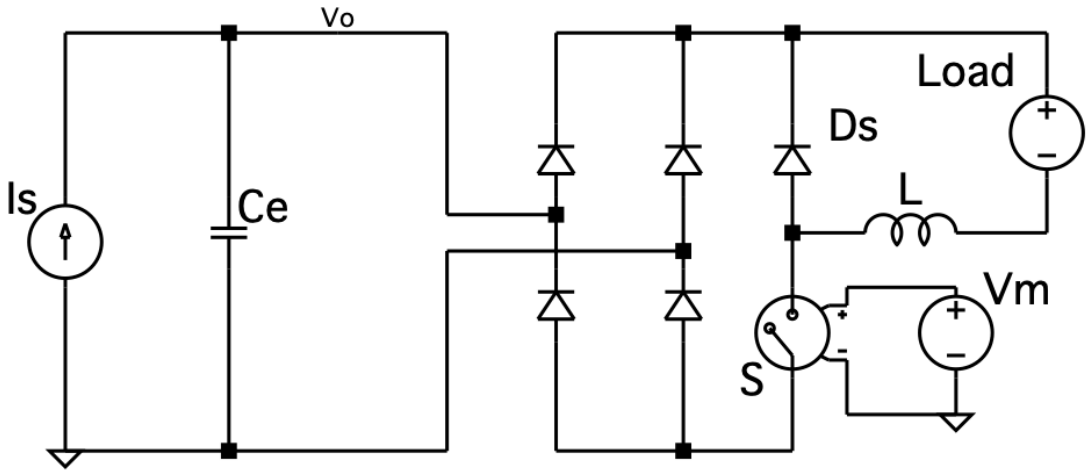


Figure 5-4 Simulation setup for ideal SECE in electret EH case.

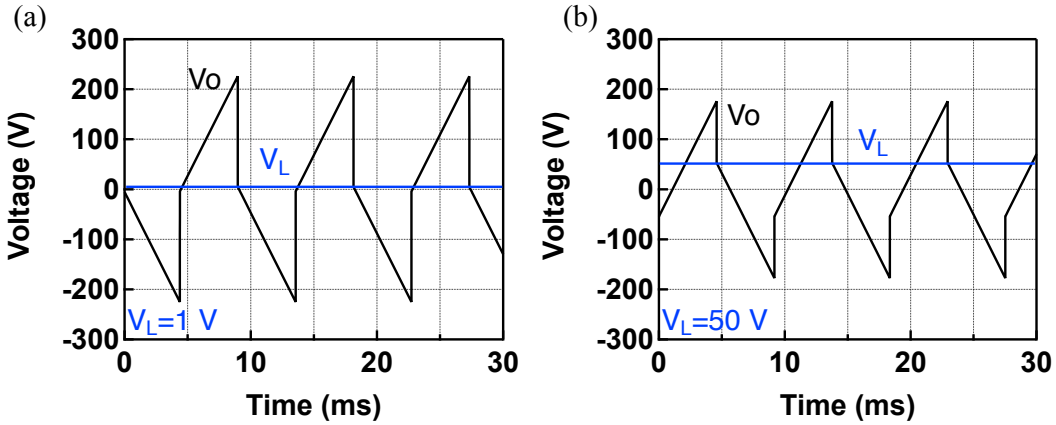


Figure 5-5 Simulated voltage waveforms of generator output in SECE case with (a) V_L=1 V and (b) V_L=50 V.

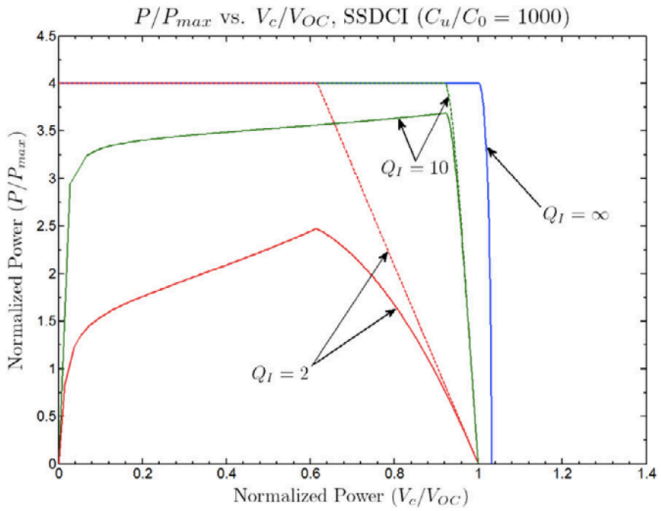


Figure 5-6 Output power as a function of load voltage in SSDCI case where switch is tuned to make V_o ramp to almost 0 [73].

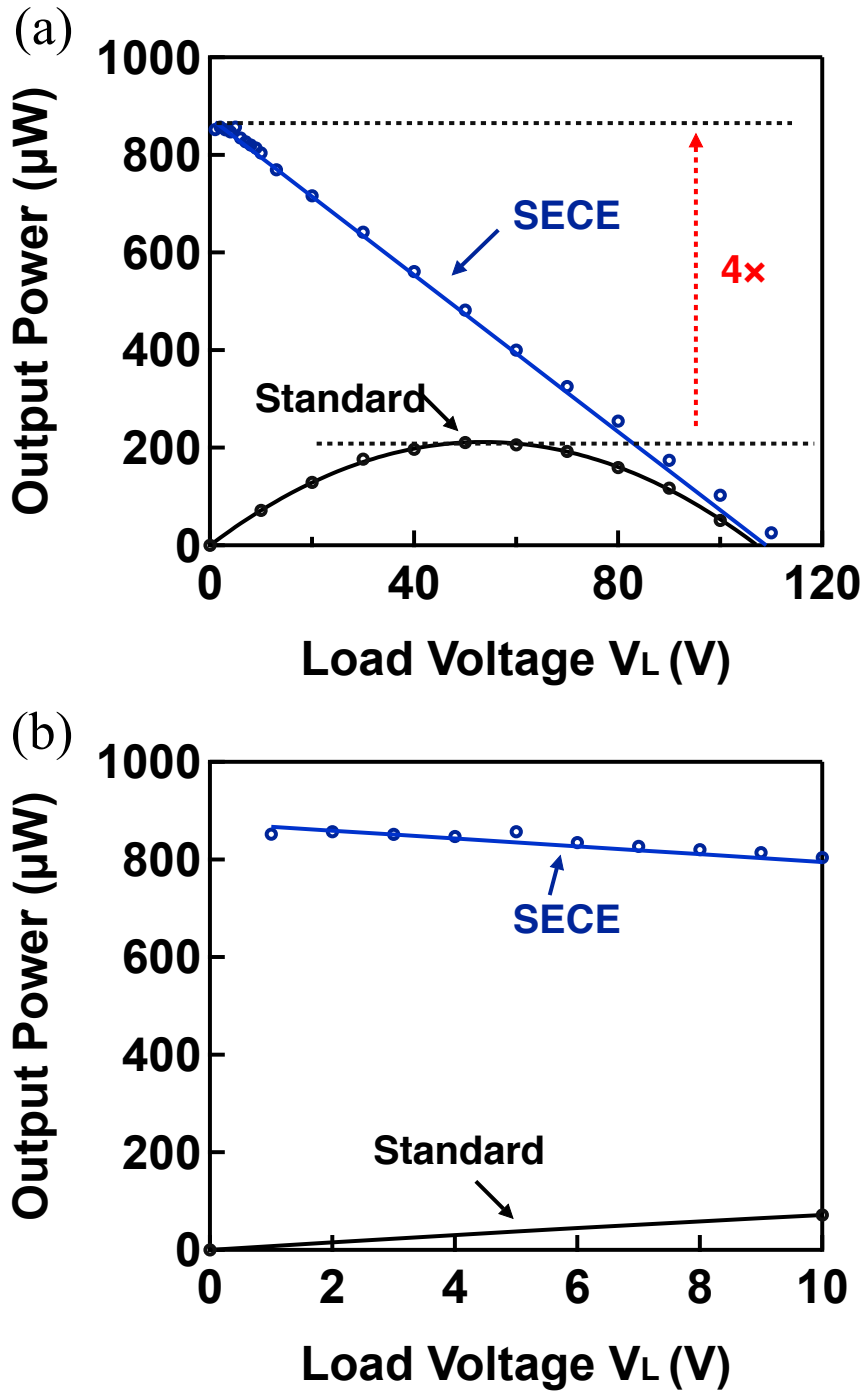


Figure 5-7 Output power of rotational electret EH as a function of load voltage V_L: (a) Full spectrum and (b) magnified view of low V_L range.

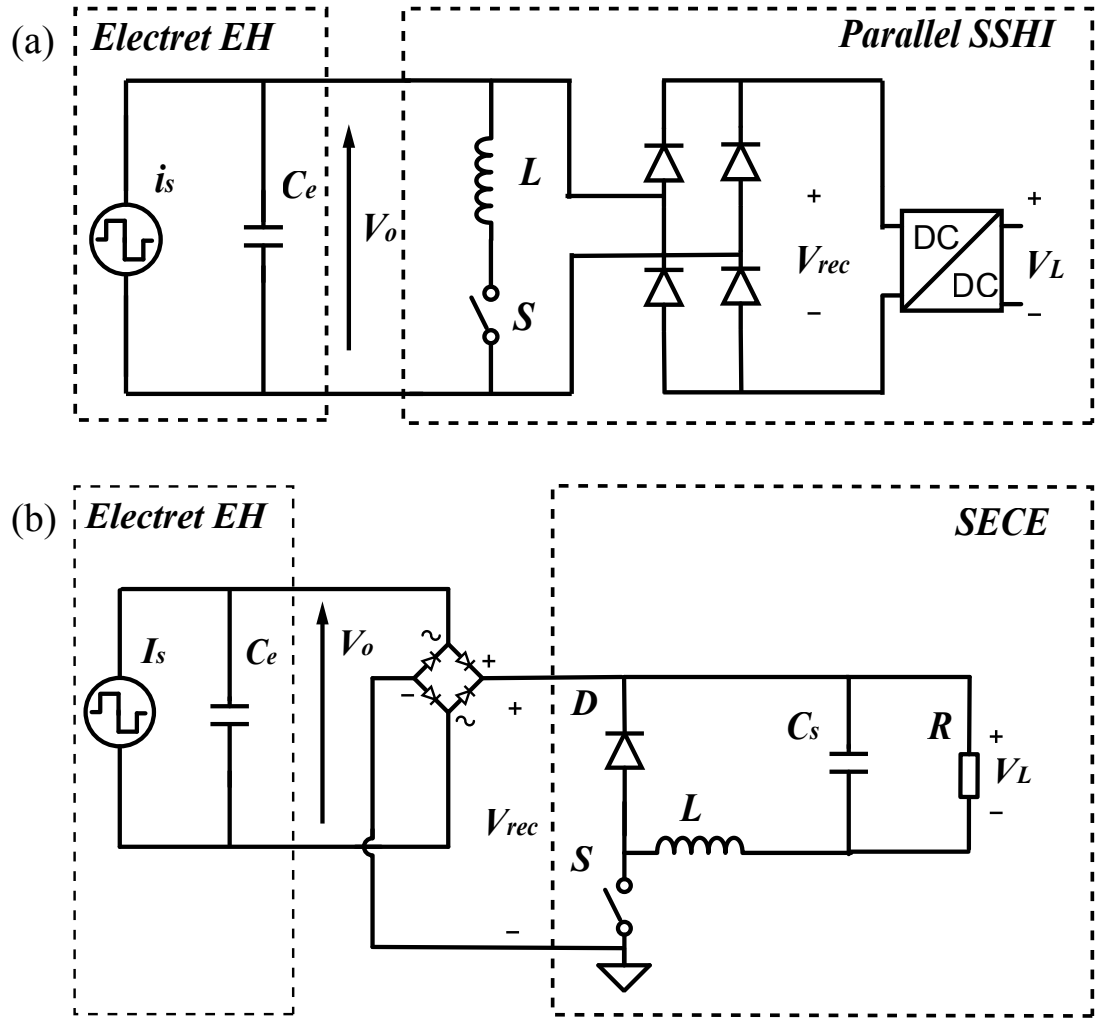


Figure 5-8 Schematics of (a) parallel SSHI and (b) SECE for comparison.

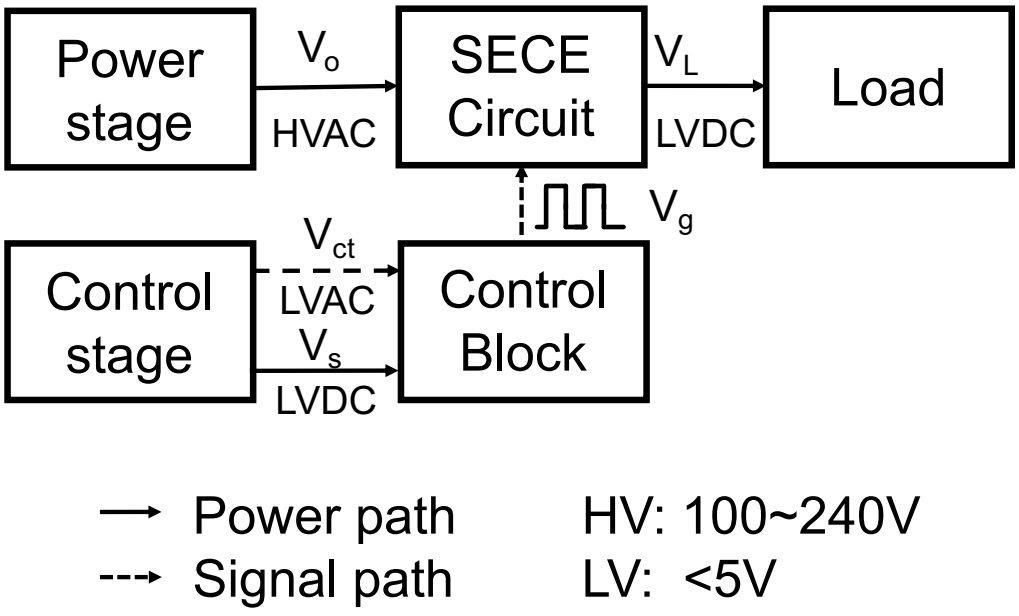


Figure 5-9 Block diagram of SECE design.

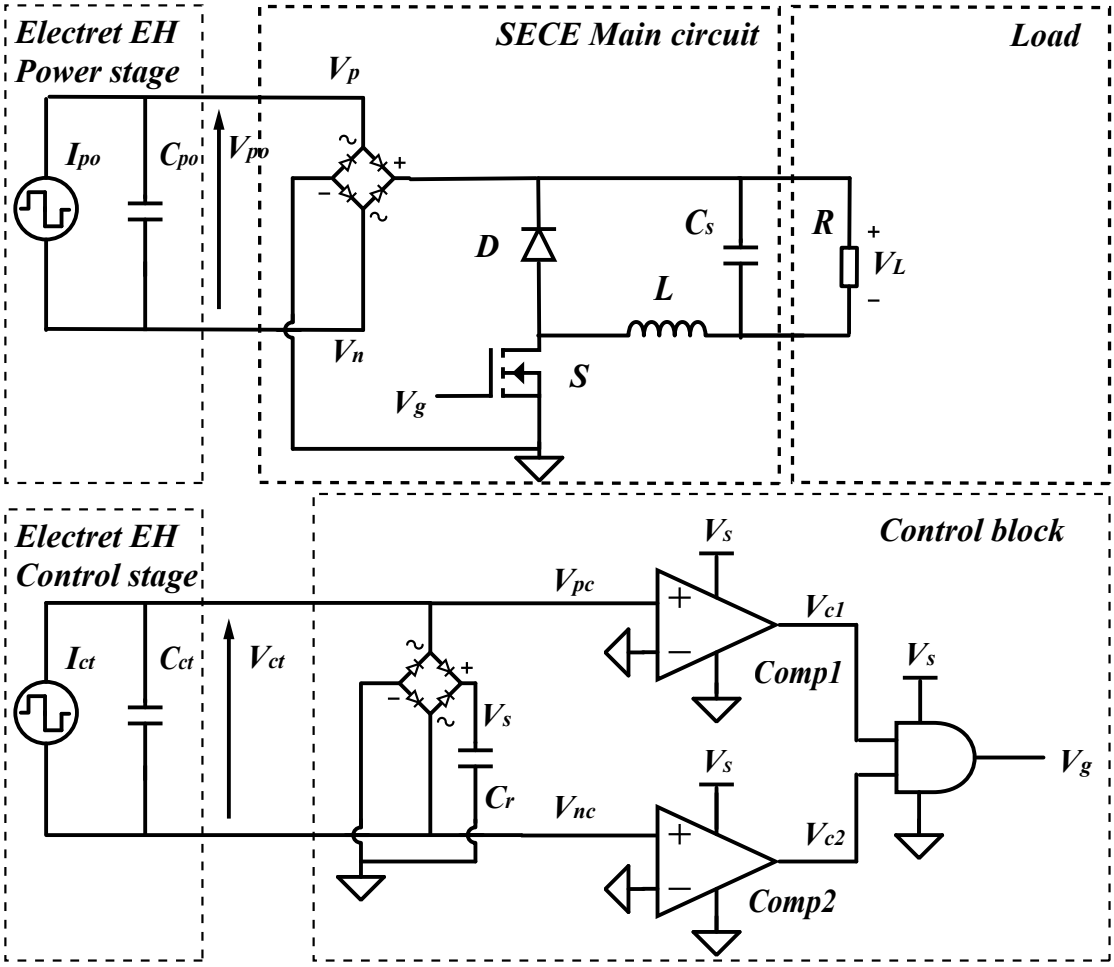


Figure 5-10 Circuit design of dual-stage SECE.

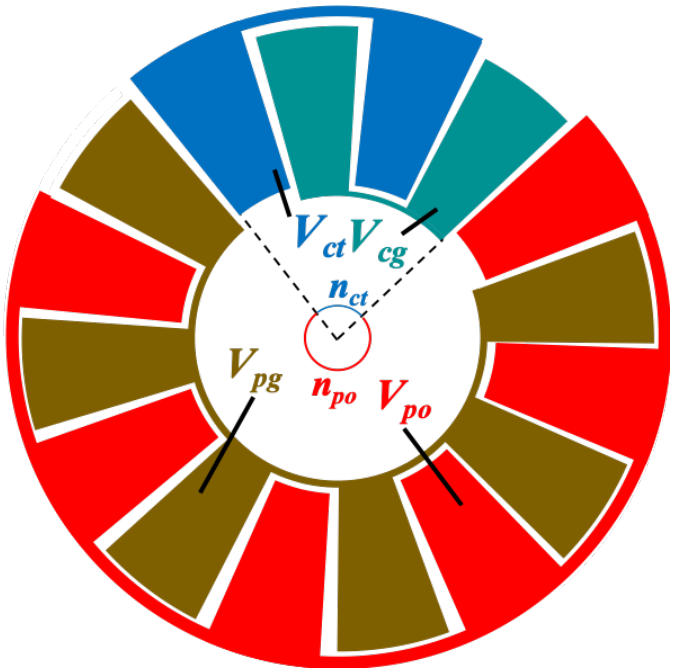
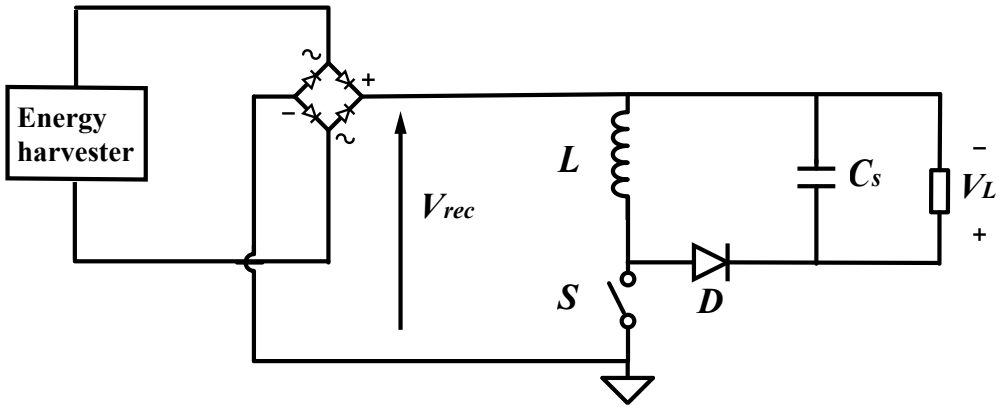
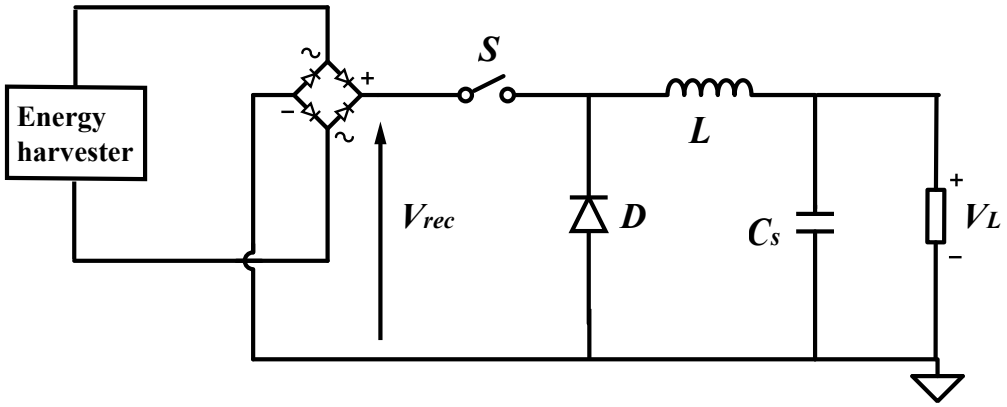


Figure 5-11 Pole-number-based dual-stage electrode design for SECE.

(a)



(b)



(c)

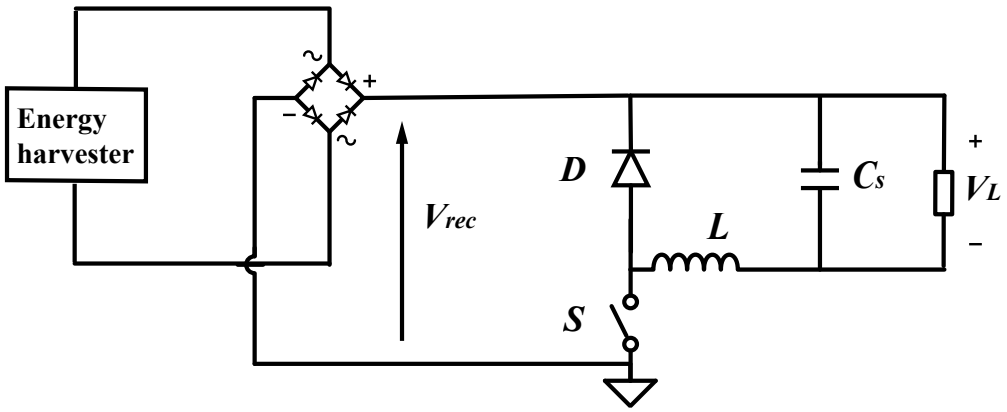


Figure 5-12 Topologies of SECE main circuit, (a) parallel L-C_s, (b) high-side switch and (c) series L-C_s.

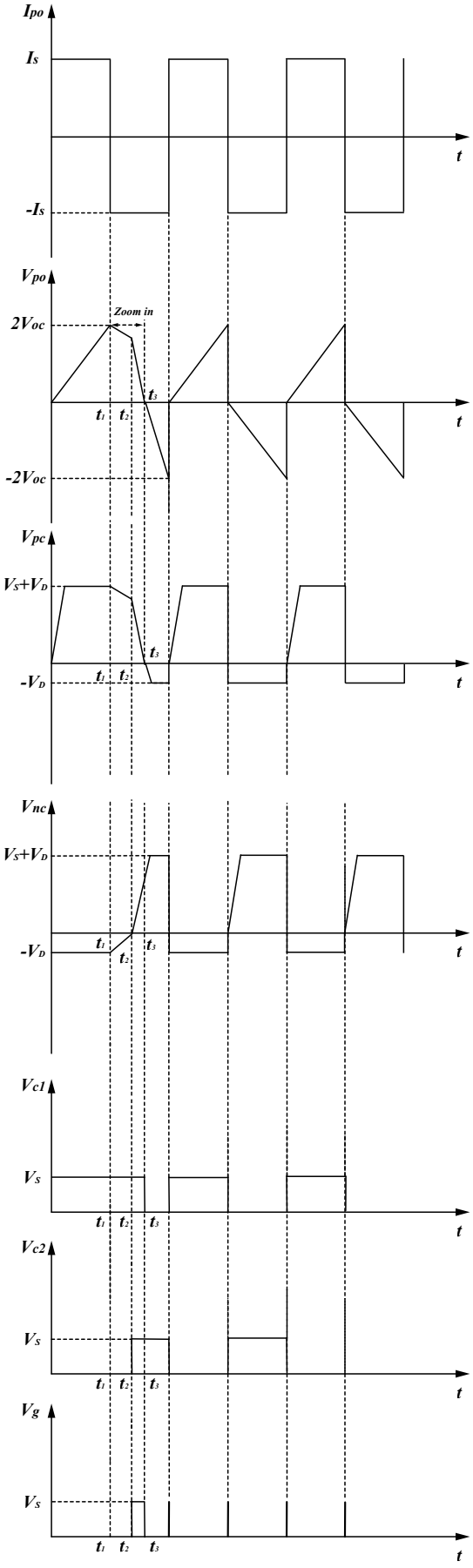


Figure 5-13 Waveforms in dual-stage SECE operation.

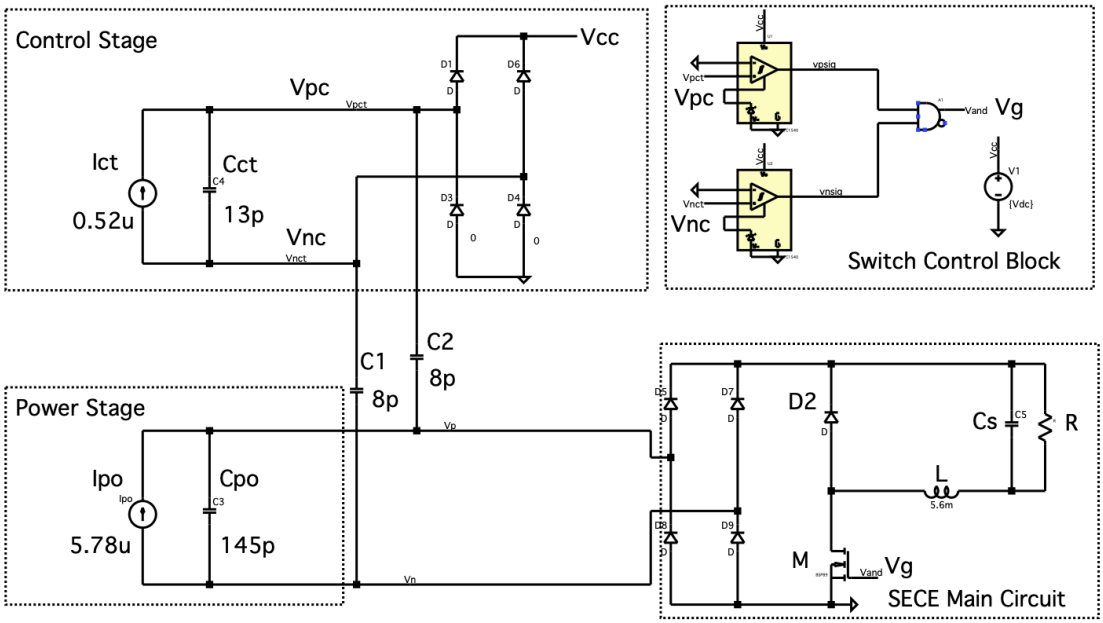


Figure 5-14 Simulation setup of dual-stage SECE.

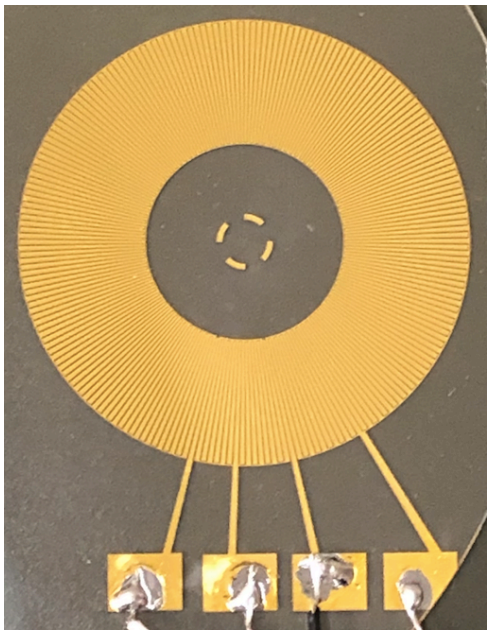


Figure 5-15 Pole-number-based dual-stage stator electrode for SECE experiment (N_{ct}=9, N_{po}=100).

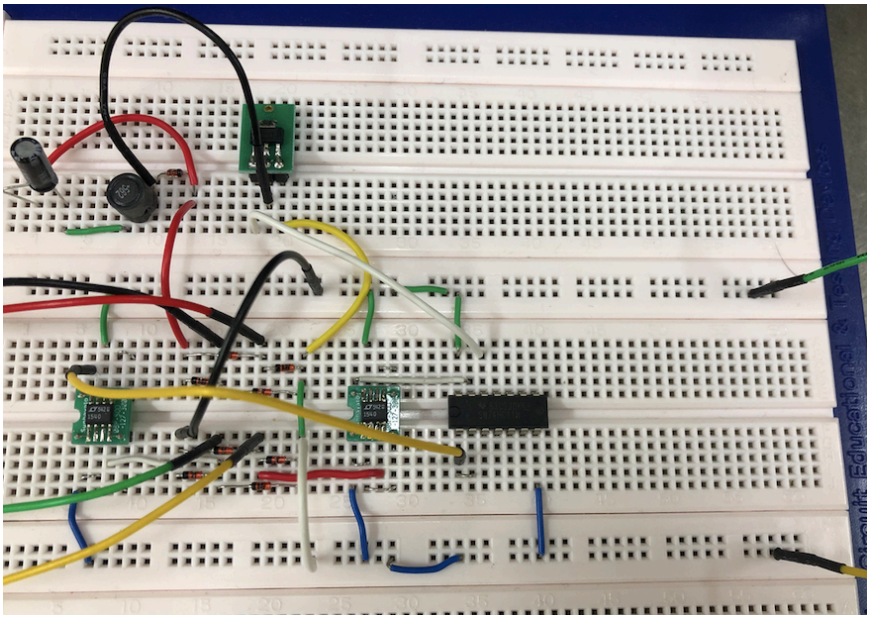


Figure 5-16 SECE circuit using discrete components.

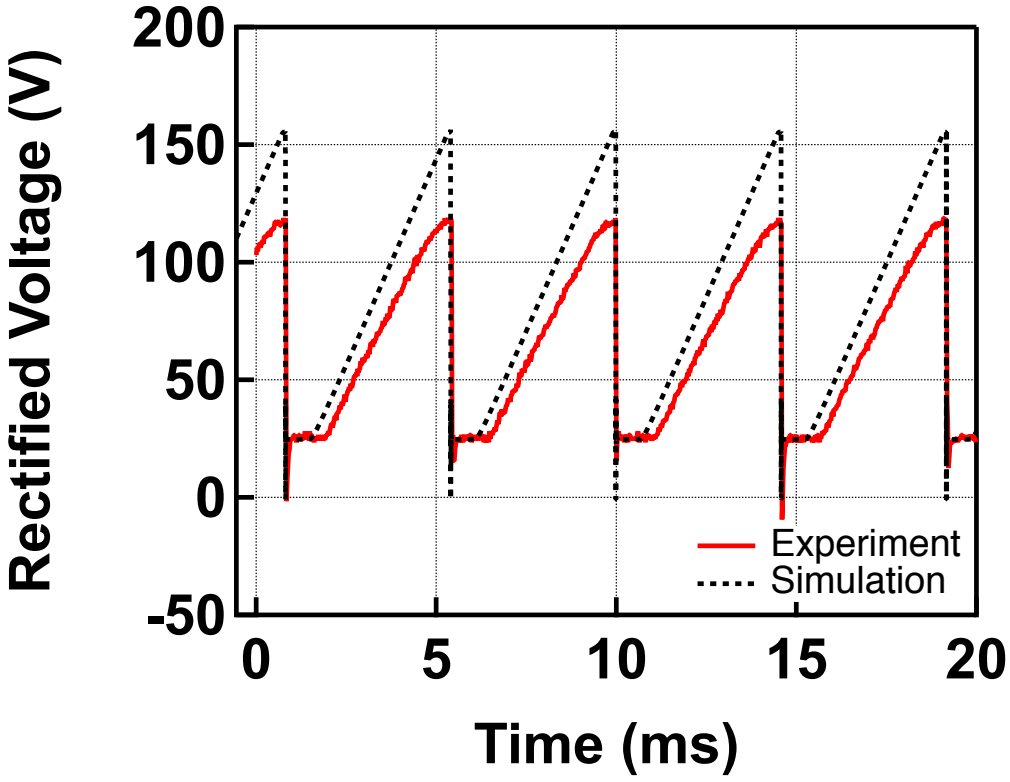


Figure 5-17 Simulated and measured generator voltage with SECE (R_L=2 MΩ).

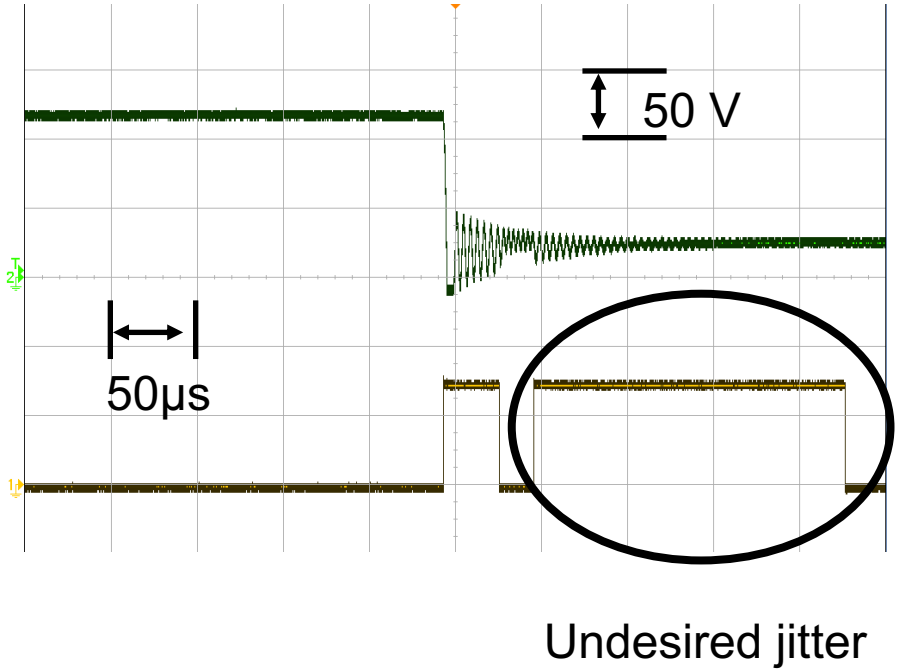


Figure 5-18 Observed unexpected switch action in SECE operation.

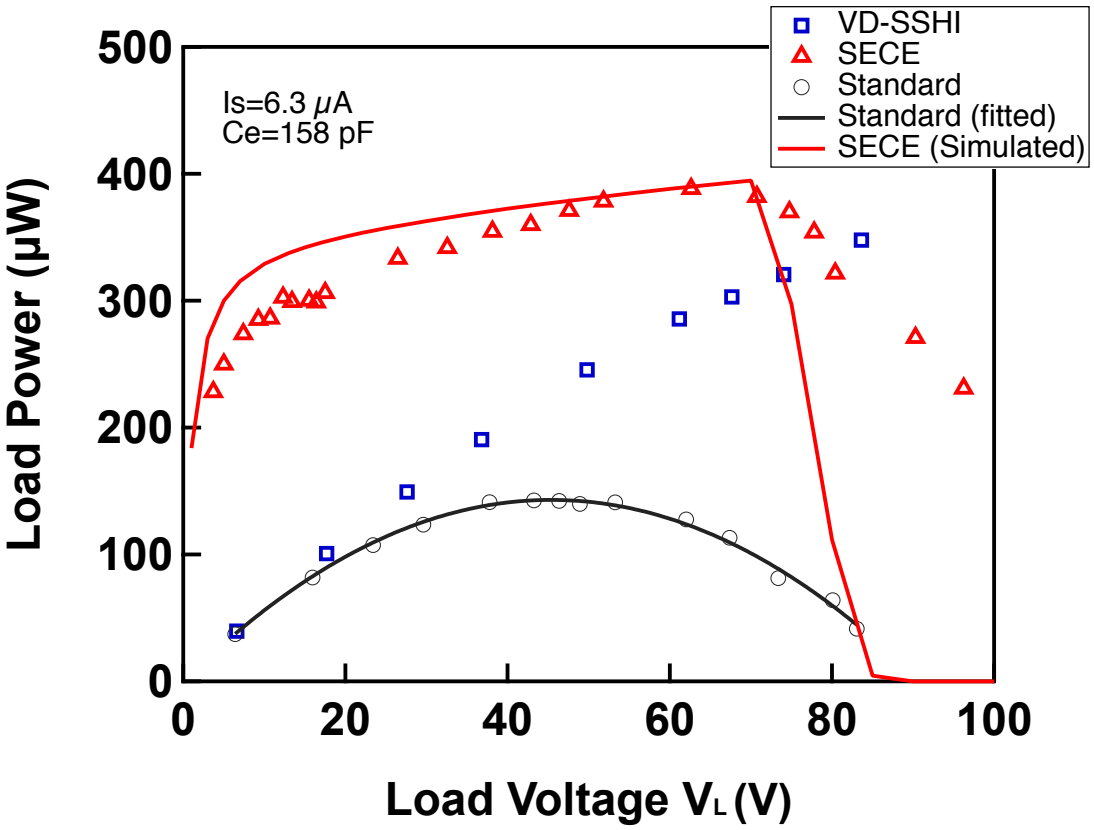


Figure 5-19 Power generation results in SECE (externally powered).

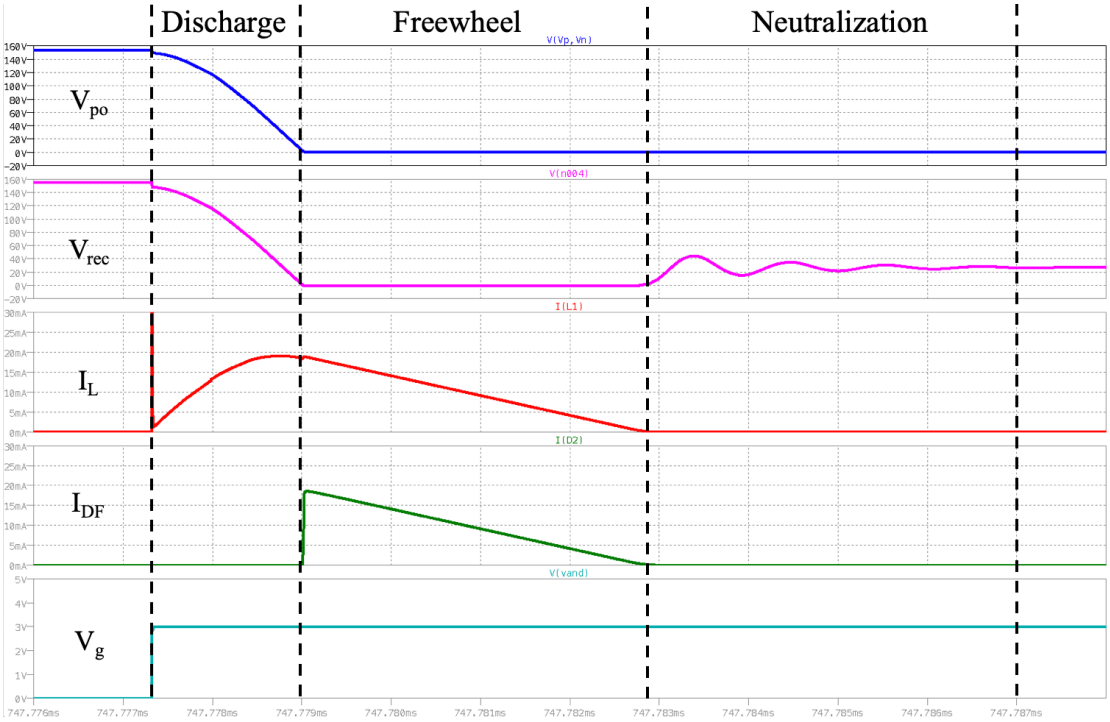


Figure 5-20 Power transfer process in SECE.

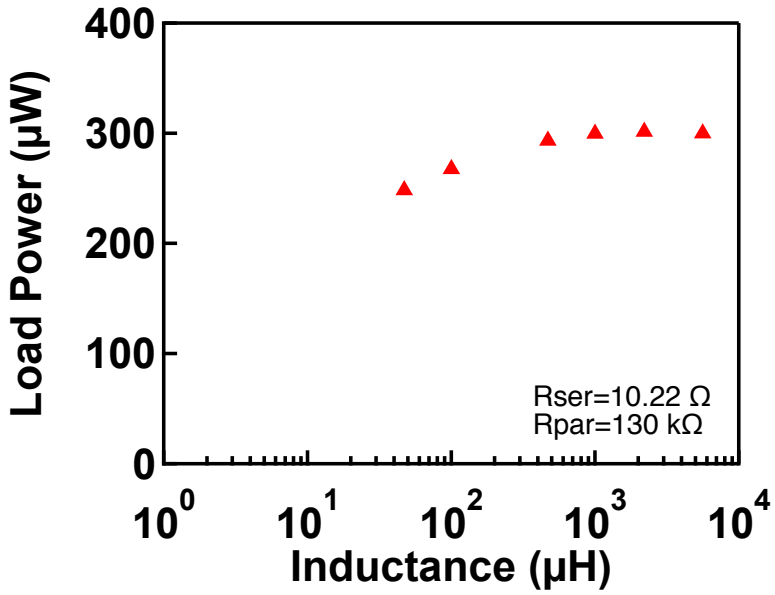


Figure 5-21 Load power as a function of the inductance of the inductor *L* at a load voltage of 5 V.

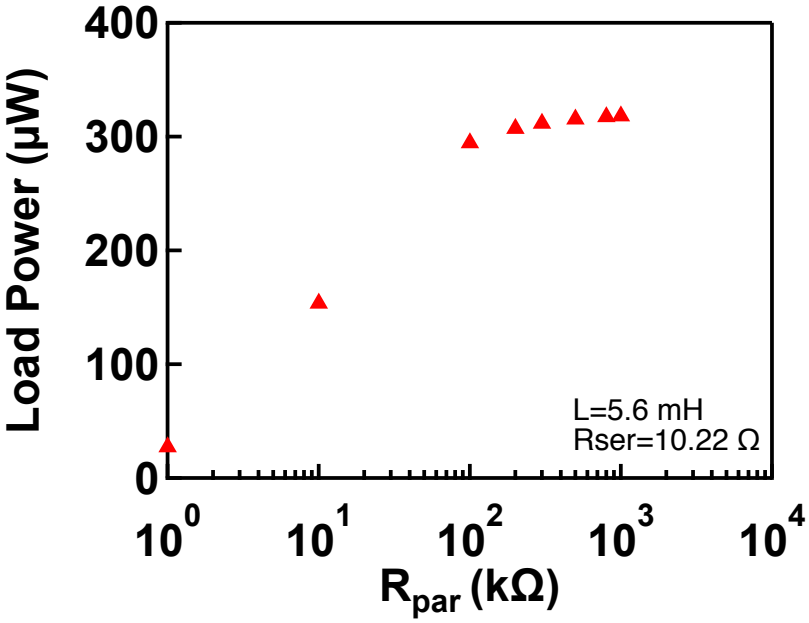


Figure 5-22 Load power as a function of the parallel resistance of the inductor R_{par} at a load voltage of 5 V.

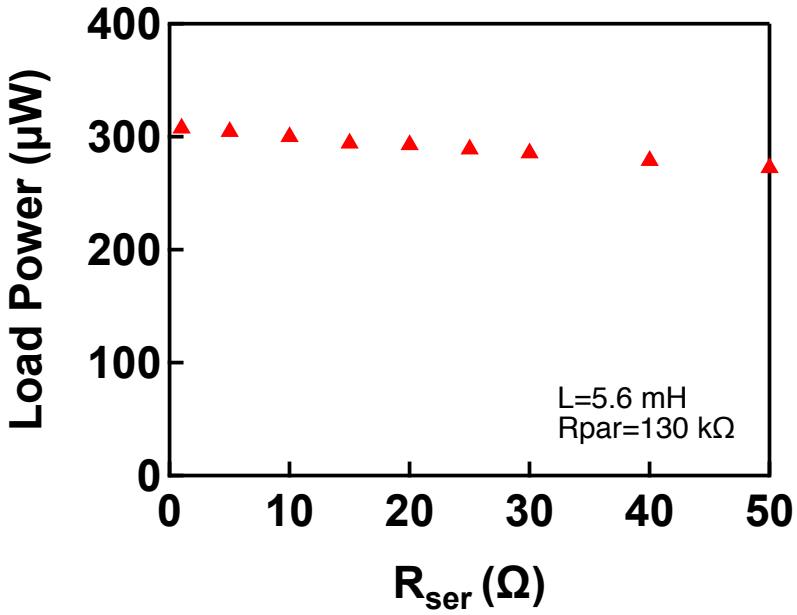


Figure 5-23 Load power as a function of the series resistance of the inductor R_{ser} at a load voltage of 5 V.

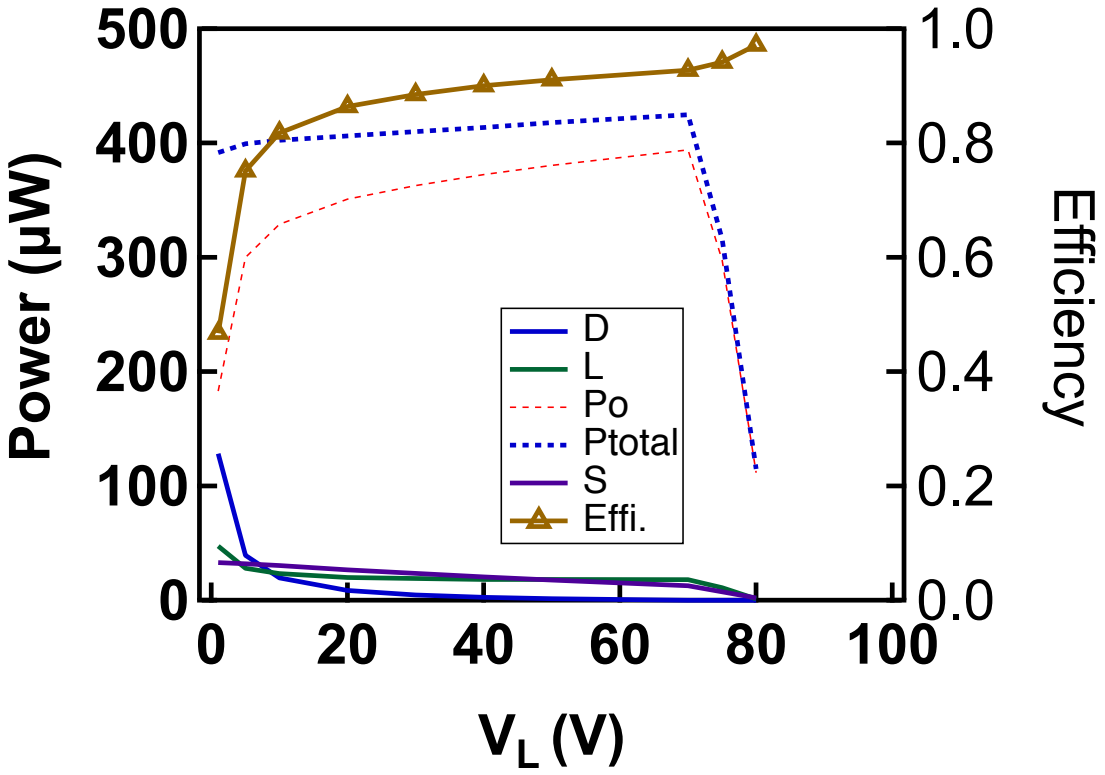


Figure 5-24 Power consumption of the components in SECE.

Chapter 6 Toward IC-friendly Nonlinear Circuits

IC technology can contribute to nonlinear circuits in three ways: (1) it can effectively reduce the volume of the circuit (especially control circuitry working in low voltage); (2) it can reduce the power consumption of components, especially the power dissipation of the control block, thereby enabling more energy efficient self-powering schemes; (3) It may increase the performance of the proposed nonlinear circuits by improved peak/zero detecting accuracy and immunity to noises. Therefore, it is meaningful to investigate the applicability of the proposed circuits to IC technology.

6. 1. PCB-based prototype of dual-stage SECE

6. 1. 1. Prototype description

Figure 6-1 shows a PCB-based prototype of dual-stage SECE using discrete components. It is fabricated to roughly estimate the volume of dual-stage SECE and to check its performance. As shown in Figure 6-2, the board contains 3 parts: (1) The main circuit of SECE, which operates at 200 V or more; (2) The control block of SECE. which operates at 5V or lower; (3) The hysteresis switch intended for sensor node operation, which operates at 5V or lower.

The total area is 24 mm x 24mm. The SECE circuit is on the front side; whilst the hysteresis switch is on the back side (Figure 6-3). The height of the SECE part is 3.6 mm, 0.3 mm taller than rotational electret energy harvester. The height of inductor (1 mH) used here is 2.6 mm. The area of this prototype can be further minimized by integrated the control circuit and the hysteresis switch using 5V CMOS technology. In that case, the total area is expected to be 15 mm x 15 mm. To further integrate the main circuit, it is possible to employ the high-voltage process shown in Figure 6-4.

6. 1. 2. Test results

In the standard case, the generator outputs, both power and control stages, are connected to a high-input-impedance (1GΩ, 5pF) voltage probe (HV-P60A), to emulate the open-circuit condition (Figure 6-5). The measured voltage amplitude in this case is around 100V (Figure 6-6).

In the SECE experiment, the control block is externally powered by a 3 V DC supply. The rectified voltage V_{rec} is measured by the HV-P60A voltage probe. The gate voltage V_g to the switch is measured by a 100:1 voltage probe.

Figure 6-8 shows the measured voltages in SECE case. The typical voltage waveform in SECE is obtained at control stage output. The measured voltage amplitude is 170V. Theoretically, the amplitude should be 200V, twice of the open-circuit voltage in standard case. The reason for this discrepancy might be (1) introduced 1 GΩ impedance by the voltage probe, (2) overlong ON-state duration of the switch.

To check the power enhancing performance, two cases, SECE and classic buck converter, are considered for a fair comparison (Figure 6-9). In the SECE case, SECE is inserted between the generator and the low-voltage load. In the classic BUCK case, a full-bridge rectifier and a classic buck converter are inserted.

Figure 6-10 shows the power generation results. The power harvested in SECE is twice of that in classic buck case, at a load voltage of 5V. The performance of SECE should be further improved by employing an inductor with higher inductance.

6. 2. IC compatibility of current nonlinear circuits

Obviously, the control block in the nonlinear circuit is compatible with low-voltage IC process. If the main circuit is also to be integrated, high-voltage IC process should be employed in the main circuit to address the voltage stress. Figure 6-4 shows the available Bipolar-CMOS-DMOS (BCD) processes provided by STMicroelectronics Co. which can tolerate as high as 800V [70].

The remaining off-chip components are inductors over nH-level and capacitors over μF-level. For capacitors, usually the storage capacitors at low-voltage load side are several microfarads. Fortunately, off-chip surface-mount capacitors are usually low in profile, so the capacitor is not a concern. As for the inductor, in dual-stage self-powered SSHI (Figure 6-11), 3 inductors cannot be integrated (1 in main circuit and 2 in dual-polarity converter), which makes the system bulky. In dual-stage SECE, only 1 inductor (~100 μH) cannot be integrated and it can be tailored to be low profile according to previous discussion. Therefore, dual-stage SECE is more IC-friendly compared with dual-stage SSHI.

6. 3. Tri-stage IC-friendly SSHI

To reduce the inductor counts in dual-stage SSHI, here a tri-stage SSHI is proposed. It employs a more energy-efficient self-powering scheme, instead of dual-polarity converter, to remove two inductors used in dual-polarity converter. A classic

unipolarity rectifier which exhibits higher efficiency and smaller size is then used for voltage regulation.

The self-powering is achieved by introducing a third stage to provide a dual-polarity voltage supply directly to the peak detector. With the aid of IC technology, it might be feasible if the power consumption of the control block reduced by IC design could match the very little power generated by the electret energy harvester.

Figure 6-12 shows the tri-stage electrode design. It contains three stages, of which function is shown in Figure 6-13. The power stage, which occupies major poles, is in charge of power generation. The sensing stage, which occupies 1~3 poles, is a low voltage serving as the input signal to the control stage. The supply stage, which occupies around 10 poles, is connected to a half-bridge rectifier, to attain a dual-polarity DC output voltage for suppling the control block.

6. 4. Summary

The IC-compatibility of the proposed circuits is investigated in this chapter. The results are summarized as follows:

(1) In view of the PCB-based prototype, dual-stage SECE circuit exhibits a volume of 24 x 24 x 3.6 mm^3 using discrete components. With control block integrated, the chip is expected to be 15 x 15 x 3.6 mm^3

(2) If high-voltage BCD process is employed, all the parts of dual-stage SECE, except the inductor, can be integrated. The inductor, on the other hand, could be tailored to be low-profile in our case. Therefore, low-profile nonlinear circuit is feasible for electret energy harvester.

(3) Toward the IC-friendly nonlinear circuits, tri-stage SSHI is proposed for efficient operation of SSHI by removing the low-efficiency dual-polarity converter. It could be achievable if the power consumption of the control block is reduced by IC design.

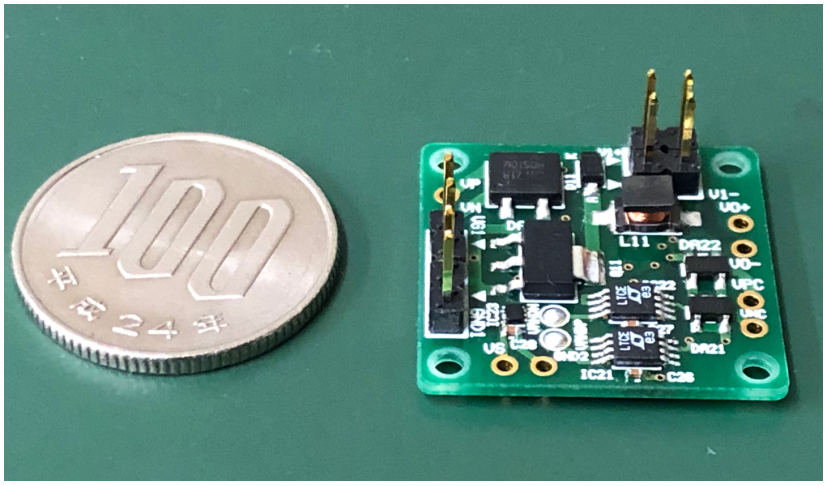


Figure 6-1 PCB-based prototype of dual-stage SECE circuit.

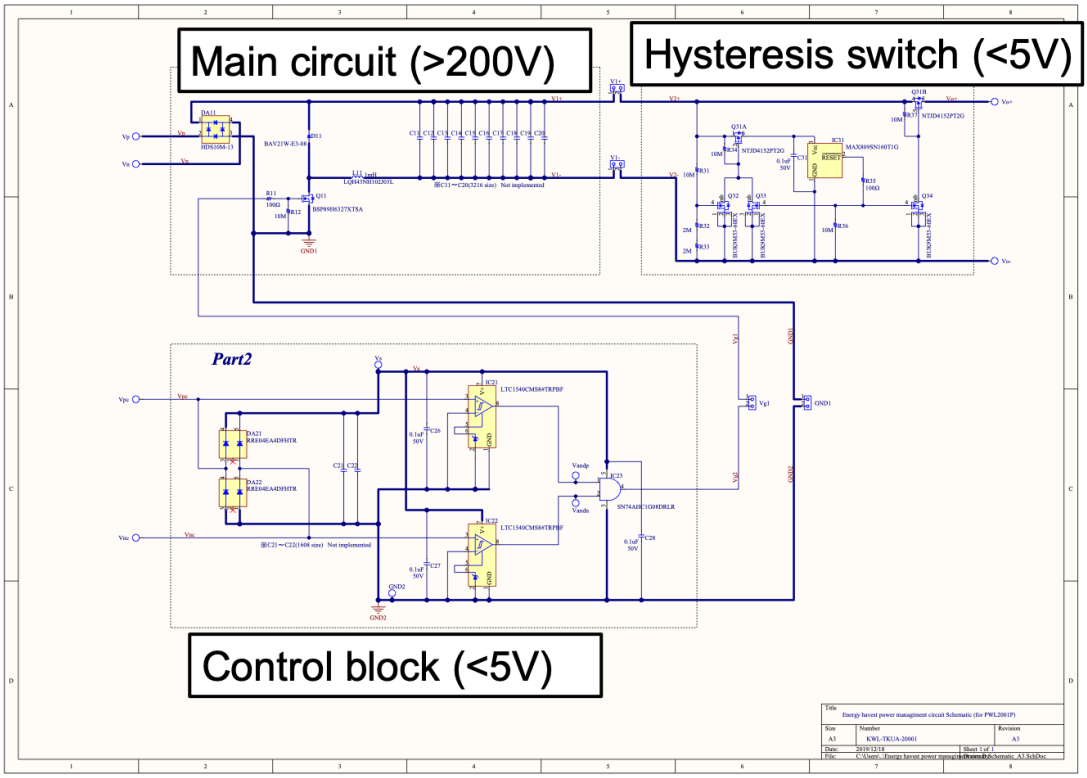


Figure 6-2 Circuit diagram of dual-stage SECE circuit (Hysteresis switch is for WSN operation).

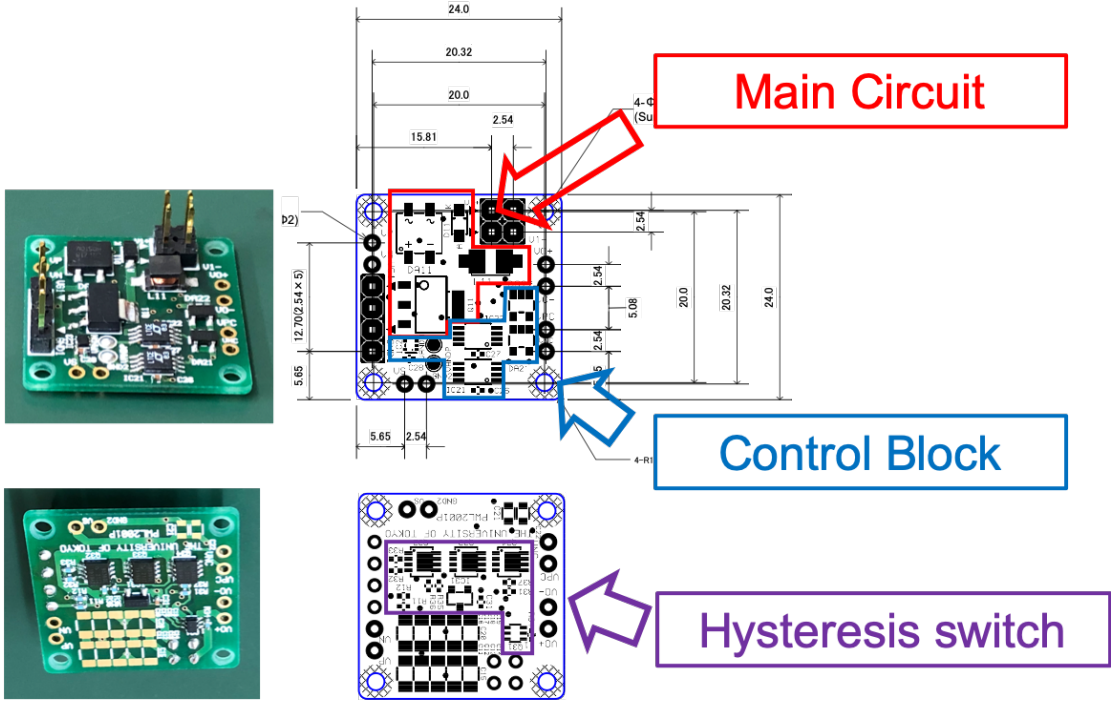


Figure 6-3 Specification of each part in the PCB-based SECE board.

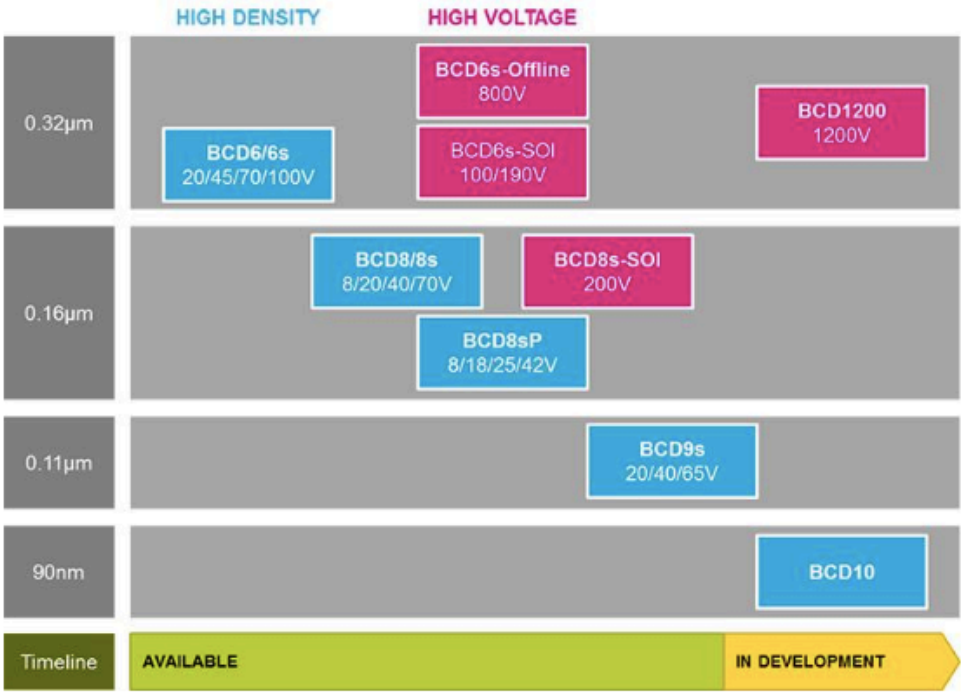


Figure 6-4 Available high-voltage IC processes for nonlinear circuits for electret energy harvester [70].

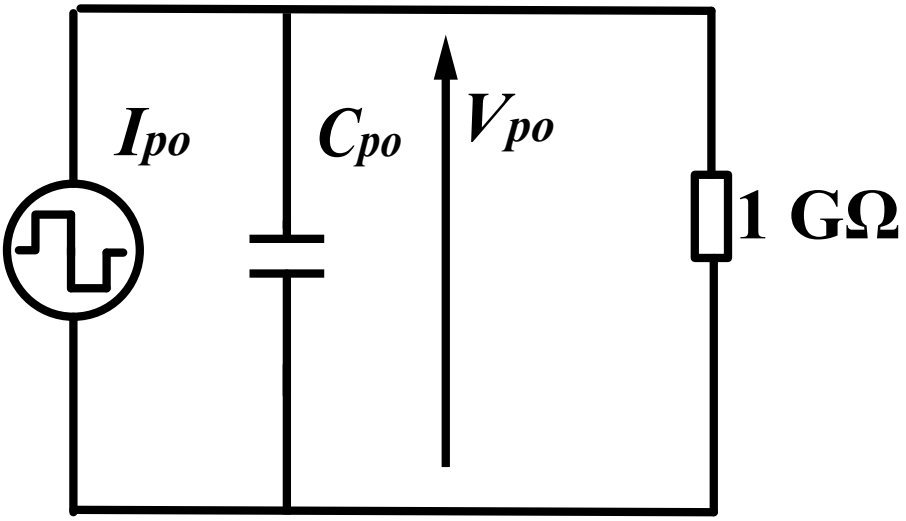


Figure 6-5 Standard case (1 GΩ denotes the input impedance of the probe).

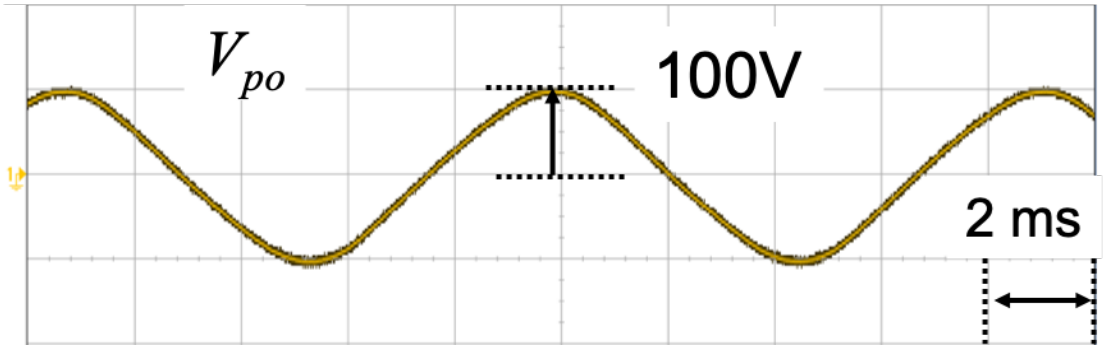


Figure 6-6 Measured open-circuit voltage in standard case.

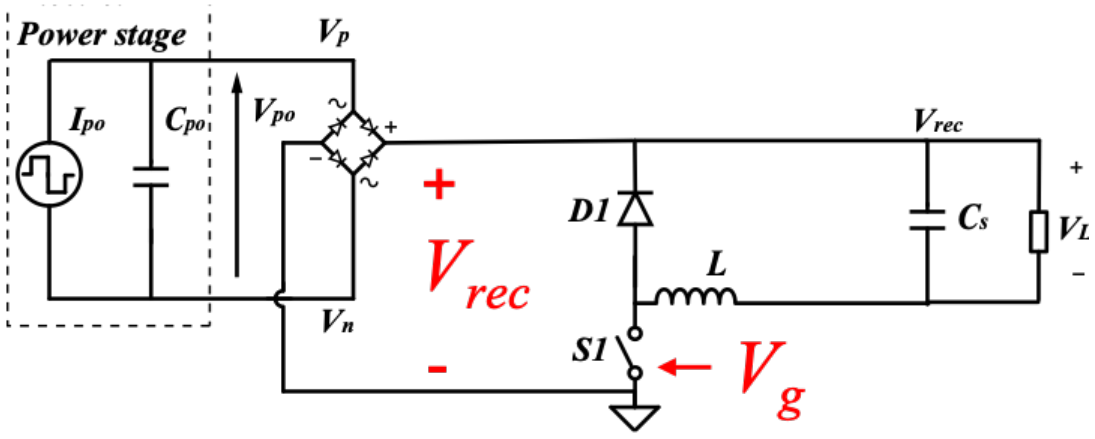


Figure 6-7 Circuit diagram of dual-stage SECE where rectified voltage V_{rec} and switch control signal V_g are to be measured.

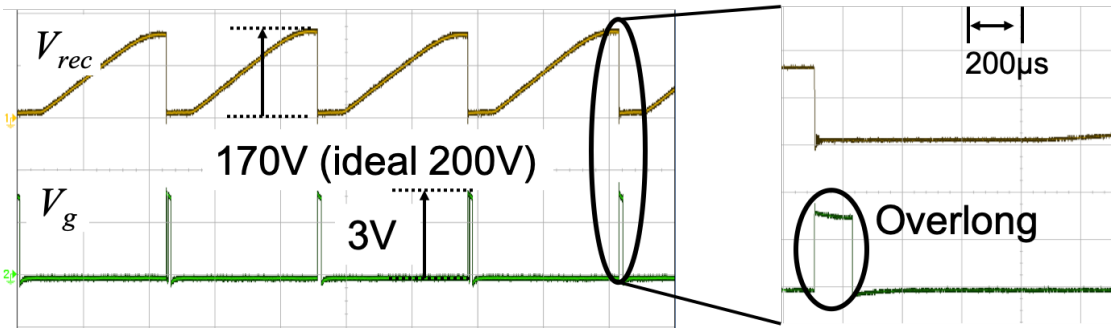


Figure 6-8 Measured voltages in SECE based on PCB board.

Figure 6-9 Cases measured in power generation experiment.

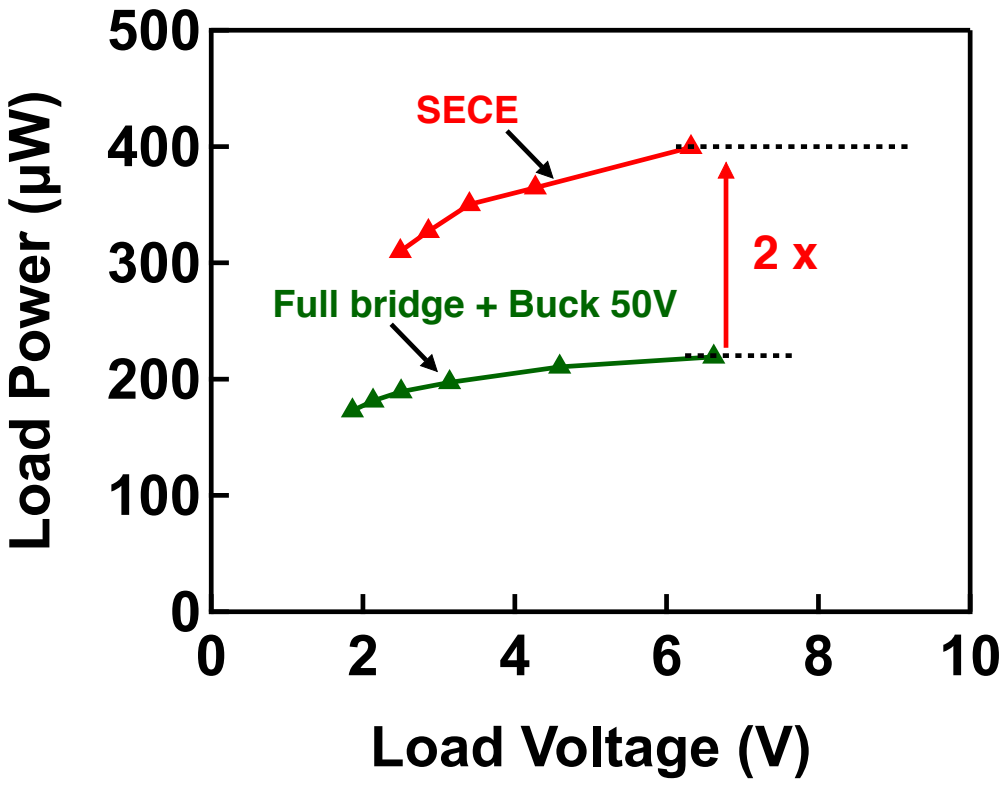
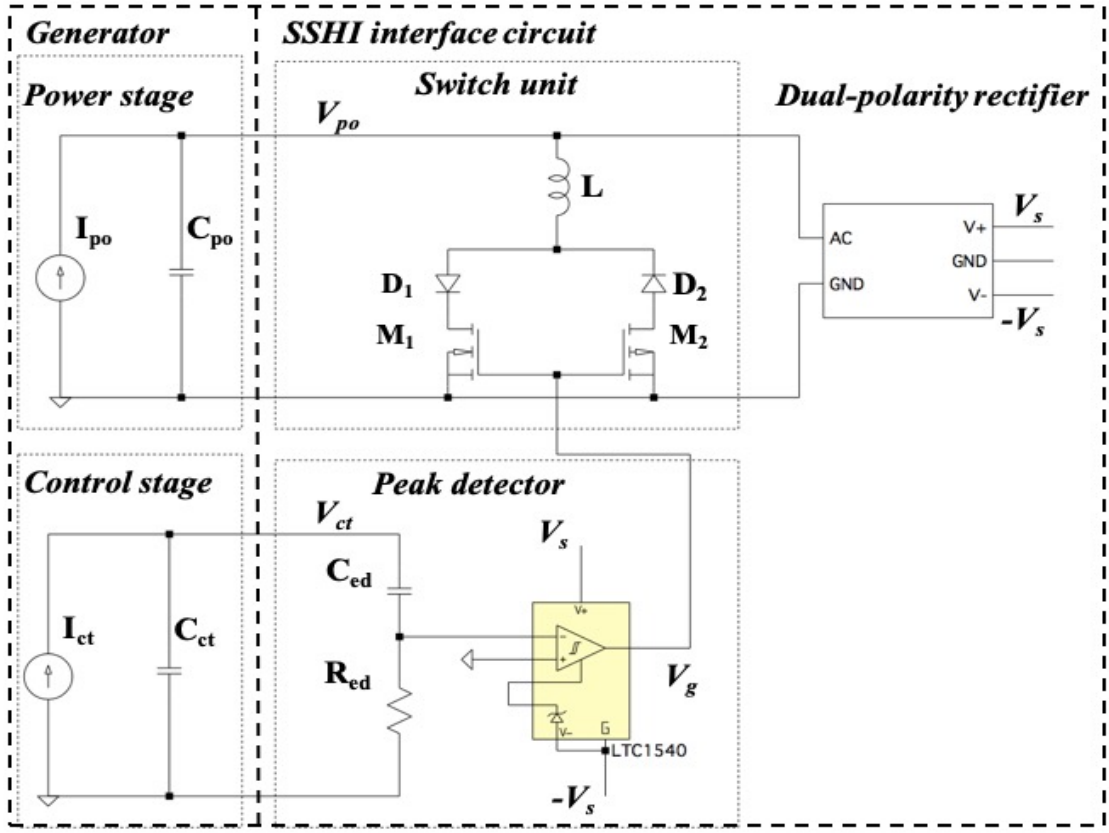


Figure 6-10 Power generation results.

(a)



(b)

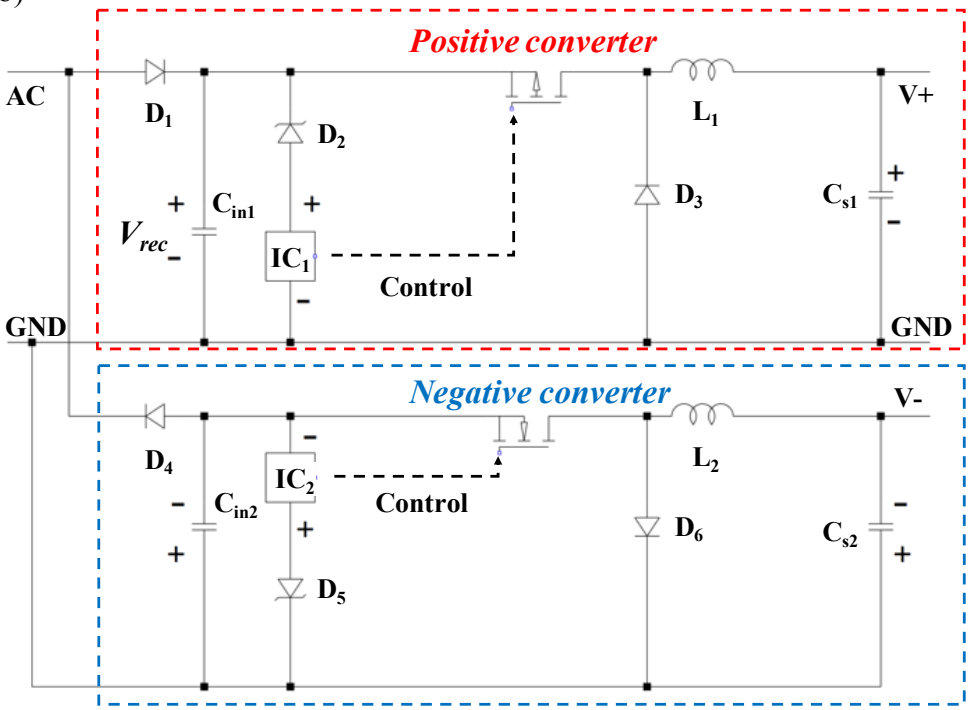


Figure 6-11 Dual-stage SSHI circuit design, (a) the whole system, (b) dual-polarity rectifier.

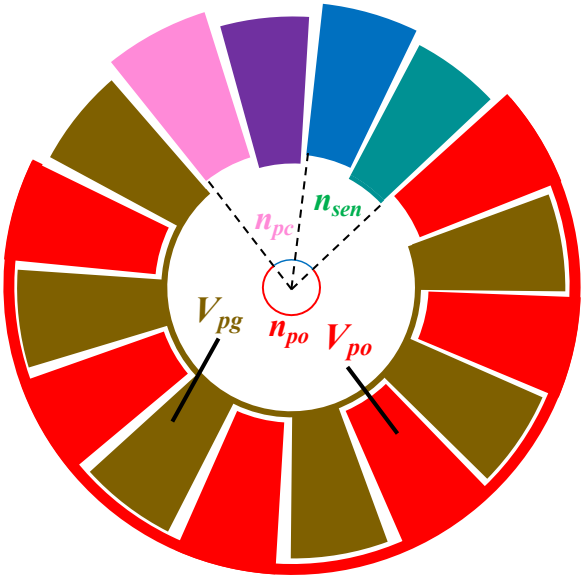


Figure 6-12 Tri-stage electrode design for efficient SSHI by removing dual-polarity converter.

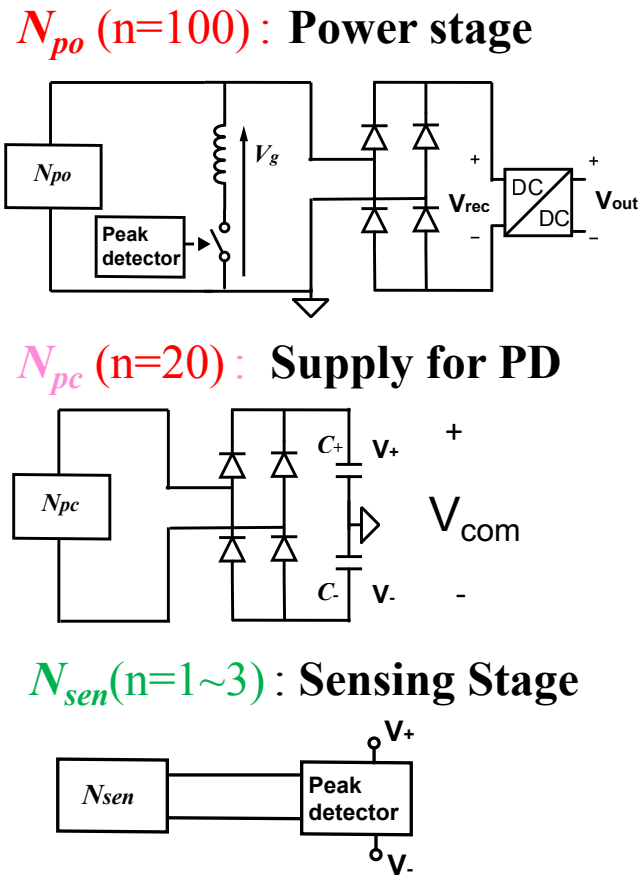


Figure 6-13 System description of tri-stage SSHI.

Chapter 7 Conclusions

The present study presents the development of nonlinear power management circuits (SSHI, SECE) for electret kinetic energy harvester for the first time, featuring a novel multiple-stage electrode design. In addition, improved analysis of nonlinear circuit operation is carried out. The new knowledge derived from this analysis could apply to circuit design for other electrostatic energy harvesters. Specifically, the following conclusions have been obtained:

(1) An explicit generator model of in-plane electret energy harvester is proposed for the first time. The model predictions are in good accordance with the experimental data using a power generation test bench of rotational electret generator. It reveals that in-plane electret EH behaves like piezoelectric ones, which confirms the applicability of nonlinear circuits (SSHI/SECE). According to the dynamic model, the electrical restoring force is proportional to the output voltage, in which the coefficient (force factor) has been analytically derived for the first time. Based on the generator model, an electromechanical model of in-plane electret linear vibration energy harvester is derived. Thanks to the absence of intrinsic stiffness, electret energy harvester presented stronger electromechanical coupling based on the case study. Based on the circuit model, it is confirmed that electret EH is susceptible to parasitic capacitance which may led by the nonlinear circuit, and sensitive to leakage current.

(2) SSHI has been developed for electret energy harvester for the first time. A power enhancing ratio of 2.47 over the conventional full-bridge rectifier has been obtained in the present experiment, with control block externally powered. Unlike in piezoelectric EHs, the inversion ratio, which is usually used as a benchmark to indicate power enhancing performance of SSHI, shows little dependence on the series resistance of the inductor. This new finding allows reducing the size of inductor at the expense of series resistance. The presented voltage-divider-based SSHI (externally powered) circuit shows merely an efficiency of 50% at optimal voltage. It is found that the main power loss lies in the lossy voltage divider and rectification diodes. In self-powered SSHI, the ratio reduced to 1.2 due to the limited efficiency and voltage rating of the proposed dual-polarity converter. The efficiency of self-powered SSHI reduces to 25% owing to the low efficiency of the proposed dual-polarity rectifier.

(3) A novel dual-stage electrode design is proposed for efficient SSHI by removing the lossy voltage divider. As a result, a power enhancing ratio of 4 over the standard case is experimentally achieved in the dual-stage SSHI (externally powered), which is 1.56 times of the power harvested with the voltage-divider SSHI. The proposed dual-stage SSHI is successfully implemented to a fully-integrated rotational electret energy harvester, with power enhancing performance, self-start and self-powering ability of dual-stage SSHI under random excitation confirmed. But, in the self-powered mode, the power enhancing ratio of dual-stage SSHI again reduces to 1.4 in the self-powered SSHI, indicating an overall efficiency of 25%, due to the low voltage rating and low efficiency of the dual-polarity converter.

(4) A novel dual-stage SECE circuit is proposed for the first time to achieve a higher overall power enhancing performance over SSHI at low load voltage range, by removing the low-efficiency and bulky dual-polarity converter. Thanks to its buck converter topology, the proposed dual-stage SECE also achieves voltage-stepping-down function. The proposed control block is easy to realize and adaptive to arbitrary internal capacitor and external inductor, thus enabling a robust operation against generator/components aging. Experimentally, a power enhancing ratio of 2.77 is obtained in SECE, with control block externally powered. More importantly, a power enhancing ratio of 2 is achieved at a load voltage as low as 5 V, which means no additional DC/DC converter is needed. The voltage stress at generator output is twice of the open circuit voltage in the standard case, which is also much lower than that in the SSHI case. Self-powering schemes are also proposed by using the charges accumulated in the storage capacitor of the control stage. Based on the simulation, the efficiency of proposed SECE circuit is above 80%, thanks to the high LC quality factor led by the ultralow internal capacitance of the generator. The inductor in SECE could be lower than 100 μH without severely reducing the power enhancing performance, which is in favor of the circuit miniaturization. Reducing the forward voltage drop of the freewheel diode is crucial to improve the SECE performance in low load voltage range.

(5) Using a PCB-based low-profile SECE board, doubled harvested power (compared with classic buck converter) was obtained at a load voltage as low as 5 V experimentally. With control block integrated with 5 V IC process, the volume of SECE board is expected to be 15 x 15 x 3.6 mm. It can be further miniaturized with the main circuit integrated using high-voltage BCD process.

(6) The RLC resonant loop in electrostatic energy harvester is found to be closer to parallel RLC model, where the quality factor is hardly influenced by the series resistance of the inductor. Therefore, it is valid to scale down the inductor at the expense of increasing the series resistance. This generic knowledge should apply to other types of electrostatic devices where LC resonance is employed.

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Publication List

International Conferences

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