博士論文

On-chip LSI Cooling Device Using Electroosmotic Flow Micropump Integrated with High-Voltage Generator

(高電圧生成回路集積
電気浸透流マイクロポンプによる
オンチップ LSI 冷却機構)

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指導教員　三田　吉郎　准教授

東京大学大学院工学系研究科
電気系工学専攻

37-177067

岡本　有貴

Abstract

Within the past decade, there has been rapid advancement of three-dimensional stacked integrated circuits (3DIC). The technology has not only improved the interconnection performance and power dissipation but also increased the number of I/Os. Although the 3DIC technology has still developed by increasing the number of stacked chips and thinning the chips, these developments decrease thermal conductance and degrade the thermal dissipation leading to increase heat density in a device. It degrades the performance of chips and causes a shorter lifetime of the chips. As a result, the cooling of 3DICs is an essential issue to be solved to develop integrated circuits.

For cooling of 3DICs, forced liquid cooling and liquid-vapor convection in micro-channels have gotten attention. While the other cooling components such as heat-pipes and vapor chambers require a large volume of a bulk heat sink on the backside of the chip, the required volume on the backside is low in the micro-channel cooling. Due to the advantage, the micro-channel cooling device can be integrated into 3DICs. However, conventional micro-channel cooling methods require extensive bulky liquid circulating systems such as a pump, condenser, and chiller. These components not only occupy lots of space but also have low reliability of cooling. Therefore, to decrease the size of the cooling components and failure rate, integrating active fluid components in cooling devices is essential.

As an active fluid component, micropumps is one of the significant parts. Electroosmotic flow (EOF) micropumps are one type of electrokinetic micropumps, and it is based on the free ion movement in conductive fluids. The attractive feature of the EOF micropump is that it does not require mechanical moving structures and air gaps and that it can output high pressure in micro-channels. However, some issues still exist to use EOF micropumps. One of the most significant issues is the driving voltages of the micropumps. Compared to mechanical micropumps, which conventionally require at most 200 V, the EOF micropumps require higher voltages than at least 40 V (in some cases over 800 V). This has prevented the integration of micropumps into 3DICs since these high voltages are higher than maximum voltages of commonly-used through-silicon-vias (TSVs) connecting stacked chips. Another issue of EOF micropumps is a measurement method of surface parameters. The performance of EOF micropump depends on the surface charges of EDL, which is changed by the surface condition. However, as the conventional method cannot measure the surface charge without breaking the device, the prediction of fabricated EOF micropumps was difficult.

This dissertation presents the design, fabrication, and testing of a novel cooling device having an on-chip micropump integrated with an on-chip high-voltage generator to drive the micropump. The high-voltage generator is realized by standard CMOS technology and MEMS post-processes called post-processed deep-trench-isolation (or mesa isolation). Due to the isolation, the breakdown voltages of the standard 5 V transistors can be extended up to 800 V.

Firstly, the process optimization of MEMS post-process deep trench-isolation to form the complete isolation of transistors has been discussed. The process optimization is performed using novel test structures that do not require breaking the measurement samples, and two

different etching modes are found. By using the optimized process, a high-voltage switch is presented to demonstrate the use of the post-processed high-voltage transistors, and also a high-voltage generator using the post-processed high-voltage transistors is presented. Then, the design, fabrication, and analysis of the on-chip integrated EOF micropump using the high-voltage generator are discussed. Besides, to predict the performance of an EOF micropump, a novel on-chip zeta potential measurement sensor is discussed. Finally, the cooling efficiency of micro-channel devices is investigated. By the experimental results, we have found two cooling modes of the micro-channels depending on the flow rate. Besides, the suitable placement of micro-channels and a micropump in each cooling mode is presented.

In summary, this dissertation reports an integrated micro-channel cooling device. The integrated on-chip EOF micropump is driven by a high-voltage generator using post-processed deep-trench-isolated transistors. Having high reliability and high-voltage output of the integrated high-voltage generators in microfluidic devices also enhances the other applications such as point-of-care devices and one-chip micro total analysis systems. The cooling demonstration using micro-channel devices indicates the future integration of these devices into power-consuming circuit chips, including a processor and 3DICs.

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CHAPTER 1

Introduction

1.1. Three-dimensional Stacked Integrated Circuit

Large-scale-integrated (LSI) circuits using metal-oxide-semiconductor field-effect transistors (MOSFETs) have rapidly been developed by scaling the transistors following the Dennard's scaling law. Scaling of the transistors has not only improved the performance of LSI circuits by increasing the number of transistors on a chip but also reduced the power consumption. However, as the leak current is drastically increased during the scaling down, the power consumption is no longer reducible. Although new structures such as multi-gate transistors are proposed and now commercially used [1], power consumption is still substantial. Moreover, the fabrication of smaller transistors such as 7 nm-nodes requires the latest technology, such as extreme ultraviolet (EUV) lithography. It causes an increase in manufacturing cost per die and the number of fabrication steps. Consequently, the development of LSI circuits by scaling transistors is now quite challenging.

Despite the issue, there is a lot of demands for higher-performance chips to process a large amount of data for high-performance computing and graphics applications. The

demand is especially apparent in memory devices such as dynamic random access memory (DRAM) and flash memories. To meet the demand, the data rate per pin of DRAM chips has increased to increase the bandwidth. However, it is hard to increase the data rate per pin more than 10 GB/s. Although multiple DRAM chips are used to obtain higher bandwidth, power consumption is extremely high in such a system. Moreover, the data congestion and degradation are considerable due to long wiring on a printed circuit board (PCB) is substantial.

To resolve these issues, three-dimensional stacked integrated circuits (3DIC) is a promising technology. 3DIC is a vertically stacked device, which is composed of several dies and interconnected using through-silicon-via (TSV). 3DIC technology has been improving interconnect performance and power dissipation. Besides, this technology allows us to increase the number of I/Os. While the conventional DRAM such as GDDR4 DRAM has 32 I/Os, wide I/O and high-bandwidth memory (HBM) have achieved 512 and 1024 I/Os, respectively [2], [3]. Due to the lots of I/Os, the bandwidth of Wide IOs and HBM in [3] are reached 68.2 GB/s on a processor and 307 GB/s next to a processor. In the latest graphics processing unit (GPU), such stacked DRAM chips are used and connected to a processing chip through silicon interposer in a package called system-in-package (2.5DIC). A GPU company expects the processing chip is also stacked with DRAM and other chips [4].

1.2. Thermal Issues in 3DICs

The 3DIC technology is still developed by increasing the number of stacked chips and thinning the stacked chips. On the other hand, as this development decreases thermal conductance, heat density in a device is sharply increased. There is a temperature difference between chips and even in a chip [3]. In HBM2 DRAM chips, to compensate for the thermal

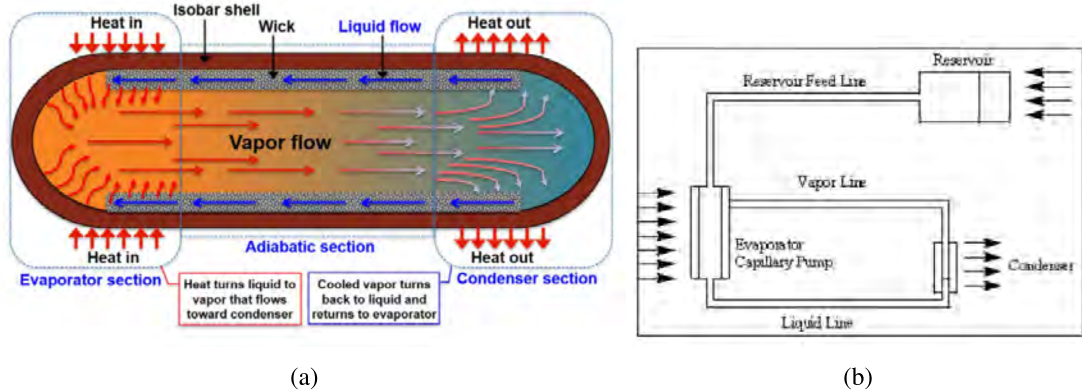
distribution, each stacked chip is divided into eight banks, and each bank has a temperature sensor. At a high-temperature bank, the refreshing rate is increased not to expire the storing data. However, such operation increases power consumption more. Sadri compared the refreshing rate under operating temperature between 2.5D DRAM chips and 3D DRAM chips [5], In 3DIC, the refresh rate is significantly higher than that of 2.5DIC because of the high thermal resistance. It causes a shorter lifetime of 3D DRAM memory chips. Besides, the maximum temperature of 3DIC is 120°C, which is exceptionally high compared to that of 2.5DIC (less than 50°C). The high-temperature areas are called a hotspot, and 3DIC has more hotspots than 2.5DIC. Tran *et al.* measured the temperature in 3DIC composed of one DRAM chip and one logic chip [6]. In the logic chip, the highest temperature in a hotspot is around 40°C higher than the other areas. Therefore, to enhance 3DIC development, cooling down chips is essential.

1.2.1 Heat pipe and vapor chambers

Cooling LSI circuits is performed by transporting heat from hot area in a chip to cold area outside the chip. The heat transfer is conventionally realized by vast metal bulk called a heat sink having large thermal conductance. The heat sink is bonded using thermal interface material (TIM). For higher power chips, liquid cooling is also used by circulating the liquid into heat sinks using mechanical pumps. In these methods, it is quite difficult to placing such vast components directly onto a chip. Even if a large heat sink can be put on a chip, heat dissipation is not enough because the size of the chip is considerably smaller than the heat sink. Consequently, the heat sink does not work effectively. Therefore, to utilize the entire heat sink, a heat spreader is another essential component, which transports the heat from the small chips to distant cooling components. As an effective heat spreader, heat

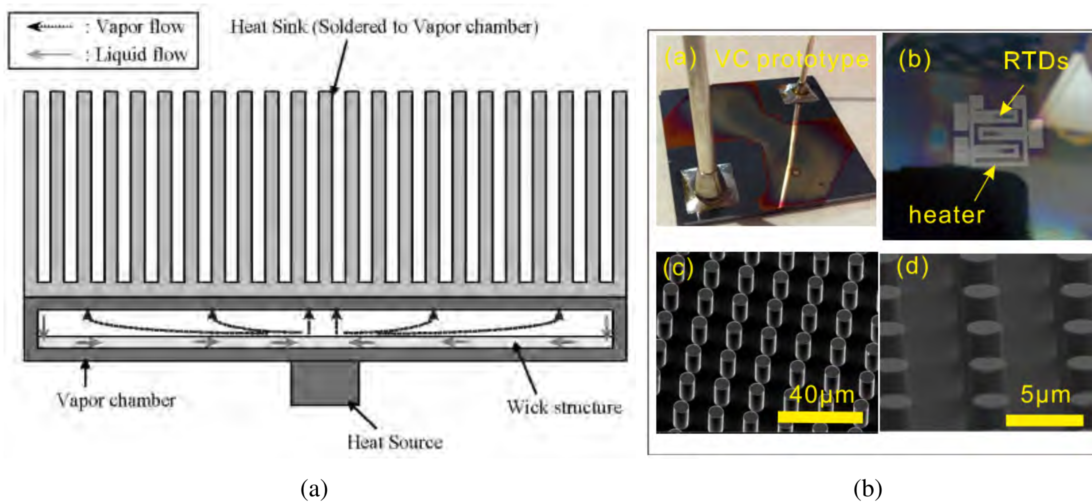
pipes are typically used [7]. A heat pipe is made from high thermal conductive materials such as copper and utilizes the phase transition to transfer the heat more effectively. In a heat pipe, working fluid such as water is sealed, and is vaporized at the high temperature. The vapor moves to the lower temperature end and is condensed into the fluid. The fluid returns to the high-temperature area along with a wick by capillary forces. In principle, a heat pipe does not require an external power supply to transfer heat. Therefore, this component is commonly used in mobile devices, and a thinning heat pipe is required. However, thinning a heat pipe causes interruption of fluid returning by the vapor fluid. Also, extending the length of a heat pipe increases the fluid resistance. In order to improve the issues, a loop heat pipe (LHP) is invented [8]. In an LHP, vapor and liquid fluids circulate along one direction, and the wick is only placed in the liquid returning area. By using this technology, Shioga realized 1 mm LHP [9]. However, the thinning LHP is still hard since LHP also utilizes the capillary forces. Besides, such a component is almost bulky copper, and it is quite challenging to integrate them with 3DIC. Although chip-level silicon LHPs such as [10] have also been studied using MEMS technology, a cooling area in a chip is so limited that it is hard to implement into 3DIC in such a device.

For obtaining a higher heat exchange rate in the chip-level cooling, a vapor chamber is also utilized. A vapor chamber is similar to a heat pipe, but thermal dissipation occurs two-dimensionally. He fabricated a 1.3 mm-thick silicon vapor chamber using micro electromechanical systems (MEMS) technology [11] shown in Fig. 1.2, and Liang fabricated a 0.75 mm-thick vapor chamber by coating copper powder to silicon micro-channels [12]. However, these devices are still thick and hard to implement between stacked chips in 3DIC since they require large volume at the chip backside.



(a) (b)

Fig. 1.1: Schematic of (a) a conventional heat pipe [7] (b) Schematic Of a looped heat pipe (LHP) [8].

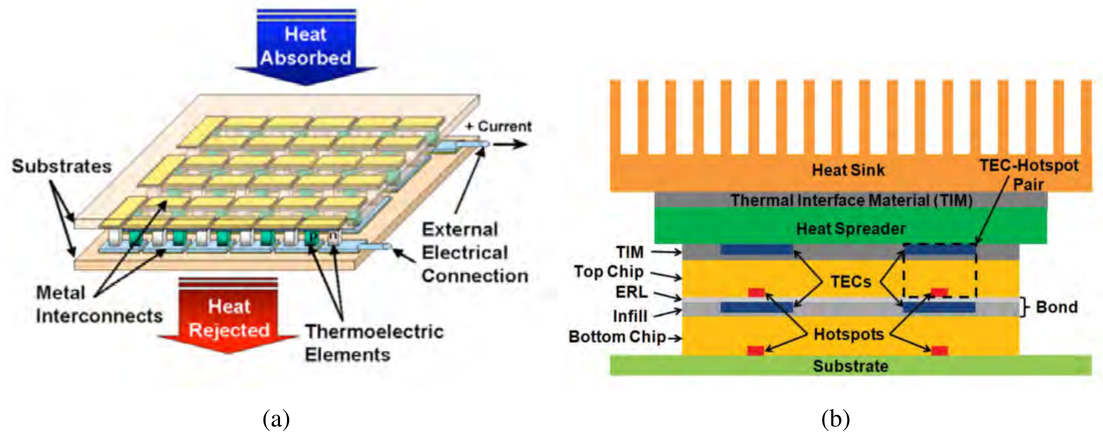


(a) (b)

Fig. 1.2: Schematic of (a) a working principle of vapor chamber [11] and (b) silicon vapor chamber bonded to a heating test chip [11].

1.2.2 Thermo-electric cooler (TEC)

Even though the heat pipes and vapor chambers can transfer heat from the top of the 3DIC, these components are not developed to integrate into 3DIC. Therefore, as the number of stacked chips increases, the thermal distribution in 3DIC is degraded more, and hotspots appear. These hotspots degrade the performance of a processor and decrease



(a)

(b)

Fig. 1.3: Schematic of (a) Schematic of commercial thermoelectric cooler using bulk materials on ceramic substrates and (b) the electronic package integrated with TEC cooler [13].

the lifetime [14].

In order to decrease the hotspots effectively, hotspot-cooling devices have been studied. Thermo-electric cooler (TEC) is considered as an effective way to cool the hotspots. TEC is composed of Peltier devices, which create a heat flux at the PN junctions. The most significant advantage of a TEC is the direction of the heat flux. As it has the vertical heat flux, TEC can dissipate the heat from hotspots to the upper floors. Besides, as TEC can be fabricated by the semiconductor technology, the compatibility to 3DICs is high. Redmod realized a TEC for hotspots in 3DIC [13]. They demonstrated a TEC could cool down hotspots in 3DICs more effectively than a bulk copper heat spreader. However, a TEC requires current larger than 8 A, and consumes massive power itself. Therefore, active cooling at junctions of the Peltier devices is required.

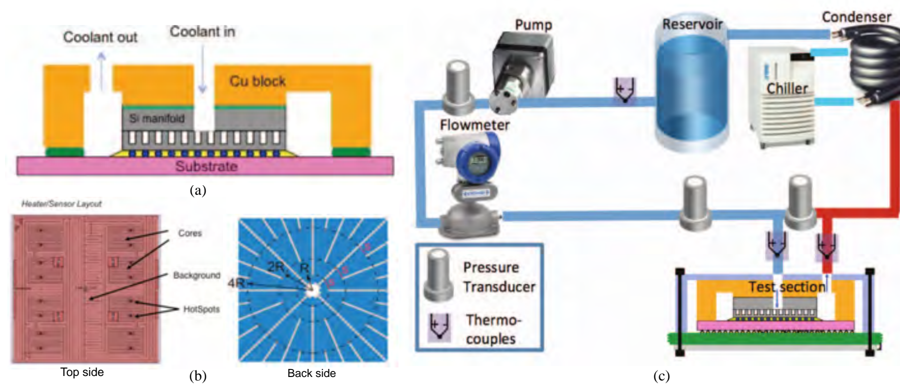


Fig. 1.4: (a) Schematic drawing of the embedded radial microchannel cooling structures for a 3D chip stack. (b) Schematic of a heating chip that simulates cores, background as well as hotspots. On the backside of the chip, radial fluidic paths are embedded [15]. (c) The system diagram of the test setup used in [15]. Blue and red lines represent the flow tubing.

1.2.3 Micro-channel cooling

Forced liquid cooling in micro-channels has also gotten attention. The micro-channels are fabricated by microfluidic technology. The original micro-channel convection demonstrated the removal of 790 W from a 1 cm^2 Si chip by Tuckeman and Pease [16]. One of the most significant advantages of the micro-channel cooling is the low volume required at the chip backside. This characteristic is different from the other cooling methods, which require large volume at the backside of cooling components. While droplet cooling devices using digital micro-channel technology known as electrowetting-on-dielectric (EWOD) can also achieve the high cooling effect [17], these devices still require sophisticated control and optimization to be applied into 3DICs. The thickness of micro-channel cooling devices can be reduced up to less than 100 μm, and these devices facilitate integration into 3DICs. Dang developed an interconnecting method of micro-channels in 3DICs using polymer fluidic vias [18]. They also developed an integration method of micro-channels at the backside of

Table 1.1: Comparison of cooling ability.

	Shioga [9]	Hale [17]	He [11]	Redmond [13]	Dang [18]	Zhang [21]	Kudo [20]
Principle	Heatpipe	Heatpipe with EWOD	Vapor chamber	TEC	Micro channel	Micro channel	Micro channel
Thermal resistance (K ·cm^2/W)	0.56	0.0175	1	↓ 9 ℃	0.48	0.269	1.6
Maximum heat flux (W/cm^2)	8.6	250	15	100	212	–	180
Thickness (mm)	1	4	1.3	0.1	0.07	0.2	0.2
Material	Cu	Si	Si	Si	Si	Si	Si
Power saving	✓✓	✓(>50 V)	✓✓	✗	✓	✓	✓(>40 V)
Stand alone	Yes	Yes	Yes	Yes	No	No	Yes
3D integrity	✗	✓	✓	✓✓	✓✓	✓✓	✓✓

heating chips [15]. They stacked the micro-channel cooling chip on a chip of test structures composed of thermometer and heaters intimating multi-core processors, and heat flux of 340 W/cm^2 is cooled down by 4°C using dielectric coolant. However, such micro-channel cooling methods require a large bulky liquid circulating system such as a pump, condenser, and chiller. These components not only occupy lots of space but also have low reliability of working, known as the bathtub curve. To decrease the size of the cooling components and failure rate, previous studies have developed closed-loop cooling devices, such as [19] and [20]. Table 1.1 shows the comparison of cooling ability. It also shows micro-channel cooling has a high potential for cooling of 3DIC.

1.3. Micropump

Microfluidic technology based on micro electromechanical systems (MEMS) technologies has garnered considerable interest for several applications during several decades [22]–[24]. This technology is used to fabricate lab-on-chip (LOC) devices and micro total analysis systems (μTAS), which can replace the bulky laboratory equipment.

For the closed-loop cooling devices, active components such as micropumps are essential. Several researchers have been developing micropumps for use in lots of applications, including cooling electronic devices. Most micropumps can be divided into two groups [25]: One group is mechanical micropumps, which has reciprocating mechanical moving structures. The principle of these micropumps employs a pump chamber encapsulated by a thin membrane (diaphragm) Oscillating movement of the diaphragm pushes the liquid in the chamber and generates a flow. These diagrams are driven by some MEMS actuators, including electrostatic [26], piezoelectric [27], thermopneumatic [28], and electromagnetic [29] actuators, as shown in Fig. 1.5a–Fig. 1.5d, respectively. As these actuators have high actuation forces, the micropumps based on these mechanical actuators generate a comparatively high flow-rate and pressure. However, the flow generated by the mechanical pumps commonly has periodic volume changes depending on the diaphragm. Moreover, an air gap is required around the micropump for the diaphragms to move. The air gap causes thermal isolation and degrades heat dissipation.

The other group of micropumps is dynamic continuous flow micropumps. Instead of mechanical actuation, these micropumps generate flow by quite different principles such as electrohydrodynamic (EHD) [30], [32]–[35], magnetohydrodynamic (MHD) [31], electroosmotic flow (EOF) [36]–[48], as shown in Fig. 1.5e, Fig. 1.5f, and Fig. 1.6, respectively. These micropumps are based on interactions between the fluid and an electromagnetic field.

EHD micropumps are based on electrostatic forces with ions in dielectric fluids. These ions are injected from electrodes by the applied large electric field. Because of the injection of ions from electrodes by electromigration, EHD micropumps require extra-high voltages. Moreover, working fluids of EHD micropumps are commonly dielectric fluids, which have

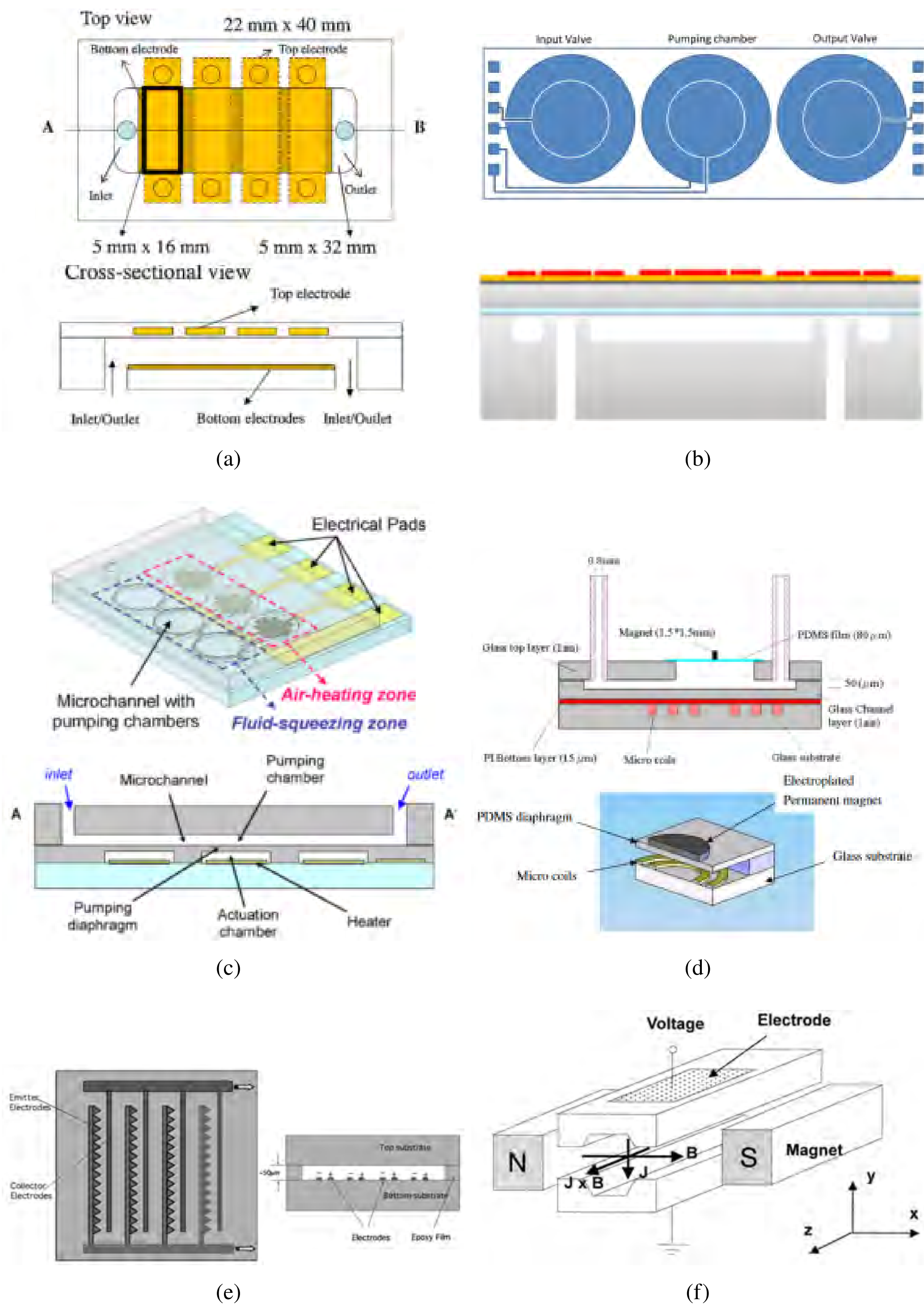


Fig. 1.5: Schematic of (a) electrostatic [26], (b) piezoelectric [27], (c) thermopneumatic [28], (d) electromagnetic [29], (e) electrohydrodynamic (EHD) [30], and (f) electroosmotic flow (EOF) micropumps [31].

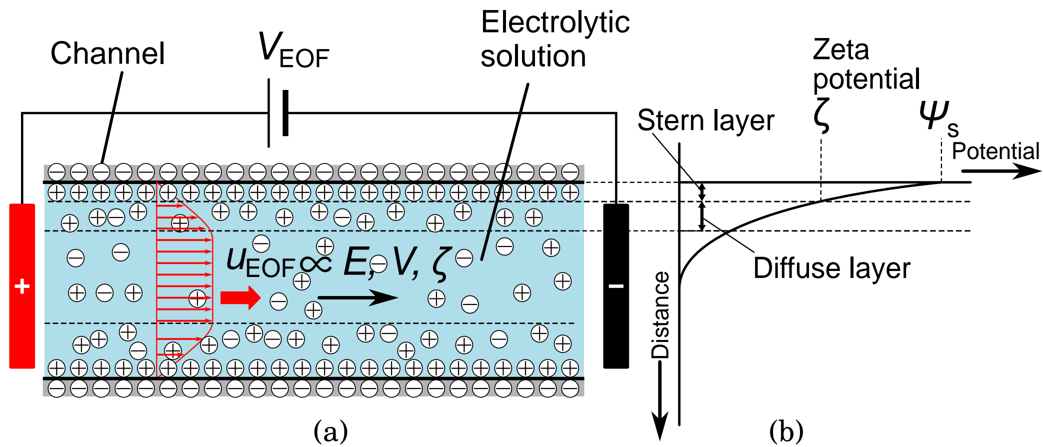


Fig. 1.6: (a) Schematic of the principle of EOF. EOF drives the movement of ions, which in turn induces the movement of the conductive fluid. The flow rate is proportional to the applied electric field and zeta potential. (b) Variation of electrostatic potential as a function of distance. ψ_s is a surface potential of a micro-channel.

lower thermal conductivity than water. Besides, EHD utilizes electromigration at electrodes to generate ions. It damages electrodes, and long-term reliability is low.

On the other hand, MHD and EOF micropumps can actuate conductive fluids. MHD micropumps are based on Lorentz force on the liquid and induce flow with low voltage. However, they require external magnets on the top and bottom sides of the micropumps. In 3DICs, such external magnets might cause undesirable noises. Therefore, MHD micropumps are not suitable for cooling micropumps.

EOF is an electrokinetic phenomenon based on a surface potential called zeta potential [37], [38]. This phenomenon is defined as the movement of the ions induced by the applied electric field, which in turn causes the movement of the conductive fluid. Due to the principle, the conductive liquid and the negative charge along the channel wall are required. Fig 1.6 shows the principle of EOF along with the variation of electrostatic potential as a function of distance. When a solid surface comes into contact with a conductive liquid, the interfacial charge on the solid surface rearranges the free ions in the liquid. The interfacial

region, along with the charged surface, is known as the electrical double layer (EDL). Zeta potential is the electrostatic potential of EDL at the boundary between the ion-immobile layer (Stern layer) and the ion-movable layer (diffuse layer). The EOF velocity (u_{EOF}) is proportional to the applied electric field and the zeta potential and can be expressed as

$$u_{\mathrm{EOF}} = -\frac{\varepsilon_{\mathrm{r}}\varepsilon_0\zeta}{\mu}E \tag{1.1}$$

where ε_{r} is the relative dielectric constant of the liquid, E is the applied electric field strength, ζ is the zeta potential of the microfluidic walls, and μ is the viscosity of the liquid. In principle, an EOF micropump is only composed of a pair of electrodes that are used to apply the electric field, and it does not require any movable mechanical structure. As EOF micropumps utilize ions induced by the surface charges, the long-term reliability is higher than EHD micropumps. Furthermore, while EHD micropumps can only use dielectric liquid, EOD micropumps can use conductive liquid, which commonly has higher heat capacity than dielectric liquid. Besides, the EOF micropumps are composed of only electrodes in a micro-channel and do not require spaces for pumping elements such as diaphragm in mechanical micropumps and magnets in MHD micropumps. Therefore, lots of researchers have studied about use of the EOF micropumps for LSI cooling [20],[47],[48].

1.4. Improving methods of EOF micropumps

In micro-channels, Raynolds number is typically low. In such hydrodynamics, the fluid velocities are proportional to the applied pressure. Therefore, the equation relating to flow rate Q and pressure difference Δp is expressed as

$$\Delta p = R_{\mathrm{hyd}}Q \tag{1.2}$$

where R_{hyd} is the hydrodynamic resistance of the micro-channels [49]. This equation is similar to Ohm's law, and Q is equivalent to the current, and Δp is equivalent to the voltage difference. However, the relationship between hydrodynamic resistance R_{hyd} and channel dimensions is not homogeneous. In rectangle channel, for instance, R_{hyd} is expressed as

$$R_{\text{hyd}} = 12\mu L\{H^3W - \frac{192}{\pi^5}H^4\sum_{m=0}^{\infty}(2m+1)^{-5}tanh[\frac{(2m+1)\pi W}{2H}]\}^{-1} \tag{1.3}$$

$$\simeq \frac{12\mu L}{H^3(W-0.6H)}$$

$$\simeq 12\mu\frac{L}{H^3W} \qquad (H << W) \tag{1.4}$$

where L is the length, W is the width, H is the height of the channel. μ is the viscosity of the fluid.

Figure 1.7 shows the equivalent circuits of an EOF micropump in a rectangle micro-channel, where $R_{\text{hyd,EOF}}$ is hydrodynamic resistance of the EOF micropump, and Δp is pressure difference between the inlet and outlet [50]. When $\Delta p = 0$, the flow rate Q_{EOF} is expressed as

$$Q_{\text{EOF}} = u_{\text{EOF}} \cdot W \cdot H. \tag{1.5}$$

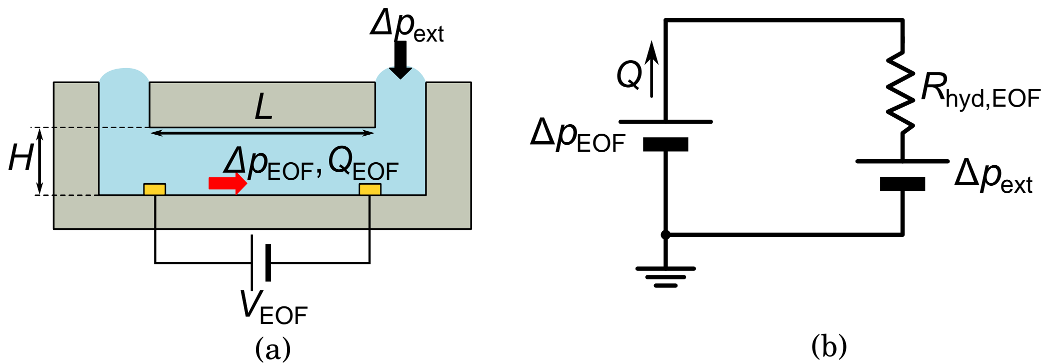


Fig. 1.7: (a) Condition of an EOF micropump and (b) Hydrodynamic equivalent circuit of the EOF micropump.

From the Eq. 1.1 and Eq. 1.4, the generated pressure difference Δp_{EOF} is expressed as

$$\Delta p_{\mathrm{EOF}} = \frac{\varepsilon_{\mathrm{r}}\varepsilon_0 \zeta V_{\mathrm{EOF}} W H}{\mu} \cdot \frac{12\mu}{H^3 W} \tag{1.6}$$

$$= \frac{12\epsilon\zeta V_{\mathrm{EOF}}}{H^2} = \frac{12\epsilon\zeta E_a L}{H^2}. \tag{1.7}$$

Therefore, from Fig. 1.7 and Eq. 1.1 and 1.7, there are three methods to increase both flow rate Q_{EOF} and the generated pressure difference Δp_{EOF}; One method is connecting micropumps in series, and the other method is increasing the applied voltage V_{EOF}.

The first method is previously studied by Takamura *et al.* [51]. They demonstrated a series-connected EOF micropump generating 25 kPa by applying a low voltage of 16 V. However, these series-connecting methods must generate indirection EOF flow, as shown in Fig. 1.8. Moreover, the loss of applied voltage to the liquid caused by chemical reactions is relatively large compared to the applied voltages. Therefore, the series-connection of low voltage EOF micropumps is not enough to obtain a high flow rate.

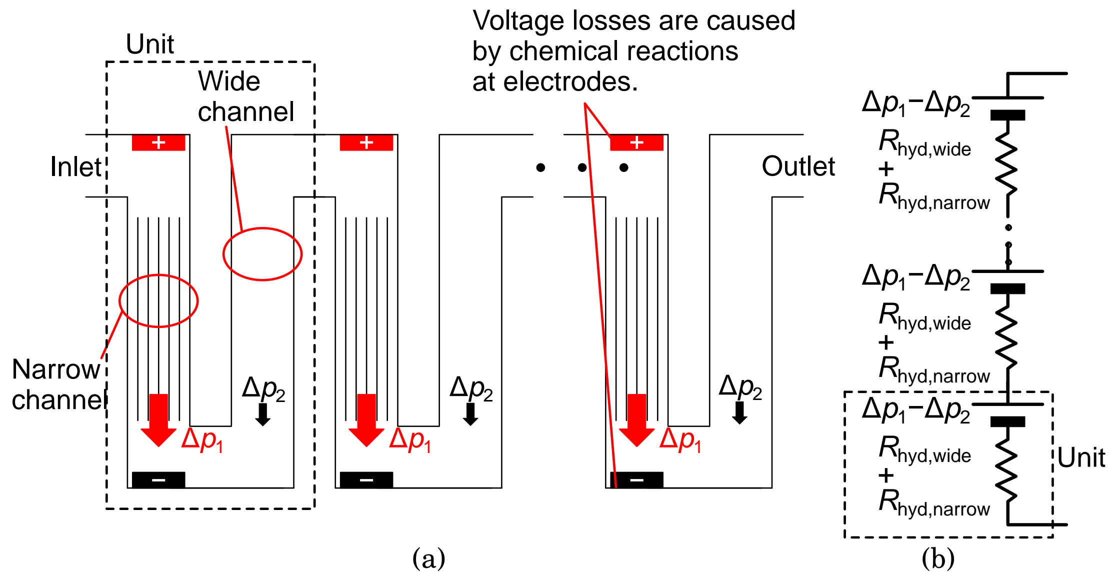


Fig. 1.8: (a) Series-connected EOF micropump proposed by Takamura [51] and (b) hydrodynamic equivalent circuit of the EOF micropump.

On the other hand, increasing applied voltages is a straightforward method. It can increase the flow rate with a simple structure of an EOF micropump. Therefore, high voltages are commonly applied to EOF micropumps. Compared to mechanical micropumps, which conventionally require at most 200 V, dynamic continuous micropumps require higher voltages than 200 V (in some cases over 800 V). Due to the high voltages, micropumps are typically driven by another external high-voltage power supply. The requirement of high-voltage power supply has prevented the integration of micropumps into 3DICs since these high voltages are higher than maximum voltages of commonly-used TSVs.

The last method to increase the performance of EOF micropumps is improving the zeta potential, which is changed by the solid surface and solution state. However, as the conventional method cannot measure the surface charge without breaking the fabricated device, the real zeta potential has not been measured. Due to the issue, although there are previous studies that demonstrated the electrical control of the zeta potential to change the EOF direction [52], [53], they did not measure the zeta potential.

1.5. Scope of This Dissertation

The objective of this research is to develop a cooling device having an on-chip micropump with the following features: (i) high flow rate and long-term reliability; (ii) integrated on-chip high voltage generator to drive the micropump; (iii) single low-voltage power supply; (iv) CMOS compatibility, especially for 3DICs using a commercial foundry CMOS process. This dissertation effort encompasses the design, fabrication, and experimental studies of the integrated cooling device.

To increase the flow rate of the EOF micropump, we focus on increasing the applied voltage and surface investigation of micro-channels. The proposed integrated device is

composed of a high-voltage generator and an EOF micropump, as shown in Fig. 1.9. Firstly, the high-voltage circuit using standard CMOS transistors and MEMS post-process has been developed to demonstrate our method for increasing maximum voltages of transistors, which can help to design high-voltage circuits using the same technology. The technology employs a standard CMOS process on a silicon-on-insulator (SOI) wafer and a MEMS post-process that isolates a transistor from each other. The MEMS post-process has been investigated using test structures, which also can be used to optimize a dry-release process of MEMS structures. Then, the novel zeta potential measurement sensor is developed for the surface investigation. Finally, the flow rate and cooling performance of the device were investigated, and future development is discussed.

1.6. Novelty and Influence

The novelties of this dissertation are summarized below: (i) A high voltage generator using standard CMOS technology and MEMS post-process is proposed; (ii) on-chip

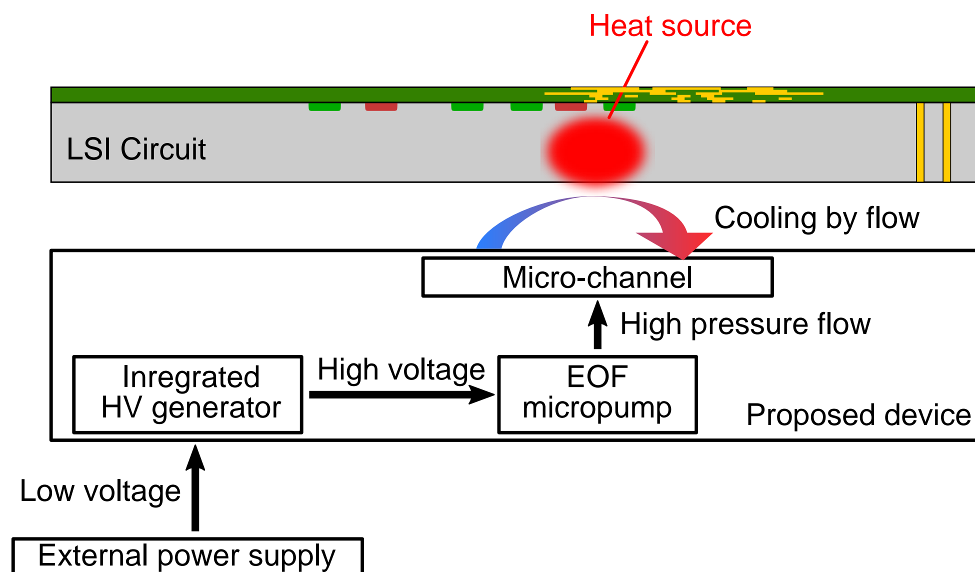


Fig. 1.9: Schematic of the proposed integrated cooling device. By using the integrated high-voltage generator, EOF micropump can be driven effectively.

integration of an EOF micropump with the high voltage generator is proposed. (iii) non-invasive zeta potential measurement method is proposed; (iv) cooling performance of an integrate EOF micropump is investigated using CMOS technology.

The influences of this dissertation are mainly on microfluidic technology and LSI-cooling technology. The proposed integration of the high-voltage generator enables us to use microfluidic devices only using a low-voltage power supply. This advantage leads to reduce the device size and accelerate the development of portable active microfluidic chips having microfluidic actuators such as micropumps. In LSI cooling, the integration of a high-voltage generator is a large impact since it enables us to integrate micropumps in cooling micro-channels. Besides, the detailed investigation of the cooling performance of an on-chip integrated EOF micropump and lead us to develop thinner cooling devices. It allows us to embed the cooling devices where we cannot integrate them, such as in 3DICs.

1.7. Thesis Organization

This dissertation is organized into seven chapters, as illustrated in Fig. 1.10. The outline of the chapters is given below.

In Chapter 1, the background and motivation for this work are provided along with a review of prior cooling devices of LSI circuits and micropumps. In Chapter 2, an overview of MEMS post-process for the high-voltage transistors is discussed, and also test structures to investigate the MEMS post-process is presented. In Chapter 3, a 30-V high-voltage switch is presented to demonstrate the use of the post-processed high-voltage transistors. And then, a high-voltage generator using the post-processed high-voltage transistors is presented, and the characteristic of the circuit is investigated. In Chapter 4, the author has discussed design, fabrication, analysis of the on-chip integrated EOF micropump. In

Chapter 5, a zeta potential measurement sensor is discussed to predict the performance of an EOF micropump. In Chapter 6, the cooling efficiency of the proposed device and higher flow rate device is investigated, and then the future development is discussed. In Chapter 7, the conclusions that can be drawn from the dissertation work are presented along with the author's contributions and thoughts on future research directions.

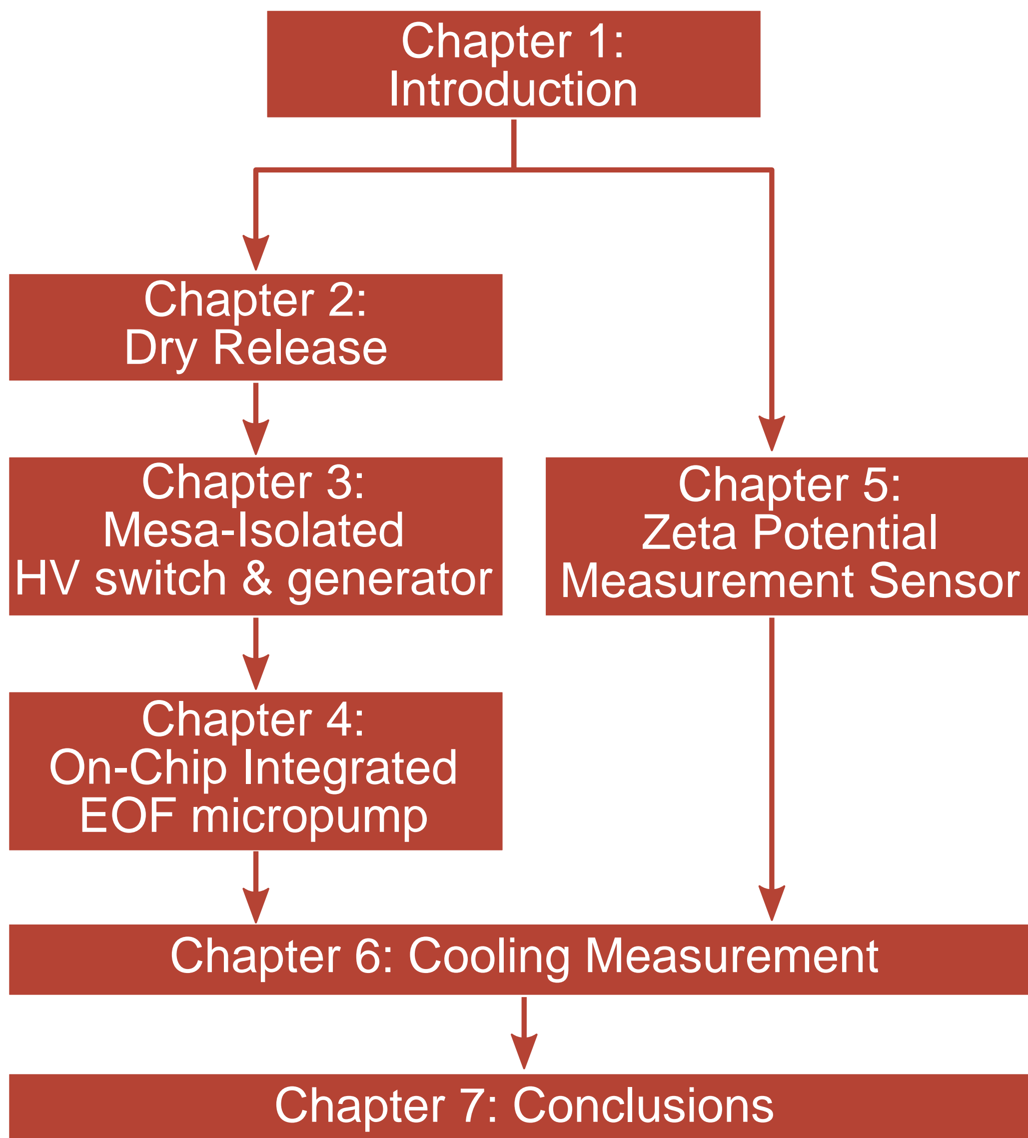


Fig. 1.10: The outline of this dissertation.

CHAPTER 2

Process Investigation of Post-Processed DTI

Some of the text and the materials of this chapter are based on the articles of the author's group entitled "A Review on Increasing of Breakdown Voltage of Standard CMOS LSI Circuits by MEMS Post-Process" published in IEEJ Transactions on Sensors and Micromachines, Vol. 138, Issue 7, pp. 319–326, 2018, and "Test Structures for End-Point Visualization of All-Plasma Dry Release of Deep-RIE MEMS Devices and Application to Release Process Modal Analysis" published in IEEE Transactions on Semiconductor Manufacturing, Vol. 30, Issue 3, pp. 201-208, 2017.

2.1. High Voltage CMOS Technologies

The microfluidic technology has been mainly developed to fabricate lab-on-chip (LOC) devices and micro total analysis systems (μTAS), which can replace the bulky laboratory equipment. Further, these miniaturized platforms facilitate the analysis with a small amount of reagent, while saving the measurement time as well. Due to these advantages, the microfluidic devices are now commonly used in chemical [54] and biological analysis [55]–[57].

The heterogeneous integration of microfabricated components in microfluidic devices

has been implemented to develop more complex LOC devices for point-of-care (POC) testing. This integration not only miniaturizes essential equipment such as pumps, valves, and huge microscopes but also provides new functionality in LOC, such as resistive flow sensors [58], [59], and droplet manipulation [60] using microelectrodes. Notably, the integration of complementary-metal-oxide-semiconductor (CMOS) large-scale-integrated (LSI) circuits has enabled several novel and informative functions in LOC devices. For example, LOC chips fabricated by the CMOS technology can themselves transfer and manage the detected data using processors and wireless communication circuits [61]. Besides, integrated electronic sensors fabricated by this technology enable LOC devices to analyze and monitor the reagent. For instance, CMOS image sensors [62] and single-photon avalanche diodes (SPAD) have been integrated to realize fast flow cytometry [63] and fluorescence imaging [64] for monitoring fluid particles in fluid without a large microscope. Moreover, CMOS technology, which is based on the principle of transistors, enables microfluidic devices to analyze the reagent by optical detectors as well as electrical and mechanical detectors such as pH sensors known as ion-sensitive FETs (ISFETs) [65] and integrated flow meter [66]. Therefore, CMOS LSI circuits play a significant role in LOC devices.

CMOS LSI technology has been used to develop microactuators as well. The actuators can be fabricated on ready-made CMOS LSI wafers by post-processing, and the integration facilitates the implementation of more complicated functions in LOC devices [67]. Among microfluidic actuators, micropumps are one of the essential active components in µTAS, which have been developed by CMOS integration. Mainly, electroosmotic flow (EOF) micropumps are widely used in many applications [38], [68] ranging from µTAS systems [43] to cooling of integrated circuits [47], [48] because of their simple structure.

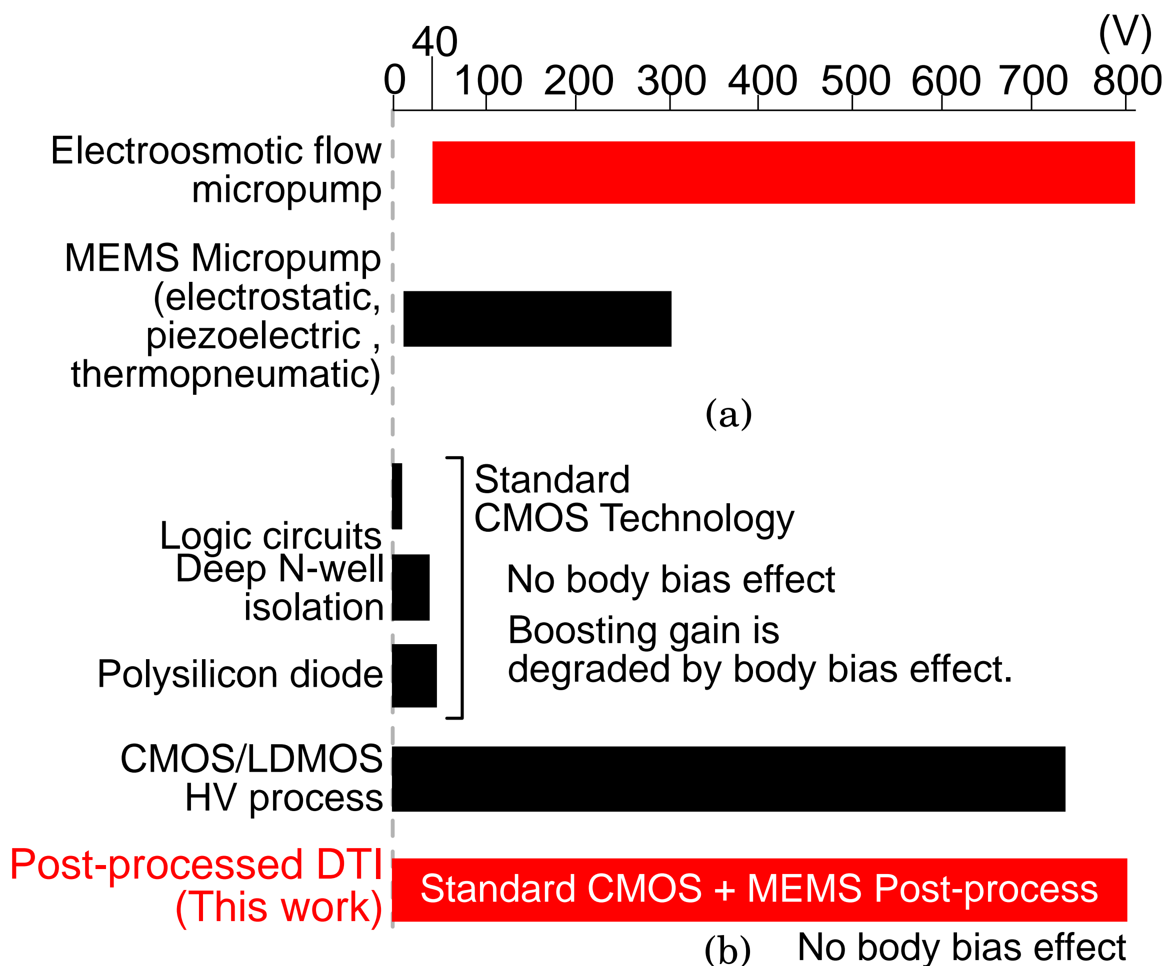


Fig. 2.1: (a) Operation voltages of MEMS and microfluidic actuators. (b) Comparison between the existing CMOS technologies accessible through foundry companies and this work.

However, the driving circuits of EOF micropumps have not been integrated or miniaturized yet. This issue is mainly due to the large difference between the maximum voltage of standard CMOS circuits and the voltage needed to drive EOF micropumps. While EOF micropumps typically require voltages higher than 40 V up to several 100 V to obtain enough flow rate, the supply voltage of standard CMOS LSI circuits is 5 V, as shown in Fig. 2.1.

Figure 2.2 shows the cross-sectional view of a typical N-channel MOSFET on P-substrate

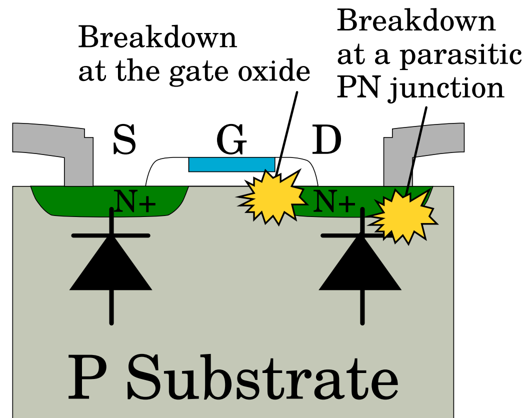


Fig. 2.2: Cross-sectional view of a standard MOSFET. When a high-voltage is applied, breakdown occurs at the gate oxide and the PN junction between N-diff and P-substrate.

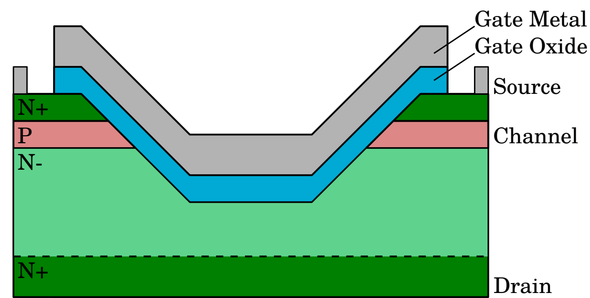


Fig. 2.3: Cross-sectional view of a DMOS transistor. The drain terminal is placed at the back-gate.

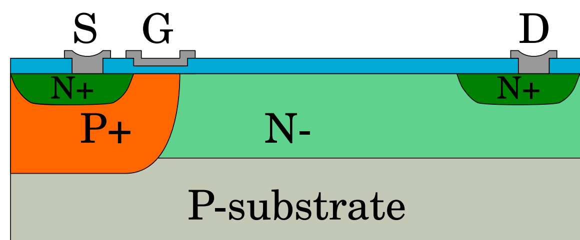


Fig. 2.4: Cross-sectional view of an LDMOS transistor. As an original DMOS is a vertical structure to reduce the electric field intensity, the channel of LDMOS was extended in planar. Also, all layers are compatible with the standard CMOS process.

fabricated by standard CMOS technology. The source and drain terminals are formed by N-type doping into the P-substrate. Between the source (or drain) terminal and P-substrate, a PN junction is formed, which sustains the reverse bias voltage. The maximum voltage of MOSFETs is typically determined by the breakdown of the PN junction diode. When the bias voltage is large, the depletion layer extends and reaches the source terminal from the drain terminal. After that, the bias voltage is only applied to the depletion layer. Finally, the breakdown occurs at the drain terminal. At the same time, when the bias voltage is considerably higher than the gate-source voltage (V_{gs}), the breakdown of the gate insulator occurs. Therefore, to sustain high voltages, preventing these breakdown is essential.

One method to realize high-voltage MOSFETs is increasing the breakdown voltages. These MOSFETs are called diffused MOS (DMOS) (Fig. 2.3) and lateral DMOS (LDMOS) (Fig. 2.4) and widely used in industrial HV CMOS technologies [69]–[71]. DMOS was firstly invented; an additional lightly N-type doped layer (N-layer) was introduced. In DMOS, the lightly doped N-layer and long gate length moderate the electric field to prevent breakdown, and V_{DD} can be increased. As current passes the lightly doped N-layer to the drain terminal, these diffused MOS transistors can be expressed as the MOSFET and resistance connected to the drain terminal. LDMOS also has the lightly doped N-layer to moderate the electric field. However, while DMOS has a vertical structure, LDMOS is a planar structure. Besides, as all layers can be fabricated by the standard CMOS technology, LDMOS transistors are now widely used in commercial HV CMOS technology in a foundry. However, although these devices can hold HV, the typical threshold voltages (V_{th}) of these HV CMOS transistors are substantially larger than those of standard CMOS transistors. Large V_{th} causes switching loss in switching circuits and degrades voltage increment in HV booster, such as charge pumps. Moreover, the fabrication cost of these transistors is

considerably higher than standard CMOS transistors.

Another method to hold HV is improving isolation methods between transistors. In this method, instead of increasing the breakdown voltages of transistors, high voltages are divided into small voltages less than breakdown voltages by connecting transistors in a series. The breakdown of PN-junctions between the doped terminals and substrate is also inhibited by changing body bias voltages of transistors. However, this method cannot be performed using standard CMOS technology. Figure 2.5a is series-connected typical N-channel MOSFETs fabricated by standard CMOS technology. As the substrate of transistors is common as GND, a breakdown between the substrate and the drain terminal occurs. Figure 2.5b shows the series-connected MOSFETs isolated by triple-well isolation (deep N-well isolation). This method isolates the transistors by the reverse biased diodes between P-substrate and deep N-well layers ($D_{DNW\backslash Psub}$). However, the maximum voltage of the deep N-well isolation in standard CMOS technology is less than 40 V. Moreover, even diodes for isolating HV transistor areas from standard low voltages transistors in HV CMOS technologies have around 300 V. To hold higher voltages, physical isolation between transistors called deep-trench-isolation (DTI) is proposed, as shown in Fig. 2.5c. This technology utilizes a silicon-on-insulator (SOI) wafer, and trenches formed deep reactive ion etching (DRIE). A transistor is isolated from each other by trenches and a buried-oxide (BOX) layer of an SOI wafer. This isolation can hold higher voltages than deep N-well isolation. However, as a trench-forming process of conventional DTI is performed before forming transistors, DTI increases some complicated fabrication steps such as embedding the trenches by isolating materials, and surface planarization by chemical mechanical polishing (CMP). Consequently, the fabrication cost to introduce conventional DTI is still high.

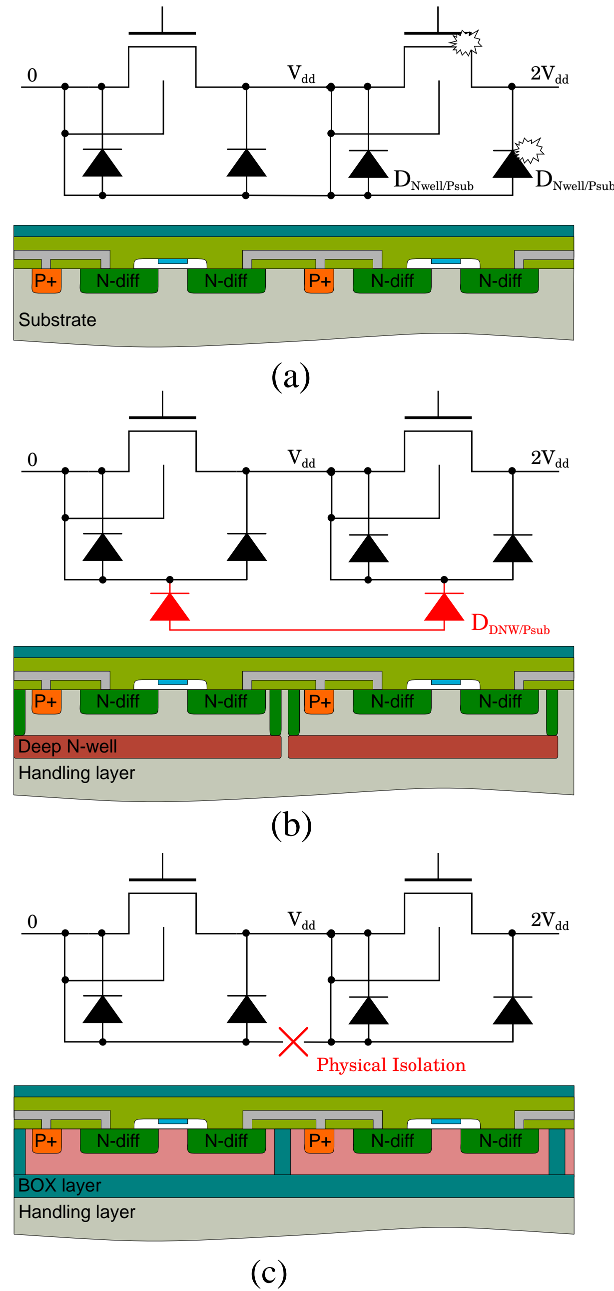
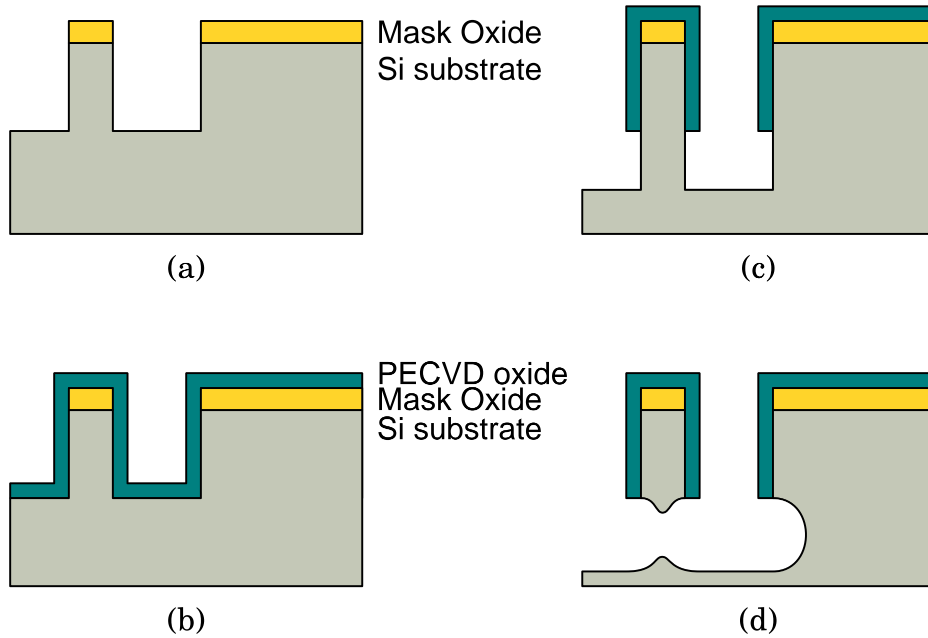


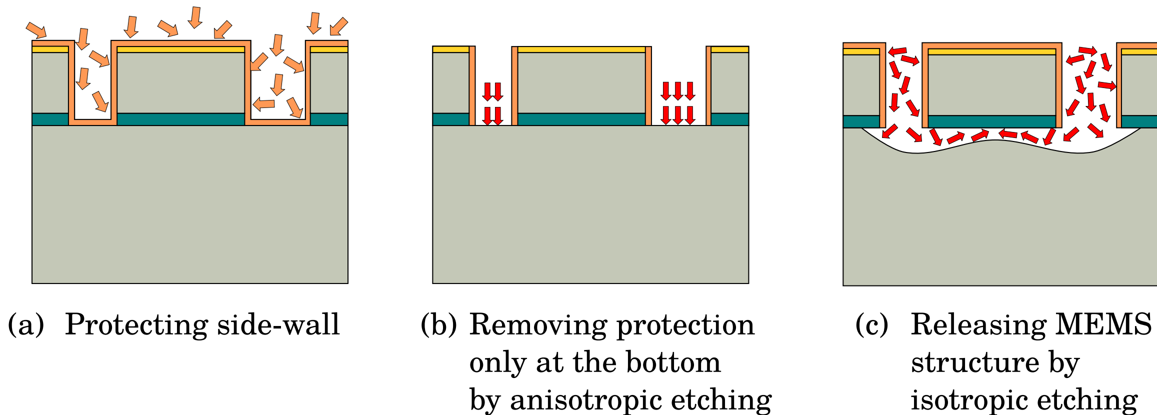
Fig. 2.5: (a) Series-connected standard NMOS transistors. Breakdown layers are compatible with the standard CMOS process. occurs between parasitic diodes between N-well and P-substrate ($D_{Nwell/Psub}$) when a large voltage is applied. (b) Series-connected deep N-well isolated transistors. Each transistor is electrically isolated by diodes between deep N-well and P-substrate ($D_{DNW/Psub}$). This method can sustain around 30 V ($10V_{DD}$). (c) Series-connected deep-trench-isolated transistors. Each transistor is physically isolated. This isolation can sustain a voltage greater than the breakdown voltage (> 700 V).



(a) (c)

(b) (d)

Fig. 2.6: Process flow of the original SCREAM process. (a) DRIE of Si substrate and forming MEMS structures. (b) Depositing surface-protecting oxide layer using PECVD. (c) Removing the bottom oxide layer and then DRIE. (d) SF_6 isotropic etching to release movable structures.



(a) Protecting side-wall (b) Removing protection only at the bottom by anisotropic etching (c) Releasing MEMS structure by isotropic etching

Fig. 2.7: Principle of the single-mask dry-release process of SOI MEMS by plasma etching [72].

To reduce the fabrication cost and steps, we have developed post-processed DTI (also called as mesa isolation). Post-processed DTI can be performed after the fabrication of CMOS transistors on an SOI wafer. One of the significant advantages of the post-processed DTI is that CMOS components are fabricated by standard CMOS technology at a commercial foundry without changing any processes. Owing to the low cost of the CMOS fabrication, fabrication cost of post-processed DTI can be suppressed, though this method requires an SOI wafer that is more expensive than a bulk silicon wafer. This method has been developed from a MEMS dry-releasing method called single-crystal-silicon reactive etching and metalization (SCREAM) proposed by Shaw [73].

SCREAM process is commonly known as a CMOS-compatible MEMS-forming method without using damaging processes to CMOS components. This method can remove the remaining silicon under the structures by isotropic etching. Typically, for releasing MEMS structures, a so-called sacrificial layer under the movable structure is used [74]. Selective removal of the sacrificial layer releases the movable structure from the substrate. Several variants have been proposed so far, depending on the structural materials, sacrificial materials, etchant, etching phase (liquid or gas), drying (anti-sticking) method, and etching process (from one side or both sides). The simplest and most widely method for the liquid-phase release of silicon structure employs silicon dioxide (SiO_2) as a sacrificial layer and hydrofluoric acid (HF) solution as a release etchant. The most severe problem with the method is sticking: the structure occasionally sticks to the substrate owing to the meniscus force of the rinsing liquids. The rinsing procedure is finished with low-surface-tension liquids to solve the sticking problem, such as by replacing HF by isopropanol, sometimes in combination with the liquid replacement of other phases, such as a freeze-drying technique based on sublimation [75] or a supercritical drying method using carbon dioxide [76].

An alternative is to perform gas-phase releasing, such as SiO_2 etching using vapor-phase HF [77], [78]. Plasma in reactive ion etching (RIE) apparatus can also be used as a release etchant. A digital micromirror device (DMD) commonly uses dry plasma release. Oxygen plasma is used to remove an organic sacrificial layer to release metallic structures [79]. SCREAM process utilizes the SF_6 isotropic plasma etching to release MEMS structures. Figure 2.6 shows the original SCREAM process to form released MEMS structures. First, the MEMS structures are formed by DRIE. And then, the SiO_2 layer is deposited using a chemical vapor deposition (CVD). After that, the bottom SiO_2 is removed by DRIE. Finally, isotropic etching is performed, and the movable MEMS structures are released by removing the backside silicon. All the processes are CMOS-compatible, and SCREAM enabled us to form the MEMS structures on CMOS-fabricated wafers.

To realize more reliable and CMOS-compatible processes, Morishita firstly developed the SCREAM method. [72], as shown in 2.7. They used C_4F_8 as a surface protecting layer, and SF_6 for etching silicon. For isotropic silicon etching, XeF_2 gas etching is also possible [80]. The XeF_2 etching has a high selectivity for silicon and may decrease the amount of unintended etching. However, the release method requires another process step involving extra equipment. In contrast to XeF_2 etching, C_4F_8 and SF_6 plasma species can be used for DRIE and do not require additional equipment. They firstly applied this method for releasing MEMS structures on a CMOS wafer, and then applied this method for post-processed DTI. Figure 2.8 shows the post-processed DTI by the dry releasing method. By applying the isotropic etching, this approach can separate the HV circuits fabrication into two parts: "reliable transistor fabrication in a foundry" and "adding new functionality in a university cleanroom," as shown in Fig. 2.9. This separation increases the reliability and functionality of standard transistors. Hirakawa demonstrated that series post-processed

Fig. 2.8: Principle of post-processed DTI.

DTI transistors could hold 800 V [81]. Table 2.1 shows HV CMOS methods. It is evident here that the post-processed DTI is an effective method to hold HV using CMOS transistors.

However, to realize the post-processed DTI, the isotropic etching requires careful optimization. To isolate a transistor from each other completely, the remaining silicon under the LSI wiring has to be fully etched. On the other hand, if the time of the isotropic etching process is too long, the etching causes the damage of the transistor, as shown in

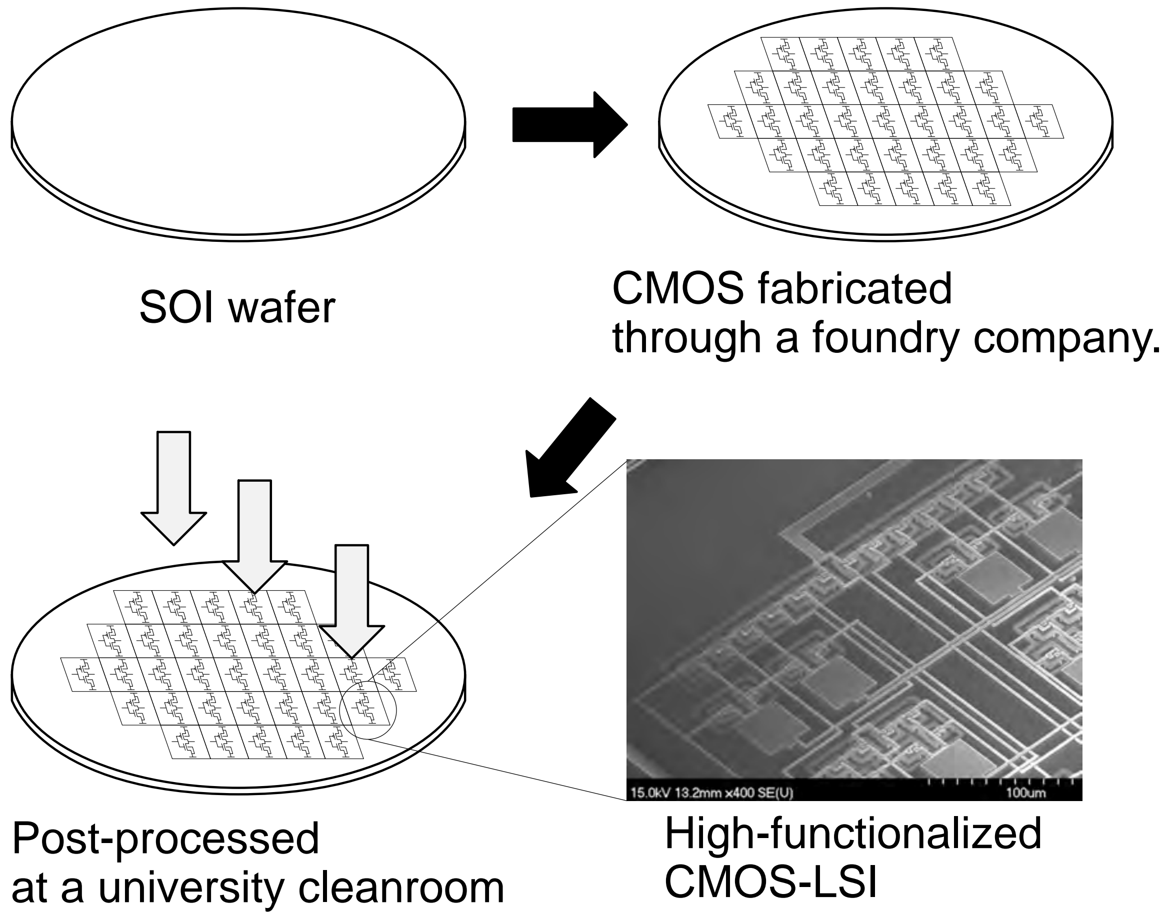


Fig. 2.9: Proposed methodology of new functionalization of reliable LSIs fabricated at an LSI foundry.

Table 2.1: Comparison of mentioned high-voltage CMOS circuits.

	Endurance Voltage (V)	Device	Isolation	Process	Cost	Accessibility
Standard CMOS	1.8-5	CMOS FET	Common substrate	Standard CMOS	Very Low	✓✓
Tarui	1000	DMOS	Deep N-well isolation	HV CMOS	High	✗
Sloan	300	LDMOS	Deep N-well isolation	HV CMOS	High	✗
Shiraki	>700	LDMOS	DTI	HV CMOS	High	✗
Hirakawa [81]	>700	CMOS FET	Post-processed DTI	Standard CMOS	Low	✓

Fig. 2.10.

The optimization of the isotropic etching is also crucial for releasing MEMS structures. In the case of MEMS releasing, a difficulty is finding the right balance between the C_4F_8 fluorocarbon protective layer thickness, the anisotropic etching time employed to remove the bottom fluorocarbon layer, and the isotropic release etching time. The release etching time is an essential parameter to be adjusted: it must be sufficiently long to release the structures entirely but must be sufficiently short so that the mask and the side-wall protective fluorocarbon layer are not etched away by the ion bombardment. Without the optimization of this parameter, the releasing process will result in severe damage to the MEMS structure, as shown in Figs. 2.11 and 2.12. The absorption at the side-wall is known as the lag effect and is more pronounced [82], [83] for the DRIE etched high-aspect-ratio microstructures (HARMS). Therefore, to use the isotropic etching for dry-releasing of MEMS structures, the damage to the protective layer by ion bombardment and the pattern dependence of the etching behavior at the bottom of the trench should be quantitatively investigated.

In both cases of the post-processed DTI and the MEMS release, the difficulty of the isotropic etching is the dependence of the undercutting speed on the size of the etching hole openings. Owing to the nature of HARMS, the undercutting process cannot be observed directly from the surface. Such investigation has been carried out destructively, i.e., by cleaving the etched wafer followed by SEM observation of the cross-sectional view, as shown in Fig. 2.13. However, as this measurement method allows us to observe the sample per sample, the sample preparation takes a long time. If such an investigation could be nondestructive, process development would be significantly accelerated. Therefore, we developed test structures that would make the process observable from the surface.

In this chapter, we subsequently discuss two topics. The first topic is a test structure that

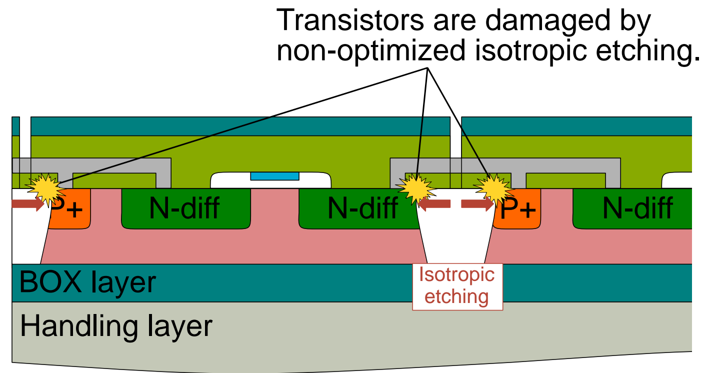


Fig. 2.10: Failure caused by too long isotropic etching in post-processed DTI. The isotropic etching reaches doped terminals and damages transistors

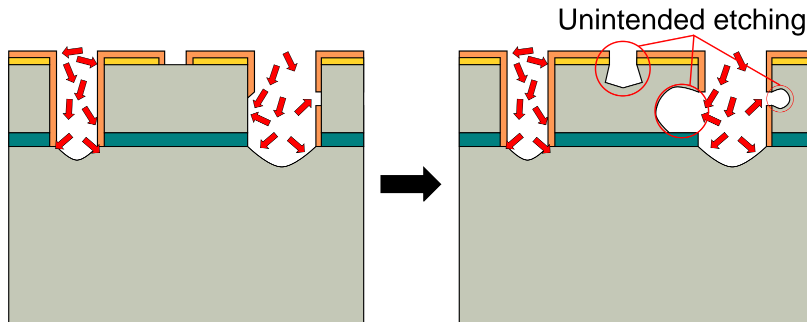


Fig. 2.11: Unintended etching occurs at some locations under unsuitable plasma conditions, adversely affecting the device performance.

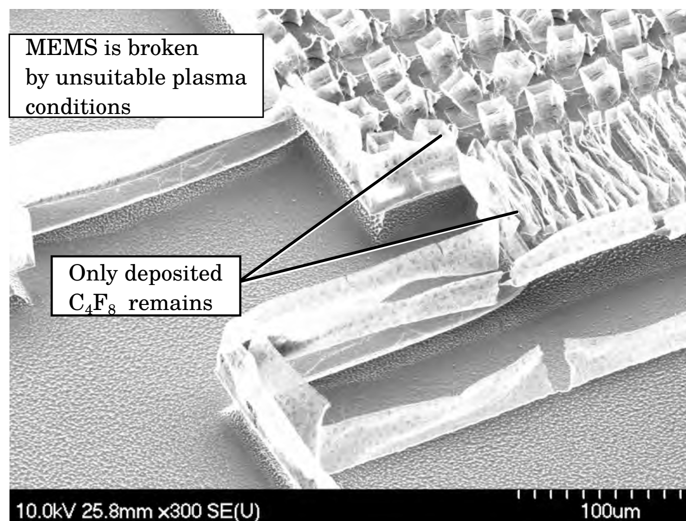


Fig. 2.12: SEM image of MEMS actuator whose silicon structure was etched entirely away during dry release owing to insufficient passivation.

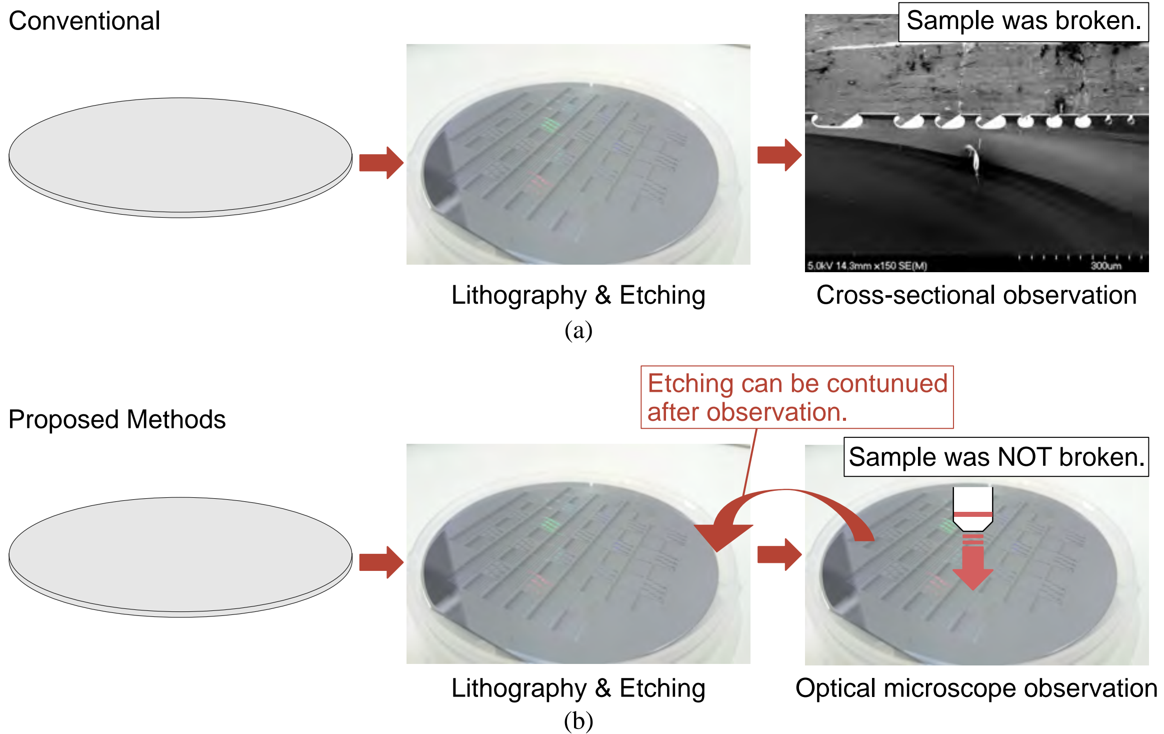


Fig. 2.13: (a) Conventional process optimization method by cross-sectional observation of samples. As the sample is broken, lithography and etching processes are required at every experiment. (b) Proposed process optimization method by optical-microscope observation. As the sample is not broken, the additional etching can be possible using the measured wafer.

can be used to visualize undercut etching at the bottom of deep-etched trenches as well as to asses the damage caused by the process only with an optical microscope. The second topic deals with etching modes. During the investigation of the bottom of the trenches, we unexpectedly found another etching mode that appeared under the specific passivation conditions. The release of structures can be achieved more rapidly as a result of a side-wall directional etching due to the condensation of the plasma. A test structure to investigate the threshold at which conventional isotropic etching changes to undercut directional etching was therefore designed, and details of the etching mode obtained by both optical microscope and scanning electron microscope (SEM) observation are presented.

2.2. Test structures for end-point visualization

2.2.1 Design of the test structures

Four types of test structures were designed to investigate the release-end-point during the optimization of process conditions using an optical microscope. Figure 2.14 shows the designs and testing parameters. The first type of test structure is a square island surrounded by a trench to extract the undercut etching rate (Fig. 2.14a). In our experiment, the thicknesses of the SOI Si device layer and SiO_2 buried oxide (BOX) layer were 9 μm and 1 μm, respectively. The designed opening width (D) was varied from 1 μm (aspect ratio of 9) to 9 μm (aspect ratio of 1) and 18 μm. The sizes of the islands (W) were 5 μm, 10 μm, and 20 μm. The second and third types of structures were the mesh and pillar patterns with various sizes of gap (Figs. 2.14b and 2.14c), respectively, used to optimize the etching rate of the movable structure for a given plasma density. Besides, to measure the undercut etching from the side, we formed a comb (interdigitated rectangle) array with no adjacent holes, small (W = 35 μm) holes, or large (W = 140 μm) holes as in figure caption (Fig. 2.14d). The total area of all the test structures was 2.7 mm × 2.7 mm.

2.2.2 Fabrication

First, a 1-μm-thick layer of aluminum was sputtered on the 9 μm-thick device layer on an SOI wafer. Then a 1-μm-thick EB resist was coated and patterned by direct EB writing. The Al layer was etched by Cl_2+ BCl_3 plasma (Fig. 2.15a). As shown in Fig. 2.15b, DRIE was performed to etch the structure using the Al layer as a mask. The BOX layer at the bottom of the Si structure was subsequently etched by CHF_3 plasma. For the protection of the side-wall during the release, a thick fluorocarbon layer was deposited using C_4F_8

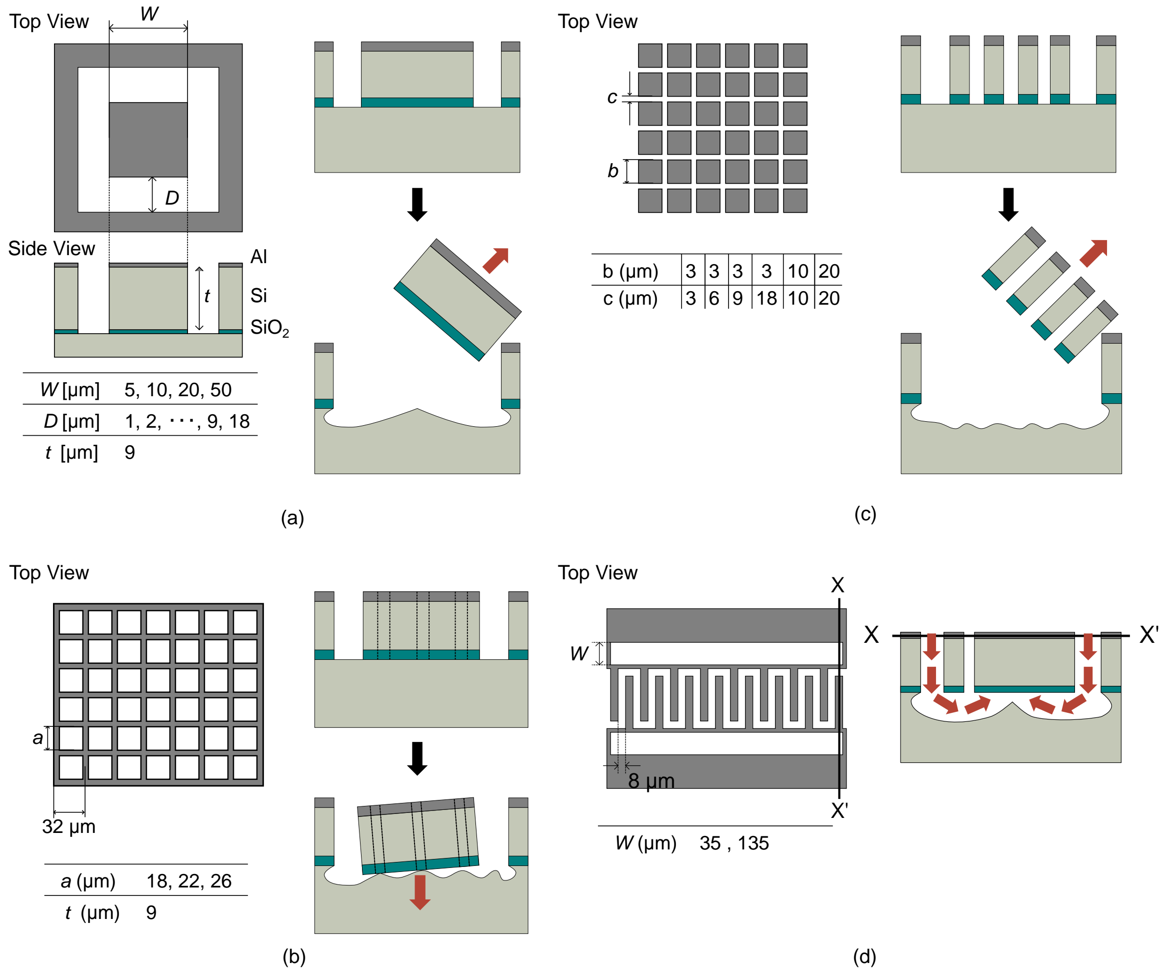


Fig. 2.14: Designs of the test structures. The purpose of the square test structures in (a) is to extract the undercut etching rate. The mesh pattern in (b) is used for damage assessment, and the pillars in (c) enable the dependence of the etching rate on the gap size and SF_6 and C_4F_8 plasma coil power to be determined. The comb array with or without holes next to the array in (d) is used to measure the undercut etching from the side.

plasma. The fluorocarbon over the BOX layer was removed by the ion bombardment of SF_6 plasma. Finally, MEMS structures were dry-released by isotropic etching by SF_6 DRIE inductively-coupled plasma (ICP). To minimize ion bombardment damage during the release step, zero bias was applied.

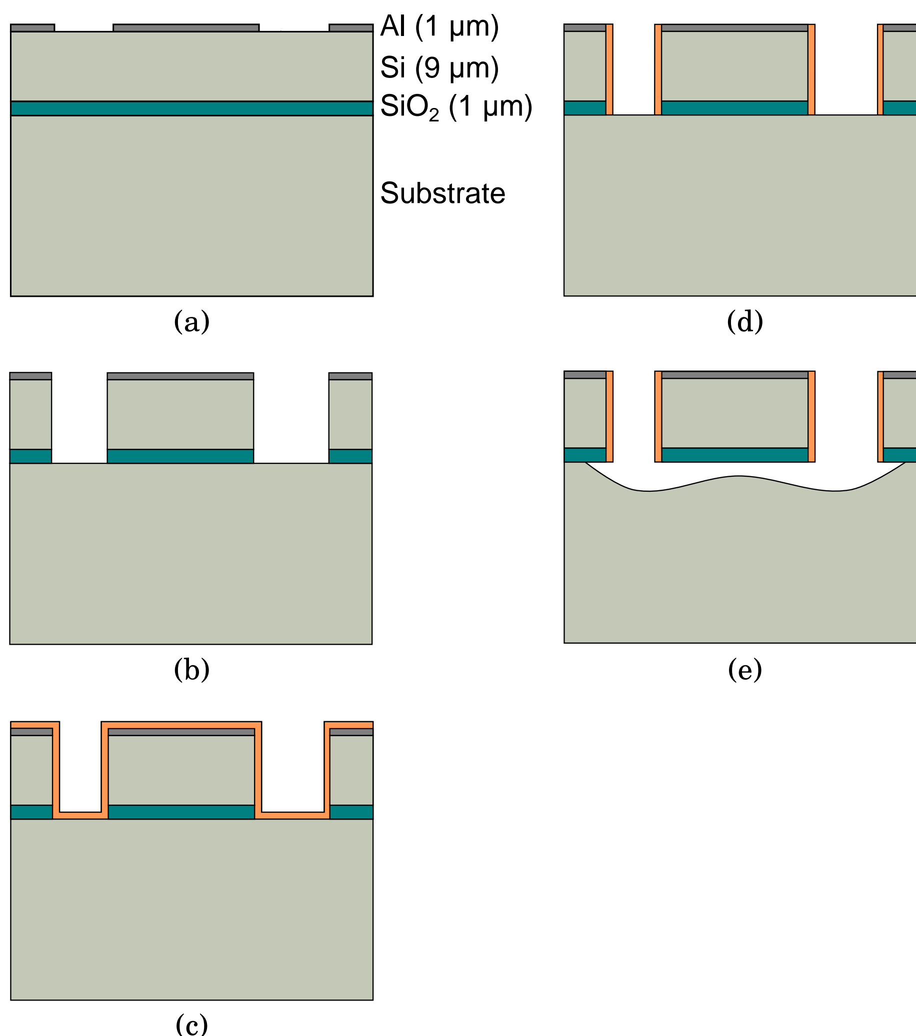


Fig. 2.15: Process flow of SOI MEMS structure fabrication by the single-mask release method. (a) Direct patterning with rapid EB writer on a thick EB resist, followed by Cl_2 plasma etching of Al mask. (b) Silicon DRIE and BOX SiO_2 etching. (c) Thick fluorocarbon deposition for side-wall protection. (d) Bottom fluorocarbon removal by SF_6 ion bombardment. (e) MEMS dry release by isotropic etching with SF_6 ICP plasma under zero substrate bias.

2.2.3 Results of dry release under two different sets of plasma conditions

The most critical parameters for a successful release are related to the plasma conditions. We investigated the ICP coil power and substrate bias as parameters under two sets of

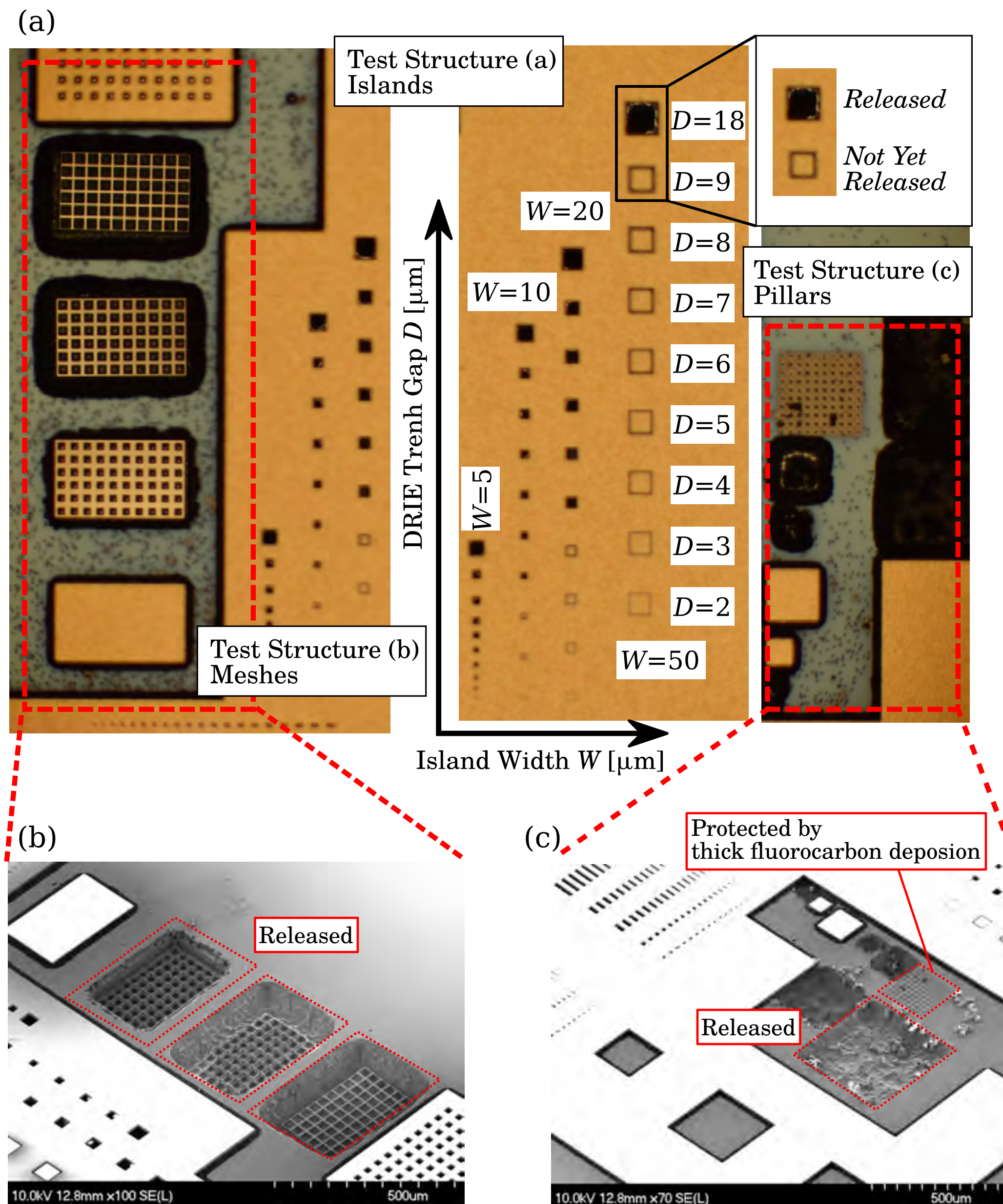


Fig. 2.16: (a) Optical microscope image of the test structure after 8.5 min of isotropic etching under condition B (Table 2.2). The etched structures are observed. (b) and (c) SEM image of the mesh structures; the mesh structures with the larger openings were etched more deeply. The result indicates that the end of the release etching of movable mesh structures. (c) SEM image of the pillar structures; fine-mesh structures were etched more deeply. The result shows the pillar array with narrow openings was etched away, while the array with large openings remained because of the thick fluorocarbon layer.

experimental conditions (Table 2.2). Under condition A, a 1800 W ICP C_4F_8 plasma with 100 W substrate bias was used for fluorocarbon deposition, a 1800 W SF_6 plasma with 100 W substrate bias was used for bottom fluorocarbon removal, and 1800 W SF_6 plasma with zero substrate bias was used for the dry release. In condition B, the ICP coil power was reduced to 600 W, but the substrate bias was maintained at 100 W for fluorocarbon removal, and an ICP power of 600 W with zero substrate bias was used for the dry release. Under condition A, the coil power in the release step was too high, and all the mesh, square, and pillar structures were either released or broken.

On the other hand, the test structures were successfully released under condition B. The larger released structures, such as the mesh structure as shown in Fig. 2.14b toppled but remained at the same location. Although some debris was released from the smaller test structures, as shown in Figs. 2.14a and 2.14c, all of it remained within the test structure area and did not affect other devices on the same wafer.

Figure 2.16 shows an optical microscope image of the test structures. The chip was etched under plasma condition B, with a fluorocarbon deposition time of 3 min, a fluorocarbon

Table 2.2: Plasma conditions used in the experiments

<table>
<tr><th></th><th></th><th>Cond. A</th><th>Cond. B</th></tr>
<tr><td rowspan="4">Fluorocarbon deposition by C_4F_8</td><td>Coil (W)</td><td>1800</td><td>1800</td></tr>
<tr><td>Bias (W)</td><td>0</td><td>0</td></tr>
<tr><td>Time (min)</td><td>3</td><td>3</td></tr>
<tr><td>Flow Rate (sccm)</td><td>150</td><td>150</td></tr>
<tr><td rowspan="4">Removing bottom fluorocarbon by SF_6</td><td>Coil (W)</td><td>1800</td><td>600</td></tr>
<tr><td>Bias (W)</td><td>100</td><td>100</td></tr>
<tr><td>Time (min)</td><td>5.5</td><td>5.5</td></tr>
<tr><td>Flow Rate (sccm)</td><td>300</td><td>300</td></tr>
<tr><td rowspan="4">Releasing by SF_6</td><td>Coil (W)</td><td>1800</td><td>600</td></tr>
<tr><td>Bias (W)</td><td>0</td><td>0</td></tr>
<tr><td>Time (min)</td><td>5.5</td><td>8.5</td></tr>
<tr><td>Flow Rate (sccm)</td><td>300</td><td>300</td></tr>
</table>

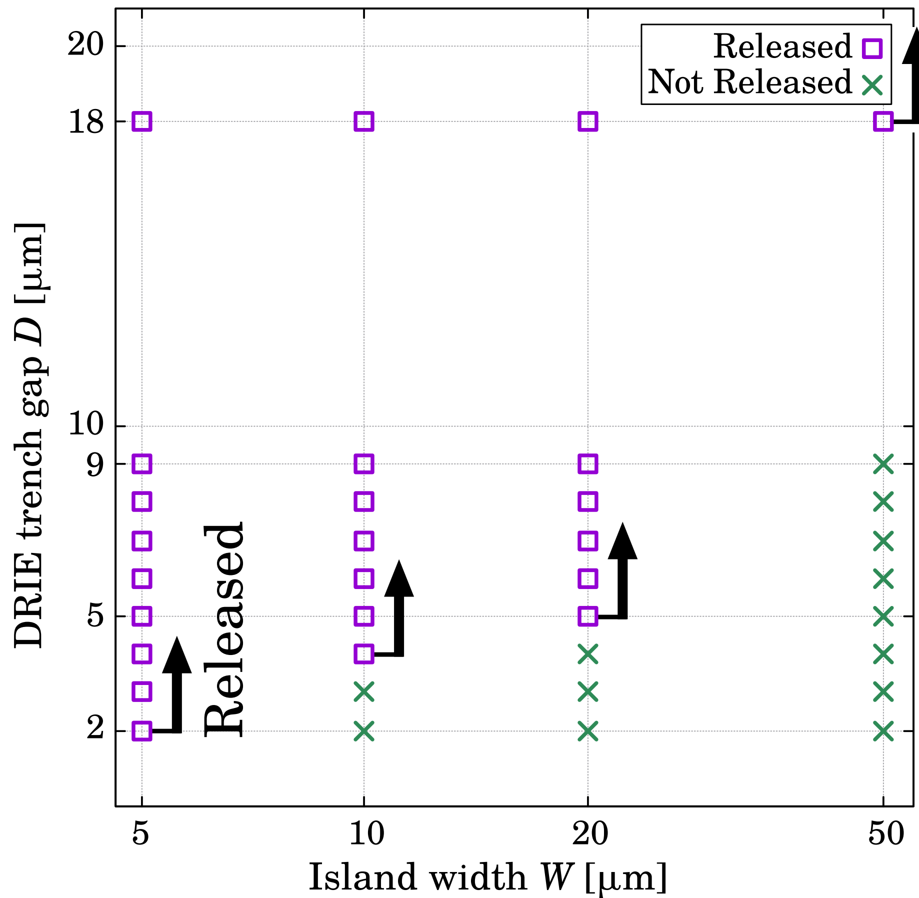


Fig. 2.17: Undercut etching dependence on the island width W and trench width D under condition B (Table 2.2). The larger the island width is, the more structures remained unreleased. Also, the narrower the trench width is, the more structure remained unreleased.

removal step time of 5.5 min, and isotropic release time of 8.5 min.

Figure 2.16a shows the released square island test structures, observed as dark squares under the optical microscope. The dependence of the structure release on the island width W and DRIE trench gap D was observed by summarizing the results, as shown in Fig. 2.17: all the structures having an island width of $W = 5$ μm were released, whereas some of the structures with a larger island width and a narrower gap were not released.

Figure 2.16b shows an SEM image of the mesh structures. Analogous to the square pattern, the full release was identified by the absence of mesh structures. It was also found

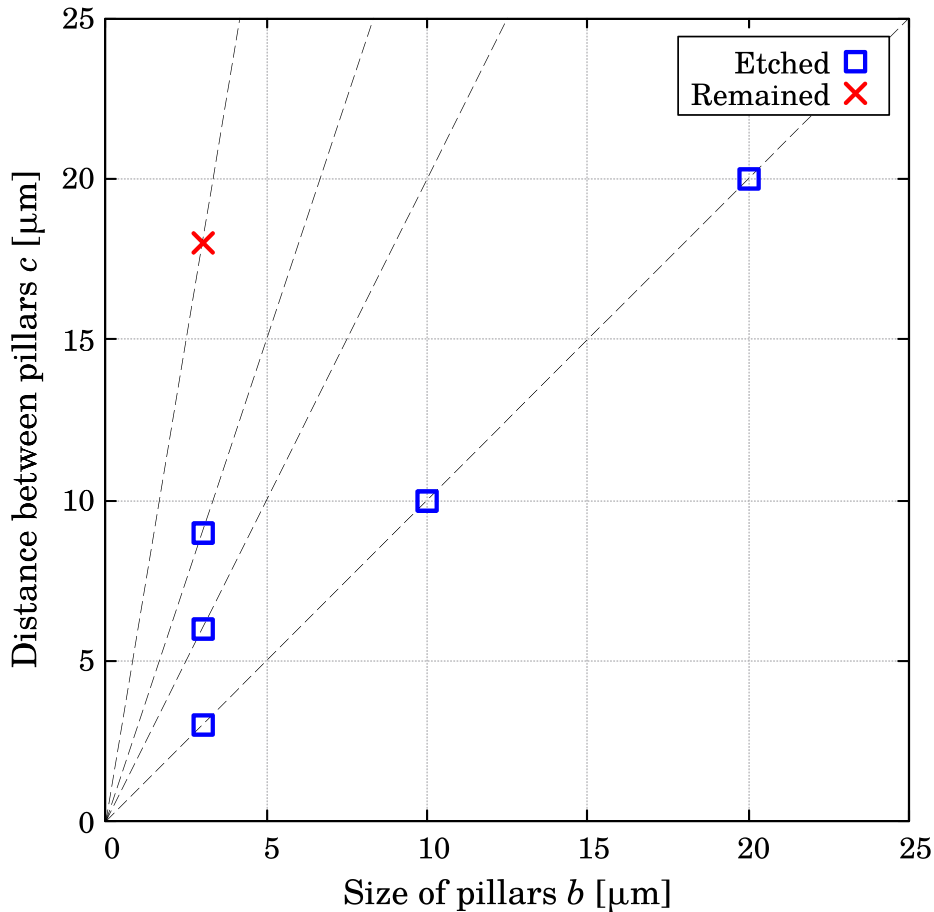


Fig. 2.18: Undercut etching dependence on the size of pillar b and the distance between pillars c under condition B (Table 2.2). As the ratio of c to b increased, the passivation layer becomes thicker, and more structures remained.

that the substrate was etched more deeply for patterns with larger mesh holes. The SEM image in Fig. 2.16c shows that the pillar structures were also completely released except in the case of a 3 µm gap. The remaining pillars were also observed with an optical microscope, as shown in Fig. 2.16a. From the summary of the pillar test structures in Fig. 2.18, the dependence of the release on the opening ratio was analyzed. Only the structures having the interval c = 18 µm remained. As the opening ratio, which is the ratio of the distance between pillars c to the size of a pillar b increased, the passivation layer became thicker and, more structures remained.

2.3. Discovery of a new dry-release mode: side-wall directional etching

2.3.1 Test structure for detection of the isotropic etching mode

In the observation of the released comb test structures, we found two types of isotropic etching modes depending on the mask opening size and plasma deposition conditions. Figure 2.19 and Fig. 2.20 show images of the two types of etching. Figure 2.19 shows the classical isotropic etching mode with plasma condition A, where the entire substrate opening is etched isotropically. For the post-processed DTI, this etching mode is suitable since the entire silicon substrate requires to be etched. Figure 2.20 shows the newly discovered etching mode under condition B: The middle of the large opening remains unetched, and only the edges of the opening are etched. The new etching mode is useful for dry-release processes since it preferentially progresses underneath the structure to be released. In other words, the etching process can be defined as an undercut directional etching mode driven by the unetched silicon island at the bottom of the opening.

As shown in Fig. 2.21, an undercut silicon island only appears for large openings. To identify the pattern dependence, other line-and-space test structures were processed and observed. Figure 2.22 shows the test structures after the DRIE process by 9 μm performed under condition B. Figure 2.23 summarizes the pattern dependence of the etching mode. The threshold at which the etching modes changes can be identified since the remaining fluorocarbon layers were observed with an optical microscope. In the case of small openings, the C_4F_8 deposition was small, and the etching occurred isotropically; on the other hand, in the case of large openings, the etching mode became the undercut directional mode.

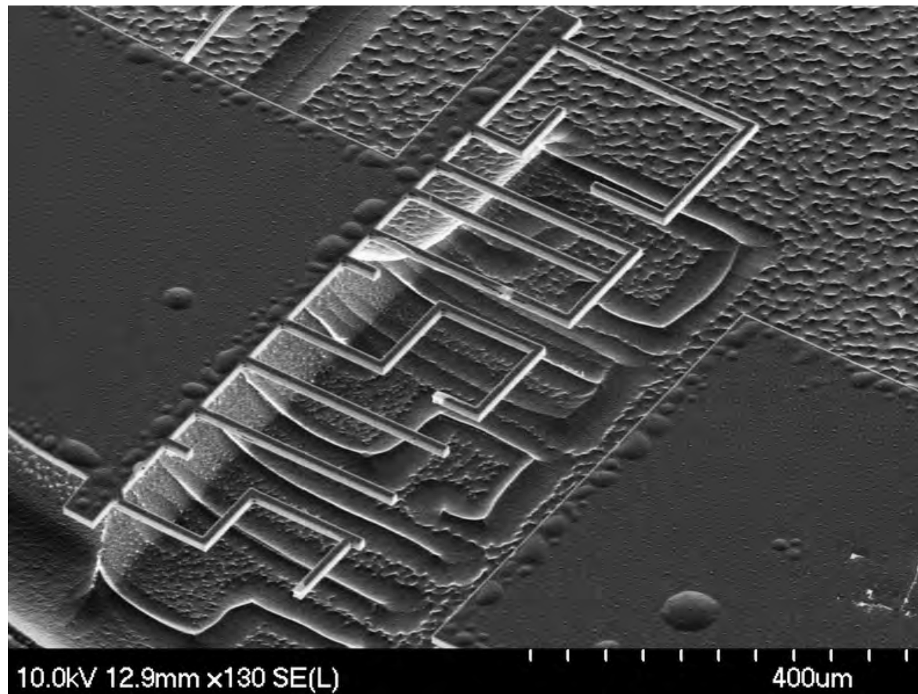


Fig. 2.19: SEM image of structures etched by SF_6 plasma under condition A, where the entire substrate opening is etched isotropically.

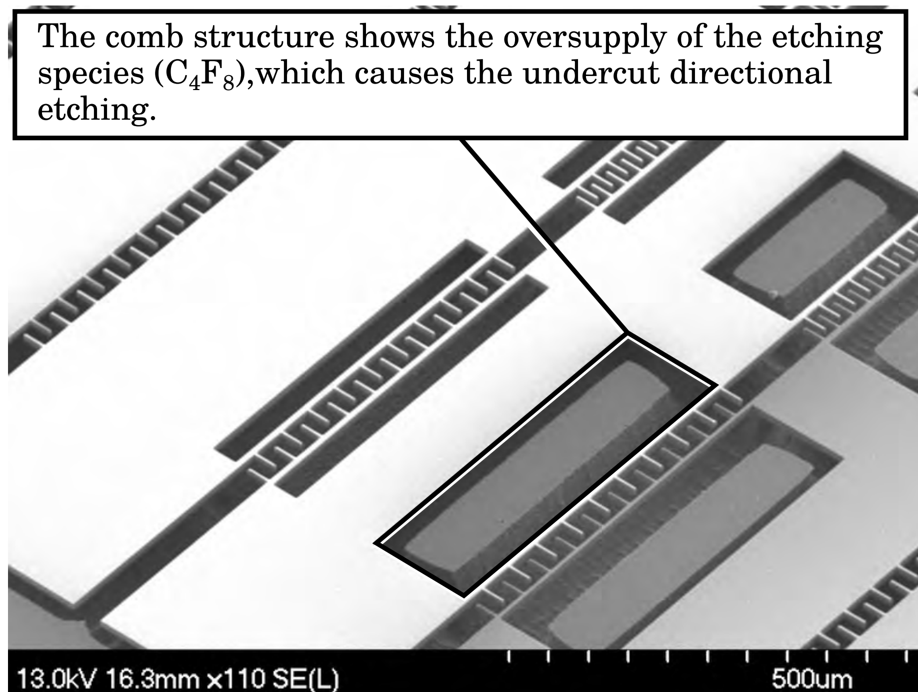


Fig. 2.20: SEM image of comb test structures shown in Fig. 2.14d etched by SF_6 plasma under condition B, where pronounced undercutting occurred, and the middle of the opening was not etched.

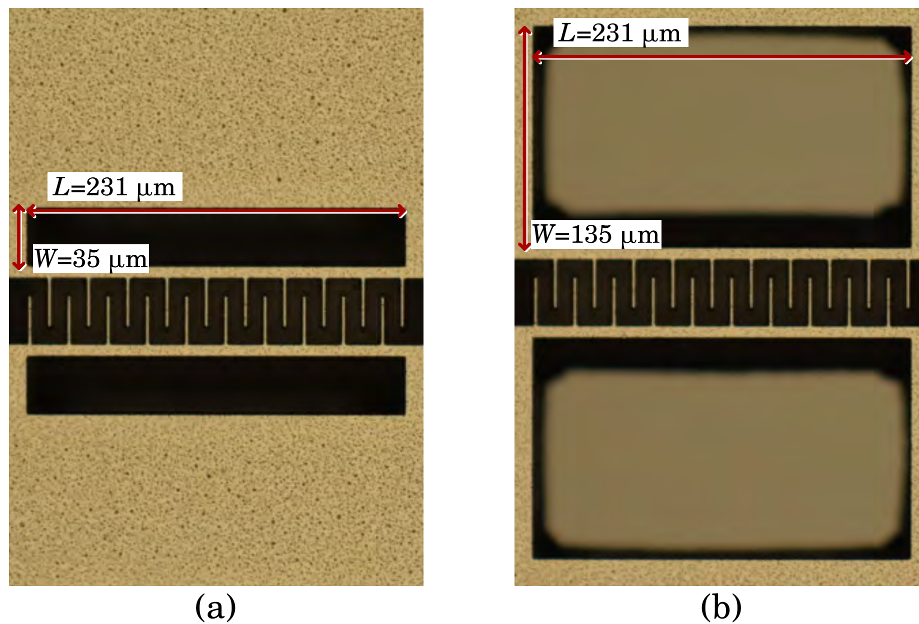


Fig. 2.21: Optical microscope image of comb with the large openings released under condition B. (a) With small openings (W=35 µm), the openings appear in black under optical microscope observation. (b) With large openings (W=135 µm), the middle of the openings remains, and only the contours of the openings appear in black.

2.3.2 Analysis of the two types of etching

Figure 2.24 and Fig. 2.25 show optical microscope and SEM images of etched trenches after DRIE, CF_4 passivation, and anisotropic etching under conditions A and B, respectively. From the figures, it can be seen that the main difference between the two results is the bottom aspect of the trench before isotropic etching. Under condition A, the middle bottom of the trench was etched, as shown in Fig. 2.24. In contrast, only the edges of the trench were etched under condition B, as shown in Fig. 2.25. This phenomenon is attributed to the oversupply of fluorocarbon species and the proximity effect of the trench side-wall. The etching species, i.e., ions and radicals, are trapped by the trench side-wall. Therefore, a smaller amount of species reaches the bottom of the trench close to the side-wall. In classical DRIE analyses, such non-uniformity is taken into account in the etching step. In

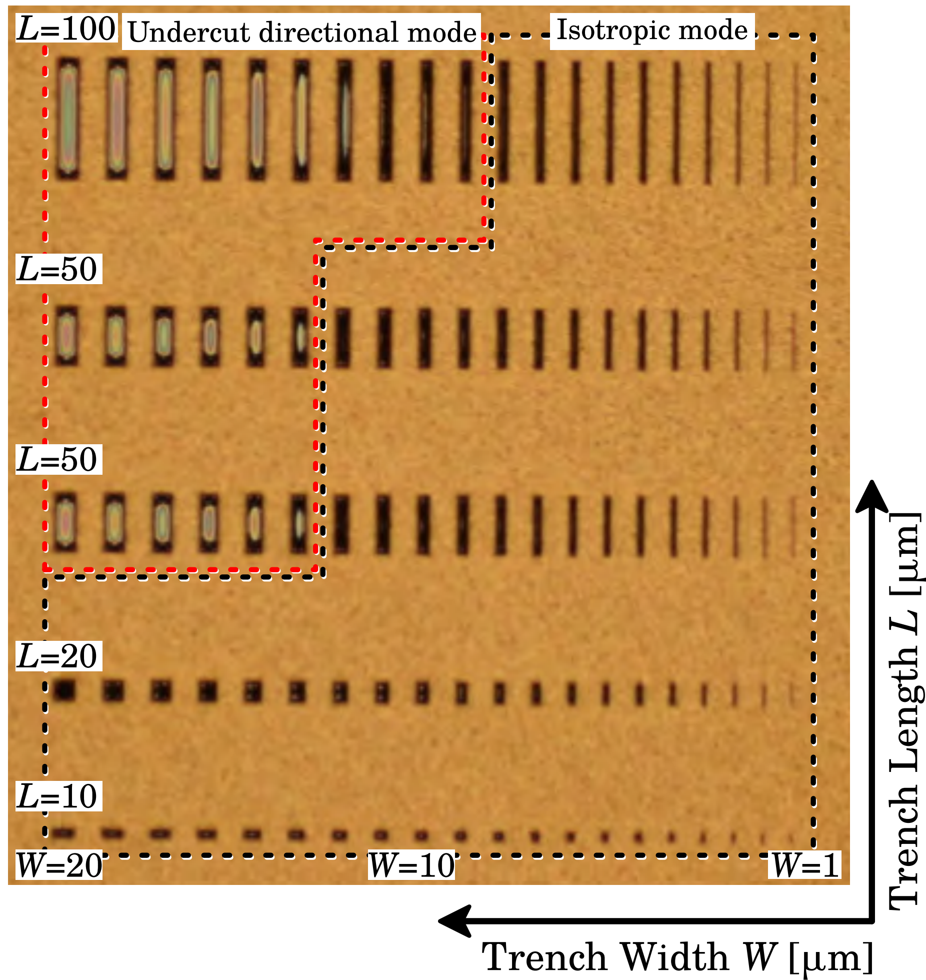


Fig. 2.22: Test structures showing the pattern dependence of the etching procedure after etching under condition B (Table 2.2).

fact, the same phenomenon occurs in the deposition of fluorocarbons, and the thickness increases with the distance from the trench wall. In standard DRIE (i.e., condition A), the fluorocarbon layer at the bottom of the trench is thoroughly removed by the biased SF_6 plasma; therefore, zero-biased SF_6 plasma etching isotropically proceeds as shown in Fig. 2.26. In contrast, when the ion bombardment is moderate, the CF_4 fluorocarbon protection layer remains in the middle of the large opening. As a result, the incoming SF_6 plasma species do not induce the etching reaction at the center bottom; they diffuse towards

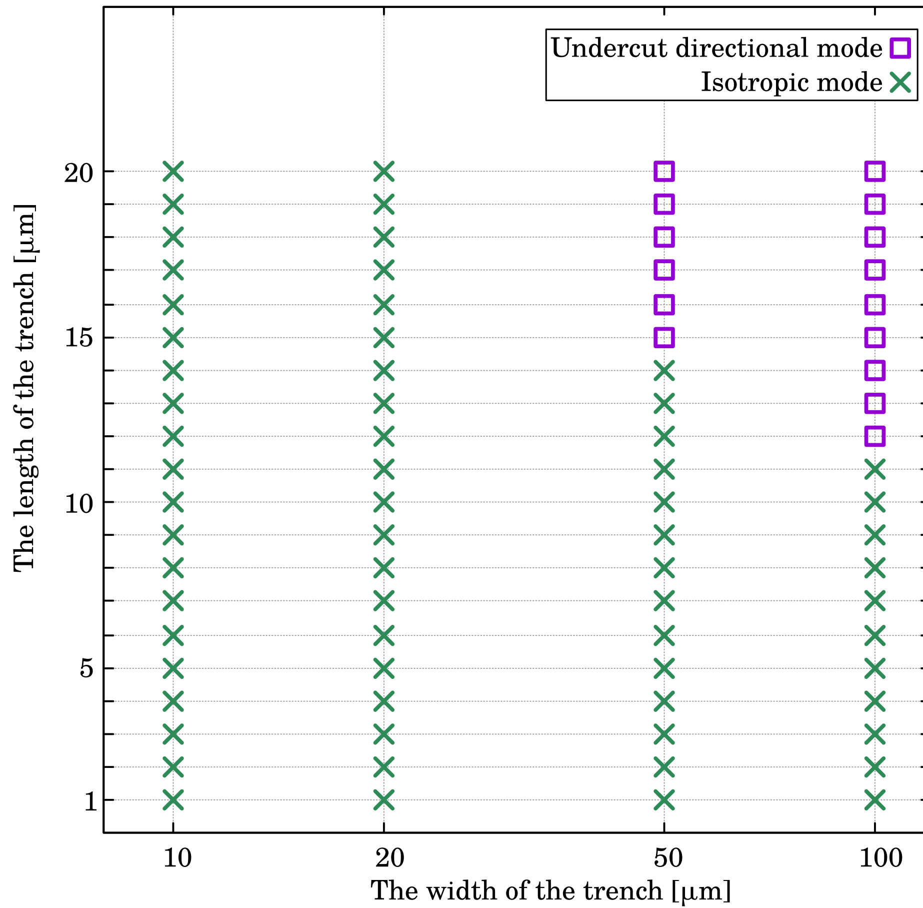


Fig. 2.23: Pattern dependence of the etching mode before SF_6 isotropic etching. As the opening becomes larger, the etching mode changes to the undercut directional mode.

the edges of the trench bottom and accumulate there. Therefore, the undercutting speed increases since it is proportional to the amount of species (Fig. 2.27). In this etching mode, the undercut etching seems to proceed from the large side openings mainly. This allows us to reduce the gaps in the comb structures easily.

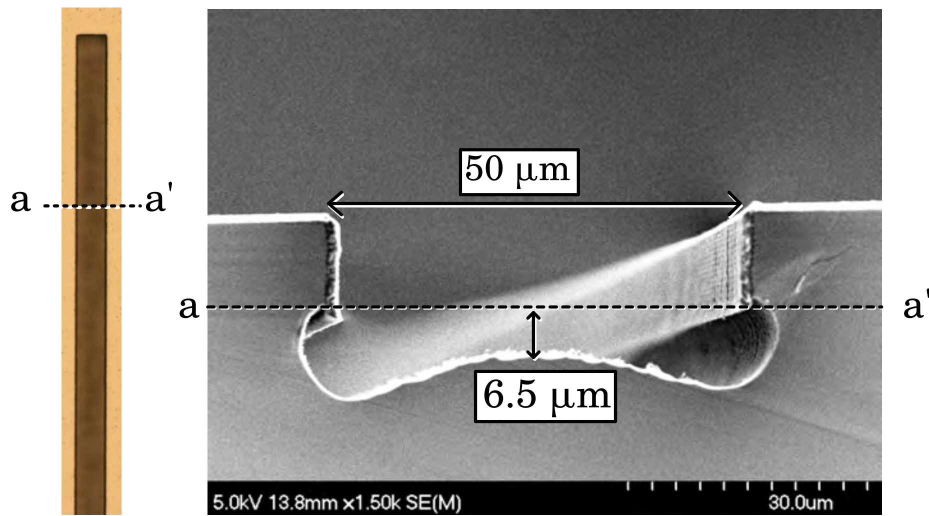


Fig. 2.24: SEM image of a trench on a silicon wafer before SF_6 isotropic etching. After etching by DRIE to form the trench, CF_4 was deposited on the trench, which was followed by etching with biased SF_6 under condition A (Table 2.2).

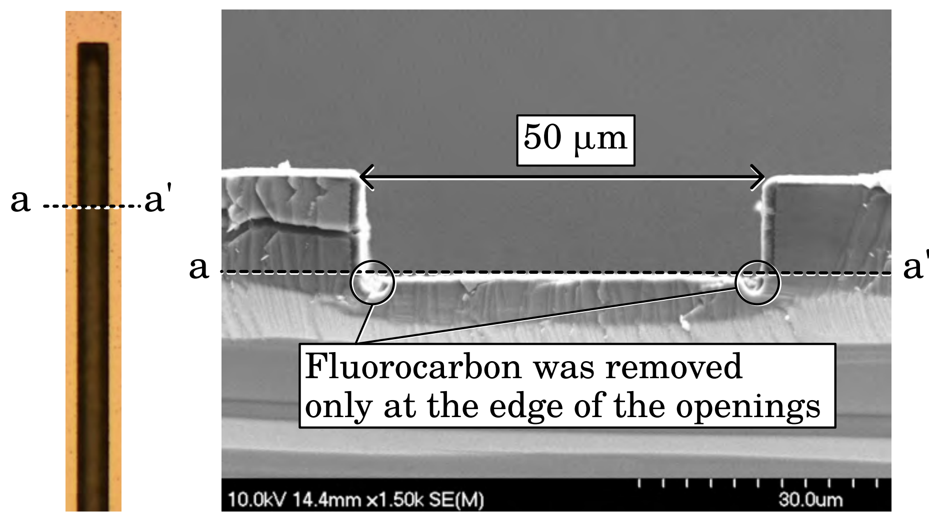


Fig. 2.25: SEM image of a trench on a silicon wafer before SF_6 isotropic etching. The DRIE condition was the same as that for Fig. 2.24. CF_4 deposition and biased SF_6 etching were performed under condition B (Table 2.2).

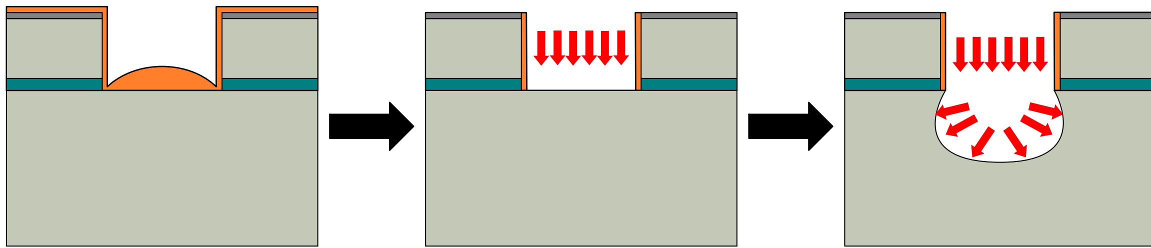


Fig. 2.26: Procedure of classic isotropic etching mode. The fluorocarbon-deposited layer at the bottom of the trench was entirely removed by biased SF_6 plasma, and zero-biased SF_6 plasma etching isotropically proceeds.

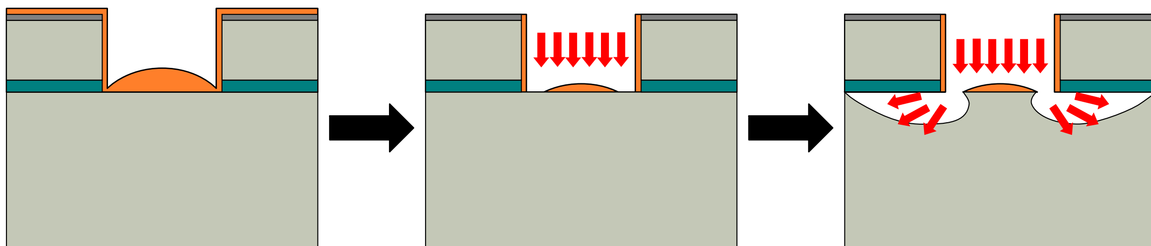


Fig. 2.27: Dependence of etching behavior on the mask opening size and the plasma deposition conditions. The fluorocarbon protection layer can remain in the middle of the large opening. Because of the oversupply of the etching species, pronounced undercutting occurs, enabling for rapid plasma release.

2.3.3 MEMS actuator fabrication using the test structure results and the undercut directional etching mode

As found by investigating the test structures, the design of the dry-released structures can be improved. Firstly, the square island structures indicate that the plasma conditions in this study cannot release structures larger than over 50 μm × 50 μm and that the opening holes next to the released structures should be larger than the structures. Secondly, placing a large hole next to a finely patterned structure such as a comb drive can cause undercut directional etching.

Figure 2.28 presents a layout that satisfies the conditions for release according to the

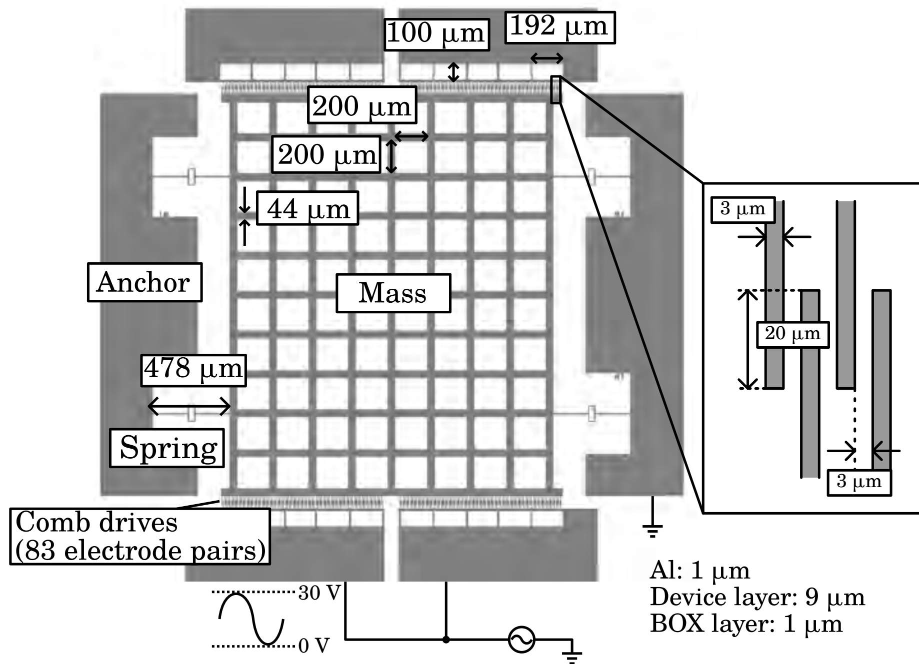


Fig. 2.28: Design of MEMS comb-drive actuator. (a) Overview, (b) design of comb drives, (c) design of springs.

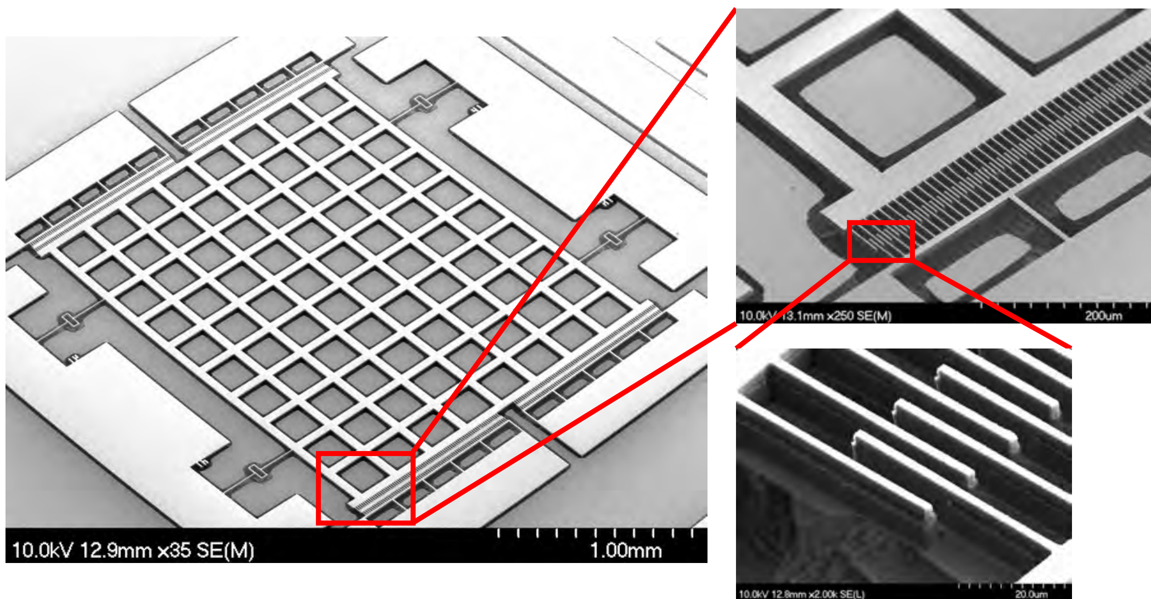


Fig. 2.29: SEM image of the dry-released comb drive subjected to the deep dry-release process.

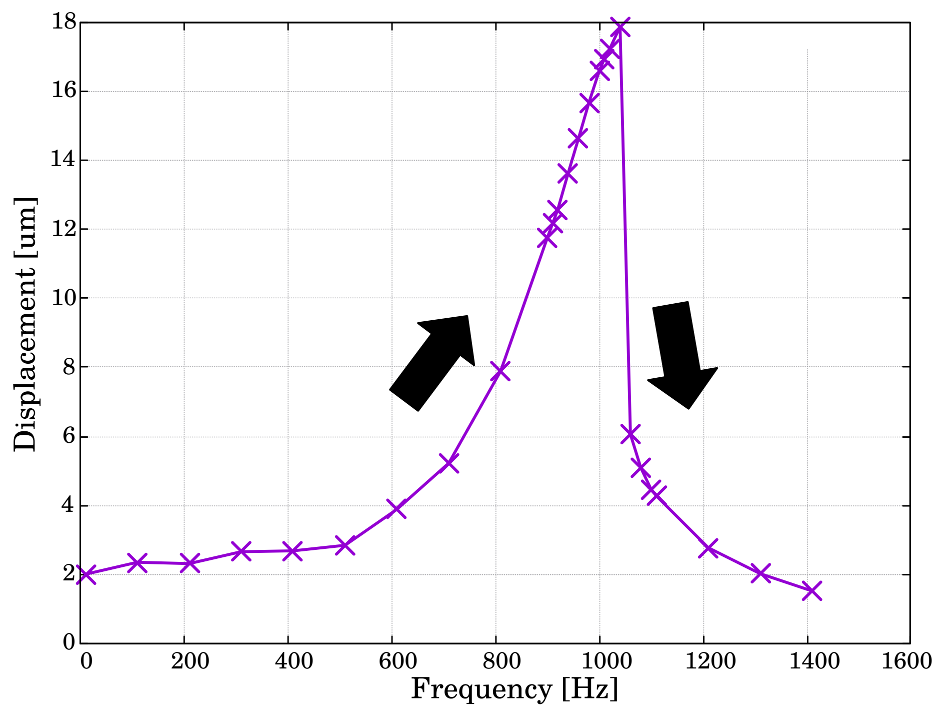


Fig. 2.30: Bode plot of the fabricated device at 30 V. The resonant frequency was 1.02 kHz.

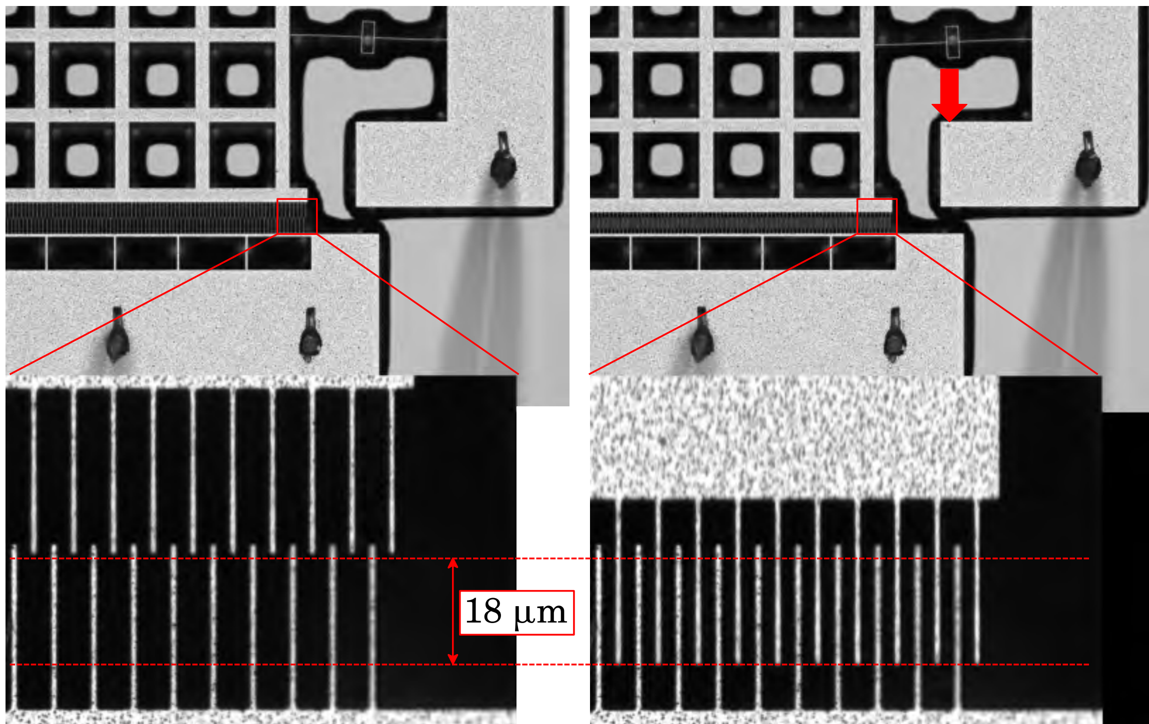


Fig. 2.31: Microscope image of the actuator under resonance at 30 V

results of the test structures and Fig. 2.29 is an SEM image of a dry-released comb actuator. Although the actuator could not be released in the first isotropic etching mode, it was released in the second side-etched isotropic etching mode. Owing to the etching mode, in spite of the small 3-μm gaps in comb structures, the structure was entirely released. It indicates that the undercut etching proceeds from the large side walls. Figure 2.30 shows a bode plot of the released MEMS actuator, indicating that its resonant frequency was 1.02 kHz. Figure 2.31 shows the displacement of the comb drive by 18 μm when applying a voltage of 30 V at the resonant frequency, 1.02 kHz. The frequency of the applied signal was swept from 10 Hz to 1.4 kHz.

2.4. Summary

Test structures were designed to indicate the endpoint of the isotropic etching process by simple observation with an optical microscope. Using the test structures, not only was the exact release time determined, but a new plasma etching mode was discovered. In contrast to standard isotropic etching, which is suitable for post-processed DTI, the new etching mode is an undercut directional etching which allows the dry release of MEMS devices. Through detailed observation with an optical microscope and SEM, the difference in the etching modes was attributed to the balance between the deposition and etching plasma phases. An additional test structure allowed us to identify the switching point between the etching modes. By using the design parameters extracted from the test structures and the undercut directional etching mode, a comb drive actuator was successfully dry-released. The usefulness of the test structure was thereby confirmed, together with the undercut directional condition.

CHAPTER 3

High-Voltage Switch & Generator

Some of the text and the materials of this chapter are based on the articles of the author's group entitled "Integrated 0–30 V switching driver circuit fabricated by mesa isolation postprocess of standard 5 V CMOS LSI for MEMS actuator applications," published in Microsystem Technologies, Vol. 24, No. 1, pp. 503–510, 2018, and "On-Chip High-Voltage Charge Pump with MEMS Post-Processed Standard 5-V CMOS on SOI for Electroosmotic Flow Micropumps," published in IEEE Electron Device Letters, Vol. 39, Issue 6, pp. 851–854, 2018.

3.1. Introduction

In this chapter, we propose high-voltage devices using the post-processed DTI transistors. First, to demonstrate the use of the post-processed DTI transistors for high-voltage devices, we discuss a 30-V switching device. Subsequently, high-voltage generators using the post-processed DTI transistors are discussed.

3.2. High-Voltage Switch

High-voltage switching is one of the critical issues that should be resolved to realize the monolithic integration of CMOS LSI and high-voltage devices such as a switching

regulator and MEMS. By introducing post-processed DTI, we propose the fabrication of a high-voltage switching circuit from a *standard* CMOS transistor. Owing to the proposed method, such high functionality with high reliability can easily be realized.

When applying the post-process LSI technology to high-voltage switching, one straightforward means of sustaining a high voltage using standard CMOS transistors is to connect transistors in series. However, since transistors in an LSI are fabricated on the same substrate, such a method causes body–drain breakdown.

By the post-processed DTI method, we can connect CMOS transistors in series on a chip in a CMOS foundry process and separate their substrates in a few steps. Using this method, we can apply independent body bias voltages to each transistor without triple-well isolation. Moreover, Hirakawa *et al.* measured the voltage hold-off capability of mesa-isolated series-connected standard transistors and proved that the method could allow standard CMOS transistors to endure up to $160V_{\mathrm{DD}}$ (800 V) [81], which is at least 16 times higher than the endurance voltage when using the triple-well isolation method.

However, series-connected transistors need many levels of gate voltage since the voltage between the drain and the source should be kept below 5 V to avoid breakdown. The effectivity of the series connection method has been well studied using the triple-well isolation method [84], [85]. However, no complete integrated circuit integrated with multiple-voltage-level shifters nor a demonstration of high (over $5V_{\mathrm{DD}}$)-voltage actuators using the post-processed DTI method has been presented. Therefore, it is essential to demonstrate and measure high-voltage switching using post-processed DTI transistors. Table 3.1 shows the comparison between previous level shifters and this work. While the DMOS HV switch requires dedicated HV CMOS technology [86], series-connected HV switches enable us to use standard CMOS technologies. However, the previous

Table 3.1: Comparison of level shifters for HV switches. $V_{DD,HV}$ is the maximum voltage of an LDMOS, and V_{DD} is the logic supplied voltage.

	Technology	Method	Demonstrated switching voltage	Voltage limitation
Khorasani [86]	HV CMOS	LDMOS	300 V	$V_{DD,HV}$
Serneels [87]	Standard CMOS	Series connection	7.5 V	$3V_{DD}$
Lin [88]	Standard CMOS	Series connection	9.9 V	$3V_{DD}$
This work	Standard CMOS+ MEMS post-process	Series connection	30 V	$N \cdot V_{DD}$

methods [87], [88] can be used only in three PMOS/NMOS transistors. Our proposed method can be used in N transistors and have a wider switching-voltage range.

In this section, we demonstrated 30 V switching with six pairs of series-connected post-processed P-N transistors on a chip, and the performance of the series-connected transistors was measured [89]. Then, in order to solve the problem of multiple-gate-voltage levels, we demonstrated a 30 V switching circuit with the monolithic integrated gate-level shift circuits. Finally, we demonstrated the dynamic driving of the MEMS actuator with high-voltage switching.

3.2.1 Fabrication

3.2.1.1 Post-Processed DTI series-connected transistors

We fabricated the post-processed DTI integrated circuit by MEMS post-processing on a standard CMOS LSI. The CMOS LSI was fabricated by a foundry company using standard 0.6 μm CMOS process technology on a silicon-on-insulator (SOI) wafer (9 μm-1 μm-625 μm) without any alternations to the process (Fig. 3.1a). Then a deep-RIE (DRIE) post-process was performed in a university MEMS cleanroom. First, a thick electron-beam

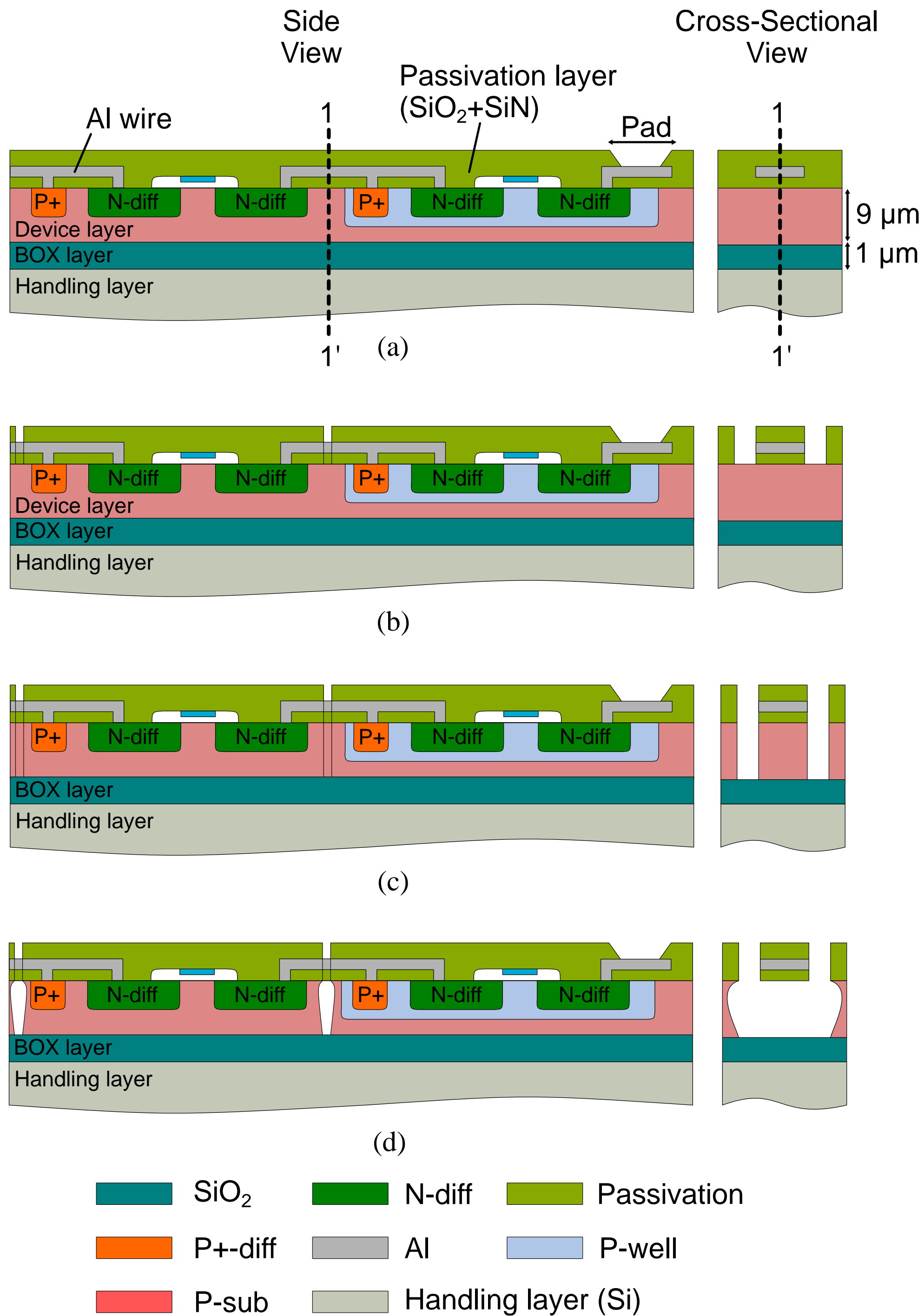


Fig. 3.1: Process flow of mesa-isolated series-connected transistors. (a) CMOS fabrication at a foundry company. (b) The passivation layer is patterned for a mask. (c) DRIE is performed. (d) SF_6 isotropic etching is performed to remove the entire silicon.

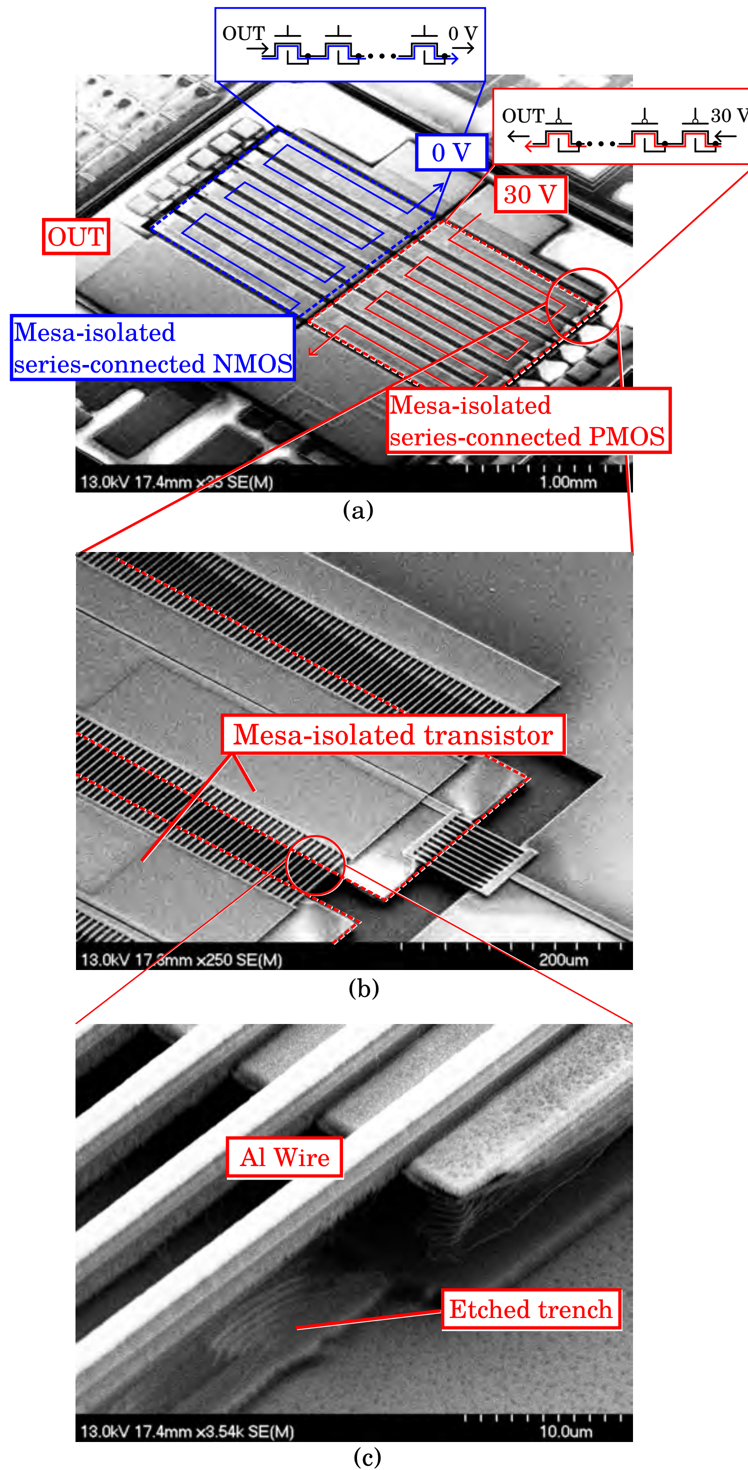


Fig. 3.2: (a) SEM image of a fabricated 30-V switching circuit using mesa-isolated series-connected transistors. (b) Close-up view of mesa-isolated transistors. (c) Close-up view of the DRIE isolation. The substrate under the metal bridges is removed by isotropic etching.

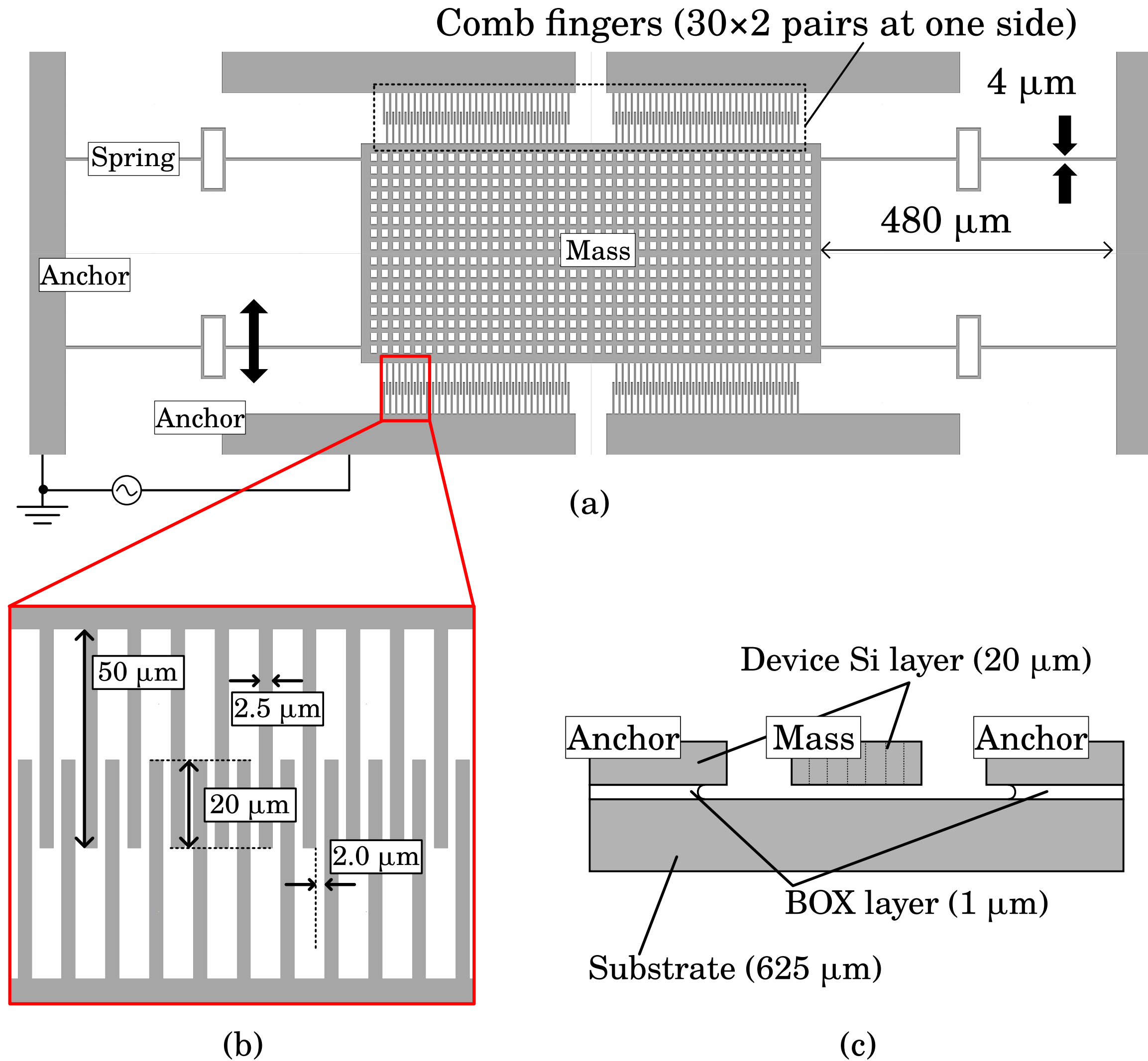


Fig. 3.3: Design of the MEMS actuator used in the dynamic driving experiment. The thickness of the movable part of the actuator is 20 μm. (a) Top view of the actuator. (b) Close-up view of the comb electrodes. (c) Side view of the actuator.

(EB) resist was directly patterned using a rapid EB writer, and then the surface SiO_2 and SiN passivation layer was etched using CHF_3 plasma (Fig. 3.1b). After that, the Si body was removed by DRIE, as shown in Fig. 3.1c. Finally, SF_6 isotropic plasma etching was carried out so that the transistors were isolated from each other, as shown in Fig. 3.1d.

An SEM image of the fabricated device is shown in Fig. 3.2a. The device is composed of six series-connected PMOS transistors and six series-connected NMOS transistors. From

the close-up view of the transistors (Fig. 3.2b), it is observed that the transistors are isolated from each other. Besides, regarding the metal bridges (Fig. 3.2c), it is observed that the Si body under the metal bridge is etched out by isotropic SF_6 plasma etching.

The dimensions of one transistor are 100×250 μm^2. The W/L ratio of the transistor was designed to be 1:4000 to allow the passage of relatively high currents (up to 100 mA). The total device dimensions are 2.5×3.4 mm^2.

3.2.1.2 Electrostatic comb-drive MEMS actuator

For a dynamic driving experiment with high-voltage switching, an electrostatic MEMS comb-drive actuator was fabricated on another SOI wafer, whose layout is shown in Fig. 3.3. First, a thick EB resist was patterned using a rapid EB writer. Then, a MEMS structure was formed by DRIE. Finally, the movable structure was released by vapor hydrofluoric acid (HF) etching.

3.2.2 Experiments and results

Figure 3.4 shows the gate voltage protocol of the high-voltage switch. To turn on the switch, as the PMOS transistors were turned on, 25 V was applied to all of their gates. On the other hand, the gates of NMOS transistors were set from 0 V up to 25 V in steps of 5 V so that the NMOS transistors were turned off. The same principle was applied when the switch was turned off, which means that the output was 0 V. Following this gate voltage protocol, we measured the static and dynamic characteristics of the fabricated device.

First, the load current (I_{load})–output voltage (V_{out}) characteristic (the static characteristic) was measured with a source measure unit (Agilent B2902A). Figure 3.5a shows the measurement setup and Fig. 3.5b shows the I_{load}–V characteristic. In the range where

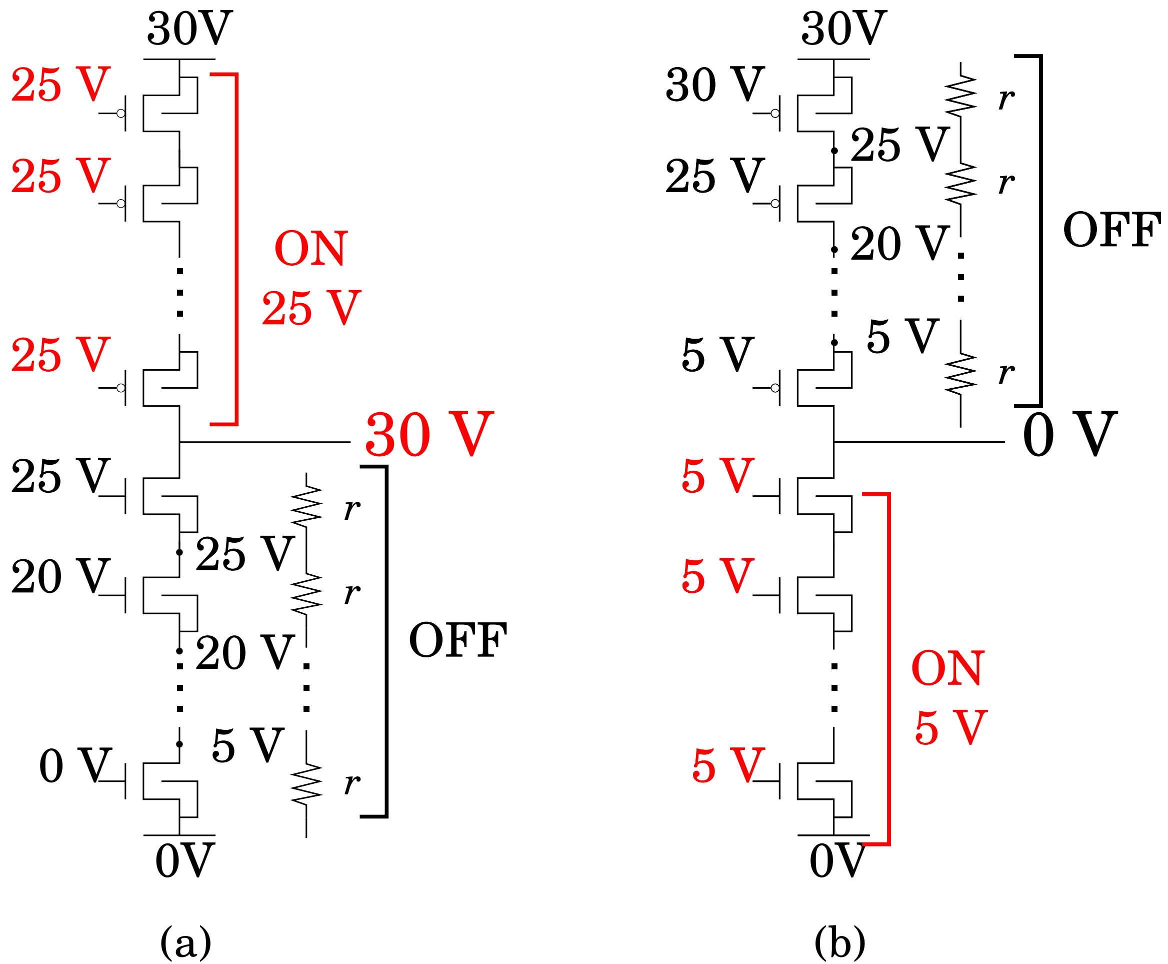


Fig. 3.4: Schematics of series-connected transistors in (a) the on-state and (b) the off-state. Off-state transistors can be regarded as resistances, and V_{gs} should be kept at 5 V. V_{ds} of on-state transistors is considered to sustain the same voltage, so V_{gs} should be V_{source}-5 V (PMOS) or V_{source} + 5 V (NMOS).

I_{load} was over 70 mA, the output sharply declined. The result shows that the switch can be used as a 30 V switching device for a 70 mA load. In the range where I_{load} was over 100 mA, the output declined to about 21.5 V. In the range where the switch works as a 30 V switching device, R_{out} was calculated as about 30 Ω. It is six times as large as the on-resistance of a PMOS transistor, which means that all of the transistors remain on-state.

Next, we measured the dynamic characteristics of the switch. Fig. 3.6 shows the waveforms of the output signal and the input signal of a 4 Hz square wave (0–5 V).

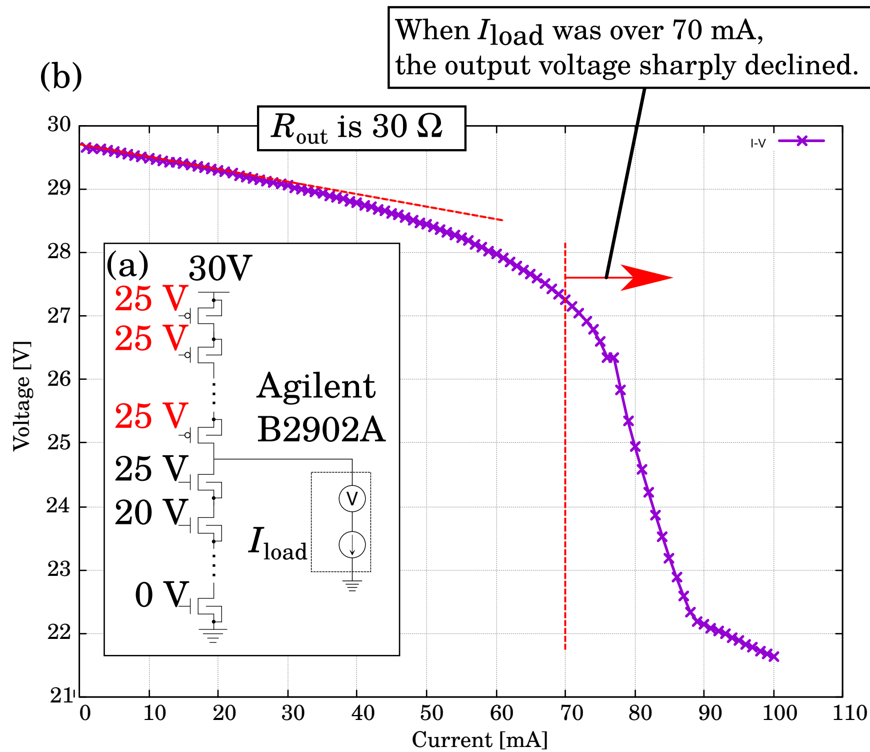


Fig. 3.5: (a) Schematic of the load test with Agilent B2902A SMU. (b) I–V characteristics of the high-voltage switch. While I_{load} is below 70 mA, R_{out} is about 30 Ω, which is six times as large as the single transistor's R_{out}.

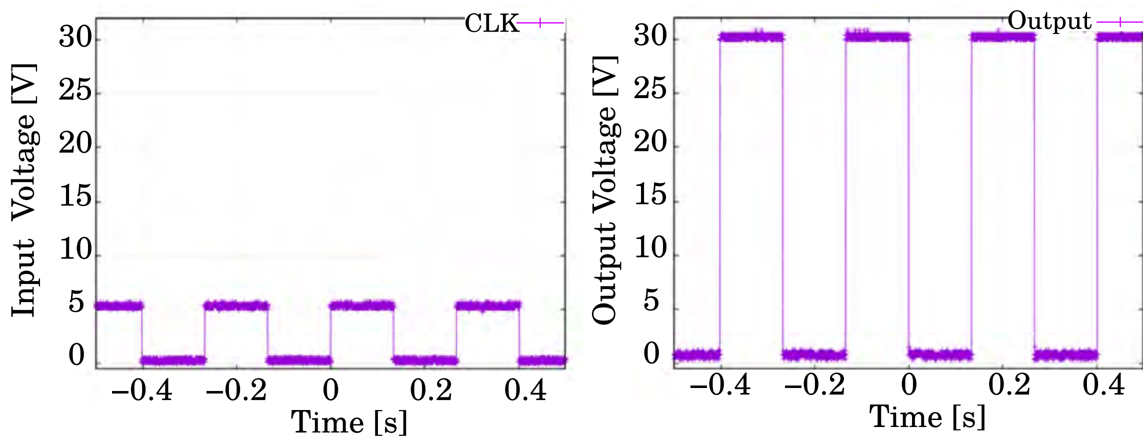


Fig. 3.6: Waveforms of the input signal and the output signal. The input signal was generated on an external PCB circuit, which is composed of the 5 V pulse oscillator and a voltage-level shifter.

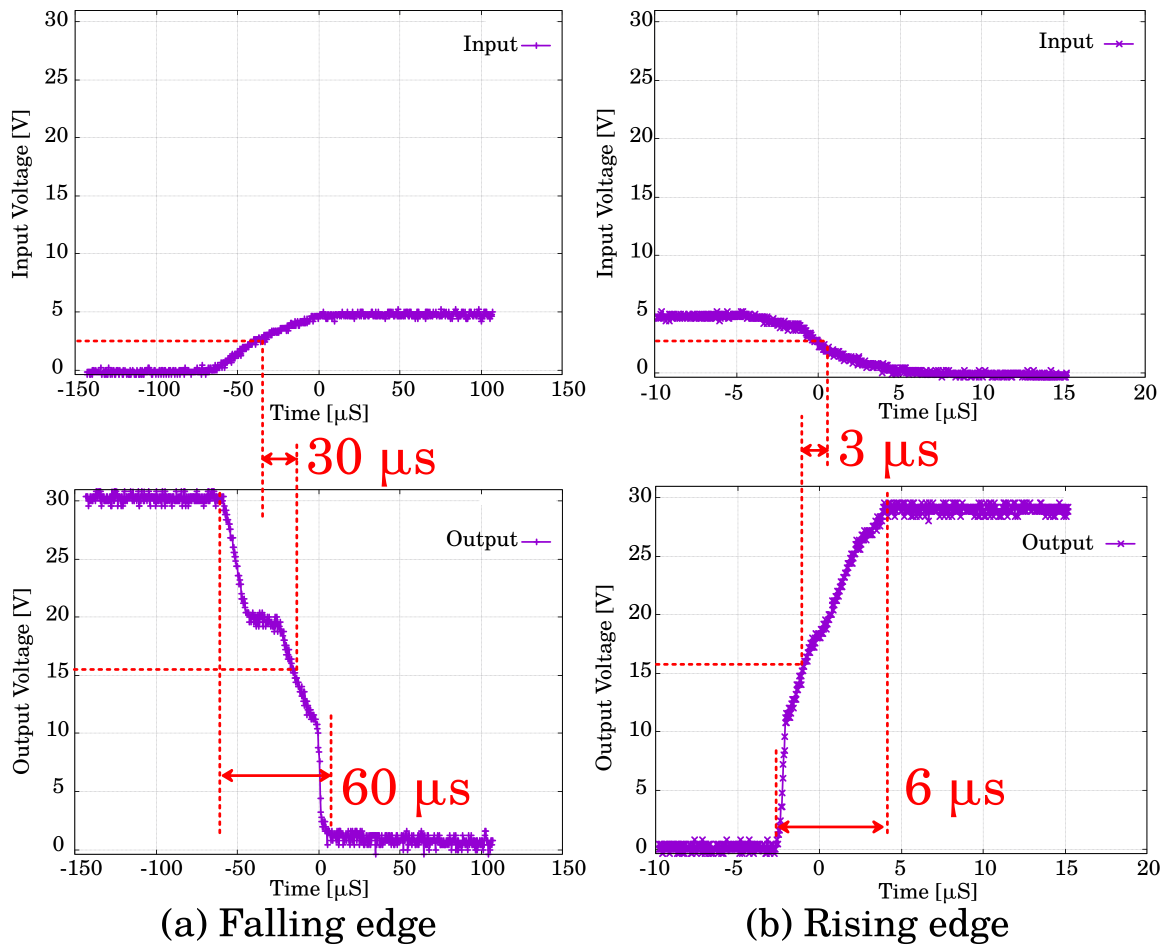


Fig. 3.7: Input to output propagation delay times of (a) falling edge and (b) rising edge. Hysteresis between the falling and rising edges was observed. For the rising edge, transistors were turned on 3 µs before the input voltage became 2.5 V, while they were turned off 30 µs after the input voltage became 2.5 V.

An external oscillator generated the input signal, and the voltage applied to each gate was generated on a PCB. The output from the device was the level-shifted square waveform (0–30 V). Then, the delay times of the falling and rising edges were measured. When the output voltage decreased, the output became 15 V, 30 µs after the input voltage increased to 2.5 V, as shown in Fig. 3.7a. On the other hand, when the output voltage rose, the output voltage became 15 V, 3 µs before the input voltage decreased to 2.5 V, as shown in Fig. 3.7b.

3.2.3 Design methodology towards scalable high-voltage switching circuit with 5 V CMOS transistors

In the previous section, the proposed high-voltage switching method is successfully confirmed for the $6V_{DD}$ (30 V) switching circuit with six pairs of post-processed DTI series-connected PMOS and NMOS transistors. In real applications, MEMS actuators have a wide range of driving voltages; for example, typical electrostatic MEMS actuators need driving voltages from $2V_{DD}$ to $10V_{DD}$ (10–50 V), and electrowetting-on-dielectric (EWOD) droplet actuators need from $3V_{DD}$ to $20V_{DD}$ (15–100 V) [90]. Therefore, the design methodology for realizing a scalable switching circuit is essential.

3.2.3.1 General design rule of $N - V_{DD}$ switching circuit

Figure 3.8 shows the N-series-connected transistor pair circuit diagram and gate voltage in the ON and OFF states. The supply voltage V_{supply} is proportional to the number of series pairs: NV_{DD}. The size of each transistor is defined by the required load current. Note that the gate width must be N times larger since the total gate length is multiplied by a factor of N.

Particular attention should be paid to the control of the gate voltages, as explained below. To turn on PMOS transistors, $V_{supply} - V_{DD}$ (i.e., $V_{gs} = -V_{DD}$) is simply applied to all gates in parallel. To turn off PMOS transistors, however, voltage levels are all different according to the order of the PMOS transistors. This complicated operation is because each transistor must hold V_{DD}, so the source voltage level increases in proportion to the number of series-connected transistors. For example, for the first PMOS transistor, where the source is connected to V_{supply}, V_{supply} (i.e., NV_{DD}) must be applied to the gate. The gate voltage of the second series PMOS transistor V_{gp2} is $(N-1)V_{DD}$, and accordingly, $(N-i+1)V_{DD}$

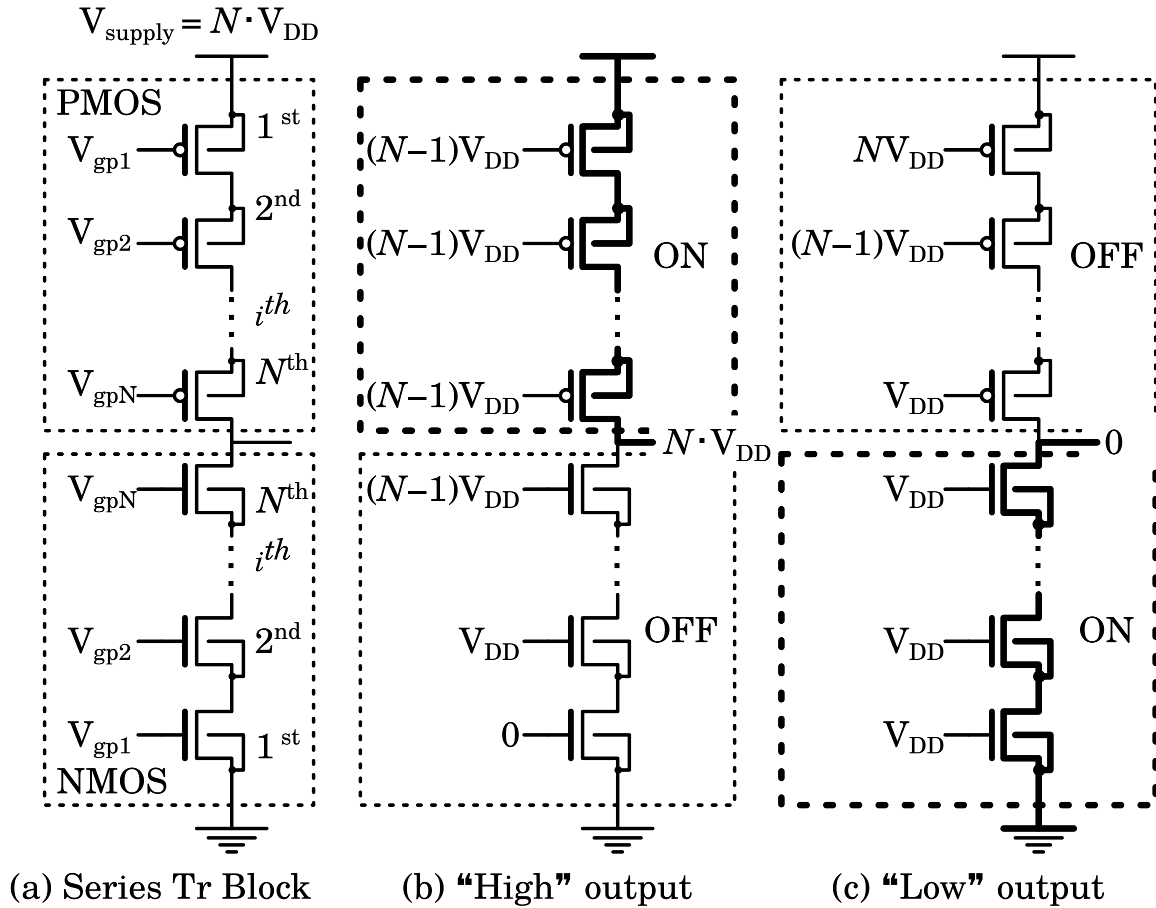


Fig. 3.8: Gate voltage protocol to drive series-connected transistors.

must be fed to the gate of the ith series PMOS transistor. Likewise, all NMOS transistors are turned on by applying $V_{gni} = V_{DD}$ and turned off by applying $V_{gni} = (i-1)V_{DD}$.

Figure 3.9 shows A block diagram of the entire HV switch. Fig. 3.9a shows the series-connected transistor block and Fig. 3.9b shows the gate voltage generator. The circuit of the gate voltage generator is composed of offset voltage addition circuits (Fig. 3.9c) and voltage amplifier circuits. According to the gate voltage swing (i.e., the difference between V_{gON} and V_{gOFF}), either of the circuits is used. For the gate voltage swing of $\pm V_{DD}$, the offset voltage addition circuit (Fig. 3.9c) is used. To generate a swing larger than $\pm V_{DD}$, voltage amplification is necessary. The voltage amplifier is a small voltage switching circuit having

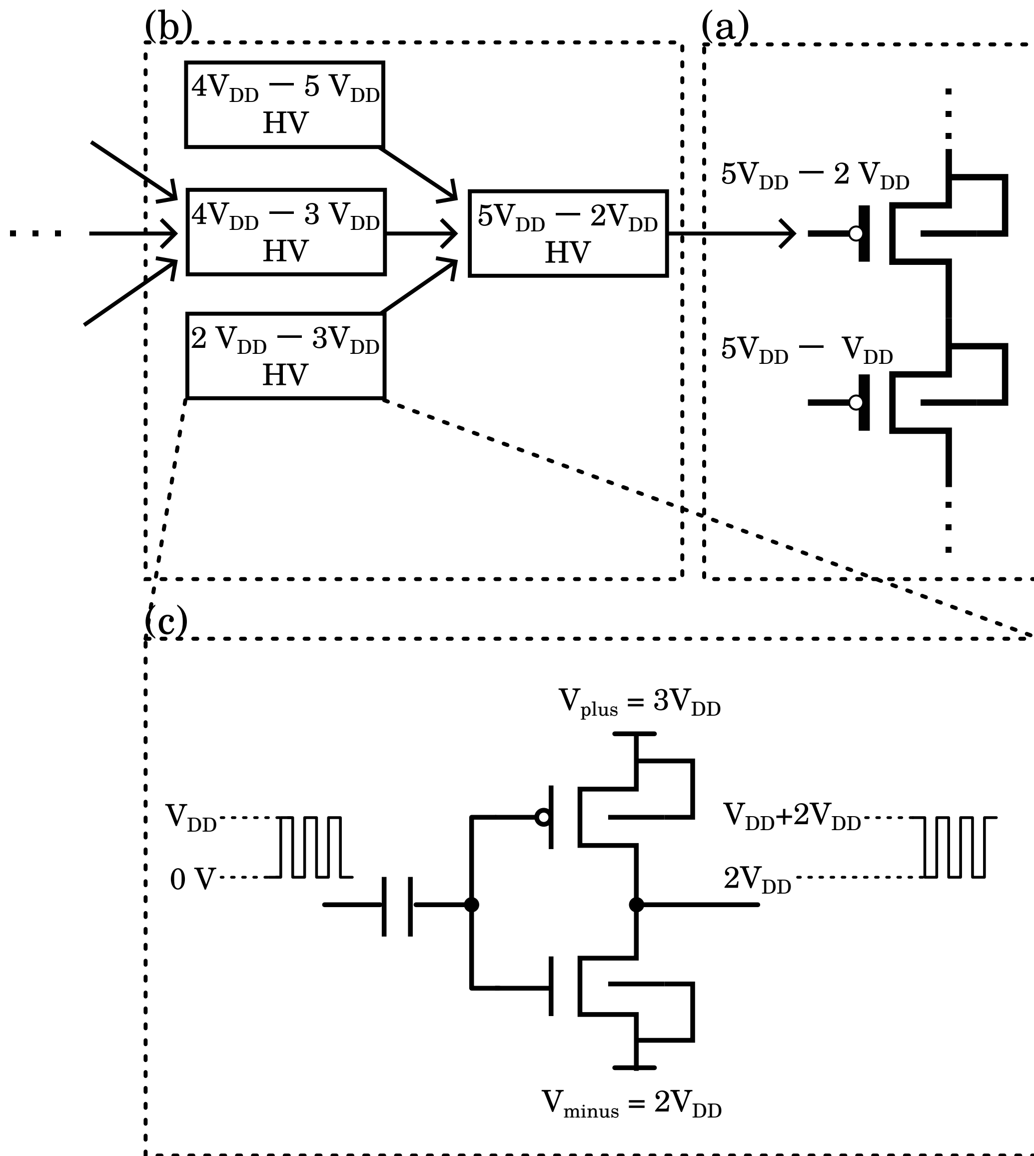


Fig. 3.9: (a) Main buffer of mesa-isolated series-connected transistors for driving the load. The sizes of these transistors depend on the load. (b) Level shift circuit. The circuit can be composed of mesa-isolated transistors. The transistors can use the minimum size. (c) Offset voltage addition circuit.

the same circuit topology as the primary switching circuit, with a smaller number of stages. Therefore, all of the subcircuits can be designed recursively, reducing the design cost of the circuits switching the desired voltage, even when a large number of voltage amplifier subcircuits are needed. For $V_{\text{supply}} = NV_{\text{DD}}$, the smallest voltage amplifier is used for the voltage swing of $2V_{\text{DD}}$, and the largest one is used for the voltage-swing of $(N-4)V_{\text{DD}}$.

3.2.3.2 Implementation of $6V_{\text{DD}}$ switching circuit integrated with level shifters

As a demonstration of the proposed methodology of the high-voltage switch, a $6V_{\text{DD}}$ (30 V) switching circuit with main-buffer series-connected transistors and gate level circuits was designed and fabricated. Fig. 3.10a shows a schematic of the 30 V switching circuit.

Fig. 3.10b shows the offset voltage addition circuit. The voltage difference between V_{plus} and V_{minus} must be V_{DD} (5 V) in order not to cause a breakdown. To add a 5 V offset, the source of the NMOS transistor is connected to a voltage of 5 V.

Fig. 3.10c shows the 5–20 V switching circuit. Although the circuit is equivalent to the 15 V switching circuit, the ground voltage is changed to 5 V.

3.2.3.3 Fabrication

The transistors of the integrated voltage shifter were fabricated by the same foundry company, and post-processed DTI was carried out in a university cleanroom. Note that the metal wiring that connects the transistors were made by the same foundry company. SF_6 isotropic etching successfully removed the silicon substrate under the wiring.

An SEM image of the fabricated device is shown in Fig. 3.11. The main (current-driving) transistors are composed of six pairs of series-connected PMOS and NMOS transistors. From the close-up view of the transistors (Fig. 3.11b), it was observed that the transistors are isolated from each other. In this design, the W/L ratio of the series transistors is 1:3,

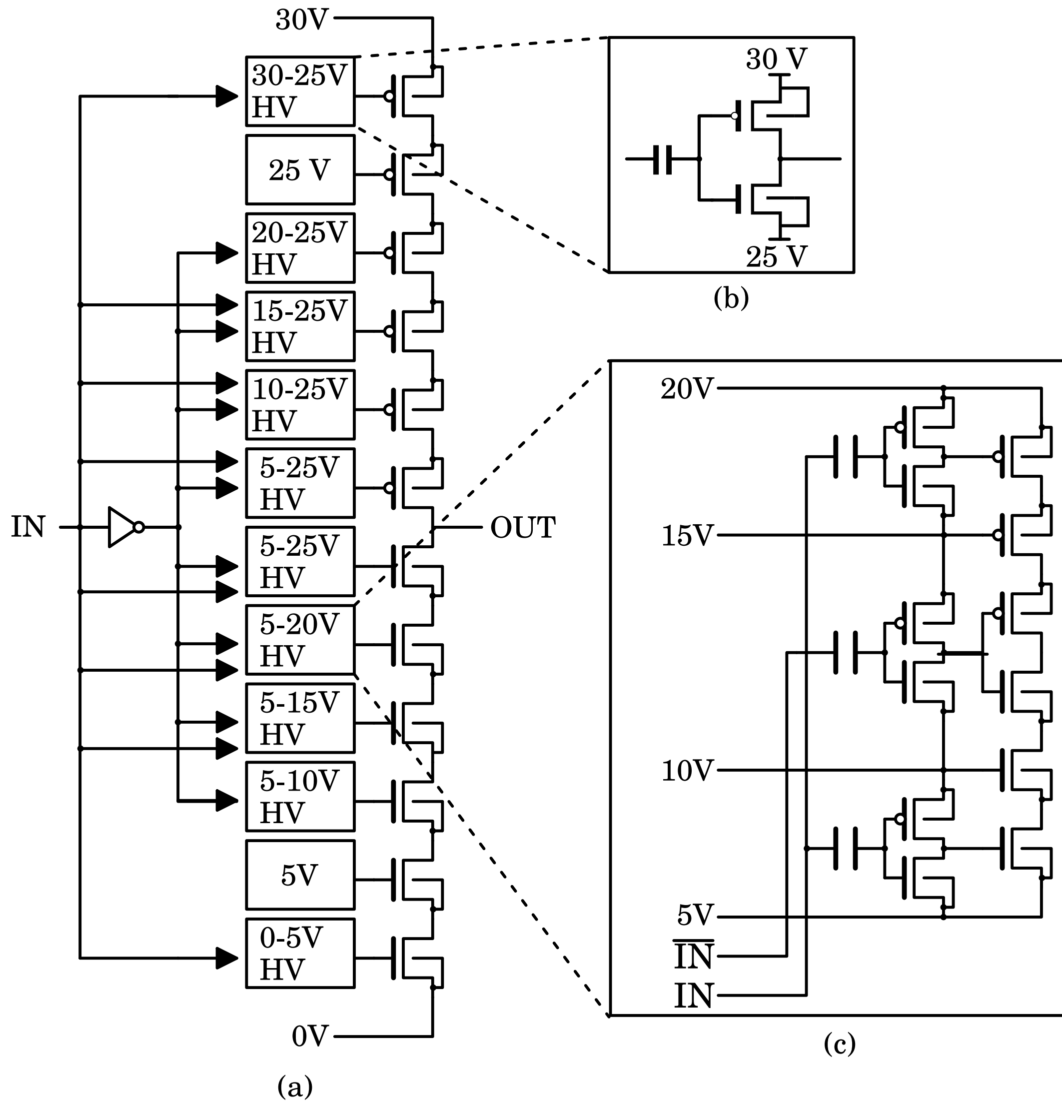
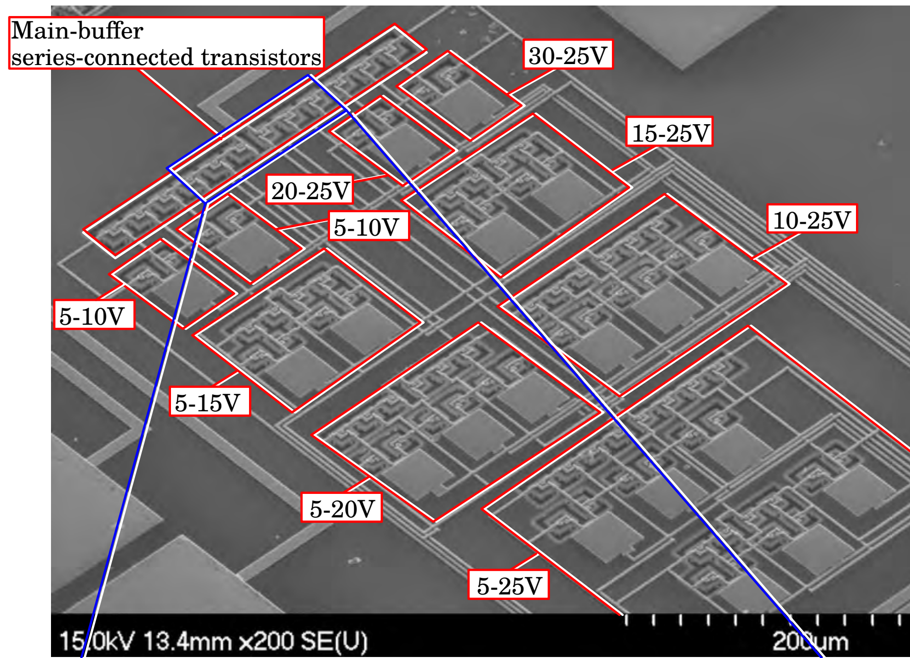


Fig. 3.10: (a) Schematic of the 0–30 V switching circuit. (b) Schematic of the offset voltage addition circuit. (c) 5–20 V switching circuit.

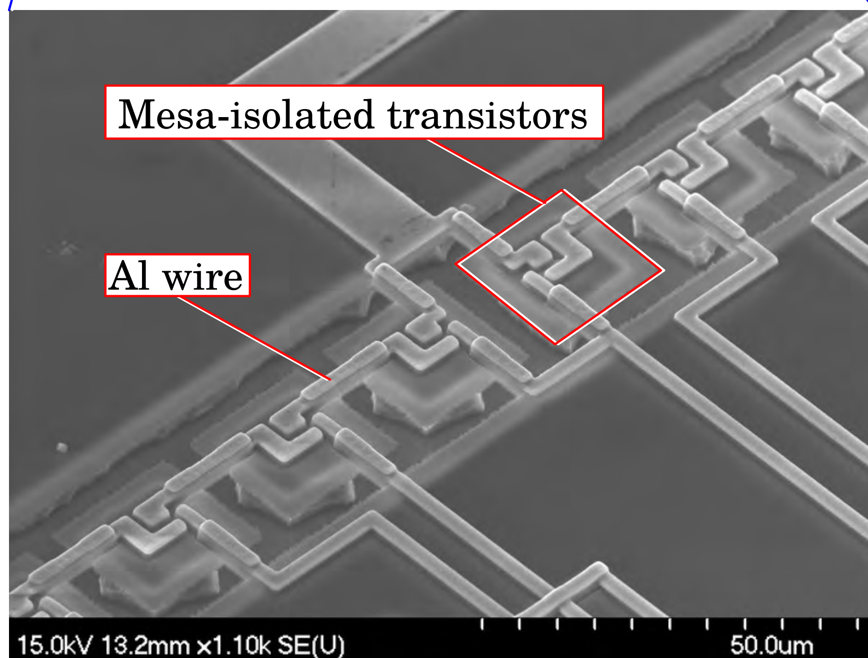
and the transistors are expected to hold a current of 1 mA. The total device dimensions are 400×640 µm^2.

3.2.3.4 Measurement

Fig. 3.12 shows the setup for the measurement of the output of the integrated high-voltage switch. Driving voltages from 0 V up to 30 V in steps of 5 V were supplied to the circuit,



(a)



(b)

Fig. 3.11: (a) SEM image of 30 V switching circuit with mesa-isolated series-connected transistors integrated with a gate-level-shift circuit. (b) Close-up view of mesa-isolated transistors.

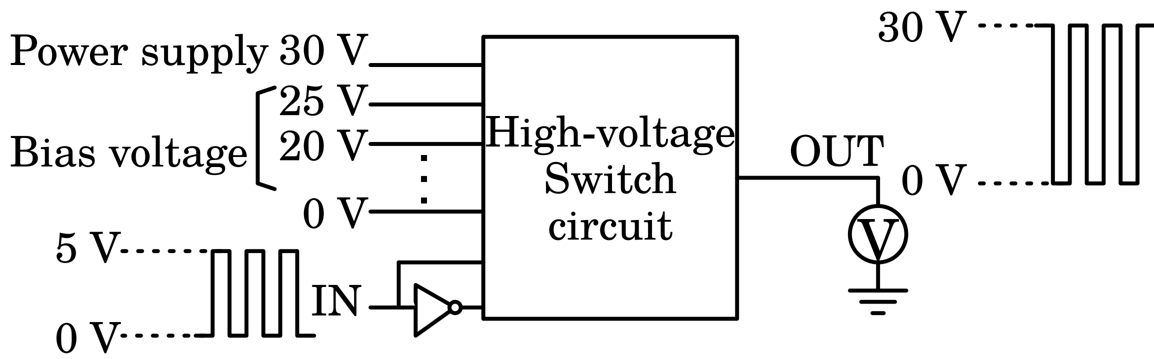


Fig. 3.12: Schematic of setup to test high-voltage switch integrated with level-shift circuits.

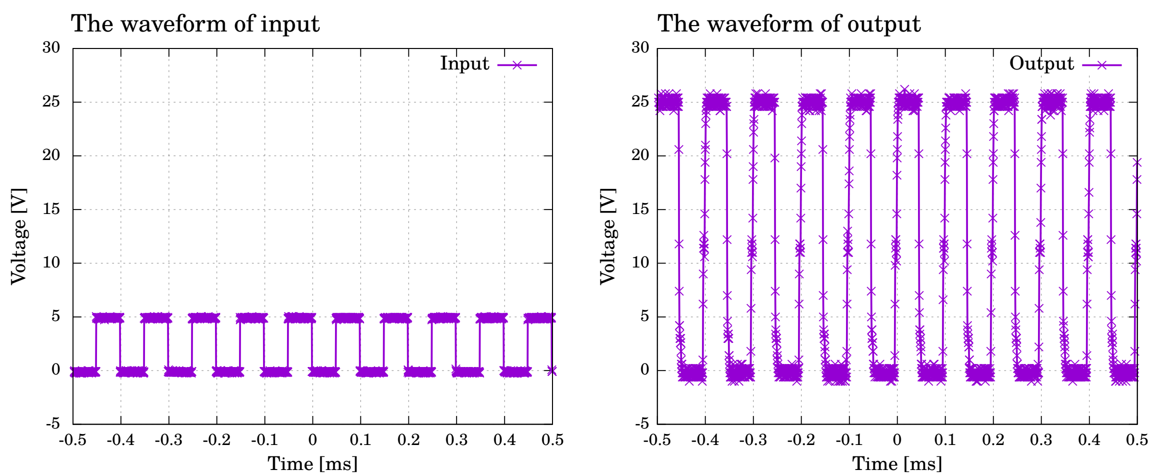


Fig. 3.13: Waveforms of input and output signals. The input signal was generated on an LSI chip.

and the input signal was a 5 V square wave of 10 kHz. Fig. 3.13 shows the waveforms of the output and input signals. An external oscillator generated the input signal. The output from the device was the level-shifted square waveform.

3.2.3.5 Demonstration of driving the MEMS actuator

For a demonstration of driving a microactuator, the $6V_{DD}$ switching circuit shown in section 4 was connected to the SOI MEMS device described in section 2.2. With the setup shown in Fig. 3.14, displacement of the MEMS comb drive of 10 µm was confirmed. The

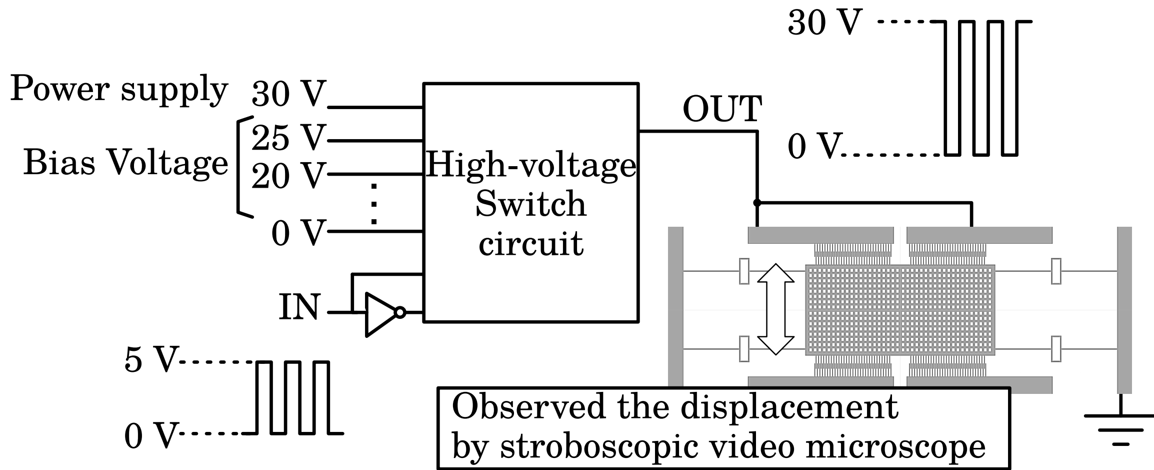


Fig. 3.14: Setup for the MEMS actuation test with a fabricated high-voltage switch. The input signal is generated by the external oscillator.

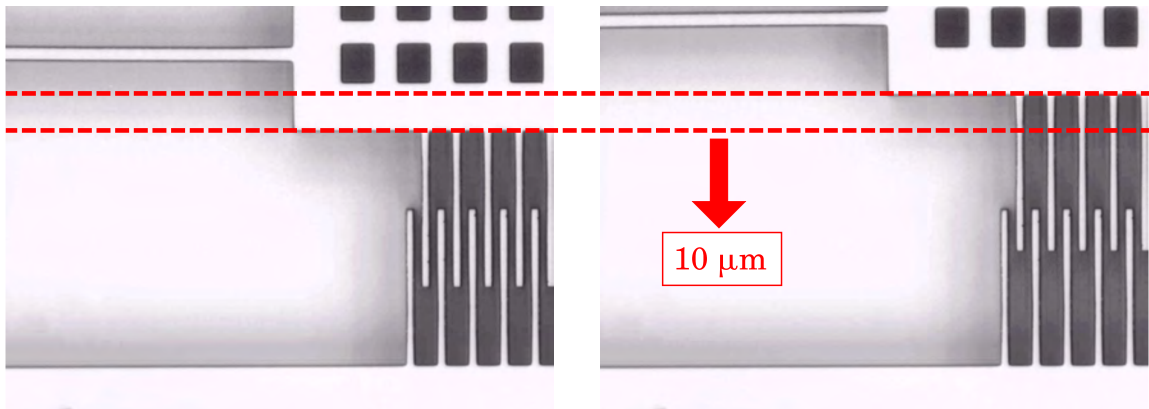


Fig. 3.15: Microscopy images of the actuator at 30 V 5 kHz square wave with the high-voltage switch. The displacement was 10 µm.

driving signal from the switch was a 0–30 V square wave of 5 kHz, as shown in Fig. 3.15.

3.2.4 Summary

We demonstrated 30 V switching using the on-chip post-processed DTI series-connected transistors. From the analysis, the device (2.5×3.4 mm^2) works as a 30 V switching circuit if the load current is below 70 mA. Then, the methodology of scalable high-voltage switches

was described. Using the methodology, we successfully demonstrated 30 V switching with the integrated level-shift circuits and series-connected transistors. The total dimensions of the device were 400×640 μm^2. Finally, we demonstrated the dynamic driving of a MEMS actuator with the switching device and a 10 μm displacement was obtained, which indicates the usefulness of the high-voltage switch circuit for MEMS actuator driving applications.

3.3. High-Voltage Generator

3.3.1 Introduction

High-voltage (HV) generators are widely used in driving not only a micropump but also today's electronic devices. Especially a voltage multiplier, such as a charge pump, is commonly used to obtain HV on a chip. The maximum voltage of the multipliers is limited by two factors: the breakdown voltages of parasitic diodes and the loss of threshold voltages of switching devices, as shown in Fig. 3.16a. Even though there exist several methods to sustain an HV, the standard CMOS technology for a low-voltage logic circuit has a fundamental limit of 50 V ($10 \times V_{DD}$) owing to the breakdown voltages of parasitic diodes. HV CMOS technologies, such as the lateral-diffused MOS (LDMOS) structure in Teledyne DALSA 0.8 μm HV CMOS process [70], [71] , are commonly used for HV generators having an endurance voltage greater than 100 V. However, the threshold voltages of these high-voltage devices are greater than those of standard CMOS devices. Besides, the threshold voltage increases as the applied body bias increases. Consequently, the increment of the HV generator degrades. Therefore, another method is required to improve the increment of the HV generator.

One method to decrease the loss of HV generators' increment is the use of non-MOS devices such as poly-silicon diodes in the standard CMOS process [91]. The other method

is to isolate each diode-connected transistor or MOS body diode by a deep N-well in standard CMOS technology [92] or by a buried oxide (BOX) SiO_2 layer in fully-depleted SOI (FDSOI) technology [93]. These methods can eliminate the body effect, and the threshold voltages are low. However, owing to the breakdown of a parasitic diode between P-substrate and N-well or a capacitor of a thin BOX layer, the maximum voltage of these

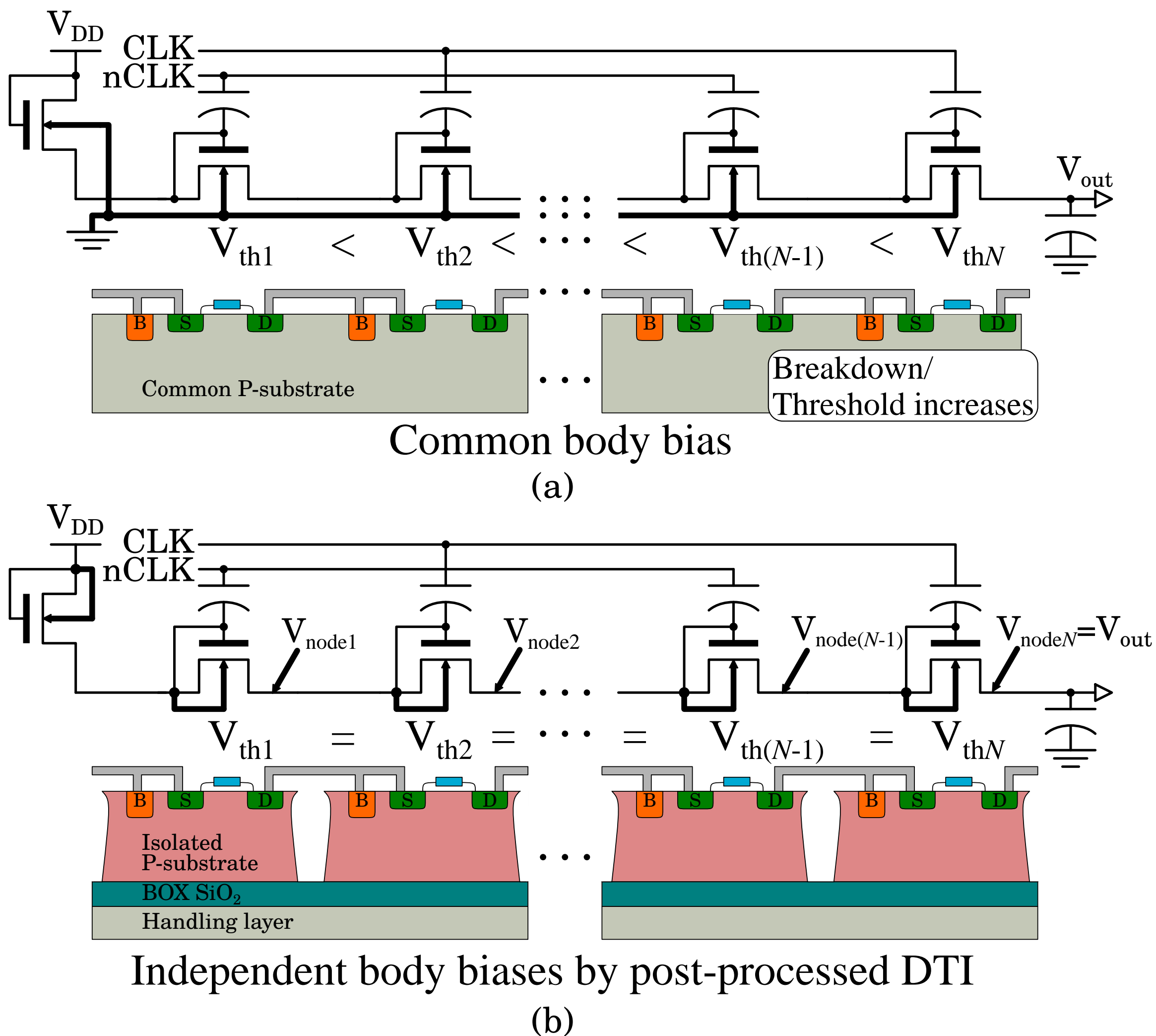


Fig. 3.16: (a) Dickson charge pump with non-isolated N-channel MOSFETs (NMOSFETs). Since the entire body is common, the threshold voltage increases as the number of stages increases owing to the body effect. (b) Dickson charge pump with deep-trench-isolated NMOSFETs. Deep-trench-isolation (DTI) separates each substrate and eliminates the body effect.

methods is 60 V, which is still small for MEMS or micropumps.

In this section, we applied post-processed DTI to standard low-voltage logic transistors for a high-increment HV generator, as shown in Fig. 3.16b. This technology can hold the same voltage level as the previous DTI process [81],[94]. Moreover,it enables us to etch out the substrate below wires on the wafers, where CMOS devices have already been fabricated through the standard CMOS process. The proposed method allows us to fabricate the devices through a low-cost foundry without any process modifications. Besides, owing to the application of DTI isolation to logic CMOS devices, threshold voltages can be limited, and the body bias voltage of each transistor can be set to zero, as shown in Fig. 3.16b. This method can realize a high-increment HV generator for an HV-requiring MEMS device (e.g., EOF micropump). We report a 100-V-class HV-generating charge-pump circuit using the standard low-voltage CMOS technology and the post-processed DTI technology. By connecting the HV generator with wires, we demonstrated the driving of an external EOF micropump.

3.3.2 Dickson charge pump using post-processed DTI transistors

3.3.2.1 Circuit implementation and fabrication

We used Dickson charge-pump circuit topology [95] as the schematic of an HV generator. The Dickson charge pump is derived from the ideal diode charge pump architecture using diode-connected MOS transistors. The circuit output voltage can be simply described as

$$V_{\mathrm{out}} = (N + 1) \cdot (V_{\mathrm{DD}} - V_{\mathrm{th}}) - \frac{N I_{\mathrm{out}}}{(C + C_S) f_{\mathrm{clk}}} \tag{3.1}$$

where the term $V_{\mathrm{DD}} - V_{\mathrm{th}}$ is called the voltage increment per stage, N is the number of stages in the charge-pump circuit, C is the capacitance of an on-chip pumping capacitor, and C_S is a

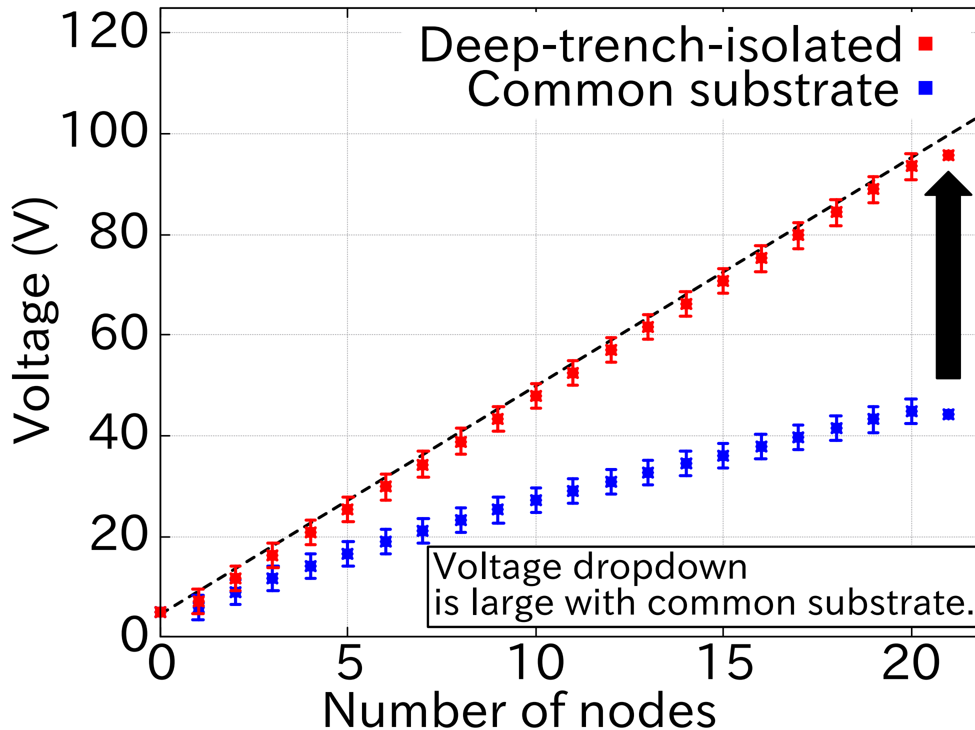
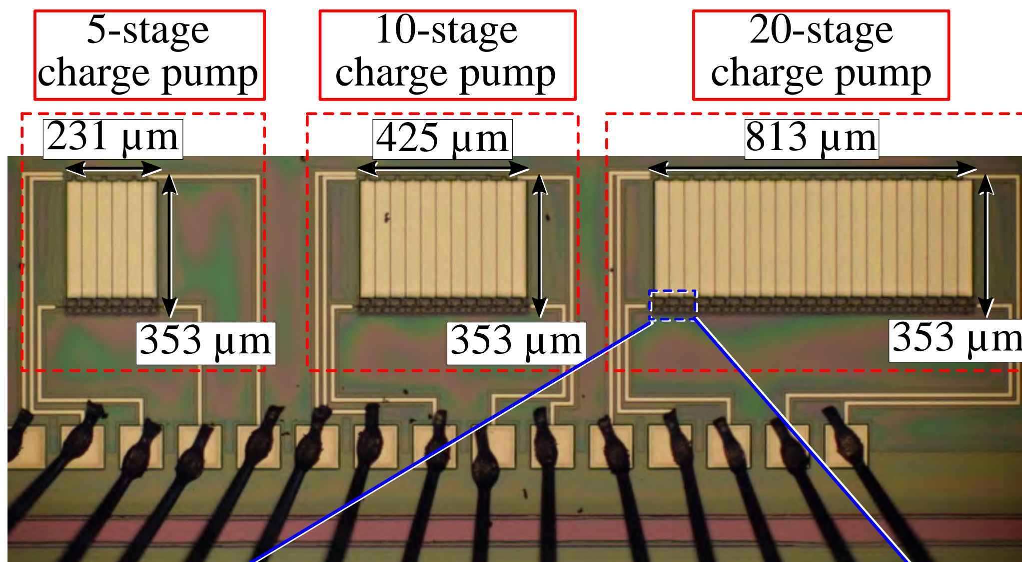


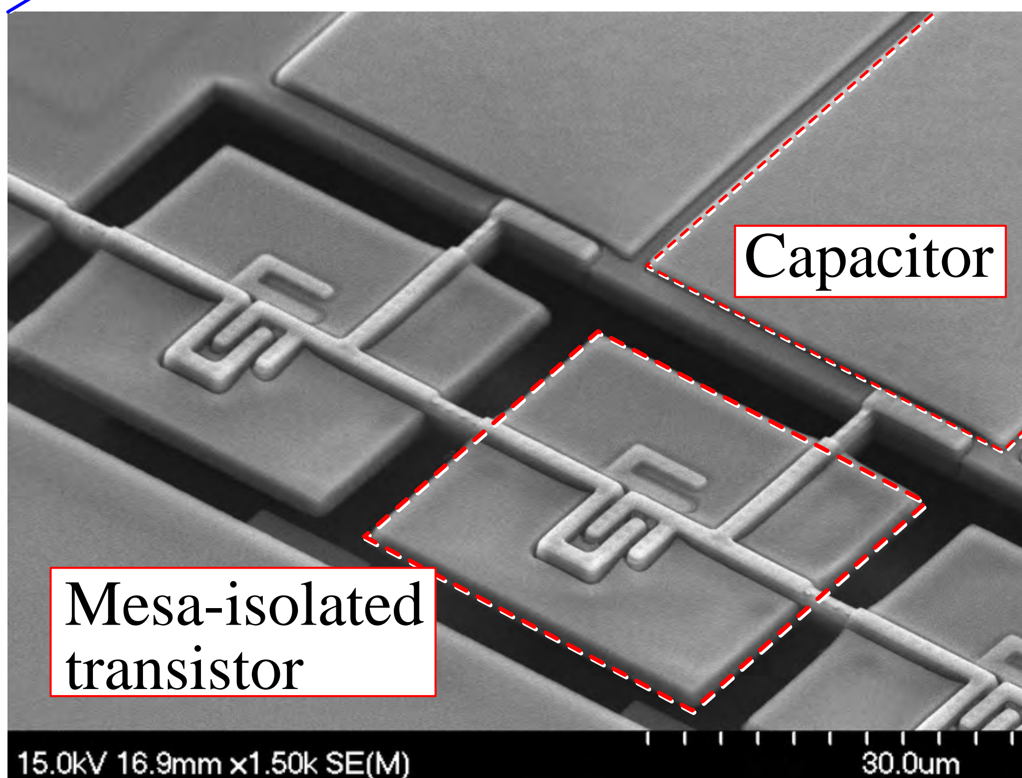
Fig. 3.17: Simulation of voltage increment with the number of nodes of a 20-stage Dickson charge pump with and without DTI, where f_{clk} is 20 MHz and V_{DD} is 5 V. Without DTI, owing to the body effect, the dropout is significant. On the other hand, with DTI, the voltage of each node increases linearly.

parasitic capacitance, and I_{out} is output current. We designed 5-stage, 10-stage, and 20-stage charge pumps. The body is connected to the source in each transistor. The width-to-length ratio of the MOS transistors was designed as 21 μm/0.6 μm, and the capacitance of the on-chip pumping capacitors was 1.3 pF using metal-1, metal-2, and poly-silicon layers.

Figure 3.17 shows the results of simulations of voltage increment with the number of nodes of 20-stage Dickson charge pumps with and without DTI, where the clock frequency f_{clk} is 20 MHz, and V_{DD} is 5 V. Without DTI, owing to the body effect, the dropout increases as the number of nodes increases. On the other hand, with DTI, the output voltage of each stage increases linearly, and the output voltage in the simulation is 95.8 V. According to the simulation result, the voltage difference between the P-well and N-diff is always less than



(a)



(b)

Fig. 3.18: (a) Photomicrograph of the fabricated high-voltage generators using mesa-isolating post-processed MOS transistors. (b) Close-up SEM image of a stage of the high-voltage generator.

$V_{PW/N+}$, which is the threshold voltage of a parasitic diode between P-well and N-diff, and these diodes can be ignored.

The CMOS LSI was fabricated by a foundry company using standard 0.6-µm CMOS process technology on an SOI wafer (9 µm-1 µm-625 µm). The detail of the post process was described in [96]. Like the previous study [81], when 800 V is applied to the circuit that has 4 µm-gap post-processed DTI, the breakdown occurs at not the parasitic diodes but random places such as probe pads. This random breakdown means the maximum voltage cannot increase beyond 800 V by changing the trench width. In our design, the trench width was 5 µm to use the etching conditions in [96]. First, the surface SiO_2 and SiN passivation layer was patterned to form a mask. Subsequently, DRIE was performed to form deep trenches. Finally, SF_6 isotropic plasma etching was performed to remove the substrate below the connecting wires. Since the depth of the DRIE was automatically stopped by the BOX layer and the isotropic etching holds the constant ratio between the undercut and the depth [94], the isotropic etching is repeatable. Besides, since the isotropic etching is performed with standard DRIE equipment that is for a wafer-scale process, the process is uniform on a large size wafer. Note that all the wires are masked by the patterned passivation layer so that the post process does not damage the wires. A photomicrograph of the fabricated charge-pump circuits having 5, 10, and 20 stages are shown in Fig. 3.18a. The size of the 20-stage charge-pump circuit was 813×354 µm^2. Figure 3.18(b) shows a close-up SEM micrograph of the fabricated deep-trench-isolated transistors.

3.3.2.2 Charge-pump measurement

Transient waveform measurements of the outputs of the fabricated 5-stage, 10-stage, and 20-stage charge pumps at startup are shown in Fig. 3.19, where f_{clk} is 20 MHz, V_{DD} is 5.0 V and the output load is 10 MΩ and 11.1 pF (including measurement scope loading). The

maximum voltages of the 5-stage, 10-stage, and 20-stage charge pumps were 26.9 V, 49.8 V, and 95.2 V, respectively. Figure 3.20 shows the dependence of the measured output voltages on the number of the stages with an output loading of 10 MΩ, where f_{clk} is 20 MHz, and V_{DD} is 5 V. The increment per stage was 4.47–4.53 V.

Figure 3.21 shows the measured output voltages of the fabricated charge-pump circuits with different f_{clk}, where V_{DD} is 5 V, with an output loading of 10 MΩ. When f_{clk} is increased, the output voltages are also increased. Figure 3.22 shows the measured output voltages of the fabricated charge-pump circuits under different V_{DD}. In Fig. 3.22, f_{clk} is 20 MHz, and the output loading is 10 MΩ. Finally, Figure 3.23 shows the I/V DC characteristics of the fabricated 5-stage charge pump. The clock frequency is 20 MHz, and V_{DD} is 5 V. As shown in Fig. 3.23, the charge-pump circuit is sufficient to drive a MEMS actuator, the typical load current of which is less than 20 μA.

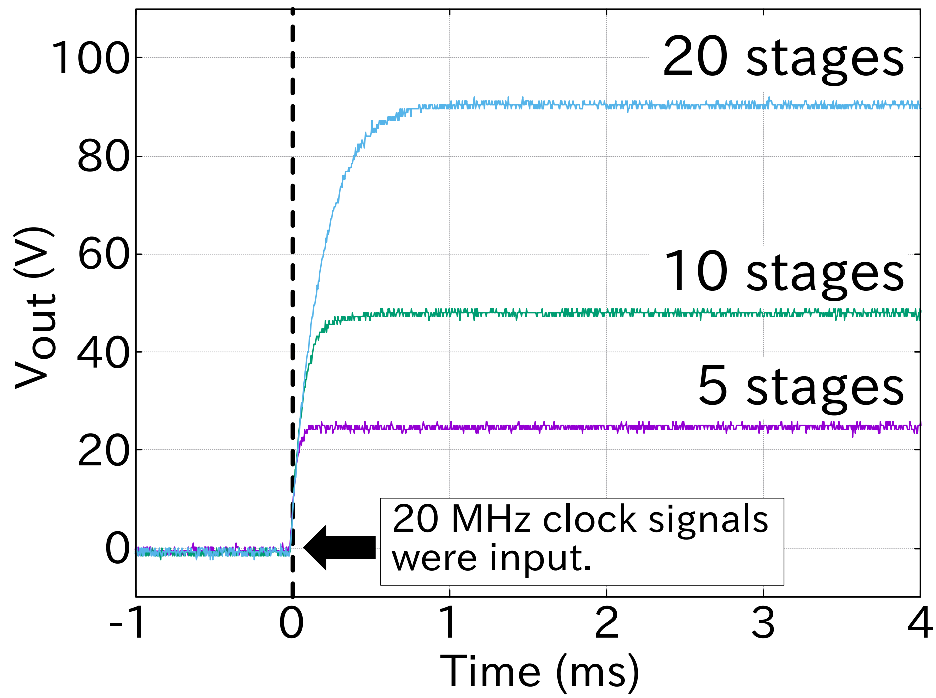


Fig. 3.19: Voltage waveforms for charge path, where f_{clk} is 20 MHz, and V_{DD} is 5 V.

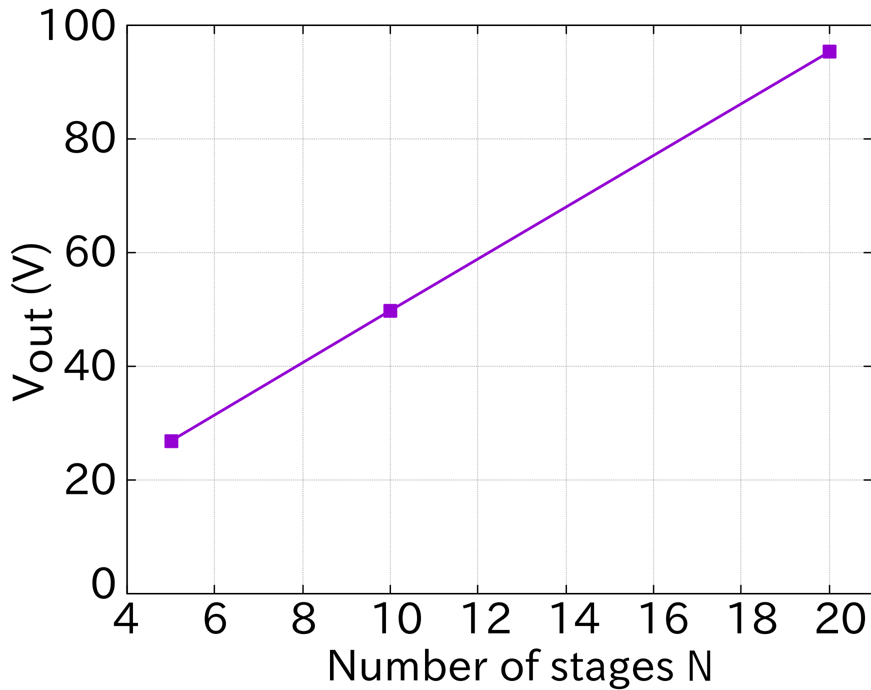


Fig. 3.20: Dependence of output voltages on the number of the stages, where f_{clk} is 20 MHz, and V_{DD} is 5 V.

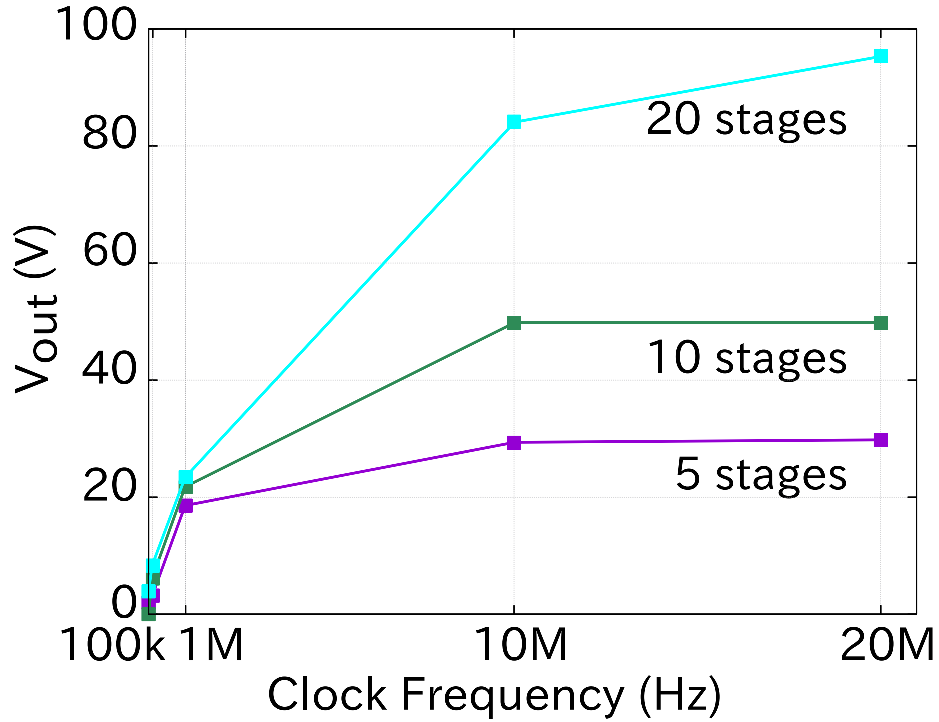


Fig. 3.21: Measured output voltages of the charge-pump circuits with an output loading of 10 MΩ (a) under different clock frequencies where the power-supply voltage V_{DD} is 5.0 V.

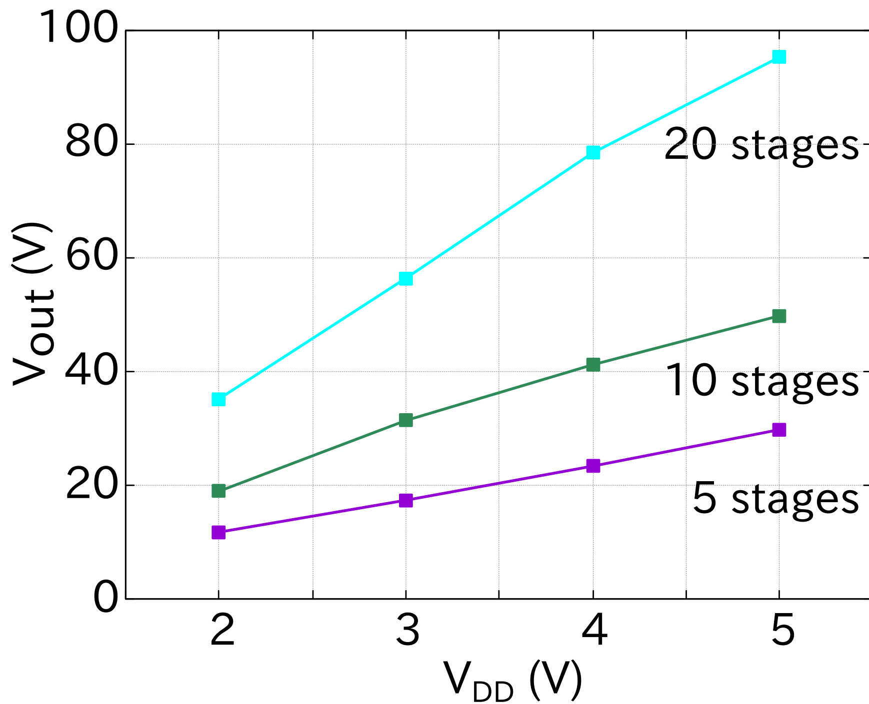


Fig. 3.22: Measured output voltages of the charge-pump circuits with an output loading of 10 MΩ under different V_{DD}, where the clock frequency f_{clk} is 20 MHz.

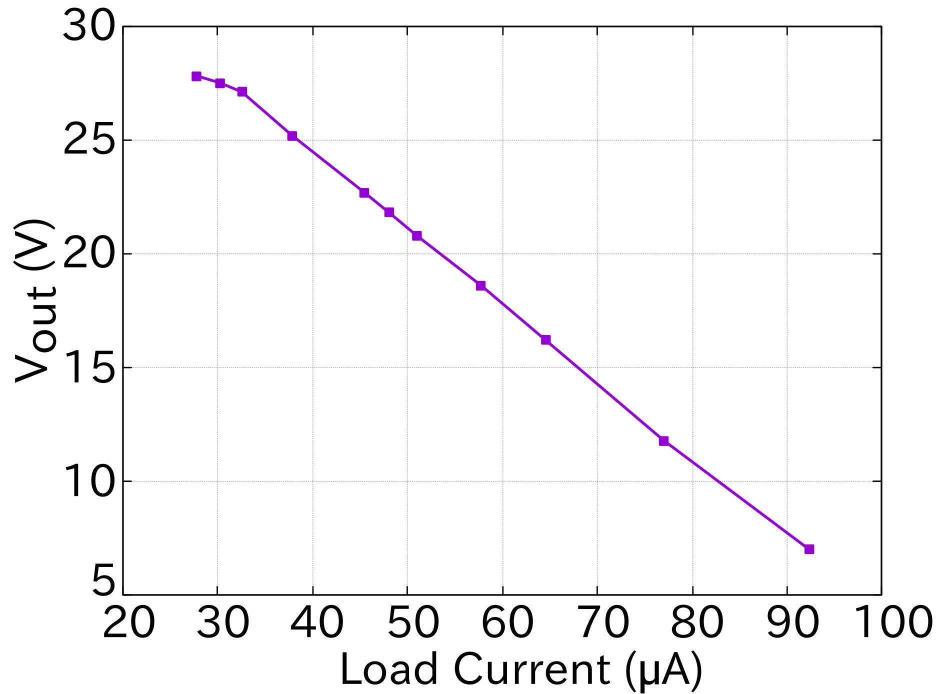


Fig. 3.23: I/V DC characteristics of the fabricated 5-stage charge pump. The clock frequency is 20 MHz, and V_{DD} is 5 V.

3.3.2.3 Driving a MEMS micropump

To assess the feasibility of the high voltage generator, the circuits were connected to a discrete EOF micropump under microscope observation, as shown in Fig. 3.24. The flow rate (u_{eof}) of the EOF micropump is described as Eq. 1.1 From the equation, the flow rate is proportional to the number of stages in a charge pump. The EOF micropump was made with poly-dimethylsiloxane (PDMS), and the channel length, width, and height were 10 mm, 200 μm, and 100 μm, respectively. In the EOF micropump, the solution was 1 mM 4-(2-HydroxyEthyl)-1-PiperazineEthaneSulfonic acid (HEPES) buffer with a pH of 7. Figure 3.25 shows the discrete EOF micropump operation by the 20-stage HV generator supply. The flow speed of the discrete EOF micropump at 95.2 V was 135 μm/s. The linear relationship of flow speed to the number of HV generator stages (i.e., output voltages) was

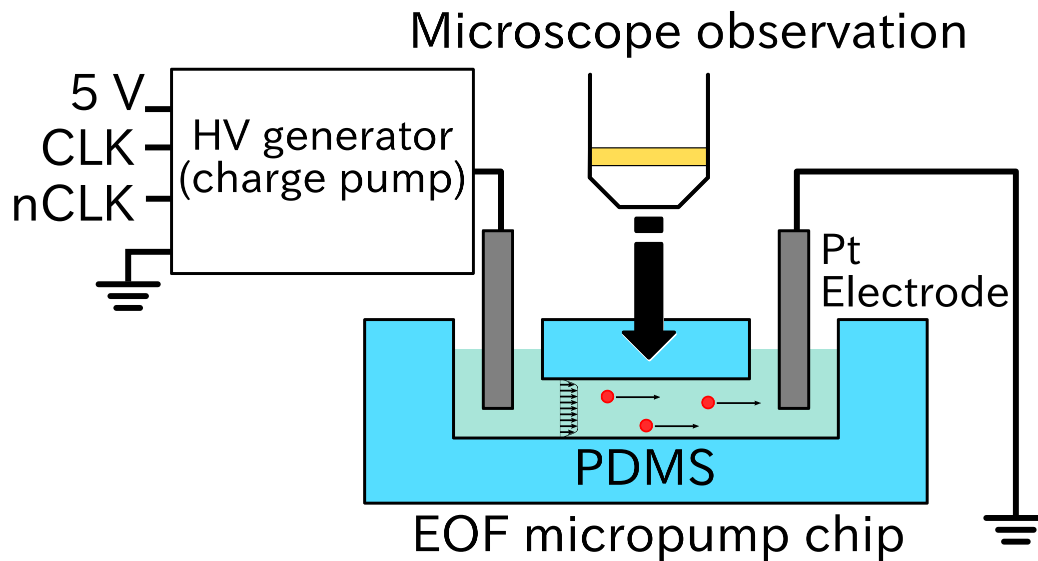


Fig. 3.24: Setup of external EOF micropump driving experiment.

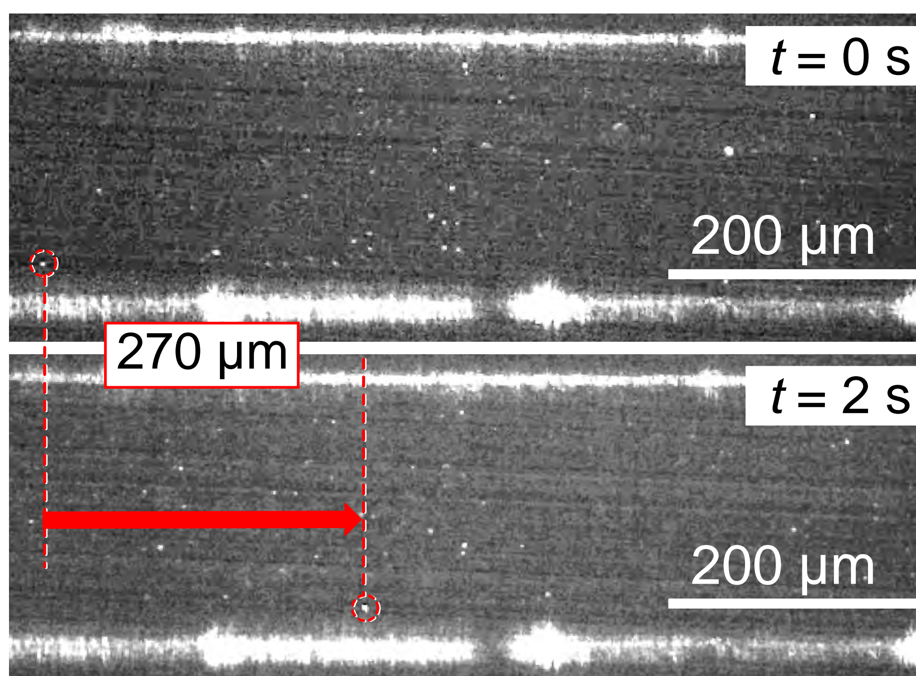


Fig. 3.25: Micrographs of the discrete EOF micropump supplied from the 20-stage charge pump. The flow speed was 135 μm/s.

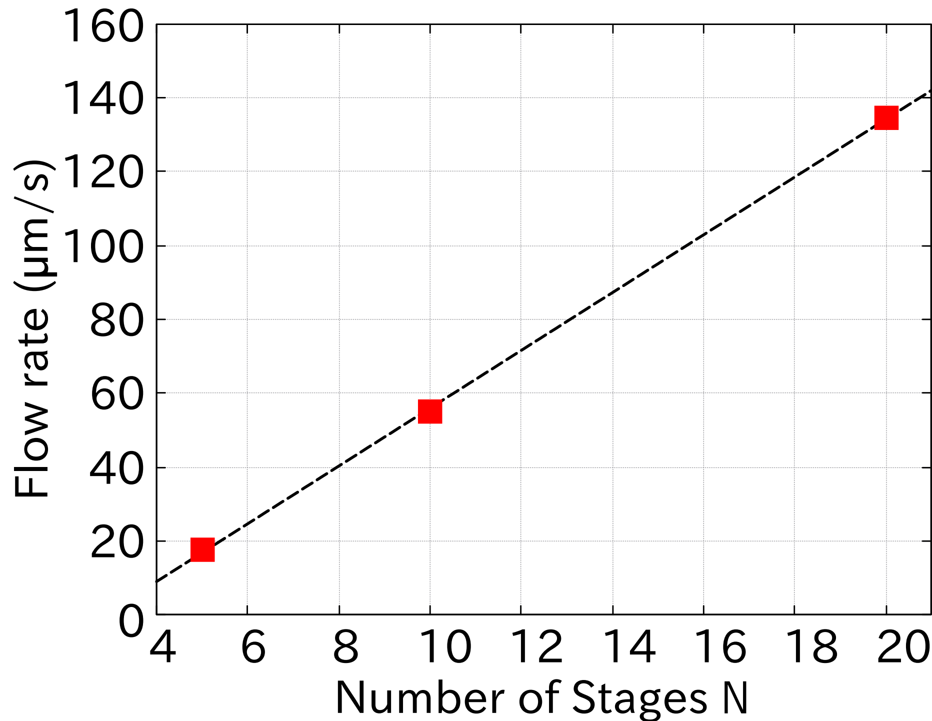


Fig. 3.26: Supply-voltage dependence of the discrete EOF micropump flow speed.

confirmed as shown in Fig. 3.26, demonstrating the scalability of the circuits.

3.3.3 Summary

We designed 5-stage, 10-stage, and 20-stage charge-pump circuits with post-processed deep-trench-isolated transistors through the commercial 5 V 0.6 μm CMOS process on SOI and MEMS post-processing. When the output load was 10 MΩ, the output voltage was 95.2 V with a power supply of 5 V, and the increment per stage of the charge pump was 4.47–4.53 V. Finally, the driving of the EOF micropump supplied by the fabricated charge pumps was demonstrated. The flow rate with the 20-stage charge pump was 135 μm/s.

CHAPTER 4

ON-CHIP INTEGRATED EOF MICROPUMP

Some of the text and the materials of this chapter are based on the articles of the author's group entitled "On-Chip CMOS-MEMS Based Electroosmotic Flow Micropump Integrated with High-Voltage Generator," published in Journal of Microelectromechanical Systems, 2019.

4.1. Introduction

Because of this incompatibility in the voltages, the EOF micropumps are commonly driven by another external high-voltage (HV) power supply, as shown in Fig. 4.1a. This integration facilitates the operation of micropumps using low-voltage power supplies such as tiny batteries and allows us to integrate EOF micropumps with 3DICs.

In this chapter, we have proposed an on-chip EOF micropump, which is monolithically integrated with an HV generator. The EOF micropump and HV generator are fabricated by the standard CMOS process and MEMS post-processing. The driving voltage of the EOF micropump is generated by the integrated circuit with a supply voltage of 5 V. Consequently, the micropump can be solely driven by a low-voltage power supply, as shown in Fig. 4.1b.

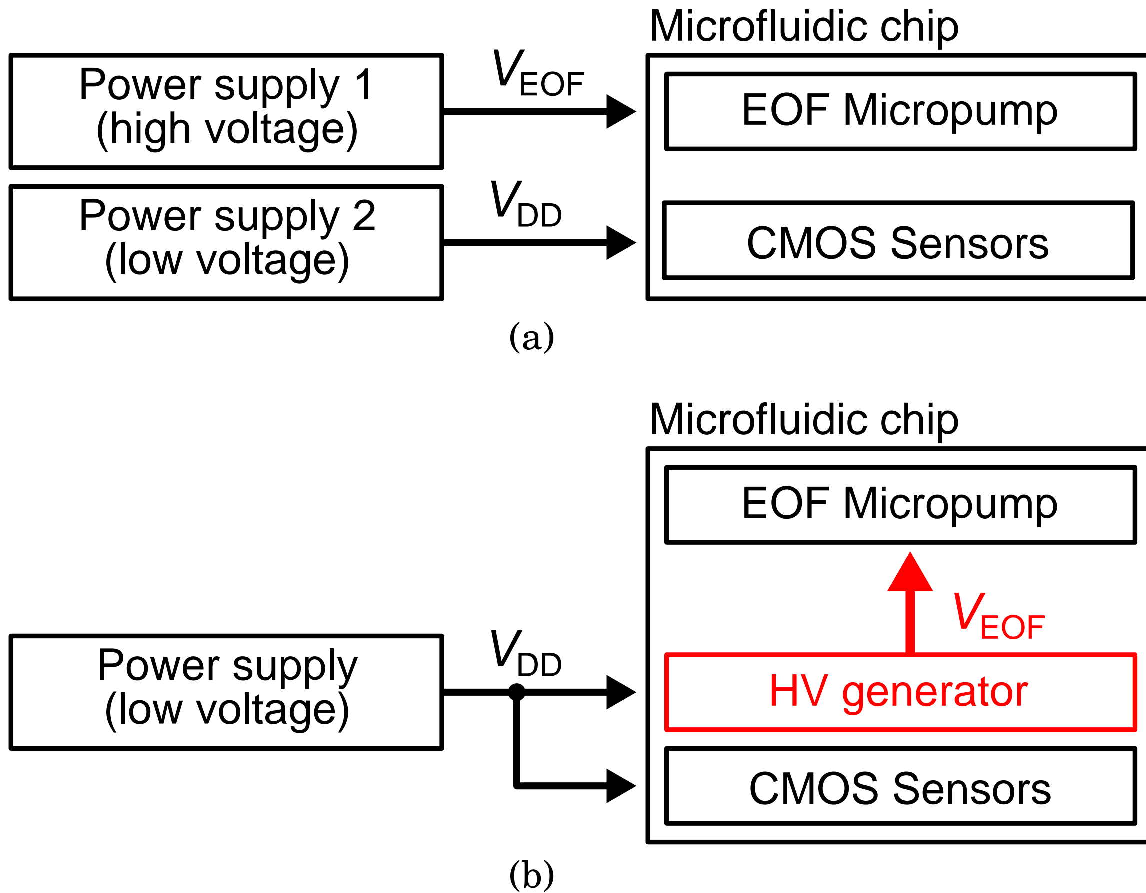


Fig. 4.1: Block diagram of power supplies in the (a) conventional CMOS-integrated microfluidic device and (b) proposed CMOS-integrated microfluidic device. The proposed method facilitates the generation of the EOF driving voltage on a chip by an integrated HV generator.

4.2. Design

The proposed on-chip EOF micropump is composed of an HV generator and two electrodes, as shown in Fig. 4.2. The electrodes are embedded in a micro-channel and connected to the HV generator on the chip. The HV generator is used to obtain higher voltages than the supply voltage of LSI circuits on a chip. The HV generator is based on Dickson charge-pump topology [95]. In the previous chapter, we demonstrated an efficient HV generator using the MEMS post-processed transistors. Although we have proved that

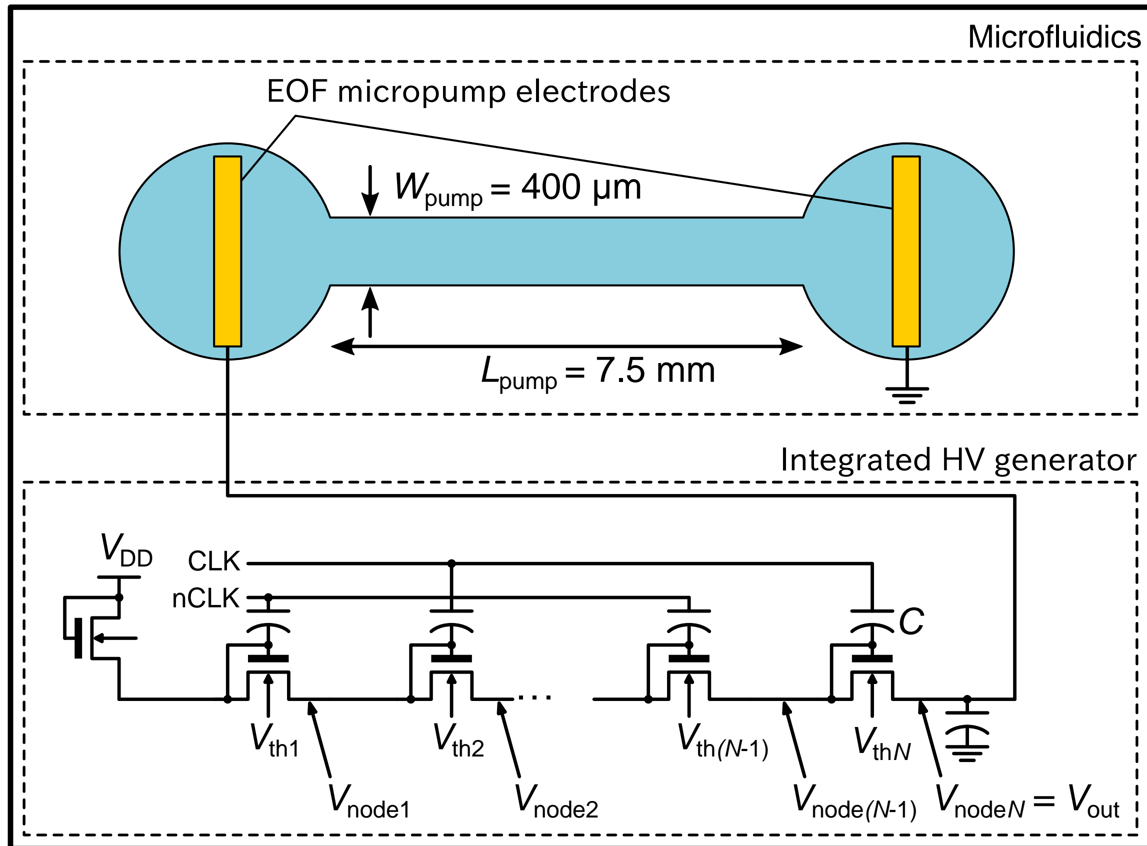


Fig. 4.2: Schematic of the proposed on-chip EOF micropump integrated with an HV generator. The circuit topology of the HV generator is based on a Dickson charge pump.

a high-efficient HV generator can be designed by 5 V CMOS technology and the MEMS post-process, the experiment was performed using an external PDMS micro-channel and bulk Pt electrodes. It means that the monolithic integration of HV driving circuits with micropumps has not been realized yet. Therefore, the demonstration of the monolithic integration of an HV generator is fundamentally crucial for the development of LOC devices. In this chapter, we mainly focus on the monolithic integration method of an HV generator with an EOF micropump.

To demonstrate the monolithic integration, we designed a 10-stage Dickson charge pump using the MEMS post-processed DTI transistor as an on-chip HV driver of the

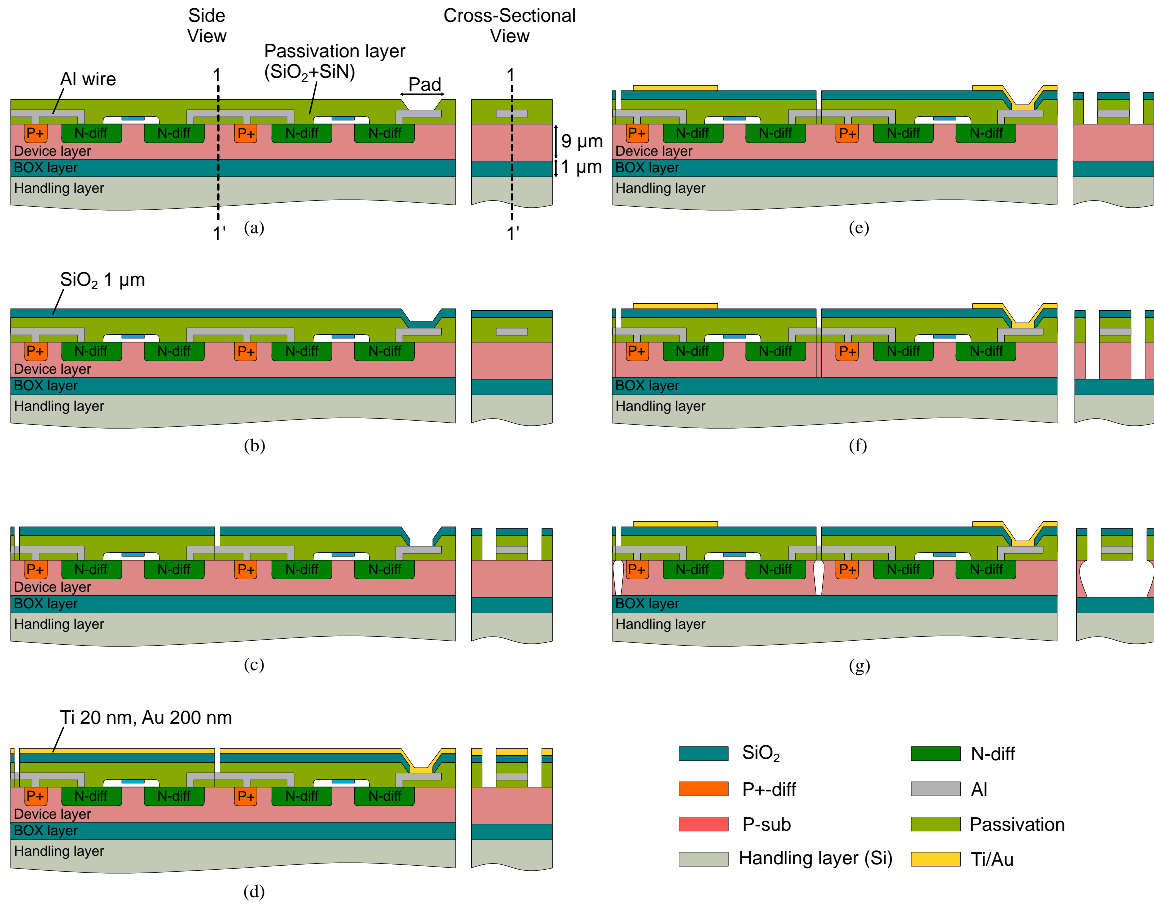
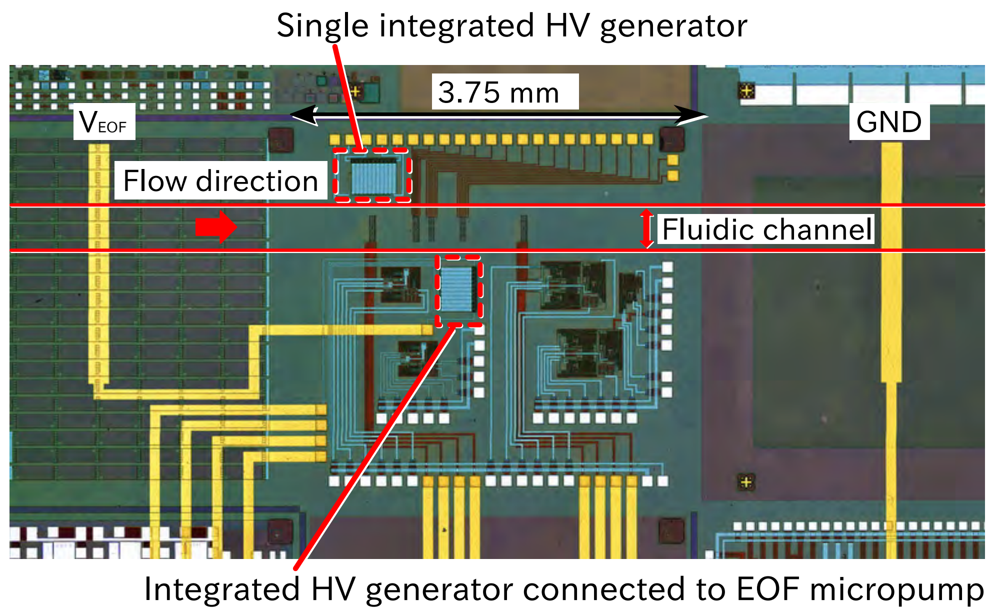
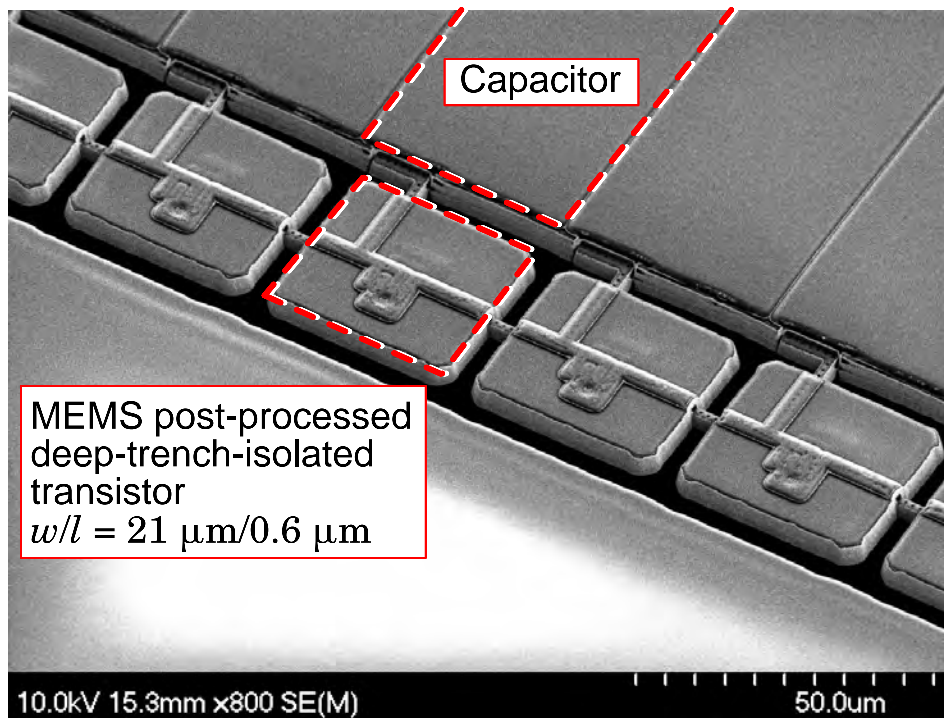


Fig. 4.3: Process flow of the proposed on-chip EOF micropump. (a) CMOS LSI circuits fabricated using a standard CMOS foundry. (b) Sputtering of SiO_2 (c) Patterning of the sputtered SiO_2 and LSI passivation layer to expose the pads and form a mask for MEMS post-processed deep trench isolation. (d) Sputtering of Ti and Au for the electrodes of EOF micropump. (e) Patterning of Ti and Au layers. (f) Deep-reactive-ion etching (DRIE). (g) Isotropic etching of Si body under the Al bridges by SF_6 plasma etching.

EOF micropump, which was based on 0.6 μm, 5 V, 2-metal CMOS technology (Phenitec Semiconductor, Okayama). The length-to-width (l-to-w) ratio of the post-processed DTI transistor was 0.6 μm/21 μm, and the capacitance of the on-chip pumping capacitor was 1.3 pF, which was formed using metal-1, metal-2, and poly-silicon layers. Since the post-process of EOF micropumps is well-combined with the post-process of DTI, the step of DTI formation can be performed just before the encapsulation by the top substrate.



(a)



(b)

Fig. 4.4: (a) Photomicrograph of the fabricated on-chip EOF micropump integrated with an HV generator using MEMS post-processed deep-trench-isolated MOS transistors. (b) Magnified SEM image of the transistors in the integrated HV generator.

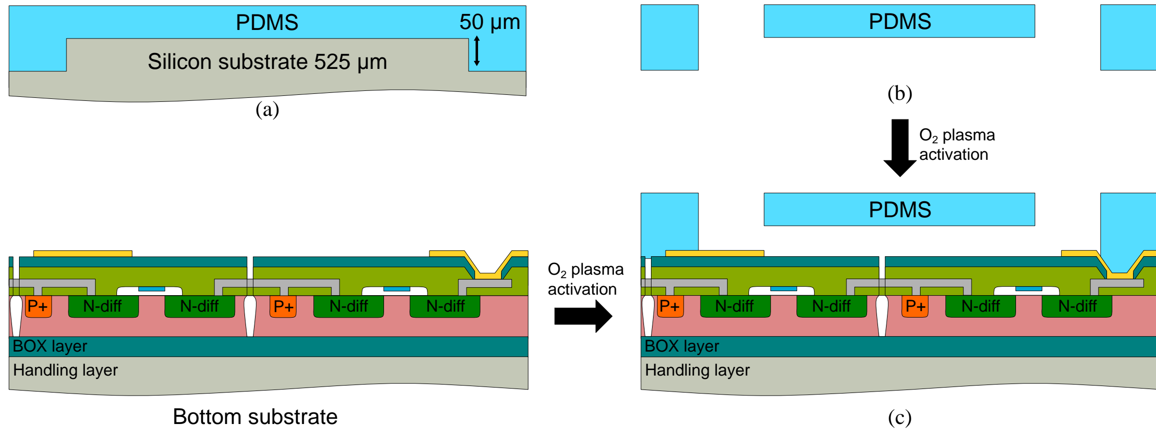


Fig. 4.5: Process flow of a micro-channel on the on-chip EOF micropump. (a) 10:1 mixture of PDMS and curing agent is poured on the Si mold, and it is thermally cured. (b) PDMS is peeled off from the mold, and the inlet and outlet holes are punched. (c) Both the top and bottom substrate are activated by O_2 plasma ashing, which are then bonded.

4.3. Fabrication

4.3.1 Fabrication of EOF electrodes

The CMOS LSI circuit was fabricated by a foundry company using the standard 0.6-µm CMOS technology on an SOI wafer (9 µm - 1 µm - 625 µm) through multi-project wafer (MPW) service (Fig. 4.3a). In our design, the trench width was set as 5 µm to replicate the etching conditions in [96]. We diced the wafer into 1.5×1.5 mm^2 chips, which also contained irrelevant circuits. Firstly, an insulating layer was deposited on the chip. Here, 1-µm-thick SiO_2 was sputtered (SIH-450, ULVAC) as the insulating layer (Fig. 4.3b). Subsequently, a thick photoresist (AZ P4620, Merck KGaA) was patterned on the SiO_2 layer using a contact mask aligner (MA-6, Karl Suss). Both the deposited SiO_2 layer and LSI passivation layer composed of SiO_2 and SiN were dry-etched by CHF_3 plasma (CE-300I, ULVAC), as shown in Fig. 4.3c. The necessary contact, i.e., Al pads were exposed to the surface by patterning this insulating layer, and the mask for the post-processed DTI was formed.

Next, 20-µm-thick Ti and 200-µm-thick Au were sputtered (CFS-4EP-LL, SHIBAURA) (Fig. 4.3d). The photoresist (7790g, JSR) was patterned by the same contact lithography machine. Au was then dry-etched by Ar plasma (CE-300I, ULVAC), as shown in Fig. 4.3e. Finally, the Ti layer was wet-etched by 5% ammonia-peroxide mixture (APM).

4.3.2 MEMS post-processed DTI

Firstly, the chip was cleaned by O_2 plasma ashing (RIE-10NR, SAMCO) to remove the photoresist. Then, deep reactive ion etching (DRIE) was performed to form deep trenches (MUC21-ASE Pegasus, SPP Technologies), as shown in Fig. 4.3f. DRIE was automatically stopped at the buried-oxide (BOX) layer to maintain a constant depth. O_2 plasma ashing was performed with the same DRIE equipment to remove the C_4F_8 layer in the trenches formed during the DRIE. Finally, SF_6 isotropic plasma etching was performed for etching the remaining silicon substrate below the connecting wires to completely isolate the transistors from each other (Fig. 4.3g). This isotropic etching was implemented based on the constant ratio between the undercut and the depth of the trenches, and the etching was repeatable. The isotropic etching was also performed with the same DRIE equipment as that used for the wafer-scaling process, and the process is applicable to large-size wafers. It is important to note that all the connecting wires in the circuit were fabricated by the CMOS process at the foundry company; these were protected by the passivation layer, and the MEMS post-processing did not cause any damage to the wires. Finally, after cleaning the chip by O_2 ashing, the chip was baked at 350 °C for two hours to eliminate the remaining electric charges in the transistors generated by plasma dry etching. Figure 4.4a shows the fabricated EOF micropump chip monolithically integrated with the MEMS post-processed charge pump. The size of the 10-stage charge-pump circuit was 425×353 µm^2. Figure 4.4b shows

a magnified SEM image of the fabricated deep-trench-isolated transistors in the charge pump.

4.3.3 Fabrication of micro-channel

Polydimethylsiloxane (PDMS) was used as a cover for the micro-channel. The micro-channel was patterned by a soft lithography method using a Si mold. To fabricate the silicon mold, a thick electron beam (EB) resist (OEBR-CAP112, TOK) was patterned on a 525-μm-thick Si wafer using rapid direct EB writer (F5112+VD01, ADVANTEST) as a mask. The Si wafer was deep etched by 50 μm using the DRIE equipment (MUC21-ASE Pegasus, SPP Technologies). The EB resist and the deposited C_4F_8 were then removed by O_2 ashing. The wafer was dipped into a fluorinated mold-release coating agent (SURECO 2101S, AGC) and rinsed by a fluorinated solvent (AE-3000, AGC) so that it could be easily peeled off. The wafer was baked at 120°C for 20 min to increase the adhesivity of the coating agent. After fabricating the silicon mold, a 10:1 mixture of PDMS (Sylgard 184, Dow Corning) and the curing agent was poured on the mold (Fig. 4.5a). The PDMS was vacuumed for one hour and cured at 90°C for two hours. The cured PDMS was peeled off, and then the inlet and outlet holes were punched (Fig. 4.5b). Subsequently, the fabricated post-processed CMOS LSI chip and PDMS were cleaned by isopropyl alcohol. Finally, these were bonded using O_2 plasma surface activation (FA-1, SAMCO), as shown in Fig. 4.5c.

4.4. Results and Discussion

4.4.1 Integrated HV generator

To investigate the characteristics of the fabricated HV generator, we first measured its output voltage V_{out} independently, while it was not connected to the EOF electrodes, as shown in Fig. 4.4. Figure 4.6 shows the transient waveform of the HV generator, where f_{clk} = 20 MHz, V_{DD} = 5.0 V, and the output load is equal to 10 MΩ and 11.1 pF, which includes the parasitic load of the oscilloscope. Figure 4.7 shows V_{out} of the fabricated HV generator under different V_{DD}, where f_{clk} = 20 MHz and the output load is 10 MΩ and 11.1 pF. It is evident here V_{out} is ten times larger than V_{DD}. Although V_{out} depends on the f_{clk}, it does not change for $f_{clk} > 10$ MHz since the loss in Eq. 3.1 becomes neglectable. In the experiment, we set the clock frequency to 20 MHz, since the previous study of driving an external EOF micropump in [97] used the same frequency. The maximum voltage of the HV generator is 49.8 V, where f_{clk} = 20 MHz, and V_{DD} = 5.0 V.

4.4.2 On-chip EOF micropump

We measured the flow velocity of the on-chip EOF micropump driven by the integrated HV generator. Figure 4.8 shows a schematic of the experimental setup for this measurement. We injected 1.0×10^{-4}M KCl solution having a pH of 7 into the micro-channel from the inlet hole using a micro pipette. We also injected charge-free micro beads to measure the flow velocity using an optical microscope. The micro beads are composed of latex particles coated with hydroxypropyl cellulose and used to measure the EOF velocity without electrophoresis effects [98]. The concentration of the micro beads is 5%.

We applied 5 V, 20 MHz clock signals to the integrated HV generator using an external

power supply. We measured the flow velocity three times in each V_{DD}. From Eq. 1.1 and Fig. 1.7, the flow velocity (u_{total}) is expressed as

$$u_{\mathrm{total}} = -\frac{\varepsilon_{\mathrm{r}}\varepsilon_0\zeta}{\mu}\frac{V_{\mathrm{EOF}}}{L_{\mathrm{pump}}} - u_{\mathrm{back}} \tag{4.1}$$

During the measurement, there was a counter flow (u_{back}) of 0.577 µm/s without applying voltages. In each measurement, A video was recorded, and micro-bead velocities are measured by tracking the micro-bead positions manually using the software ImageJ (https://imagej.net/). The flow rate is determined by the average velocity of three micro beads, as shown in Fig. 4.9. Then, we changed V_{out} of the HV generator by varying the V_{DD} for validating the efficiency and accuracy of the integrated HV generator. Figure 4.10 shows the dependence of V_{DD} on the flow velocity (u_{total}). It is clear here that the flow velocity is proportional to the output voltage of the integrated HV generator. Here, the maximum flow velocity was 137 µm/s. Gray-colored dashed line is the fitting line following Eq. 4.1.

Table 4.1 shows the comparison between the previously reported CMOS-compatible EOF micropumps and the proposed micropump. It is evident here that the proposed EOF micropump generates the highest flow rate with an input voltage of 5 V, except for the EOF micropump with the input voltage of 400 V, requiring a HV power supply. Moreover, from the viewpoint of the efficiency, which is defined as the normalized flow rate per supplied voltage, the proposed EOF micropump has the higher score than previous works.

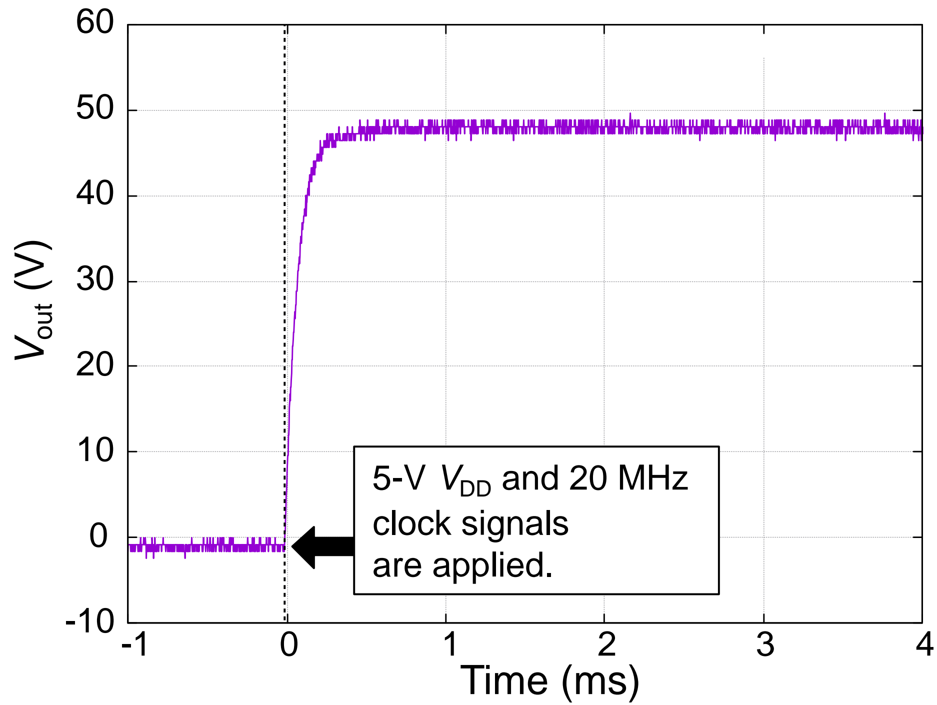


Fig. 4.6: Voltage waveform of the integrated HV generator for the charge path in the absence of micropump electrodes, where f_{clk} = 20 MHz and V_{DD} = 5 V.

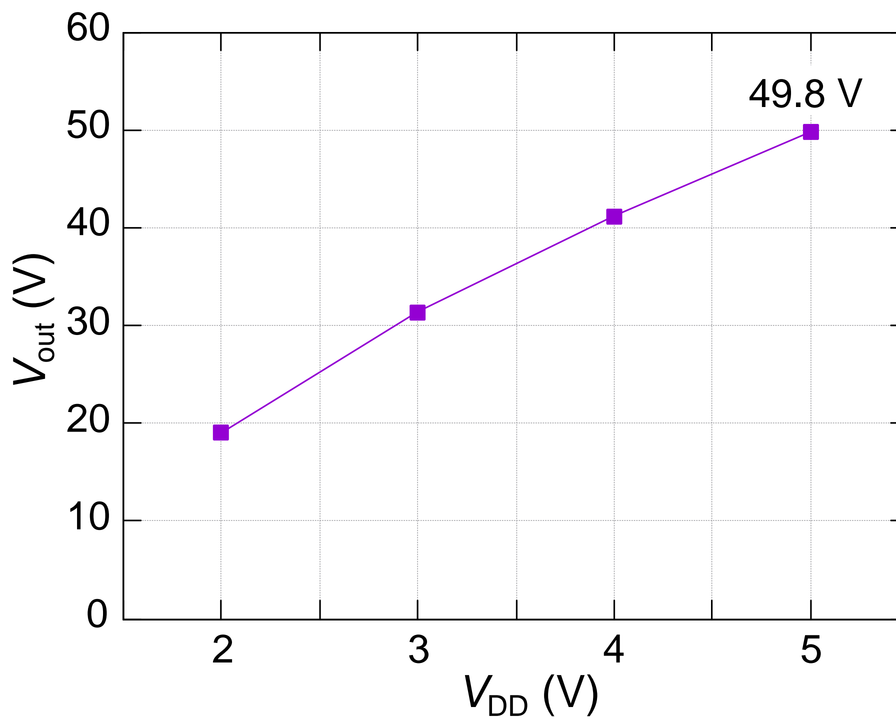


Fig. 4.7: Measured output voltage (V_{out}) of the integrated HV generator with an output loading of 10 MΩ under different V_{DD}. The clock frequency (f_{clk}) is set to 20 MHz.

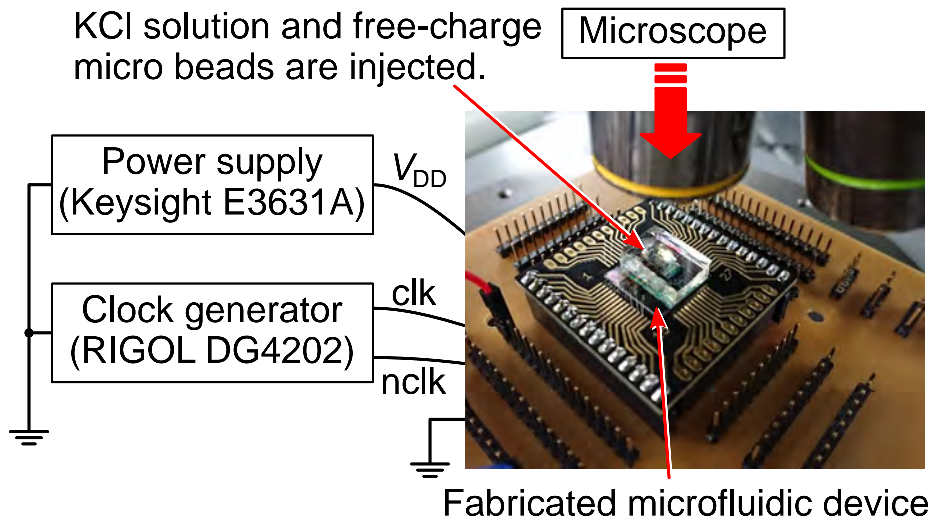


Fig. 4.8: Schematic of the experimental setup for measuring the flow rate of the fabricated device.

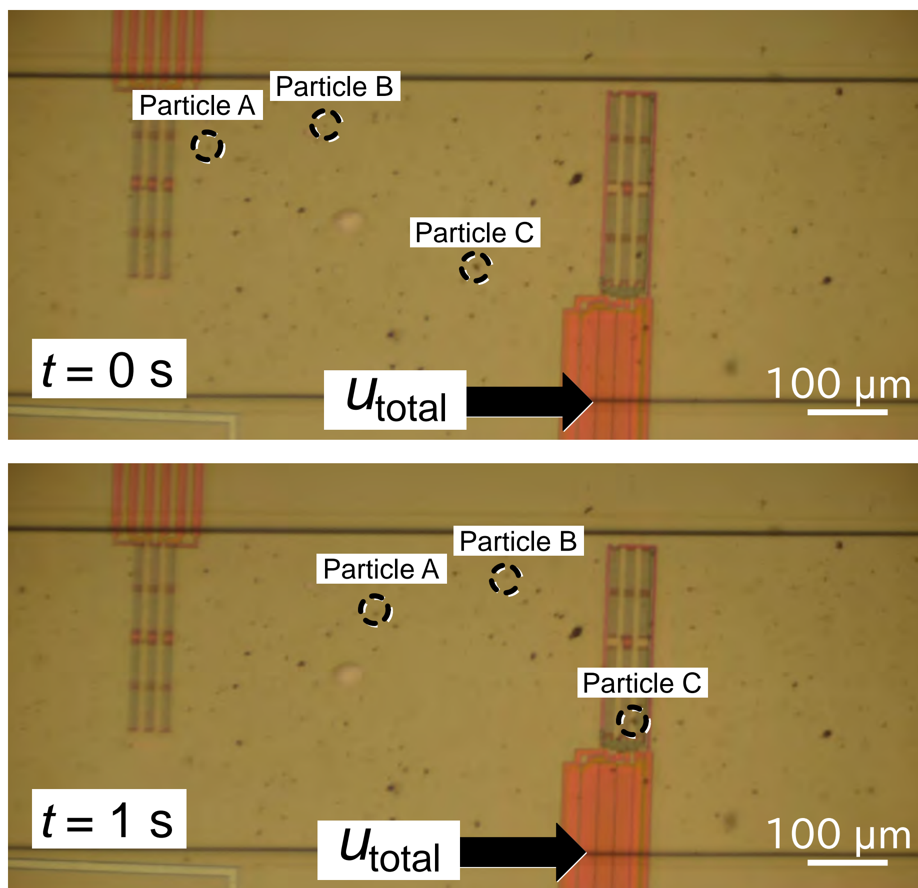


Fig. 4.9: Micrographs of the EOF micropump driven by the integrated HV generator for $V_{DD} = 5$ V. Velocities of three micro beads are measured.

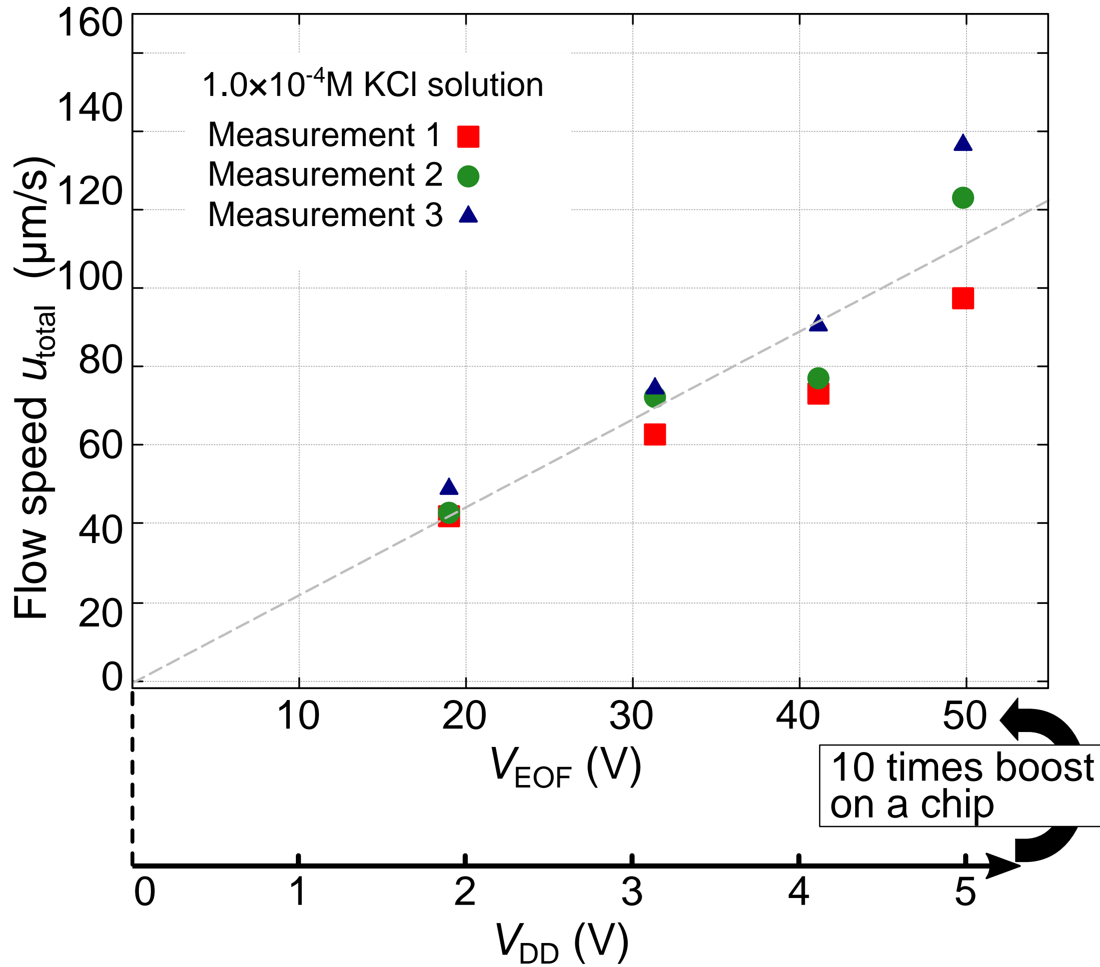


Fig. 4.10: Dependence of driving voltage (V_{EOF}) on flow velocity of the fabricated EOF micropump, where f_{clk} = 20 MHz. V_{EOF} is boosted from V_{DD} by the integrated HV generator.

Table 4.1: Performance comparison between the previously reported CMOS-compatible EOF micropumps and the proposed micropump.

	Laser, 2003 [48]	Seibel, 2008 [45]	Eng, 2010 [47]	This work
Channel material	Oxidized Si	Si, SU-8, Glass	Oxidized Si	SiO_2 sputtered Si, PDMS
HV power supply	Required	Required	NOT required	NOT required
Channel dimension $W \times H \times L$ (μm^3)	$28 \times 70 \times 100$	$3 \times 15 \times 100$	$40 \times 30 \times 2000$	$400 \times 50 \times 7500$
Flow velocity (μm/sec)	$2.8{\times}10^4$	120	18.5	137
Flow rate per channel (nL/min)	340	0.263	1.35	164
Normal. flow rate per channel (μL/cm^2·min)	$2.43{\times}10^4$	584	111	820
Total flow rate (nL/min)	170×10^3 (500 channels)	10.0 (38 channels)	203 (152 channels)	164 (1 channel)
EOF driving voltage V_{EOF} (V)	400	40	4	49.8
Supplied voltage V_{DD} (V)	400	40	4	5
Efficiency of flow per V_{DD} (μL/cm^2·min·V)	60.8	14.6	27.8	164

4.5. Summary

In this chapter, we have proposed a novel on-chip micropump integrated with an HV generator. The HV (49.8 V) generator was based on the Dickson charge pump and fabricated on a silicon-on-insulator (SOI) substrate by the standard CMOS process, and they were isolated from each other by MEMS-post-processed DTI. We confirmed that the integrated HV generator could generate an output 49.8 V with a 5 V supply. The maximum flow velocity and flow rate of the EOF micropump driven by the integrated 49.8 V generator were 137 μm/s and 164 nL/min, respectively. As the micropump can be fabricated through standard CMOS technologies and MEMS post-process, our micropump has a more significant potential of integration with CMOS sensors. Further, compared to the previously reported CMOS-compatible micropumps, the efficiency of our micropump is higher without using an HV power supply. It indicates that the proposed micropump is suitable for portable LOC devices to monitor liquids with a high flow rate.

CHAPTER 5

Integrated Zeta Potential Measurement Sensor

Some of the text and the materials of this chapter are based on the articles of the author's group entitled "Stick-to-Analyze Zeta Potential Measurement Chip with Integrated Electroosmotic Micropump and Liquid Flow Sensor," published in the proceedings of The 32th IEEE International Conference on Micro Electro Mechanical Systems (IEEE MEMS 2019), Seoul, Korea, 2019.

5.1. Introduction

As mentioned above, one of the essential parameters in EOF micropumps is zeta potential. Zeta potential is electrostatic potential at the boundary between the stern layer and diffuse layer. Zeta potential is related to not only the electrokinetic applications but also biomedical polymers [99]. Because of its importance, several measuring methods are proposed to evaluate zeta potential, e.g., by measuring the mobility of EOF and by measuring the streaming current generated by an external force such as pressure-driven flow [100]. Amongst the evaluating methods, measuring the mobility of EOF is the most common method through Eq. 1.1.

Despite the simple measurement of u_{EOF}, the conventional zeta potential measurement system is bulky and often requires high voltage (over 100 V). Arulanandam [101] used over 1000 V to measure the EOF velocity by monitoring the electrical current during one solution replacing another solution using a long capillary. Although Sze developed the system with a microfluidic chip, the applied voltage was still higher than 200 V. On the other hand, the methods proposed by Song [102] and Ross [103] do not need such a high voltage to measure zeta potential. However, these methods require an external liquid controller or laser microscope to trace a microbead. In addition, replacing the surface material is hard, so that measuring several objects are time-consuming. Therefore, another measurement sensor is required to scale down the zeta potential measurement system and to increase the throughput of measurement.

In this chapter, we propose to integrate a micromachined liquid sensor with an EOF micropump into a micro-channel. As a liquid flow-rate sensor, we used a resistive type sensor that can observe the flow-rate electrically by measuring the change of resistance. The sensor can be integrated on a microfluidic channel [104]. To realize more precise measurements, we performed a differential measurement of two resistive sensors and put a reference heat at the center. The advantages of the proposed sensor are (1) stand-alone measurement by the integrated sensor-actuator, (2) reduction of EOF voltage (less than 10 V) due to the scaled-down feature, and (3) non-invasive measurement that enables us to investigate wafers before MEMS process shown in Fig. 5.1. Non-invasive measurement is also a significant feature because it informs the real property of the processed wafer to engineers, thereby ensuring the correct operation of the fabricated fluidic MEMS. The sensor and the EOF micropump have CMOS process compatibility [105]. Besides, CMOS LSIs on a thick-SOI wafer is well studied, and the possibility of MEMS post-process to the

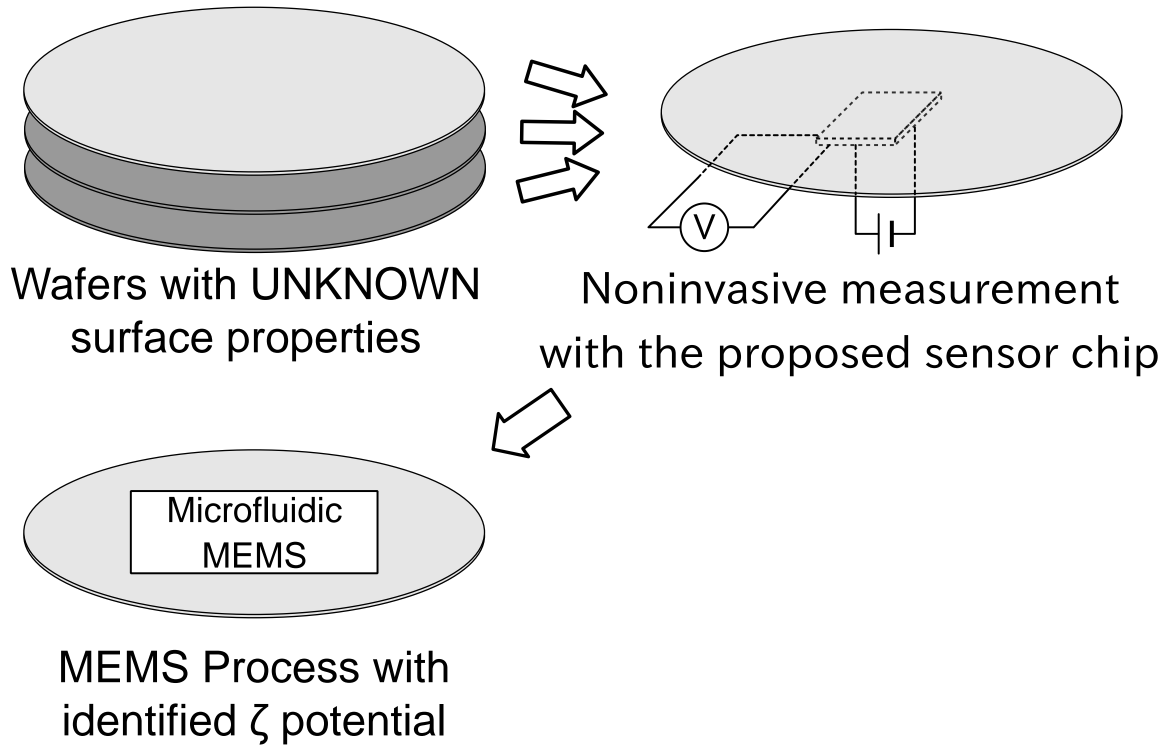


Fig. 5.1: Concept of the zeta potential measurement sensor. The measurement is noninvasive, and the measured materials can be used for microfluidic MEMS devices.

CMOS wafer is also studied. Therefore, the proposed structure has great potential to be integrated with CMOS circuits.

5.2. Methodology

Figure 5.2 shows the schematic of the proposed one-chip zeta potential measurement sensor. The measuring object is stuck on the top of the sensor to form a micro-channel with the opening channel on the sensor. The velocity of EOF in the sensor is proportional to the zeta potential of both the bottom substrate and the measuring object. The EOF actuator is composed of two electrodes placed at both ends of the micro-channel. The metal resistors in the middle of the channel work as the flow sensor. The center resistor of the flow sensor is used as heat reference, and the resistance shift of the other two resistors (R_1 and R_2)

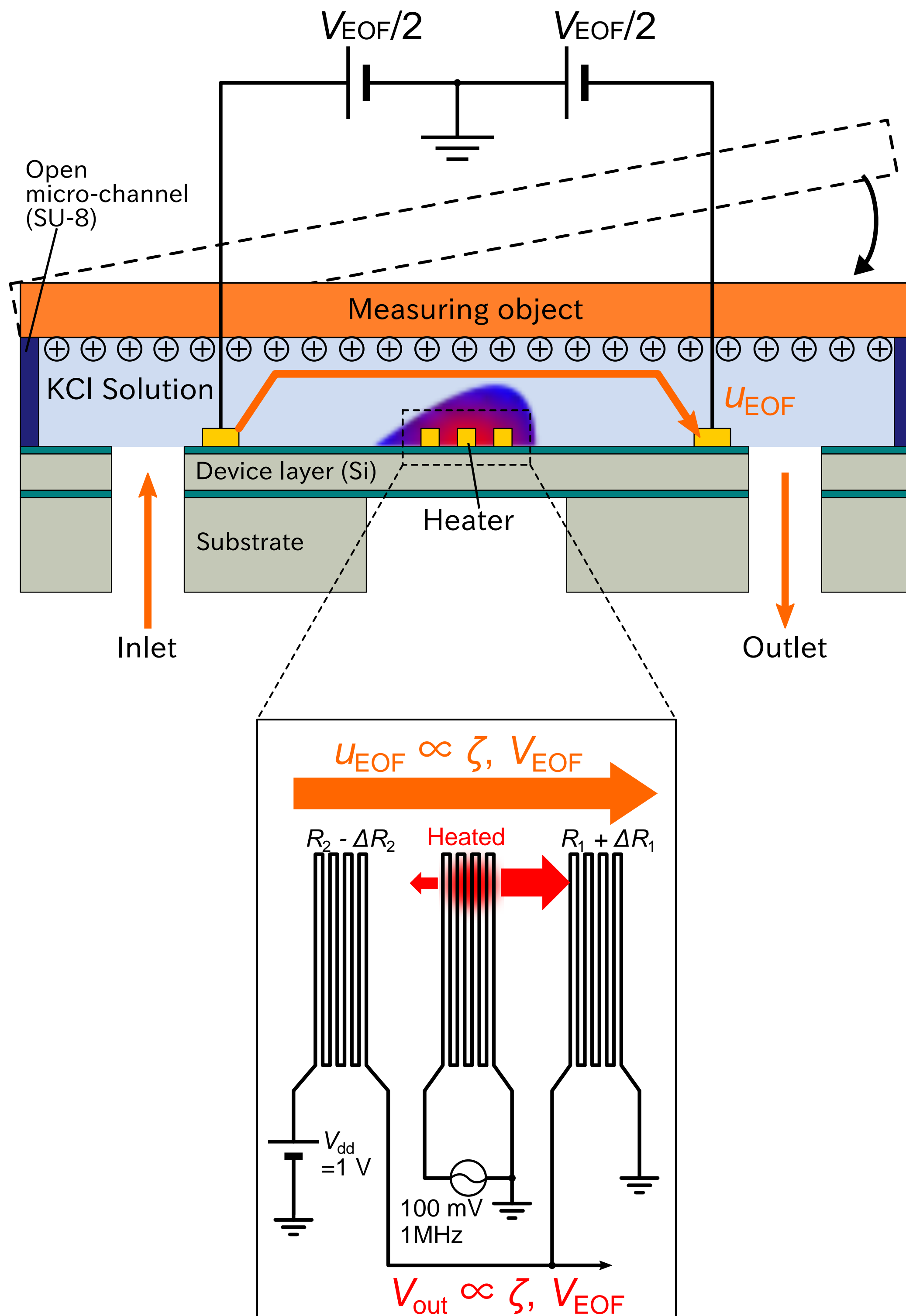


Fig. 5.2: Schematic of the on-chip zeta potential measurement sensor. EOF mobility is measured using the integrated flow sensor to obtain a material' s zeta potential.

across the referential heat resistor are measured. The resistance shift of R_1 is expressed as

$$\Delta R_1 = \alpha u_{\mathrm{EOF}}, \tag{5.1}$$

where α is proportional constant. In order to avoid applying offset voltages to the resistances and the heater and not to cause electrolysis, the center of micro-channel is kept to 0 V. To know the resistance shift corresponding to the velocity of EOF and zeta potential, the output voltage from the half-bridge composed of a couple of the resistive sensors (V_{out}) was observed, and at the same time, V_{EOF} is changed from 0 V to 8 V. Therefore, from the Eq. 1.1 and Eq. 5.1, V_{out} is expressed as

$$\begin{aligned}
V_{\mathrm{out}} &= \frac{R_1 + \Delta R_1}{(R_1 + \Delta R_1) + (R_2 + \Delta R_2)} V_{\mathrm{dd}} \\
&\simeq \frac{R_1 + \Delta R_1}{R_1 + R_2} V_{\mathrm{dd}} \\
&= \frac{R_1}{R_1 + R_2} V_{\mathrm{dd}} + \frac{1}{R_1 + R_2} \cdot V_{\mathrm{dd}} \cdot \alpha u_{\mathrm{EOF}} \\
&= \frac{R_1}{R_1 + R_2} V_{\mathrm{dd}} + \frac{1}{R_1 + R_2} \cdot V_{\mathrm{dd}} \cdot \alpha \frac{\epsilon_0 \epsilon_r \zeta}{\mu} V_{\mathrm{EOF}} \\
&= \frac{\alpha \epsilon_0 \epsilon_r V_{\mathrm{EOF}}}{\mu (R_1 + R_2)} \zeta + \frac{R_1}{R_1 + R_2} V_{\mathrm{dd}}.
\end{aligned} \tag{5.2}$$

Therefore, V_{out} is proportional to the zeta potential. In this experiment, we set V_{dd} to 1 V.

5.3. Chip manufacture

Figure 5.3 shows the fabrication process of a measurement device. Firstly, 1 µm SiO_2 layer was sputtered on an SOI wafer, whose device and buried-oxide (BOX) layers are 10 µm and 1 µm, respectively. Then, 10 nm-thick Ti and 200 nm-thick Au were sputtered. Next, the 2 µm-thick positive photoresist (JSR PFR 7790G) was patterned, and the metals were etched by Au etchant AURUM-302 and 5% APM. After the photoresist was stripped

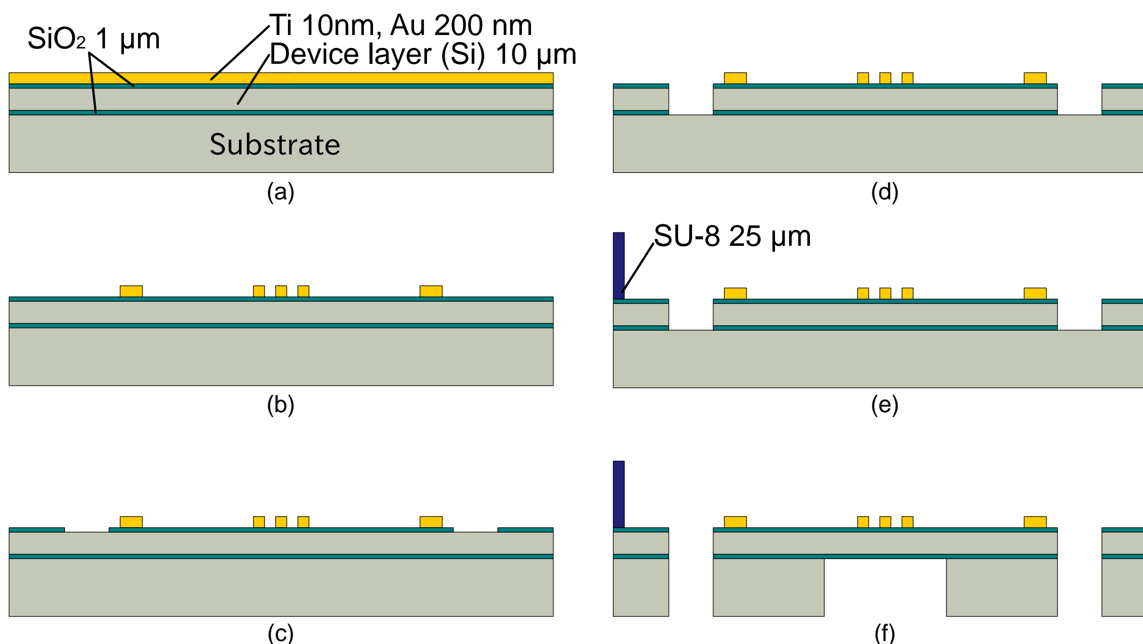
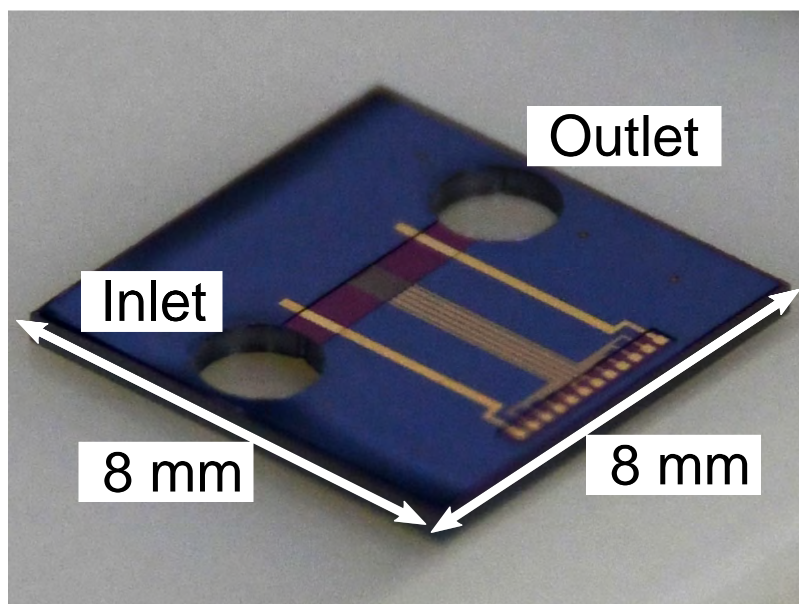


Fig. 5.3: Schematic of the fabrication process. (a) Ti and Au were sputtered on an oxidized SOI chip. (b) The electrodes were patterned. (c) Surface SiO_2 was etched. (d) Top-side DRIE was performed (e) Micro-channel was made with SU-8 resist (f) Back-side DRIE was performed to form inlet and outlet holes.

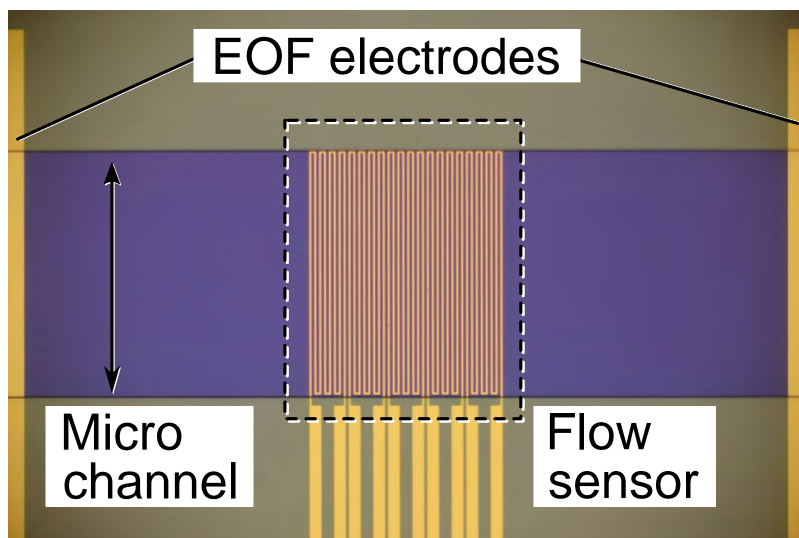
by O_2 ashing, the BOX layer was etched by CHF_3 plasma with ULVAC CE-300I using the same photoresist. Following the BOX layer's pattern, DRIE of the device layer was performed by SPP Technologies MUC-21 ASE-Pegasus. To make a micro-channel, SU-8 3025 negative epoxy photoresist was patterned. Finally, to make inlet and outlet holes, backside-DRIE was performed.

5.4. Results

Figure 5.4(a) shows the fabricated device and Fig. 5.4(b) shows the close-up photomicrograph of the electrode-integrated micro-channel. The size of the sensor chip is 8×8 mm^2 . The length, width, and thickness of the micro-channel of SU-8 3025 are 5.5 mm, 800 μm, and 25 μm, respectively. The gap between the EOF electrodes is 2.5 mm. We



(a)



(b)

Fig. 5.4: a) Image of the fabricated sensor chip. (b) Close-up photomicrograph of the flow sensor and EOF electrodes integrated into the micro-channel.

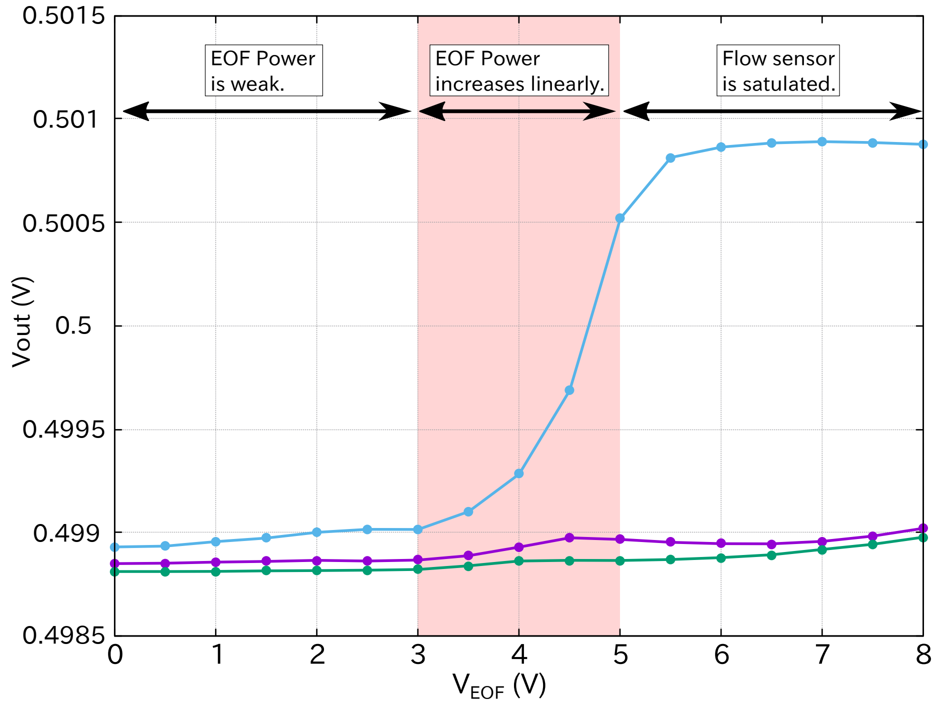


Fig. 5.5: Output of the flow sensor when the V_{EOF} is swept from 0 V to 8 V with quartz, 500nm-thick oxidized silicon, and 165 nm-thick oxidized silicon. 1.0×10^{-4} M KCl solution was used.

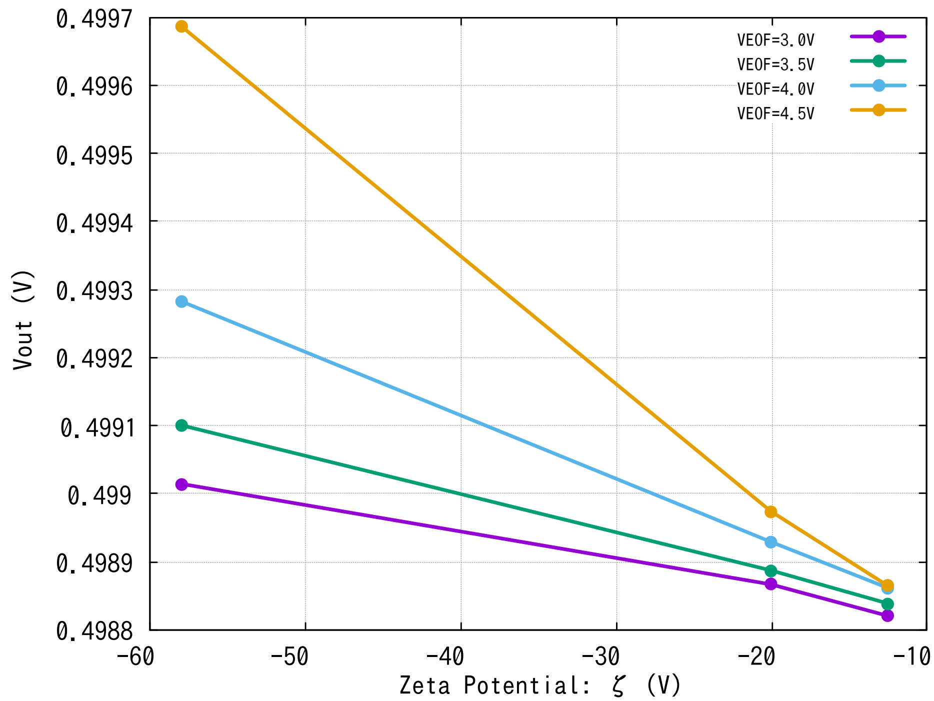


Fig. 5.6: Correspondence of the output of the flow sensor on the zeta potentials measured in advance with each V_{EOF}.

measured three planar samples; 525 μm-thick bulk quartz, 500 nm-thick, and 165 nm-thick oxidized chips, which have different zeta potential properties. As flow liquid, we used 10^{-4} M KCl solution. Figure 5.5 shows the changes of the flow sensor when V_{EOF} is swept from 0 V to 8 V. The flow was electrically observed through half- bridge output voltage (V_{out}). When the V_{EOF} is less than 3 V, the V_{out} is not changed. This is because EOF is not enough to overcome the flow resistance in the micro-channel. From 3 V up to 5 V, the V_{out} was increased linearly. When the V_{EOF} is higher than 5 V, the V_{out} is saturated. It can be considered that electrolysis occurs and that bubbles generated by the electrolysis make a too-fast flow to be measured by the integrated flow sensor. From the result, using nominal applied voltages, in other words, during 3 V < V_{EOF} <5 V presented by the red part in Fig. 5, the sensor can measure the zeta potential. Figure 5.6 shows the flow sensor output voltages during 3 V < V_{EOF} <5 V according to three zeta potentials of the pre-calibrated materials. The pre-measurement was performed using OTSUKA Electronics ELSZ-2000Z. In the pre-result, the zeta potentials of bulk quartz, 500 nm-thick oxidized Si chip, and 165 nm-thick oxidized Si chip were evaluated as −58.0 mV, −20.05 mV, −12.54 mV, respectively under the same pH. From the result, the linear relationship between sensor output and zeta potential can be observed with every V_{EOF} .

5.5. Summary

In this chapter, we have proposed and developed a newl world smallest fully-integrated zeta potential measurement sensor: we fabricated, for the first time, an integrated electroosmotic flow (EOF) micropump with a micro flow sensor in an open micro-channel on an 8×8 mm^2 SOI chip. The sensor can realize stand-alone measurement by the integrated sensor-actuator, and reduction of EOF voltage (less than 10 V) due to the scaled-down

feature. Due to its noninvasive measurement, the analyzed wafer can further be MEMS-processed to realize microfluidic devices with a well-identified surface electrical property. As mentioned, the components of the proposed sensor have the potential to be integrated with CMOS LSIs since the process has CMOS compatibility. Future work is to integrate CMOS circuits to observe and amplify the output voltage from the flow sensor on a chip.

CHAPTER 6

Cooling Measurement

Some of the text and the materials of this chapter are based on the articles of the author's group entitled "Hotspot Liquid Microfluidic Cooling: Comparing The Efficiency between Horizontal Flow and Vertical Flow," PowerMEMS, Paris, France, 2016.

6.1. Introduction

Cooling of integrated circuits using microfluidic devices has been widely studied. Although microfluidic devices are proved as a superior cooling method to conventional cooling methods, these microfluidic devices employ large external equipment. To reduce the size of a cooling system, integrated cooling microfluidic devices have also been studied. The integrated cooling devices have an on-chip micropump, and an EOF micropump is commonly used. However, due to the trade-off relationship between the high-voltage and flow-rate, the EOF micropumps in previous studies are low performance (low flow-rate) or require high voltages.

We have developed the integrated EOF micropump with a high-voltage generator, as mentioned in chapter 4. The developed EOF micropump can overcome the trade-off, and a

future small cooling device is expected by applying the proposed technology. In this chapter, the cooling demonstration of EOF micropumps in the fabricated chip is presented. Besides, the cooling demonstration of a high-flow-rate micro-channel device is also presented to discuss the heat-transfer more in detail. Finally, the future improvement of an LSI cooling device is discussed.

6.2. Thermal equivalent circuit model

Heat transfer processes are classified into three types; conduction, convection, and radiation [106]. The conduction is defined as heat transfer through intervening matter without bulk motion of the matter. The heat transfer rate $\dot{Q}$ between two reservoirs having different temperature (T_A and T_B, $T_A > T_B$) can be expressed as

$$\left.\frac{\partial \dot{Q}}{\partial (T_A - T_B)}\right|_{T_A - T_B = 0} = \frac{kA}{L} \tag{6.1}$$

where k is a proportional factor depending on material and temperature, A is the cross-sectional area. In the limit for any temperature difference ($T_A - T_B \rightarrow 0$) across a length ($L \rightarrow 0$), $\dot{Q}$ can be expressed

$$\dot{Q} = -kA\frac{T_B - T_A}{L} = -kA\frac{\partial T}{\partial x}. \tag{6.2}$$

The heat transfer per unit area ($\dot{q}$) is defined as

$$\dot{q} = \frac{\dot{Q}}{A} = -k\frac{\partial T}{\partial x}. \tag{6.3}$$

$\dot{q}$ is called the heat flux, and Eq. 6.3 is called Fourier's law of heat conduction. The constant k is called thermal conductivity. Taking the limit as a length, the heat transfer rate is zero,

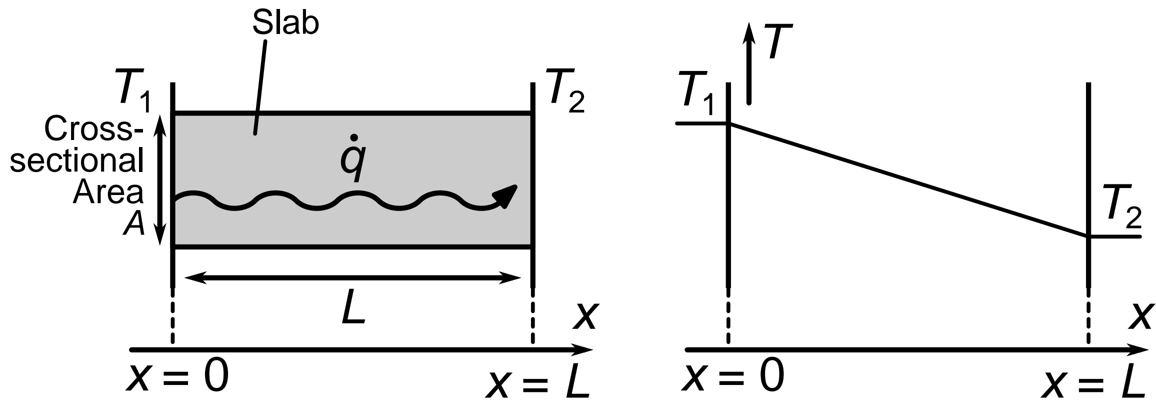


Fig. 6.1: Condition of conductive heat transfer along a block

and we can obtain

$$\frac{d\dot{Q}}{dx} = \frac{d}{dx}(kA\frac{dT}{dx}) = 0, \tag{6.4}$$

$$\frac{d^2T}{dx^2} + (\frac{1}{A}\frac{dA}{dx})\frac{dT}{dx} = 0. \tag{6.5}$$

Figure 6.1 shows a slab such as a block of copper, that has one surface at a high temperature (T_1) and one at a lower temperature (T_2). In such case, the are is not a function of x,

$$\frac{d^2T}{dx^2} = 0, \tag{6.6}$$

$$\frac{dT}{dx} = \text{const.} \tag{6.7}$$

From the condition that $T(x = 0) = T_1$ and $T(x = L) = T_2$, the temperature can be expressed as

$$T(x) = T_1 + \frac{T_2 - T_1}{L}x. \tag{6.8}$$

Therefore, heat flux $\dot{q}$ is given by

$$\dot{q} = -k\frac{T_2 - T_1}{L}x. \tag{6.9}$$

This relationship is similar to the electrical circuits. $\dot{Q}$ is current, $\dot{q}$ is current density, and $T_1 - T_2$ is voltage difference. From the viewpoint of the electrical circuits, the heat transfer can be written by

$$R_{\text{cond}} = \frac{L}{kA}, \tag{6.10}$$

$$\dot{Q} = \frac{T_1 - T_2}{R}, \tag{6.11}$$

where R_{cond} is the thermal resistance of conductive heat transfer. By using the thermal equivalent circuits, the heat transfer can be modeled and simulated. In transient heat transfer, heat to the slab $\dot{Q_{in}}$ is

$$\dot{Q_{in}} = -\rho Vc\frac{dT}{dt} \tag{6.12}$$

where ρ is the density of the slab, V is its volume, and c is its specific heat. The heat transfer rate is also expressed as Eq.6.11,

$$Ah(T - T_\infty) = -\rho Vc\frac{dT}{dt} \tag{6.13}$$

From the condition that $T(t = 0) = T_0$, the equation is expressed as

$$C = \rho Vc, \tag{6.14}$$

$$\frac{T - T_\infty}{T_0 - T_\infty} = e^{-\frac{t}{RC}} \tag{6.15}$$

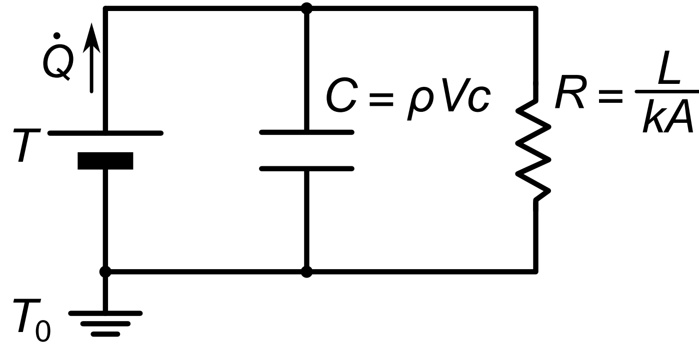


Fig. 6.2: Schematic of thermal equivalent circuits.

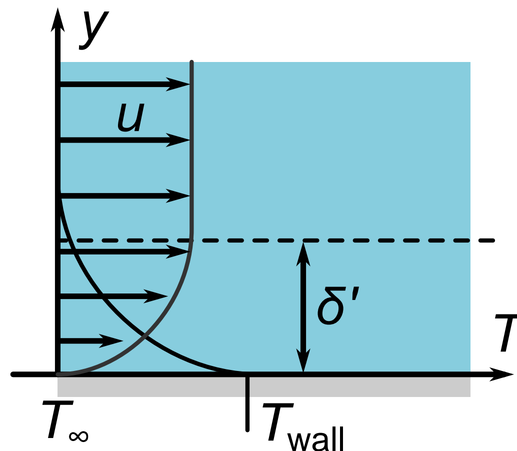


Fig. 6.3: Condition of convective heat transfer.

where C is called heat capacity. From Eq. 6.15, the transient heat transfer is also the same as the electrical circuits, as shown in Fig. 6.2.

Convective heat transfer can also be modeled by equivalent circuits. Figure 6.3 shows the conditions around the surface. In the region of δ', fluid moving is slow, and most of the heat transfer occurs. In the other region, the temperature is almost uniform. Therefore, heat flux can be expressed as

$$\dot{q} = \frac{\dot{Q}}{A} = \frac{k_{\text{fluid}}(T_{\text{wall}} - T_{\infty})}{\delta'} \tag{6.16}$$

Since δ' depends on the flow, δ' is not known and requires to be measured experimentally.

Therefore, instead of δ', heat transfer coefficient $h = \frac{k}{\delta'}$ is used, and heat flux is defined by

$$\dot{q} = \frac{\dot{Q}}{A} = h(T_{\text{wall}} - T_{\infty}) \tag{6.17}$$

The equation is called Newton's Law of Cooling. As increasing the flow rate, h also increases. Using this equation, the thermal resistance of convective heat transfer is expressed as

$$R_{\text{conv}} = \frac{1}{hA}. \tag{6.18}$$

In microfluidic cooling of LSI circuits, the conduction through silicon chips and the convection though fluid in micro-channels are essential. By calculating these thermal resistances, the cooling effect can be numerically investigated. Figure 6.4 shows the thermal equivalent circuit of the micro-channel cooling system following the model shown in Fig. 6.5.

6.3. Cooling measurement of low flow rate micro-channel

The cooling measurement is performed using the same CMOS chips used in Chapter 4. In this chapter, in order to investigate the cooling performance more in detail by changing and extending the EOF voltages, the EOF electrodes are not connected to the on-chip HV generator. Figure 6.6 shows the process flow and Fig. 6.7 shows the fabricated chip.

Temperature is measured by a sensing polysilicon resistor having a resistance of 8.7 kΩ, which is directly under the micro-channel, as shown in Fig. 6.8. The heat flux is input by applying voltages into the microheater, which is a polysilicon resistor having a resistance of 17 kΩ.

Figure 6.9 shows the experimental setup used in the cooling measurement. The resistance

change is measured by an LCR meter (4284A, Keysight). A voltage of 15 V is applied to the microheater using a DC power supply (E3631A, Keysight). The total input power is 13.2 mW, and the power density is 165 W/cm^2, which is a typical power density of power-consuming LSI circuits. The EOF micropump is driven by an HV DC power supply (PMX250-0.25A, KIKUSUI). The current consumption of the EOF micropump is 0.8 µA, and 1.6 µA when V_{EOF} = 50 V and 100 V, respectively.

To calculate the correlation between the temperature and the resistance of the sensing

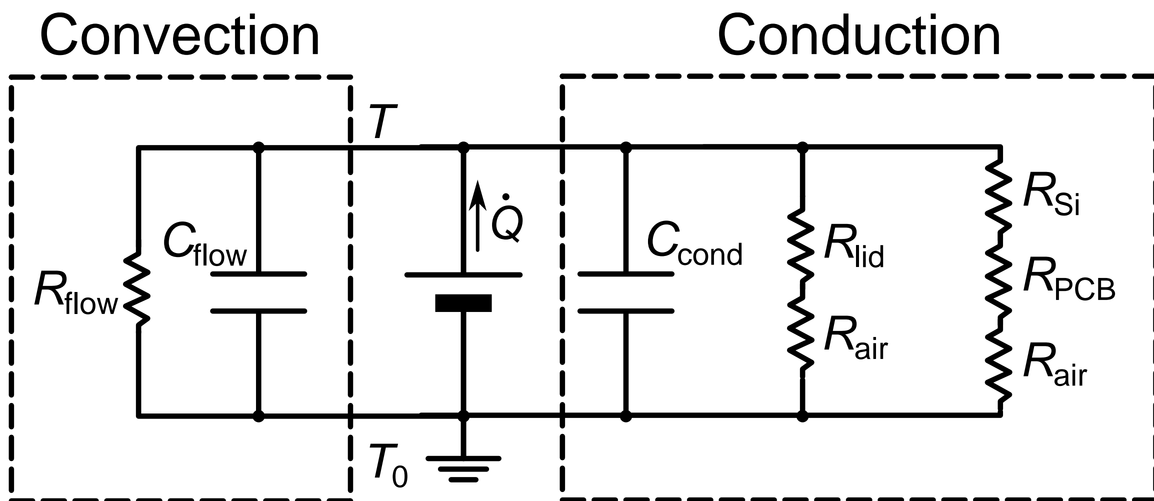


Fig. 6.4: Schematic of thermal equivalent circuits of the micro-channel cooling system.

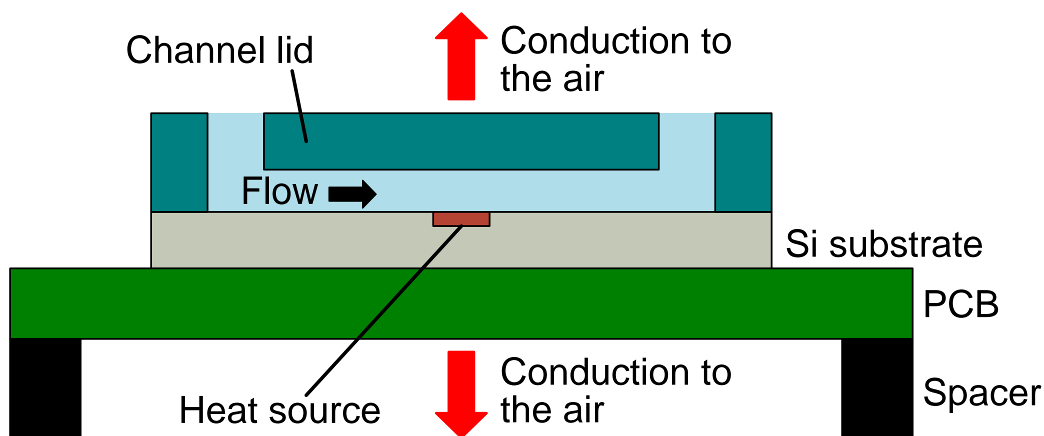


Fig. 6.5: Schematic of the micro-channel cooling system in the experiment.

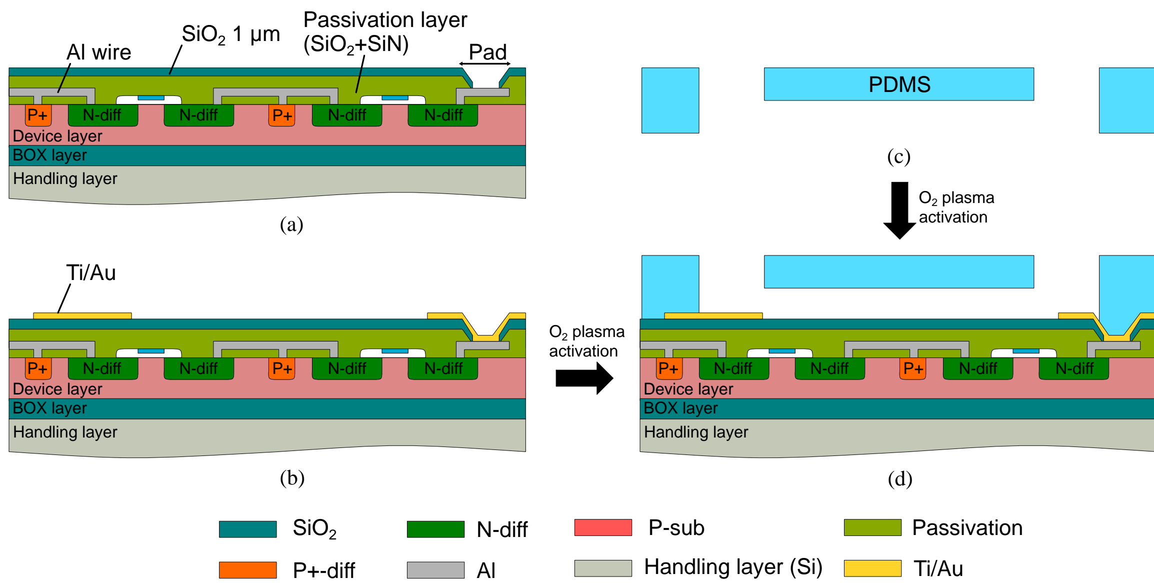


Fig. 6.6: Process flow of the cooling measurement chip. (a) SiO_2 is sputtered and patterned. (b) Au/Ti electrodes are sputtered and patterned. (c) PDMS is patterned using a silicon mold, and holes are punched. (d) Both the top and bottom substrate are activated by O_2 plasma ashing, and then they are bonded.

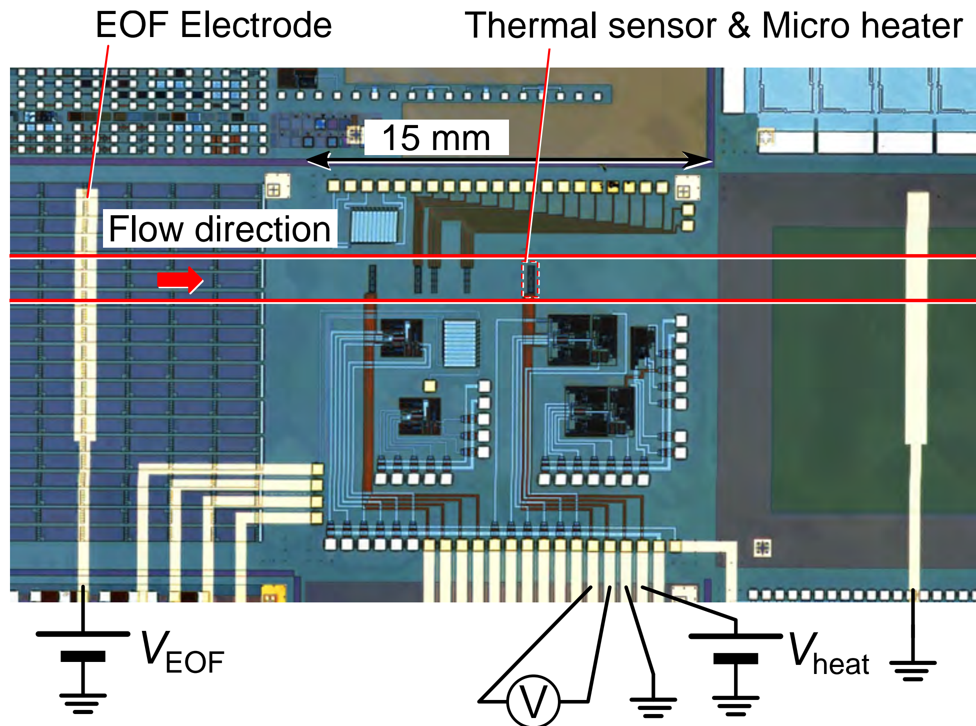


Fig. 6.7: Photomicrograph of the fabricated on-chip for cooling measurement.

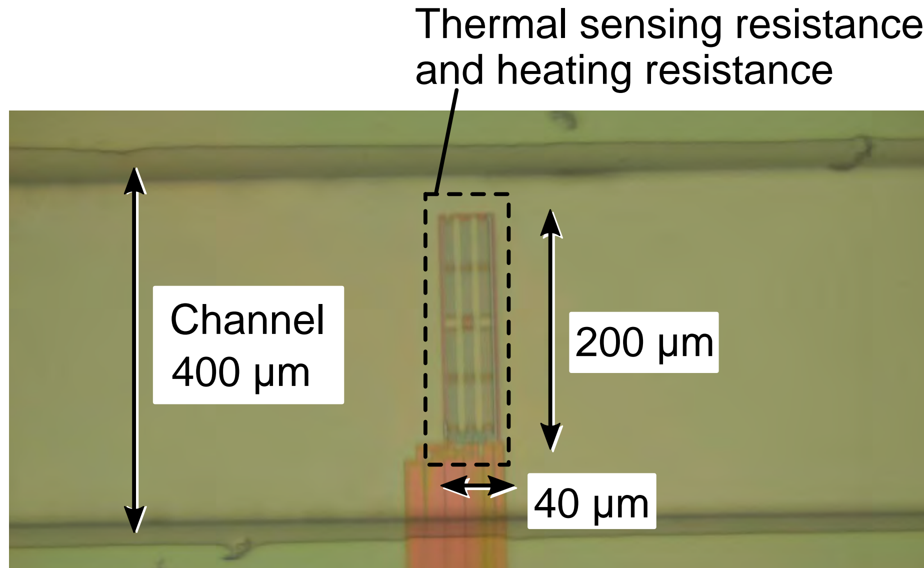


Fig. 6.8: Close-up image of the thermal sensing resistance and heating resistance. These components are directly under the micro-channel.

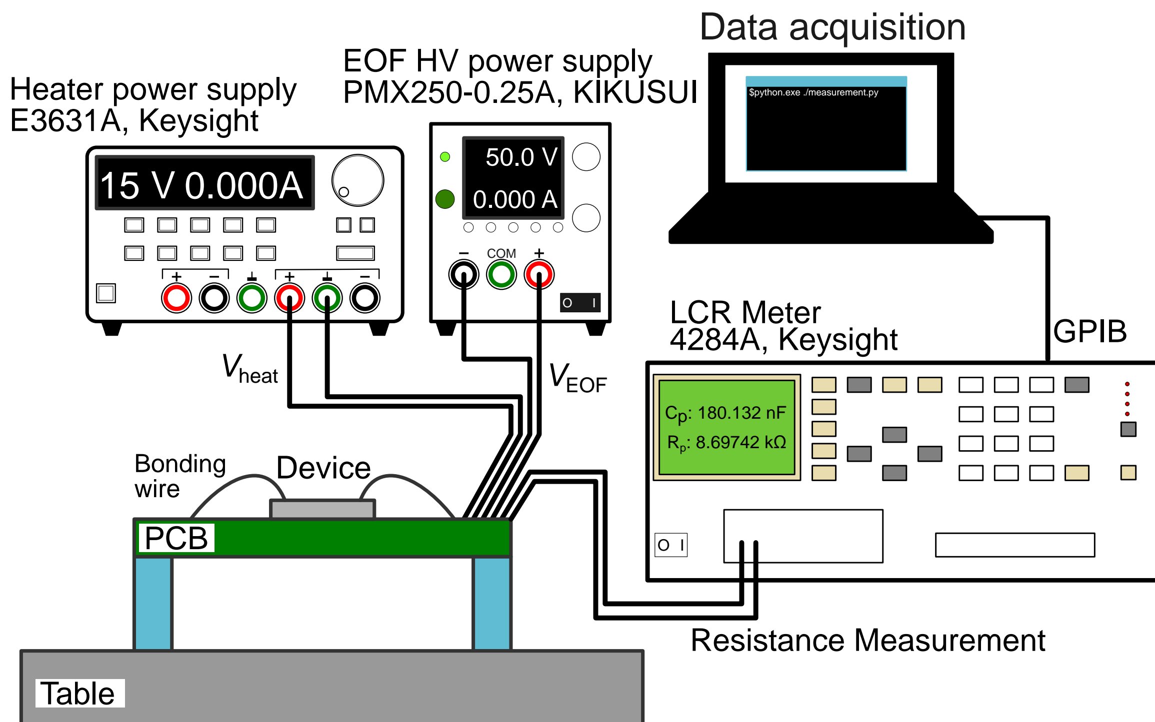


Fig. 6.9: Schematic view of the experimental setup used for cooling measurement.

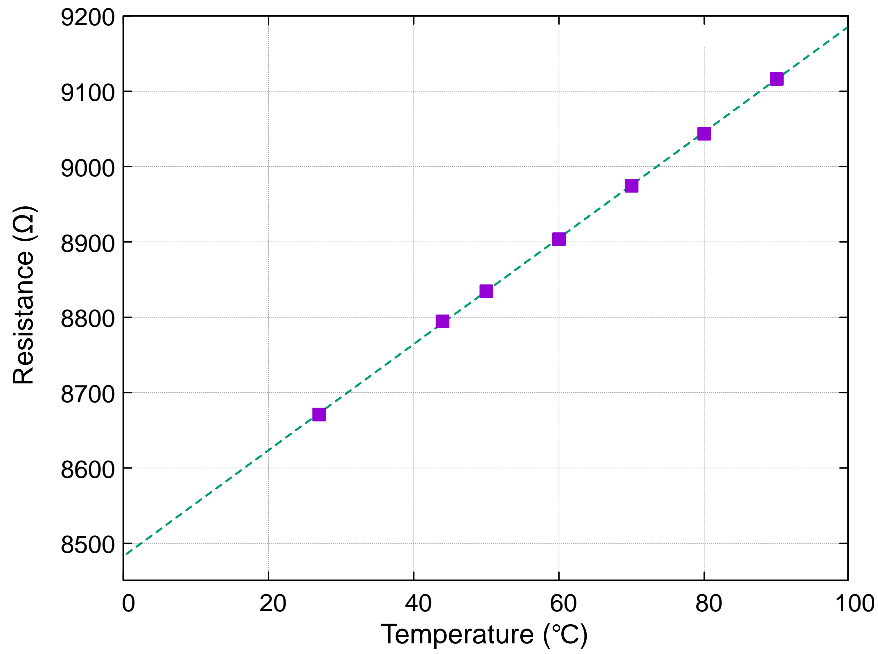


Fig. 6.10: Relationship between resistance and temperature of the thermal sensing resistance used in the cooling measurement on the chip shown in Fig. 6.7.

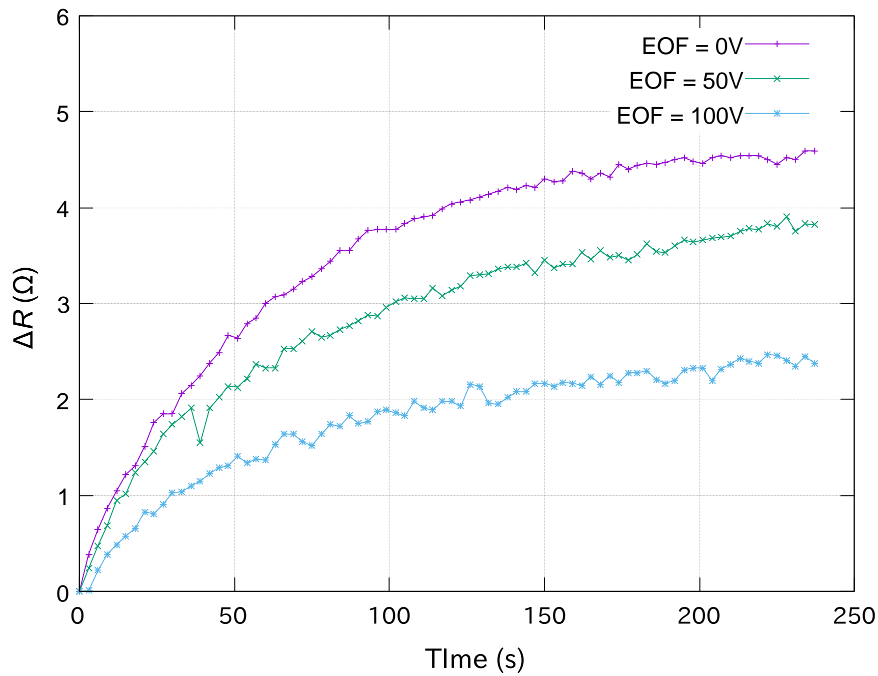


Fig. 6.11: Measurement result of the change of thermal sensing resistance. At $t = 0$, the power is supplied to the microheater.

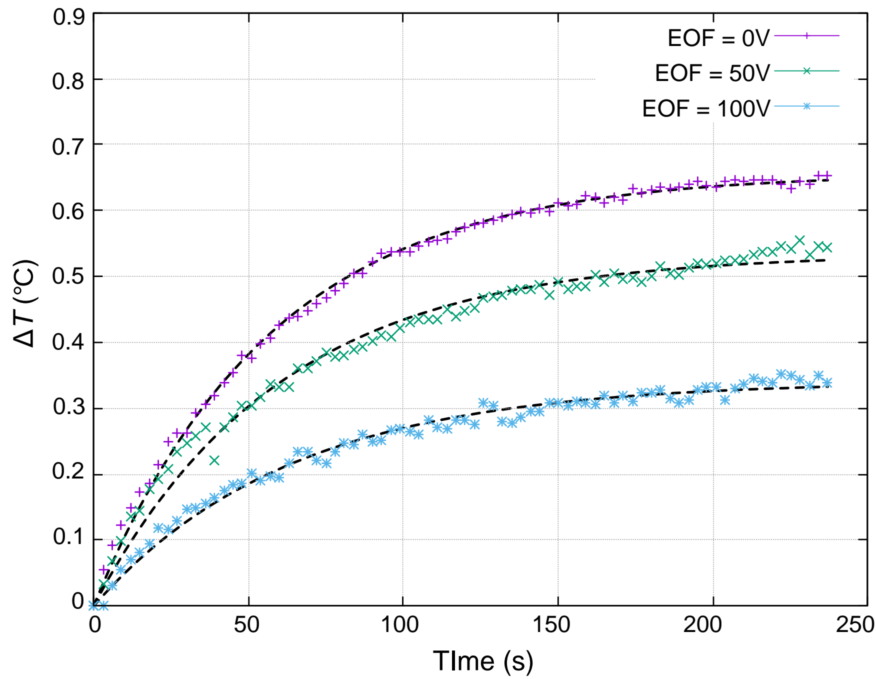


Fig. 6.12: Measurement result of the change of temperature calculated by using the result shown in Fig. 6.10. At $t = 0$, the power is supplied to the microheater.

resistance, the resistance change is measured by sweeping the temperature from 27°C up to 90°. The measured chip is directly put on a hot plate (HP-1SA, AS-ONE). Figure 6.10 shows the dependence of the resistance on the temperature. From Fig. 6.10, the coefficient between the resistance and the temperature is calculated as 7.028 Ω/°C.

By using the coefficient, the temperature change is measured. Figure 6.11 shows the measurement results of the change of thermal sensing resistance. At $t = 0$, the power is supplied to the micro-heater. Figure 6.12 shows the measurement results of the change of thermal temperature, which is calculated by using the coefficient. When the EOF applied voltage (V_{EOF}) is 50 V, the increase of the temperature is smaller than that when $V_{EOF} = 0$ V. Besides, when $V_{EOF} = 100$ V, the temperature increase is suppressed 0.3°C more than the case of $V_{EOF} = 0$ V.

From the measurement in Chapter 4, the flow rate is 164 nL/min and 328 nL/min under

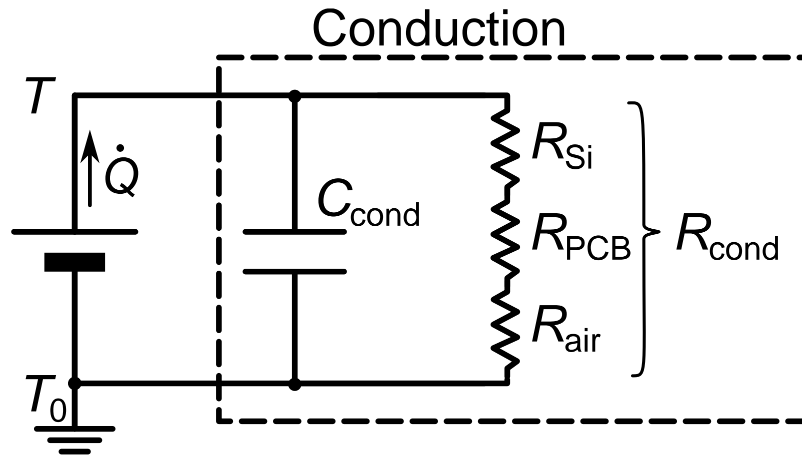


Fig. 6.13: Schematic of thermal equivalent circuits of the experiment.

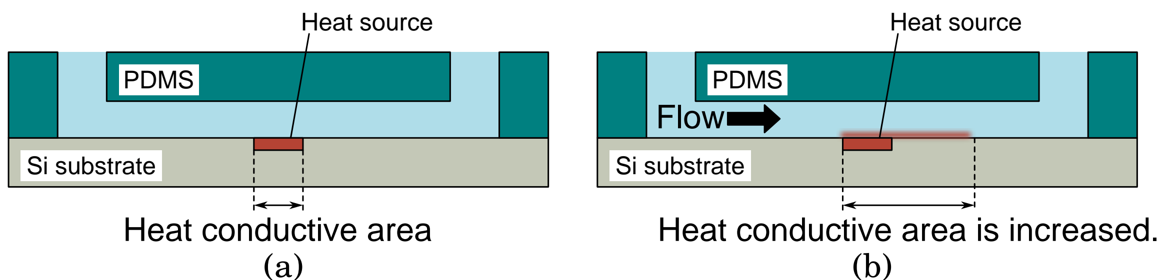


Fig. 6.14: Conduction heat transfer through silicon substrate (a) without flow and (b) with flow generated by an EOF micropump. When the EOF micropump is turned on, the thermal resistance of the silicon substrate is improved. We suppose that it is because the effective area is expanded by the flow.

V_{EOF} = 50 V and 100 V, respectively. In such a condition, the heat flux transferred by convection is small compared to the input power to the micro-heater. Therefore, the dominant heat transfer phenomenon is conduction, and the thermal equivalent circuit can be simplified, as shown in Fig. 6.13. Following this model and fitting Eq. 6.15 to the results shown in Fig. 6.12, the thermal resistance and capacitance are calculated as 49.6 K/W and 1.16 J/K, 40.4 K/W and 1.48 J/K, and 27.8 K/W and 2.48 J/K when V_{EOF} is 0 V, 50 V, and 100 V, respectively. The results indicate that the flow improved thermal resistance in spite of the low flow rate. We suppose that it is because of an expansion of the conductive heat

transfer area between the heat source and the silicon. Figure 6.14a shows the schematic of the conductive heat transfer area without the flow. When V_{EOF} = 0 V (no flow), the area is only around the heat source. On the other hand, when there is a flow in the micro-channel, the heat is dissipated by the micro-channel. We suppose that the heat-transfer area is expended, as shown in Fig. 6.14b.

6.4. Cooling measurement of high flow-rate micro-channel

While the conductive heat transfer is dominant in case that the flow rate is low such as the previous section, the convective heat transfer becomes the cooling dominant when the flow rate is high. In such a condition, increasing the values of h and δ' is essential. Improving h can be performed by increasing the flow rate. On the other hand, to increase δ', the flow direction is also a key factor. However, most of the previous research on a micro-channel cooling system have focused on improving the micropump performance

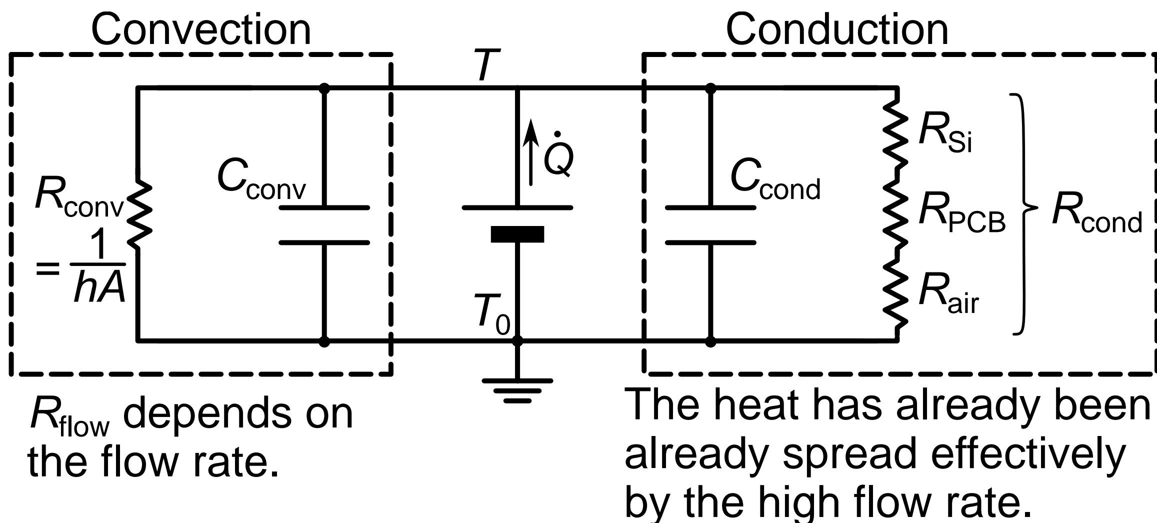


Fig. 6.15: Schematic of thermal equivalent circuits when the flow rate is high, and convection is also dominant heat transfer.

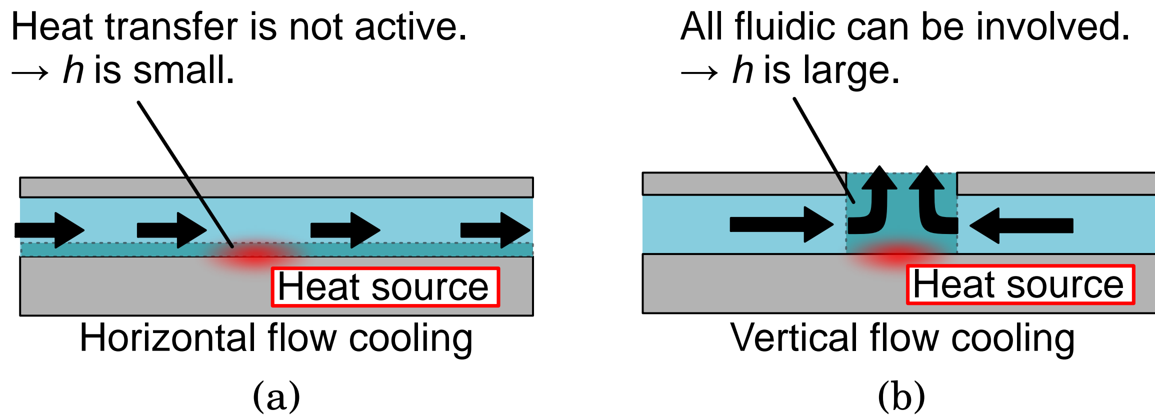


Fig. 6.16: (a) Cooling a hotspot by the horizontal flow. Out-of-plane heat spread is small due to laminar flow. (b) Cooling a hotspot by the vertical flow. All flow can contribute to cooling a hotpot over the hotspot.

and characterization of in-plane micro-channels. A horizontal in-plane micro-channel only involves the surface of the micro-flow, as shown in Fig. 6.16a. To involve all the liquid over the hotspot, the authors propose to make use of vertical flow (Fig. 6.16b). The purpose of the section is to investigate the improvement of convective heat transfer by increasing the flow rate. Besides, the effect of the flow direction is experimentally investigated.

6.4.1 Experimental results

6.4.1.1 FEM simulation

Figure 6.17a and b show the simulated temperature of a hotspot cooled with horizontal in-plane flow and vertical out-of-plane flow. In the simulation, 400×400 μm^2 square Al heater is put on Si substrate as a hotspot, and a micro-channel is placed on the Al heater. In the in-plane cooling simulation, the height of the channel is 30 μm, and the flow is made from left to right, as shown in Fig. 6.17a. In the case of the out-of-plane channel, the inlet is the 30 μm channel, and the 750 μm outlet is above the hotspot, as shown in Fig. 6.17b. The input power is supposed to be 2 W, and input liquid is supposed to be DI-water at a

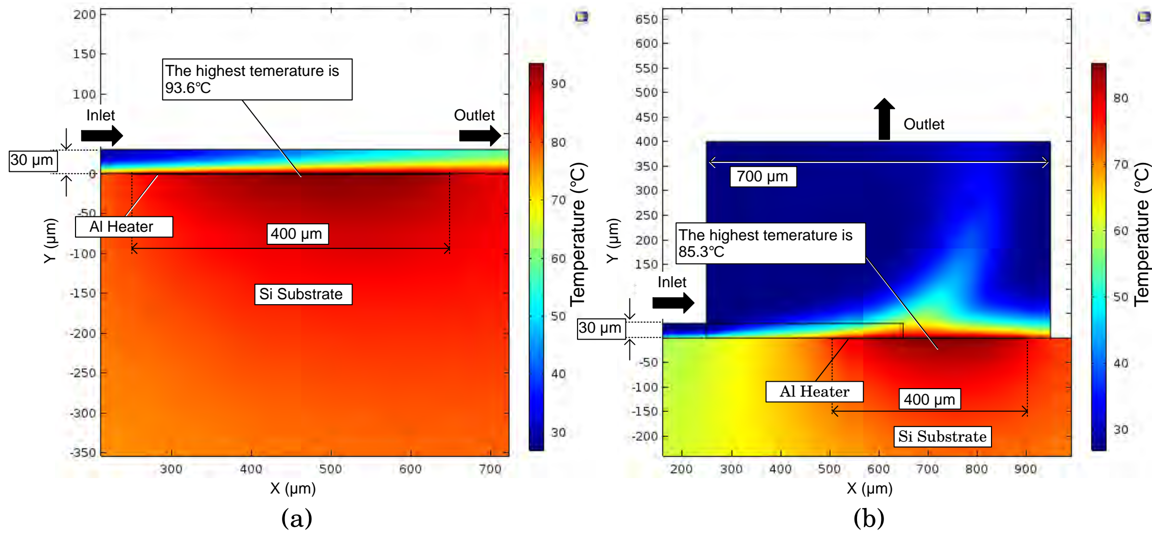


Fig. 6.17: FEM simulation of (a) horizontal in-plane cooling (b) vertical out-of-plane cooling

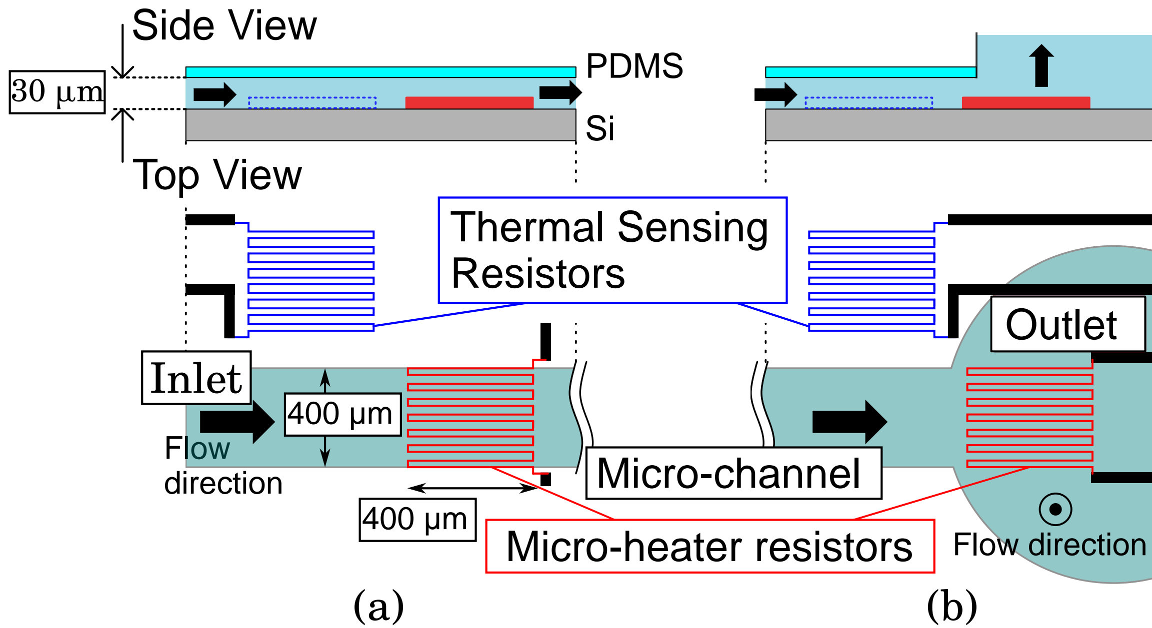


Fig. 6.18: Schematic of the fabricated device to measure the impact of (a) horizontal flow and (b) vertical flow to cool the hotspot. A resistor is placed next to a micro-heater to measure the temperature .

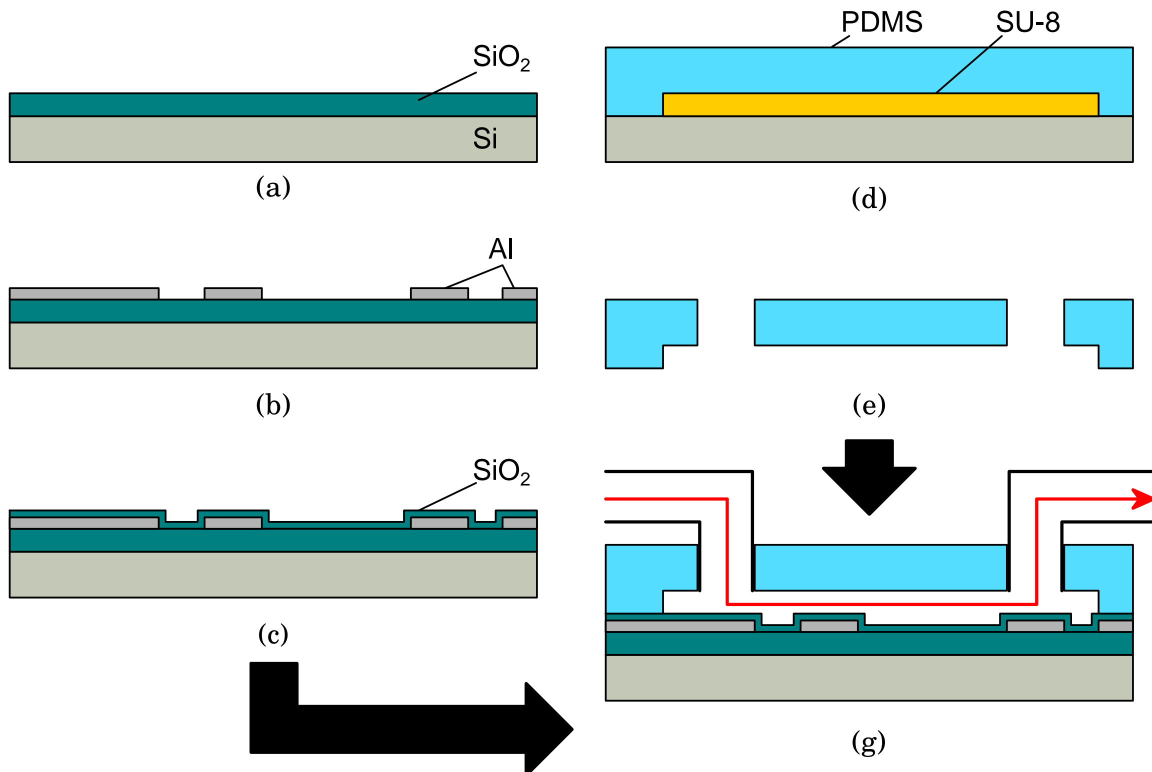


Fig. 6.19: Process flow of the fabricated device. (a) 500 nm-thick SiO_2 is sputtered. (b) 500 nm-thick Al is sputtered and patterned. (c) SiO_2 is sputtered again to avoid electrolysis. (d) PDMS is patterned using a silicon/SU-8 mold. (e) PDMS is peeled off from the mold, and then inlet and outlet holes are made. (f) The top and bottom substrate are bonded using O_2 plasma activation, and then tubes are connected to the inlet and outlet holes.

flow-rate of 500 µm/min. While the highest temperature with horizontal in-plane cooling is 93.6°C, the highest temperature with vertical out-of-plane cooling is 85.3°C. It means that the vertical flow can take out the heat from the hotspot thanks to the flow direction and the larger volume of cooling involved liquid.

6.4.1.2 Temperature measurement of in-plane cooling and out-of-plane cooling

To measure the temperature and to heat locally, we fabricated microresistors as thermal sensors and an artificial hotspot, as shown in Fig. 6.18. The design of the device follows the simulated layout.

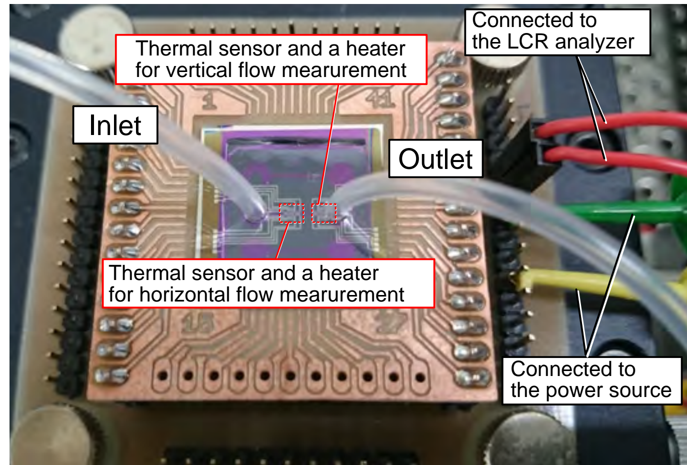


Fig. 6.20: Setup of the experiment. The channel is connected to the external pump (450 μL/min). the resistor for a thermal sensor is connected to an LCR parameter analyzer, and the resistor for a micro-heater is connected to a power source.

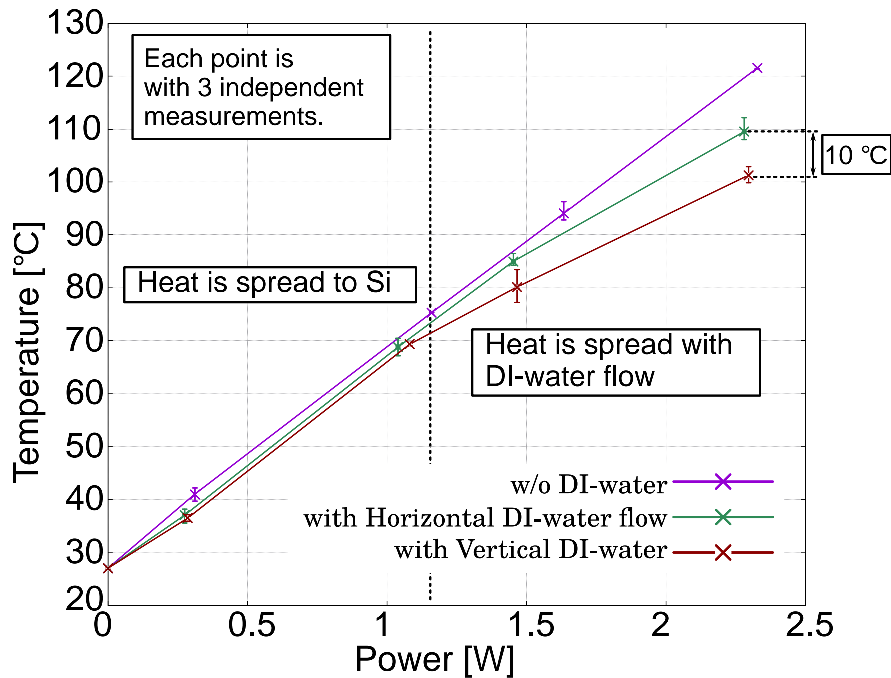


Fig. 6.21: The temperature when the power is input to a micro-heater. When the input power is around 2.3 W is, the difference of the temperature between around the horizontal flow and with the vertical flow is 10 °C

One microheater was placed under the horizontal flow, and the other was placed under the vertical flow. For fabricating a bottom plate, SiO_2 was sputtered by 500 nm as an insulator (Figure 6.19-(a-1)), and then Al was sputtered by 500 nm and patterned (Fig. 6.19a-2). After the patterning, 50 nm SiO_2 was sputtered again to avoid electrolysis when liquid flowing (Fig. 6.19a-3). As a top plate with micro-channels, we patterned PDMS using a SU-8 mold (Fig. 6.19b-1). After peeling off the PDMS from the mold, inlet and outlet holes were made (Fig. 6.19b-1). Finally, both of them were bonded after O_2 plasma activation (Fig. 6.19c).

The micro-channel was connected to an external pump, whose flow rate was 450 µL/min. The micro-heater as a hotspot was connected to a power source, and the thermal sensor was connected to an LCR meter (4284A, Keysight), as shown in Fig. 6.20. After the correspondence of the change of the resistance against the temperature is measured, we calculated the temperature around a hotspot from the resister next to the hotspot, as shown in Fig. 6.21. After power consumption of a micro-heater reaches more than about 1 W, the temperature around the hotspot under the vertical flow becomes smaller than that of under the horizontal flow. It means that the heat which cannot spread to the Si substrate is spread by the water flow and that the vertical flow can carry the heat more efficiently than the horizontal flow. When the power input to the hotspot is about 2.3 W, the difference of the temperature between the horizontal flow and the vertical flow reaches 10°C. Consequently, while the temperature rises up to 122°C without DI-water and flow, the temperature is 112°C and 102°C with the horizontal and vertical flow, respectively. It indicates that the convective heat transfer is effective when the flow rate is high and that changing flow direction improves the heat transfer more.

Following the equivalent circuit, as shown in Fig. 6.15, and the result without flow, the

thermal resistance of conduction (R_{cond}) when the input power is 2.3 W is calculated as $(122 - 25)/2.3 = 42.2$ K/W. The heat transferred by the flow is calculated as $2.3\mathrm{W} - (112 - 25)/42.2 = 0.24$ W, and $2.3\mathrm{W} - (102 - 25)/42.2 = 0.48$ W with horizontal and vertical flow, respectively. Therefore, the thermal resistance of convection (R_{conv}) is calculated as 363 K/W, and 160 K/W with the horizontal and vertical flow, respectively.

6.5. Discussions

From the results of the measurement, we have found the two modes of micro-channel cooling, as shown in Fig. 6.22. When the flow rate is low, the convective heat transfer is small compared to the conductive heat transfer. Therefore, conduction through the substrate is the dominant heat transfer. However, as seen in the experimental result in the previous section, the flow improves the efficiency of the conduction. We consider that it is because the flow promotes the conduction by spreading the heat transfer into a larger area, as shown in Fig. 6.22a. This cooling mode can be effective in reducing hotspots in LSI circuits. On the other hand, when the flow rate is high, the convective heat transfer is also a main cooling factor, as shown in Fig. 6.22b. In this cooling mode, we consider that the conductive thermal resistance can be reduced by the heat spreading effect and that the

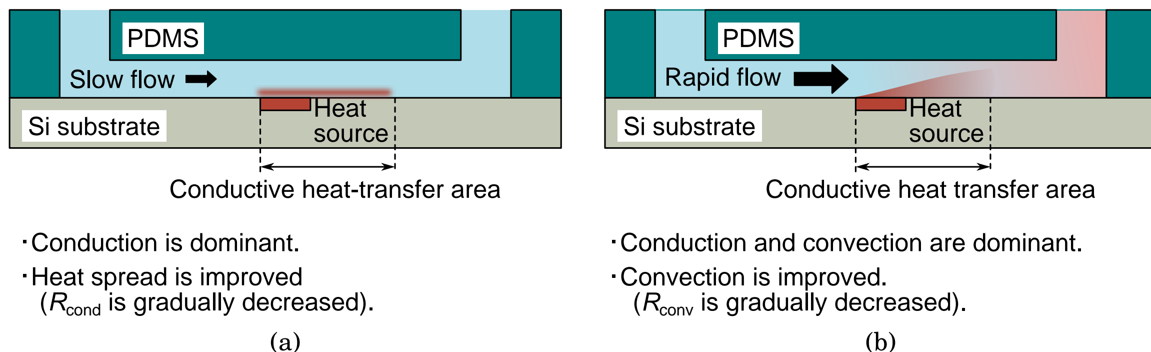


Fig. 6.22: Schematic of Cooling modes when the flow rate is (a) low and (b) high.

convective thermal resistance can be decreased more by increasing the flow rate.

However, in the low flow-rate cooling experiment, the input power was about 0.013 W, which is relatively small compared to the high flow-rate cooling experiment. We consider that the heat spreading effect is saturated as the input heat increases. When input heat increases, the conductive heat transfer area also increases. If the conductive heat transfer area is large and the additional area extended by the flow is relatively small, the heat spreading mode is invalid. Therefore, the heat spreading effect may work when the flow rate is moderately high and the size extended area is significantly large compared to the heat transfer area before cooling. In fact, the heat spreading effect was also observed in the high flow-rate experiment when the convective heat transfer did not occur considerably, as shown in Fig. 6.21. Besides, in this experiment, the temperature of cooling water is always the same as the room temperature. When the heat in the hottest spot is large and the background temperature in the other area is also high, the water is heated before reaching the hottest spot. Due to these reasons, we consider that the cooling performance may be degraded in real cooling applications such as high power chips. Therefore, to find out the valid range of the heat spreading mode, future extended experiments using higher heat flux are required.

An application of the low-flow-rate cooling device is a thin heat sink to reduce hotspots in a portable device, as shown in Fig. 6.23. In such an application, a smaller amount of liquid is more suitable to save space. Also, on-chip closed-loop micro-channels integrated with an EOF micropump is effective.

In order to realize the more efficient cooling by utilizing both convection and conduction, the placement of the fluid components is also essential. The vertical flow enhances the convective heat transfer. Therefore, the most power-consuming heat source should be

placed directly under the outlet hole of micro-channels.

Besides, in the experiment, we have only focused on single-phase liquid cooling, but utilizing phase change of the liquid is also attractive since the vaporization absorbs a more significant amount of heat. We consider that EOF micropumps are also effective in the multi-phase cooling device. As previous studies and the experimental results, an EOF micropump can output the high pressure. The integration of an HV generator allows us to increase the output pressure. Moreover, EOF micropumps can be connected in series and can output the higher pressure. On the other hand, as explained in the introduction, conventional multi-phase cooling devices, such as a heat-pipe and an LHP, use capillary forces to circulate the liquid. However, as thinning these cooling devices causes increasing

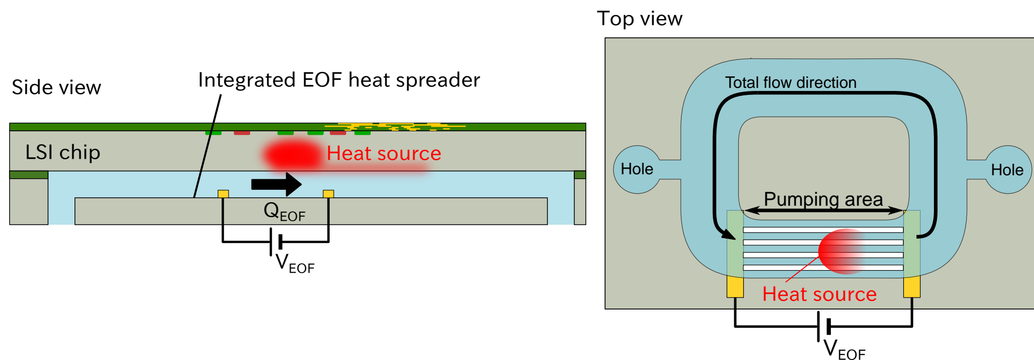


Fig. 6.23: Schematic of a thin integrated EOF heat-spreading cooling device.

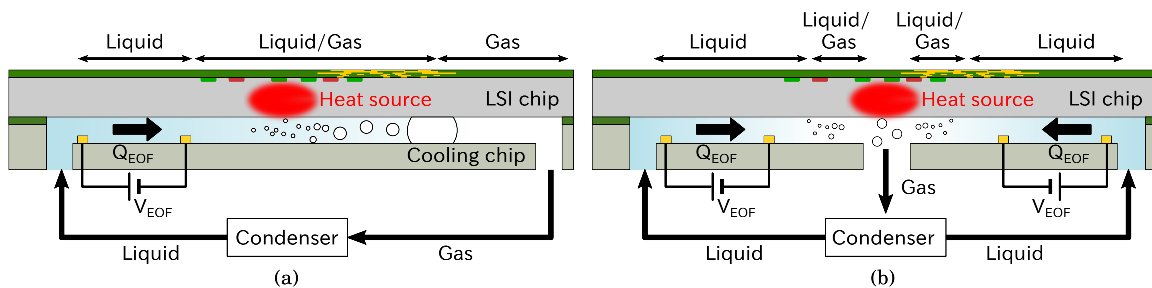


Fig. 6.24: Schematic of a thin integrated multi-phase cooling device using (a) horizontal micro-channels and (b) vertical micro-channels.

the interruption of fluid by the vapor, the minimum thickness of them is limited. The EOF micropumps can work in such thin structures without decreasing the output pressure. Therefore, we consider that the EOF micropumps can be placed in the cooling device and enables us to realize a thin cooling device. In such usage, the EOF pumping part requires to be placed before the heating areas not to be halted by the bubbles in micro-channels, as shown in Fig. 6.24a. Moreover, if the layout allows us to put the outlet just under the heat source, vertical micro-channels can make cooling more effectively, as shown in Fig. 6.24b.

In either usage of micro-channels, micro-channels enable us to realize thin cooling devices. It also enables us to embed the cooling device between 3DICs, such as a logic circuit chip and DRAM memory chips.

6.6. Summary

The cooling effect of the integrated EOF micropump is investigated, which is presented in the previous chapters. Despite the low flow-rate because of the limited size, and the thermal resistance consequently decreases. When a voltage of 100 V is supplied to the EOF micropump, the temperature is 0.3°C lower than a case without EOF. We suppose that this is because this device is valid to expand the conducive heat-transfer areas around hotspots. We consider that a low-flow-rate micro-channel device can be used as a heat-spreader, and suitable for a portable device to save cooling component space. Also, to find out the valid range of the heat spreading mode, future extended experiments using higher heat flux are required.

On the other hand, as increasing the flow rate, convection also becomes effective, and the thermal resistance decreases more. In such a case, the flow direction improving the cooling performance by enhancing the convective heat transfer.

Taking account into a multi-phase cooling system, an EOF micropump is suitable to prevent the return of the vapor instead of a wick since the micropump can output the high-pressure. We consider that it can lead to realizing a thin cooling system that could not be realized before.

CHAPTER 7

Conclusions

In this chapter, a summary of the work is presented, along with the contributions made to the field. The discussions for the possible future research directions are also given.

7.1. Summary

This work is mainly focused on developing a micro-channel cooling system for the power-consuming LSI chips. Notably, this dissertation focuses on the integration of an on-chip high-voltage generator to enhance an EOF micropump using post-processed DTI technology. The results are summarized below:

For the optimization of the isotropic etching used in the post-processed DTI, the test structures were designed to indicate the endpoint of the isotropic etching process by simple observation with an optical microscope. By using the test structures, not only was the exact release time determined, but a new plasma etching mode was discovered, which is suitable for releasing MEMS structures.

As a proof-of-concept of using post-processed DTI transistors to HV applications, we firstly demonstrated 30 V switching circuits through the commercial 5 V 0.6 µm CMOS

process on SOI and MEMS post-processing. The 30 V switching circuits integrated the gate-level-shift circuits and can be controlled by 5 V signals. Then, high-voltage generators following the Dickson charge-pump circuits using post-processed DTI transistors. The output of the 20-stage, 10-stage, 5-stage HV generator is 95.2 V,49.8 V, 26.9 V,respectively.

Then we designed an EOF micropump integrated with the proposed 10-stage high-voltage generator. The flow rate of the fabricated integrated EOF micropump was 164 nL/min using the 5 V power supply.

To realize the examine the parameters of EOF micropumps after the fabrication, a non-invasive zeta potential measurement sensor is demonstrated. It could measure the zeta potential of 500 µm-thick and 165 µm-thick oxidized Si substrates and a quartz substrate.

Finally, we measured the cooling ability of the proposed EOF micropump. Even though the flow rate of the EOF micropump is low because of the limitation of the chip size, the device successfully reduced the temperature of a 40×200 μm^2 hot spot by 0.3°C, where input power was 13 mW (165 W/cm^2). We suppose that this is because the flow spread the heat and that conductive heat transfer is enhanced. To observe the change of cooling ability by increasing the flow rate, we measured the temperature of a hot spot under a high flow-rate micro-channel. From the measurement, the conductive heat transfer can be decreased. Besides, cooling efficiency can be more improved by changing the direction of flow.

7.2. Contributions

The primary contribution of this work is a more in-depth understanding of CMOS integrated micropumps and LSI cooling using the micropumps with more thorough experimental measurement and analysis. The author's contributions are summarized below:

- Test structures for quantitative investigation of Si isotropic etching used in the MEMS posed-processed DTI are developed. The test structures can be used to investigate the etching conditions of MEMS releasing.
- The design of an NV_{DD}-high-voltage switch integrated with level-shifter using MEMS post-processed DTI is developed. The design of the level shifter is not limited by the switching voltage.
- The design of high-voltage generators using MEMS post-processed DTI is developed. Owing to the nature of the post-processed DTI, the loss of voltage increments is significantly reduced.
- The design and fabrication method of an on-chip EOF micropump integrated with a high-voltage generator are developed. These also enhance the integration of microfluidic actuators into microfluidic devices for point-of-care applications.
- A non-invasive zeta potential measurement sensor is developed, which allows us to use the measured samples for microfluidic substrate. This enhances the parametric design of microfluidic devices using zeta potential.
- The measuring method of cooling performance of integrated micropumps using CMOS LSI components is developed.
- Two modes of LSI cooling using micro-channels are found. One mode is heat spreading mode and indicates that the low flow rate microfluidic device is also effective to enhance the conduction through the substrate. The other mode indicates that increasing the flow rate decreases the convective thermal resistance and the cooling performance is improved.

7.3. Possible Improvements and Future Scope

The EOF micropump itself is improved in a few ways. Most significantly, the output pressure can be increased by series-connecting of multiple EOF micropumps. By using integrated high-voltage generators, the output pressure per stage is much higher than the previous studies.

In this dissertation, the output voltages of the developed integrated high-voltage generator are limited to less than 100 V. However, as the current consumption of EOF micropumps is small, the increase of the output voltage can be expected by increasing the number of stages up to several hundreds of volts. Besides, the proposed high-voltage generator follows a basic circuit model, and the efficiency can be more improved by circuit topology.

In this work, the cooling effect of low flow-rate micro-channels using an integrated EOF micropump is experimentally measured, and it could not be investigated by the FEM simulation. However, we consider that it can be simulated by optimizing the heat-transfer model. Also, as the investigation was performed only in the case of the low-rate flow measurement, the input heat was relatively small compared to the high-power consuming logic circuits. The more experiment using such large heat flux will lead to understanding the effective heat range of the low flow-rate cooling mode.

By using an improved high-pressure EOF micropump, an efficient thin multi-phase cooling device can be realized, which can cope with high power-consuming circuits in a 3DIC.

APPENDIX A

LARGE-AREA DRIE

A.1. Introduction

A.1.1 Large MEMS structures

Micro-electromechanical Systems (MEMS) are widely used for sensors and actuators. The size of MEMS devices is typically tens to thousands of micrometers, which contributes to the miniaturization of electric devices such as smartphones. To realize more compact devices, continuous efforts such as CMOS integration have been paid to scale down the entire MEMS. In some application fields, in contrast, the MEMS structure is becoming larger owing to its application requirements. Laser scanner [107], [108] and energy harvesting devices [109] are typical applications that require large MEMS fabrication.

Among applications that need large-displacement MEMS, displays [110]–[112] and light detection and ranging (LiDAR) scanning systems particularly require larger MEMS actuators because the resolution of displays and scanning systems is proportional to the performance of the MEMS mirror. The performance is expressed as the index $\theta_{\mathrm{OPT}} \cdot D \cdot f$,

where θ_{OPT} is the optical scan angle, D is the mirror diameter, and f is the scan frequency. In terms of display resolution, the important parameter is $\theta_{\mathrm{OPT}} \cdot D$, since the number of pixels N is proportional to $\theta_{\mathrm{OPT}} \cdot D$ (Fig. A.1). For example, to realize a MEMS display with 1280×1080 pixels (HD1080 standard), $\theta_{\mathrm{OPT}} \cdot D$ should be larger than 84.4 mm · deg and f should be 40.5 kHz [107]. To obtain a large scan angle, a laser scanner is operated in the resonant mode. In this method, the scanner is actuated at the resonant frequency, where the displacement of the movable structure is enlarged. To further increase displacement in resonance, a cascaded mirror structure using mechanical coupling was reported [113],[114] to enhance resonant work. In this method, the inner mirror is driven at a resonant frequency by applying force to a large outer frame. Owing to mechanical coupling, the displacement of the inner mirror is considerably larger than the resonance of a single mirror. In such a design, however, the die becomes substantially larger than the single mechanical resonant mirror. The scanner used in a previous research for actuation was 3.75×6.15 mm^2, to actuate a 1.4 mm inner mirror frame [113]. Therefore, to realize a higher quality MEMS mirror, the die size of the actuator must reach the centimeter order.

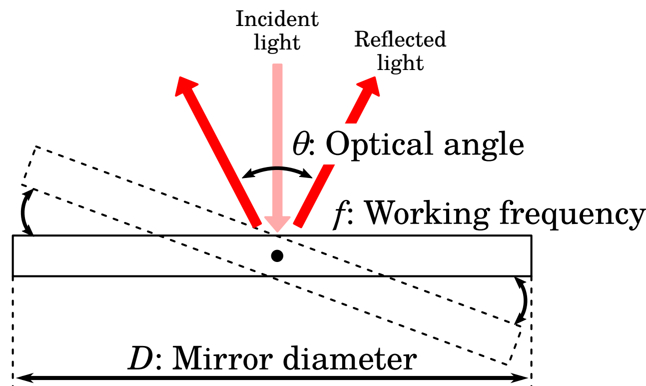


Fig. A.1: Schematic of a MEMS mirror. The performance is expressed as the index $\theta_{\mathrm{OPT}} \cdot D \cdot f$.

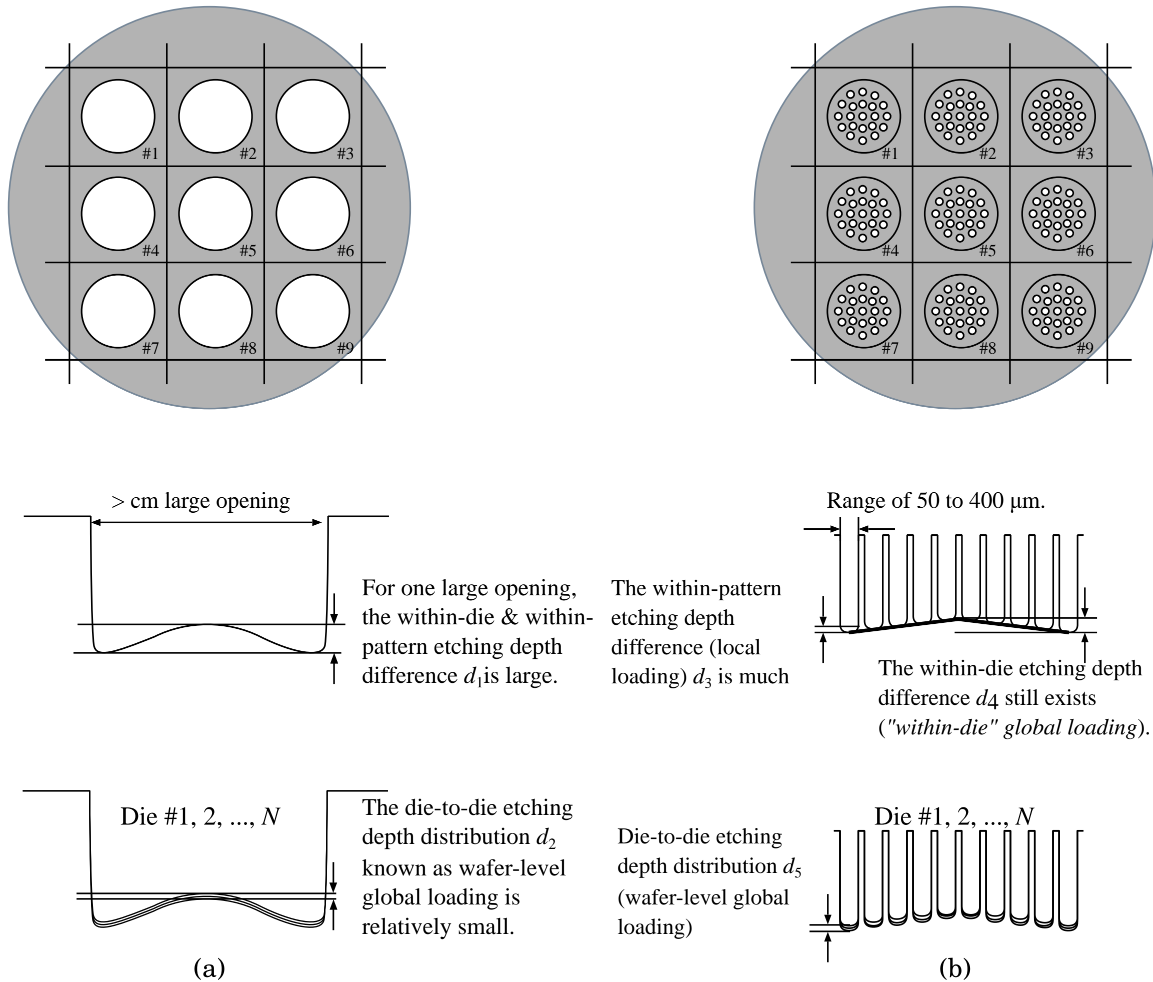


Fig. A.2: Etching depth distribution in a wafer (a) with single large-opening patterns and (b) with filling mesh opening patterns.

A.1.2 Fabrication issues of large MEMS structures

In processing a large opening, the etching depth difference between the center and edge of the opening is one of the critical issues. The difference causes damage to the structure before all the backside substrate is etched out. Therefore, it is essential to uniformize the etching depth distribution. However, owing to the nature of deep reactive ion etching (DRIE), the etching rate is nonuniform.

The main issue of etching nonuniformity is caused by two well-known phenomena,

both related to plasma density [82], [115], [116]. The first is aspect-ratio-dependent etching (ARDE) [116]. ARDE is affected by the relationship between the etching rate and the ratio of etching hole depth to opening size (aspect ratio). In MEMS DRIE, radical species contribute to fast etching; however most of such radical species are trapped by the high-aspect-ratio wall before reaching the bottom [117]. The narrower the opening becomes, the fewer the plasma species that reach the bottom. Therefore, a larger opening is etched faster than a narrower one.

The second is global loading effect, which is related to pattern density, i.e., the area of exposed silicon [116], [118]. It causes nonuniformity in etching rate on a large scale. In such large-area etching, the ratio of the resist-protected area to the not-protected area is extremely different. In high-pattern-density areas such as the center, the plasma density is relatively lower than that in low-pattern-density areas such as the edge. This results in etching rate nonuniformity. Because of these, with the single large pattern shown in Fig. A.2a, the within-die (within-pattern) etching depth difference d_1 is large.

On the other hand, a die-to-die etching depth distribution exists because of plasma uniformity. We call the etching depth distribution d_2 the (wafer level) global loading.

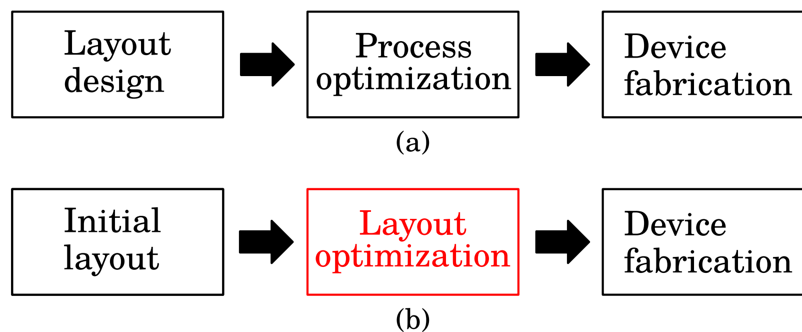


Fig. A.3: Methods of improving undesirable etching nonuniformity (a) using in-house equipment and (b) through a MEMS foundry. Process optimizations are impossible since the foundry process is fixed and the optimization has to be carried out in the design step.

Despite continuous effort of equipment developers to reduce d_2 [119], [120] by providing wafer-level-uniform plasma, the equipment improvement does not directly contribute to d_1 reduction because d_1 is induced at the chip level and is pattern dependent.

Such chip-level depth difference (i.e., d_1) is one of the main causes of process failure for large-area MEMS devices. In the case of a MEMS mirror, a silicon-on-insulator (SOI) is used and the back-side silicon of the MEMS mirror must be etched out completely. The buried oxide (BOX) is expected to protect the MEMS mirror throughout the entire backside etching; the first-formed SiO_2 part is continuously exposed to heavy bombardment by the etching species, while waiting for the large opening to be etched out. The time difference from the first SiO_2 exposure to the end of etching is proportional to the depth difference d_1. The larger d_1 becomes, the longer the "overetching time" must be, then the higher the risk of SiO_2 protection layer breaking during the process. d_1 tends to increase in proportion to the release diameter. To reduce such risk, one of the "right things" to do is to optimize etching conditions to decrease d_1 depending on the designed pattern, as shown in Fig. A.3(a); however, such optimization is not always possible, for example, when using an external foundry service that refuses process optimization and/or in the case of rapid prototyping where MEMS designers have limited time.

In this article, we propose a method of uniformly etching a deep large-area opening using only *as-is-given* process conditions. As shown in Fig. A.3(b), it is the layout, not the process condition, that is optimized. Our method enables device engineers to obtain a large opening by a given standard process, without any etching condition optimization. To show the feasibility of the proposed method, a MEMS mirror with a large backside opening of over 1 cm^2 was successfully fabricated using the result of the test structure measurement.

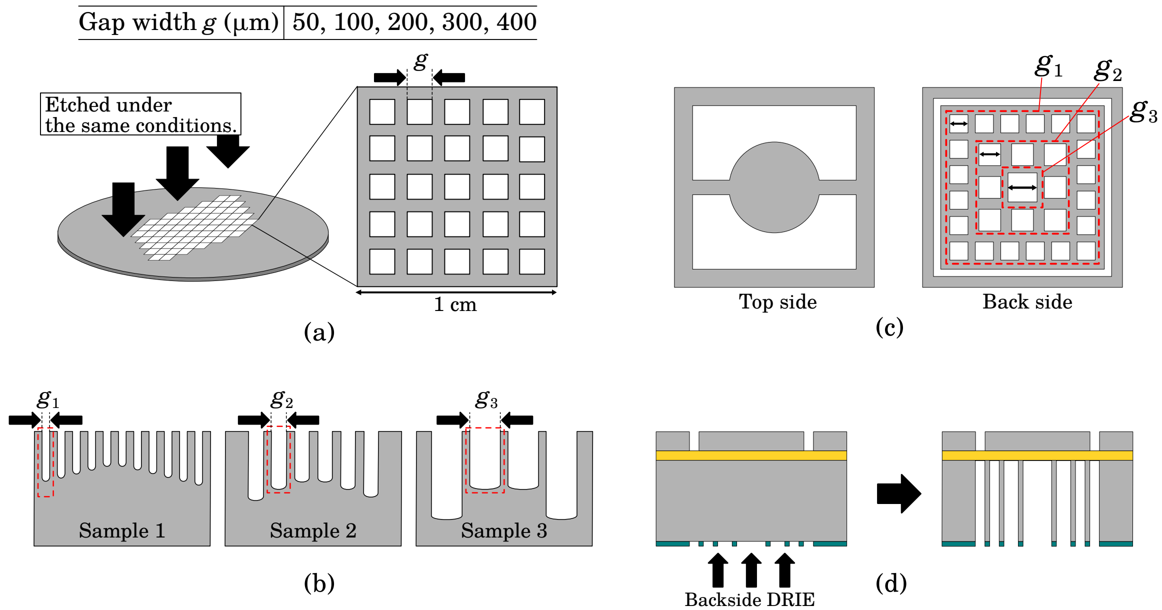


Fig. A.4: Proposed method of large-hole DRIE with a compensated dummy mesh pattern to increase uniformity. (a) Designing mesh structures.The gaps of the meshes are different from each other. All the test structures are etched under the same conditions. (b) The etching depth distribution is measured. (c) Designing MEMS structure that needs large-hole backside etching. The backside is a compensated dummy mesh pattern using the test structure measurement result. (d) Fabricated by standard process, which does not need any process alternation.

A.2. Proposed method

Our method proposes to fill a large opening with a "compensated mesh" pattern. The opening diameter g is gradually changed from the largest at the center to the smallest at the edge of the initial opening. g is defined according to the value obtained by a single test structure etching and measurement process.

When a large hole is replaced by smaller openings as shown in Fig. A.2b, the depth difference between the wall and the center of *the same* hole, d_3 (hereafter, denoted as the "within-pattern" difference), becomes substantially smaller than the original difference d_1. Many methods of uniform etching found in the literature [121]–[126] put dummy

fillers having the same hole size, to exploit the notion that $d_3 < d_1$. However, there still exists a non-negligible depth difference between the edge and center of the mesh, d_4 (hereafter, denoted as the "within-die" difference). d_4 is still large. It ranges from 11.7% (25 µm/212.5 µm) to 18.2% (50 µm/275 µm) of the etching depth, as will be reported later in this article (Fig. A.6). To further reduce d_4, we propose a new method. Note that the depth *distribution*s in between different chips on a wafer, d_2 in Fig. A.2a and d_5 in Fig. A.2b, are relatively small and can be independently improved by machine and process developers; therefore, they are beyond this article's scope.

Our method enables device engineers to obtain a large opening by a given standard process, without any etching condition optimization. To show the feasibility of the proposed method, a MEMS mirror with a large backside opening of over 1 cm^2 was successfully fabricated using the result of the test structure measurement.

Figure A.4 shows the proposed process steps. Several wafers having mesh structures of different hole gaps g are pattened and etched under the same DRIE conditions [Fig. A.4(a)]. After etching, all the etched meshes are observed and the etching depth as well as the within-die depth distribution d_4 are measured [Fig. A.4b]. From the test structure measurement, the "compensated mesh" pattern is designed. The gap of the mesh is determined to maintain the same etching depth over the entire hole area. For example, as shown in Fig. A.4(c), the gap at the center is set to the largest value (g_3) to compensate for the lowest etching rate, which is due to the within-die global loading. On the other hand, the gap at the hole fringe is set to the smallest value (g_1) to reduce the high etching speed. Using the pattern, uniform backside etching can be obtained with no process alterations [Fig. A.4(d)]. Once the d_4 dependence on specific mesh size and the distance from the pattern fringe is obtained, dummy mesh patterns for different large-opening patterns can be

designed in the same manner.

A.3. Results of test structure measurements and proposed compensated pattern

We prepared five test structures as shown in Fig. A.4(a). The pattern consisted of square holes of a certain size that filled a 1 cm^2 square area at 10 μm intervals. The size of each hole was parameterized as g, and five samples with g values of 50, 100, 200, 300, and 400 μm were tested.

The test structures were fabricated on a 525-μm-thick bulk silicon wafer. First, a 1-μm-thick EB resist (TOK OEBR CAP-112) was coated and patterned by direct EB writing. Then, DRIE was performed to etch the test structure. The DRIE conditions are shown in Table A.1 using an SPP Technologies MUC21-ASE Pegasus ICP etching machine. All the test structures with different gaps were processed under the same condition. After removing the resist by O_2 plasma ashing, all the processed samples were cleaved and

Table A.1: DRIE conditions used in the experiments

Step	Section	C_4F_8 (sccm)	SF_6 (sccm)	Time (s)	Pressure (Pa)	Coil (W)	Bias (W)
Deposition	Fluorocarbon deposition	400	–	2.5	6.0	2500	0
Etching	Removing bottom fluorocarbon	–	300	2.5	4.0	2500	80
	Isotropic etching of Si	–	300	6.0	20.0	2500	20

Table A.2: Maximum distributions with uniform gaps.

Gap g (μm)	50	100	200	300	400
Max. difference d_4 (μm)	25	28	40	50	50

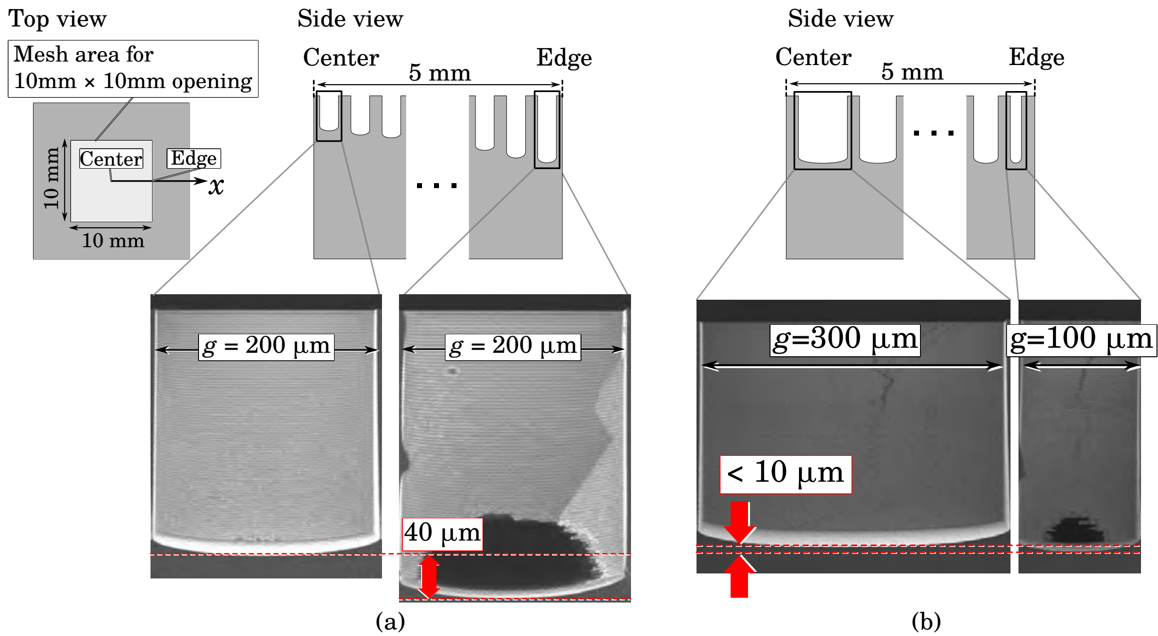


Fig. A.5: Cross-sectional views of (a) the g = 200 µm mesh pattern at the center and edge and (b) the proposed compensated mesh pattern at the center and edge.

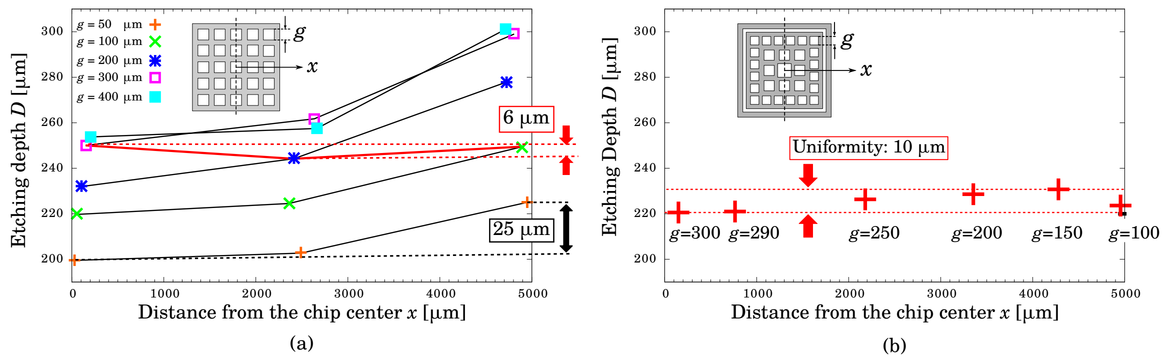


Fig. A.6: (a) Results of the measurement of etching depth distribution using test structures. If the gap is compensated for, the gap can be reduced to 6 µm. (b) Results of etching depth distribution determined using the compensated mesh pattern. The gap of the mesh was 300 µm at the center and gradually reduced to 100 µm at the edge. The distribution was reduced to 10 µm.

their cross-sectional views were observed for the measurement of etching depth using a scanning electron microscope (SEM). The etching depth of each opening in each sample was measured.

Figure A.5a shows cross-sectional views of the $g = 200$ µm mesh pattern at the center and edge. It shows that the etching depth difference between the center and edge is $d_4 = 40$ µm. Figure A.6a shows the etching depth difference of the test structures. Table A.2 shows the maximum etching depth difference d_4 dependence on g. In the structure with a constant mesh gap, the etching depth at the center of the device is at least 25 µm shallower than at the edge of the sample. Figure A.6a also shows that, if the gap is optimally chosen, that is, 300 µm at the center and 100 µm at the edge, the etching depth difference can be reduced to 6 µm.

Then, a proposed mesh pattern was fabricated on a silicon wafer. The gap was 300 µm at the center of the mesh patten, and gradually decreased to 100 µm at the edge of the pattern. Figure A.5b shows cross-sectional views of the compensated mesh patterns. Figure A.6b shows the result of etching distribution determined using the compensated mesh pattern. The process conditions were the same as those for the test structure measurement. However, the etching depth difference was reduced to 10 µm. This indicates that the DRIE distribution was successfully uniformized not by tuning the process condition but by optimizing the backside layout.

A.4. MEMS mirror fabrication using the test structure results

In this section, the application of a large-area backside etching is reported. The demonstrated example was a MEMS mirror. Details of the mirror designs and characteristics are omitted in this article because the scope of this article is only the reliable fabrication of the device, and the method discussed is applicable to all types of existing and/or future mirror designs.

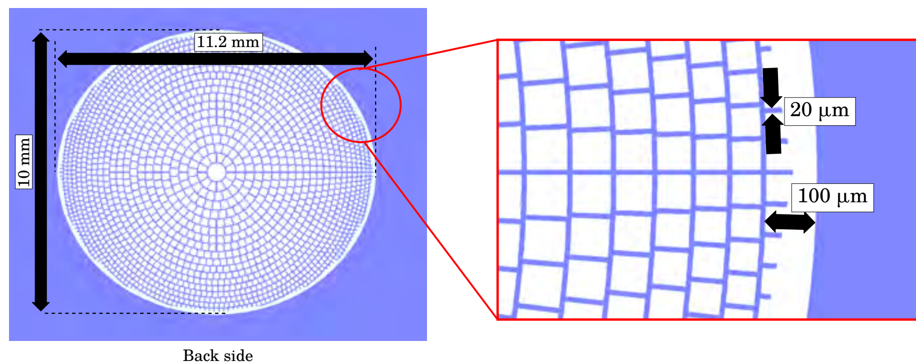


Fig. A.7: Backside layout of fabricated device. The compensated mesh pattern was designed for uniform etching distribution.

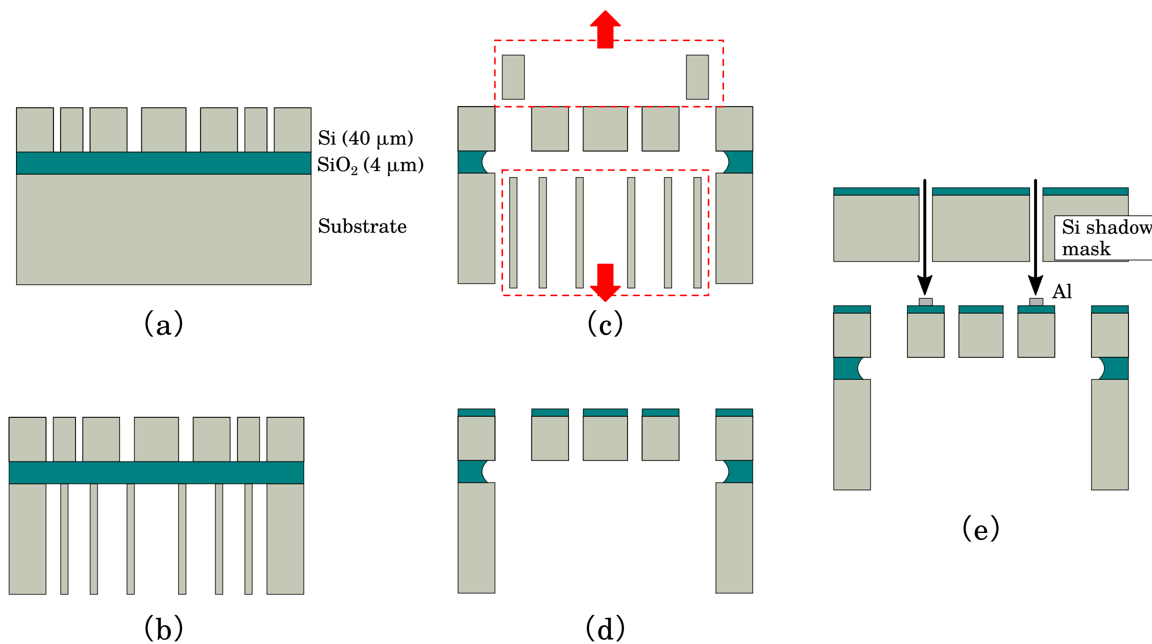


Fig. A.8: Process flow of fabricating the mirror device using the proposed compensated mesh pattern on the backside. (a) Patterning and DRIE of a top-side Si. (b) DRIE of a backside substrate. The proposed mesh pattern is used. (c) Removed unnecessary dummy pattern using HF acid. (d) Sputtering 500 nm SiO_2 as an insulating layer. (e) Depositing and pattening Al wire using a Si shadow mask.

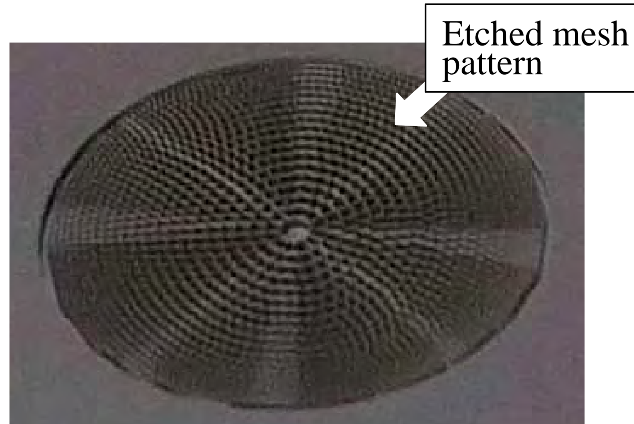
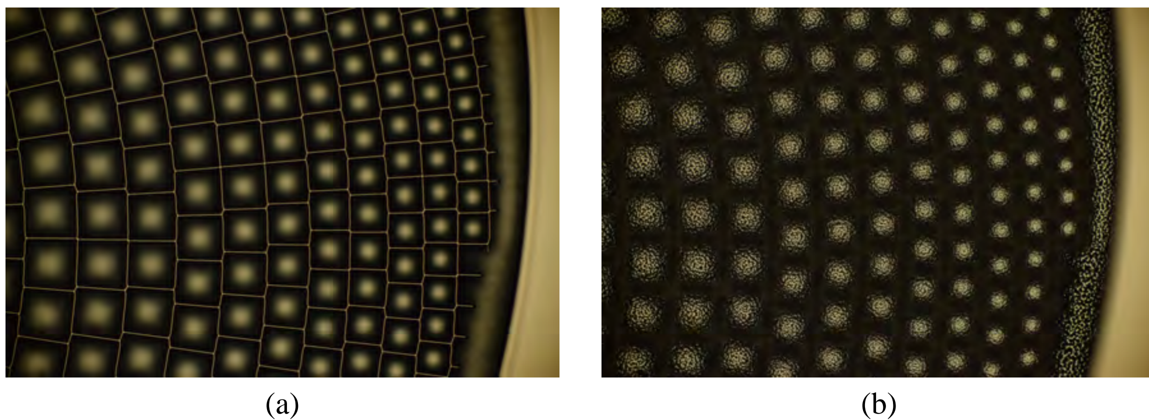


Fig. A.9: Photograph of the device under backside etching. The proposed compensated mesh pattern is clearly visible.



(a) (b)

Fig. A.10: Photomicrographs of the (a) top and (b) bottom of the mesh pattern.

Figure A.7 shows the backside layout with the compensated mesh pattern. The size of the front-side layout frame was 10×8 mm^2, including the mirror structure and the dummy filling patterns for reducing the thermal impact of a large hole. To expose the whole MEMS mirror, the etching of an 11.2×10 mm^2 oval area was necessary. Following the results of the test structure measurements, the large backside opening was filled with the compensated mesh pattern. The size of the openings was gradually changed from the center to the edge of the etched area. For simplicity of the layout, the large center hole was designed as a circle

and the rest of the holes were square. The size of the center circle opening was 660 μm, and the size of the square pattern was linearly changed from 320 μm at the center to 120 μm at the edge. The mesh pattern was isolated from the outer area by 100 μm to ensure the removal of the mesh pattern.

Figure A.8 shows the process flow of the device. An SOI wafer composed of a 40-μm-thick device layer, a 4-μm-thick BOX, and a 500-μm-thick handling wafer was used. The wafer was cut into 2×2 cm^2. First, a 2-μm-thick photoresist (JSR PFR 7790G) was spin-coated and patterned by UV lithography. Then, DRIE was performed to etch the MEMS mirror structure [Fig. A.8(a)]. On the backside, a 7.1-μm-thick photoresist (AZ P4620) was patterned, followed by through-the-wafer DRIE [Fig. A.8(b)]. During the DRIE, the chip was fixed on a 4-inch silicon wafer covered with aluminum. Diffusion pump oil was put as a heat transfer material and four sides were firmly covered with polyimide tape. Figure A.9 shows a photograph of the device under backside etching, on which the mesh pattern is clearly visible. The device was observed by optical microscopy. Figures A.10(a) and A.10(b) show photomicrographs of the top and bottom of the mesh pattern. Uniform etching was confirmed by observing the mesh bottom [Fig. A.10(b)].

After the DRIE of both sides, oil was washed with hexane and then the photoresist was removed using acid Piranha solution (H_2O_2/H_2SO_4/H_2O). The MEMS mirror was released by etching the BOX layer in 50% HF acid solution [Fig. A.8(c)]. Both backside mesh and front-side dummy patterns on both sides were simultaneously removed. Next, a 500-nm-thick SiO_2 insulating layer was sputtered [Fig. A.8(d)]. Finally, an Al wire was deposited using a silicon shadow mask, which was fabricated by the DRIE of a 525 μm silicon wafer [Fig. A.8(e)]. A MEMS mirror driving experiment was performed using a Laser Doppler vibrometer and clear resonance operation was confirmed, thus showing the

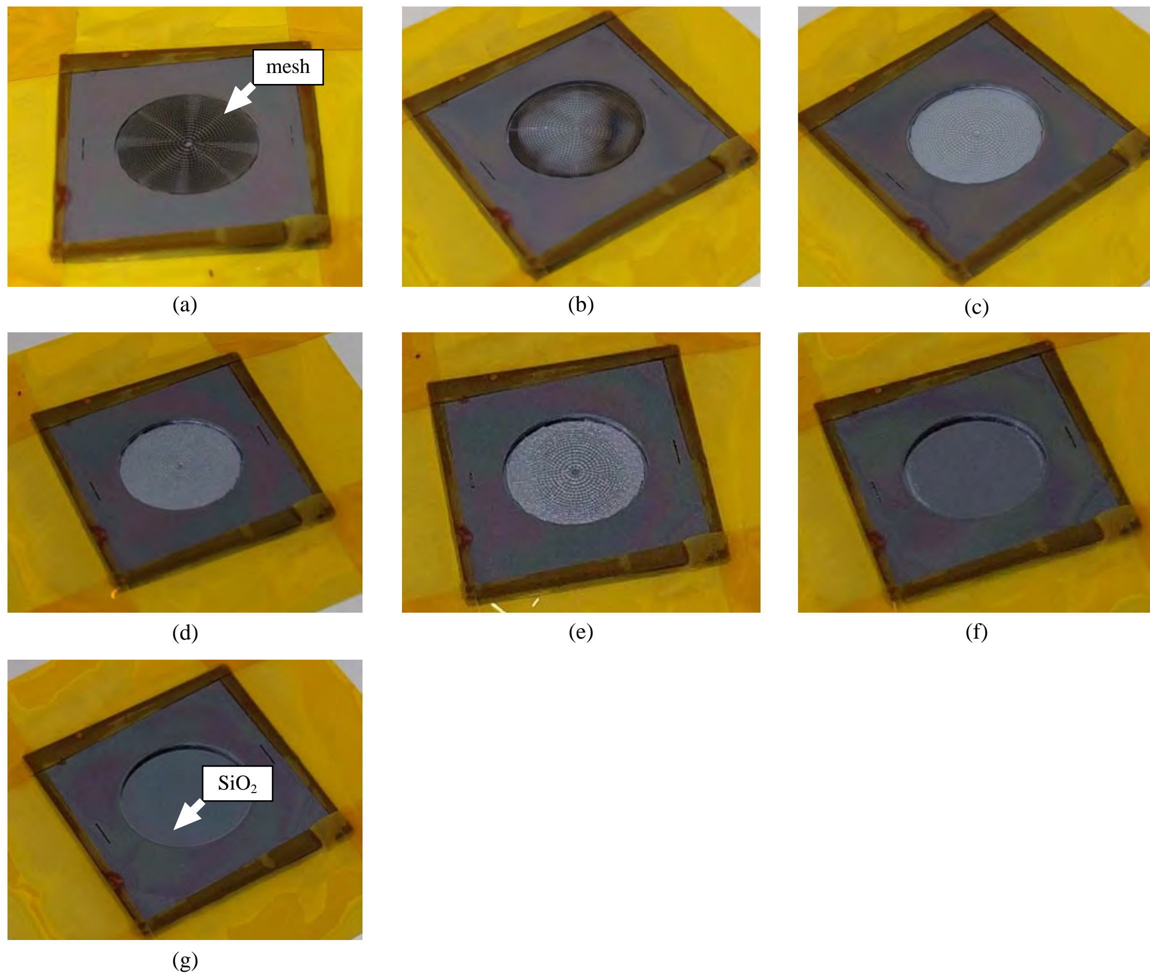


Fig. A.11: Simultaneous backside etching and mesh pattern removal method was applied to the 11.2 × 10 mm^2 oval opening DRIE over 500 µm. (a) After DRIE, (b) 4 min SF_6 etching, (c)-(f) + 4 min SF_6 etching each, (g) total 24 min SF_6 isotropic etching revealed SiO_2 completely.

applicability of the proposed large-area etching process.

A.4.1 Towards higher reliability: all-dry uniform backside etching

The successful fabrication of a large-area MEMS demonstrated the applicability of the proposed methods for backside DRIE of a large MEMS. However, the removal of dummy filler patterns may be problematic for reliable MEMS fabrication. For

frontside dummy removal, a couple of methods have been proposed, such as the double-lithography-and-etching method called "contour lithography" [127]. For backside etching, we propose a combined process of anisotropic deep etching and isotropic dummy removal. As shown in Fig. A.10, DRIE using the compensated mesh pattern stops before reaching the BOX layer; then isotropic etching simultaneously reveals the BOX SiO_2 surface and removes the unnecessary mesh.

The same compensated mesh used in the previous experiment was patterned on the 7.1-µm-thick photoresist (AZ P4620) on the backside of the SOI chip. Then DRIE using the parameter in Table A.1 was performed for 100 cycles. Then 23 cycles of DRIE were performed under "milder" conditions: coil power was reduced to 1500 W, and bias power was reduced to 0, 45, and 10 W for Teflon deposition, Teflon removal, and silicon etching, respectively. In this example, the resist almost disappeared after 123 cycles, probably owing to the smaller heat exchange. Then only SF_6 isotropic etching was performed with 300 sccm SF_6, a coil power of 1800 W, and a bias power of 50 W. The SF_6 isotropic etching was stopped every 4 min and the chip was optically observed.

Figure A.11 shows photographs of the progress of the isotropic etching. It was confirmed that the mesh pattern made with DRIE [Fig. A.11(a)] gradually disappeared owing to the DRIE, and after six times of 4 min isotropic etching, the backside mesh pattern was completely removed, and a flat SiO_2 surface was revealed [Fig. A.11(g)]. By comparing Figs. A.11(e) and A.11(f), it is confirmed that most of the silicon substrate patterns have been removed, thereby showing the high uniformity of the proposed process.

A.5. Conclusions

The author proposed a method of uniform backside etching of wafers for large (centimeter order) MEMS devices. The "compensated mesh" pattern, whose density and gap are gradually changed from the center to the edge of the opening achieves uniformity by inversely compensating for the global loading by the local loading. The method does not need any etching condition optimization, thereby enabling device engineers to obtain a large opening using only an *as-is-provided* standard process. The gap of the mesh pattern filling a large-opening hole area on the backside is defined by the test structure measurement. As a result, the gap size gradually changes from the largest at the center to the smallest at the edge. In the test structure measurement, we confirmed that the proposed mesh pattern reduces the difference in etched depth from 50 to 10 μm. Using the test structure measurement result, we successfully performed the backside etching of a 11.2×10.0 mm^2 oval area, which provided a working MEMS mirror device. Towards more reliable processes, we also demonstrated a method of removing mesh patterns at the end of the process by SF_6 isotropic etching.

APPENDIX B

Closed-Loop EOF Micropump

In this section, a closed-loop EOF micropump is demonstrated. Figure B.1 shows the schematic of a designed closed-loop EOF micropump. Figure B.2 shows the hydrodynamic equivalent circuit of a closed-loop EOF micropump. Although the pressure difference between the inlet and outlet (Δp_{ext}) is zero in the closed-loop condition, there is a counter EOF. In the experiment, five narrow channels are designed as EOF micropump areas, and the other fluid channels are wider than the EOF channels. As the EOF in the narrow channels is stronger than the counter EOF flow in the other channels, this asymmetric design totally generates a unidirectional flow in the channel, as shown in Fig. B.1.

Figure B.3 shows the fabrication processes of the closed-loop EOF micropump. First, the 525 μm-thick silicon wafer is thermally oxidized. Then, the Ti/Au electrodes are sputtered and patterned using gold etched (AURUM-302, KANTO KAGAKU) and 5% APM. PDMS is patterned by using a silicon mold, where the channels are patterned by DRIE. After the PDMS substrate is peeled off, two holes are made to introduce liquid into the channel. Figure B.4 shows the close-up image of the channel.

We used 1.0×10^{4}M KCl solution for the fluid and 500-nm free-charge micro to observe

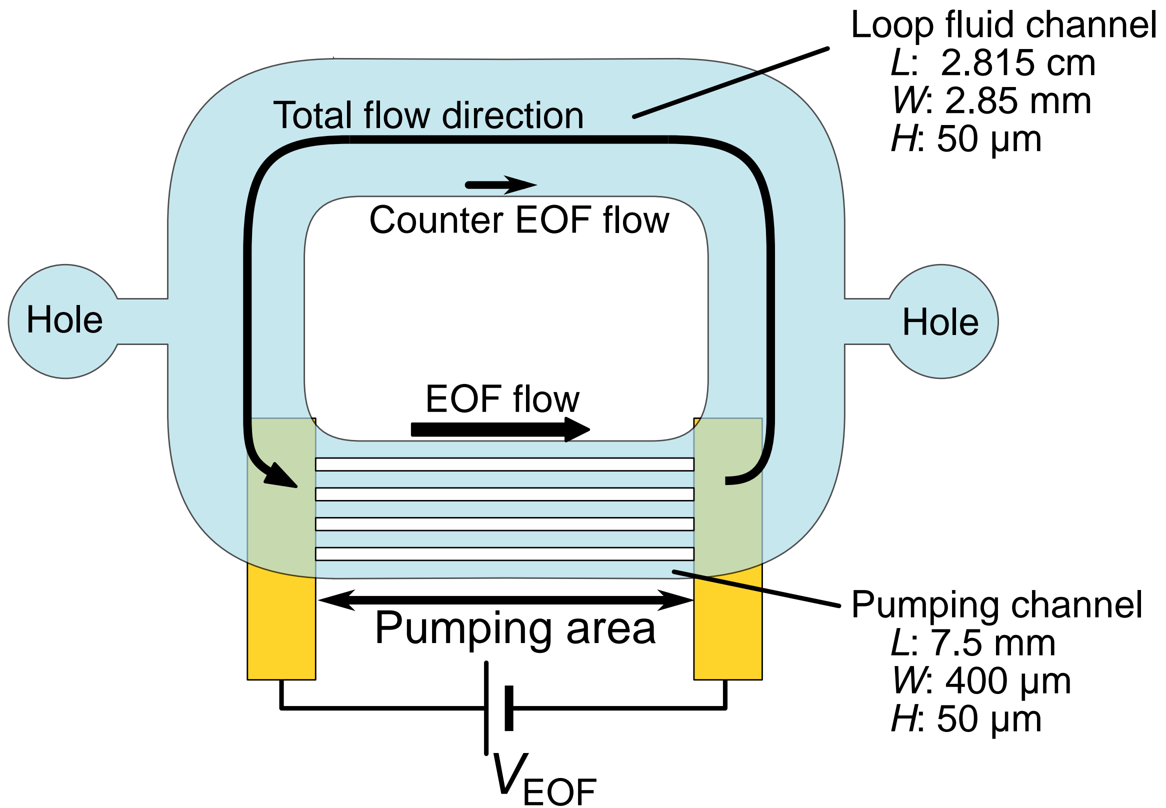


Fig. B.1: Schematic of a closed-loop EOF micropump.

the flow speed using a microscope. After the introduction of the solution and micro-beads, we applied a voltage of 100 V to the EOF electrodes using an HV power supply. Figure B.5 shows the close-up image of the narrow channel. In the experiment, the flow speed in the closed-loop channel is 141 μm/sec.

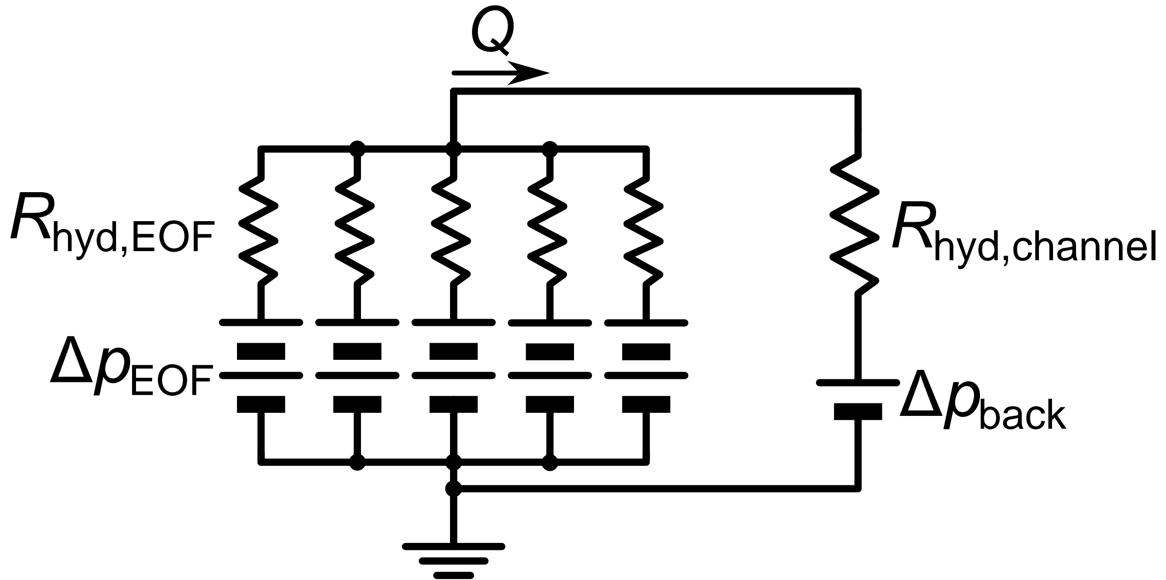


Fig. B.2: Schematic of the hydrodynamic equivalent circuit of a closed-loop EOF micropump.

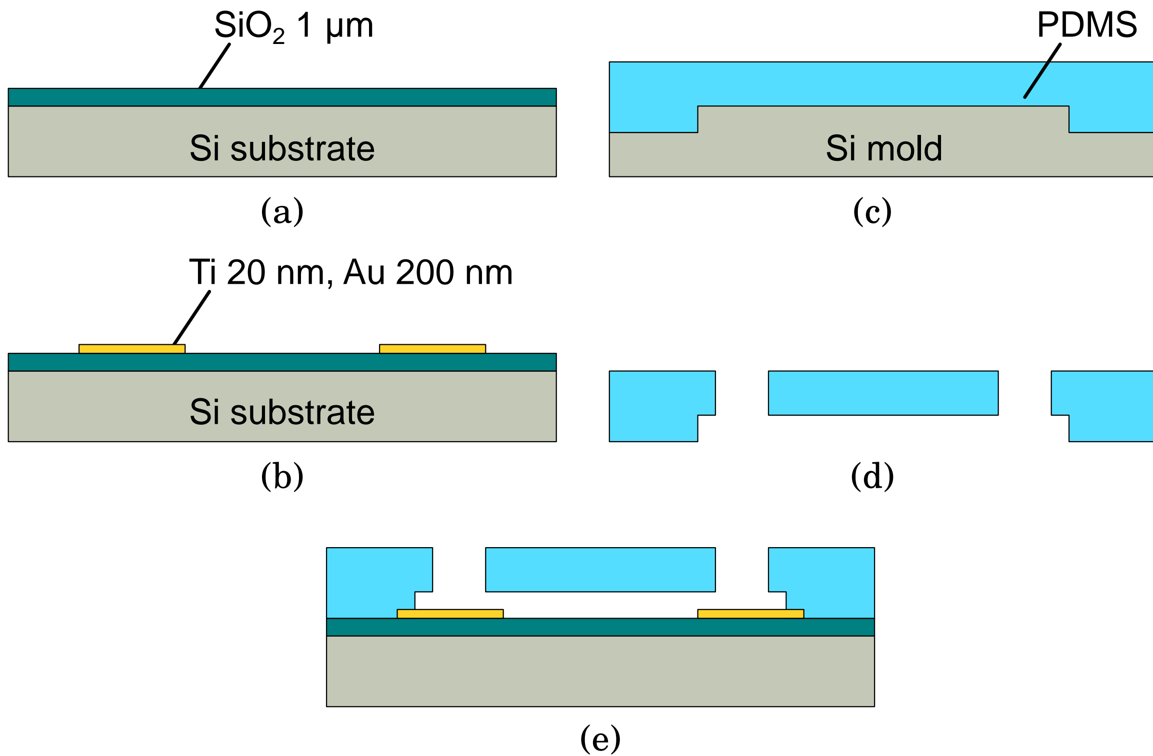


Fig. B.3: Process flow of a closed-loop EOF micropump. (a) Si substrate is thermally oxidized. (b) EOF electrodes are patterned. (c) PDMS is patterned using a Si mold. (d) PDMS is peeled off, and holes are made. (e) Si substrate and PDMS are bonded using O_2 plasma activation.

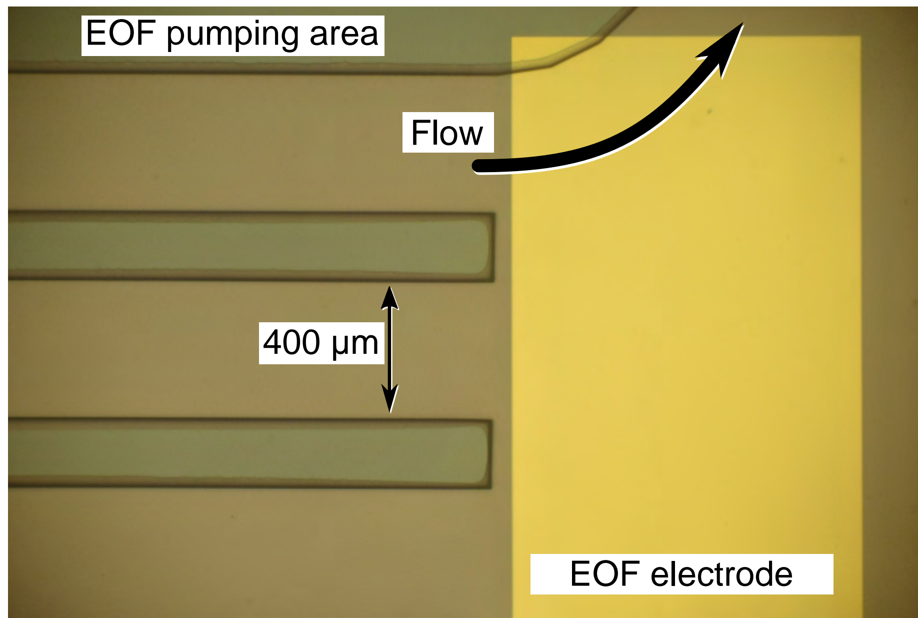


Fig. B.4: Close-up image of a fabricated closed-loop EOF micropump.

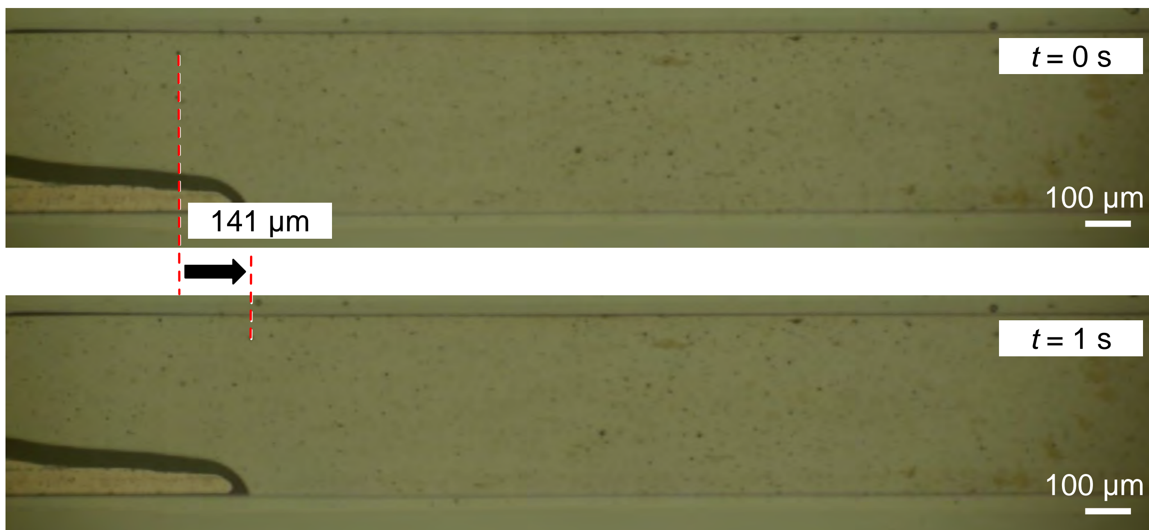


Fig. B.5: Micrographs of the closed-loop EOF micropump when V_{EOF} = 100 V. Velocities of three micro-beads are measured.

APPENDIX C

VOLTAGE DISTRIBUTION IN AN EOF MICROPUMP

In this section, voltage distribution in a micro-channel of an EOF micropump is investigated. As explained in Chapter 1, an EOF micropump requires the electric field to make a flow, as shown in Fig. 1.6 and Eq. 1.1. Therefore, the electric field must be uniformly distributed in micro-channels of the EOF micropump. However, in the conventional electrochemical reaction of liquid, the voltage drop is caused only by the electrolysis at the electrodes, and the voltage is constant in the bulk liquid, as shown in Fig C.1a. This is because the electrolytic liquid used in the conventional experiment has high conductivity, and the IR drop can be ignored. Although it is suitable for electrolytic reactions to accelerate the reactions, the IR drop requires to increase, as shown in Fig C.1b. Therefore, to increase the IR drop, the electrical resistance in micro-channels must be high. To confirm the voltage distribution for the required electric field, we investigated the voltage distribution in the micro-channel.

Figure C.2 shows the design of the measurement device. To measure the voltage distribution, we put four electrodes in the micro-channel. The two electrodes are used

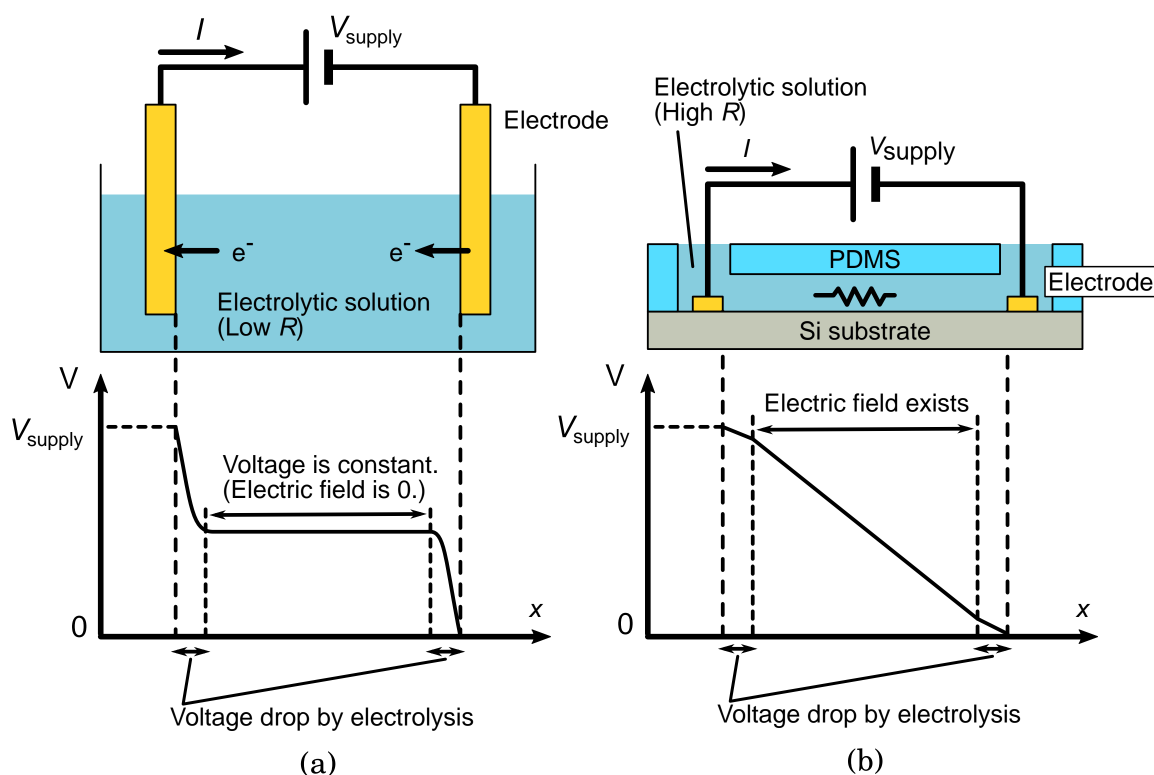


Fig. C.1: schematic of voltage distribution of (a) a conventional electrochemical experiment and (b) a microfluidic experiment.

to measure the voltages around the electrodes (V_1 and V_4), and the other two electrodes are used to measure the voltages in the micro-channel (V_2 and V_3). The fabrication process is the same as the closed-loop EOF micropump in Appendix B, as shown in Fig. B.1.

We used 0.2 M phosphate buffered saline (PBS), having a pH of 6.8 for the liquid. The driving voltage of the EOF micropump (V_{EOF} is set to 100 V. We measured the four voltages (V_1, V_2, V_3, and V_4) simultaneously using an oscilloscope. Figure C.3 shows the measurement result. In the inlet and outlet holes, the voltages are constant since the amount of the liquid is enough. On the other hand, there is an IR drop between both ends of the micro-channel. It indicates that the electric field exists in the micro-channel to drive the EOF micropump.

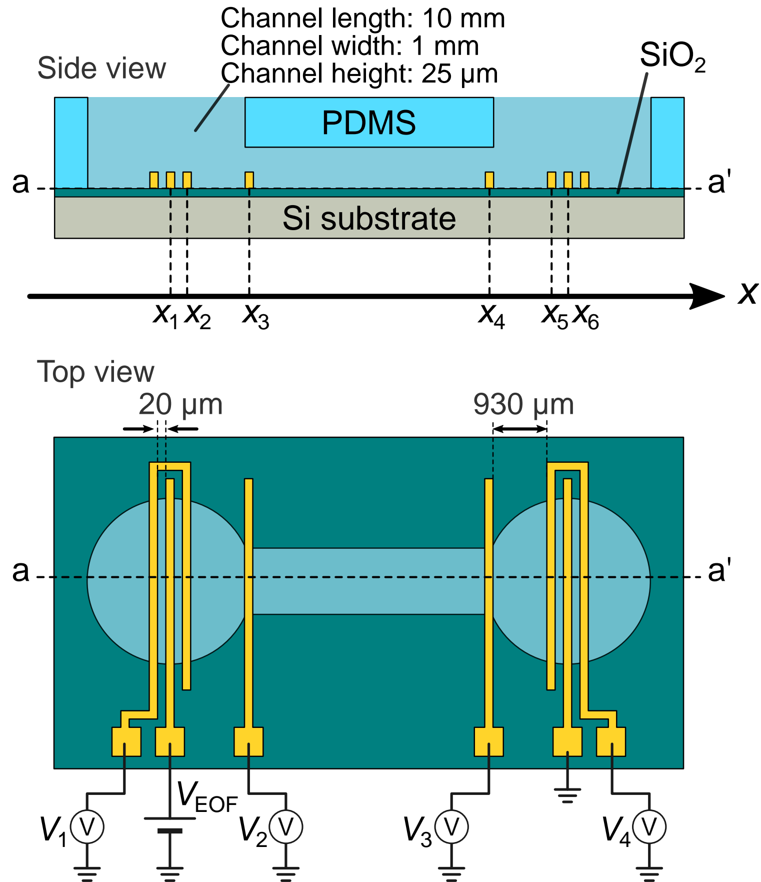


Fig. C.2: Design of the measurement device. Two electrodes are used for an EOF micropump, and the other four electrodes are used to measure the voltage distribution.

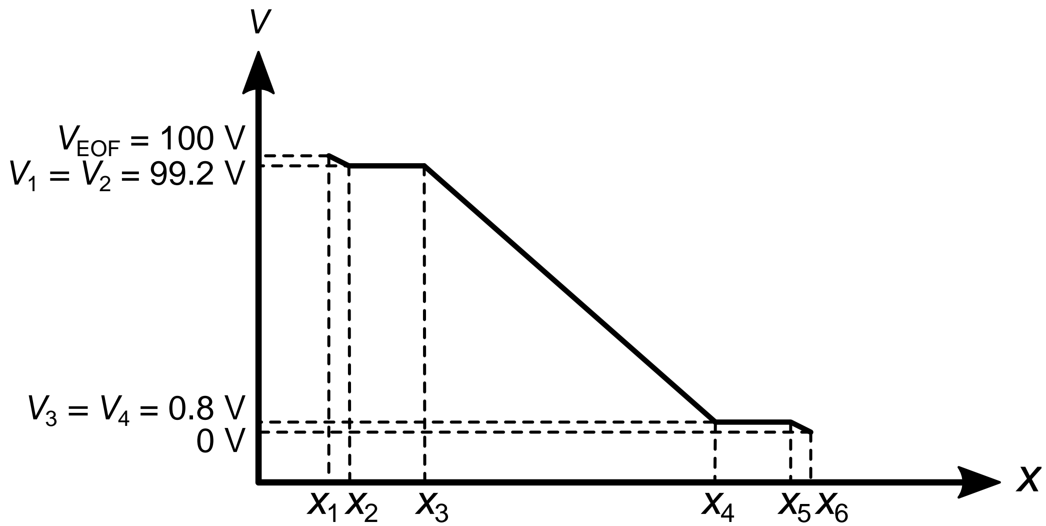


Fig. C.3: Measurement result of the voltage distribution.

APPENDIX D

FEM Simulation of The Heat Transfer in The Experimental Setup

In this section, FEM simulation results of the device used in cooling measurement in Chapter. 6 is presented. Figure D.1 shows the detailed dimensions of the printed circuit board (PCB) and the fabricated silicon device having a heat source and micro-channel. In the FEM simulation, we supposed thermal dissipation, including natural convection, conduction to the atmosphere, and radiation from the outer surface of the PCB and device as the boundary condition. The room temperature is set to 25°C.

Figure D.2 shows the measurement results without EOF flow and FEM simulation result. At the beginning of the measurement ($t < 100$ s), the FEM simulation result does not correspond to the measurement simulation result. This is because the FEM simulation goes to the next step before the calculation converges well. In the part where the convergence is progressed ($t > 100$ s), the FEM simulation result corresponds to the measurement result.

Although the heat dissipation without EOF flow is simulated, simulation with EOF is quite difficult. This is because the experiment involves not only sensible heat cooling but latent heat cooling. It makes us simulate the condition difficult.

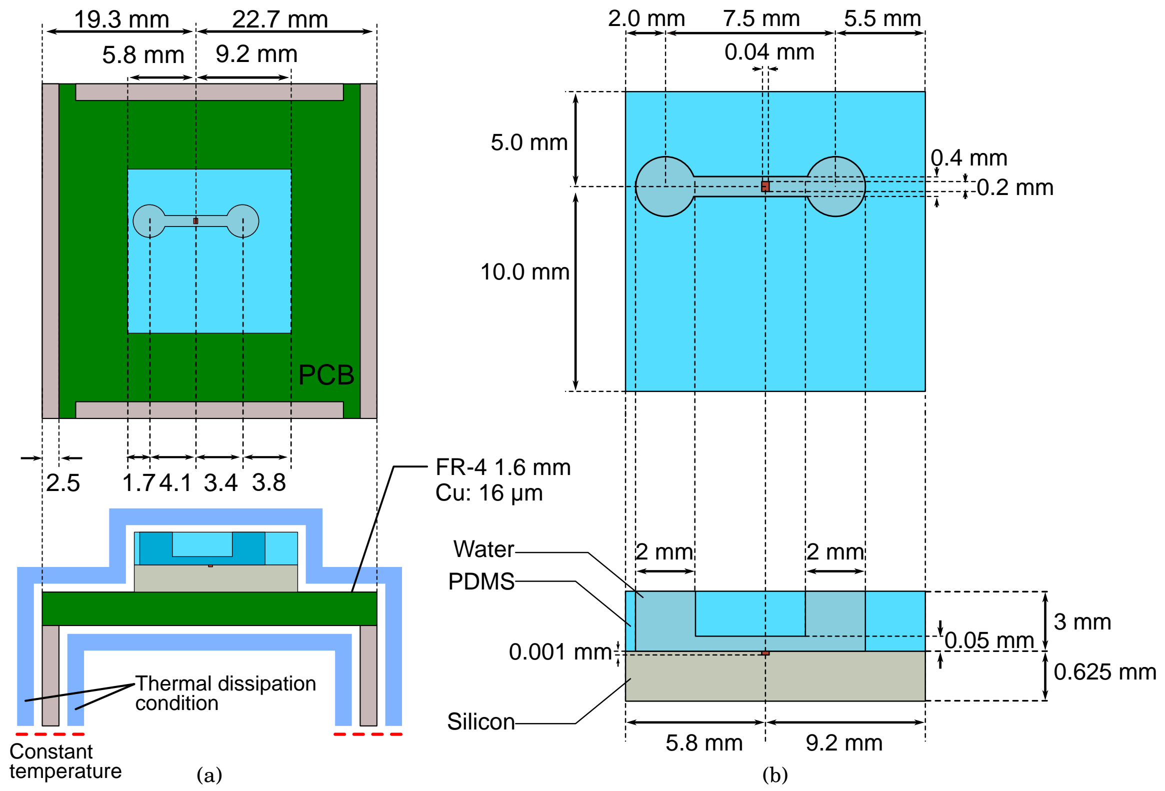


Fig. D.1: Dimensions of (a) a PCB and (b) silicon device.

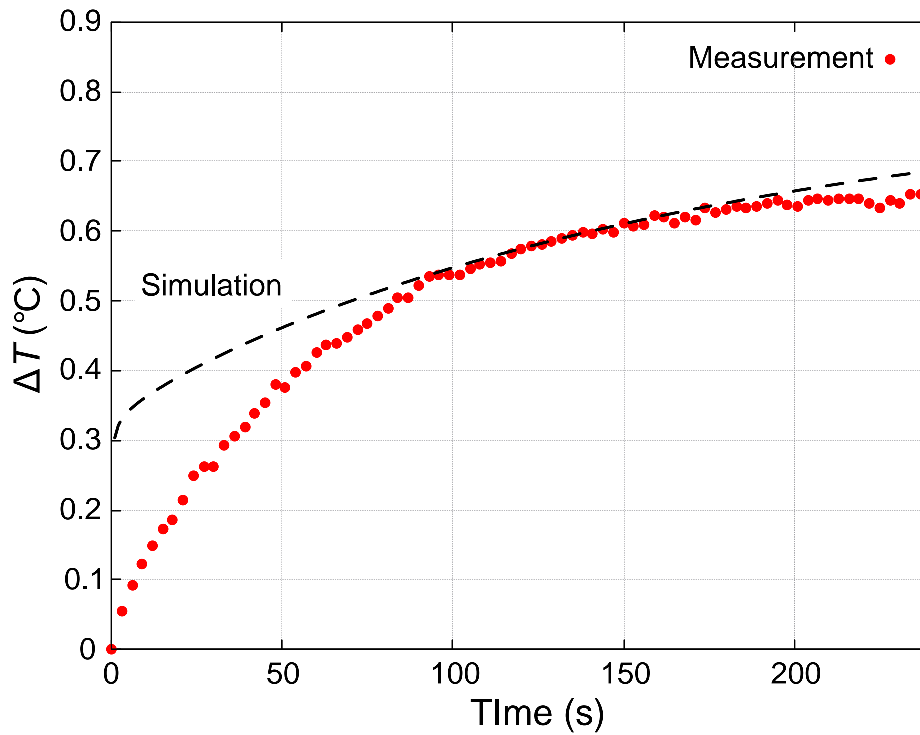


Fig. D.2: Measurement result and FEM simulation result of the change of temperature.

References

[1] I. Ferain, C. A. Colinge, and J.-P. Colinge, “Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors,” *Nature*, vol. 479, no. 7373, p. 310, 2011.

[2] Y. J. Yoon, B. D. Jeon, B. S. Kim, K. U. Kim, T. Y. Lee, N. Kwak, W. Y. Shin, N. Y. Kim, Y. Hong, K. P. Kang, D. Y. Ka, S. J. Lee, Y. S. Kim, Y. K. Noh, J. Kim, D. K. Kang, H. U. Song, H. G. Kim, and J. Oh, “18.4 an 1.1v 68.2gb/s 8gb wide-io2 dram with non-contact microbump i/o test scheme,” in *ISSCC*, Jan 2016, pp. 320–322.

[3] K. Sohn, W.-j. Yun, R. Oh, C.-s. Oh, S.-y. Seo, M.-s. Park, D.-h. Shin, W.-c. Jung, S.-h. Shin, J.-m. Ryu, H.-s. Yu, J.-h. Jung, H. Lee, S.-y. Kang, Y.-s. Sohn, J.-h. Choi, Y.-c. Bae, S.-j. Jang, and G. Jin, “A 1.2 V 20 nm 307 GB / s HBM DRAM with At-Speed Wafer-Level IO Test Scheme and Adaptive Refresh Considering Temperature Distribution,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 250–260, 2017.

[4] L. T. Su, S. Naffziger, and M. Papermaster, “Multi-chip technologies to unleash computing performance gains over the next decade,” in *IEDM*, vol. Part F134366, 2017, pp. 1.1.1–1.1.8.

[5] M. Sadri, M. Jung, C. Weis, N. Wehn, and L. Benini, “Energy optimization in 3D MPSoCs with Wide-I/O DRAM using temperature variation aware bank-wise

refresh," in *DATE*, March 2014, pp. 1–4.

[6] K. Tran, "Scaling the Next-Generation System Architecture," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 35–42, 2016.

[7] S. M. Sohel Murshed and C. A. Nieto de Castro, "A critical review of traditional and emerging techniques and fluids for electronics cooling," *Renewable and Sustainable Energy Reviews*, vol. 78, no. April, pp. 821–833, 2017.

[8] J. Kirshberg, K. Yerkes, D. Trebotich, and D. Liepmann, "Cooling effect of a mems based micro capillary pumped loop for chip-level temperature control," in *ASME MEMS*, vol. 2, 2000, pp. 1–8.

[9] T. Shioga and Y. Mizuno, "Micro loop heat pipe for mobile electronics applications," in *IEEE SEMI-THERM*, vol. 2015-April, 2015, pp. 50–55.

[10] S. H. Moon and G. Hwang, "Development of the micro capillary pumped loop for electronic cooling," in *THERMINIC*, no. September, 2007, pp. 72 – 76.

[11] B. He, M. Wei, S. Somasundaram, C. S. Tan, and E. N. Wang, "Experiments on the Ultrathin Silicon Vapor Chamber for Enhanced Heat Transfer Performance," in *IEEE ITherm*, 2016, pp. 3–7.

[12] J. Liang, M. S. Bakir, and Y. Joshi, "Microfabricated Thin Silicon Vapor Chamber for Low Profile Thermal Management," in *IEEE ITherm*, vol. 0, 2017.

[13] M. Redmond, K. Manickaraj, O. Sullivan, S. Mukhopadhyay, and S. Kumar, "Hotspot cooling in stacked chips using thermoelectric coolers," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 5, pp. 759–767, 2013.

[14] H. F. Hamann, A. Weger, J. A. Lacey, Z. Hu, P. Bose, E. Cohen, and J. Wakil, "Hotspot-limited microprocessors: Direct temperature and power distribution

measurements," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 56–64, 2007.

[15] B. Dang, E. Colgan, F. Yang, M. Schultz, Y. Liu, Q. Chen, J. W. Nah, R. Polastre, M. Gaynes, G. McVicker, P. Parida, C. Tsang, J. Knickerbocker, and T. Chainer, "Integration and Packaging of Embedded Radial Micro-Channels for 3D Chip Cooling," in *ECTC*, vol. 2016-Augus, 2016, pp. 1271–1277.

[16] D. B. Tuckerman and R. F. W. Pease, "High-performance heat sinking for vlsi," *IEEE Electron Device Letters*, vol. 2, no. 5, pp. 126–129, May 1981.

[17] R. S. Hale and V. Bahadur, "Electrowetting Heat Pipes for Heat Transport Over Extended Distances," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 10, pp. 1441–1450, 2015.

[18] B. Dang, M. S. Bakir, D. C. Sekar, C. R. King, and J. D. Meindl, "Integrated microfluidic cooling and interconnects for 2D and 3D chips," *IEEE Transactions on Advanced Packaging*, vol. 33, no. 1, pp. 79–87, 2010.

[19] Y. S. Kim, H. Kitada, R. Ohigashi, M. Ichiyanagi, J. Nakatsuka, I. Kinefuchi, Y. Matsumoto, and T. Ohba, "Hot Spot Cooling Evaluation using Closed-Channel Cooling System (C 3 S) for MPU 3DI Application," in *Symposium on VLSI Technology*, vol. 30, 2011, pp. 140–145.

[20] H. Kudo, Y. Oguri, A. Tsukune, Y. S. Kim, H. Kitada, K. Fjimoto, I. Kinefuchi, Y. Matsumoto, and T. Ohba, "High performance closed-channel cooling system using multi-channel electro-osmotic flow pumps for 3D-ICs," in *IEDM*, vol. 11, no. 121, 2013, pp. 735–737.

[21] Y. Zhang, C. R. K. Jr, J. Zaveri, Y. J. Kim, V. Sahu, Y. Joshi, and M. S. Bakir, "Coupled Electrical and Thermal 3D IC Centric Microfluidic Heat Sink Design and

Technology," in *ECTC*, 2011, pp. 2037–2044.

[22] D. R. Reyes, D. Iossifidis, P.-A. Auroux, and A. Manz, "Micro Total Analysis Systems. 1. Introduction, Theory, and Technology," *Analytical Chemistry*, vol. 74, no. 12, pp. 2623–2636, 2002.

[23] P.-A. Auroux, D. Iossifidis, D. R. Reyes, and A. Manz, "Micro Total Analysis Systems. 2. Analytical Standard Operations and Applications," *Analytical Chemistry*, vol. 74, no. 12, pp. 2637–2652, 2002.

[24] E. Verpoorte and N. F. De Rooij, "Microfluidics meets MEMS," *Proceedings of the IEEE*, vol. 91, no. 6, pp. 930–953, June 2003.

[25] P. Woias, "Micropumps — past , progress and future prospects," *Sensors and Actuators B: Chemical*, vol. 105, pp. 28–38, 2005.

[26] I. Lee, P. Hong, C. Cho, B. Lee, K. Chun, and B. Kim, "Four-electrode micropump with peristaltic motion," *Sensors and Actuators A: Physical*, vol. 245, pp. 19 – 25, 2016.

[27] P.-H. Cazorla, O. Fuchs, M. Cochet, S. Maubert, G. L. Rhun, Y. Fouillet, and E. Defay, "A low voltage silicon micro-pump based on piezoelectric thin films," *Sensors and Actuators A: Physical*, vol. 250, pp. 35 – 39, 2016.

[28] B. T. Chia, H.-H. Liao, and Y.-J. Yang, "A novel thermo-pneumatic peristaltic micropump with low temperature elevation on working fluid," *Sensors and Actuators A: Physical*, vol. 165, no. 1, pp. 86 – 93, 2011, transducers 2009.

[29] C.-Y. Lee, H.-T. Chang, and C.-Y. Wen, "A MEMS-based valveless impedance pump utilizing electromagnetic actuation," *Journal of Micromechanics and Microengineering*, vol. 18, no. 3, p. 035044, feb 2008.

[30] J. Darabi and H. Wang, "Development of an electrohydrodynamic injection

micropump and its potential application in pumping fluids in cryogenic cooling systems," *Journal of Microelectromechanical Systems*, vol. 14, no. 4, pp. 747–755, 2005.

[31] J. Jang and S. S. Lee, "Theoretical and experimental study of mhd (magnetohydrodynamic) micropump," *Sensors and Actuators A: Physical*, vol. 80, no. 1, pp. 84 – 89, 2000. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0924424799003027

[32] M. K. Russel, P. R. Selvaganapathy, and C. Y. Ching, "Electrohydrodynamic injection micropump with composite gold and single-walled carbon nanotube electrodes," *Journal of Microelectromechanical Systems*, vol. 24, no. 5, pp. 1557–1564, Oct 2015.

[33] E. D. Fylladitakis, M. P. Theodoridis, and A. X. Moronis, "Review on the history, research, and applications of electrohydrodynamics," *IEEE Transactions on Plasma Science*, vol. 42, no. 2, pp. 358–375, Feb 2014.

[34] A. Richter, A. Plettner, K. A. Hofmann, and H. Sandmaier, "A micromachined electrohydrodynamic (EHD) pump," *Sensors and Actuators: A. Physical*, vol. 29, no. 2, pp. 159–168, 1991.

[35] C. K. Lee, A. J. Robinson, and C. Y. Ching, "Development of ehd ion-drag micropump for microscale electronics cooling," in *THERMINIC*, Sep. 2007, pp. 48–53.

[36] C. H. Chen and J. G. Santiago, "A planar electroosmotic micropump," *Journal of Microelectromechanical Systems*, vol. 11, no. 6, pp. 672–683, 2002.

[37] C. Zhao and C. Yang, "Advances in electrokinetics and their applications in micro/nano fluidics," *Microfluidics and Nanofluidics*, vol. 13, no. 2, pp. 179–203,

Sep 2012.

[38] X. Wang, C. Cheng, S. Wang, and S. Liu, "Electroosmotic pumps and their applications in microfluidic systems," *Microfluidics and Nanofluidics*, vol. 6, no. 2, pp. 145–162, Feb 2009.

[39] M. Gao and L. Gui, "Development of a fast thermal response microfluidic system using liquid metal," *Journal of Micromechanics and Microengineering*, vol. 26, no. 7, p. 075005, jun 2016.

[40] Z. Ye, R. Zhang, M. Gao, Z. Deng, and L. Gui, "Development of a high flow rate 3-d electroosmotic flow pump," *Micromachines*, vol. 10, no. 2, p. 112, 2019.

[41] K. Yoshida, T. Sato, S. In, J.-w. Kim, and S. Yokota, "A study on an AC electroosmotic micropump using a square pole – Slit electrode array," *Sensors & Actuators: A. Physical*, vol. 265, pp. 152–160, 2017.

[42] A. Y. Celik, K. Kaya, and S. Mutlu, "Paper based integrated microfluidic system using electro-osmotic pumps with liquid bridges," in *IEEE MEMS*, Jan 2018, pp. 1225–1228.

[43] A. Manz, J. Fettinger, E. Verpoorte, H. Lüdi, H. Widmer, and D. Harrison, "Micromachining of monocrystalline silicon and glass for chemical analysis systems A look into next century's technology or just a fashionable craze?" *TrAC Trends in Analytical Chemistry*, vol. 10, no. 5, pp. 144 – 149, 1991.

[44] Y. Okamoto, K. Fujimoto, H. Ryoson, T. Ohba, and Y. Mita, "Stick-to-Analyze Zeta Potential Measurement Chip with Integrated Electroosmotic Micropump and Liquid Flow Sensor," in *IEEE MEMS*, 2019, pp. 437–440.

[45] K. Seibel, L. Schöler, H. Schäfer, and B. Markus, "A programmable planar electroosmotic micropump for lab-on-a-chip applications," *Journal of*

Micromechanics and Microengineering, vol. 18, p. 025008, 2008.

[46] A. Manz, D. J. Harrison, J. C. Fettinger, E. Verpoorte, H. Ludi, and H. M. Widmer, "Integrated electroosmotic pumps and flow manifolds for total chemical analysis systems," in *Transducers*, June 1991, pp. 939–941.

[47] P. F. Eng, P. Nithiarasu, and O. J. Guy, "An experimental study on an electro-osmotic flow-based silicon heat spreader," *Microfluidics and Nanofluidics*, vol. 9, no. 4-5, pp. 787–795, Mar 2010.

[48] D. J. Laser, A. M. Myers, S. Yao, K. F. Bell, K. E. Goodson, J. G. Santiago, and T. W. Kenny, "Silicon Electroosmotic Micropumps for Integrated Circuit Thermal Management," in *Transducers*, vol. 1, June 2003, pp. 151–154.

[49] A. Ajdari, "Steady flows in networks of microfluidic channels: building on the analogy with electrical circuits," *Comptes Rendus Physique*, vol. 5, no. 5, pp. 539 – 546, 2004.

[50] W. Morf, O. Guenat, and N. de Rooij, "Partial electroosmotic pumping in complex capillary systems: Part 1: Principles and general theoretical approach," *Sensors and Actuators B: Chemical*, vol. 72, no. 3, pp. 266 – 272, 2001.

[51] Y. Takamura, H. Onoda, H. Inokuchi, S. Adachi, A. Oki, and Y. Horiike, "Low-voltage electroosmosis pump for stand-alone microfluidics devices," *Electrophoresis*, vol. 24, no. 1 - 2, pp. 185–192, 2003.

[52] R. B. Schasfoort, S. Schlautmann, J. Hendrikse, and A. Van Den Berg, "Field-effect flow control for microfabricated fluidic networks," *Science*, vol. 286, no. 5441, pp. 942–945, 1999.

[53] S. Muthu, F. Svec, C. H. Mastrangelo, J. M. J. Frechet, and Y. B. Gianchandani, "Enhanced electro-osmotic pumping with liquid bridge and field effect flow

rectification," in *17th IEEE International Conference on Micro Electro Mechanical Systems. Maastricht MEMS 2004 Technical Digest*, Jan 2004, pp. 850–853.

[54] Y. Yang, E. Noviana, M. P. Nguyen, B. J. Geiss, D. S. Dandy, and C. S. Henry, "Paper-based microfluidic devices: Emerging themes and applications," *Analytical Chemistry*, vol. 89, no. 1, pp. 71–91, 2017.

[55] D. Liu, H. Zhang, F. Fontana, J. T. Hirvonen, and H. A. Santos, "Current developments and applications of microfluidic technology toward clinical translation of nanomedicines," *Advanced Drug Delivery Reviews*, vol. 128, pp. 54 – 83, 2018.

[56] C. M. B. Ho, S. H. Ng, K. H. H. Li, and Y.-J. Yoon, "3d printed microfluidics for biological applications," *Lab on a Chip*, vol. 15, pp. 3627–3637, 2015.

[57] V. van Duinen, S. J. Trietsch, J. Joore, P. Vulto, and T. Hankemeier, "Microfluidic 3d cell culture: from tools to tissue models," *Current Opinion in Biotechnology*, vol. 35, pp. 118 – 126, 2015.

[58] O. Tabata, H. Inagaki, and I. Igarashi, "Monolithic pressure-flow sensor," *IEEE Transactions on Electron Devices*, vol. 34, no. 12, pp. 2456–2462, Dec 1987.

[59] Y. Okamoto, H. Ryoson, K. Fujimoto, K. Honjo, T. Ohba, and Y. Mita, "Hotspot liquid microfluidic cooling: Comparing the efficiency between horizontal flow and vertical flow," *Journal of Physics: Conference Series*, vol. 773, p. 012066, nov 2016.

[60] J. Lee, H. Moon, J. Fowler, T. Schoellhammer, and C.-J. Kim, "Electrowetting and electrowetting-on-dielectric for microscale liquid handling," *Sensors and Actuators A: Physical*, vol. 95, no. 2, pp. 259 – 268, 2002.

[61] Y. Liao, H. Yao, A. Lingley, B. Parviz, and B. P. Otis, "A 3-μWCMOS Glucose Sensor for Wireless Contact-Lens Tear Glucose Monitoring," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 335–344, Jan 2012.

[62] L. Hartley, K. V. I. S. Kaler, and O. Yadid-Pecht, “Hybrid Integration of an Active Pixel Sensor and Microfluidics for Cytometry on a Chip,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 99–110, Jan 2007.

[63] D. Sato, T. Shindo, T. Mitsunaka, Y. Fujimoto, K. Iizuka, S. Tago, Y. Takayama, T. Fujii, and S. H. Kim, “Integrated Parallel Flow Cytometry Deice with Time Gated SPADS,” in *Transducers*, Jun 2019, pp. 17–20.

[64] B. Jang, P. Cao, A. Chevalier, A. Ellington, and A. Hassibi, “A CMOS fluorescent-based biosensor microarray,” in *ISSCC*, Feb 2009, pp. 436–437,437a.

[65] T. Matsuo and K. D. Wise, “An Integrated Field-Effect Electrode for Biopotential Recording,” *IEEE Transactions on Biomedical Engineering*, vol. BME-21, no. 6, pp. 485–487, Nov 1974.

[66] C. Yang and H. Søeberg, “Monolithic flow sensor for measuring millilitre per minute liquid flow,” *Sensors and Actuators A: Physical*, vol. 33, no. 3, pp. 143 – 153, 1992.

[67] P. R. Gascoyne, J. V. Vykoukal, J. A. Schwartz, T. J. Anderson, D. M. Vykoukal, K. W. Current, C. McConaghy, F. F. Becker, and C. Andrews, “Dielectrophoresis-based programmable fluidic processors,” *Lab on a Chip*, vol. 4, no. 4, pp. 299–309, 2004.

[68] N.-T. Nguyen, X. Huang, and T. K. Chuan, “MEMS-micropumps: a review,” *Journal of fluids Engineering*, vol. 124, no. 2, pp. 384–392, 2002.

[69] Y. Tarui, Y. Hayashi, and T. Sekigawa, “Dsa enhancement-depletion mos ic,” in *1970 International Electron Devices Meeting*. IEEE, 1970, pp. 110–110.

[70] J. F. Richard and Y. Savaria, “High voltage charge pump using standard CMOS technology,” in *NEWCAS*, June 2004, pp. 317–320.

[71] D. L. Sloan, G. H. Hall, C. J. Backhouse, and D. G. Elliott, “300 V integrated charge pump for lab on chip applications,” in *IEEE NANO*, Aug 2014, pp. 939–942.

[72] S. Morishita, M. Kubota, K. Asada, I. Mori, F. Marty, and Y. Mita, "A Bridge-Connected Isolated Silicon Islands Post-Processing Method for Fine-Grain-Integrated ± 10V-Operating CMOS-MEMS by Standard 5V CMOS Process Technology," in *MME*, Sep. 2009, pp. 48–51.

[73] K. A. Shaw, Z. Zhang, and N. C. MacDonald, "SCREAM I: A single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures," *Sensors and Actuators A: Physical*, vol. 40, no. 1, pp. 63–70, 1994.

[74] M. Gad-el Hak, *The MEMS handbook*. CRC Press, 2001.

[75] H. Guckel, J. Sniegowski, T. Christenson, S. Mohney, and T. Kelly, "Fabrication of micromechanical devices from polysilicon films with smooth surfaces," *Sensors and Actuators*, vol. 20, no. 1, pp. 117–122, 1989.

[76] G. T. Mulhern, D. S. Soane, and R. T. Howe, "Supercritical carbon dioxide drying of microstructures," in *Transducers*, 1993, pp. 7–10.

[77] Y. I. Lee, K. H. Park, J. Lee, C. S. Lee, H. J. Yoo, C. J. Kim, and Y. S. Yoon, "Dry release for surface micromachining with HF vapor-phase etching," *Journal of Microelectromechanical Systems*, vol. 6, no. 3, pp. 226–233, 1997.

[78] Y. Fukuta, H. Fujita, and H. Toshiyoshi, "Vapor hydrofluoric acid sacrificial release technique for micro electro mechanical systems using labware," *Japanese Journal of Applied Physics*, vol. 42, no. 6 A, pp. 3690–3694, 2003.

[79] P. F. V. Kessel, L. J. Hornbeck, R. E. Meier, and M. R. Douglass, "A MEMS-based projection display," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1687–1704, Aug 1998.

[80] J.-F. Gong, Z. Y. Xiao, and P. C. H. Chan, "Integration of an RF MEMS resonator with a bulk CMOS process using a low-temperature and dry-release fabrication

method," *Journal of Micromechanics and Microengineering*, vol. 17, no. 1, p. 20, 2007.

[81] A. Hirakawa, S. Morishita, I. Mori, M. Kubota, and Y. Mita, "Experimental evaluation of high voltage hold-off capability of post-process mesa-isolated series standard CMOS transistors," in *Transducers*, Jun 2013, pp. 2423–2426.

[82] H. V. Jansen, M. J. de Boer, S. Unnikrishnan, M. C. Louwerse, and M. C. Elwenspoek, "Black silicon method: X. A review on high speed and selective plasma etching of silicon with profile control: an in-depth comparison between Bosch and cryostat DRIE processes as a roadmap to next generation equipment," *Journal of Micromechanics and Microengineering*, vol. 19, no. 3, p. 033001, 2009.

[83] M. A. Gosalvez, Y. Zhou, Y. Zhang, G. Zhang, Y. Li, and Y. Xing, "Simulation of microloading and ARDE in DRIE," in *Transducers*, June 2015, pp. 1255–1258.

[84] B. Serneels, M. Steyaert, and W. Dehaene, "A 5.5 V SOPA line driver in a standard 1.2 V 0.13 µm CMOS technology," in *ESSCIRC*, Sep. 2005, pp. 303–306.

[85] S. Pashmineh and D. Killat, "Self-biasing high-voltage driver based on standard CMOS with an adapted level shifter for a wide range of supply voltages," in *NORCAS*, Oct. 2015, pp. 1–4.

[86] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and S. Martel, "Low-power static and dynamic high-voltage cmos level-shifter circuits," in *2008 IEEE International Symposium on Circuits and Systems*, May 2008, pp. 1946–1949.

[87] B. Serneels, T. Piessens, M. Stepert, and W. Dehaene, "A high-voltage output driver in a standard 2.5 v 0.25 /spl mu/m cmos technology," in *2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No.04CH37519)*, Feb 2004, pp. 146–518

Vol.1.

[88] C.-Y. Lin and Y.-L. Chiu, “Design of embedded scr device to improve esd robustness of stacked-device output driver in low-voltage cmos technology,” *Solid-State Electronics*, vol. 124, pp. 28 – 34, 2016.

[89] Y. Okamoto, I. Mori, and Y. Mita, “Demonstration of 0–30V comb-drive MEMS actuator by integrated switching circuit with post-mesa-isolated standard 5V CMOS transistors,” in *DTIP*, May 2016, pp. 317–320.

[90] Y. Li, W. Parkes, L. Haworth, A. Stokes, K. Muir, P. Li, A. Collin, N. Hutcheon, R. Henderson, B. Rae, and A. Walton, “Anodic Ta_2O_5 for CMOS compatible low voltage electrowetting-on-dielectric device fabrication,” *Solid-State Electronics*, vol. 52, no. 9, pp. 1382–1387, Sep. 2008.

[91] M. D. Ker and S. L. Chen, “Ultra-High-Voltage Charge Pump Circuit in Low-Voltage Bulk CMOS Processes with Polysilicon Diodes,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 1, pp. 47–51, Jan 2007.

[92] M. Takayasu, A. Shirane, S. Lee, D. Yamane, H. Ito, X. Mi, H. Inoue, F. Nakazawa, S. Ueda, N. Ishihara, and K. Masu, “An 8 channel, 20 V output CMOS switching driver with 3.3 V power supply using triple-well biasing techniques for integrated MEMS device control,” *Japanese Journal of Applied Physics*, vol. 53, no. 4S, pp. 04EE131–04EE138, Mar 2014.

[93] M. R. Hoque, T. McNutt, J. Zhang, A. Mantooth, and M. Mojarradi, “A high voltage Dickson charge pump in SOI CMOS,” in *CICC*, Sep 2003, pp. 493–496.

[94] Y. Mita, E. Lebrasseur, Y. Okamoto, F. Marty, R. Setoguchi, K. Yamada, I. Mori, S. Morishita, Y. Imai, K. Hosaka, A. Hirakawa, S. Inoue, M. Kubota, and M. Denoual, “Opportunities of CMOS-MEMS integration through LSI foundry and open facility,”

Japanese Journal of Applied Physics, vol. 56, no. 6S1, p. 06GA03, May 2017.

[95] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun 1976.

[96] Y. Okamoto and Y. Mita, "Integrated 0–30 v switching driver circuit fabricated by mesa isolation postprocess of standard 5 v cmos lsi for mems actuator applications," *Microsystem Technologies*, vol. 24, no. 1, pp. 503–510, Jan 2018.

[97] Y. Okamoto, H. Takehara, K. Fujimoto, T. Ichiki, T. Ohba, and Y. Mita, "On-Chip High-Voltage Charge Pump With MEMS Post-Processed Standard 5-V CMOS on SOI for Electroosmotic Flow Micropumps," *IEEE Electron Device Letters*, vol. 39, no. 6, pp. 851–854, June 2018.

[98] T. Akagi, K. Kato, N. Hanamura, M. Kobayashi, and T. Ichiki, "Evaluation of desialylation effect on zeta potential of extracellular vesicles secreted from human prostate cancer cells by on-chip microcapillary electrophoresis," *Japanese Journal of Applied Physics*, vol. 53, no. 6S, p. 06JL01, may 2014.

[99] C. Werner, U. König, A. Augsburg, C. Arnhold, H. Körber, R. Zimmermann, and H.-J. Jacobasch, "Electrokinetic surface characterization of biomedical polymers— a survey," *Colloids and Surfaces A: Physicochemical and Engineering Aspects*, vol. 159, no. 2-3, pp. 519–529, 1999.

[100] A. Sze, D. Erickson, L. Ren, and D. Li, "Zeta-potential measurement using the smoluchowski equation and the slope of the curren-time relationship in electroosmotic flow," *Journal of Colloid and Interface Science*, vol. 261, no. 2, pp. 402 – 410, 2003.

[101] S. Arulanandam and D. Li, "Determining ζ potential and surface conductance by

monitoring the current in electro-osmotic flow," *Journal of Colloid and Interface Science*, vol. 225, no. 2, pp. 421 – 428, 2000.

[102] Y. Song, K. Zhao, M. Li, X. Pan, and D. Li, "A novel method for measuring zeta potentials of solid-iquid interfaces," *Analytica Chimica Acta*, vol. 853, pp. 689 – 695, 2015.

[103] D. Ross, T. J. Johnson, and L. E. Locascio, "Imaging of electroosmotic flow in plastic microchannels," *Analytical chemistry*, vol. 73, no. 11, pp. 2509–2515, 2001.

[104] M. Dijkstra, M. de Boer, J. Berenschot, T. Lammerink, R. Wiegerink, and M. Elwenspoek, "Miniaturized thermal flow sensor with planar-integrated sensor structures on semicircular surface channels," *Sensors and Actuators A: Physical*, vol. 143, no. 1, pp. 1 – 6, 2008.

[105] S. Dalola, S. Cerimovic, F. Kohl, R. Beigelbeck, J. Schalko, V. Ferrari, D. Marioli, F. Keplinger, and T. Sauter, "Mems thermal flow sensor with smart electronic interface circuit," *IEEE Sensors Journal*, vol. 12, no. 12, pp. 3318–3328, 2012.

[106] "16.unified: Thermodynamics and propulsion," https://web.mit.edu/16.unified/www/FALL/thermodynamics/notes/.

[107] S. T. S. Holmström, U. Baran, and H. Urey, "Mems laser scanners: A review," *Journal of Microelectromechanical Systems*, vol. 23, no. 2, pp. 259–275, April 2014.

[108] F. Senger, T. von Wantoch, C. Mallas, J. Janes, U. Hofmann, B. Wagner, and W. Benecke, "Mems scanning mirrors for high power laser display and lighting applications," in *The 4th Laser Display and Lighting Conference (LDC' 15), Yokohama, Japan, Apr*, 2015.

[109] H. Honma, H. Mitsuya, G. Hashiguchi, H. Fujita, and H. Toshiyoshi, "A three-ports structure for electrostatic energy-harvester to lower constraint force and to enhance

fast storage," in *2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, June 2017, pp. 2167–2170.

[110] A. Wolter, S.-T. Hsu, H. Schenk, and H. K. Lakner, "Applications and requirements for mems scanner mirrors," in *MOEMS and Miniaturized Systems V*, vol. 5719. International Society for Optics and Photonics, 2005, pp. 64–75.

[111] H. Urey, D. W. Wine, and T. D. Osborn, "Optical performance requirements for mems-scanner-based microdisplays," in *MOEMS and Miniaturized Systems*, vol. 4178. International Society for Optics and Photonics, 2000, pp. 176–185.

[112] U. Hofmann, M. Aikio, J. Janes, F. Senger, V. Stenchly, J. Hagge, H.-J. Quenzer, M. Weiss, T. von Wantoch, C. Mallas *et al.*, "Resonant biaxial 7-mm mems mirror for omnidirectional scanning," *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 13, no. 1, p. 011103, 2013.

[113] U. Baran, D. Brown, S. Holmstrom, D. Balma, W. O. Davis, P. Muralt, and H. Urey, "Resonant pzt mems scanner for high-resolution displays," *Journal of microelectromechanical systems*, vol. 21, no. 6, pp. 1303–1310, 2012.

[114] A. Arslan, D. Brown, W. O. Davis, S. Holmstrom, S. K. Gokce, and H. Urey, "Comb-actuated resonant torsional microscanner with mechanical amplification," *Journal of Microelectromechanical Systems*, vol. 19, no. 4, pp. 936–943, 2010.

[115] H. Jansen, M. de Boer, R. Wiegerink, N. Tas, E. Smulders, C. Neagu, and M. Elwenspoek, "Rie lag in high aspect ratio trench etching of silicon," *Microelectronic Engineering*, vol. 35, no. 1, pp. 45–50, 1997.

[116] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *Journal of Applied Physics*, vol. 108, no. 5, p. 051101, 2010.

[117] B. E. Volland and I. W. Rangelow, "The influence of reactant transport on the

profiles of gas chopping etching processes: a simulation approach," *Microelectronic engineering*, vol. 67, pp. 338–348, 2003.

[118] C. Mogab, "The loading effect in plasma etching," *Journal of the Electrochemical Society*, vol. 124, no. 8, pp. 1262–1268, 1977.

[119] S. Lai, D. Johnson, and R. Westerman, "Aspect ratio dependent etching lag reduction in deep silicon etch processes," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 24, no. 4, pp. 1283–1288, 2006.

[120] R. L. Bates, M. J. Goeckner, and L. J. Overzet, "Correction of aspect ratio dependent etch disparities," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 32, no. 5, p. 051302, 2014.

[121] J. Kiihamäki, H. Kattelus, J. Karttunen, and S. Franssila, "Depth and profile control in plasma etched mems structures," *Sensors and Actuators A: Physical*, vol. 82, no. 1-3, pp. 234–238, 2000.

[122] S. Hsu, T. Klose, C. Drabe, and H. Schenk, "Fabrication and characterization of a dynamically flat high resolution micro-scanner," *Journal of Optics A: Pure and Applied Optics*, vol. 10, no. 4, p. 044005, 2008.

[123] P. Docker, P. Kinnell, and M. Ward, "Development of the one-step drie dry process for unconstrained fabrication of released mems devices," *Journal of Micromechanics and Microengineering*, vol. 14, no. 7, p. 941, 2004.

[124] B. Chui, T. Sun, R. Lim, M. Olivo, W. Sun *et al.*, "Simplified monolithic process for fabricating low-cost, high-frequency, high-flatness scanning micromirrors," in *2013 Transducers & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*. IEEE, 2013, pp. 1036–1039.

[125] S. Jensen, J. M. Jensen, U. J. Quaade, and O. Hansen, "Uniformity-improving dummy structures for deep reactive ion etching (drie) processes," in *Micromachining and Microfabrication Process Technology X*, vol. 5715. International Society for Optics and Photonics, 2005, pp. 39–46.

[126] F. Lärmer and A. Urban, "Challenges, developments and applications of silicon deep reactive ion etching," *Microelectronic Engineering*, vol. 67, pp. 349–355, 2003.

[127] Y. Mita, M. Kubota, T. Harada, F. Marty, B. Saadany, T. Bourouina, and T. Shibata, "Contour lithography methods for drie fabrication of nanometre–millimetre-scale coexisting microsystems," *Journal of Micromechanics and Microengineering*, vol. 16, no. 6, p. S135, 2006.

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List of Publications

Journal Papers

[1] Isao Mori, **Yuki Okamoto**, Yoshio mita, "A scalable, optically-driven, high-voltage switch for remote MEMS device operation fabricated with a standard CMOS process," *IEICE Electronics Express* , Vol.14, no.3, p.20171174, 2017.

[2] Yoshio Mita, Eric Lebrasseur, **Yuki Okamoto**, Frédéric Marty, Ryota Setoguchi, Kentaro Yamada, Isao Mori, Satoshi Morishita, Yoshiaki Imai, Kota Hosaka, Atsushi Hirakawa, Shu Inoue, Masanori Kubota and Matthieu Denoual, "Opportunities of CMOS-MEMS integration through LSI foundry and open facility," *Japanese Journal of Applied Physics* , Vol. 56, No. 6S1, p. 06GA03, 2017.

[3] **Yuki Okamoto**, Eric Lebrasseur, Isao Mori, Frédéric Marty, Yoshio Mita, "Test Structures for End-Point Visualization of All-Plasma Dry Release of Deep-RIE MEMS Devices and Application to Release Process Modal Analysis," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 30, Issue: 3, pp.201-208, 2017.

[4] **Yuki Okamoto**, Yoshio Mita, "Integrated 0–30 V switching driver circuit fabricated by mesa isolation postprocess of standard 5 V CMOS LSI for MEMS actuator applications," *Microsystem Technologies*, Vol 24, No. 1, pp.503-510, 2018.

[5] **Yuki Okamoto**, Yukiya Tohyama, Shunsuke Inagaki, Mikio Takiguchi, Tomoki Ono, Eric Lebrasseur, and Yoshio Mita, "High-uniformity centimeter-wide Si etching method for MEMS devices with large opening elements," *Japanese Journal of Applied Physics*, Vol. 57, No. 4S, p.04FC03, 2018.

[6] Yoshio Mita, Atsushi Hirakawa, Bruno Stefanelli, Isao Mori, **Yuki Okamoto**, Satoshi Morishita, Masanori Kubota, Eric Lebrasseur, Andreas Kaiser, "Progress and opportunities in high-voltage microactuator powering technology towards one-chip MEMS," *Japanese Journal of Applied Physics*, 2018.

[7] **Yuki Okamoto**, Hiroaki Takehara, Koji Fujimoto, Takanori Ichiki, Takayuki Ohba, and Yoshio Mita, "On-Chip High-Voltage Charge Pump with MEMS Post-Processed Standard 5-V CMOS on SOI for Electroosmotic Flow Micropumps," *IEEE Electron Device Letters*, Vol. 39, Issue 6, pp. 851-854, 2018 (2018.04).

[8] **Yuki Okamoto**, Yoshio Mita, "A Review on Increasing of Breakdown Voltage of Standard CMOS LSI Circuits by MEMS Post-Process," *IEEJ Transactions on Sensors and Micromachines*, 2018.

[9] **Yuki Okamoto**, Hiroyuki Ryoson, Koji Fujimoto, Takayuki Ohba, Yoshio Mita, "On-Chip CMOS-MEMS Based Electroosmotic Flow Micropump Integrated with High-Voltage Generator," *Journal of Microelectromechanical Systems*, 2019.

International Conferences

[10] **Yuki Okamoto**, Isao Mori, Kentaro Kawahara, Eric Lebrasseur and Yoshio Mita, "Solar-Powered ElectroWetting for Silicon Pondskater," *Microswimmers 2015* , Bordeaux, France, 2015.

[11] **Yuki Okamoto**, Eric Lebrasseur, Isao Mori and Yoshio Mita, "An End-point Visualization Test Structure for All Plasma Dry Release of Deep-RIE MEMS,"*IEEE*

Conference on Microelectronic Test Structures (ICMTS) , Yokohama, Japan, 2016.

[12] **Yuki Okamoto**, Isao Mori and Yoshio Mita, "Demonstration of 0-30V Comb-Drive MEMS Actuator by integrated switching circuit with post-mesa-isolated standard 5V CMOS transistor," *2016 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)*, Budapest, Hungary, 2016.

[13] **Yuki Okamoto**, Hiroyuki Ryoson, Koji Fujimoto, Keiji Honjo, Takayuki Ohba and Yoshio Mita, "Hotspot Liquid Microfluidic Cooling: Comparing The Efficiency between Horizontal Flow and Vertical Flow,"*PowerMEMS*, Paris, France, 2016.

[14] **Yuki Okamoto**, Yoshio Mita, "Wireless operation of EWOD by the on-chip CMOS silicon photovoltaic cell array,"*International Conference on Solid State Devices and Materials (SSDM)*, Sendai, Japan, 2017.

[15] **Yuki Okamoto**, Yukiya Tohyama, Naoto Usami Yoshio Mita, "The large-area backside etching method by changing backside layout using loading effect and ARDE for foundry-based fabrication,"*International Conference on Solid State Devices and Materials (SSDM)*, Sendai, Japan, 2017.

[16] **Yuki Okamoto**, Koji Fujimoto, Hiroyuki Ryoson, Takayuki Ohba, Yoshio Mita, "Stick-to-Analyze Zeta Potential Measurement Chip with Integrated Electroosmotic Micropump and Liquid Flow Sensor," *The 32th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2019)*, Seoul, Korea, 2019.

[17] **Yuki Okamoto**, Ayako Mizushima, Naoto Usami, Jun Kinoshita, Akio Higo, Yoshio Mita, "Damage Assessment Structure of Test-Pad Post-Processing on CMOS LSIs," *IEEE Conference on Microelectronic Test Structures (ICMTS 2019)* , Kita-Kyushu, Japan, 2019.

[18] **Yuki Okamoto**, Taku Tsuchiya, Charles Moslonka, Yu-Sheng Lin, Sung Tsang,

Frédéric Marty, Ayako Mizushima, Chen-li Sun, Hsiang-Yu Wang, Agnés Tixier-Mita, Olivier Français, Bruno Le Pioufle, and Yoshio Mita, "Z-Axis Controllable Mille-Feuille Electrode Electrorotation Device Utilizing Levitation Effect,"*The 20th International Conference on Solid State Sensors and Actuators (Transducers 2019 - EUROSENSORS XXXIII)*, Berlin, Germany,2019.

Journal Papers (Unrelated)

[19] Daigo Terutsuki, Hiefumi Mitsuno, Takeshi Sakurai, **Yuki Okamoto**, Agnés Tixier-Mita, Hiroshi Toshiyoshi, Yoshio Mita, Ryohei Kanzaki, "Increasing cell-device adherence using cultured insect cells for receptor-based biosensors,"*Royal Society Open Science*, Vol. 5, No. 3, March, 2018.

[20] Mathieu Pouliquen, Matthieu Denoual, Corentin Jorel, Constantin Radu, Didier Robbes, J Grand, H Awala, S Mintova, M Harnois, O de Sagazan, S Inoue, Eric Lebrasseur, Kentaro Yamada, **Yuki Okamoto**, Agnés Mita-Tixier, and Yoshio Mita, "Self-identification algorithm for zeolite-based thermal capacity gas sensor," *Microsystem Technologies*, 2018.

[21] Akio Higo, Yoshio Mita, Haibin Wang, Takaya Kubo, Hiroshi Segawa, Naoto Usami, **Yuki Okamoto**, Kentaro Yamada, Yudai Takeshiro, and Masakazu Sugiyama, "Fabrication of PbS QD/Silicon Hybrid Infrared Photodiode for LSI Platform," *IEEJ Transactions on Sensors and Micromachines*, 2018.

[22] Kentaro Yamada, Julien Grand, **Yuki Okamoto**, Rangareddygari Ranga Reddy, Matthieu Denoual, Svetlana Mintova, Agnés Tixer-Mita and Yoshio Mita, "Impact Test for Gas Sensing Using Large Particle Size Zeolite," *IEEJ Transactions on Sensors and Micromachines*, vol. 138, no. 9, 2018.

[23] Ranga Reddy, Keisuke Komeda, **Yuki Okamoto**, Eric Lebrasseur, Akio Higo,

Yoshio Mita, “A zero-power sensing MEMS shock sensor with a latch-reset mechanism for multi-threshold events monitoring,” *Sensors and Actuators A: Physical*, 2019

International Conferences (Unrelated)

[24] Toru Nakura, **Yuki Okamoto**, Yoshio Mita, and Kunihiro Asada, “One week TAT of 0.8μm CMOS gate array with analog elements for educational exercise,”*EWME* Southampton, UK, 2016

[25] Daigo Terutsuki, Hidefumi Mitsuno, **Yuki Okamoto**, Takeshi Sakurai, Agnés Tixier-Mita, Hiroshi Toshiyoshi, Yoshio Mita and Ryohei Kanzaki, “Odor sensitive Field Effect Transistor (OSFET) Based on Insect Cells Expressing Insect Odrant Receptor,”*MEMS 2017*, 2017.

[26] Stewart Smith, Yudai Takeshiro, **Yuki Okamoto**, Jonathan G. Terry, Anthony J. Walton, Rimon Ikeno,Kunihiro Asada and Yoshio Mita, “Test Sructures for Nano-Gap Fabrication Proctromechanical Systems,” *ICMTS 2017*, Grenoble, 2017.

[27] Naoto Usami, Jun Kinoshita, Rimon Ikeno, **Yuki Okamoto**, Masaaki Tanno, Kunihiro Asada and Yoshio Mita, ”An arrayed test structure for transistor damage assessment induced by circuit analysis and repairing processes with back-side-accessing Focused Ion Beam“, *ICMTS 2017*, Grenoble, France, 2017.

[28] Kohei Shimamura, Kosumo Matsui, Waku Hatakeyama, Kohei Fujiwara, Hidehiko Yamaoka, **Yuki Okamoto**, Masatoshi Suzuki, Ayako Mizushima, Shunsuke Minakawa, Kimiya Komurasaki, “Microstrip antenna and rectifier for wireless power transfar at 94GHz,” *WPTC*, Taiwan, 2017.

[29] Matthieu Denoual, Mathieu Pouliquen, Corentin Jorel, Constantin Radu, Didier Robbes, M Harnois, O de Sagazan, J Grand, H Awala, S Mintova, S Inoue, Eric

Lebrasseur, Kenshiro Yamada, **Yuki Okamoto**, Agnés Mita-Tixier, and Yoshio Mita, "Zeolite-based thermal mass gas sensor with self-identification algorithm," DTIP 2017, Bordeaux, France, 2017.

[30] Akio Higo, Hai-bin Wang, Takaya Kubo, Naoto Usami, **Yuki Okamoto**, Kentaro Yamada, Hiroshi Segawa, Masakazu Sugiyama, and Yoshio Mita, "Fabrication of PbS Quantum dots and Silicon Device for Near-Infrared Detection," *OMN*, New Mexico, USA, 2017.

[31] Yudai Takeshiro, **Yuki Okamoto**, Yoshio Mita, "Mask-programmable on-chip photovoltaic cell array (Late News)," PowerMEMS , Kanazawa, Japan (2017.11)

[32] Naoto Usami, Akio Higo, Ayako Mizushima, **Yuki Okamoto** and Yoshio Mita, "Test Structure for Electrical Assessment of UV Laser Direct Fine Patterned Material," *ICMTS 2018*, Austin, USA, 2018.

[33] R Ranga Reddy, **Yuki Okamoto**, Yoshio Mita, "An On-chip Test Structure for Studying the Frictional Behavior of Deep-RIE MEMS Sidewall Surfaces," *ICMTS 2018*, Austin, USA, 2018

[34] Ken Saito, Daniel S. Contreras, Yudai Takeshiro, **Yuki Okamoto**, Yuya Nakata, Taisuke Tanaka, Satoshi, Satoshi Kawamura, Minami Kaneko, Fumio Uchikoba, Yoshio Mita, and Kristofer S. J. Pister, "Study on silicon device of microrobot system for heterogeneous integration," *ICEP-IAAC*, Mie, Japan, 2018.

[35] Taisei Kuriyama, Akiyoshi Suzuki, **Yuki Okamoto**, Yoshio Mita, "A Micromachined All-Solid On-Chip Thin-Film Battery towards Uninterruptible Photovoltaic Cells,"*DTIP 2018*, Roma, Italy, 2018.

[36] Daigo Terutsuki, Hidefumi Mitsuno, Takeshi Sakurai, **Yuki Okamoto**, Agnés Tixier-Mita, Hiroshi Toshiyoshi, Yoshio Mita, and Ryohei Kanzaki, "Cell-sensor

interface analysis of a bio-hybrid electric odorant sensor," *BIOSENSORS 2018*, Miami, Florida, USA 2018.

[37] Makoto Ogasawara, Yuji Kosugi, Jiaqi Zhang, **Yuki Okamoto**, Yoshio Mita, Akira Otomo, Yoshiaki Nakano, Takuo Tanemura, "Electro-optic polymer surface-normal modulator using silicon high-contrast grating resonator," *CLEO*, San Jose, California, USA, 2019.

[38] Shunsuke Inagaki, **Yuki Okamoto**, Akio Higo, Yoshio Mita, "High-Resolution Piezoelectric MEMS Scanner Fully Integrated with Focus-Tuning And Driving Actuators," *Transducers 2019*, Berlin, Germany, 2019.