論 文 の 内 容 の 要 旨

論文題目 Automatic Test Pattern Generation Methods for Multiple Stuck-at Faults
（多重縮退故障のためのテストパタン生成手法）

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As the number of transistors in the fabricated circuits becomes extremely larger, it is unavoidable for faults to happen in the fabricated chips. Therefore, we need to use test patterns to thoroughly test and determine whether the functionalities of the fabricated chips are correct or not before shipping to consumers. There are commonly used fault models to efficiently represent the faults and generate the test patterns, such as stuck-at fault, delay fault, bridge fault and others. Automatic Test Pattern Generation technology has been developed to prepare as small as possible set of test patterns which cover almost all the faults in a chip. In this thesis, we mainly discuss stuck-at fault and its corresponding test generation technologies.

In fact, not only the single stuck-at faults, but also the multiple stuck-at faults are likely to happen in the circuits, especially for the large scale circuit. Multiple faults are difficult to be fully covered due to the exponentially enormous number of all possible faults. To be specific, if there are m possible faulty locations in the circuit, the combinations of multiple faults are in total 3^m-1, which are practically impossible to be detected one by one, when m is large. It is even not at all easy to simply list up all of such fault combinations. Although there are methods proposed to deal with the multiple faults, they fail to generate compact test patterns to detect all faults within an acceptable running time.

Nevertheless, there are exponentially more multiple faults than single faults in any given circuit design, only a few additional test patterns are needed to cover all of the multiple faults, if the test generation starts from the complete test set for single faults. In this thesis, we first show the case where test patterns for single faults are sufficient to cover all multiple faults, and then explain in which conditions some of the multiple faults may be overlooked. Based on this analysis, we propose a method which can efficiently generate the complete test set for double faults without traversing all the faults. Since most of the double faults can be detected by single faults' test set, the proposed method only selects the uncovered double faults by analyzing the propagation paths of single faults and then generating new

test patterns only for those uncovered faults. The experimental results show that based on the single faults' test set, the proposed method only needs to create a small number of additional test patterns to cover all double faults in most of the given circuits.

Based on the method for double faults, we proposes an incremental Automatic Test Pattern Generation method to deal with multiple stuck-at faults. Instead of traversing the entire n multiple faults list, the proposed method only selects the fault undetected by the existing test patterns for n-1 faults, and then generates additional test patterns. Staring from a complete test set for single faults, the proposed method can be incrementally applied to handle all multiple faults. Moreover, since the number of the undetected faults that are selected is extremely smaller comparing to the total number of the entire fault list, the proposed method can generate compact test patterns to cover all faults within an acceptable running time.

As the proposed incremental Automatic Test Pattern Generation method can be used to find redundant multiple faults, we proposes a logic optimization method to remove the redundancy in the circuit. In order to remove as many as possible the redundancy, instead of removing the redundant single faults first, we clear up the redundant faults from higher cardinality to lower cardinality. The experiments prove that the proposed method can successfully eliminate more redundancy comparing to the redundancy removal command in the synthesis tool SIS.