博士論文

Field-effect transistors and photodetectors based on bilayer graphene in all-two-dimensional layered heterostructures

(完全 **2** 次元層状ヘテロ構造における **2** 層グラフェン電界効果型トランジスタ及び光検出器に関する研究**)**

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Chapter 1 Introduction

1.1 Graphene as a semiconductor material

Semiconductors play a crucial role in many components in modern electronic appliances nowadays. Many of their applications utilize carrier generation by electrostatic gating or by optical excitation. Important factors that determine their suitable applications are band gap size and carrier mobility. The inverse proportional relationship of band gap and carrier mobility is known from Kane model. In Kane model, the band structure of a semiconductor can be written by k・p theory as

$$E_{\pm k} = \frac{\bar{h}^2 k^2}{2m} \pm \sqrt{\left(\frac{E_g}{2}\right)^2 + \left(\frac{\bar{h}}{m} k \cdot P\right)^2}.$$

Here E_g is the band gap size, ± denotes the conduction band and valence band, and m is free electron mass. In order to consider Fermi energy in valence band, P is substitute as $P = mv$, where v is Fermi velocity. The equation can be written as

$$E_f = \frac{\bar{h}^2 k^2}{2m} + \sqrt{\left(\frac{E_g}{2}\right)^2 + \left(\bar{h} v k\right)^2}.$$

Effective mass can be derived from the equation of dispersion relation.

$$m^* = \bar{h}^2 \left(\frac{d^2 E_f}{dk^2}\right)^{-1} = \left(\frac{1}{m} + \frac{\left(\frac{E_g v}{2}\right)^2}{\left[\left(\frac{E_g}{2}\right)^2 + \left(\bar{h} v k\right)^2\right]^{3/2}} \right)^{-1}$$

By taking $k = 0$

$$m^* = \left(\frac{1}{m} + \frac{2v^2}{E_g}\right)^{-1}$$

is obtained. Carrier mobility is

$$\mu \equiv \frac{q\tau}{m^*} = q\tau \left(\frac{1}{m} + \frac{2v^2}{E_g}\right).$$

One can see that the carrier mobility of a semiconductor is inversely proportional to the size of band gap. The reported carrier mobility and band gap of various semiconductors are plotted in **Fig. 1.1**. Suitable applications for each semiconductors depend on their carrier mobility and band gap size. Wide gap semiconductors are mostly used in devices. Semiconductors with band gap around 1 eV such as Si are commonly used in MOSFET (Metal Oxide Semiconductor-Field Effect Transistor). Due to their increased carrier mobility, small gap semiconductors are used in magnetic field sensors. Graphene, as the ultimate limit of Kane model, has zero band gap but highest room temperature mobility. In FET application, faster operation can be achieved by using

channel with higher mobility. From this perspective, graphene is an attractive candidate for FET application. However, graphene has zero band gap, making FET not able to turn off. In bilayer graphene, band gap up to 0.3 eV can be created by applying electric field perpendicularly to the graphene layers, showing a possibility of FET application. Also, this band gap energy range corresponds to that of far infrared, suggesting additional possibility for infrared detection application.

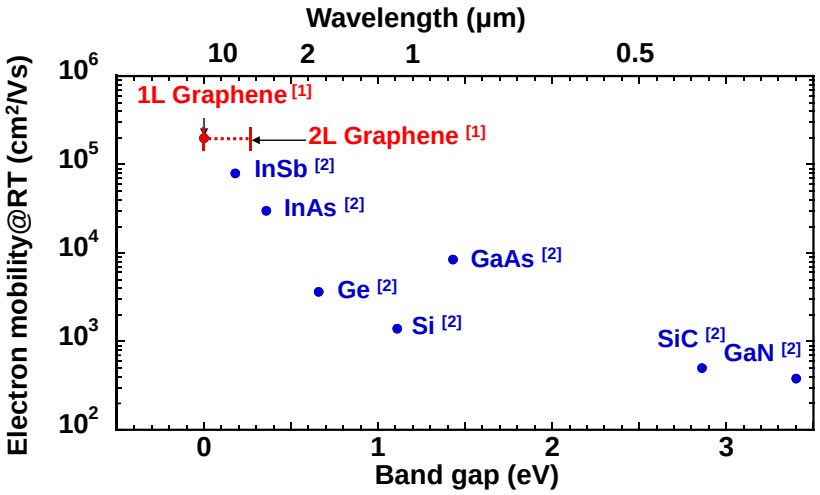


Figure 1.1 Room temperature electron mobility and band gap of semiconductors.

1.2 MOSFET

Increase in integration degree of FETs is one of the primary driving forces in information and communication industries. In order to increase the integration degree, FETs are "scaled" down by reducing the dimensions of FETs to increase the number of FETs that can be fabricated in the same chip area, and improve the performance. The trend of number of transistors in one chip was forecast by Gordon Moore in 1965 that the number of transistors will double about every two year. The prediction proved accuracy for several decades and has been used as targets for research and development in semiconductor industries (**Fig. 1.2**). In 1974, a systematic study about scaling of FET was proposed by Dennard et al.. Consider a simple example about transconductance (g_m) which indicates the ability to modulate the current in the channel, and channel conductance are given by

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D} = \frac{\mu \varepsilon_{ox} W}{Ld}(V_G - V_T)$$

$$g_D = \left(\frac{\partial I_D}{\partial V_D}\right)_{V_G} = \frac{\mu \varepsilon_{ox} W}{Ld} V_D$$

where I_D is drain current, V_G, V_D, V_T are gate, drain and threshold voltage, μ is channel mobility, ε_{ox}, d are gate insulator dielectric constant and thickness, L, W are channel

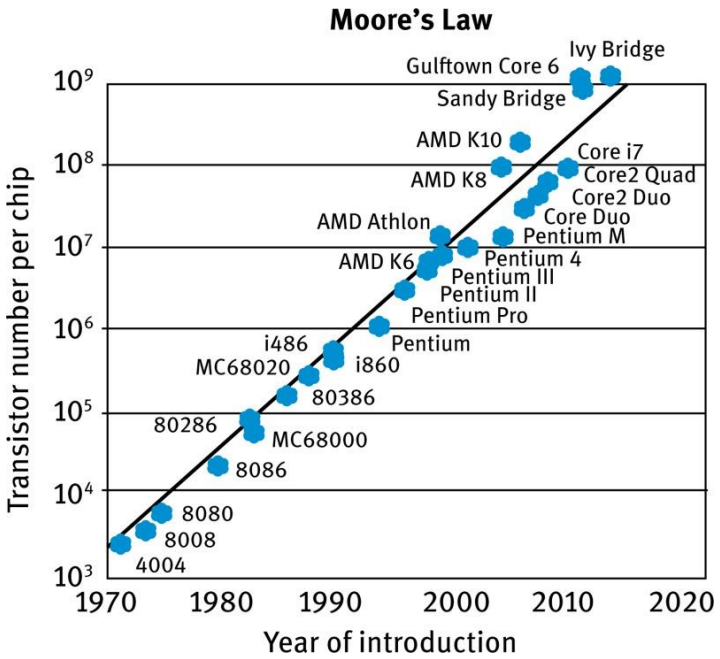


Figure 1.2 Number of transistors in CPU. [3]

length and width respectively. If W, L, d are scaled by 1/k (k>1) g_m and g_D will increase. Other figures of merit can be improved by scaling other device parameters. The improvements by scaling are summarized in **Table. 1.1**.

Table 1.1 Constant electric field scaling of device parameters. [2]

Parameters	Scaling factor
Device dimensions	1/k
Doping concentration	k
Voltage	1/k
Delay time	1/k
Power consumption	$1/k^2$
Integration degree	$1/k^2$
Power density	1

However, the scaling has limits. When the gate insulator becomes too thin, leakage current becomes large, and when the channel length becomes too short, the potential from gate is strongly affected by drain voltage (**Fig. 1.3**), which is called "short channel effect". In order to prevent gate leakage while keeping the same gate capacitance,

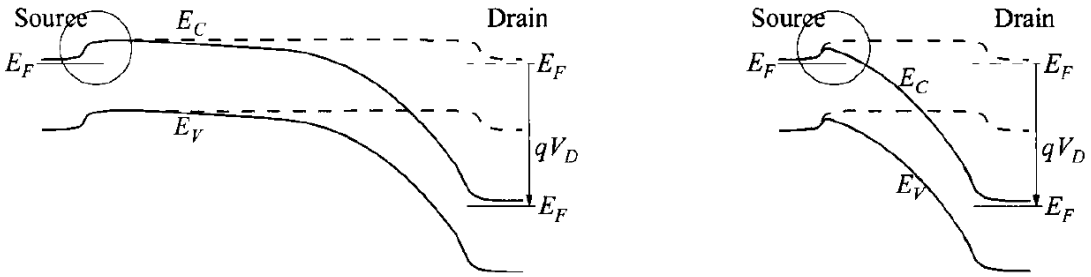


Figure 1.3 Short channel effect. [2]

high-k gate stack have been used. To avoid short channel effect, the channel length has to be at least six times longer than the natural length of the channel, given by [4]

$$\lambda = \sqrt{\frac{1}{N}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{ch} t_{ox}}.$$

where N is the number of gate, ε_{ch}, t_{ch} are the dielectric constant ant the thickness of channel, respectively. Short channel effect in Si MOSFET has been suppressed by increasing N. However, the dielectric constant of Si is 11.9 and mobility in thin channel suffers greatly from roughness, limiting the scaling. On the other hand, graphene is stable even in monolayer form and its dielectric constant is about 4 [5], suggesting the possibility for further scaling than Si.

Transition metal dichalcogenides (TMDC) have sufficient band gap for FET application, but their mobility is only a few thousand cm^2/Vs because the conduction band is from d orbital. On the other hand, the conduction band of graphene is from p_z orbital, making its mobility the highest among two-dimensional layered materials. Using such high mobility, it is predicted that graphene FET can have faster switching time than other two-dimensional layered materials (**Fig. 1.4**), making it suitable for high-performance FET. In this study, high performance application of bilayer graphene will be focused.

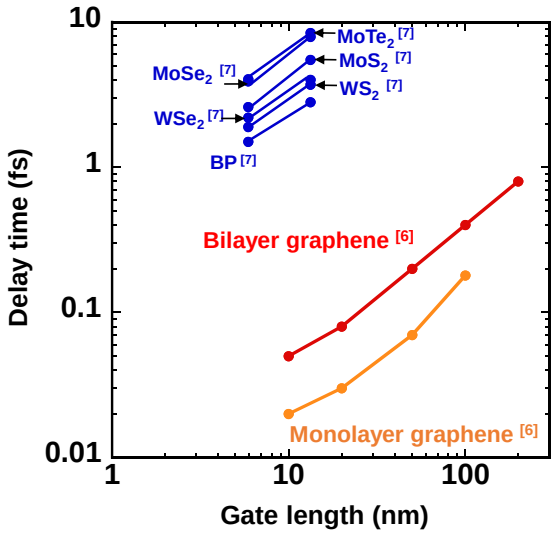


Figure 1.4 Delay in switching time and gate length.

1.3 Infrared detectors

Self-driving technology requires infrared detectors that have fast response and can operate at room temperature to detect humans and obstacles. The wavelength range used is 8 μm～13 μm due to high atmospheric transmittance (**Fig 1.5**). Detectivity (D*) of various infrared detectors are shown in **Fig 1.6**. D* can be taken as normalized signal noise ratio (S/N ratio) per unit area per 1 W of incident light, given by

$$D^* = \frac{S/N \cdot \Delta f^{1/2}}{P \cdot A^{1/2}}$$

where Δf is noise bandwidth, P is incident energy, A is detector area, respectively. Quantum detectors detect signal by optical excitation of carriers across the band gap, therefore have high responsivity and fast response speed. However, for long wave range

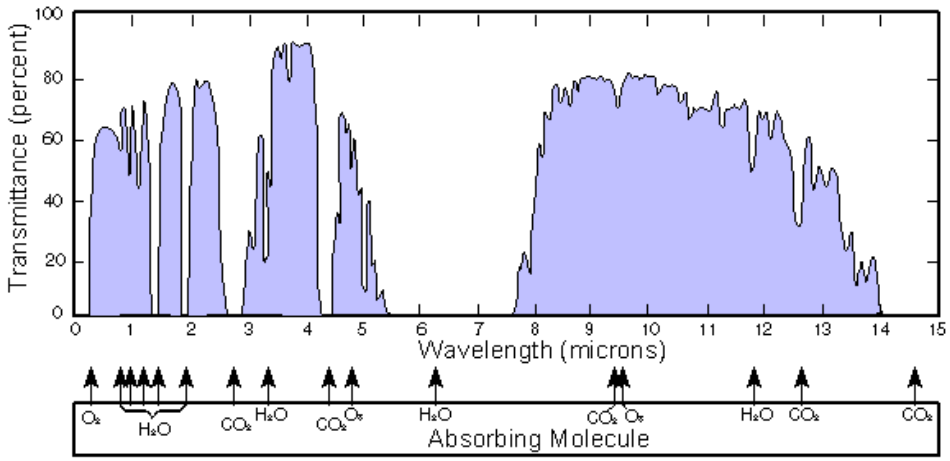


Figure 1.5 Infrared transmittance in atmosphere. [7]

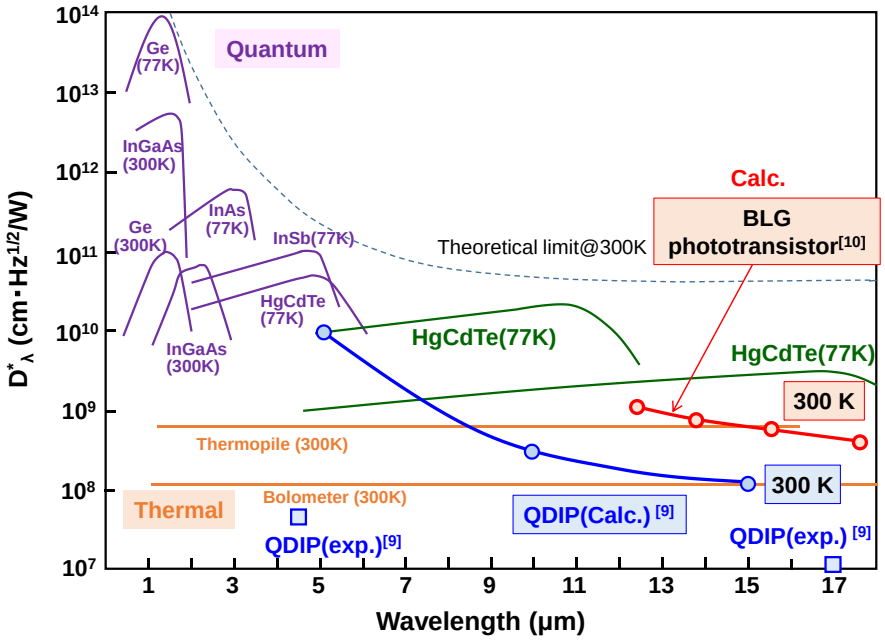


Figure 1.6 Detectivity and operating wavelength. [8]

detectors, the band gap of the detector materials is smaller than 150 meV. Thermal generation of carriers can greatly increase the dark current, increasing the noise compared to the photocurrent. This results in drastic reduction of D* at elevated temperature, making cooling the detectors necessary. Thermal detectors detect current change resulted from temperature change after absorbing infrared. They, can operate at room temperature but have slow response speed due to the delay in temperature change. This is the dilemma for long wavelength infrared detectors.

Quantum detectors

Until recently, HgCdTe detectors has been the mainstream. Band gap of HgCdTe can be tuned by varying the component of Hg and Cd (**Fig 1.7**). Due to its high quantum efficiency of 67% due to direct band gap and mobility of 1×10^4 cm^2/Vs HgCdTe has been widely used as long wave range detectors. Despite low thermal generation, HgCdTe still inevitably requires cooling to achieve high detectivity. Other disadvantages of HgCdTe are nonuniformity over large area and surface instability due to weak Hg-Te bond.

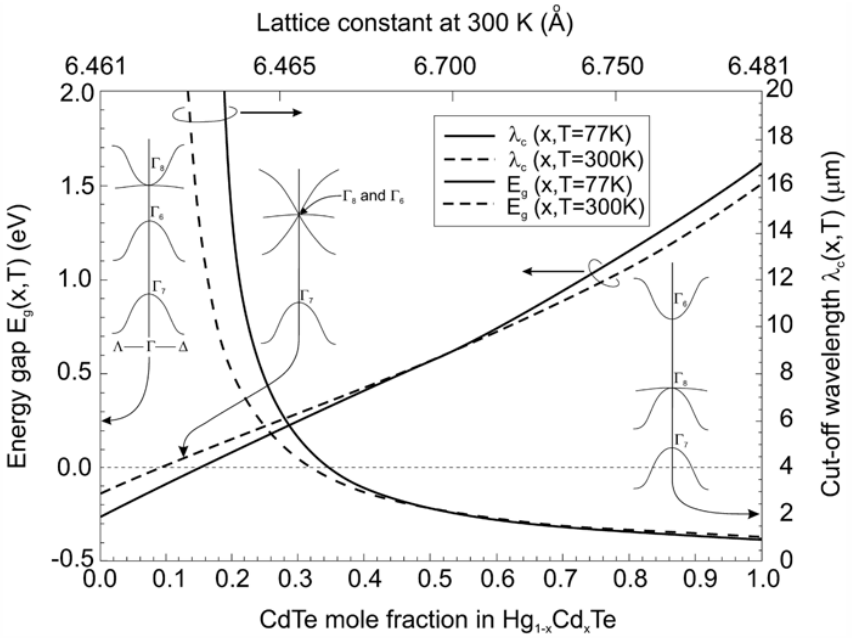


Figure 1.7 Band gap and composition of HgCdTe. [11]

Due to its matured technology, GaAs/AlGaAs quantum well infrared detectors (QWIP) were presented as a rival to HgCdTe. In quantum well, electrons are bound to subband formed in GaAs. Infrared absorption will excite electrons into the continuum transport states (**Fig 1.8**). Due to matured material growth technology, good uniformity over large area can be achieved in QWIP. However, the disadvantage is high thermal generation. This is because energy levels are quantized only in the growth direction leaving a continuum in the rest two directions, allowing thermal generation by longitudinal optical phonons (LO phonons). The comparison of calculated dark current density is shown in **Fig. 1.9**.

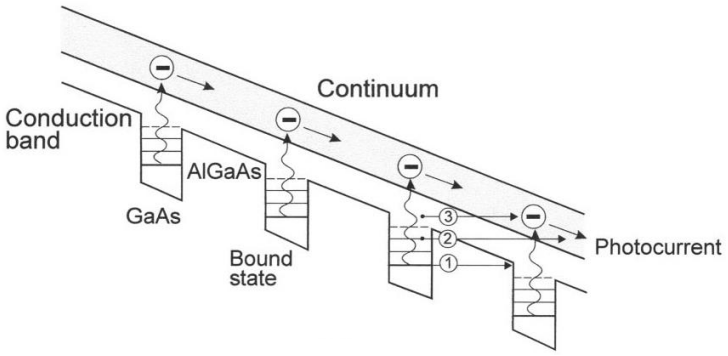


Figure 1.8 Infrared detection in GaAs/AlGaAs quantum well. [12]

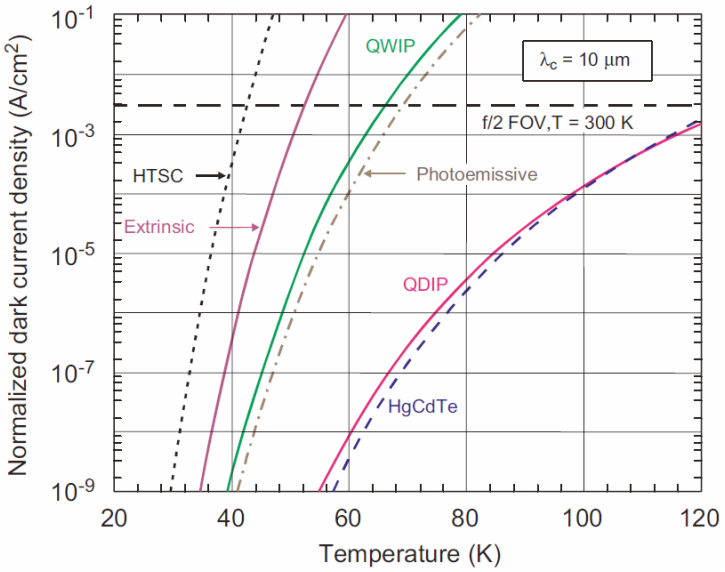


Figure 1.9 Comparison of calculated dark current in infrared detectors. [9] HTSC is high-temperature superconductor. "Extrinsic" denotes extrinsic semiconductor. "Photoemissive" is silicon Schottky barrier diode.

Quantum dot infrared detectors (QDIP) are predicted to have lower dark current at elevated temperature than HgCdTe and QWIP. For long wave range infrared detection, InAs/GaAs quantum dots are mainly used. They can be fabricated by growing InAs on GaAs substrate. When InAs thickness exceed the critical thickness of 1.7 layer, they self-assemble into coherent islands to release the strain from lattice mismatch. Electrons are trapped in subband formed in InAs. Infrared absorption will excite electrons into the conduction band of GaAs, generating photocurrent (**Fig 1.10**). Unlike in QWIP, due to energy quantization in all three directions, electron generation by LO phonons is prohibited, making predicted dark current at near room temperature smaller than HgCdTe and QWIP (**Fig 1.11**). On the other hand, the disadvantage of QDIP is low quantum efficiency. Due to intraband transition and the variation of dot size, experimentally measured quantum efficiency was only 2%. [9] As a result D* is not as high as expected at the present.

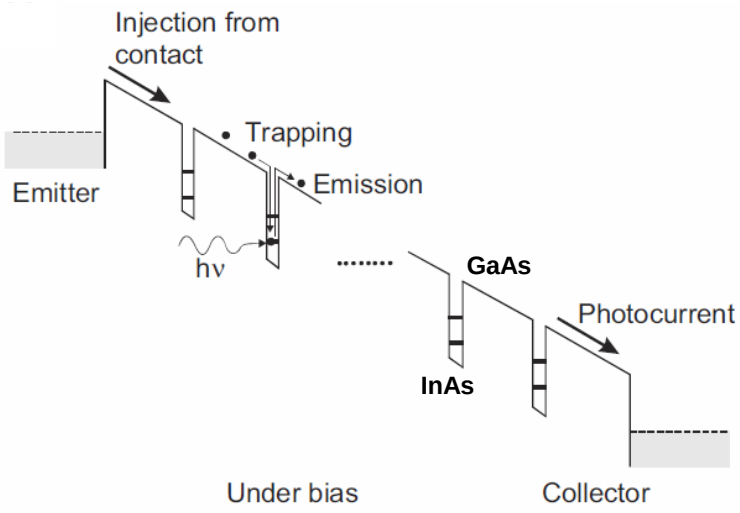


Figure 1.10 Infrared detection in InAs/GaAs quantum dot. [9]

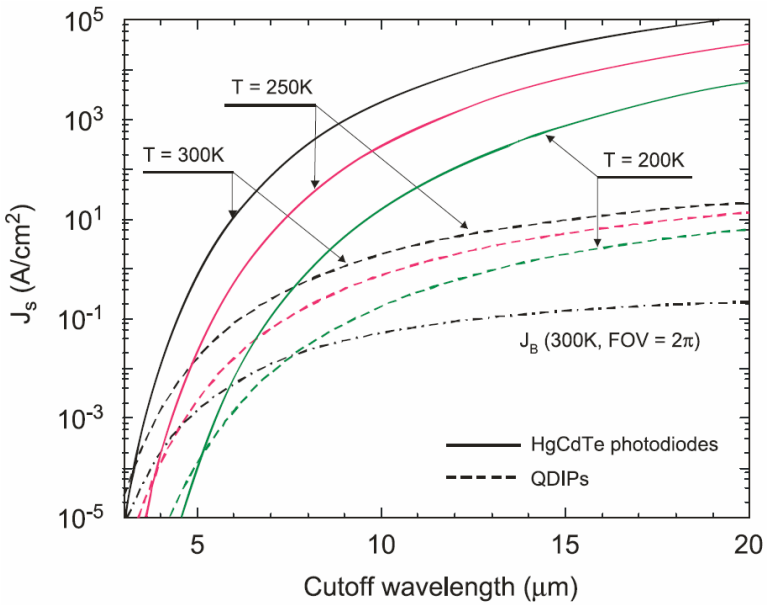


Figure 1.11 Calculated dark current in quantum dots and HgCdTe. [9]

Thermal detectors

In order to eliminate the necessity of cooling and reduce cost for general use of infrared image sensors, uncooled thermal detectors have been developed and commercialized. The currently used system is uncooled infrared focal plane array (IRFPA). IRFPA system is shown in **Fig. 1.12**. Lens is used to focus incident infrared from the field of view onto an array of sensors**.** Field of view is the size of area that can be observed by the detector array and instantaneous field of view is the size of area that a pixel can observe. Each pixel is composed of infrared absorber, thermal sensor, and read-out circuit which serves as heat sink. If thermal conductance of support structure is sufficiently small, a detectible temperature change can occur in detector. Infrared is detected by temperature change by infrared absorption in absorber, which is then detected by thermal sensor. Generated signal from thermal sensor is amplified and sent out by read-out circuit. The performance is limited by thermal noise due to thermal

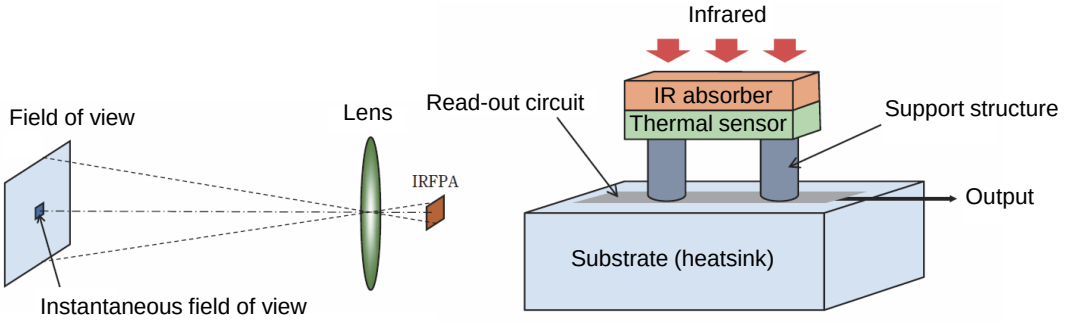


Figure 1.12 Uncooled infrared focal plane array and general structure of a pixel. [13]

conduction through support structure to heat sink. Therefore, reducing thermal conductance of support structure is the key to improvement. At first, detector was connected to Si read out circuit by metal bump (**Fig. 1.13 (a)**). Afterwards, organic mesa and thin film metallic electrode, which have smaller thermal conductance has been used to reduce thermal conductance to heat sink (**Fig. 1.13 (b)**). From 1990s micro electro mechanical systems (MEMS) have been used to further reduce thermal conductance of support structure by separating detector from heatsink, leaving heat conduction path to only small surface area and long support structure (**Fig. 1.13 (c)**).

Reducing pixel size can reduce production cost and reduce camera size. However, reducing pixel area will also reduce the amount of incident infrared per pixel, making signal even smaller. Therefore, the performance can be maintained and improved by increasing sensitivity and reducing thermal conductance of support structure. In past 25 years, the sensitivity has not been improved much; the development has mainly relied on reducing thermal conductance of support structure to compensate for reduced sensitivity. [13] The trend of pixel size and corresponding thermal conductance are shown in **Fig. 1.14**. Thermal conductance of support structure was observed to be proportional to 2.7 power of pixel pitch size. This trend has been used as targets for reducing thermal conductance for certain pixel size in IRFPA. Currently, microbolometer (VO_x or amorphous Si) and silicon-on-insulator (SOI) diode are mainstream for IRFPA. In microbolometer, absorber and bolometer film is suspended from substrate by support legs. Reflection layer is used to reflect remaining incident infrared that transmitted through absorber back to absorber to increase absorption (**Fig. 1.15 (a)**). In SOI diode, single crystal pn junction diode is used as temperature sensor (**Fig. 1.15 (b)**). The diode is forward-biased and the current is kept constant. The change in temperature results

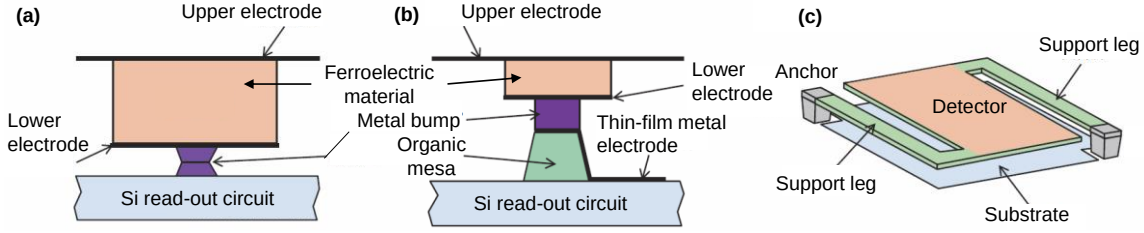


Figure 1.13 (a) Hybrid structure of a pixel. [13] **(b)** Improved hybrid structure. [13] **(c)** MEMS IRFPA pixel structure. [13]

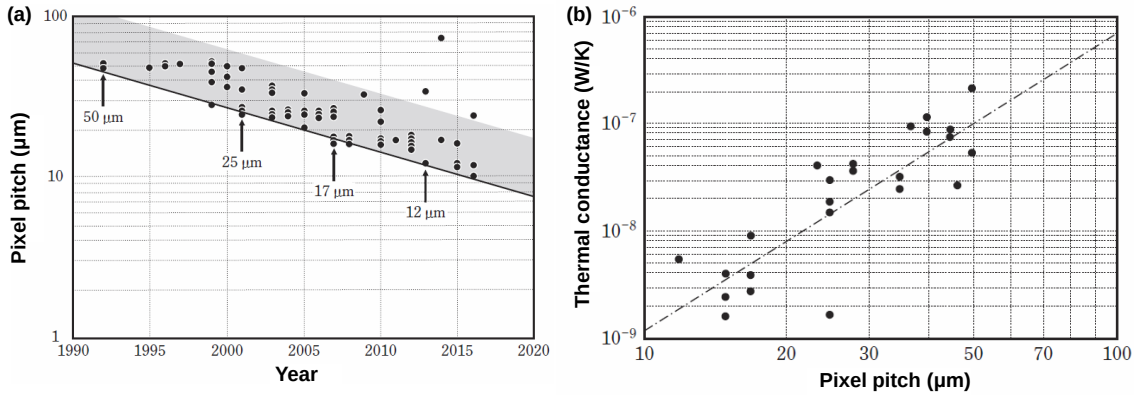


Figure 1.14 (a) Pixel pitch in each year. [13] **(b)** Thermal conductance for each pixel pitch. [13]

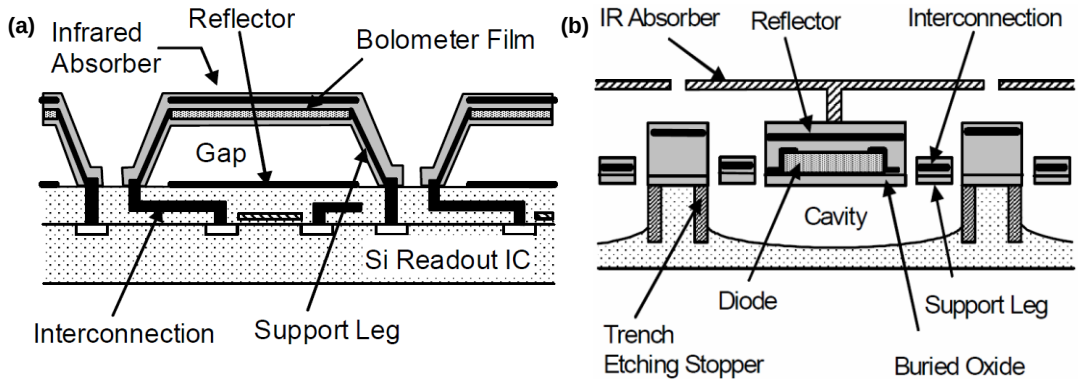


Figure 1.15 (a) Microbolometer pixel structure. [14] **(b)** SOI diode pixel structure. [14]

in variation of bias voltage required for the same current. Therefore, the temperature can be measured from bias voltage. The sensitivity of SOI diode is smaller than amorphous microbolometer but the thermal noise in SOI diode is smaller than amorphous microbolometer, resulting in no significant difference in general performance. However, in SOI diode, the variation of structural parameters that affect sensitivity is smaller, resulting in higher uniformity as an advantage. The maximum framerate reported is 30 fps with 10 ms response time at the present [13].

Bilayer graphene phototransistors

Phototransistors based on bilayer graphene is predicted to show higher D* at room temperature than quantum dots. [10] Although optical absorption is only 2.3% in each graphene layer, it is predicted that current amplification in phototransistor regime shown in **Fig 1.16** can increase the photocurrent to overcome thermal noise and thus, enable room temperature operation. Optical generation of electron-hole pair occurs at the gapped region in dual gated area. Electrons will be swept to drain but holes will accumulate in dual gated area, lowering the potential barrier for electrons from source. As a result, electrons from source will diffuse through the dual gated region, achieving higher current gain. This concept has not been experimentally realized, therefore its realization will be a goal in this study.

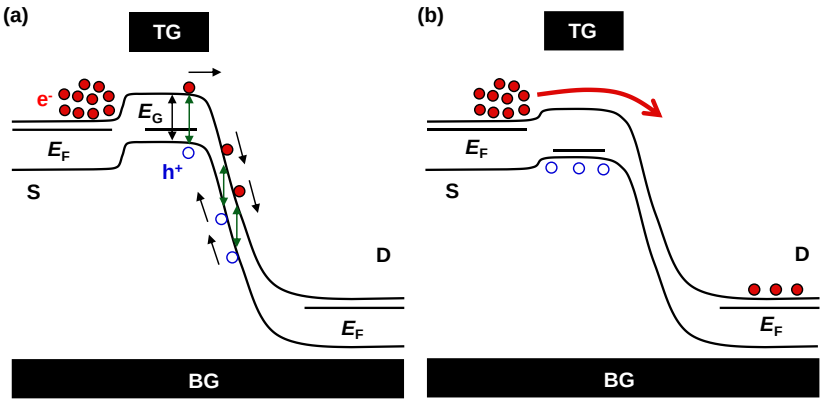


Figure 1.16 (a) Schematics of bilayer graphene phototransistor.
(b) Current amplification by accumulated holes in dual gated area. [10]

1.4 Bipolar transistors and phototransistors

The proposed phototransistor action in bilayer graphene is based on phototransistor action in bipolar transistors. Therefore, operation mechanism of bipolar transistors and phototransistors will be introduced.

Bipolar transistors

Bipolar transistors are generally composed of n-p-n or p-n-p junction transistors. Here, n-p-n case will be considered. The circuit structure, doping profile and band diagram are shown in **Fig. 1.17**. The shown bipolar transistor is composed of emitter, base and collector. Depending on bias configuration, various operation modes are possible (**Fig 1.18**). For general operation, common-base and normal/active regime will be considered, i.e. base is connected to common, negative (forward) bias is applied to emitter, and positive (reverse) bias is applied to collector. The direction of bias and current for this case are shown in **Fig. 1.17 (a)**. In this bias configuration, electrons from the emitter are injected into the base, diffuse through the base and finally collected at the collector, giving collector current. The base acts as barrier to electrons from emitter and ideally does not collect electrons. On the other hand, holes from base diffuse to emitter, manifesting as base current. The current gain of the device is given by the ratio between collector current and base current. Here, the effects of surface recombination-generation and series resistance are neglected. Next, the collector current (I_C) and the base current (I_B) and the current gain will be considered. The current in each component of the device are given by

$$I_E = I_{nE} + I_{rE} + I_{pE}$$
$$I_C = I_{nC} + I_{CO}$$
$$I_B = I_{pE} + I_{rE} + (I_{nE} - I_{nC}) - I_{CO}.$$

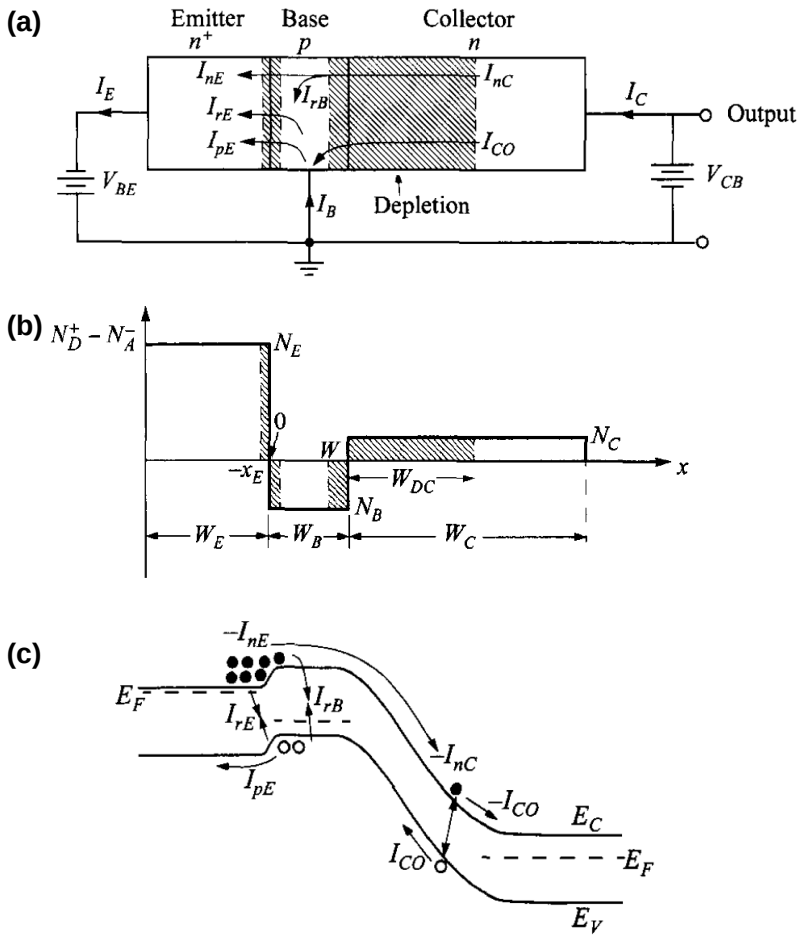
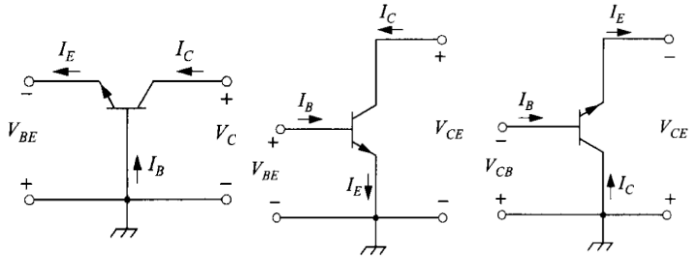


Figure 1.17 (a) Schematics of n-p-n bipolar transistor. [2]

(b) Doping profile of **(a)**. [2]

(c) Band diagram of **(a)**. [2]

(a)



	Common-Base	Common-Emitter	Common-Collector
V gain	High	Medium	Low
I gain	Low	Medium	High

(b)

Operation mode	Emitter-base bias	Collector-base bias
Normal, Active	Forward	Reverse
Saturation	Forward	Forward
Cutoff	Reverse	Reverse
Inverse	Reverse	Forward

Figure 1.18 (a) Bias configuration for bipolar transistor. [2]

(b) Operation mode bipolar transistor. [2]

Here, I_E is emitter current, I_{nE}, I_{rE}, I_{pE} are electron diffusion current, recombination current, hole diffusion current at emitter-base junction, respectively. I_{nC} and I_{CO} are electron diffusion current reaching the collector and reverse current at collector-base junction. The direction of each of these currents in the circuit are shown in **Fig. 1.17 (a)**, while the schematic of physical origin is shown in **Fig. 1.17 (c)**.

First, electron diffusion through the base will be considered. The injected electron distribution is governed by continuity equation

$$0 = -\frac{n_p - n_{p0}}{\tau_n} + D_n \frac{d^2 n_p}{dx^2}.$$

Here, D_n is diffusion constant and τ_n is recombination time. The left side of equation represents the time change. In this case a steady state is considered, therefore time change is zero. The first term on the right side is the recombination and the second term is electron diffusion in base. The general solution is given by

$$n_p(x) = n_{p0} + C_1 \exp\left(\frac{x}{L_n}\right) + C_2 \exp\left(\frac{-x}{L_n}\right)$$

Where C_1 and C_2 are constants and $L_n \equiv \sqrt{D_n \tau_n}$ is electron diffusion length in base. The boundary conditions at each junction are given by

$$n_p(0) = n_{p0} \exp\left(\frac{qV_{BE}}{kT}\right)$$

$$n_p(W) = n_{p0} \exp\left(\frac{qV_{BC}}{kT}\right).$$

The position of 0 and W are at emitter-base junction and collector-base junction shown in **Fig.1.17 (b)**. C_1 and C_2 can be obtained from these boundary conditions;

$$C_1 = \left\{n_p(W) - n_{p0} - \left[n_p(0) - n_{p0}\right] \exp\left(\frac{-W}{L_n}\right)\right\} / 2 \sinh\left(\frac{W}{L_n}\right)$$

$$C_2 = \left\{\left[n_p(0) - n_{p0}\right] \exp\left(\frac{W}{L_n}\right) - \left[n_p(W) - n_{p0}\right]\right\} / 2 \sinh\left(\frac{W}{L_n}\right)$$

I_{nE} and I_{nC} are given by

$$I_{nE} = A_E q D_n \left.\frac{dn_p}{dx}\right|_{x=0}$$

$$= \frac{A_E q D_n n_{p0}}{L_n} \coth\left(\frac{W}{L_n}\right)\left\{\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] - \operatorname{sech}\left(\frac{W}{L_n}\right)\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right]\right\}$$

$$I_{nC} = A_E q D_n \left.\frac{dn_p}{dx}\right|_{x=W}$$

$$= \frac{A_E q D_n n_{p0}}{L_n} \operatorname{cosech}\left(\frac{W}{L_n}\right)\left\{\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] - \coth\left(\frac{W}{L_n}\right)\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right]\right\}$$

Where A_E is cross sectional area of emitter-base junction. In normal mode where $V_{BC} < 0$ and $n_p(W) = 0$, electron currents at the two boundaries are given by

$$I_{nE} = \frac{A_E q D_n n_{p0}}{L_n} \coth\left(\frac{W}{L_n}\right) \exp\left(\frac{qV_{BE}}{kT}\right)$$

$$I_{nC} = \frac{A_E q D_n n_{p0}}{L_n} \operatorname{cosech}\left(\frac{W}{L_n}\right) \exp\left(\frac{qV_{BE}}{kT}\right)$$

The ratio of I_{nC}/I_{nE} is called base transport factor (α_T), and the ratio of I_{nE}/I_E is called emitter injection efficiency (γ). It should be noted that if $W/L_n >> 1$, I_{nC} will approach zero which means the transistor action will be lost.

Next, other current components will be considered. I_{pE} is given by

$$I_{pE} = \frac{A_E q D_{pE} p_{n0E}}{W_E} \left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right]$$

The recombination current is proportional to

$$I_{rE} = \frac{1}{\tau} \exp\left(\frac{qV_{BE}}{mkT}\right)$$

where m is close to two. The reverse current at collector-base junction is given by

$$I_{CO} \approx A_C q \left(\frac{D_{pC} p_{n0C}}{W_C - W_{DC}} + \frac{D_n n_{p0}}{W}\right)$$

The collector current (I_C) and the base current (I_B) as a function of base-emitter voltage (V_{BE}) are shown in **Fig. 1.19**. Four regimes can be observed: low-current non-ideal regime,

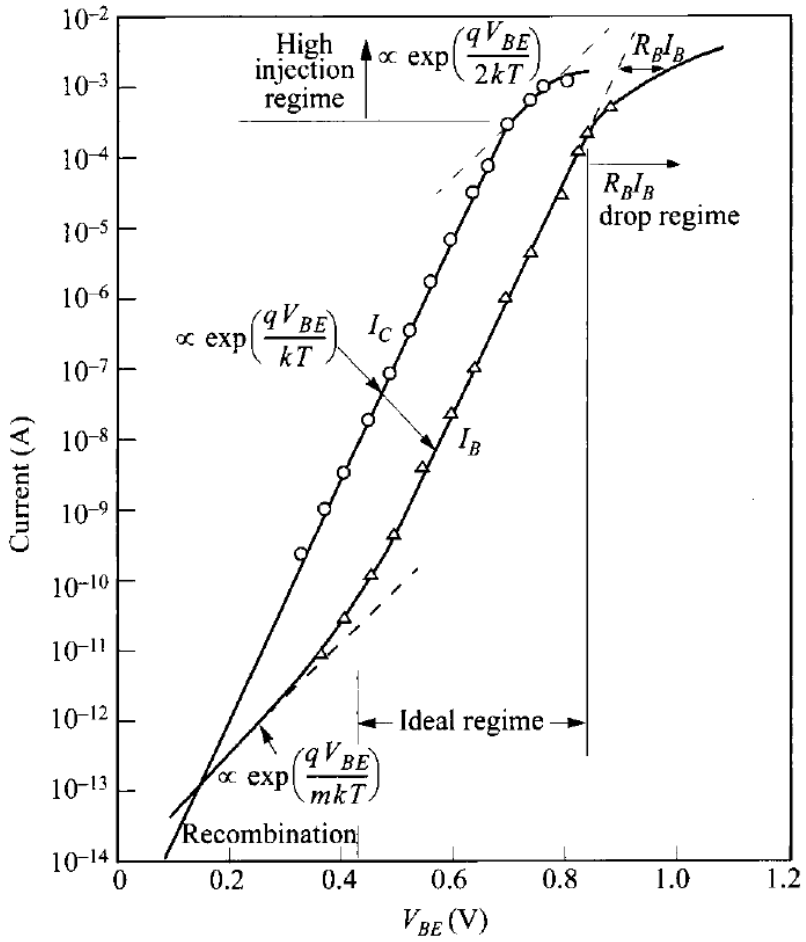


Figure 1.19 Collector current and base current as a function of base-emitter voltage. [2]

ideal regime, moderate-injection regime and high-injection regime. In low-current regime, recombination is more prominent. In moderate-injection regime, voltage drop on base resistance is observed. The current gain for base-common configuration is defined by

$$\alpha_0 \equiv I_{nC}/I_E = \gamma\alpha_T \approx I_C/I_E$$

It can be seen that the current gain is largest and rather constant in ideal regime.

Phototransistors

Phototransistors differ from conventional bipolar transistors by having large base-collector junction area as light-collecting element as shown in **Fig. 1.20 (a)**. The base is kept floating and positive bias is applied to collector while emitter is connected to common (**Fig. 1.20 (b)**). As shown in **Fig. 1.20 (c)**, photogenerated holes at base/collector depletion region flow to energy maximum and are trapped in the base. The accumulation of holes lowers the base energy and allows a large flow of electrons from emitter to

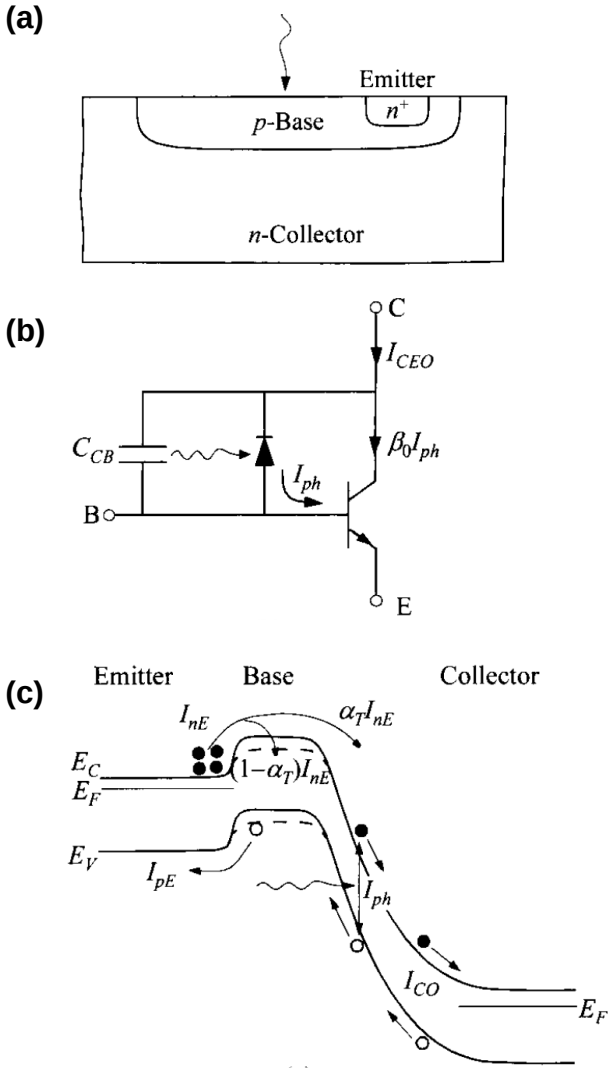


Figure 1.20 (a) Schematics of n-p-n phototransistor. [2]

(b) Circuit configuration. [2]

(c) Band diagram of **(a)**. [2]

collector. This gives a current gain that is larger than one. First, the collector current in common-emitter can be written as

$$I_C = \beta_0 I_B + I_{CEO}$$

where β_0 is defined as common-emitter current gain, given by

$$\beta_0 \equiv h_{FE} = \alpha_0/(1-\alpha_0) \approx I_C/I_B$$

and I_{CEO} is I_{CO} when I_B is zero. The total collector current is given by

$$I_C = I_{ph} + I_{CO} + \alpha_T I_{nE}$$

where I_{ph} is photocurrent at base-collector junction. Because base is open, the net base current is zero

$$I_B = I_{pE} + I_{rE} + (I_{nE} - I_{nC}) - I_{CO} - I_{ph} = 0$$

Ignoring recombination current, one can obtain

$$I_{pE} + (1-\alpha_T) I_{nE} = I_{ph} + I_{CO}$$

Here, using $I_{nE} = \gamma I_E$, it can be shown that

$$I_{CEO} = (I_{ph} + I_{CO})(\beta_0 + 1) \approx \beta_0 I_{ph}$$

indicating a photocurrent gain of (β_0+1). In homojunction transistors gains can be from 50 to a few hundred. In heterojunction phototransistors gain can reach up to 10000. Response time in homojunction phototransistors is around 1-10 µs, limiting operational frequency to 200 kHz. For heterojunction phototransistors, frequency can go beyond 2 GHz. Light intensity dependence in collector current of a phototransistor is similar to base current dependence in bipolar transistor operating in common-emitter configuration shown in **Fig. 1.21**.

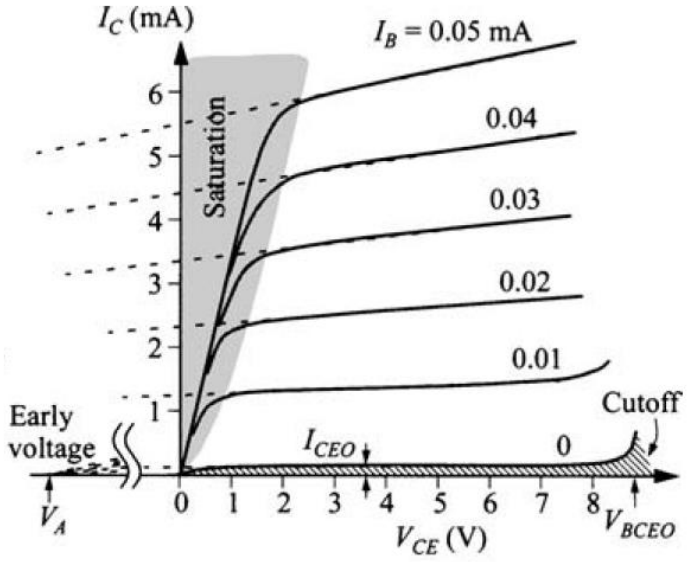


Figure 1.21 Base current dependence for collector current in common-emitter configuration. [2]

Experimental examples

An important factor to be considered in order to achieve phototransistor action is base thickness compared to diffusion length. Here, several base materials will be introduced along with their thickness and diffusion length.

The effect of base thickness on performance of phototransistor was investigated. [15] n-p-n heterojunction phototransistors with InAs/GaSb as base were grown by molecular beam epitaxy (**Fig. 1.22 (a, b)**). Electron diffusion length in p-type InAs/GaSb was calculated and reported to be 3-7 μm in a different study. [16] Device performance was

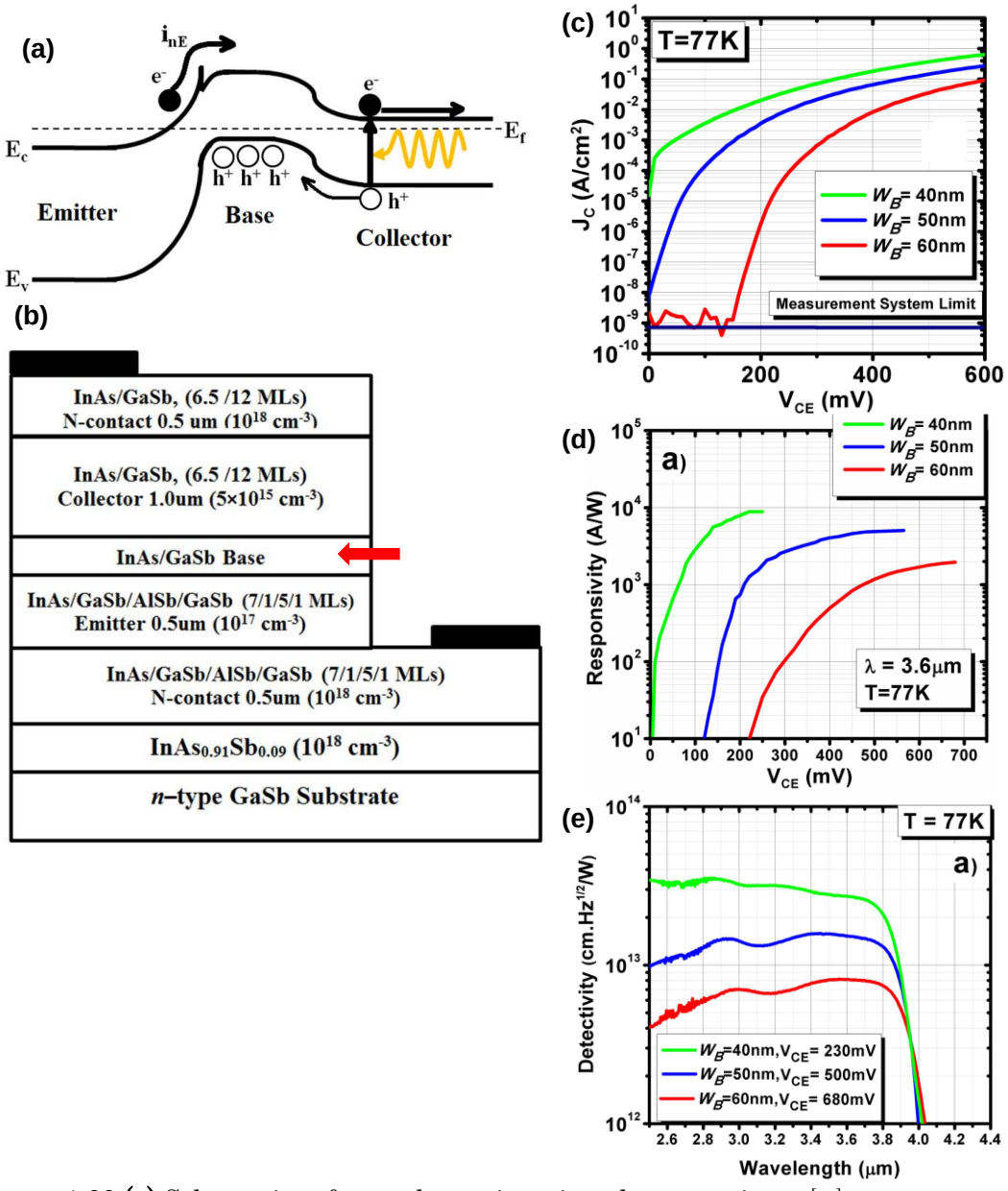


Figure 1.22 (a) Schematics of n-p-n heterojunction phototransistor. [15]

(b) Structure of the device. Base is denoted by red arrow [15]

(c) Dark current as a function of collector-emitter voltage. [15]

(d) Responsivity as a function of collector-emitter voltage. [15]

(e) Detectivity as a function of incident light wavelength. [15]

investigated in devices with base thickness of 40, 50 and 60 nm. Lower dark current was observed in device with thicker base as shown in **Fig. 1.20 (c)**. However, larger responsivity and higher detectivity was obtained in device with thinner base (**Fig. 1.20 (d, e)**). It is interesting that despite small base thickness difference compared to diffusion length, a noticeable performance difference can be observed.

Here, examples of base thickness compared to diffusion length in other bipolar phototransistors will be shown. In p-GaAs/n-Ge/p-Ge, n-Ge base thickness is 0.14 μm [17], while hole diffusion length in Ge is ~220 μm. In n-GaInP/p-GaAs/n-GaAs, p-GaAs base thickness is 70 nm while electron diffusion length is calculated to be 0.5 μm. [18] It can be observed that the base thickness are generally designed to be about two order smaller than diffusion length.

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Chapter 2 FET application for bilayer graphene

2.1 Band gap formation

2.1.1 Theory

Band gap opening in bilayer graphene (BLG) can be explained by tight-binding method. The structure of BLG is shown in **Fig.2.1**. The unit cell is composed of four carbon atoms, denoted as A1, B1, A2 and B2. The two graphene layers are stacked in such way that A2 is directly above B1, which is known as AB stack. The lattice constant a is known to be 0.246 nm. Here $\gamma_0, \gamma_1, \gamma_3, \gamma_4$ are hopping integral between each pair of the nearest neighbor carbon atoms in the unit cell. Their experimental values are shown in **Table. 2.1**. γ_2 and γ_5 are hopping integral between the closest carbon atoms in the first layer and the third layer in graphite and trilayer graphene. Therefore, they will not be considered. The energy of A1, A2, B1, B2 is ε_{A1}, $\varepsilon_{A2}, \varepsilon_{B1}, \varepsilon_{B2}$, respectively. The time-independent Schrödinger equation is given by

$$H\varphi = ES\varphi,$$

where H is hopping integral matrix, E is eigen value of energy, S is overlap integral matrix, and φ is wave function. For non-trivial solution the condition

$$\det (H\text{-}ES) = 0$$

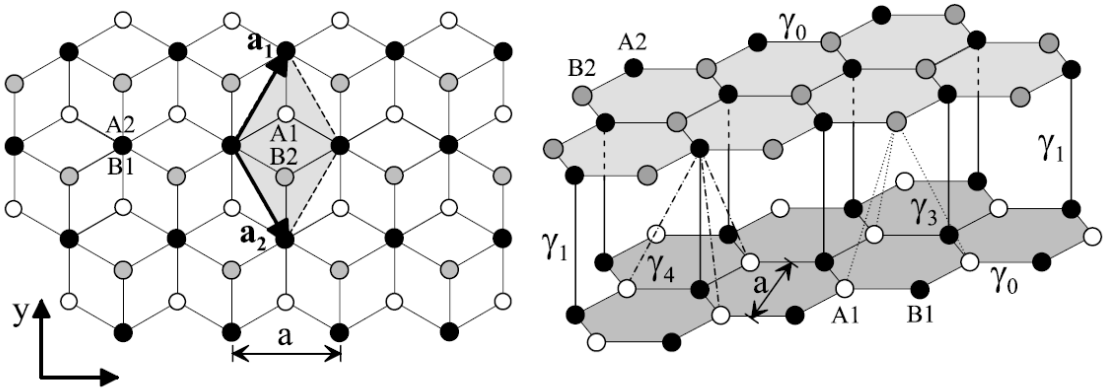

Figure 2.1 Bilayer graphene structure. [1]

Table 2.1 Tight-binding parameters (unit is eV). [1]

Parameter	Graphite [35]	Bilayer [36]	Bilayer [37]	Bilayer [38]	Bilayer [39]	Trilayer [40]
γ_0	3.16(5)	2.9	3.0[a]	—	3.16(3)	3.1[a]
γ_1	0.39(1)	0.30	0.40(1)	0.404(10)	0.381(3)	0.39[a]
γ_2	−0.020(2)	—	—	—	—	−0.028(4)
γ_3	0.315(15)	0.10	0.3[a]	—	0.38(6)	0.315[a]
γ_4	0.044(24)	0.12	0.15(4)	—	0.14(3)	0.041(10)
γ_5	0.038(5)	—	—	—	—	0.05(2)
Δ	−0.008(2)	—	0.018(3)	0.018(2)	0.022(3)	−0.03(2)
Δ′	0.050(6)	—	0.018(3)	0.018(2)	0.022(3)	0.046(10)

[a] This parameter was not determined by the given experiment, the value quoted was taken from previous literature.

is required. Around K point i.e. Dirac point, S can be approximated as unit matrix. H is given by

$$H = \begin{pmatrix} \varepsilon_{A1} & v\pi^* & -v_4\pi^* & v_3\pi \\ v\pi & \varepsilon_{B1} & \gamma_1 & -v_4\pi^* \\ -v_4\pi & \gamma_1 & \varepsilon_{A2} & v\pi^* \\ v_3\pi^* & -v_4\pi & v\pi & \varepsilon_{B2} \end{pmatrix}.$$

Here, $v = \sqrt{3}a\gamma_0/2\hbar, v_3 = \sqrt{3}a\gamma_3/2\hbar, v_4 = \sqrt{3}a\gamma_4/2\hbar$. $\pi = p_x + ip_y, \pi^* = p_x - ip_y$ are for momenta $\mathbf{p} = \hbar\mathbf{k} - \mathbf{K}$ using K point as reference. The upper left 2×2 elements of H represent the Hamiltonian of the lower graphene layer, and the lower right 2×2 elements represent the Hamiltonian of the upper graphene later, the rest of the elements represent interlayer interaction. Now, the effect of potential difference between the two graphene layers and each parameters will be investigated.

Zero potential difference between two graphene layers ($\varepsilon_{A1} = \varepsilon_{A2} = \varepsilon_{B1} = \varepsilon_{B2} = 0$)

i) Effect of γ_1

This parameter defines the difference in E-k relationship between monolayer and BLG. Here, $\gamma_3 = \gamma_4 = 0$, therefore

$$\det(\mathrm{H} - \mathrm{ES}) = \det\begin{pmatrix} -E & v\pi^* & 0 & 0 \\ v\pi & -E & \gamma_1 & 0 \\ 0 & \gamma_1 & -E & v\pi^* \\ 0 & 0 & v\pi & -E \end{pmatrix} = E^4 - \{2v^2p^2 + {\gamma_1}^2\}E^2 + v^4p^4 = 0$$

$$(E^2 - v^2p^2)^2 = (\gamma_1 E)^2$$

$$E^2 - v^2p^2 = \pm\gamma_1 E$$

$$\left(E \pm \frac{\gamma_1}{2}\right)^2 - (vp)^2 = \left(\frac{\gamma_1}{2}\right)^2.$$

E-k relationship for BLG is hyperbolic, as shown in **Fig. 2.2**. Although in tight-binding method, conduction band and valence band seem to touch each other, in first principle calculation they are slightly overlapped [2]. Red bands and black bands represent contribution from each graphene layer. Near Dirac point, E-k relationship can be considered as parabolic. The effective mass is given by

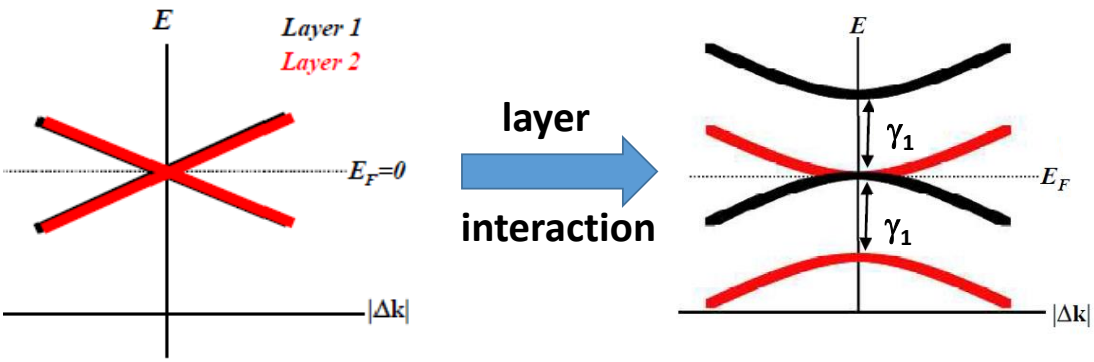

Figure 2.2 Band structure of bilayer graphene when considering only γ_0 and γ_1.

$$m^* = \hbar^2 \left(\frac{d^2E}{dk^2} \right)^{-1}.$$

Therefore the effective mass of electron and hole in BLG is $m^* = \gamma_1/2v^2 = 2.986 \times 10^{-32}$ kg [3], corresponding to 0.033 time of the mass of free electron. On the other hand, the effective mass of carriers in monolayer graphene cannot be determined by the same method due to its linear E-k relationship, so cyclotron mass is used (**Fig. 2.3**). Although carriers in monolayer graphene are called massless Dirac fermion, the effective mass strongly depends on carrier density and becomes heavier than BLG at carrier density larger than 2.6×10^{12} cm^{-2}. The advantage for BLG is that effective mass of carriers is independent of carrier density and much lighter than other two-dimensional layered materials as shown in **Table. 2.2**

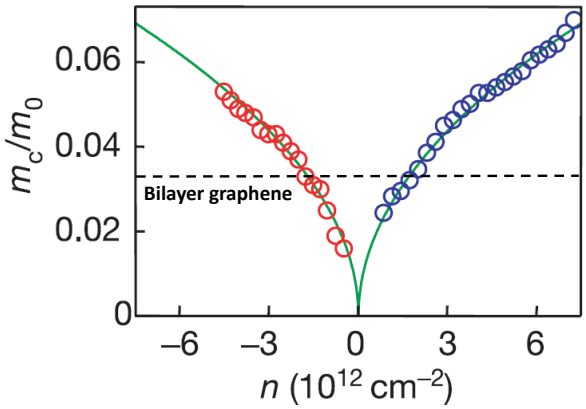

Figure 2.3 Effective mass and carrier density. [4]

Table 2.2 Electron effective mass in two-dimensional layered materials.

Material	**Electron effective mass**
Bilayer graphene	0.033 [5]
MoS_2	0.45 [6]
$MoSe_2$	0.52 [6]
$MoTe_2$	0.57 [6]
WS_2	0.26 [6]
WSe_2	0.31 [6]
Black phosphorus	0.3 [7]

ii) Effect of γ_3

Here γ_3 is also considered. $\gamma_4 = 0$ therefore

$$\det(\mathrm{H} - \mathrm{ES}) = \det\begin{pmatrix} -E & v\pi^* & 0 & v_3\pi \\ v\pi & -E & \gamma_1 & 0 \\ 0 & \gamma_1 & -E & v\pi^* \\ v_3\pi^* & 0 & v\pi & -E \end{pmatrix}$$

$$= E^4 - \{(2v^2 + {v_3}^2)p^2 + {\gamma_1}^2\}E^2 + (v^4p^4 + {\gamma_1}^2{v_3}^2p^2 - \gamma_1 v^2 v_3\{(\pi)^3 + (\pi^*)^3\})$$

$$= E^4 - \{(2v^2 + {v_3}^2)p^2 + {\gamma_1}^2\}E^2 + (v^4p^4 + {\gamma_1}^2{v_3}^2p^2 - 2\gamma_1 v^2 v_3 p^3 \cos 3\varphi) = 0.$$

Here, φ is the angle between **p** and real axis in complex plane

$$\therefore E^2 = \frac{{\gamma_1}^2}{2} + \left(v^2 + \frac{{v_3}^2}{2}\right)p^2 \pm \sqrt{\frac{1}{4}({\gamma_1}^2 - {v_3}^2p^2)^2 + v^2p^2({\gamma_1}^2 + {v_3}^2p^2) + 2\gamma_1 v_3 v^2 p^3 \cos 3\varphi}$$

Let E_l be the solution for lower sub-band when signature is minus and E_h be the solution for upper sub-band when signature is plus. Approximation is possible when $vp/\gamma_1 \ll 1$, $v_3/v \ll 1$ and one can obtain

$${E_l}^2 = (v_3 p)^2 - \frac{v_3 p^3}{m}\cos 3\varphi + \left(\frac{p^2}{2m}\right)^2$$

$${E_h}^2 = {\gamma_1}^2 + 2v^2p^2 + \frac{v_3 p^3}{m}\cos 3\varphi - \left(\frac{p^2}{2m}\right)^2.$$

As shown in **Fig. 2.4**, the equivalent energy surface becomes three-folded symmetric, which is called "trigonal warping".

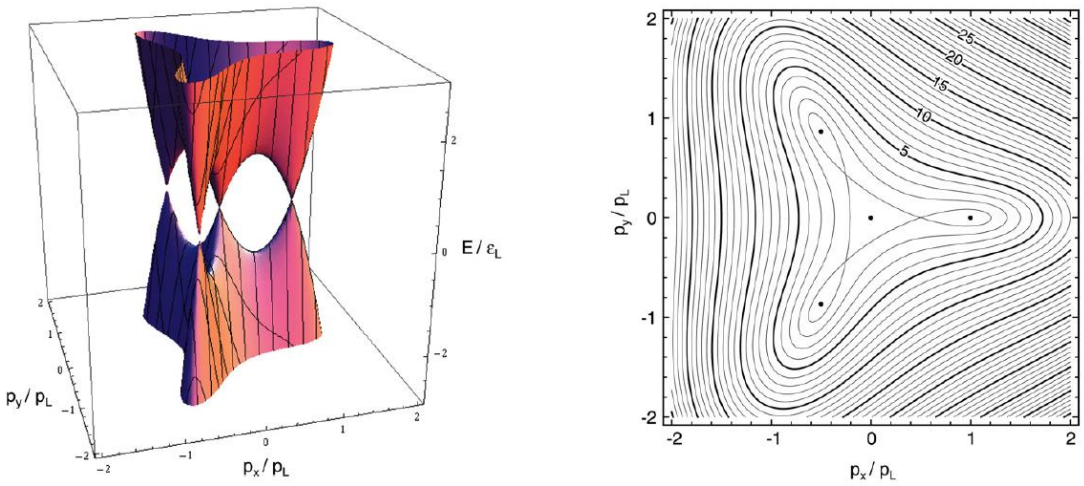

Figure 2.4 Effect of γ_3 on band structure of bilayer graphene. [1]

iii) Effect of γ_4

To investigate the effect of γ_4, consider $\gamma_3 = 0$

$$\det(\mathrm{H} - \mathrm{ES}) = \det\begin{pmatrix} -E & v\pi^* & -v_4\pi^* & 0 \\ v\pi & -E & \gamma_1 & -v_4\pi^* \\ -v_4\pi & \gamma_1 & -E & v\pi^* \\ 0 & -v_4\pi & v\pi & -E \end{pmatrix}$$

$$= E^4 - \{{\gamma_1}^2 + 2(v^2 + {v_4}^2)p^2\}E^2 + 4\gamma_1 v v_4 p^2 E + (v^2 - {v_4}^2)^2 p^4 = 0$$

Using approximation, the energy of the conduction band and the valence band of the lower subband are

$$E_l^c \approx E_l^0 \times \left(1 + \frac{\frac{2v_4}{v}}{\left(1 + \frac{2p^2v^2}{{\gamma_1}^2}\right) - \frac{2v_4}{v}}\right) \approx E_l^0 \times \left(1 + \frac{2v_4}{v}\right)$$

$$E_l^v \approx E_l^0 \times \left(1 - \frac{\frac{2v_4}{v}}{\left(1 + \frac{2p^2v^2}{{\gamma_1}^2}\right) - \frac{2v_4}{v}}\right) \approx E_l^0 \times \left(1 - \frac{2v_4}{v}\right).$$

For the upper sub-band,

$$E_h^c \approx E_h^0 \times \left(1 - \frac{\frac{2vv_4p^2}{{\gamma_1}^2}}{\left(1 + \frac{p^2v^2}{{\gamma_1}^2}\right)\left(1 + \frac{2p^2v^2}{{\gamma_1}^2}\right) + \frac{2vv_4p^2}{{\gamma_1}^2}}\right) \approx E_h^0 \times \left(1 - \frac{2vv_4p^2}{{\gamma_1}^2}\right)$$

$$E_h^v \approx E_h^0 \times \left(1 + \frac{\frac{2vv_4p^2}{{\gamma_1}^2}}{\left(1 + \frac{p^2v^2}{{\gamma_1}^2}\right)\left(1 + \frac{2p^2v^2}{{\gamma_1}^2}\right) - \frac{2vv_4p^2}{{\gamma_1}^2}}\right) \approx E_h^0 \times \left(1 + \frac{2vv_4p^2}{{\gamma_1}^2}\right).$$

This means the slope of the black curves in **Fig. 2.2** becomes smaller, and the slope of the red curves becomes sharper, creating asymmetry between valence band and conduction band as shown in **Fig. 2.5**. The electron effective mass in lower sub-band becomes 1.2 time of the hole effective mass in upper subband. It should be noted that large value of γ_4 is used in **Fig. 2.5** to emphasize the difference.

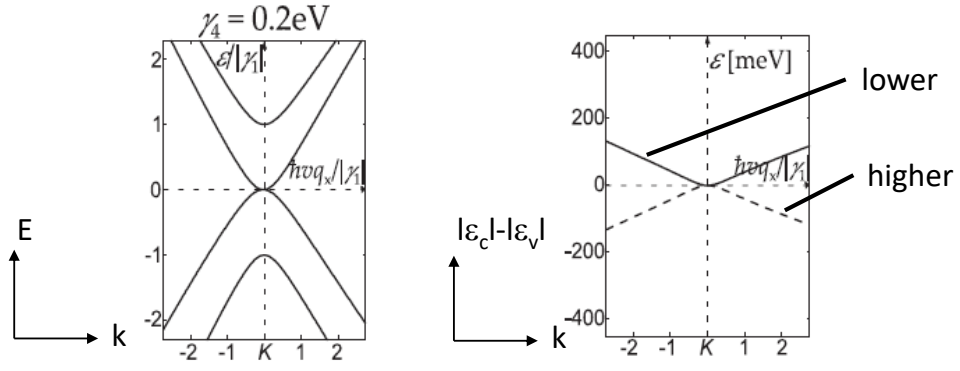

Figure 2.5 Effect of γ_4 on band structure of bilayer graphene. [8]

Finite potential difference between two graphene layers ($\varepsilon_{A1} = \varepsilon_{B1} = -U/2$, $\varepsilon_{A2} = \varepsilon_{B2} = U/2$)

There are several methods to induce potential difference between two graphene layers, such as doping the upper layer by depositing atoms or molecules, causing charge transfer to only the upper layer [9, 10], or applying vertical electric field to create different carrier density in the two layers [11]. For device application, applying vertical electric field is simple and also enables reversible control of band gap. The mechanism of this method is shown in **Fig. 2.6**. One layer of graphene cannot completely screen electric field, causing the electric field to induce smaller carrier density in the layer far from gate electrode. Let n (positive charge) be the total amount of carrier density induced by gate electrode, n_1 be the carrier density induced in the layer near the gate electrode (first layer), and n_2 be the carrier density induced in the layer far from the gate electrode (second layer, both negative charge). Also, $n = n_1 + n_2$. For ease of calculation, let us treat this case as the first layer is given equal amount positive and negative charge, hence not affecting the total charge of the system. This situation is depicted in **Fig. 2.7** where it is assumed that the electric field lines are all terminated by the first layer, and there is a voltage difference V between the two graphene layers induced by a carrier density of n_2. The interlayer capacitance is given by $C_b = \varepsilon_r\varepsilon_0/c_0$, and $V = en_2/C_b = en_2c_0/\varepsilon_r\varepsilon_0$. Here, ε_r is the relative dielectric constant between the two graphene layers, ε_0 is the permittivity of vacuum, c_0 is interlayer distance, e is elementary charge. Let $\triangle_0$ be the energy difference between the two layers caused by external sources such as charged impurities. The energy difference between the two graphene layers is given by

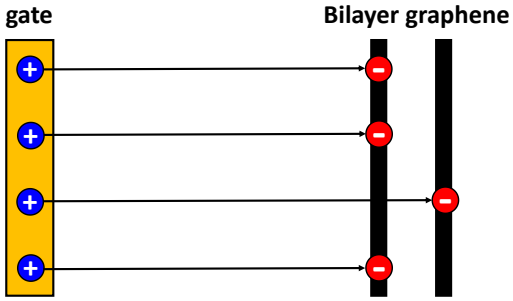

Figure 2.6 Incomplete screening of vertical electric field in bilayer graphene.

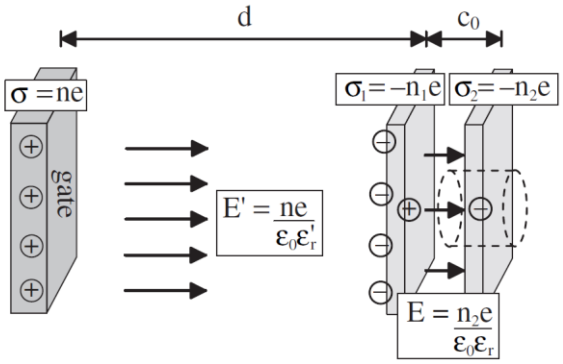

Figure 2.7 Depiction of interlayer capacitance. [12]

$$\Delta(n) = \varepsilon_2 - \varepsilon_1 = \Delta_0 + \frac{e^2 n_2 c_0}{\varepsilon_r \varepsilon_0}.$$

For ease of calculation, the energy for the upper layer and the lower layer are assumed to be U/2 and -U/2 respectively. Now, the effect of each parameters will be investigated.

i) Effect of γ_1

Assume $\gamma_3 = \gamma_4 = 0$,

$$\det(\mathrm{H} - \mathrm{ES}) = \det\begin{pmatrix} -\frac{U}{2} - E & v\pi^* & 0 & 0 \\ v\pi & -\frac{U}{2} - E & \gamma_1 & 0 \\ 0 & \gamma_1 & \frac{U}{2} - E & v\pi^* \\ 0 & 0 & v\pi & \frac{U}{2} - E \end{pmatrix}$$

$$= E^4 - \left\{(2v^2 + {v_3}^2)p^2 + {\gamma_1}^2 + \frac{U^2}{2}\right\}E^2$$

$$+ \left(\frac{U^4}{16} - \frac{1}{2}p^2v^2U^2 + \frac{1}{4}U^2{\gamma_1}^2 + v^4p^4 + \frac{1}{4}U^2{v_3}^2p^2\right.$$

$$\left. - \gamma_1 U^2 v_3\{(\pi)^3 + (\pi^*)^3\}\right) = 0$$

$$E^2 = \frac{{\gamma_1}^2}{2} + \frac{U^2}{4} + v^2p^2 \pm \sqrt{\frac{{\gamma_1}^4}{4} + v^2p^2({\gamma_1}^2 + U^2)}$$

The equation is plotted in **Fig. 2.8**. A band gap in a shape of Mexican hat is created and the size of band gap U_g is proportional to the interlayer energy difference U with the upper limit of γ_1 = 0.38 eV where U approaches infinity.

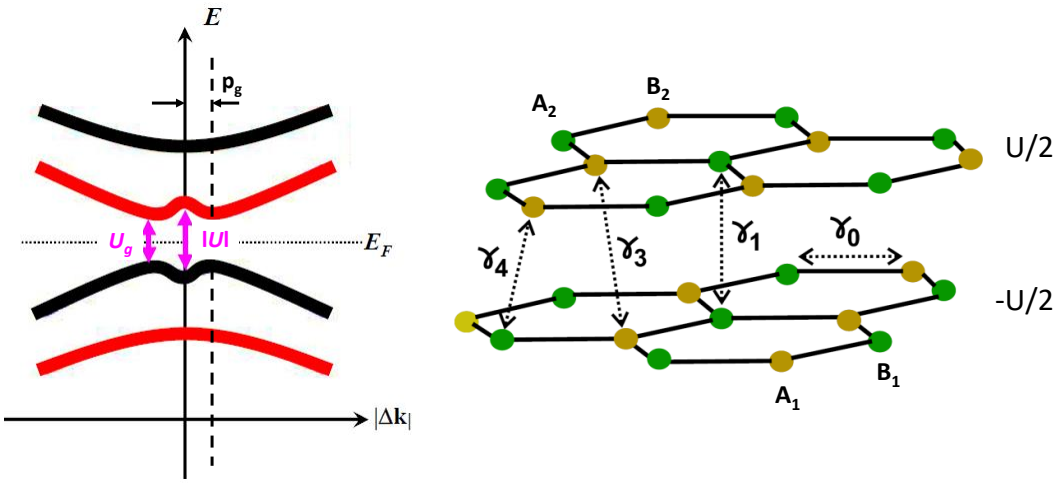

Figure 2.8 Bandgap opening in bilayer graphene. [13]

ii) Effect of γ_3

Assume $\gamma_4 = 0$

$$\det(\mathrm{H} - \mathrm{ES}) = \det\begin{pmatrix} -U/2 - E & v\pi^* & 0 & v_3\pi \\ v\pi & -U/2 - E & \gamma_1 & 0 \\ 0 & \gamma_1 & U/2 - E & v\pi^* \\ v_3\pi^* & 0 & v\pi & U/2 - E \end{pmatrix}$$

$$= E^4 - \left\{(2v^2 + {v_3}^2)p^2 + {\gamma_1}^2 + \frac{U^2}{2}\right\}E^2$$

$$+ \left(\frac{U^4}{16} - \frac{1}{2}p^2v^2U^2 + \frac{1}{4}U^2{\gamma_1}^2 + v^4p^4 + \frac{1}{4}U^2{v_3}^2p^2\right.$$

$$\left. - \gamma_1U^2v_3\{(\pi)^3 + (\pi^*)^3\}\right) = 0$$

$$\therefore E^2 = \frac{{\gamma_1}^2}{2} + \frac{U^2}{4} + \left(v^2 + \frac{{v_3}^2}{2}\right)p^2$$

$$\pm \sqrt{\frac{1}{4}({\gamma_1}^2 - {v_3}^2p^2)^2 + v^2p^2({\gamma_1}^2 + U^2 + {v_3}^2p^2) + 2\gamma_1v_3v^2p^3\cos 3\varphi}$$

This causes trigonal warping in upper sub-band and in lower sub-band.

iii) Effect of γ_4

The effect of γ_4 on gapped BLG is shown in **Fig. 2.9**. The red curves show when $\gamma_4 = 0$, and the black curves show when $\gamma_4 \neq 0$. γ_4 causes conduction band and valence band in gapped BLG to be asymmetric [14].

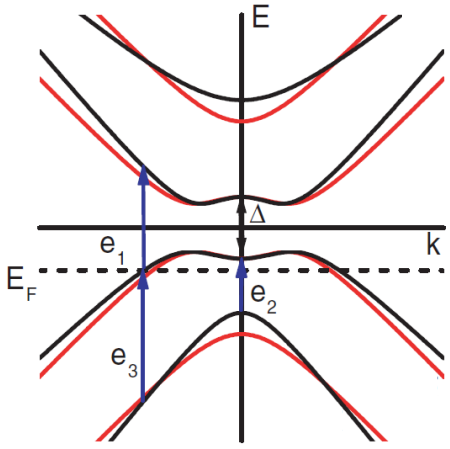

Figure 2.9 Effect of γ_4. [14]

2.1.2 Experiments

Here, previous studies on band gap opening in BLG will be introduced.

Magnesium atoms deposition [9]

The E-k relation of BLG grown on SiC substrate was investigated by angle-resolved photoemission spectroscopy. Initially, the layer close to the substrate is n-doped, so the band gap is already formed (**Fig. 2.10 (a)**). Depositing Mg atoms on the upper layer resulted in n-doping of the upper layer, reducing the carrier density difference between the two graphene layers, leading to the closing of the band gap (**Fig. 2.10 (b)**).further deposition of Mg atoms created carrier density difference between the two graphene layers, therefore opening the band gap again (**Fig. 2.10 (c)**).

Perpendicular electric field [11]

Using dual gate FET structure, different carrier density can be induced in the two layers of graphene. As the back gate voltage is applied, the resistance at charge neutrality point increased, indicating band gap opening (**Fig. 2.11**). The band gap size was investigated by infrared spectroscopy, and was found to be in agreement with the calculation.

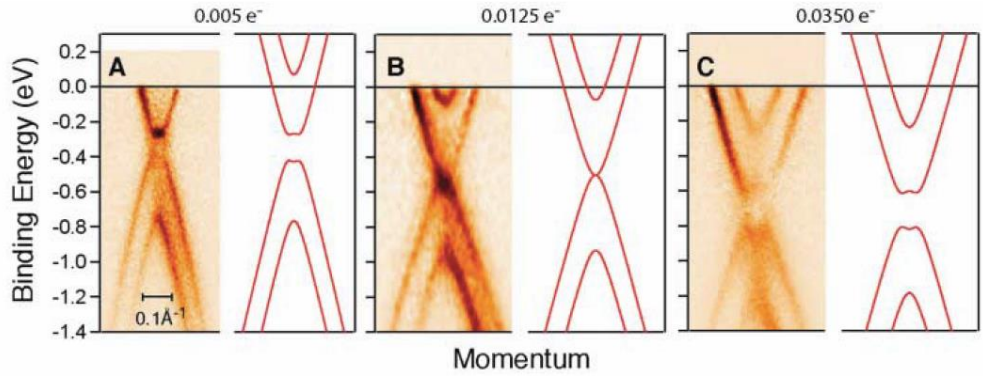

Figure 2.10 (a) E-k relationship of an as-grown bilayer graphene. [9]

(b) Band gap closing afer depositing Mg atoms. [9]

(c) Band gap opening after further Mg deposition. [9]

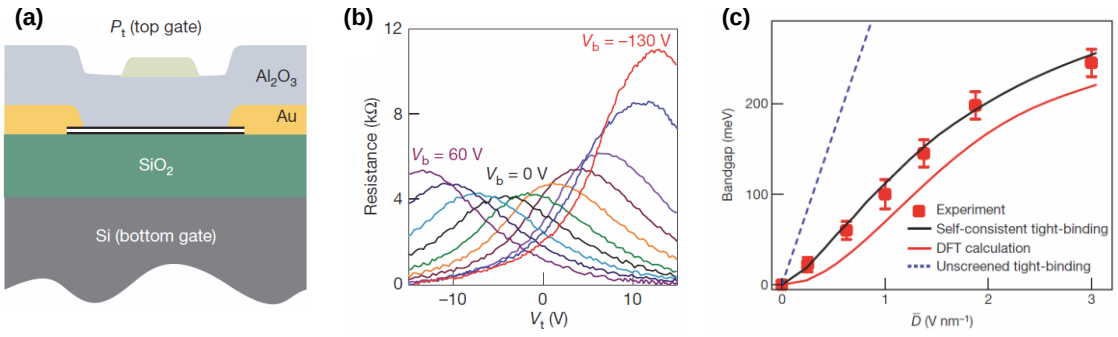

Figure 2.11 (a) Schematics of Dual gate bilayer graphene FET. [11]

(b) Resistance as a function of gate voltage. [11]

(c) Band gap size as a function of displacement field $\bar{D}$. [11]

In experiments, displacement field, $\bar{D}$ is used to imply the magnitude of interlayer potential difference, which is proportional to the band gap size. The displacement field is originally used for electric flux density with unit C/m^2, but for experiments on BLG it is widely used with unit V/nm. $\bar{D}$ is given by [11].

$$\bar{D} = \frac{1}{2}\left[\frac{\varepsilon_{BG}}{d_{BG}}(V_{BG} - V_{BG}^0) - \frac{\varepsilon_{TG}}{d_{TG}}(V_{TG} - V_{TG}^0)\right]$$

$\varepsilon_{BG(TG)}$ is back (top) gate insulator dielectric constant, $d_{BG(TG)}$ is back (top) gate insulator dielectric thickness, $V_{BG(TG)}$ is back (top) gate voltage, $V^0_{BG(TG)}$ is the Dirac point offset caused by doping from environment. Also,

$$\delta D = \frac{\varepsilon_{BG}}{d_{BG}}(V_{BG} - V_{BG}^0) + \frac{\varepsilon_{TG}}{d_{TG}}(V_{TG} - V_{TG}^0)$$

indicates the total amount of carrier density induced by gates, implying Fermi level.

2.2 Present issues in bilayer graphene FET

2.2.1 The necessity of stacking with *h*-BN

To obtain high I_{on}/I_{off} at room temperature for FET application maximum band gap opening is necessary. To open band gap to the maximum, $\bar{D}$ =3 V/nm is required. Therefore, high-k/BLG/SiO_2 gate stack structures have been utilized for this goal so far. However, even in high quality Y_2O_3 gate stack, interface states (D_{it}) of 10^{13} cm^{-2}eV^{-1} was detected by conductance method [15]. This value is two order larger than that in Si/SiO_2 system. Moreover, carrier mobility if graphene devices with oxide gate stack was limited to less than 10,000 cm^2/Vs due to surface roughness of SiO_2 and remote phonon scattering. Conventional semiconductors have sufficient band gap compared to potential fluctuations, therefore their performance has been improved by reducing D_{it} at gate insulator/semiconductor interface. On the other hand, band gap in BLG is about 0.3 eV at most, and is formed by interlayer potential difference. Fixed charges in oxide gate insulators can introduce potential fluctuations of 20-30 meV [16, 17], causing variation of

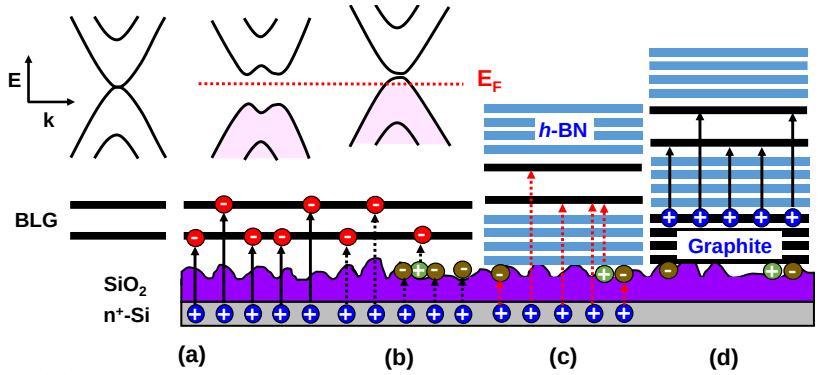

Figure 2.12 (a) Band gap opening in bilayer graphene by applying electric field.
(b) Band gap variation by potential fluctuations.
(c) Electric field screening in SiO_2/n^+-Si back gate.
(d) Electric field from graphite gate electrode.

band gap in the channel (**Fig. 2.12 (b)**). As a result, off-current (I_{off}) is high even at the maximum bad gap, leading to low I_{on}/I_{off}. In order to reduce the variation of band gap in the channel, the potential fluctuation in the channel must be reduced.

Hexagonal boron nitride (*h*-BN) is atomically flat two-dimensional layered insulator. It has smaller charged impurities than SiO_2 as shown in **Fig. 2.13 (b)**. Increased carrier mobility was achieved by using *h*-BN as gate insulator for graphene FET [18]. At first graphene was transferred from transparent polymer films to *h*-BN on SiO_2 substrate by dissolving the polymer. This left polymer residue on graphene even after annealing. Afterwards, a new transfer method which resulted in even higher carrier mobility was reported [19]. In this method *h*-BN on transparent polymer was used to pick graphene up from SiO_2 substrate and then transferred onto *h*-BN on another SiO_2 substrate, encapsulating graphene with *h*-BN without exposing graphene to polymer (**Fig. 2.14**). This was possible because the adhesive force between hydrophobic two-dimensional layered materials is stronger than that between two-dimensional layered material and the hydrophilic SiO_2. Using this "pick-up" method, more complicated heterostructures can be fabricated. Although *h*-BN itself has small charged impurities, using SiO_2/n^+-Si substrate as back gate would still resulted in screening of applied electric field by charged impurities in SiO_2, as shown in **Fig. 2.12 (c)**. This could still propagate the potential fluctuations onto the channel. Therefore, graphite gate electrodes (**Fig. 2.12 (d)**) have been utilized in many recent studies. Because *h*-BN has small dielectric constant of ~4, it has been mainly used in physics study about quantum transport at low carrier density. However, to suppress I_{off} for FET operation, *h*-BN is considered necessary even for device application. By reducing potential fluctuations in graphene FET, various physical phenomena have been discovered. The phenomena that can affect the performance of FET will be discussed.

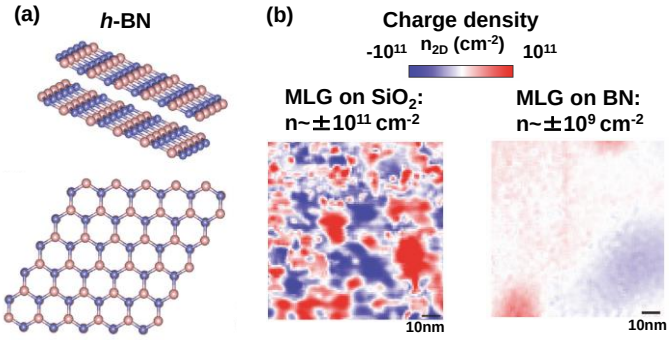

Figure 2.13 (a) Structure of *h*-BN. [20]
(b) Remnant carrier density at Dirac point calculated from STM voltage. [21]

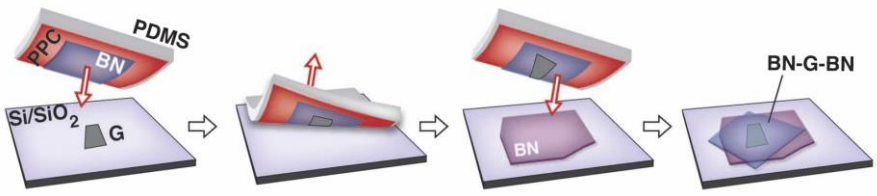

Figure 2.14 Pick-up method. [19]

2.2.2 Topological conduction

In general, topological conduction is metallic conduction that occurs at the edge of two-dimensional insulators or the surface of three-dimensional insulators. The condition required for such phenomena is that the edge or surface of the insulator is "helical" which has time-reversal symmetry, allowing opposite sign of spin current to flow in opposite direction without backscattering. Time-reversal symmetry appears when E-k dispersion is symmetric between k and -k. Without magnetic field, backscatter of single sign of spin cannot occur, leading to momentum locking for each spin. Topological conduction was reported in BLG-FET with a band gap created by applying vertical electric field. Such conduction could limit the suppression of I_{off}, affecting FET performance.

AB-BA domain wall [22]

At AB-BA domain wall in BLG (**Fig. 2.15 (a)**) energy band at k point and k' point are degenerate. Because the sign of momentum at k point and k' point are opposite (**Fig. 2.15 (b)**), their direction of electron conduction are opposite. In this case the states are called "chiral" and are topologically protected, leading to topological conduction at AB-BA domain wall. The chiral edge states appear in the middle of the band gap, and are double spin degenerate leading to four conducting channels **Fig. 2.15 (c, d)**.

AB-BA domain wall can be identified by dark field transmission electron microscopy. [23, 24] The difference in electron beam diffraction angle gives contrast (**Fig. 2.16**). AB-BA domain wall can also be identified by near-field infrared nanoscopy. In this method,

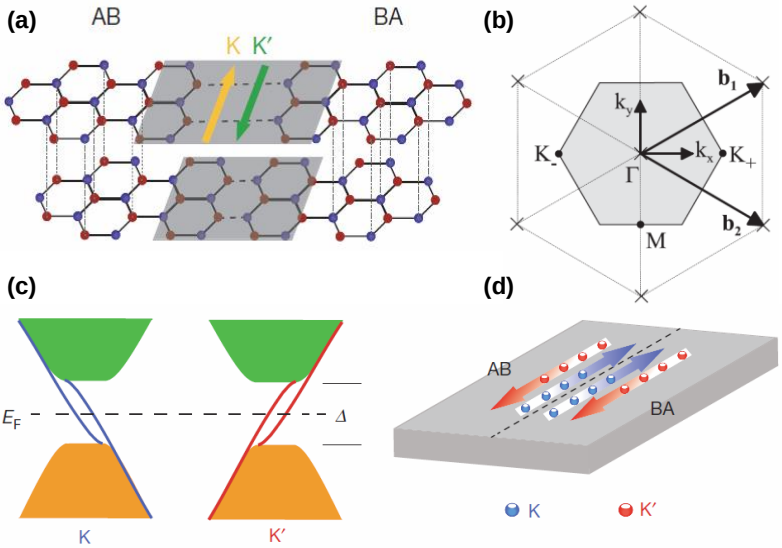

Figure 2.15 (a) AB-BA domain wall. [22]

(b) Reciprocal lattice of graphene. [1]

(c) Chiral edge states in bilayer graphene with AB-BA domain wall. [22]

(d) Topological conduction at AB-BA domain wall. [22]

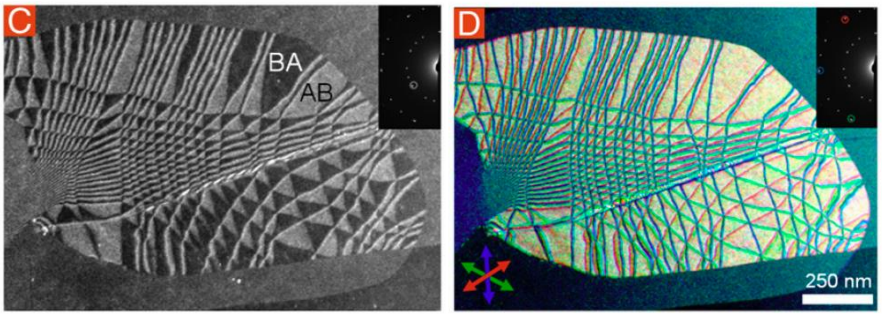

Figure 2.16 Electron beam diffraction image of a bilayer graphene flake. [23]

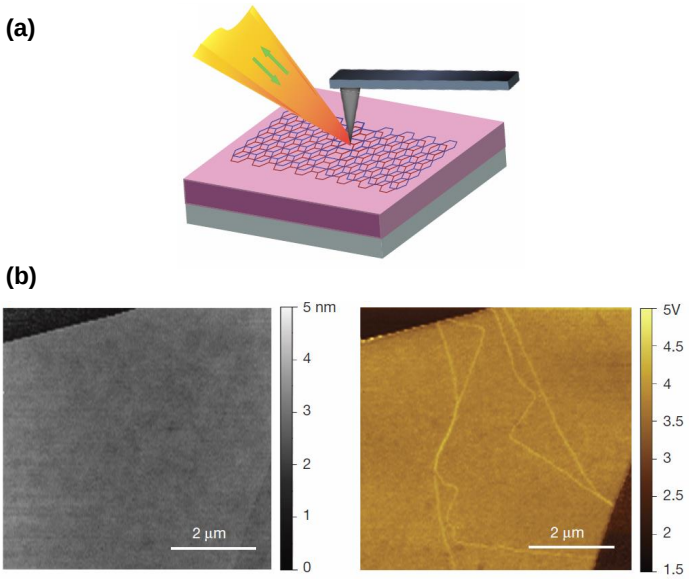

Figure 2.17 (a) Schematics for near field infrared spectroscopy. [22]
(b) AFM image of bilayer graphene. [22]
(c) Near field infrared spectroscopy image of the same sample. [22]

infrared beam is focused on metal-coated AFM cantilever (**Fig. 2.17 (a)**), and infrared absorption is measured from the scattered radiation. AB-BA domain wall has different infrared absorption from the bulk of BLG, and is seen as bright lines in **Fig, 2.17 (c)**.

Dual gate FETs were fabricated on the area with and without AB-BA domain wall in the same BLG flake. The transport measurement results are shown in **Fig. 2.18**. Device without AB-BA domain wall showed continual increase in resistivity at charge neutrality point as back gate voltage was increased, while device with AB-BA domain wall in the channel showed saturated resistivity as back gate voltage was increased. Moreover, the resistivity at charge neutrality point in the device without AB-BA domain wall increased at low temperature, showing insulating behavior, while the resistivity at charge neutrality point in the device with AB-BA domain wall showed no temperature dependence, indicating metallic behavior.

The channel length dependence of the conductivity at charge neutrality point was investigated. In the device with AB-BA domain wall the conductivity at charge neutrality point from the channel length of 200 nm to 1000 nm were of an order of conductance quantum ($2e^2/h$). Especially, in the device with the shortest channel length, the conductivity approached $4e^2/h$ (**Fig. 2.19**). This corresponded to the chiral edge modes theoretically predicted in AB-BA domain wall. The mean free path calculated from the results of the device with AB-BA domain wall was 420 nm, compared to 8 nm in the device without AB-BA domain wall, suggesting the protection from backscattering, which is one of the characteristics of topological conduction.

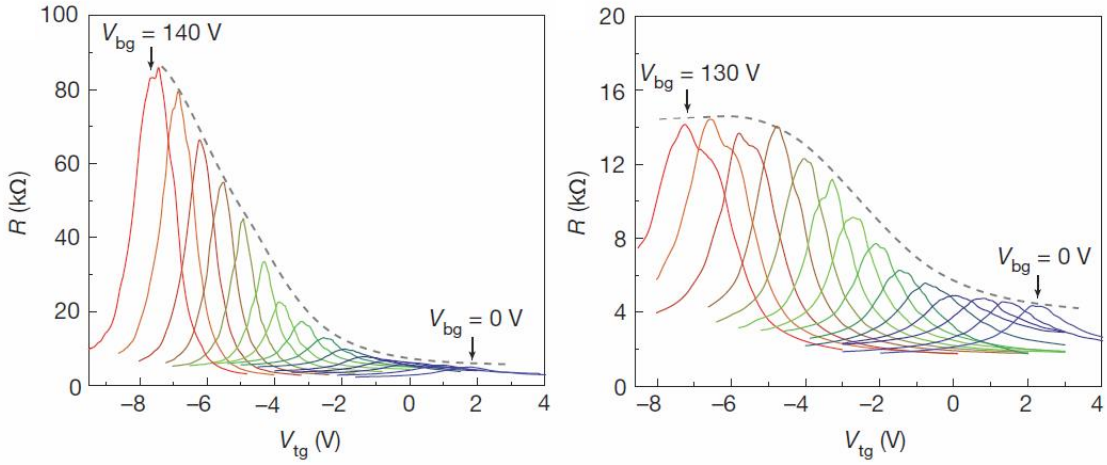

Figure 2.18 Resistivity as a function of gate voltage for device without **(left)**, and with **(right)** AB-BA domain wall. [22]

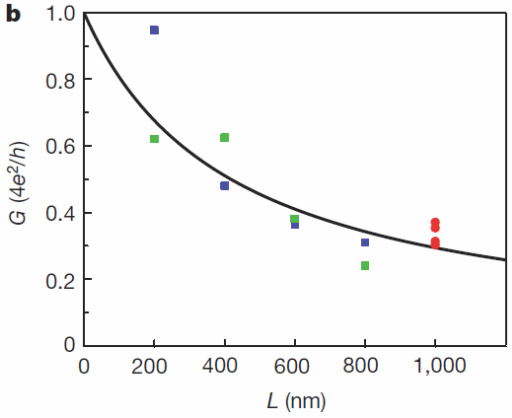

Figure 2.19 Conductivity at charge neutrality point versus channel length. [22]

Gate controlled conductive channel [25]

Opposite displacement field were applied on two close region of BLG to create topological conductive channel between the two gates as shown in **Fig. 2.20 (a)**. By applying opposite displacement field, the potential of the two graphene layers cross and become zero in the middle, causing confinement of electron wave function into one-dimensional topological conducting channel.

Conductivity was measured when the displacement field of the left device was fixed to -0.25 V/nm or 0.25 V/nm while the back gate voltage of the right device was varied (**Figure 2.21**). When the displacement field of both side is the same, suppression of conductivity was observed, suggesting insulating behavior. On the other hand, when the displacement field of both side is reversed, the conductivity was not suppressed, suggesting metallic conduction of chiral mode. Moreover, the channel length dependence of the conductivity in reversed displacement field can be fitted by Landauer-Buttiker equation, confirming one-dimensional conducting behavior of the channel.

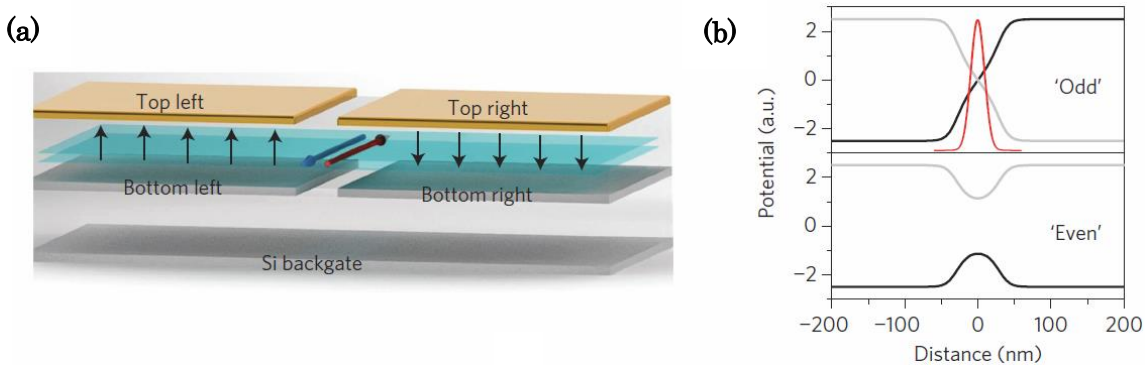

Figure 2.20 (a) Schematics for devices with opposite displacement field. [25]
(b) Potential distribution for displacement field with the opposite sign (Odd) and the same sign (Even). [25]

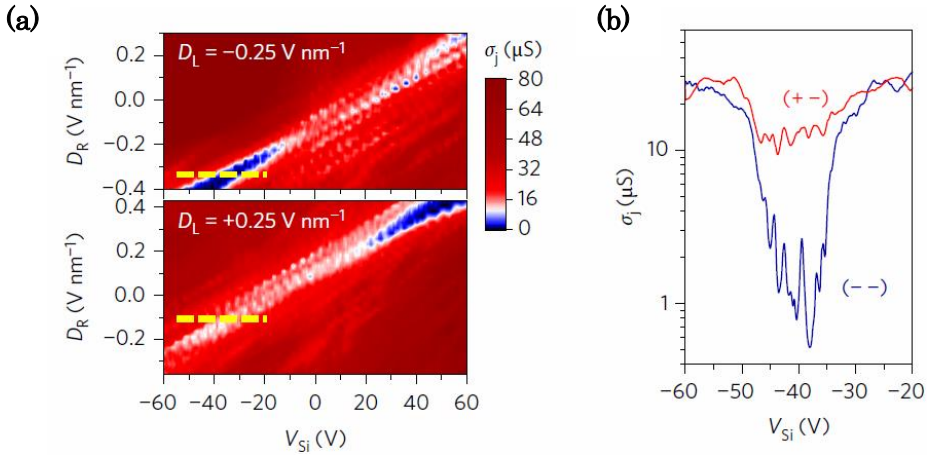

Figure 2.21 (a) Conductivity as a function of displacement field and back gate voltage. [25]
(b) Conductivity measured along the yellow lines in **(a)**. [25]

2.2.3 Edge conduction

Edge conduction in gapped BLG was investigated by observing superconductivity in Josephson junction, and by comparing transport properties in Hall bar configuration and Corbino disc [26].

Superconductor/BLG/superconductor Josephson junction devices with channel

length of 300 - 500 nm and width 3 - 5 μm were fabricated. By measuring critical current as a function of perpendicular magnetic field, local current density in the channel can be deduced. When the displacement field was increased, the current density in bulk was reduced, while the current density in the edge remained relatively higher than in the bulk (**Fig. 2.22**).

In the device with Hall bar configuration, saturation of the resistivity at charge neutrality with increasing displacement field was observed. On the other hand, in the device with Corbino disc configuration, continual increase of resistivity charge neutrality with increasing displacement field was observed (**Fig. 2.23**). These results suggest the possibly of edge conduction in Hall bar device as Corbino disc configuration did not expose any edge of BLG. Moreover, the same behavior in Hall bar configuration was also observed in un-annealed and unpatterned device, suggesting that device fabrication process was not the cause of edge conduction. The exact mechanism of observed edge conduction was unclear but all possible mechanism involves topological conduction.

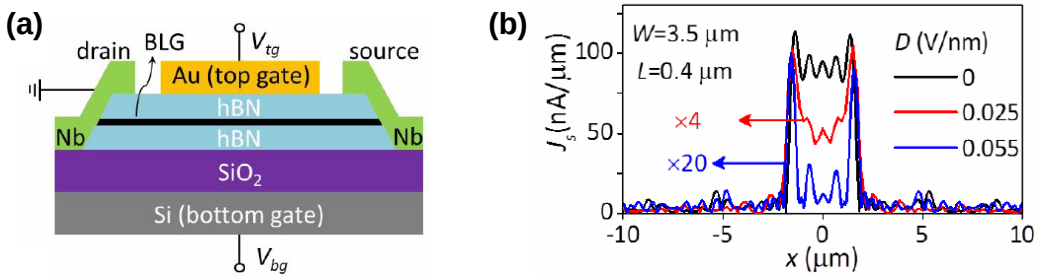

Figure 2.22 (a) Device structure. [26]

(b) Deduced Local density of super current. [26]

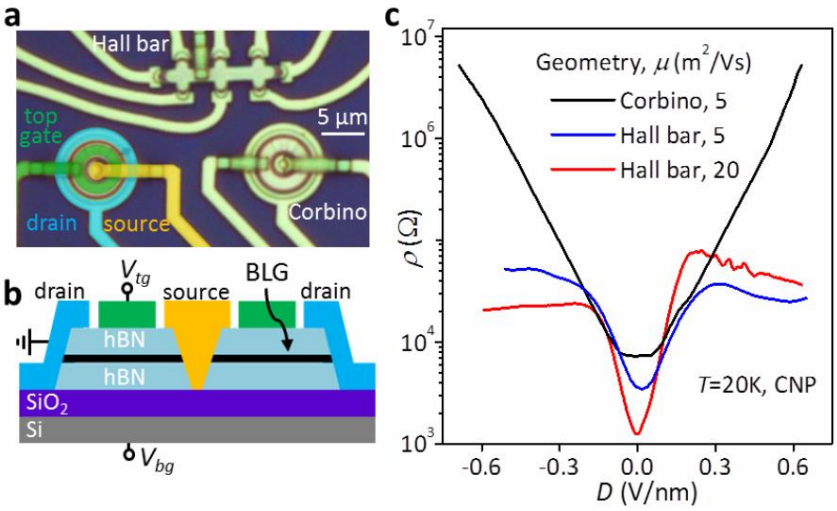

Figure 2.23 (a) Optical image of Hall bar devices and Corbino disc devices. [26]

(b) Schematics of Corbino disc configuration. [26]

(c) Resistivity at charge neutrality as a function of Displacement field. [26]

2.2.4 Rotational angle

When BLG stacking is rotated from AB stack, the E-k dispersion for each layer will also be rotated from each other, creating a different band structure. In this case, the effect of band gap opening at Dirac point with displacement field will be weakened as graphene layers behave more like two separate monolayer graphene sheets (**Fig. 2.24**). [27] Recently, superconductivity was observed in twisted BLG with the so called "magic angle" of 1.1° [28] (**Fig. 2.25**), sparking many research interests in manipulating band structure with twist angle.

In *h*-BN encapsulated graphene, the rotational angle between graphene and *h*-BN can alter the band structure of graphene. When the rotational angle of graphene is close to that of *h*-BN Moiré pattern is created, introducing additional periodic potential to graphene. This opens band gap at charge neutrality point and creates replica Dirac point at higher energies, as seen in transport characteristics (**Fig. 2.26**).

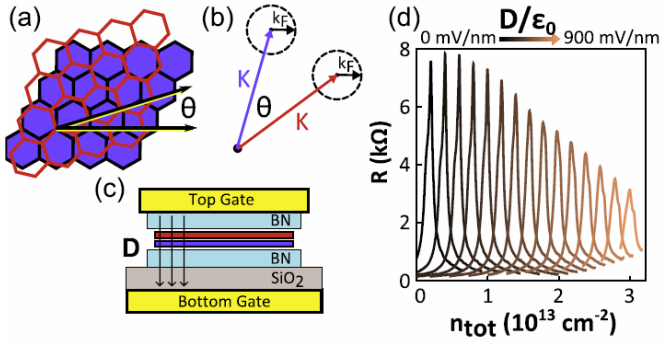

Figure 2.24 **(a)** Twisted bilayer graphene. [27]

(b) Effect of twist angle on E-k relationship. [27]

(c) Device structure. [27]

(d) Resistivity as a function of displacement field. [27]

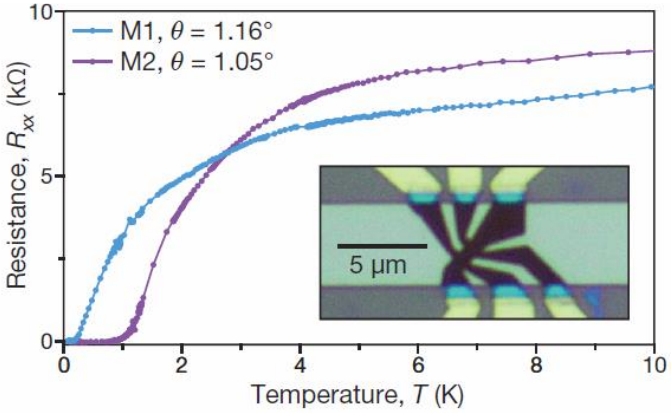

Figure 2.25 Zero resistance at low temperature in bilayer graphene with twist angle near magic angle. [28]

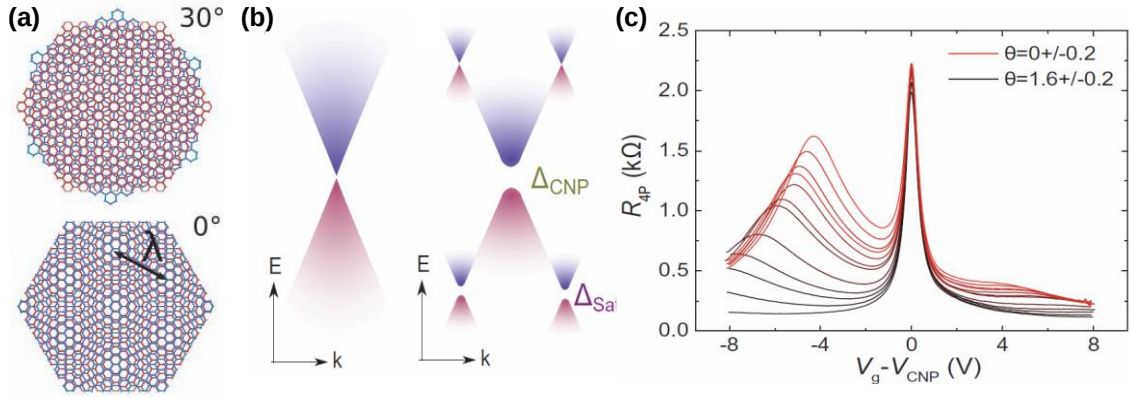

Figure 2.26 (a) Moiré wavelength in aligned graphene/*h*-BN superlattice. [29]

(b) Band structure modification by moiré potential. [29]

(c) Resistivity as a function of gate voltage for each rotational angle. [29]

2.3 Quantum capacitance

Due to its small density of states (DOS), when gate voltage is applied on graphene, some of electrostatic energy will be used to move Fermi energy in order to induce carrier in graphene. The used energy is treated as quantum capacitance.

Quantum capacitance due to small DOS [30]

Consider capacitors made of three parallel plates (**Fig. 2.27 (a)**). If the plate in the middle (Q) is metal, the electric field lines will all be terminated by it. But if Q is two-dimensional metal (such as two-dimensional electron gas in a quantum well), some electric field lines will penetrate it and induce charge in the lower plate, due to Q having small DOS. As a result, the equivalent circuit will be as shown in **Fig. 2.27 (b)**. Here, C_1, C_2 are geometric capacitance and C_Q is quantum capacitance, where

$$C_i = \frac{\varepsilon_i}{4\pi d_i}, i = 1,2$$

$$C_Q = \frac{g_v m e^2}{\pi \hbar^2} = g_v \frac{m}{m_0} \times 6.00 \times 10^7 \ cm^{-2}.$$

m is electron effective mass in direction perpendicular to quantum well and g_v is valley degeneracy factor. Below the derivation of the equivalent circuit and equations above will be described.

Let σ_1, σ_2, σ_Q be charge density in electrode 1, 2 and the quantum well, respectively. The charge neutrality condition $\sigma_1 + \sigma_2 + \sigma_Q = 0$ can be written in the form of

$$\sigma_2 = -\sigma_1 sin^2(\varphi)$$
$$\sigma_Q = -\sigma_1 cos^2(\varphi)$$

where φ is a variational parameter to be determined by minimizing the total energy of the system (E_{tot}). E_{tot} is the total energy between energy for the field energies (E_i) and

Fermi-degeneracy energy (E_Q), which are given by

$$E_i = \int_0^{d_i} \frac{\varepsilon_i {F_i}^2 dx}{8\pi} = \frac{2\pi d_i {\sigma_i}^2}{\varepsilon_i}, i = 1,2$$

$$E_Q = \frac{\pi\hbar^2 {\sigma_Q}^2}{2g_v m e^2}.$$

Here, electron interaction was neglected. Varying $\delta E_{tot} = 0$ we find

$$tan^2(\varphi) = \frac{\hbar^2 \varepsilon_2}{4mg_v d_2 e^2} \equiv \frac{C_2}{C_Q}$$

Which prove the equivalent circuit in **Fig. 2.27(b)**. The charge induced in the lower metal plate is

$$\sigma_2 = -\sigma_1 \frac{C_2}{C_2 + C_Q}.$$

Quantum capacitance is a consequence of Pauli principle of exclusion which require extra energy to fill up a quantum well with electrons. In classical limit where $\hbar \to 0$ or $m \to \infty$, C_Q will become ∞ making C_Q and C_2 become negligible as they should. For MOS structure on Si (100) surface, $g_v = 2$, $m = m_l = 0.98\ m_0$, therefore $C_Q \gg C_1 = C_{oxide}$ for all realistic oxide thicknesses. When m becomes small, C_Q will become comparable to geometric capacitance, so C_Q needs to be considered.

In graphene the effect of C_Q can be observed when geometric capacitance is comparable to C_Q. Carrier density induced for each SiO_2 gate thickness is shown in **Fig. 2.28**. When gate geometric capacitance is large enough with thin thickness, the behavior of carrier induced is affected by C_Q. By measuring total capacitance and extracting C_Q, DOS can be calculated. DOS of two-dimensional material is given by [31]

$$C_Q = q^2 g_{2D} \left[1 + \frac{\exp(E_g/2k_B T)}{2\cosh(qV_{Ch}/k_B T)}\right]^{-1}$$

where $g_{2D} = g_s g_v m^*/2\pi\hbar^2$ is the band-edge DOS, g_s and g_v are the spin and valley degeneracy factors. At low temperature, C_Q can be approximated as $C_Q = e^2$ DOS.

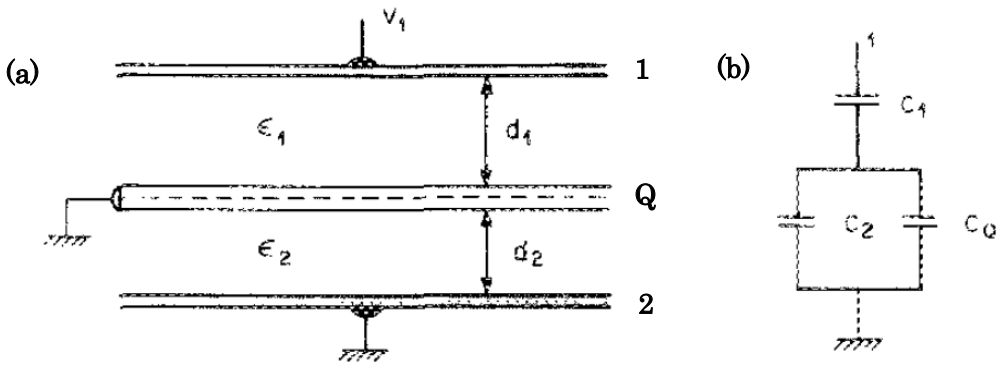

Figure 2.27 (a) Three-parallel plate capacitor.

(b) Equivalent circuit for when Q is two-dimensional metal.

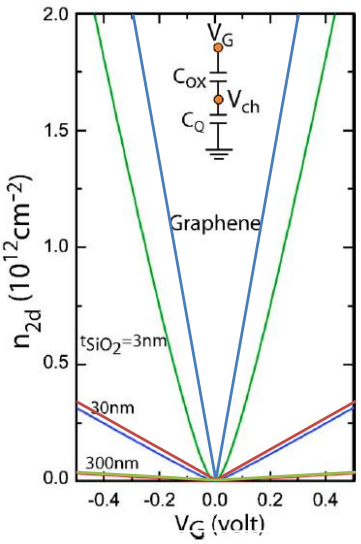

Figure 2.28 Carrier density induced by various SiO_2 thickness. Inset: equivalent circuit with graphene. [32]

Quantum capacitance due to Fermi level change

Total capacitance of inversion layer in bulk Si and SOI MOSFET is the serial capacitance composed of gate geometric capacitance and effective thermodynamic density-of-states capacitance (C_{dos}). Effective thermodynamic density-of-states capacitance is composed of a serial capacitance between capacitance related to thermodynamic density of states when Fermi level remains constant (C_N), and capacitance related to increasing Fermi level (C_{level}). Their comparison is shown in **Fig. 2.29**.

In BLG, quantum capacitance is composed of serial capacitance between capacitance related to small DOS, and capacitance related to band structure changing along with changing Fermi level. By keeping displacement field constant, capacitance related to small DOS can be extracted. In the thesis, capacitance related to small DOS will simply be referred as C_Q

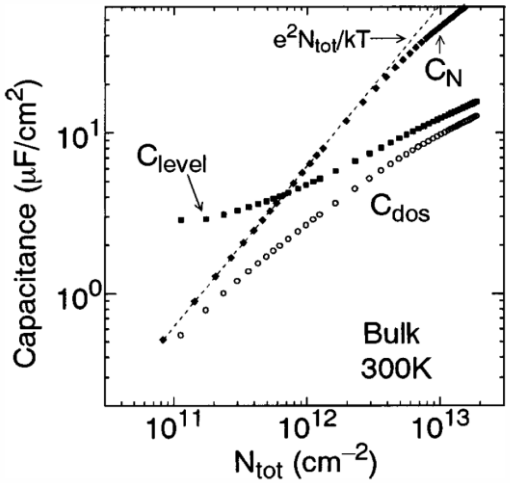

Figure 2.29 C_{DOS}, C_N, C_{level} plotted against carrier density induced in bulk silicon. [33]

2.4 Capacitance measurement in bilayer graphene

Capacitance measurement can be used to investigate band gap in gapped BLG. The behavior of CV curve is strongly affected by disorder from potential fluctuations, therefore features in CV curve of gapped BLG can be used for qualitative and quantitative evaluation of band gap in the device.

2.4.1 van Hove singularity

In gapped BLG, DOS becomes zero around Dirac point and approaches infinity at gap edges (**Fig. 2.30**). This is called Van Hove singularity (VHS). Here the DOS in each graphene layers will be considered. A dual gate structure is shown in **Fig.2.31** where v is potential, n is carrier density, C is capacitance, 1&2 denote first and second layer, and t&b denote top gate& back gate, respectively.

The divergence of DOS is related to electronic compressibility in each layer and interlayer electronic compressibility. Electronic compressibility is thermodynamic DOS, and is expressed in form of matrix with each component given by [30]

$$\nu_{ij} = -\frac{\partial n_i}{\partial v_j}.$$

Electronic compressibility components in BLG can be calculated as

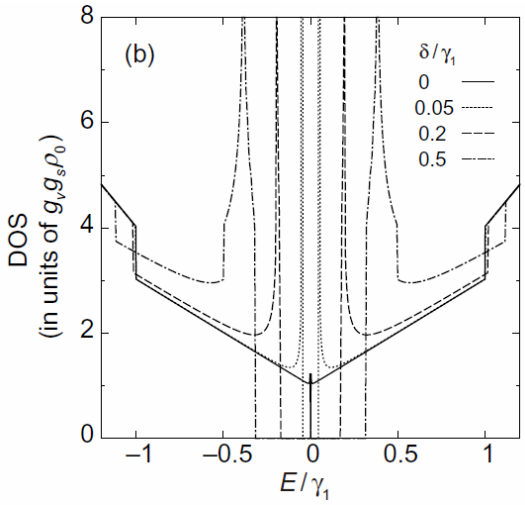

Figure 2.30 DOS of gapped bilayer graphene. δ denotes interlayer potential difference. [5]

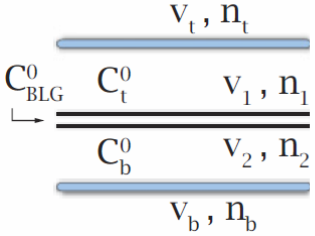

Figure 2.31 Potential and carrier density in each graphene layer.

$$\nu_{11} = \frac{1}{2}\nu_0 \frac{|v_+| - v\_sgn\, v_+}{\sqrt{v_+^2 - v_-^2}} + \frac{1}{4}\widetilde{\nu_0}$$

$$\nu_{22} = \frac{1}{2}\nu_0 \frac{|v_+| + v\_sgn\, v_+}{\sqrt{v_+^2 - v_-^2}} + \frac{1}{4}\widetilde{\nu_0}$$

$$\nu_{12} = \nu_{21} = -\frac{1}{4}\widetilde{\nu_0}$$

where $v_0 = 2me^2/(\pi\bar{h}^2)$, $v_\pm = \frac{1}{2}(v_1 \pm v_2)$, $\widetilde{\nu_0} = \nu_0 ln\left[\frac{2\Lambda}{e\left(|v_+| + \sqrt{v_+^2 - v_-^2}\right)}\right]$, e=2.71828, Λ is UV cut-off value. ν_{11}, ν_{22} are electronic compressibility of the first and second layer themselves, reflecting DOS of each layer. ν_{12}, ν_{21} are interlayer compressibility, ν_+ represents Fermi energy and ν_- is interlayer potential difference. When $v_1 \to 0$, the denominator of the first term of ν_{11} will become zero making ν_{11} approach ∞, while ν_{22} remains finite. In other words, when the potential in layer 1 becomes zero, the DOS becomes ∞, showing VHS. Similarly, when $v_2 \to 0, \nu_{22}$ will approach ∞ while ν_{11} stay finite. These cases happen when ν_+ is at the gap edge. As a result, two VHS peaks occur from different graphene layer. An example is shown in **Fig. 2.32** where ν_- is set to 50meV, and $\nu_{11}, \nu_{22}, \nu_{12}$ are plotted. The DOS of gapped BLG can be considered as the summation of $\nu_{11}, \nu_{22}, \nu_{12}, \nu_{21}$. When disorder from charged impurities is present, VHS will become smeared and band gap will appear smaller.

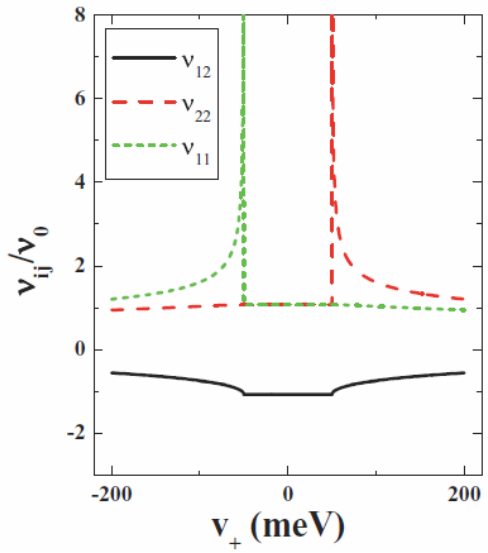

Figure 2.32 Electronic compressibility components in gapped bilayer graphene. [33]

2.4.2 Capacitance measurement methods

Here, measurement methods used to extract DOS in gapped BLG will be introduced.

Top gate capacitance method

In this method, gate voltage is applied on top gate and capacitance is measured by source (**Fig 2.33 (a)**). The measured capacitance (C_{TG}) is given by

$$\frac{1}{C_{TG}} = \frac{1}{C_{TG}^0} + \frac{1}{C_Q}$$

where C_{TG}^0 is geometric capacitance of top gate, and C_Q is quantum capacitance related to small DOS. When displacement field is applied and band gap is formed, C_{TG} decrease around charge neutrality point (**Fig.2.33 (b)**). When VHS occurs in the lower layer, its response will be screened by finite electron compressibility of the upper layer. As a result, VHS seen in CV curve will be asymmetric, making VHS in the layer near the top gate appear larger than the other (**Fig.2.33 (c)**). This is called "Near layer capacitance enhancement" [34]. If disorder is present, band gap will appear smaller and VHS will be smeared (**Fig. 2.33 (d)**).

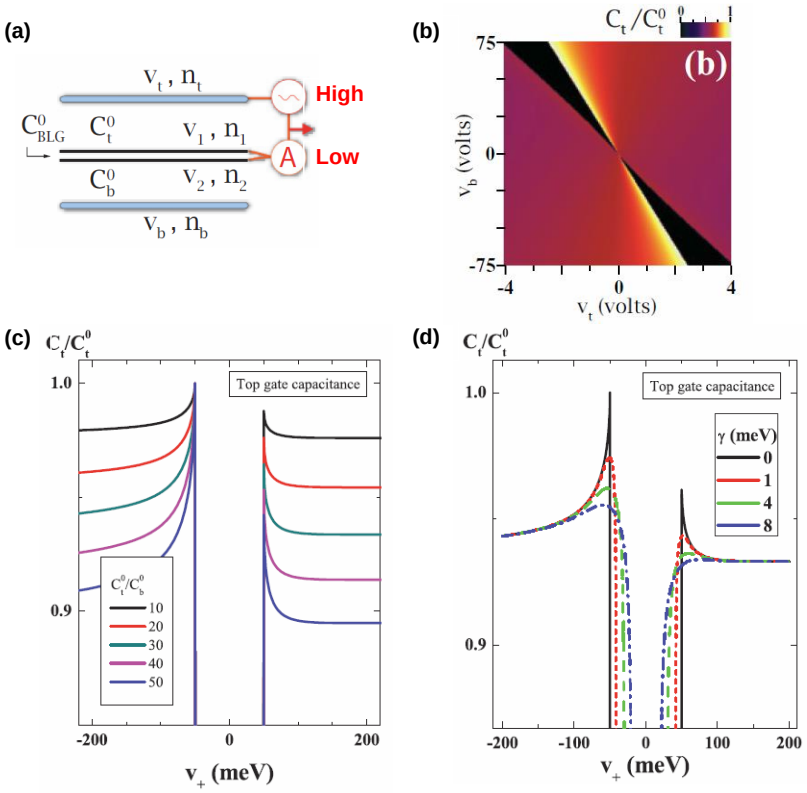

Figure 2.33 (a) Schematics for measurement setup. High & Low are LCR meter terminals.

(b) Measured capacitance as a function of gate voltage. [34]

(c) Asymmetric van Hove singularities. Each color show the ratio between top and back gate capacitances. [34]

Penetration field method [35]

In this method source is grounded, and DC voltages are applied independently on top and back gate. AC voltage signal is applied to back gate and capacitance is measured at top gate electrode (**Fig. 2.34 (a)**). The measured capacitance is given by

$$\frac{1}{C_{bt}} = \frac{1}{C_{bg}} + \frac{1}{C_{tg}} + \frac{1}{C_{bg}}\frac{1}{C_{tg}} e^2 \frac{\partial n}{\partial \mu}.$$

DOS is related to $e^2 \frac{\partial n}{\partial \mu}$. In this method, electric field from AC signal will be screened by electronic compressibility in both graphene layers. Therefore VHSs will be symmetric (**Fig. 2.34 (c)**). Disorder will make band gap appear smaller and smear VHSs like in top gate capacitance method (**Fig. 2.33 (d)**).

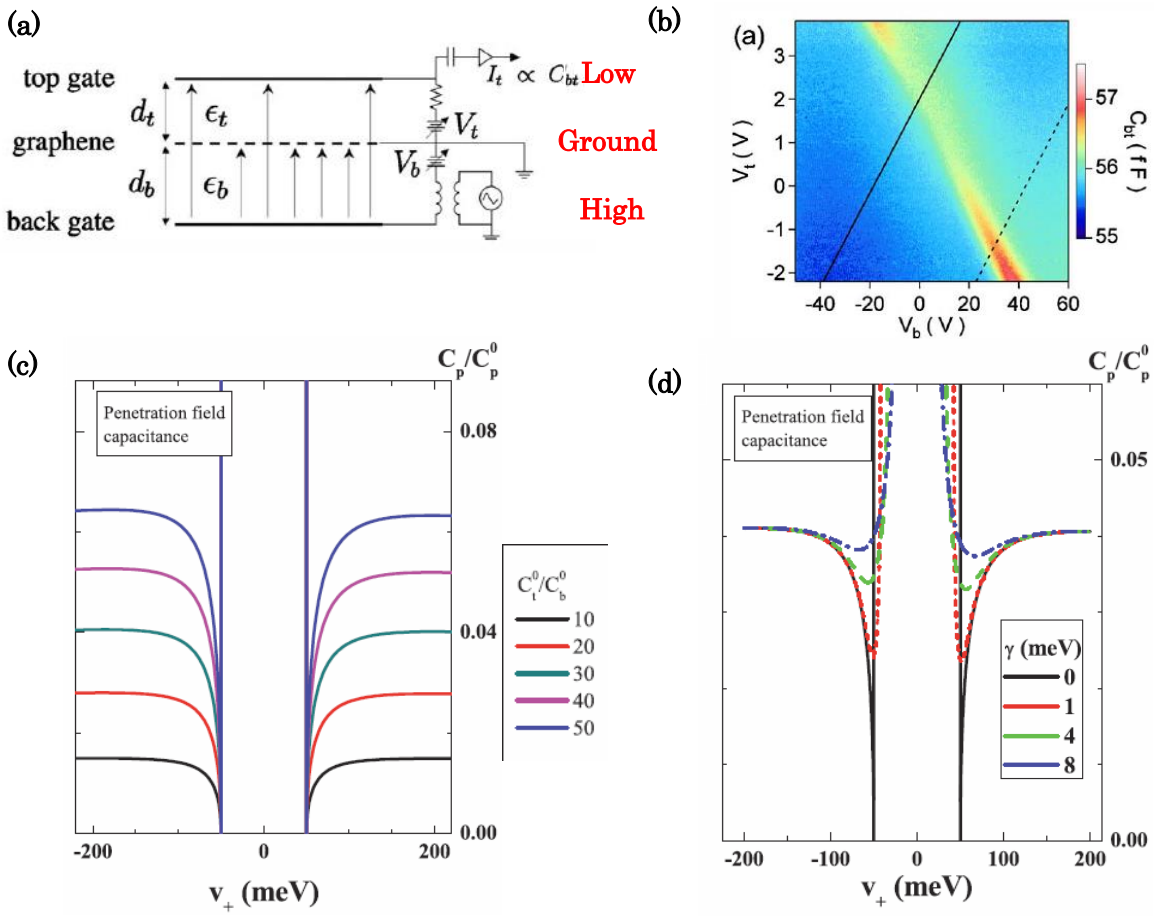

Figure 2.34 (a) Schematics for measurement setup. High & Low are LCR meter terminals.

(b) Measured capacitance as a function of gate voltage. [35]

(c) Asymmetric van Hove singularities. Each color show the ratio between top and back gate capacitances. [34]

(d) Effect of disorder on CV curve. γ denotes disorder energy. [34]

2.5 Conductance method

This method is well-established Si/SiO_2 system, and is widely used to extract interface states density in MOSFET by measuring impedance [36]. When AC signal is applied to quickly Fermi level, the response of trap states is slower than that in the bulk. This trapping and detrapping process can be taken as charging capacitor and the delay can be seen as resistance with phase lagging behind the depletion capacitance of the channel. As a result, frequency dependence of capacitance is observed. The equivalent circuit can be written as shown in **Fig.2.35 (a)**, where C_{TG} is top gate geometric capacitance, C_D is depletion capacitance, C_{it} and R_{it} are capacitance and resistance associated with the interface traps, R_S is series resistance. The equivalent can be converted to parallel capacitance and conductance (**Fig.2.35 (b)**), using the following equations

$$\frac{G_P}{\omega} = \frac{C_{it}}{2\omega\tau_{it}} ln(1 + (\omega\tau_{it})^2)$$

$$C_P = C_D + \frac{C_{it}}{\omega\tau_{it} \tan \omega\tau_{it}}.$$

where $\tau_{it} = R_{it}C_{it}$ is time constant for the trap states. Interface state density (D_{it}) can be calculated from the maximum value of $G\mathrm{p}/\omega$ and the time constant from the frequency of maximum $G\mathrm{p}/\omega$ which gives

$$D_{it} = \frac{(C_{it})_{max}}{q^2} = \frac{1}{0.402q^2}\left(\frac{G_p}{\omega}\right)_{max}$$

$$\tau_{it} = \frac{1.98}{\omega_p} = \frac{1.98}{2\pi f_p}.$$

By measuring impedance at different Fermi energy in band gap, the behavior of D_{it} at various energy levels can be investigated. Potential fluctuations can be evaluated by fitting $G\mathrm{p}/\omega$ as a function of frequency with Gaussian distribution and take the standard deviation as the potential fluctuations. An example of $G\mathrm{p}/\omega$ measured at varying gate voltage in Si/SiO_2 is shown in **Fig. 2.35 (c)**, and previously reported D_{it} in Si/SiO_2 system is shown in **Fig. 2.35 (d)**.

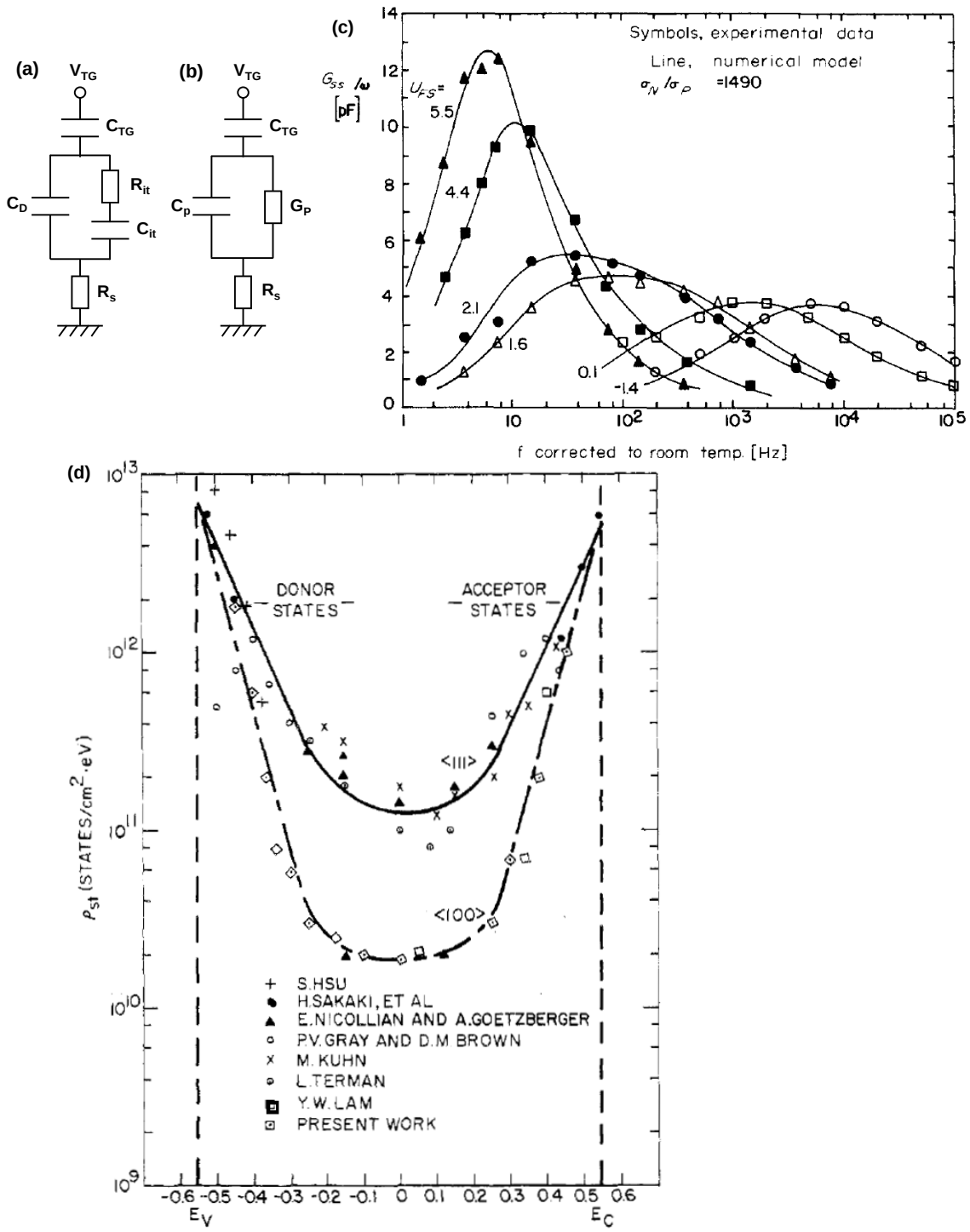

Figure 2.35 (a) Equivalent circuit including the contribution of interface traps in the device.

(b) Converted equivalent circuit.

(c) Gp/ω as functions of frequency for each gate voltage in Si/SiO_2. [37]

(d) D_{it} in Si/SiO_2 as a function of Fermi level. [38]

2.6 High-*k*/2D interface

Because high-k oxide gate stack was first used as gate insulator for BLG and 2D layered materials, electrical property of high-k/2D was investigated. In high-k Y_2O_3/BLG device, D_{it} was measured by conductance method. [15] Frequency dependence of capacitance within band gap region was observed even after removing parasitics from substrate (**Fig.2.36 (a)**). Gp/ω was extracted from impedance measured as a function of frequency while band gap is kept constant (**Fig.2.36 (b)**). As a result, D_{it} of an order of 10^{13} $cm^{-2}eV^{-1}$ and τ_{it} of 4 μs was obtained. The value of D_{it} is two order larger than in Si/SiO_2, suggesting the need for improvement of interface quality. Charge traps in Y_2O_3 and local AB stack breaking were considered as possible origins for D_{it}. However the measured time constants were too fast for charge trapping in Y_2O_3 and the absence of displacement field dependence of D_{it} contradicts with the trend expected for local AB stack breaking, which suggests that D_{it} should decrease at larger displacement field. Therefore, the exact origin of D_{it} was inconclusive.

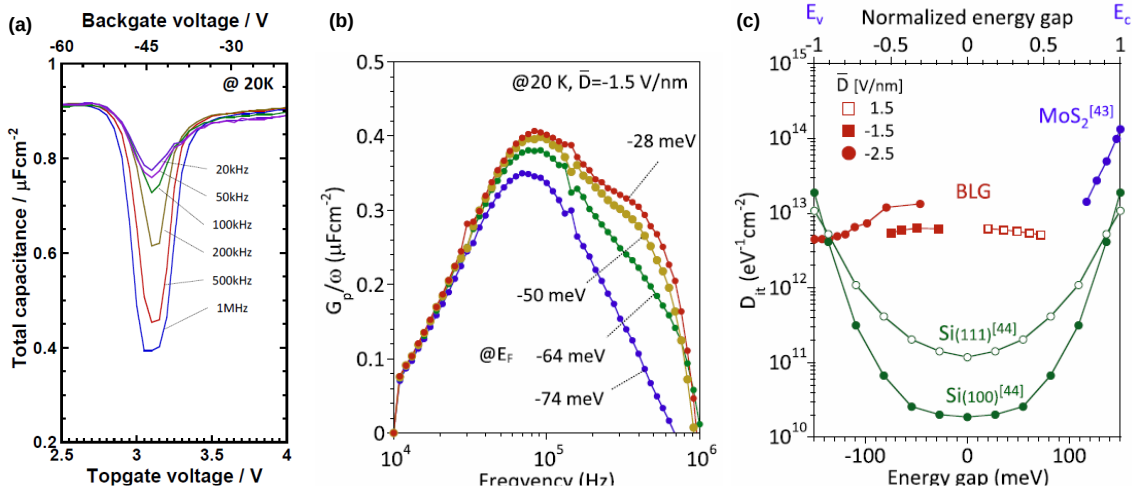

Figure 2.36 (a) Frequency dependence of capacitance. [15]

(b) Gp/ω as functions of frequency for each displacement field. [15]

(c) D_{it} at Y_2O_3/BLG as a function of Fermi level. [15]

In Y_2O_3/MoS_2 D_{it} was investigated from transport measurement, capacitance measurement and conductance measurement. [39] From transport measurement (**Fig.2.37 (a)**), subthreshold swing (SS) can be used to estimate D_{it} from

$$SS = \ln 10 \frac{k_B T}{e} \frac{C_{ox} + C_{it}}{C_{ox}}$$

where C_{ox} is gate capacitance and C_{it} is capacitance related to interface traps. D_{it} was also extracted from capacitance measurement. Frequency dependence of capacitance was observed even in the device with the highest mobility in the study. D_{it} can be extracted from

$$\frac{1}{C_{total}} = \frac{1}{C_{TG}} + \frac{1}{(C_Q + C_{it})}$$

D_{it} extracted from transport measurement and capacitance measurement at 300 K in three different samples are shown in **Fig. 2.37(d)**. Temperature dependence of the relation of C_Q and C_{it} was also observed (**Fig. 2.37 (e)**). D_{it} measured in the study is compared to Si/SiO_2 and the position of D_{it} due to sulfur vacancy. It is suggested that the observed D_{it} was not from sulfur vacancy but from other origin. Mo-S bond bending related to strain at Y_2O_3/MoS_2 or MoS_2/SiO_2 interface was suggested to be the origin.

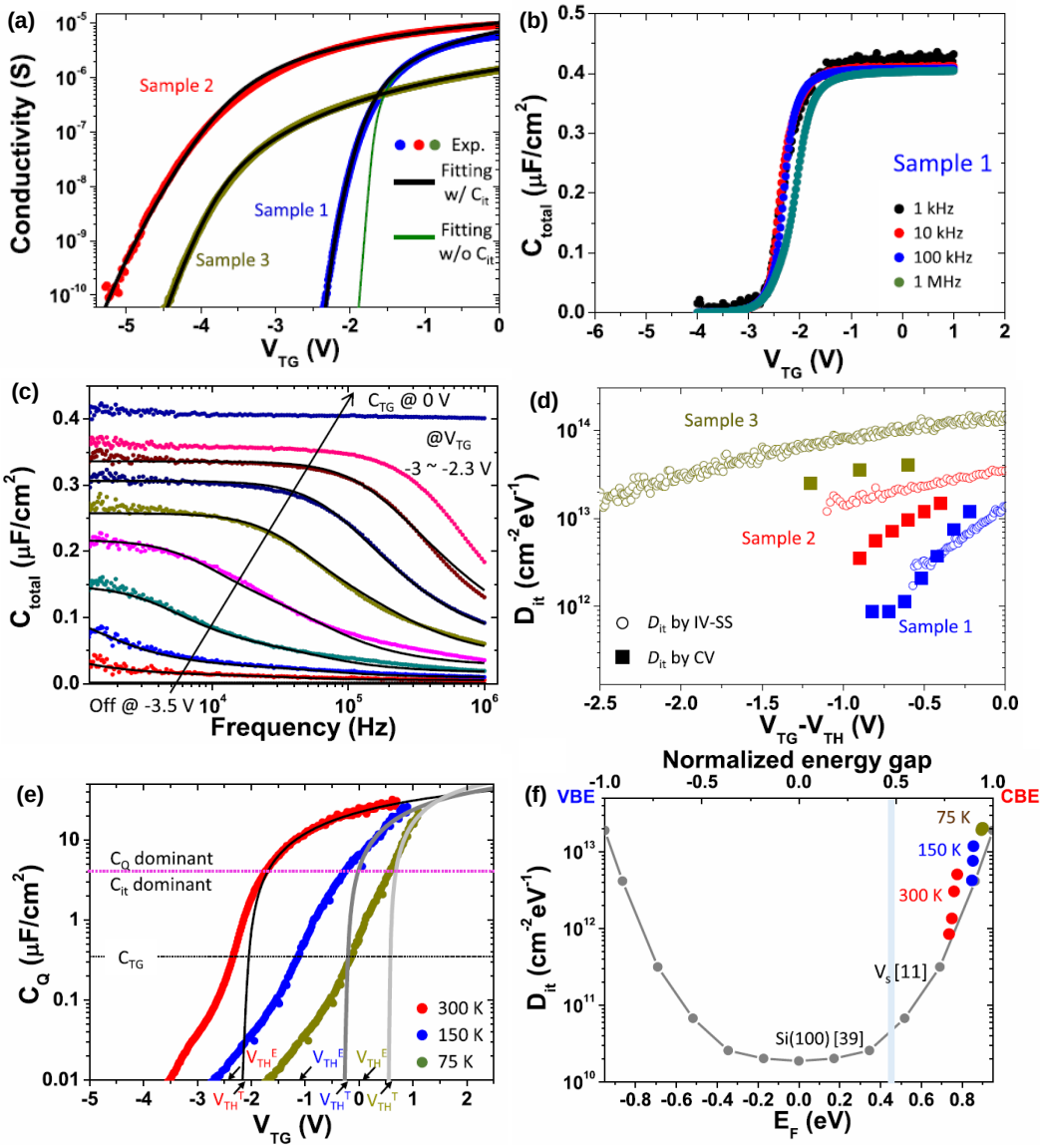

Figure 2.37 (a) Conductivity as function of top gate voltage measured at 300 K. [39]

(b) Total capacitance as a function of top gate voltage for sample 1. [39]

(c) Frequency dependence in **(b)**. [39]

(d) D_{it} extracted from **(a)** and **(b)** as function of gate voltage shift. [39]

(e) Temperature dependence of C_Q. [39]

(f) D_{it} as a function of Fermi energy. [39]

2.7 2D/2D interface

D_{it} at *h*-BN/BLG has not been investigated; it will be investigated in this study. Here, possible origin of D_{it} at *h*-BN/BLG will be discussed.

In graphene, formation energy of a single vacancy is sufficiently high (7.5 eV), that generation of detectable amount of point defects is not allowed at thermal equilibrium below melting point. [40] However, nonequilibrium defects can be generated by crystal growth, irradiation with energetic particles or chemical treatment. The presence of defects can be identified by Raman spectroscopy where defect-related peak at 1350 cm^{-1} (D band) can be seen. Device fabrication process can introduce defects in graphene. If electron beam evaporation or sputtering is used to form contacts, defects may be introduced in channel due to high energy x ray generated from bombardment of target metal. Therefore, in this study metal contacts are formed by thermal evaporation. Defects generation by chemical treatment is unlikely to happen because heterostructure is formed by picking up BLG with *h*-BN and encapsulating with another *h*-BN, protecting BLG channel from chemicals used in device fabrication process. Kish graphite (Covalent material) which is known for high quality and high impurity was used in this study. Therefore defects of BLG is unlikely to be the dominant origin of D_{it}.

In *h*-BN defects originated from carbon impurities were reported. [41] The presence of defects in *h*-BN was shown by scanning tunneling microscopy (STM) measured on monolayer graphene transferred on *h*-BN. Monolayer graphene was used as conductive path for electrical current in measurement to reveal electrical states in *h*-BN. Despite clean interface seen in topological image, defects in *h*-BN were detected as bright and dark dots and ring shape in differential conductance (dI/dV) image (**Fig. 2.38 (a, b)**). The ring shape defects can be manipulated by STM tip voltage (**Fig. 2.38 (c)**), suggesting that this kind of defect is at *h*-BN surface and can trap or emit carriers into graphene. *h*-BN used in this study is confirmed by the provider that carbon impurity is below detection limit. [42] Therefore, carbon impurities should not be the dominant origin of D_{it} in *h*-BN/BLG interface.

During stacking process of 2D heterostructure, adsorbates at 2D crystal surface can be trapped in the heterointerface. Annealing *h*-BN/BLG heterostucture can facilitate the aggregation of trapped adsorbates into bubbles (Ostwald ripening) due to hydrophobic nature of *h*-BN and BLG surface, leaving the interface without bubbles clean. However, identification of bubbles in *h*-BN encapsulated BLG may be difficult because the thickness of top *h*-BN layer (few 10 nm) can be more than bubble height (few nm). The presence of interfacial bubbles can cause strain in BLG and break AB stacking. Disorder in BLG such as AB stack breaking or variation of band gap from charge inhomogeneity can create localized states within band gap and therefore can be considered as possible origin for D_{it} .

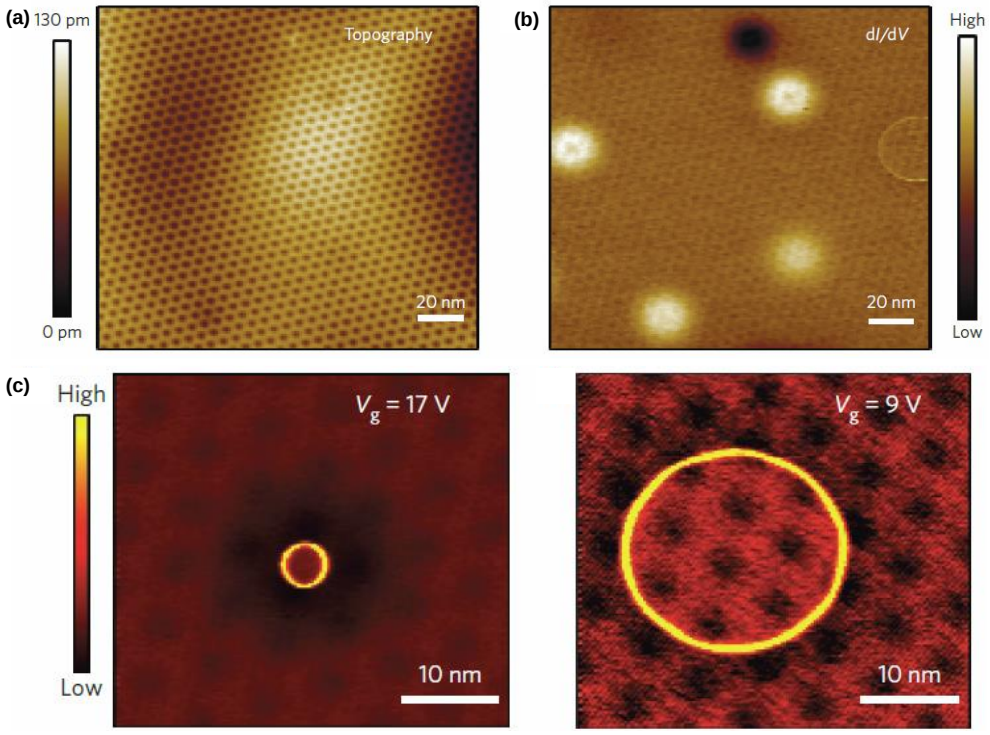

Figure 2.38 (a) Topological image of monolayer graphene on *h*-BN. [41]
(b) Differential conductance image measured in **(a)**. [41]
(c) Manipulation of ring shape defect by STM tip voltage. [41]

2.8 References

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Chapter 3 Photoresponse in bilayer graphene

3.1 Photoresponse mechanisms in graphene

Photovoltaic effect

The first reported photoresponse in graphene was based on photovoltaic effect at graphene/metal contact. [1] Photocurrent image, suggests that doping profile of graphene contacted with metal electrode is solely controlled by the metal, regardless of back gate voltage. This creates potential difference between the region controlled by metal electrode and the channel similar to pn junction, which will separate photogenerated electron-hole pair, giving rise to photocurrent (**Fig. 3.1(a)**). The magnitude of photocurrent is highest at graphene/metal junction. Sweeping gate voltage changes the doping profile of the channel region, therefore changing the potential difference compared to the region controlled by metal electrode. This results in variation of magnitude and direction of photocurrent (**Fig. 3.1 (b, c)**).

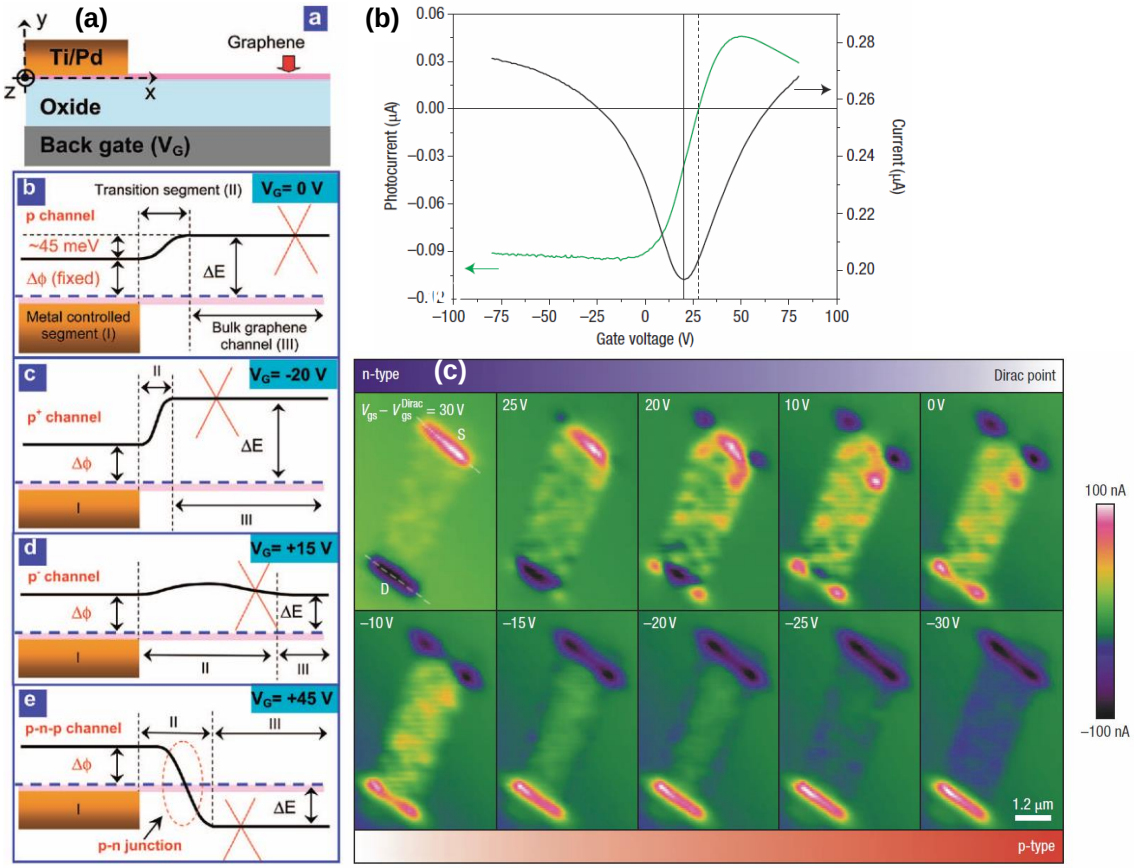

Figure 3.1 (a) Mechanism of photovoltaic effect at graphene/metal contact. [2]

(b) AFM image of a graphene device. [1]

(c) Photocurrent image of **(b)**. [1]

(d) Photocurrent image for each back gate voltage. [1]

Photothermoelectric effect

Photothermoelectric effect occurs when temperature gradient is present. The difference in temperature induces difference in electron energy, resulting in electromotive force. Photothermoelectric effect was observed at pn junction in monolayer graphene as well as bilayer graphene. The observed photocurrent is a magnitude larger than the photocurrent from photovoltaic effect at metal contacts. This was suggested from the sign change of photocurrent across each back gate and top gate voltages. The photocurrent sign change resembled the photocurrent from photothermoelectric effect more than that of photovoltaic effect, suggesting that photothermoelectric effect dominates the photoresponse in the device. [3]

Photothermoelectric effect was also observed in monolayer graphene/bilayer graphene boundary. Because of their difference in DOS, for the same carrier density, Fermi level in monolayer graphene will be above that of the bilayer graphene, resulting in built-in potential difference when Fermi level is aligned. For photovoltaic effect, photoexcited electron is expected to flow from bilayer graphene to monolayer graphene. On the other hand, for photothermoelectric effect, electron would flow to the material with larger DOS, which is the opposite for photovoltaic effect in this device. The sign of photocurrent suggests that photothermoelectric effect is dominant in this device. [4]

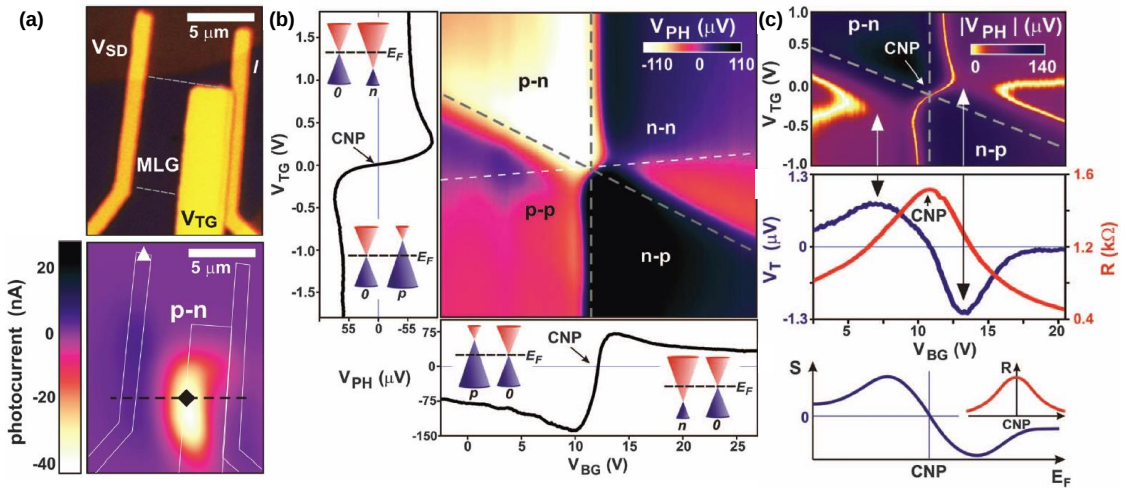

Figure 3.2 (a) Optical image and photocurrent image for graphene device. [3]

(b) Contour plot of photovoltage at each gate voltage [3]. Line cuts are measured along gray lines. [3]

(c) Photovoltage sign change compared to Seebeck coefficient. [3]

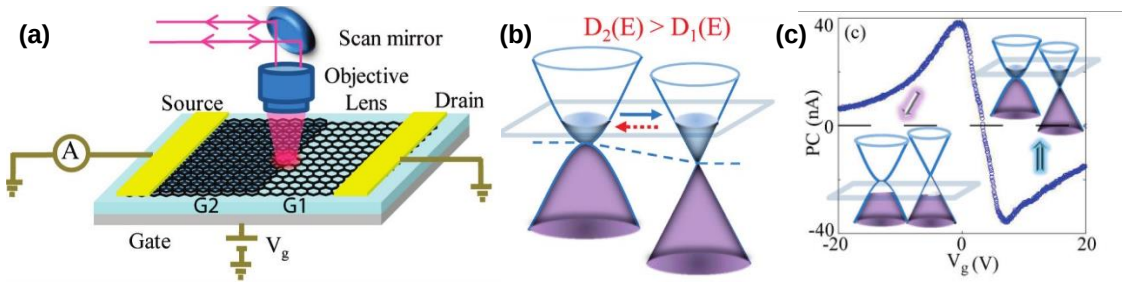

Figure 3.3 (a) Measurement setup. [4]

(b) Band diagram of the device. Blue and red arrow shows photovoltaic and photothermoelectric current, respectively. [4]

(c) Photocurrent as a function of back gate voltage. [4]

Bolometric effect

Bolometric effect is the change of resistance of a material due to temperature increase after absorbing the incident light. Bolometric effect was observed in gapped bilayer graphene. [5] Pronounce photovoltage was observed around charge neutrality (**Fig. 3.4 (a, b)**). The dominant mechanism was determined by comparing photovoltage results to other parameters. If the photoconduction is dominant, photovoltage will be proportional to R^2 (R is resistivity) and carrier density. However, as shown in **Fig. 3.4 (c)**, photovoltage seem to increase faster than R^2 as displacement field is increased, and at increased carrier density (**Fig. 3.4 (b)**) suggesting that other mechanism is dominant. On the other hand, response by electrical heating was found to be the same magnitude as optical response, suggesting that the photoresponse is dominated by bolometric effect, with optical energy lost first to hot electrons and then to acoustic phonons (**Fig. 3.4 (d)**). The photoresponse diminished greatly as temperature is increased and vanished beyond 40 K.

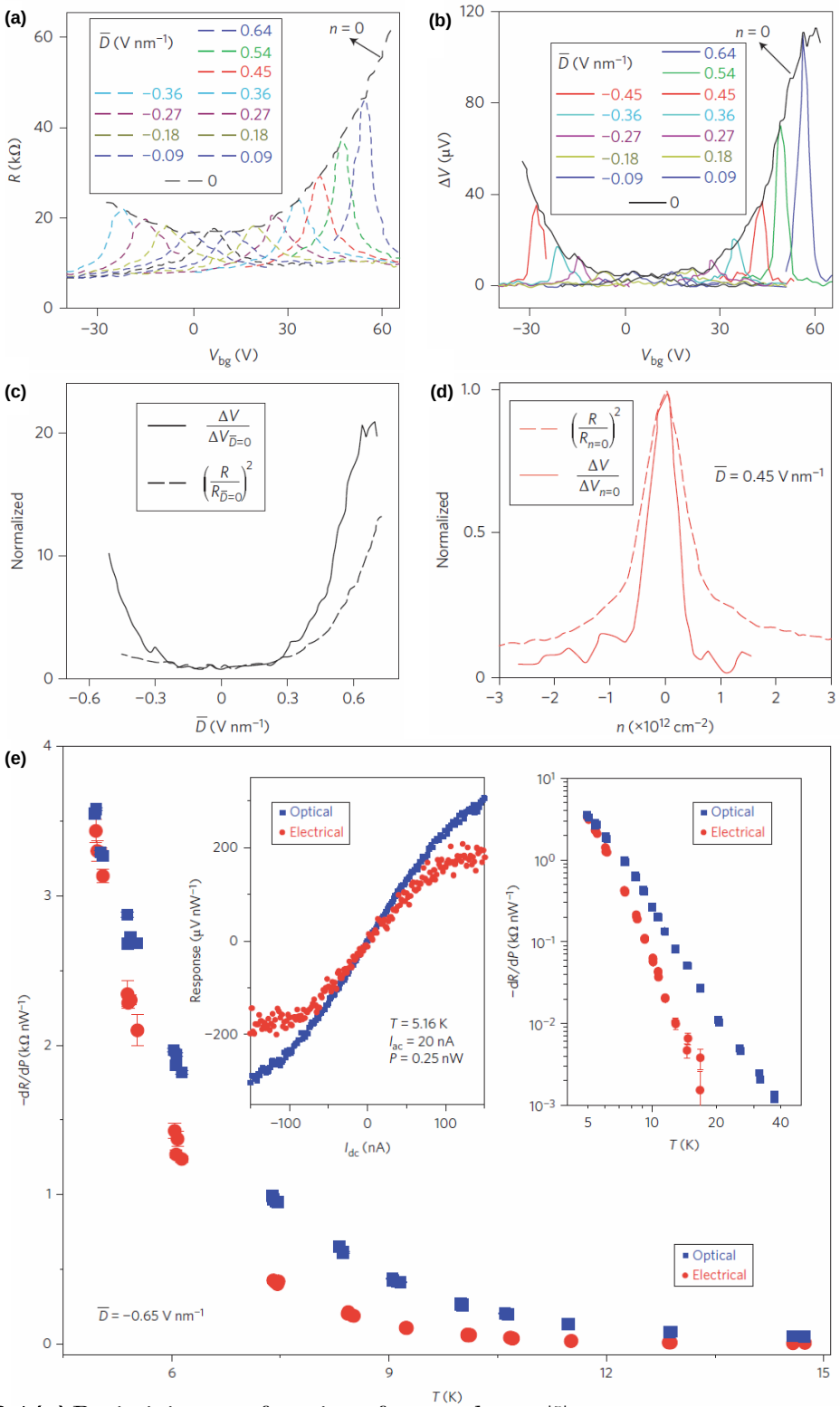

Figure 3.4 (a) Resistivity as a function of gate voltage. [5]

(b) Photoresponse as a function of gate voltage. [5]

(c) Normalized photovoltage and resestance at charge neutrality as a function of displacement field. [5]

(d) Normalized photovoltage and resestance as a function of carrier density. [5]

(d) Comparison of photoresponse and electrical heating at charge neutrality point. Left inset: photoresponse as a function of DC current. The slope near zero DC current in left inset is plotted in the main panel. Right inset: data of main panel in log scale. [5]

3.2 Fourier transform photocurrent spectroscopy

Excitons were observed in gapped bilayer graphene by Fourier transform photocurrent spectroscopy (FTPS). [6] In this method, infrared light from polychromatic source is directed into Michelson interferometer, creating optical path difference and then focused onto sample. Photocurrent is obtained by Fourier transform of the measured signal (**Fig. 3.5 (a)**). This is equivalent to using the device as a detector in Fourier transform infrared spectroscopy. Two photocurrent peaks were observed at energies lower than the band gap which gives continuous smooth absorption. Interestingly the position of two peaks shifted as displacement field was increased (**Fig. 3.5 (c)**). The possibility of the origin being van Hove singularity was eliminated because it could not explain the first peak, and the second peak was much sharper than the predicted peak from van Hove singularity. The possibility of impurity-originated absorption was eliminated by measuring doping dependent absorption spectrum, finding that the peaks were robust against doping. Therefore, the two peaks were associated with optical transition to exciton 1s and 2p state, respectively.

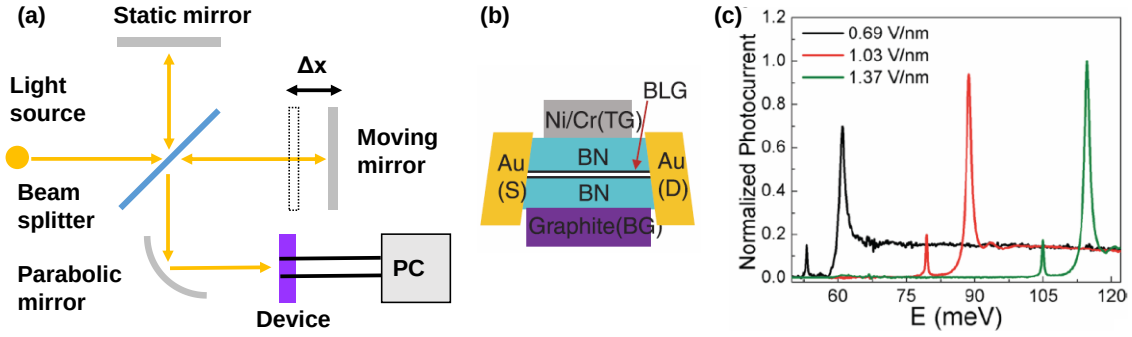

Figure 3.5 (a) Schematics for Fourier transform photocurrent spectroscopy. [6]
(b) Device structure. [6]
(c) Normalized photocurrent spectra. [6]

3.3 Photoresponse in 2D materials

Here, photodetectors based on two-dimensional layered materials will be introduced. Their performance and mechanisms will be discussed. As shown in **Fig. 3.6 (a)**, most of two-dimensional layered materials have energy gap that corresponds to the range of near infrared to visible light. For black phosphorus, band gap can be tuned down to mid infrared. Responsivity and response time are compared in **Fig. 3.6 (b)**. The responsivity and response commercial InGaAs and Si photodetectors are also plotted. It can be seen that transition metal dichalchogenides show higher responsivity but slower response time than graphene and black phosphorus. The fast response time for graphene in this figure is based on photovoltaic effect at graphene metal contacts. [7, 8] The response of

black phosphorus is that of a device with black phosphorus laid over Si waveguide. [9] The responsivity and response time seem to be inversely proportional. This issue will be discussed along with introducing factors that can affect photorespone in two-dimensional layered materials.

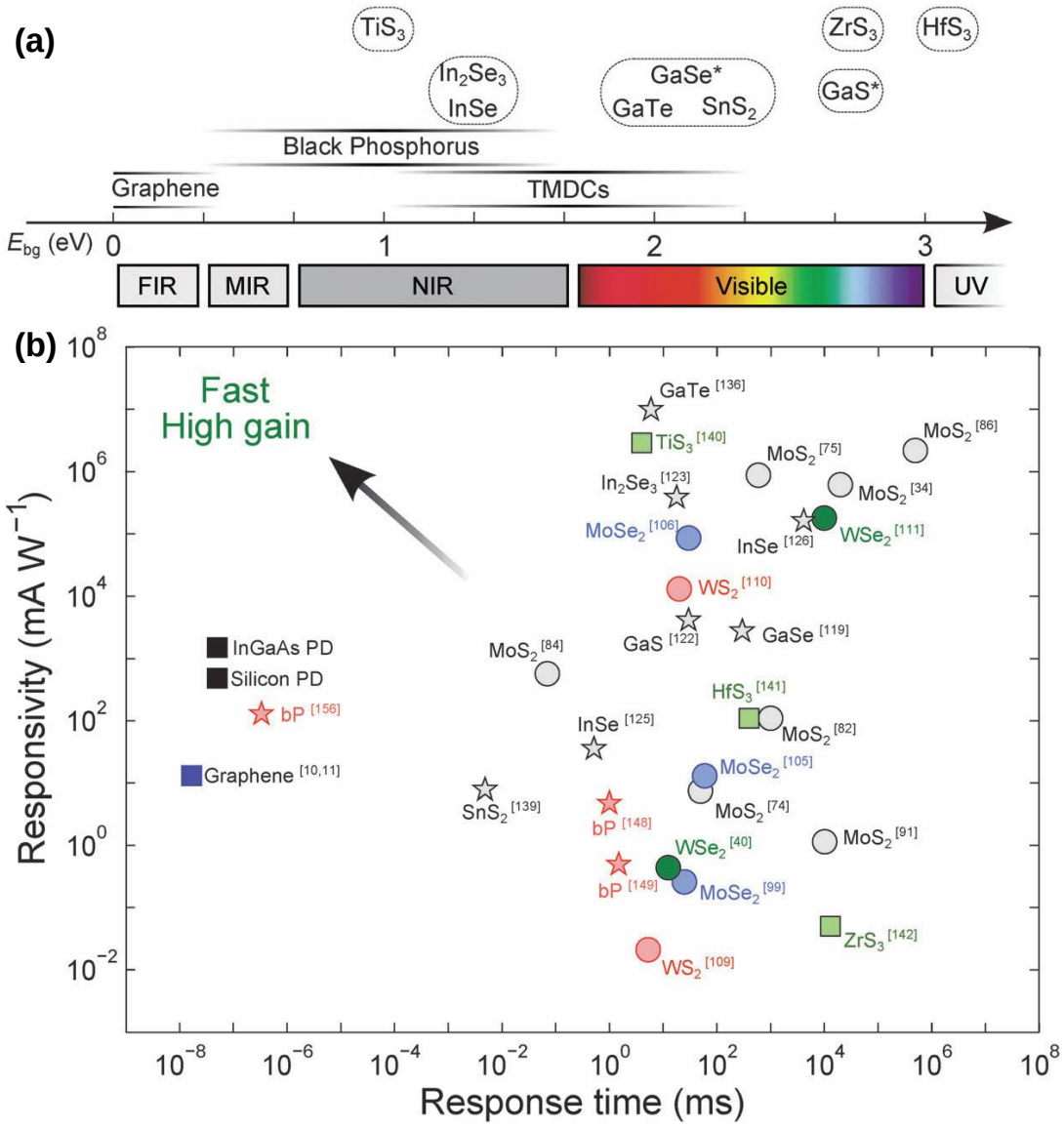

Figure 3.6 (a) Band gap and corresponding photon energy range. [10]
(b) Responsivity and response time. [10]

Photoconductive effect

The first reported photoresponse in single layer MoS_2 FET was observed with gate voltage dependence. [11] It was associated with Shcottky barrier modulation at contacts by gate voltage, as shown in **Fig. 3.7**. It is considered that barrier becomes smaller at positive gate voltage due to Fermi level alignment of the channel with regard to the contact, allowing more photocarriers to reach drain electrode. The device shows response

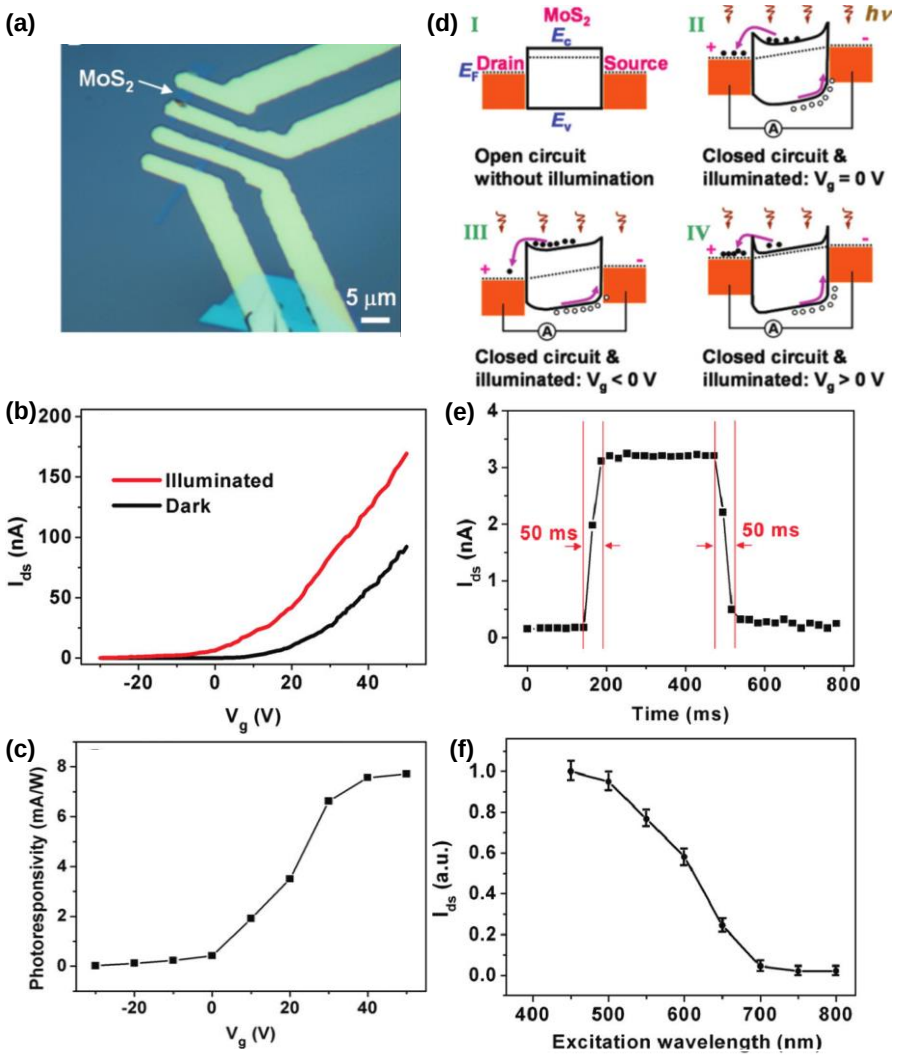

Figure 3.7 (a) Optical image of MoS_2 FET. [11]

(b) Drain current as a function of gate voltage. [11]

(c) Responsivity in **(b)**. [11]

(d) Schematics for gate voltage dependence in responsivity. [11]

(e) Time response. [11]

(f) Photocurrent spectrum. [11]

time of ~50 ms. The cut-off excitation wavelength is ~670 nm which corresponds to single layer MoS_2 band gap energy of 1.8 eV.

Photogating effect

Incident light modulation frequency dependence in photoresponse was observed in monolayer MoS_2. [12] When incident light was modulated by chopper, strong background photocurrent and a much smaller photocurrent component which oscillates similarly to modulation frequency, as shown in inset of **Fig. 3.8 (a)**. The fast component was attributed to photoconduction and the slow component was attributed to photogating effect. Photogating effect occurs when one type of photocarrier is trapped in the channel. The trap carriers act as local gate, altering the behavior of gate by inducing additional

carriers in the channel or screening the gate electric field. In this device, holes are trapped and therefore should induce additional electrons, giving positive photocurrent. Photoconductive response in presence of traps was calculated based on model shown in **Fig. 3.8 (b, c).** In this situation, Fermi energy is slightly below the conduction band edge, so band tail states at valence band edge can act as hole traps and mid-gap states can act as recombination sites. The experimental data in **Fig. 3.8 (d)** can be fitted with this model. The decrease of photocurrent in negative gate voltage seen in **Fig. 3.8 (e)** can be explained as the result of additional electron trapping by band tail states at conduction band when Fermi energy is around mid-gap. It should be noted that the device in **Fig. 3.7** and **Fig. 3.8** have the same Ti (5 nm)/Au (50 nm) contacts but their origins of gate voltage dependence for photocurrent were explained differently.

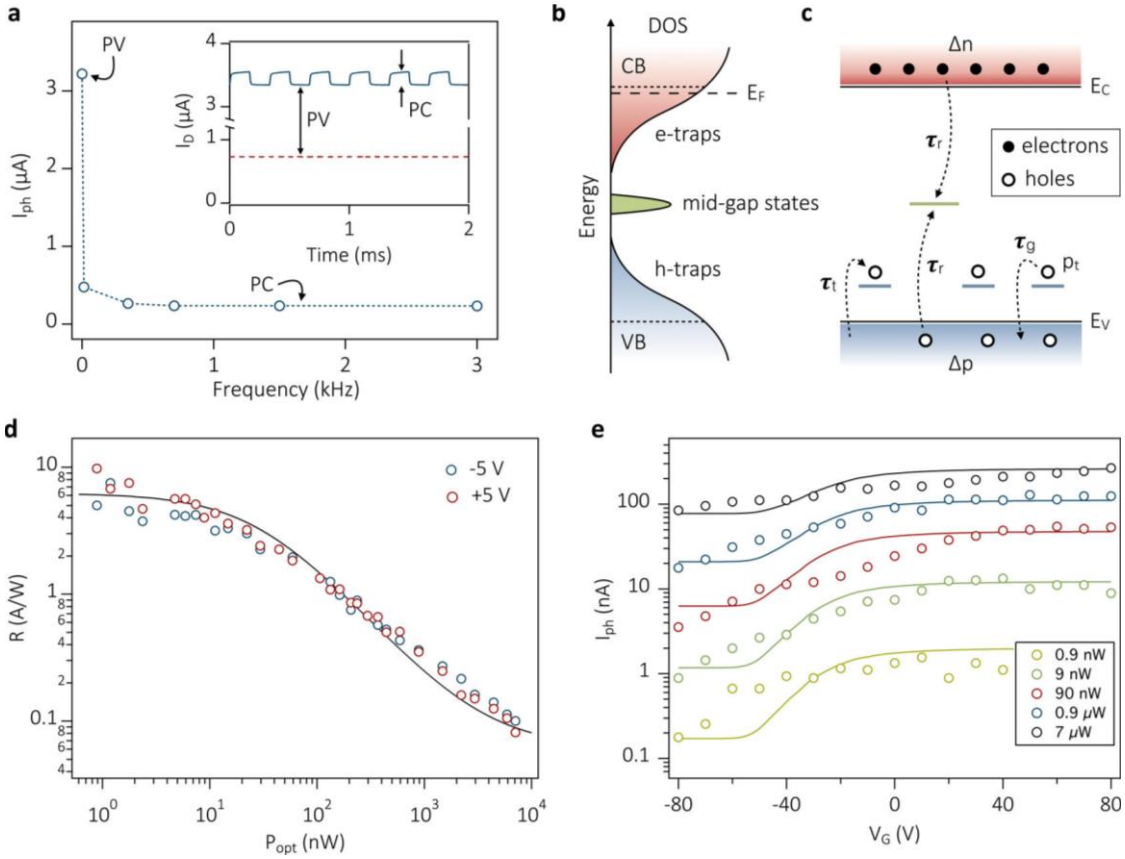

Figure 3.8 (a) Photocurrent as a function of light modulation frequency. [12] Inset is time response.

(b) Density of states used in photoresponse calculation. [12]

(c) Band diagram of traps. [12]

(d) Responsivity as a function of optical power. [12]

(e) Photocurrent as a function of gate voltage. [12]

Photovoltaic effect

Photocurrent in photovoltaic effect is generated separating photocarriers by built-in voltage, unlike photoconductive effect where drain bias is applied to separate photocarriers. Built-in voltage can be created by various methods which will be introduced here. Different contact metals can be used to obtain photovoltaic effect in MoS_2. [13] Using difference in work function of Pd and Au, Schottky barriers of different height were formed at the contacts, resulting in photocurrent generation without having to apply drain voltage, i.e. built-in potential, as shown in **Fig. 3.9**.

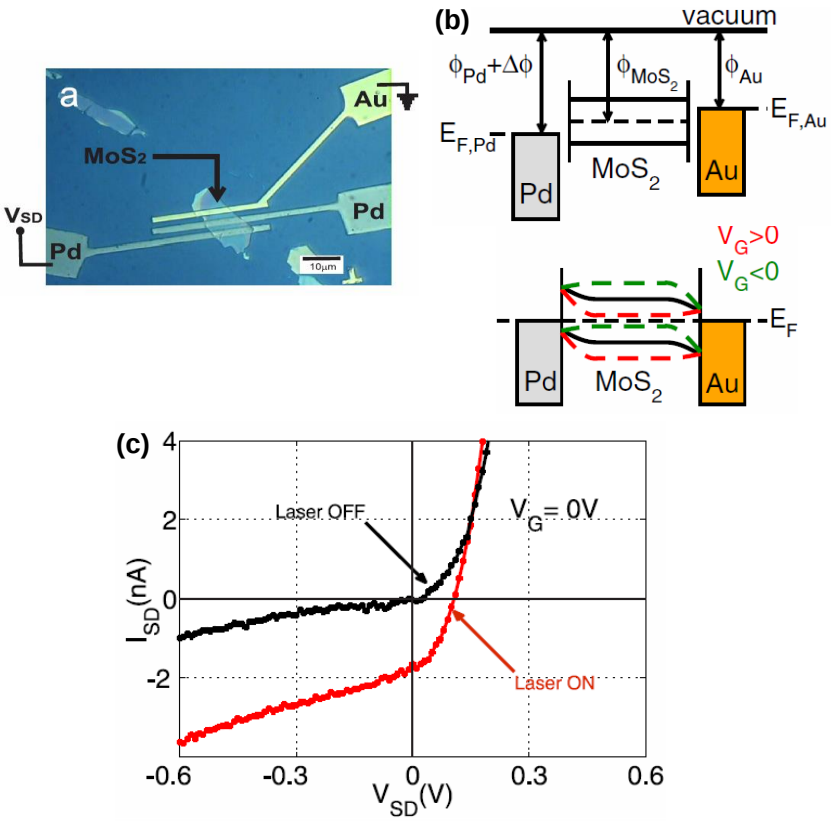

Figure 3.9 (a) MoS_2 FET with Au and Pd contacts. [13]

(b) Band diagram. [13]

(c) Drain current as a function of drain voltage. [13]

Electrostatically defined pn junctions can be used for built-in voltage in WSe_2. [14] Two separate local gates were used to create pn junction, resulting in photovoltaic response, as shown in **Fig. 3.10**. Photoresponse in photoconductive mode and photovoltaic mode were compared. Photoconductive mode shows the same time response but higher photocurrent. The device also exhibits photothermoelectric response when temperature gradient was introduced by using temperature change from absorption in thick flakes, as shown in **Fig. 3.10 (d, e)**.

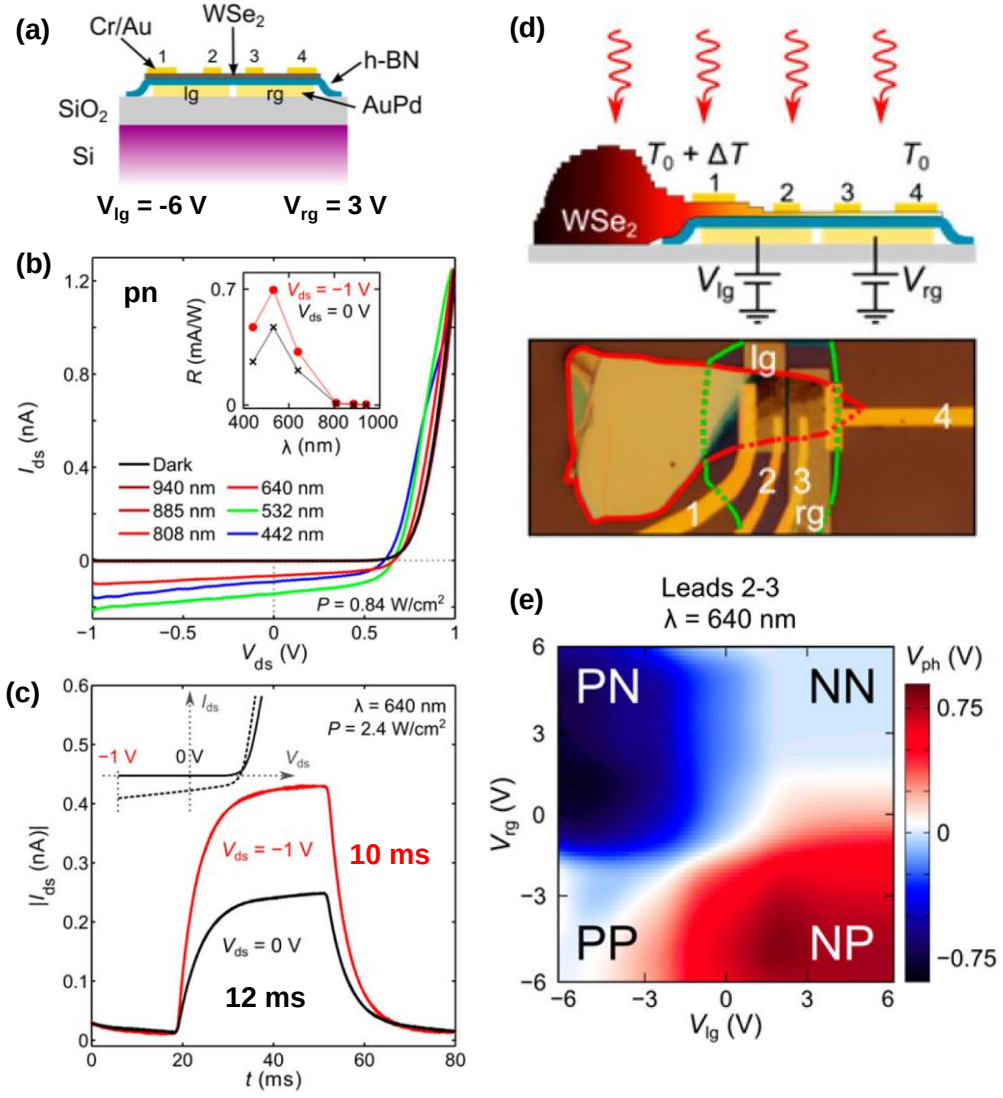

Figure 3.10 (a) WSe_2 FET with two local gates. [14]

(b) Drain current as a function of drain voltage. [14]

(c) Time response. [14]

(d) Schematic for temperature gradient. [14] The part with thick flakes can absorb more light, giving higher temperature than other parts.

(e) Photovoltage as a function of left and right local gate voltage. [14]

Vertical pn junction can be formed by van der Waals heterostructure. Photovoltaic effect was observed in *h*-BN/graphene/WS_2/graphene/*h*-BN. [15] In such device, graphene is used as transparent electrodes and can increase charge separation efficiency due to high mobility (**Fig. 3.11 (a-c)**). Photocarriers can be separated by applying gate voltage (**Fig. 3.11 (d)**) or asymmetric doping of graphene electrodes (**Fig. 3.11 (e)**).

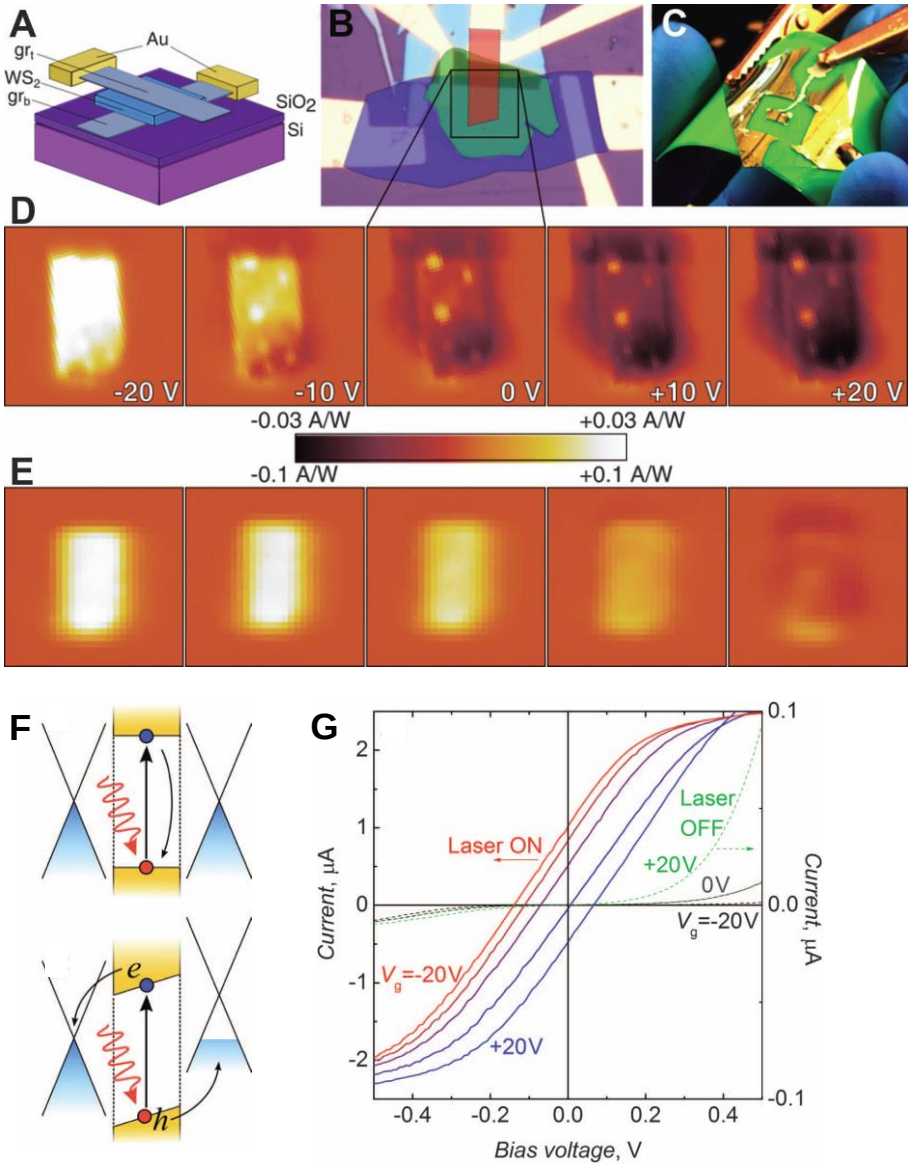

Figure 3.11 (a) Schematic of WS_2 sandwiched between graphene. [15]

(b), (c) Optical image of the device. [15]

(d) Photocurrent mapping as a function of gate voltage. [15]

(e) Photocurrent mapping as a function of gate voltage after doping the top graphene layer with water. [15]

(f) Band structure for carrier separation. [15]

(g) Current as a function of bias voltage. [15]

Photovoltaic effect was observed in vertical hetero pn junction made of MoS_2/WSe_2. [13] Rectification and gate tunable photovoltaic effect was observed (**Fig. 3.12**). Moreover, exciton quenching at the junction was also observed, proving charge transfer at the junction.

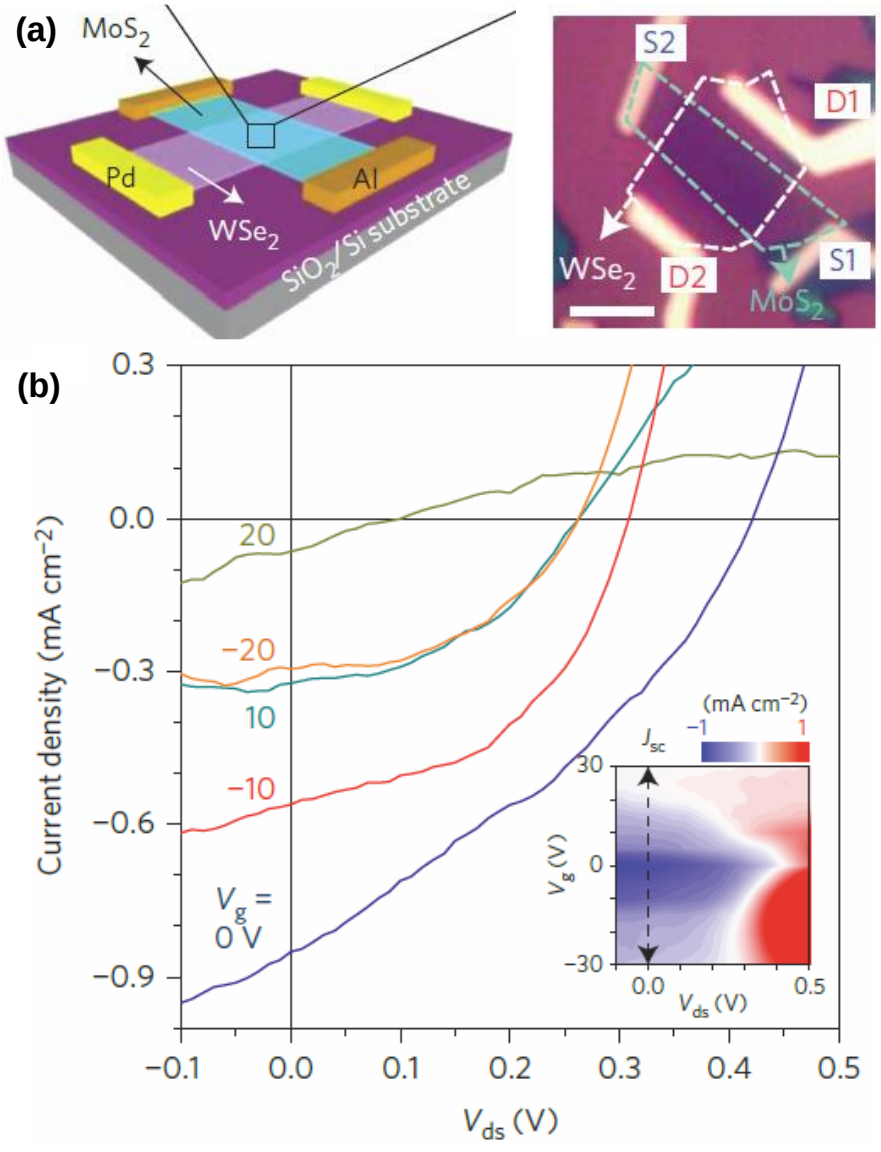

Figure 3.12 (a) MoS_2/WSe_2 vertical heterostructure. [16]

(b) Rectification properties of pn junction. [16] Inset is color plot of current as a function of gate voltage and drain voltage.

Photothermoelectric effect

Other than at pn junction with temperature gradient, photothermoelectric effect was observed around MoS_2/metal contact. [17] Unlike other cases where photothermoelectric response can only be detected when laser spot is at pn junction, photoresponse can be observed even when laser spot is focused on metal area (**Fig. 3.13 (a)**). Because no gate voltage dependence in the peak position of photoresponse was observed (**Fig. 3.13 (c)**), it was proposed that photothermoelectric effect is the dominant mechanism, not photovoltaic effect at Schottky contact where peak position of photoresponse is expected to shift with gate voltage change (**Fig. 3.13 (d)**).

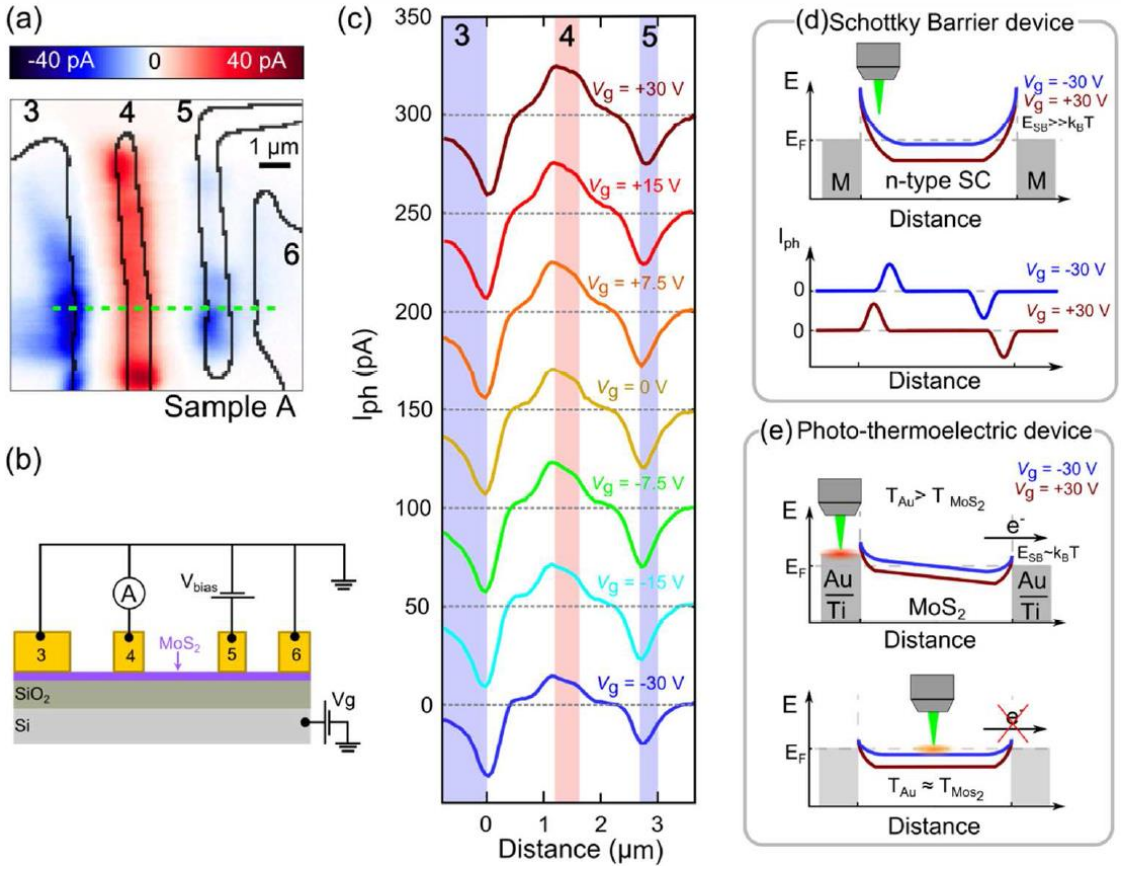

Figure 3.13 (a) Photocurrent mapping. [17] Electrodes are outlined by black lines.

(b) Schematic of electrode positions. [17]

(c) Line scan of along green dotted line in **(a)**. [17]

(d) Gate dependence in photocurrent peak position for photovoltaic effect. [17]

(e) Photothermoelectric effect at Schottky junction. [17]

Phototransistor action

A larger photocurrent was observed in MoS_2 FET with local back gate compared to in global back gate device. [18] This was associated with similar mechanism of phototransistor action in bipolar transistor. In such device, local back gate is in the middle of the channel, as shown in **Fig. 3.14 (a)**. Drain bias dependence of photocurrent is shown in **Fig. 3.14 (b)**. For global back gate devices, the photocurrent would be linearly proportional to drain bias. Although, non-linearity of drain bias dependence of photocurrent may be observed in devices with sufficiently high Schottky barrier at

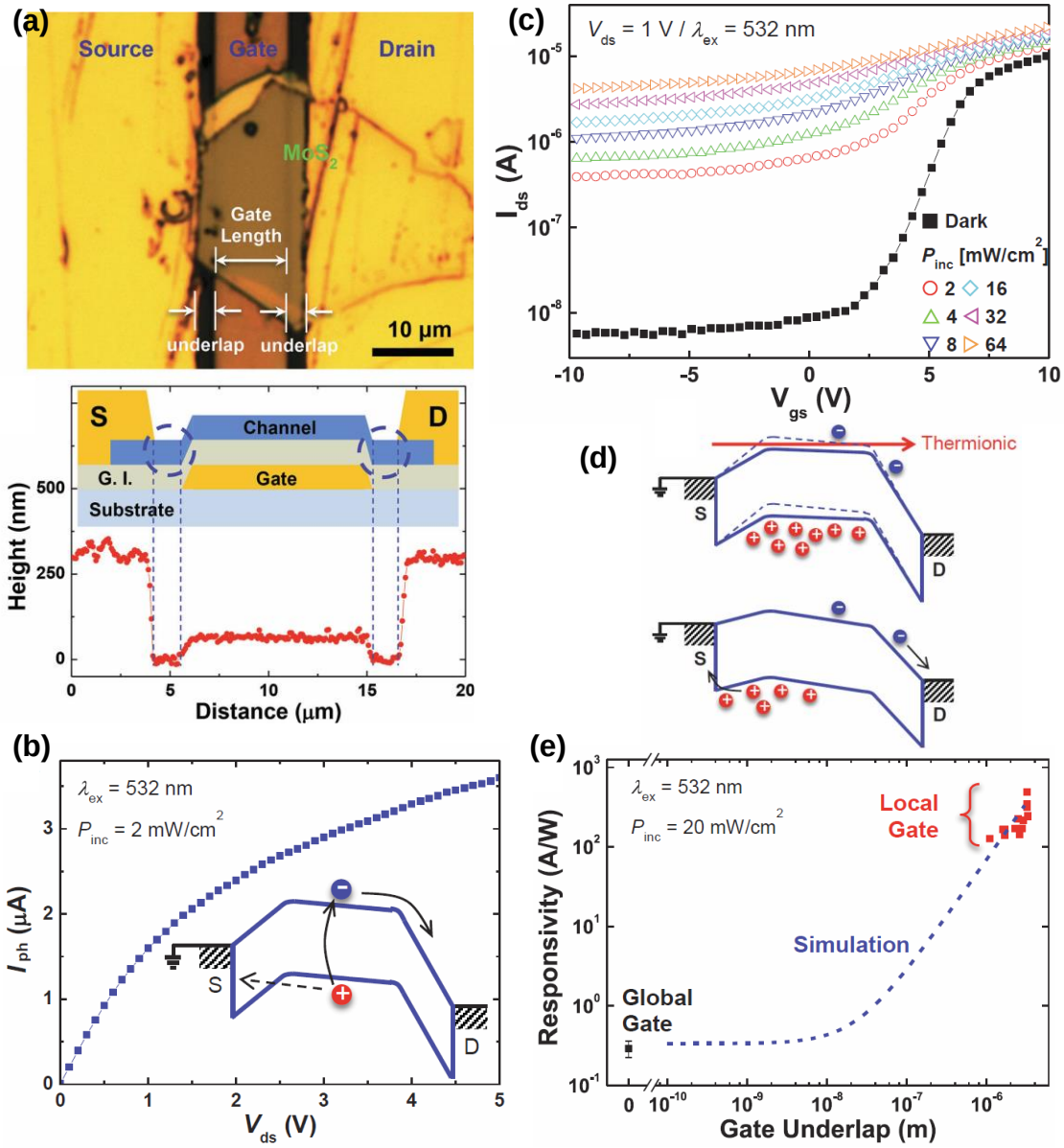

Figure 3.14 (a) Optical image and height profile of MoS_2 FET with local gate. [18]

(b) Drain voltage dependence of photocurrent. [18]

(c) Drain current as a function of gate voltage. [18]

(d) Band structure for current amplification in MoS_2 FET with gate underlap. [18]

(e) Gate underlap dependence of responsivity. [18]

contacts, Schottky barrier at the contacts this device was estimated from the saturation of on-current to be ~10 meV, therefore its effect on photoresponse was neglected. The non-linearity of drain bias dependence of photocurrent suggested a different mechanism. A band structure with potential barrier as a result of local gate similar to phototransistor was proposed. Increasing drain bias results in only more photogenerated electrons flow across the channel but not holes, because photogenerated holes accumulate within the potential barrier, as shown in inset of **Fig. 3.14 (b)**. Gate bias dependence of photocurrent was investigated. Larger photocurrent was observed at higher gate voltage (**Fig. 3.14 (c)**). Using the proposed model, it was described as positive gate voltage modulate Fermi level in gated region, lowering the potential barrier for hole, which allows more holes to reach source electrode, increasing the total photocurrent (**Fig. 3.14 (d)**). The effect of local gate length on responsivity was also investigated (**Fig. 3.14 (e)**). Higher responsivity was observed in devices with gate underlap compared to global back gate devices. This suggests current amplification by hole accumulation within potential barrier at gate underlap region shown in **Fig. 3.14 (d)**. It should be noted that gate underlap in this experiment is 10 μm which is much longer than diffusion length in MoS_2 (~450 nm [19]), contradicting with the principle of current amplification in bipolar phototransistor. It is possible that the observed increase in photocurrent is the result of increased photoconductive gain. In photoconductive effect, if one type of carrier has much longer transit time than the other type of carrier, the faster moving carrier will reach electrode first, breaking the charge neutrality of the channel. This will cause additional faster moving carriers to be injected into the channel, increasing the total current, giving current gain. In photovoltaic effect one pair of photogenerated carriers are separated and gives only one unit of photocurrent, but in photoconductive effect one pair of photogenerated carriers can give more than one unit photocurrent, based on the difference in transit time explained above. It is possible that hole accumulation within potential barrier causes transit time of holes to be much longer than electrons, thus giving current gain which results in larger photocurrent observed.

3.4 Photoresponse in carbon nanotubes

Carbon nanotubes (CNTs) were discovered about ten years before graphene, and their photoresponse have been rigorously investigated. Being closely related to graphene, their photoresponse mechanisms should give useful insights for considering photoresponse in bilayer graphene in this study. CNT band structure is composed of subbands which have different angular momenta. As a result, optical transition in CNT obeys selection rules, i.e. optical absorption can vary based on wavelength and polarization of light with respect to CNT axis (**Fig. 3.15**). Another important issue in photoresponse in CNT is exciton binding energy. Due to quasi-one-dimensional confinement, Coulomb interaction is enhanced, leading to significant exciton binding energy (~0.4 eV [20]) which dominates optical absorption from visible to mid-infrared. Therefore, sufficiently large electric field is required for separating dissociating excitons in photovoltaic effect and photoconductive effect. Apart from the issues mentioned, the behaviors of photoresponse mechanisms experimentally observed in individual CNT are generally similar to graphene. The detectivity and wavelength are summarized in **Fig. 3.16**. It can be seen that the order of highest detectivity is from photovoltaic effect, photoconductive effect, bolometric effect, and photothermoelectric effect, respectively. Here, photoresponse in individual semiconducting single-walled CNT will be introduced.

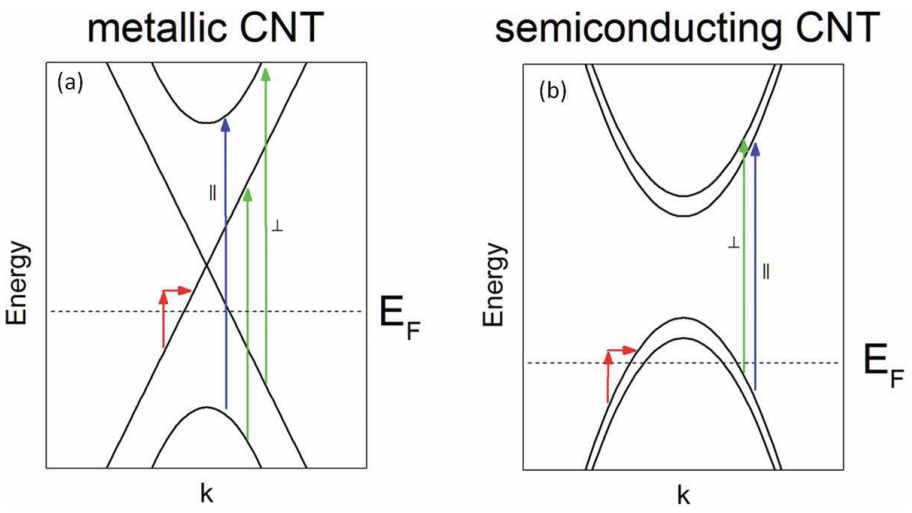

Figure 3.15 Band structure and optical transition in CNT. [21] Blue and green arrows are optical transitions for light parallel and perpendicular to CNT axis, respectively. Red arrows are intraband transitions for doped CNT.

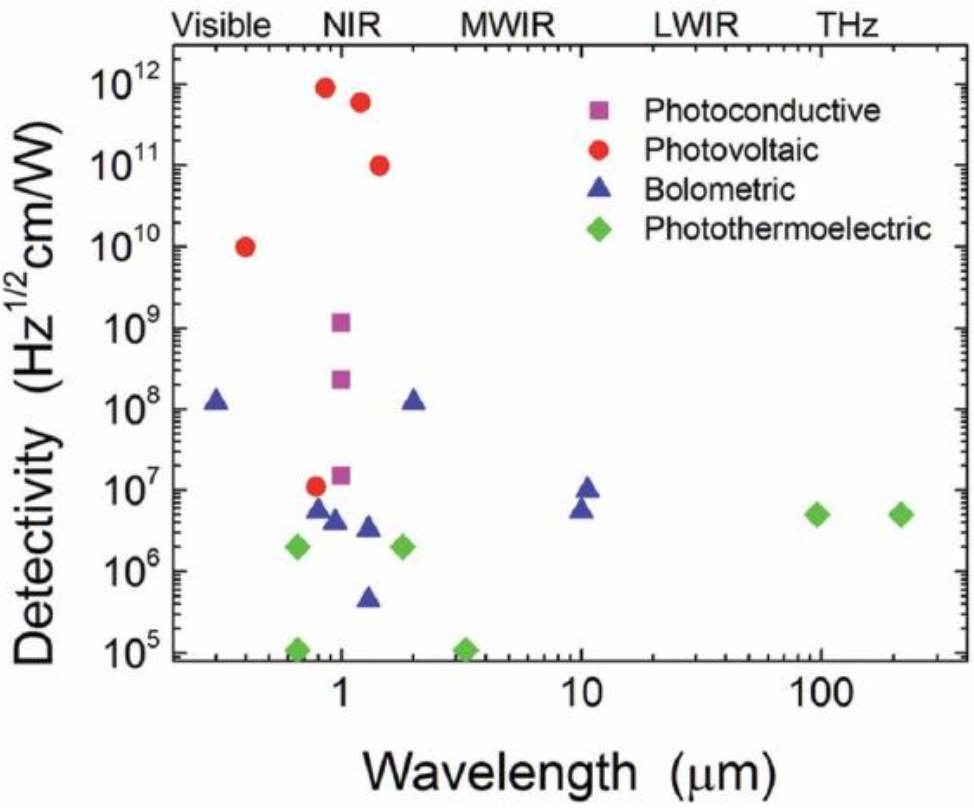

Figure 3.16 Room temperature detectivity and wavelength for CNT operating with different photoresponse mechanisms. [21]

Photoconductive effect

One of the first reported photoresponse in CNTs is based on photoconductive effect. [22] Semiconducting CNTs with band gap of ~0.7 eV were dispersed from dichloroethane suspension on p^+-Si/SiO_2 substrate which is used as back gate, and source drain contacts were formed by Ti (**Fig. 3.17 (a)**). Drain voltage of 1 V was applied on the device to separate photogenreated carriers. Upon infrared laser irradiation an increase in drain current of an order of magnitude and a shift of 600 mV in IV curve was observed (**Fig. 3.17 (b)**). Light polarization angle dependence of photocurrent was observed (**Fig. 3.17 (c)**). The maximum photocurrent was obtained when light was polarized in the direction of CNT axis. Linear dependence of photocurrent to light intensity implies the photoconductive effect (**Fig. 3.17 (d)**).

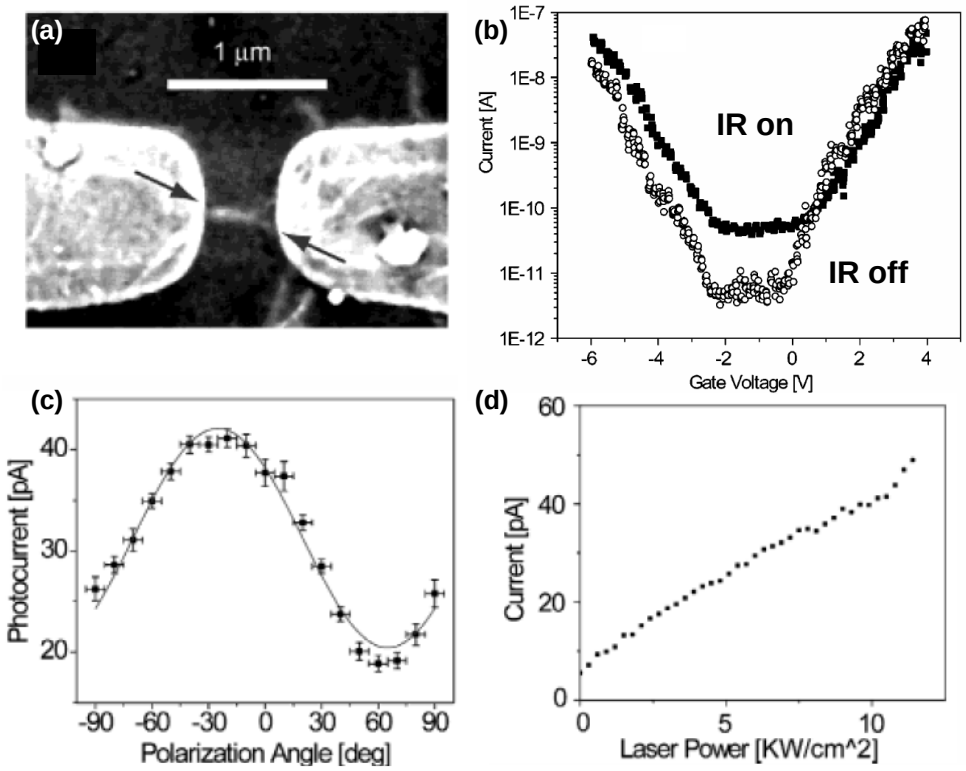

Figure 3.17 (a) SEM image of the device. [22]

(b) Drain current as a function of gate voltage. [22]

(c) Light polarization angle dependence of photocurrent. [22]

(d) Light intensity dependence of photocurrent. [22]

Photovoltaic effect

Photovoltaic effect was observed in CNT with electrically defined pn-junction. [23] Two local gates were fabricated and the gate oxide in the area between them were removed to suspend CNT (**Fig. 3.18 (a)**). CNT was suspended to improve CNT properties by reducing charged impurities and carrier recombination. The two local gates were oppositely biased to separate photocarriers (**Fig. 3.18 (b)**). Photovoltaic current offset was observed with increasing light intensity as shown in **Fig. 3.18 (c)**.

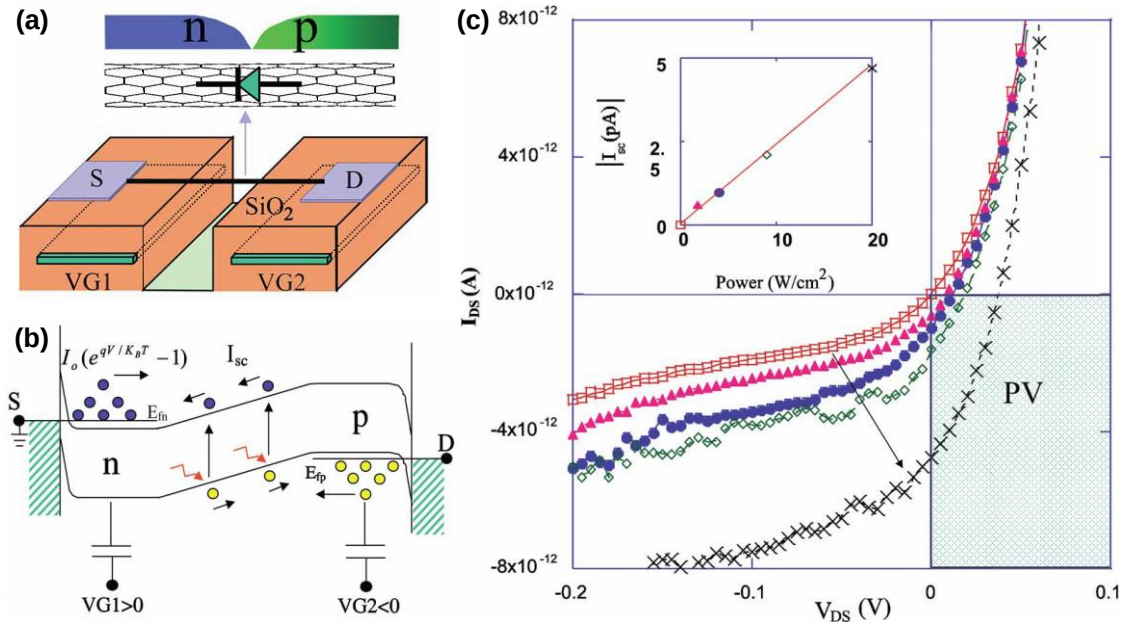

Figure 3.18 (a) Schematic of suspended CNT with two local gates. [23]

(b) Band structure for device operation. [23]

(c) Drain current as a function of drain voltage at each light intensity. [23] Inset shows intensity dependence of photocurrent.

Photothermoelectric effect

Photothermoelectric effect was observed in addition to photovoltaic effect in suspended CNT with electrostatically defined pn-junction. [24] In this device, electrodes and trench were fabricated first, then CNT was grown from catalyst on drain electrode across to source (**Fig. 3.19 (a)**). Scanning photocurrent microscopy was used to observe the photocurrent and its position and direction at various local gate voltages. When the local gates were oppositely biased to form pn-junction, photocurrent flowing to source was observed at pn-junction, as shown in **Fig. 3.19 (b)**. This is consistent with photovoltaic effect at pn-junction. When both local gates were biased to n-n, photocurrent was observed around the metal contacts (**Fig. 3.19 (c)**). This is due to metal contacts are W/Pt which is p-type contact. Photocurrent in this case is also in consistent with photovoltaic effect. A different photocurrent direction was observed when local gates were biased to p-p (**Fig. 3.19 (d)**). The direction of photocurrent contradicts with photovoltaic effect, indicating that a different photoresponse mechanism may be dominant. Photothermoelectric was proposed as the dominant mechanism in this case. A color plot of photocurrent at each local gate voltage is shown in **Fig. 3.20 (a)**. Sign reversal of photocurrent can be seen between p-n and p-p^+ and between n-p and p^+-p as shown in line cuts in **Fig. 3.20 (b)**. The photocurrent sign change can be explained by the magnitude relation of Seebeck coefficient (**Fig. 3.20 (c)**). The order of the largest Seebeck coefficient to smallest is from p^-, p, p^+ and n. Thermoelectric current flows from region

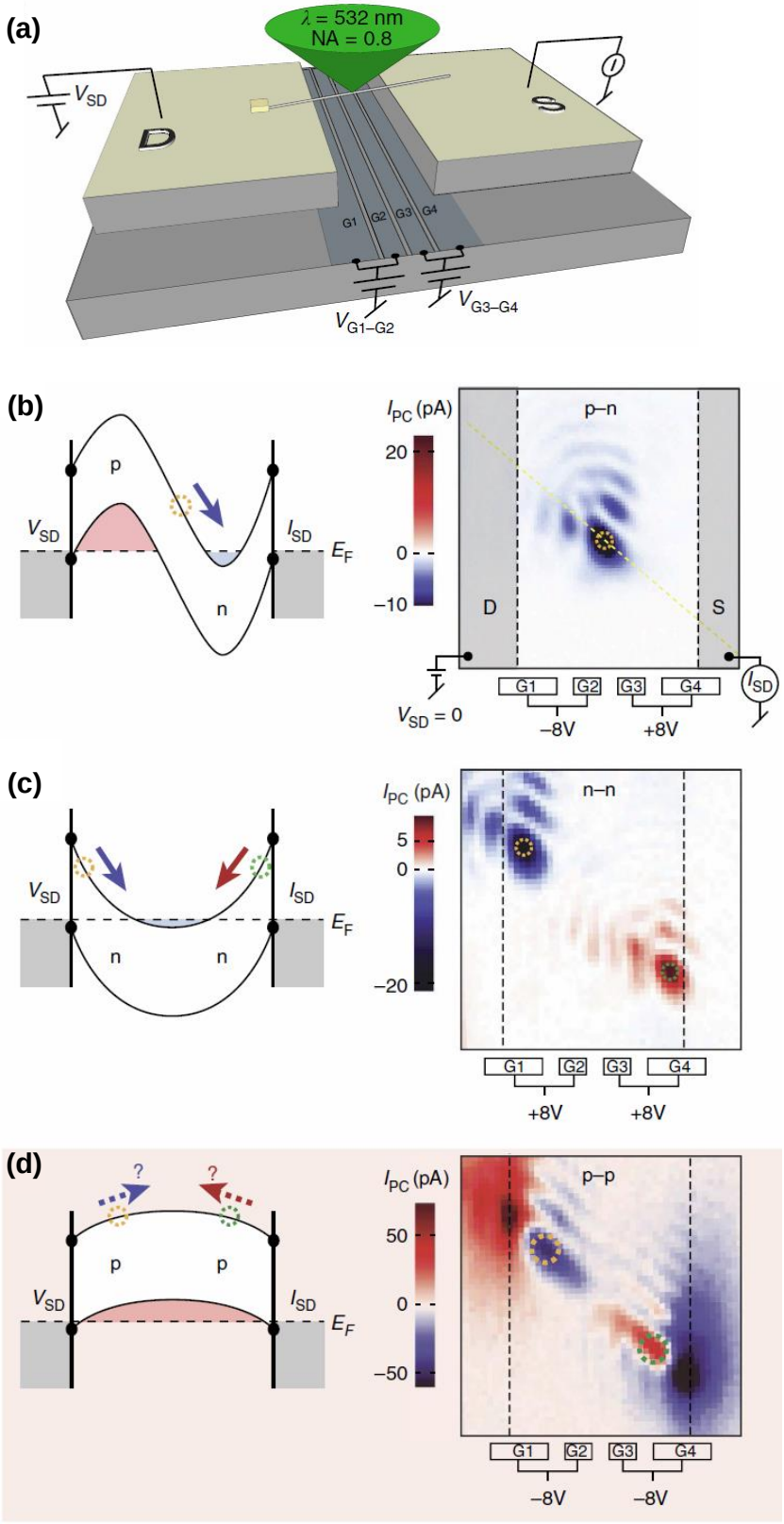

Figure 3.19 (a) Schematic of the device. [24]

(b) Schematic of photoresponse and photocurrent mapping for p-n. [24]

(c) Schematic of photoresponse and photocurrent mapping for n-n. [24]

(d) Schematic of photoresponse and photocurrent mapping for p-p. [24]

with larger Seebeck coefficient to smaller Seebeck coefficient. The measured photocurrent was considered to be composed of photovoltaic component and photothermmoelectric component (**Fig. 3.20 (d)**). For p-n, the two components have the same direction, hence a behavior consistent with photovoltaic effect. For p-p^- and p-p^+, thermoelectric current has the opposite direction to photovoltaic current. From the results, it was observed that photothermoelectric current dominated photovoltaic current. Moreover, the maximum photocurrent was observed in p-p^+ region, indicating that photothermoelectric effect is dominant in this device. However, the maximum photocurrent was expected in p-n because of the maximum difference in Seebeck coefficient. Also, similar behavior to p-p was not observed in n-n. This may be due to high contact resistance for n-type. Photothermoelectric response closer to ideal can be observed when contact resistance is low for both p-type and n-type, such as in metallic CNT and graphene.

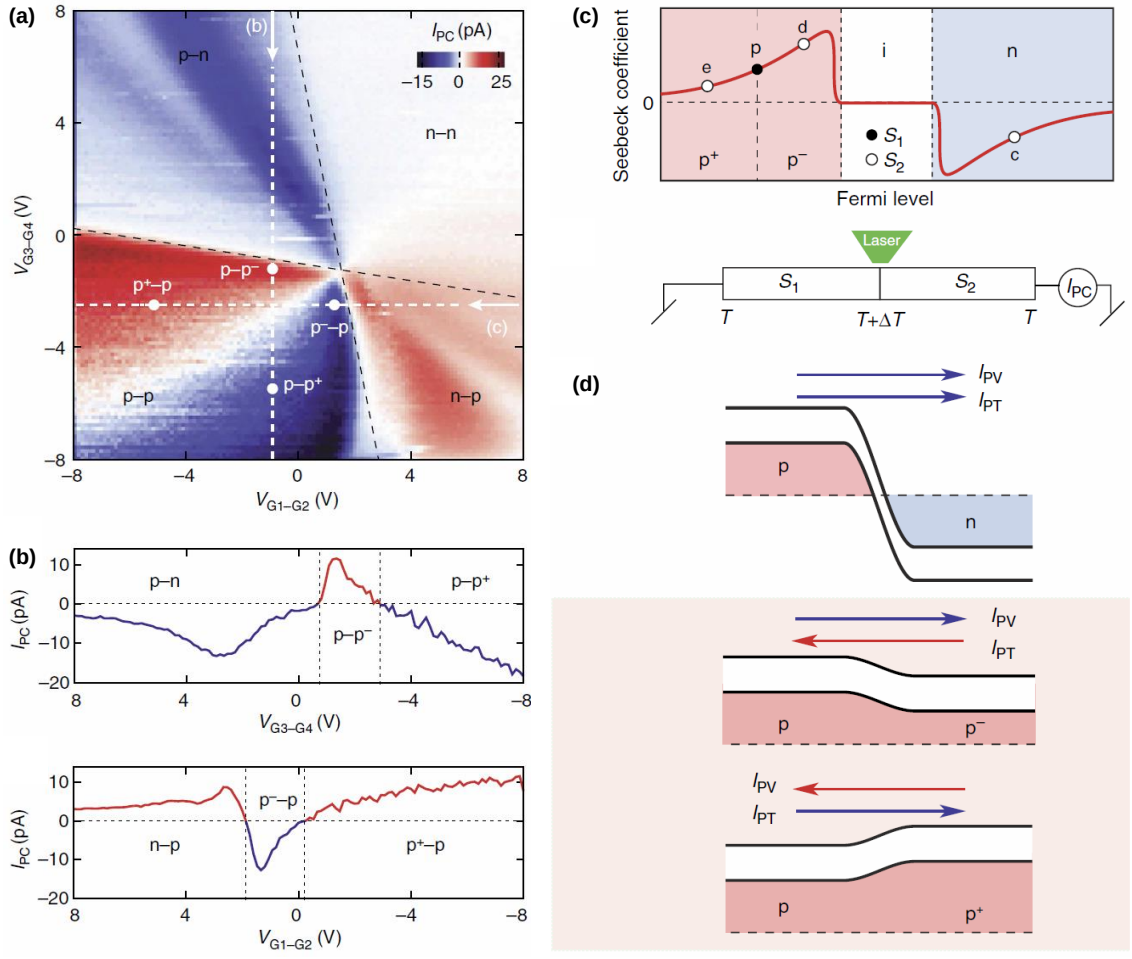

Figure 3.20 (a) Color plot for photocurrent as a function of local gate voltage. [24]

(b) Line cuts in **(a)**. [24]

(c) Seebeck coefficient for different doping and temperature gradient. [24]

(d) Photovoltaic and photothermal current for different doping. [24]

Bolometric effect

Bolometric response at room temperature was reported in suspended SNT sheets. [25] CNT sheet was suspended on SiO_2/Si substrate with periodic trenches (**Fig. 3.21 (a)**). Improved bolometric response compared to supported CNT was achieved due to reduced thermal conduction between CNT and substrate. The response time was 50 ms, which is comparable to conventional bolometers (**Fig. 3.21 (b)**). Responsivity was increased at higher bias current but detectivity shows peak value of 4.5×10^5 cm $Hz^{1/2}$/W around bias current of 10^{-4} A (**Fig. 3.21 (c, d)**).

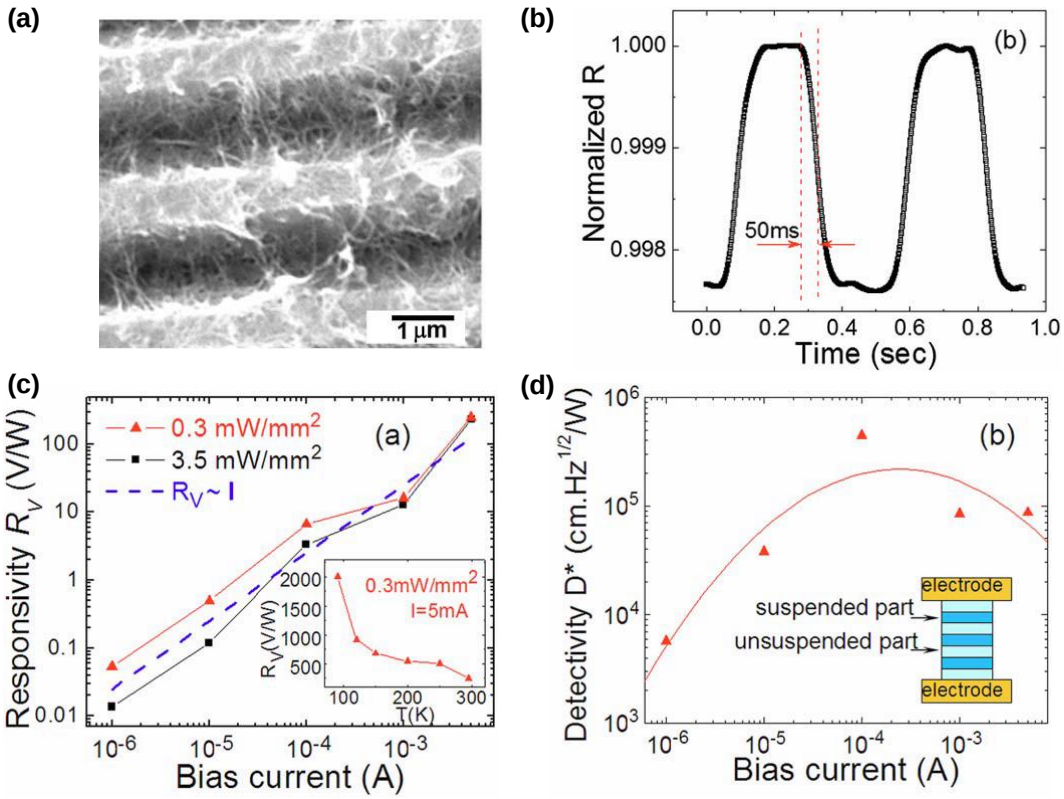

Figure 3.21 (a) SEM image of the device. [25]

(b) Time response for resistance. [25]

(c) Responsivity as a function of bias current. [25]

(d) Detectivity as a function of bias current. [25]

An improved performance was reported in CNT microbolometer array. [26] CNT film was suspended on Si_3N_4/Si substrate which was patterned into pixels, as shown in **Fig. 3.22 (a)**. The device showed broadband response in infrared wavelength from 0.8-6 μm, with peak photoresponse at 2 μm (**Fig. 3.22 (b)**). The response time was 10 ms and noise spectra showed a behavior like 1/f noise (**Fig. 3.22 (c)**), which is common among CNT devices operating in atmospheric conditions. Detectivity was measured to be 5.5×10^6 cm $Hz^{1/2}$/W at 40 Hz modulation (**Fig. 3.22 (d)**).

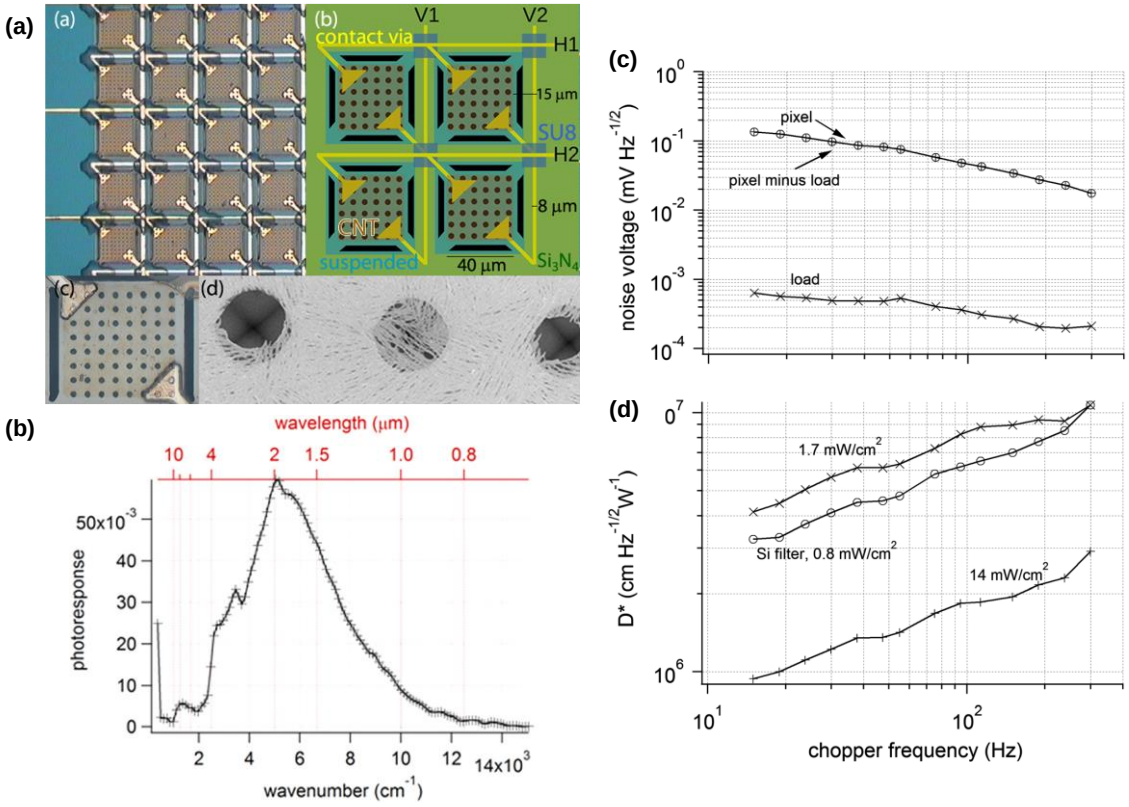

Figure 3.22 (a) Optical image and SEM image of the device. [26]

(b) Photoresponse spectra. [26]

(c) Noise voltage as a function of chopper frequency. [26]

(d) Detectivity as a function of chopper frequency. [26]

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Chapter 4 Objectives

The overall goal of this study is to evaluate the possibility of bilayer graphene FETs and photodetectors. The outline of this study is as follows:

1. All-2D heterostructure BLG-FET fabrication.
2. Determination of dielectric constant of *h*-BN from capacitance measurement.
3. Evaluation of FET properties based on transport properties.
   3.1 Qualitative evaluation of potential fluctuations from suppression of off-current.
   3.2. Quantitative evaluation of band gap by temperature dependence of conductivity at Dirac point in transport measurement.
   3.3. Quantitative evaluation of potential fluctuations from remnant band gap at zero displacement field.
4. Evaluation of FET properties based on *h*-BN/BLG interface properties from capacitance measurements.
   4.1. Quantitative evaluation of band gap from quantum capacitance.
   4.2. Quantitative evaluation of interface trap density by conductance method.
5. Evaluation of photodetector properties.
   5.1 Investigation of basic photoresponse mechanism without phototransistor action in device with top gate length longer than diffusion length.
   5.2. Identification of phototransistor action from photoresponse in a device with top gate length shorter than diffusion length.

Chapter 5 Hetero-FET fabrication

5.1 Assembly of heterostructures

Transparent substrate

Polydimethylsiloxane (PDMS) was used as elastomer stamp due to its elasticity and large thermal expansion coefficient. Silicone elastomer from Shinetsu chemical was used to prepare 1 mm thick PDMS. The hardness and stickiness can be adjusted by the ratio of silicone base and curing agent. In this study, silicone base: curing agent ratio of 10:1 was used for hardness and ease of peeling polymer stack from SiO_2 surface. The amount of silicone base required to achieve 1 mm thickness depends on the size of petri dish. For petri dishes with 9 cm diameter, 10 g of silicone base is the suitable amount. After mixing the silicone base and the curing agent, the mixture was placed in vacuum desiccator for 30 minutes for degassing. Then, the mixture was poured onto petri dish and spin coated at 200 revolutions per minute (rpm) for 3 seconds to spread the mixture throughout the petri dish evenly. Lastly, the mixture was dried in convection oven at 50°C for one day.

An area of 1 cm^2 of prepared PDMS was cut by cutter and was placed on a glass slide. Polemethylmethacrylate (PMMA) 11 wt% in anisole (MicroChem) was spincoated on PDMS at 3000 rpm for 60 seconds. The substrate was then baked at 75°C for 45 minutes to evaporate anisole. This condition was used to avoid wrinkles resulted from the difference between thermal expansion of PDMS and PMMA.

Preparation of *h*-BN on transparent substrate

The transparent substrate was treated with air-plasma with a current of 5 mA for 1 minute to make the PMMA surface active, increasing the adhesion to *h*-BN. *h*-BN crystals synthesized at high pressure [1] were mechanically exfoliated by Scotch tape. Here, the adhesiveness of the tape has to be sufficiently reduced so that the tape can be peeled of PMMA without peeling off PMMA from PDMS. Then the tape was cut by scissors into a size smaller than PDMS and one edge of tape was folded together to be held by tweezers for ease of peeling. The tape was placed on newly treated PMMA, without touching the edges of PMMA. If the edges of PMMA come to contact with the tape, PMMA will be easily peeled off by the tape. The tape was gently rubbed, and peeled off slowly from PMMA, leaving exfoliated *h*-BN on PMMA. A schematic of the process is shown in **Fig. 5.1**.

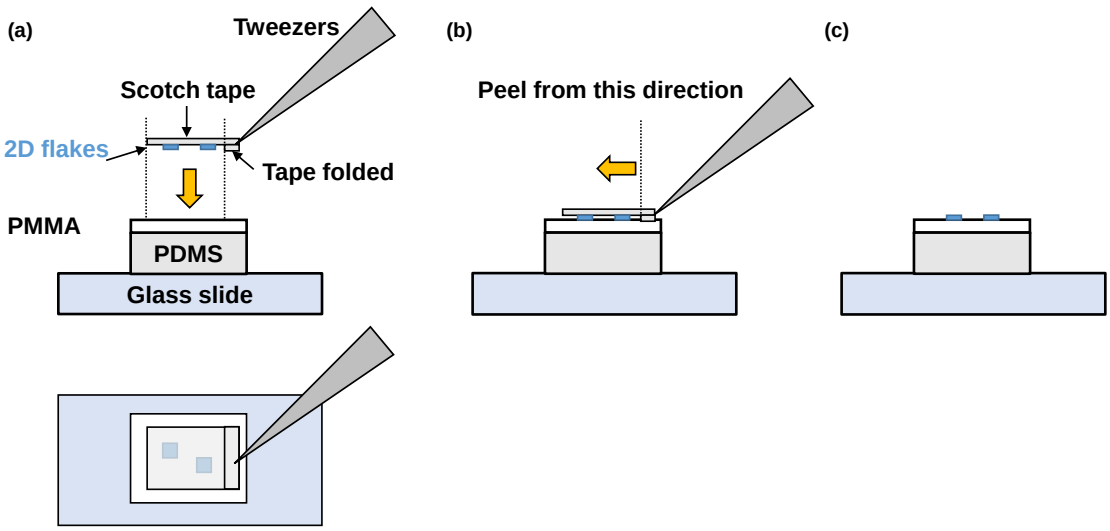

Figure 5.1 (a) Schematic for exfoliating 2D flakes onto PMMA/PDMS/glass slide from side and top view.

(b) Peeling off direction.

(c) 2D flakes exfoliated onto PMMA/PDMS/glass slide.

Preparation of two-dimensional layered crystals on SiO_2/Si substrate

Bilayer graphene (BLG), graphite (G) and *h*-BN were mechanically exfoliated by Scotch tape onto n^+-Si/SiO_2 (90 nm) substrates annealed in O_2 atmosphere at 1050°C for 5 minutes. BLG was identified by optical contrast. Graphite and *h*-BN were chosen based on their thickness and surface flatness. The thickness can be estimated by color, based on past data (**Fig. 5.2 (a)**). A thickness above 20 nm is required for *h*-BN to prevent gate leakage and to eliminate the roughness of substrate (**Fig. 5.2 (b)**). For graphite to be used as back gate electrodes, thickness above 10 nm is required to prevent voltage drop resulted from quantum capacitance related to small DOS in thin graphite films. *h*-BN thinner than 20 nm can be used with graphite back gate electrode because the total 2D crystal thickness required to eliminate SiO_2 surface roughness can be mainly covered by graphite back gate. The surface flatness of *h*-BN and graphite can be confirmed by enhancing optical contrast. By setting the input range for contrast to the values of RGB around that of the target crystal, a step of 1 nm height can be identified by optical microscope (**Fig. 5.3**).

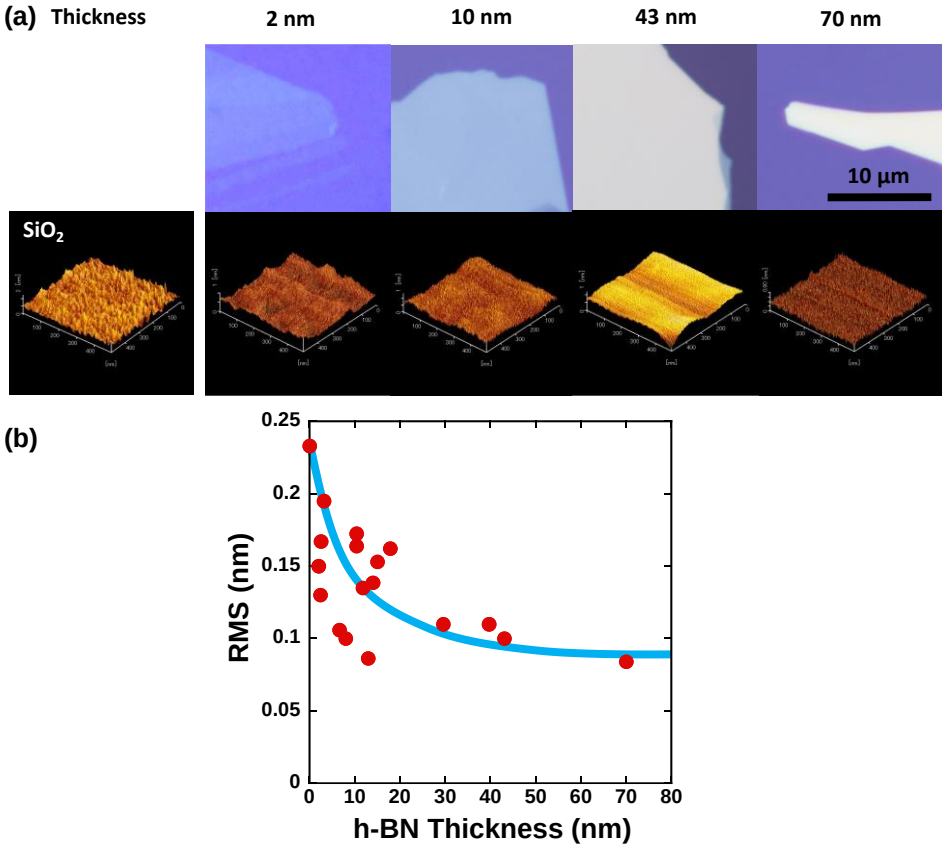

Figure 5.2 (a) Optical images of *h*-BN with different thickness and AFM image of their surfaces.

(b) Root mean square of surface height and thickness of *h*-BN.

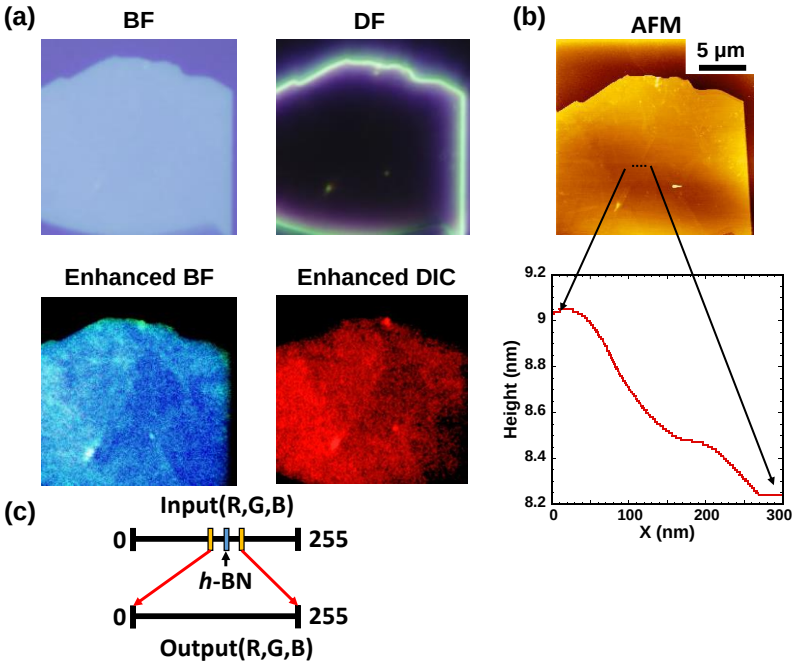

Figure 5.3 (a) Optical image of *h*-BN in each modes.

(b) AFM image of the same *h*-BN.

(c) Contrast enhancement.

Stacking two-dimensional layered heterostructure

Heterostructures were assembled in ambient condition by a micromanipulator with Peltier module shown in **Fig. 5.4**. The position of *h*-BN and BLG were aligned by stepping motor, and then SiO_2/Si substrate was heated to 100°C for 5 minutes to drive away the adsorb water on the substrate surface. After the substrate temperature cooled down to near room temperature, BLG on SiO_2/Si substrate was brought into contact with *h*-BN while being heated to 60°C to facilitate the contact between the two crystals. After that, the Peltier was switched off, and the lower stage was lowered slowly to peel two substrates from each other. Using the same mechanism as "pick-up" method [2] BLG can be picked up by *h*-BN on transparent substrate. By repeating the procedure, *h*-BN/BLG/*h*-BN/G stack was obtained on transparent substrate. A fused silica substrate with Au marks was treated by UV ozone for 5 minutes to remove resist residue. The stack was brought into contact with freshly treated fused silica substrate and heated to 90°C for 5 minutes to increase PMMA adhesion to fused silica. The two substrates were placed in acetone while being kept attached, in order to dissolve PMMA. After leaving the substrates in acetone for one night, glass slide and PDMS detached from fused silica substrate, leaving the heterostructure on fused silica. The sample was rinsed with isopropyl alcohol (IPA). Optical images for the process are shown in **Fig. 5.5**.

Raman spectra taken along the stacking process (**Fig. 5.6**) showed that after picking BLG with *h*-BN, the split of the components of 2D peak, which is directly related to the band gap, became more pronounced. This was because the peak width for each component became narrower, suggesting the reduction in disorder and potential fluctuations.

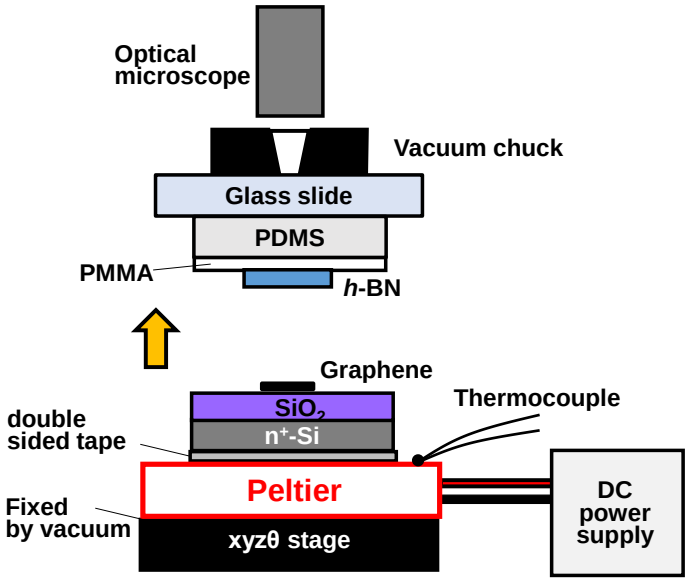

Figure 5.4 Schematic for micromanipulator system.

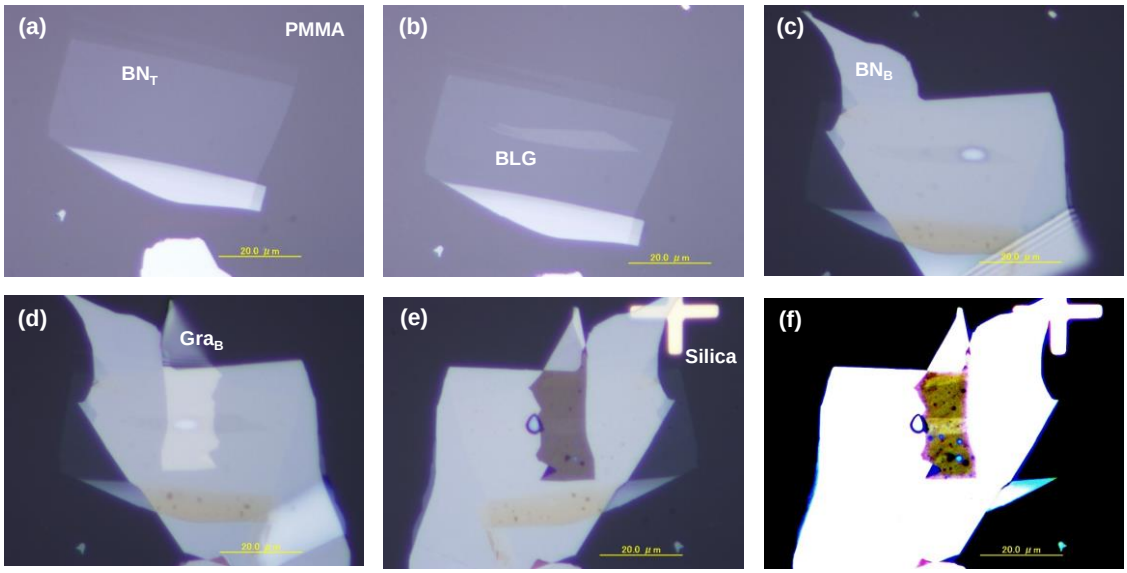

Figure 5.5 **(a)** Optical image of top *h*-BN on PMMA. Scale bar length is 20 μm.
(b) *h*-BN/BLG.
(c) *h*-BN/BLG/*h*-BN.
(d) *h*-BN/BLG/*h*-BN/G.
(e) *h*-BN/BLG/*h*-BN/G transferred onto silica substrate.
(d) Enhanced contrast for **(e)** highlighting BLG in graphite region.

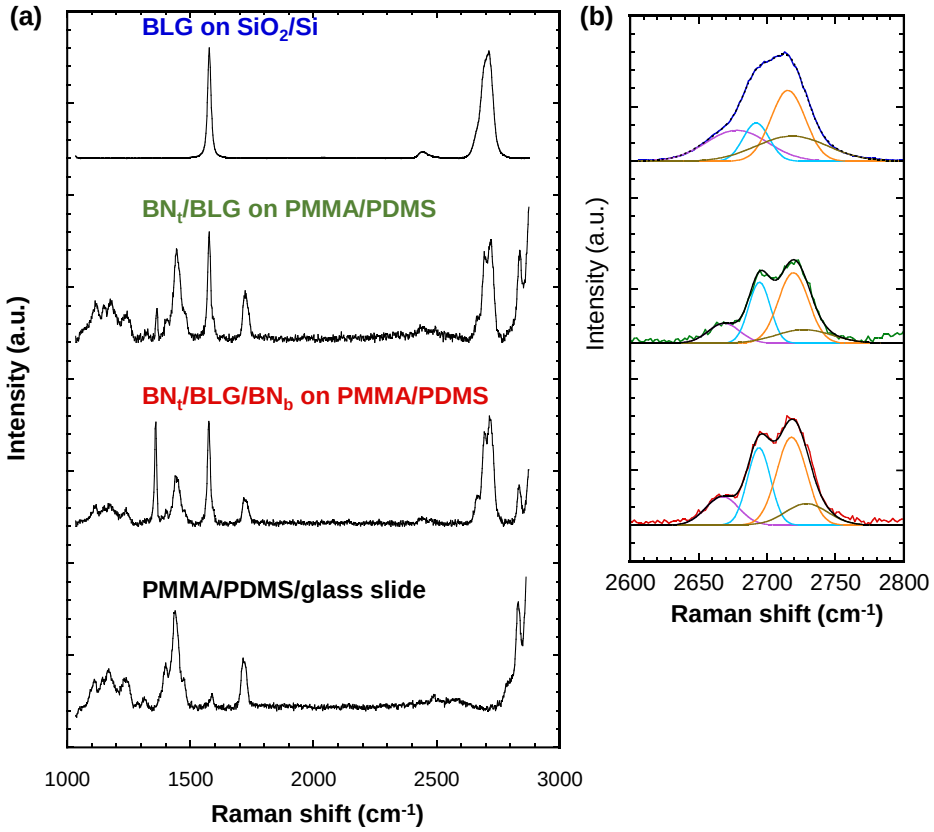

Figure 5.6 **(a)** Normalized Raman spectra at each step of stacking.
(b) 2D peaks in **(a)** fitted by four components.

The heterostructure was annealed in H_2/Ar atmosphere at 200°C for 3 hours to facilitate the adhesion of the interfaces. Unlike, graphene on *h*-BN, interfacial bubbles in *h*-BN encapsulated graphene did not aggregate after annealing, because their movement was hindered by top *h*-BN (**Fig. 5.7**). It was found that using BLG with a width narrower than 2 μm can reduce the amount of bubbles trapped in the channel area, as can be seen from the fraction of length of clean area and total length (**Fig. 5.8**). Furthermore, it was observed that bubbles formed near the edges of BLG after encapsulation often migrated out of the BLG flake after annealing, making it possible to obtain a larger clean interface area in narrow BLG for further device fabrication.

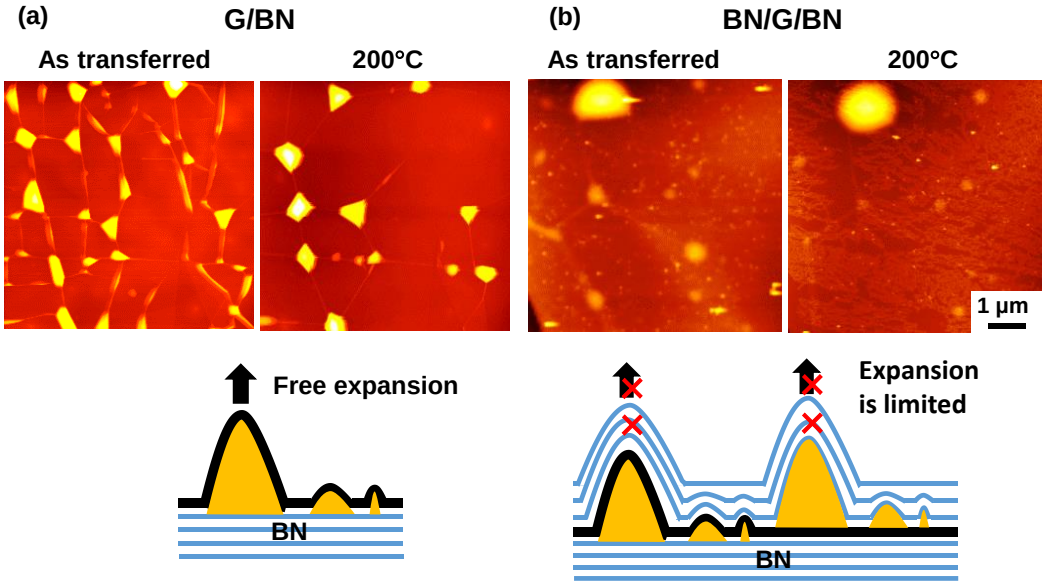

Figure 5.7 (a) AFM image of graphene on *h*-BN before and after annealing.
(b) AFM image of *h*-BN encapsulated graphene before and after annealing.

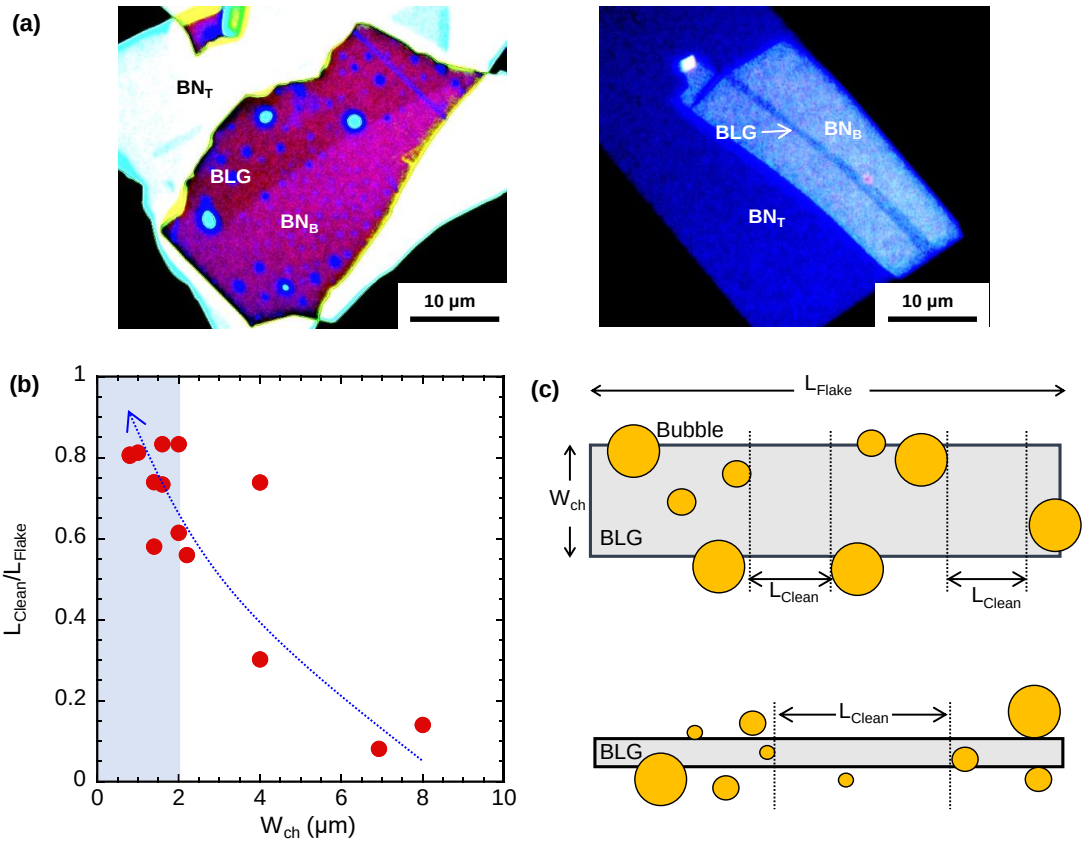

Figure 5.8 (a) Optical images of *h*-BN encapsulated BLG.

(b) Fraction of the length of clean BLG area (L_{Clean}) and the length of BLG flake as a function of BLG width (W_{ch}).

(c) Definition of L_{Clean} and L_{Flake} in **(b)**.

5.2 Contact formation

Because BLG was completely encapsulated in *h*-BN, electrical contacts cannot be directly formed on BLG. In previous studies, the contact region was entirely etched by CHF_3/O_2 plasma with 60 W power in a tilted profile to form edge contact with metal electrodes (**Fig. 5.9**). [2] In this study, it was found that *h*-BN can be selectively etched by CF_4 plasma with the power of 18 W. The selectivity of *h*-BN compared to BLG is due to chemical reaction being more dominant in low power plasma, while in high power plasma physical etching is dominant. The etching rate difference between *h*-BN and BLG by CF_4 plasma shown in **Fig. 5.10 (a)** originated from the difference between bonding energies. B-N bonding energy is 389 kJ/mol while B-F bonding energy is 613 kJ/mol [3], meaning that rather than staying as *h*-BN, forming B-F is more energetically favorable, leading to high reactivity of *h*-BN to CF_4 plasma. On the other hand, C-F bonding energy is 485 kJ/mol, while C=C bonding energy is 602 kJ/mol, [3] meaning that remaining as graphene is more energetically favorable than forming C-F, leading to low reactivity of graphene to CF_4 plasma.

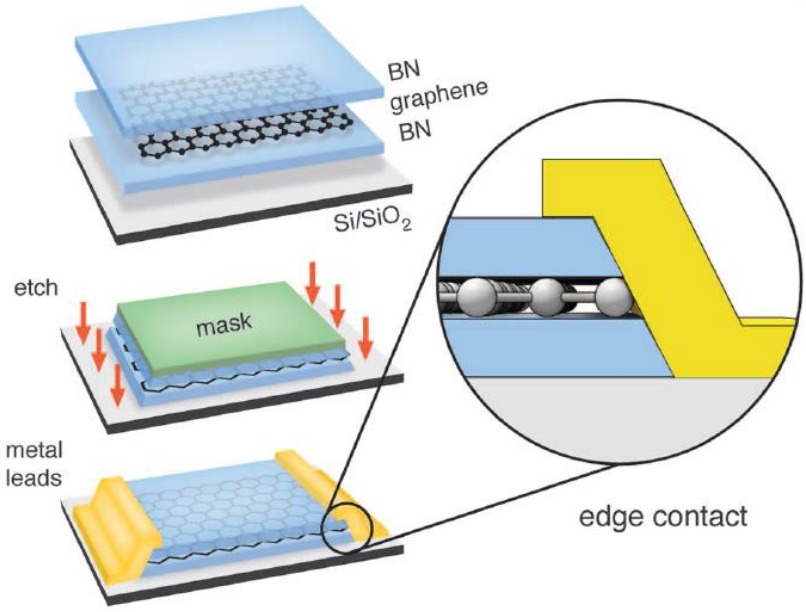

Figure 5.9 Edge contact formation. [2]

An example of etching process is shown in **Fig. 5.11**. Electrode patterns were formed by electron beam lithography. CF_4 was introduced into chamber with flow rate of 1 sccm while the pressure was kept at 10 Pa, which generated current of 6 mA. Using this condition top *h*-BN was selectively etched exposing BLG surface for formation of planar electrical contact on BLG. The difference in the etching rate is high enough that, 12 nm-thick *h*-BN top gate and 32 nm-thick *h*-BN back gate were completely etched while BLG remains the same, even protecting *h*-BN under it. After CF_4 etching, the presence of BLG in contact areas were confirmed by Raman spectroscopy. This enables the formation of surface electrical contact on BLG. Then, the contact areas were exposed to O_3 plasma in order to remove contaminants, [4] and lastly Ni/Au electrodes were deposited by thermal evaporation. The contacts formed were ohmic contact as shown in **Fig. 5.11 (d)**. The yield for ohmic contacts is greater than 80 % because of the large contact area available in surface contacts. It can be seen that the implementation of this method can be much simpler and easier than forming edge contacts.

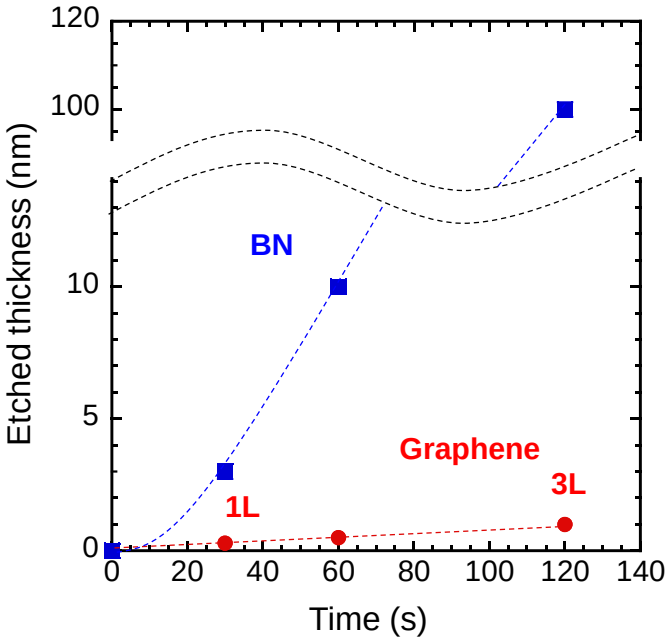

Figure 5.10 Etching rate by CF_4 plasma.

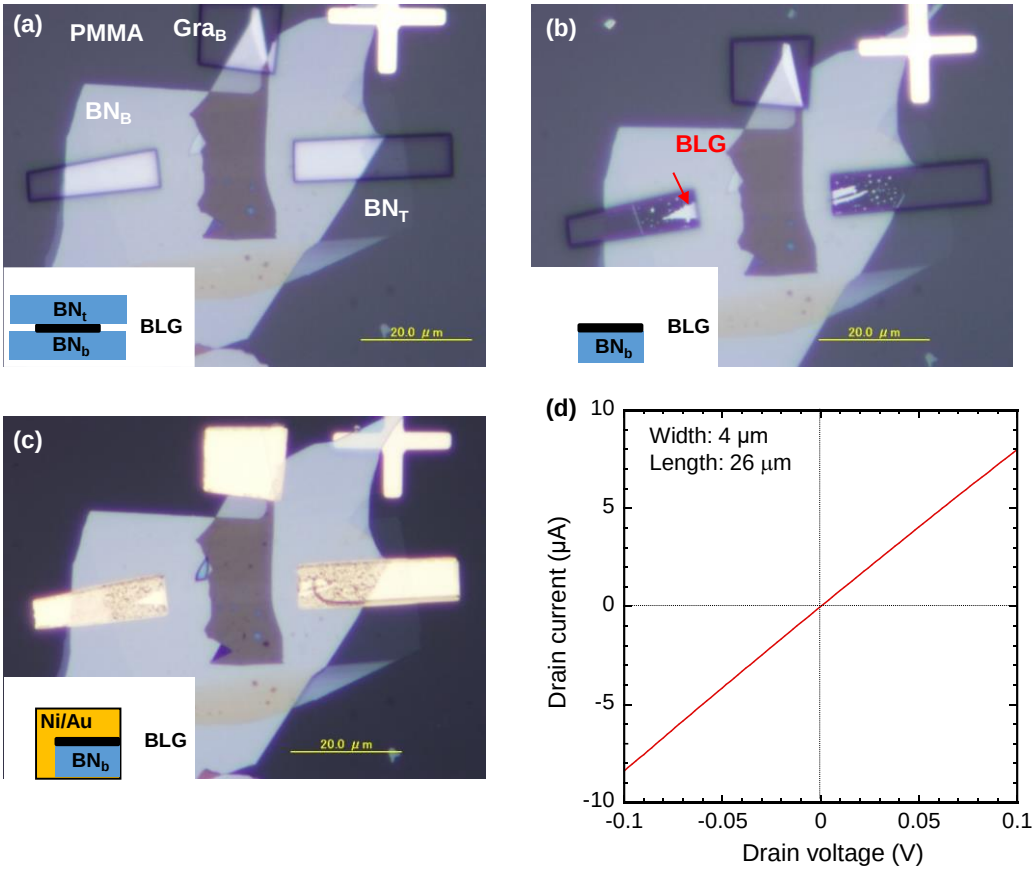

Figure 5.11 **(a)** Optical image of electrode pattern before etching. Inset shows side view.

(b) After CF_4 plasma etching.

(c) After depositing Ni/Au.

(d) Drain current as a function of drain voltage measured from device in **(c)**.

5.3 Top gate electrode

Metal top gate electrodes have been conventionally used in BLG devices so far. However, electron back scatter diffraction pattern (EBSD) analysis revealed that the Ni/Au top gate metal electrode was tiny polycrystalline (**Fig. 5.12**), which can lead to an increase in the potential fluctuation in BLG due to the variation of the work function for different crystal orientations. Therefore, to minimize the potential fluctuations in BLG, graphite was also used as the top gate electrode for *h*-BN-encapsulated BLG, creating all-2D heterostructure, as shown in **Fig. 5.13**. The cross sectional transmission electron microscope (TEM) image (**Fig. 5.13 (c)**) indicates that the interface between *h*-BN and BLG is clean and atomically sharp, unlike that of Y_2O_3/BLG. [5]

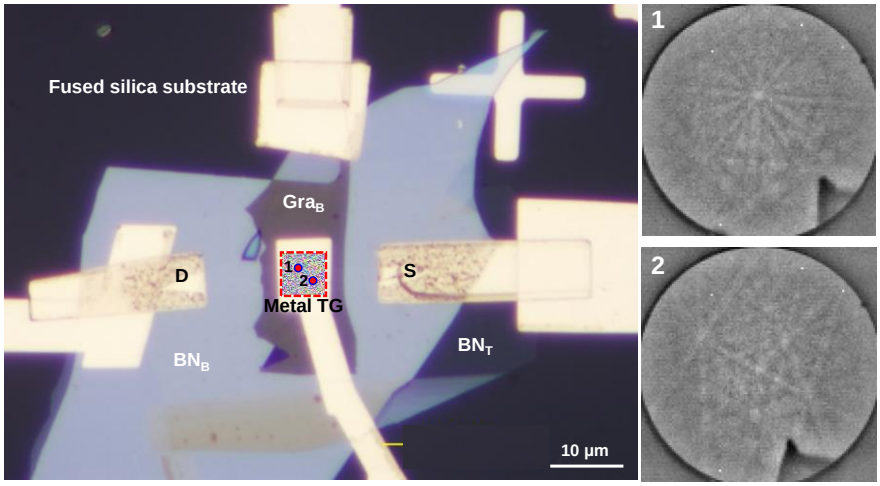

Figure 5.12 Electron back scatter diffraction pattern in metal top gate electrode.

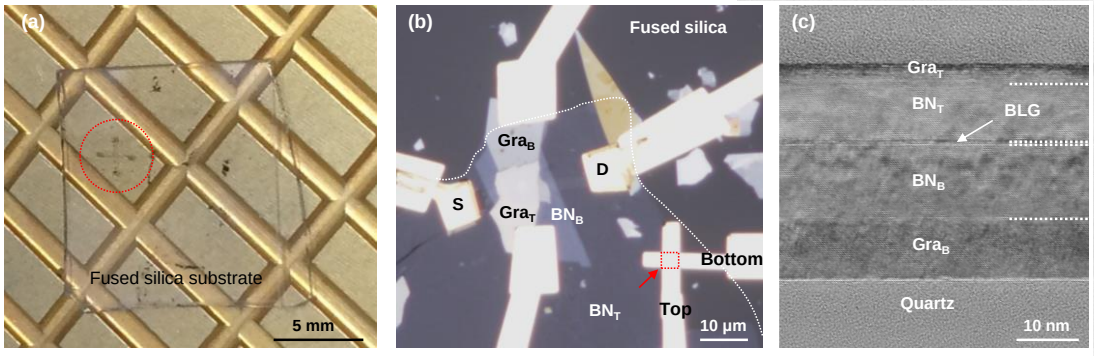

Figure 5.13 (a) Optical image of an all-2D hetero-FET on fused silica substrate.
(b) Enlarged image of **(a)**.
(c) Cross section TEM image.

5.4 Temperature correction for silica substrate

Fused silica substrate has much smaller thermal conductivity than n^+-Si/SiO_2 substrate. In measurement at low temperature, this can cause non-negligible temperature difference between stage temperature and substrate surface temperature. The surface temperature of fused silica substrate and n^+-Si/SiO_2 was measured by placing probes on Si diode temperature sensor attached to substrate surface and measuring voltage difference at constant current from 10 K up to 300 K. Temperature was calculated by comparing voltage difference to the data sheet given with Si diode. The difference between temperature measured at substrate surface and stage temperature is shown in **Fig. 5.14**. Fused silica substrate shows larger temperature difference than n^+-Si/SiO_2. Calculations based on temperature dependence in devices in this study will be adjusted based on this data.

It was also observed that the temperature of probes was higher than the stage at temperature below 220 K. This is because the stage is directly connected with cryostat and heater, making temperature control precise. On the other hand, probes are only connected to the stage through copper wires, making temperature control for probes far less accurate. Therefore, the substrate surface temperature measured may be affected by probe temperature, resulting in difference between substrate surface temperature and stage temperature. The thermal conductivity of substrate may also affect the heat conduction between probes and stage through substrate, resulting in larger temperature difference in fused silica substrate.

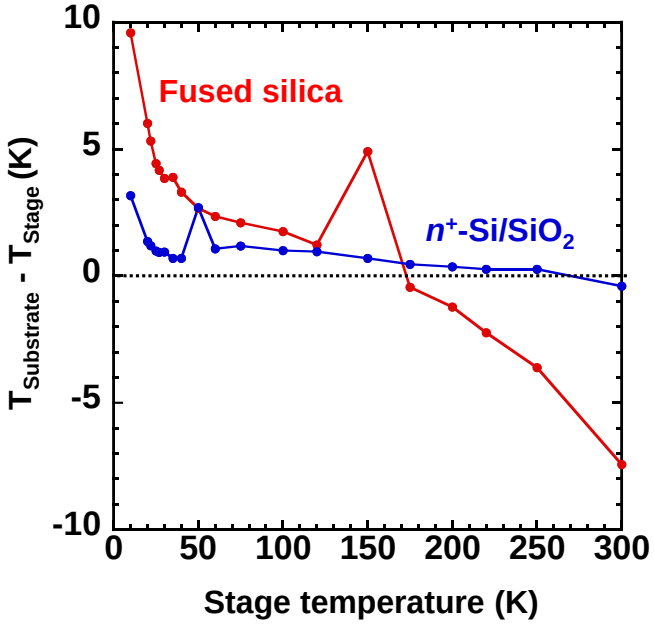

Figure 5.14 Difference between substrate surface temperature and stage temperature.

5.5 References

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Chapter 6 Determination of dielectric constant of *h*-BN

In order to accurately calculate quantum capacitance and displacement field, the exact value of dielectric constant and thickness of *h*-BN are required. The dielectric constant can be calculated from

$$C = \frac{\varepsilon_{BN}\varepsilon_0}{t_{BN}}A.$$

Here C is capacitance, ε_{BN} is dielectric constant of *h*-BN, ε_0 is the permittivity of vacuum, t_{BN} is the thickness of *h*-BN, and A is electrode area. In this chapter, *h*-BN thickness and dielectric constant were determined and compared to other studies.

6.1 Thickness determination

In bulk insulators, their thickness can be accurately measured by elipsometry. But exfoliated *h*-BN has small size of ~10 μm, making measurement by elipsometry extremely difficult. In previous studies the thickness of *h*-BN was determined from atomic force microscopy (AFM). It is known that thickness of thin 2D crystal measured on SiO_2 can contain an error up to nm order because of SiO_2 surface roughness and adsorbed water on SiO_2 surface, as shown in **Fig. 6.1**. Using the fact that SiO_2 surface roughness can be lessen by 2D crystal and hydrophobic interface between 2D crystals, *h*-BN thickness in this study was determined from thickness measured by AFM in G/*h*-BN/G. Moreover, the utilization of G electrodes allows device fabrication on fused silica substrates which can drastically reduce parasitic capacitance. An example of fabricated device is shown in **Fig. 6.1**.

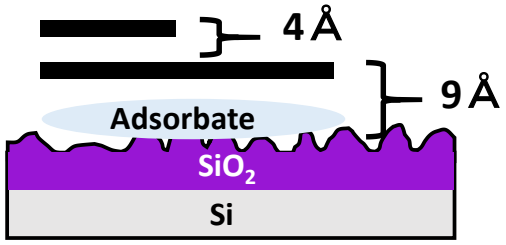

Figure 6.1 Thickness error in AFM.

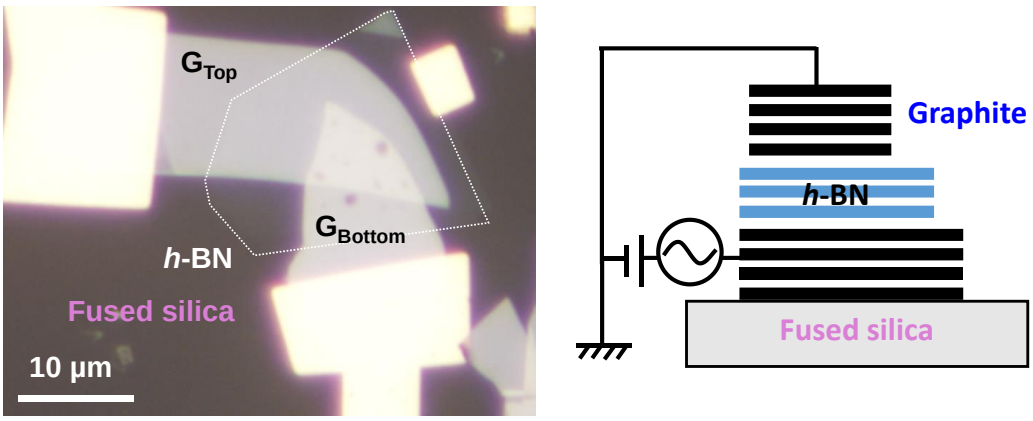

Figure 6.2 G/*h*-BN/G capacitor.

6.2 Capacitance measurement

Capacitance of G/*h*-BN/G was measured at frequency from 10 kHz to 2 MHz at temperature of 10 K to 300 K. As shown in **Fig. 6.3 (a)**, there was no significant frequency dependence, suggesting reliability for impedance measurement in conductance method. The dielectric constant at each temperature was calculated with consideration of the effect of thermal expansion on the thickness and area. It was found that there was no significant temperature dependence on dielectric constant. The thickness of measured *h*-BN were 10 nm and 4.4 nm, and the obtained dielectric constant were 2.28 and 1.86 respectively. Here, the difference in thickness determination method is shown in **Fig. 6.3 (b)**. Dielectric constant would be overestimated if the thickness measured on SiO_2 was used.

Dielectric constant normal to c plane and thickness of *h*-BN measured in this study are compared with other studies in **Fig. 6.4**. Pyrolytic *h*-BN [1] has the largest dielectric constant because of its polycrystalline nature where dielectric response in the direction parallel to c plane could contribute (dielectric constant parallel to c plane ~ 7). The dielectric constants measured from capacitance in this study are smaller than the ones measured from capacitance in other studies [2-5], possibly because in other studies the thickness of *h*-BN was measured by AFM on SiO_2 substrate which could result in overestimation of dielectric constant. The dielectric constants of thin *h*-BN measured by other methods [5, 6] are smaller than calculated values. [7] In calculation, ion polarization and electron polarization are considered. For electric field at optical frequency (~10^{13} Hz) ion polarization cannot catch up, causing the dielectric constant (optical dielectric constant) measured in this condition to be smaller than one measured at electrical frequency (~1 MHz). This suggests the possibility of reduced ion polarization response in samples where dielectric constant was determined by capacitance measurement. The reduction of dielectric constant in thin *h*-BN was suggested in previous studies as the

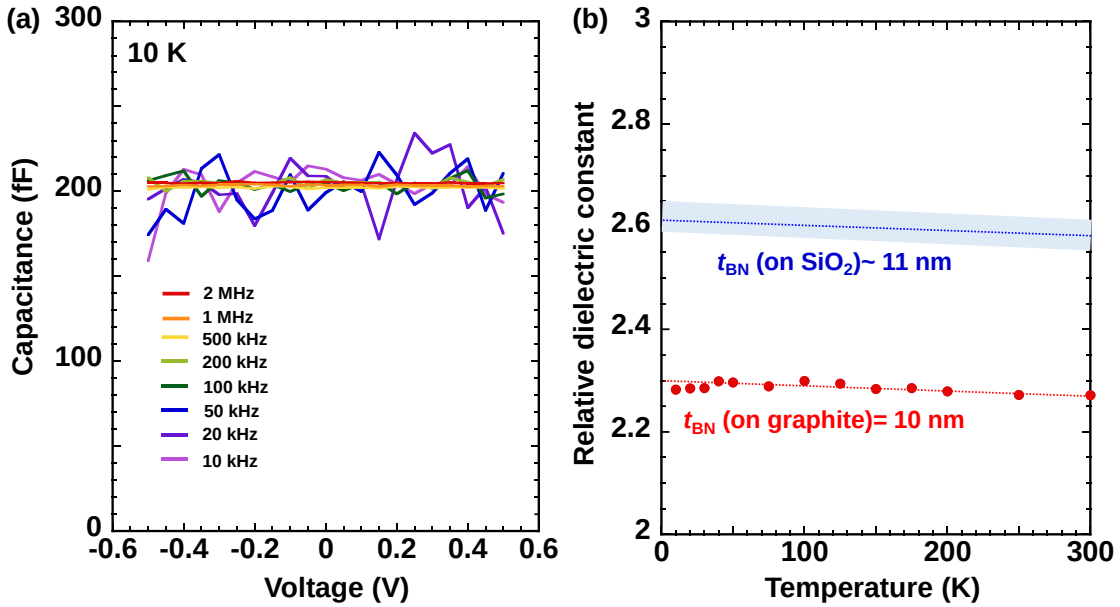

Figure 6.3 (a) Capacitance as a function of voltage for each frequency at 10 K. (b) Dielectric constant calculated from (a).

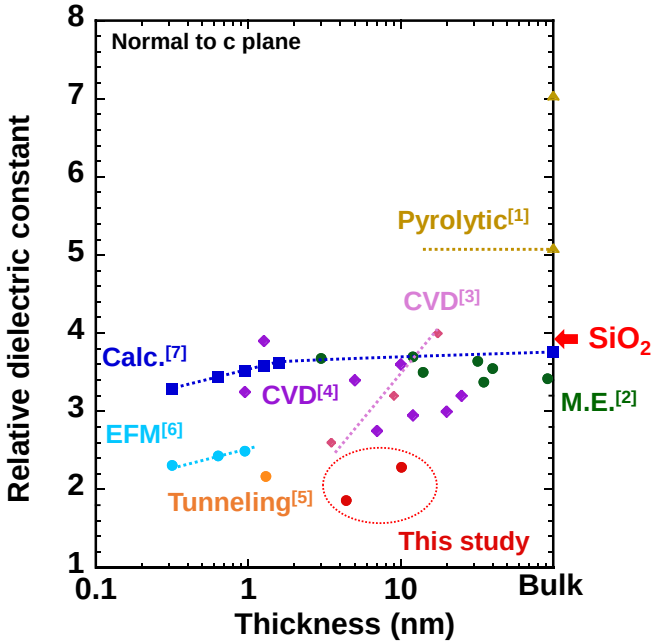

Figure 6.4 Dielectric constant normal to c plane of *h*-BN and thickness.

result of reduced ability to screen electric field. [5-7]

Although *h*-BN has break down electric field of 12 MV/cm normal to c plane [8] which is comparable to SiO_2, the measured dielectric constant was almost down to half of that of SiO_2. This can be a significant disadvantage for applying high displacement field to open large band gap in bilayer graphene.

6.3 References

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Chapter 7 Transport characteristics

IV measurements were performed on all-2D heterostructure BLG. Band gap formation and its uniformity were evaluated from current on/off ratio (I_{on}/I_{off}). Band gap size was determined from temperature dependence and potential fluctuations were determined by remnant band gap at zero displacement field. The importance of reducing potential fluctuations in BLG for FET application will be discussed.

7.1 Suppression of I_{off} by band gap opening

Transport characteristics measured at 20 K are shown in **Fig. 7.1**. As back gate voltage is increased, I_{off} became smaller, confirming band gap opening. As shown in the enlarged figure (**Fig. 7.1(b)**), I_{off} was suppressed to the measurement limit at $\bar{D} < -1.34$ V/nm, where the resistance was larger than ~5 GΩ. This value is quite similar to the recent report [1] and exceeds previously reported values of ~10-100 kΩ.[2-5] I_{off} in all-2D heterostructure BLG was reduced compared to *h*-BN-encapsulated BLG on SiO_2/Si as well as high-*k* Y_2O_3/BLG on SiO_2/Si at the same $|\bar{D}|$, as shown in **Fig. 7.1(c)**, indicating drastic reduction of the charged impurities and hence the spatial uniformity of the band gap of BLG. As a result, I_{on}/I_{off} was greatly increased compared to other devices at the same $|\bar{D}|$, and the maximum I_{on}/I_{off} at 20 K was 4.6×10^5 at $\bar{D} = -1.48$ V/nm, which is the best data thus far for *h*-BN-encapsulated BLG-FETs. Field effect mobility was estimated to be ~20000 cm^2/Vs at 20 K. Hysteresis was not detected and subthreshold swing was 40 mV/dec, suggesting the improvement in interface properties. Minor peaks were observed near the Dirac point for each back gate voltage at lower temperature. These could be minigap formed by moiré potential from *h*-BN. [6, 7]

It should be noted that resistivity at Dirac point did not saturate with increasing $\bar{D}$ unlike in the previous studies. [8, 9] Two different origins are proposed. One is the topological current along the AB-BA domain boundary in gapped BLG where resistivity saturation was observed at around $\bar{D}$ ~1 V/nm. [8] In this study, such behavior was not

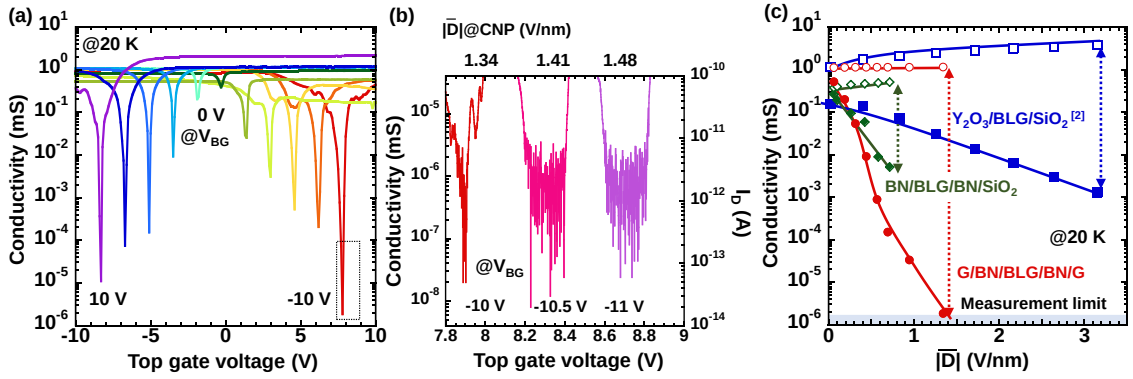

Figure 7.1 (a) Conductivity as a function of gate voltage at 20 K.

(b) Enlarged area in **(a)** measured at drain voltage of 0.01 V.

(c) Conductivity for I_{on} and I_{off} as functions of $|\bar{D}|$ at 20 K.

observed as the resistivity continued to increase up to $\bar{D}$ = -1.48 V/nm. This $\bar{D}$ value is one of the highest for *h*-BN encapsulated BLG so far and is sufficient to discuss the resistivity saturation. Therefore, it is suggested that there was no contribution of the current along the AB-BA domain boundary. The other origin is the topological edge current in gapped BLG where resistivity of the device with the Hall bar geometry saturated at around $\bar{D}$ = ~0.2 V/nm. [9] This contradicts the present study. In general, the edge current requires the zigzag edge structure, and the channel length should be shorter than the localization length. In this study, the channel length of ~20 μm could be much longer than the localization length, resulting in the absence of edge current. However, for a short channel, the edge structure should also be controlled to prevent topological edge current.

7.2 Temperature dependence

The temperature dependence of the conductivity at Dirac point shows two activation processes in measured temperature range, as shown in **Fig. 7.2 (a)**. They are known as thermal activation (TA) at high temperature and nearest neighbor hopping (NNH) at low temperature. [2, 4, 5] The conductivity at Dirac point is given by

$$\sigma_{\mathrm{Total}} = \sigma_{\mathrm{TA}}^{0}\exp\left[-\frac{E_{\mathrm{g}}}{2k_{\mathrm{B}}T}\right] + \sigma_{\mathrm{NNH}}^{0}\exp\left[-\frac{E_{0}}{k_{\mathrm{B}}T}\right],$$

where $\sigma_{\mathrm{TA}}{}^{0}$ and $\sigma_{\mathrm{NNH}}{}^{0}$ are prefactors, and E_{g} and E_0 are band gap and hopping energy, respectively. Here, temperature dependence of carrier mobility and band offset were not considered. All the conductivity data were well fitted with the above equation. E_{g} and E_0 were extracted and plotted as functions of $\bar{D}$ in **Fig. 7.2 (b, c)**. The maximum band gap opened in the all-2D heterostructure was ~90 meV at $\bar{D}$ = -1.34 V/nm, which is limited due to the small dielectric constant of *h*-BN and the dielectric breakdown field of ~1.2 V/nm for the thickness used in this experiment. [10] For $\bar{D}$ calculated by assuming bulk *h*-BN dielectric constant ε = 4, the measured E_{g} was smaller than the value calculated

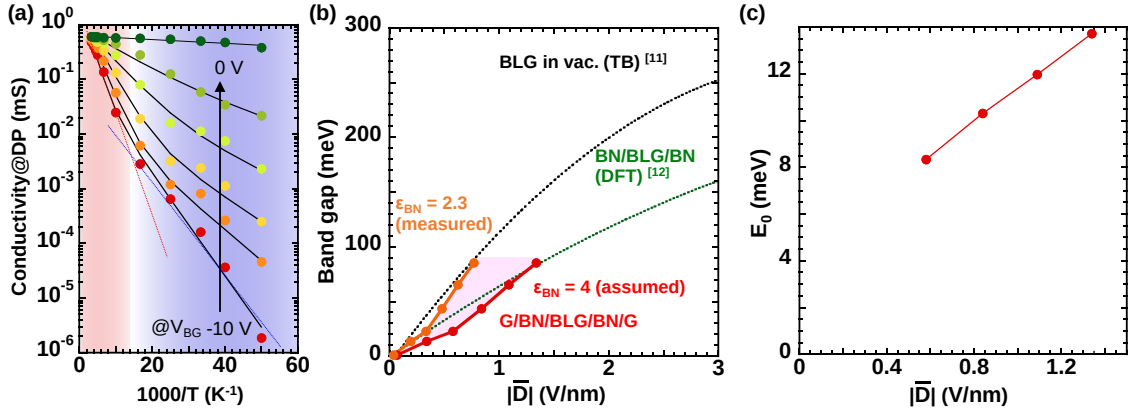

Figure 7.2 (a) Temperature dependence for conductivity at Dirac point.
(b) Band gap extracted from (a) as a function of $|\bar{D}|$.
(c) Hopping energy extracted from (a) as a function of $|\bar{D}|$.

by tight-binding method [11] for BLG in vacuum. The measured E_g seems to be closer to a case of band gap opening in *h*-BN encapsulated BLG. [12] In this calculation, it was shown that band gap of BLG encapsulated by *h*-BN will be smaller than that in BLG in vacuum at the same $\bar{D}$ in due to the screening of the electrical field by *h*-BN. On the other hand, for $\bar{D}$ calculated by measured 10 nm thick *h*-BN dielectric constant $\varepsilon = 2.3$, the value of measured E_g seems to be closer to the value calculated by tight-binding method for BLG in vacuum. Therefore there can be two possible reasons for deviation from calculation in the measured E_g. One is electric field screening by *h*-BN, the other is thickness dependence of dielectric constant of *h*-BN which results in error in calculation of $\bar{D}$.

Because NNH occurs by carrier hopping between localized states in the band gap, E_0 can be used as a measure for the amount of localized states in the band gap; i.e., the larger E_0 is, the smaller the amount of localized states in the band gap. In all-2D heterostructure BLG device, E_0 was extracted to be 14 meV at the maximum $\bar{D} = -1.34$ V/nm, as shown in **Fig. 7.2 (c)**. This is much larger than $E_0 = 2.8$ meV at a larger value of $\bar{D} = -3.1$ V/nm in the high-*k* Y_2O_3/BLG device, [2] supporting that there are fewer impurity-induced localized states in the band gap.

7.3 Estimation of potential fluctuations

The reduction of potential fluctuations from charged impurities has been qualitatively demonstrated. Here, the potential fluctuations in energy unit will be extracted. Ideally, E_g should be zero at $\bar{D} = 0$ V/nm, but in experiments, finite E_g at $\bar{D} \sim 0$ V/nm has been observed in previous studies because the potential fluctuations prevent the gap from closing locally. Therefore, $E_g/2$ at $\bar{D} \sim 0$ V/nm can be associated with the root-mean-square amplitude of the potential fluctuation (Φ_{rms}) in BLG. [4] **Figure 7.3 (a)** compares $E_g/2$ as a function of $\bar{D}$ for all-2D heterostructure and high-*k* Y_2O_3/BLG devices. In high-*k* Y_2O_3/BLG device, [2] Φ_{rms} was estimated to be 26 meV which is in agreement with the previous literature data on other high-*k*/BLG cases. [4] A significantly smaller value of $\Phi_{rms} = \sim 0.5$ meV was observed in several all-2D heterostructure devices fabricated in this study. The carrier density equivalent to such potential fluctuations was estimated to be 1.3×10^{10} cm^{-2} by the relation of $n = \Phi_{rms}(2m^*/\pi\hbar^2)$, where a constant 2D DOS for small energy deviation of E_F is assumed for simplicity. It should be emphasized that BLG is most sensitive to the potential fluctuations because band gap opening is the result of carrier density difference between the top and bottom graphene layers, suggesting that the utilization of all-2D heterostructure is crucial. Moreover, although the observed potential fluctuations in all-2D heterostructure seems to be comparable to those extracted from recently reported high-quality *h*-BN-encapsulated BLG on SiO_2/Si [13, 14] or on the metal electrode, [14] the difference between with and

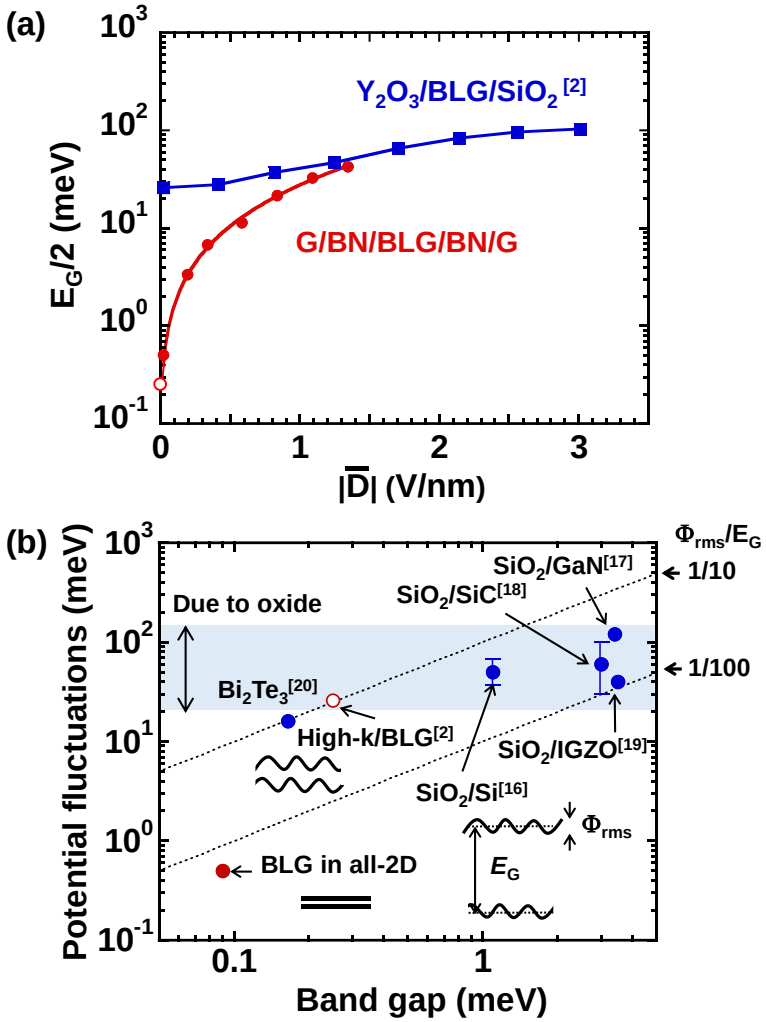

Figure 7.3 (a) $E_G/2$ as a function of $|\bar{D}|$.
(b) Potential fluctuations and band gap.

without the graphite back gate electrode becomes more obvious in the I_{on}/I_{off} data in **Fig. 7.1 (c)**. This indicates that the role of the graphite back and top gate electrodes is to apply uniform $\bar{D}$ as well as to screen charged impurities in SiO_2.

Figure 7.3 (b) summarizes the value of the band gap and Φ_{rms} due to charged impurities and fixed charges in various semiconductor/insulator systems. The value of potential fluctuations in SiO_2/Si, SiO_2/SiC and SiO_2/GaN were obtained by conductance method where the parallel conductance (G_p/ω) as a function of frequency is fitted with Gaussian distribution and the standard deviation is taken as potential fluctuations.[15-18] The potential fluctuations in SiO_2/IGZO were obtained from percolation conduction where the variance of potential barrier height represents potential fluctuations. [19] The potential fluctuations in Bi_2Te_3 were taken by measuring Dirac energy by STM and extracting the standard deviation by fitting the data with Gaussian distribution. [20] Although these values have been evaluated in different ways, a comparison is roughly possible because of their similar physical origins. The hatched region (20~100 meV) indicates the potential fluctuations inevitably induced by amorphous oxide insulators,

while the dotted and dot-dashed lines indicates Φ_{rms}/E_g = 1/10 and 1/100, respectively. In systems where semiconductor channels that have sufficiently large band gap compared to potential fluctuations from amorphous oxide insulators such as SiO_2/Si, the effect of potential fluctuations is negligibly small because sufficiently low off-current can be attained. Their main issue has been switching properties such as SS, which is directly affected by D_{it}. Therefore research in those systems have been focusing on improving oxide/semiconductor interface quality to reduce D_{it}. For small-gap semiconductors and topological insulators [20] the effect of potential fluctuations due to amorphous oxide insulators is more prominent. In BLG, it results in non-negligible variation of Fermi level and spatial uniformity of band gap, leading to high off-current. This issue was eliminated by using *h*-BN instead of amorphous oxide gate stack to reduce potential fluctuations. It can be seen that assembly of van der Waals layered heterostructure can be a promising regime for studying physical properties where resolution of small energy (a few meV) is required.

7.4 Current saturation

Drain current saturation at high drain voltage can be observed in conventional MOSFETs where the semiconductor channel has sufficient band gap. When drain voltage is comparable to gate voltage, the potential around the drain end approaches zero, reducing channel formation by inversion in that area. This is known as "pinch-off" which results in current saturation as the conductivity of area in drain end does not increase and it limits the total conductivity of FET.

Current saturation was investigated in all-2D heterostructure BLG-FET at maximum attainable band gap of 90 meV (**Fig. 7.4**). Saturation was not observed. This may be because band gap is too small, such that drain potential could easily induce carriers around drain end. In BLG with oxide gate stack, current saturation was observed at $\bar{D}$ = -1.7 V/nm which should yield band gap about 170 meV. [21] Another possibility may be due to parasitic resistance in the device as top gate does not cover the entire channel and access region is presence.

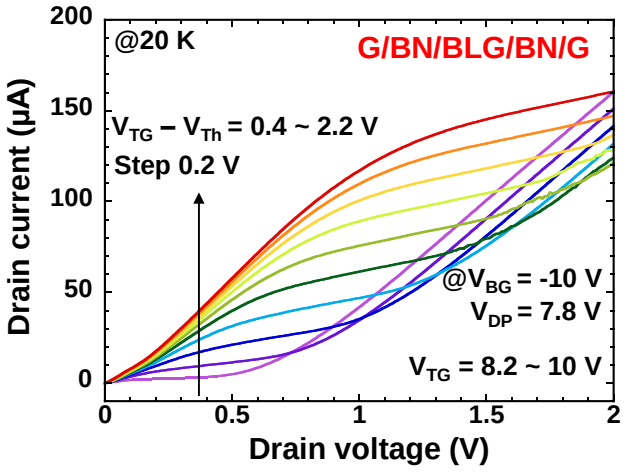

Figure 7.4 Drain current as a function of drain voltage.

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Chapter 8 Interfacial properties

Interfacial properties of *h*-BN/BLG in all-2D heterostructure BLG was evaluated by capacitance measurements and conductance method. Quantum capacitance was extracted from measured capacitance, and its features were used to evaluate band gap and the magnitude of disorder. Conductance method was employed to measure mobile carrier response at gap states. The interfacial properties of *h*-BN/BLG will be discussed.

8.1 CV measurement

To measure the capacitance of the limited active channel area in all-2D heterostructure, it is critical to reduce parasitic capacitance (C_{Para}). The parasitics of the measurement system were removed by performing open and short corrections before measuring the samples (the electrical correction), resulting in the noise floor of ~ 2 fF. In this experiment, the total capacitance between the top gate and source was measured, therefore C_{Para} observed is that between the top gate and source. However, the order of measured capacitance is of several 10 fF due to the limited area of top gate in the heterostructure, even though *h*-BN is thin. In this case, the contribution from the metal electrode pads is quite large because of their relatively large areas. Therefore, the limiting factor is the remaining frequency-dependent parasitics from the sample, not from the measurement system. These issues are critical for investigating the interface trap density by the conductance method, as frequency dependence resulted from the substrate will be included in frequency dependence resulted from the interface traps. Therefore, the quartz substrate was used to eliminate these problems. Frequency dependence of top gate capacitance (C_{TG}) measured at a voltage where there is no contribution of quantum capacitance is shown in **Fig. 8.1 (a)**. In devices fabricated on n^+-Si substrate, large frequency dependence in C_{TG} was observed because of SiO_2 behaving

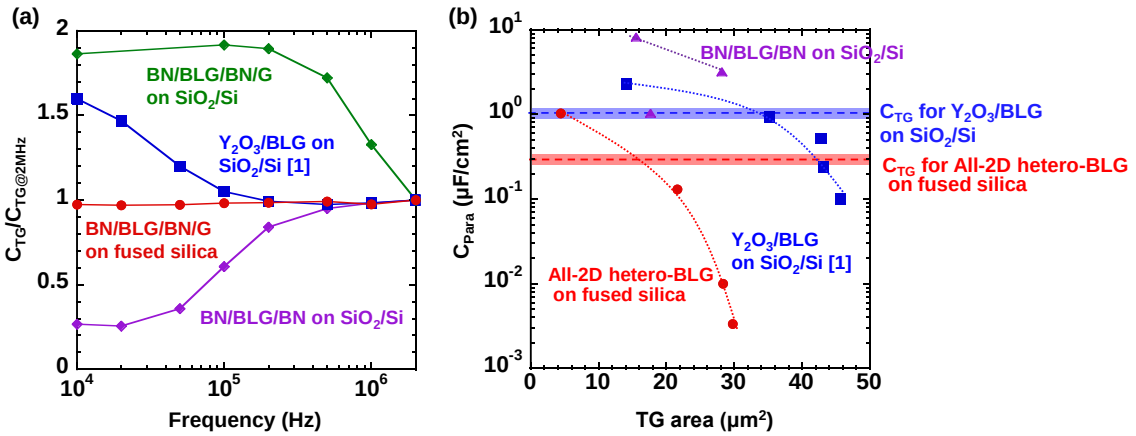

Figure 8.1 (a) Normalized C_{TG} as a function of frequency.

(b) C_{Para} for devices with different gate area on different substrates.

as a capacitor between the metal electrode pad and the n^+-Si substrate. On the other hand, for devices fabricated on a fused silica substrate, the frequency dependence in C_{TG} disappeared, resulting in negligible C_{Para} (**Fig. 8.1 (b)**).

The total capacitance (C_{Total}) between the top gate and source was measured at a frequency of 1 MHz by sweeping V_{TG} at each fixed V_{BG} in vacuum at 20 K, as shown in **Fig. 8.2 (a)**. Constant $\bar{D}$ lines, which indicate constant band structure, are depicted by black dotted lines. C_{Total} is composed of C_{TG} and quantum capacitance (C_Q) of BLG and C_{Para}, as shown by the simplified equivalent circuit in **Fig. 8.2 (b)**. C_Q is regarded as the energy cost of inducing carriers in BLG and is directly given as $C_Q = q^2$DOS at low temperature limit, where q and DOS are the elementary charge and the density of states, respectively.[2] When band gap is formed, C_Q at Dirac point decreases, resulting in the reduction of C_{Total}. C_{TG} was estimated to be 0.287 μF/cm². Here, C_Q was extracted at each $\bar{D}$ as a function of Fermi energy (E_F) by measuring C_{Total} along the constant $\bar{D}$ using C_{Para} as a fitting parameter, as shown in **Fig. 8.2 (c)**. Although C_{Para} is extremely small

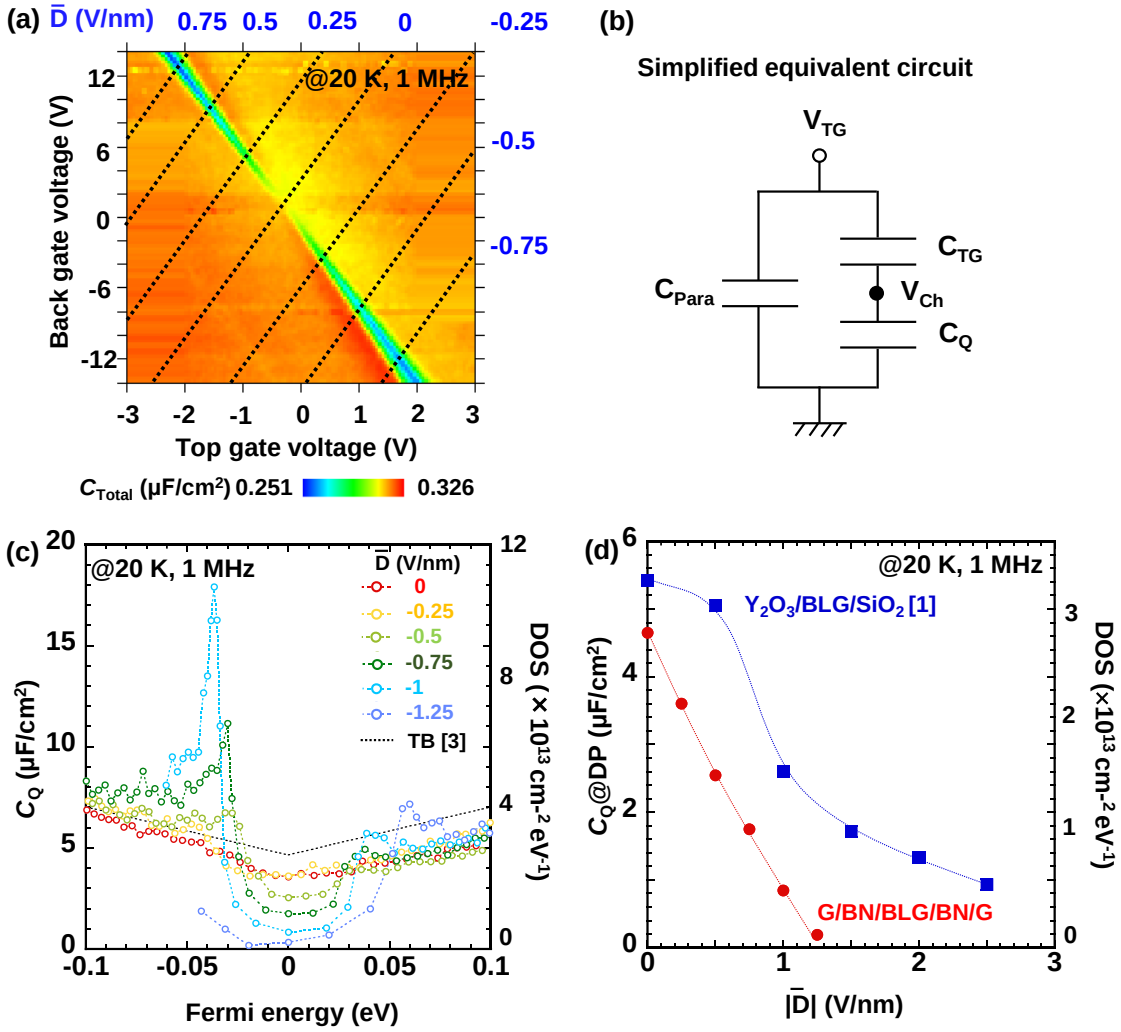

Figure 8.2 (a) Color plot of C_{total} measured at a frequency of 1 MHz at 20 K.

(b) Simplified equivalent circuit for CV measurement in BLG-FET.

(c) C_Q as a function of Fermi energy at $\bar{D}$=0 to -1.25 V/nm at 20 K.

(d) C_Q at Dirac point in **(c)** as a function of $|\bar{D}|$.

in devices fabricated on fused silica substrate, using C_{Para} = 1 fF which is equivalent to 3.361 nF/cm² for the top gate area of 29.75 μm², produced better fits. The extracted C_Q at $\bar{D}$ = 0 V/nm fits reasonably well with the theoretical value for bilayer graphene calculated by the tight-binding model. [3] E_F was calculated by the same method as in previously reported measurement. [1] E_F is expressed as $E_F = qV_{Ch}$ which can be calculated from a relation of serial capacitors given by

$$V_{Ch} = V'_{TG} - \int_0^{V'_{TG}} C'_{Total} / C_{TG} dV'_{TG}.$$

V_{TG}' and C_{Total}' are defined as $V_{TG}' = V_{TG} - V_{CN}$, where V_{CN} is the charge neutrality voltage for each V_{TG}, and $C_{Total}' = C_{Total} - C_{Para}$, respectively. As $\bar{D}$ increases, C_Q at Dirac point decreases due to band gap opening in BLG. In gapped BLG, van Hove singularities (vHS) are clearly observed at gap edges. Increasing disorder, such as charged impurities, results in more smearing of vHS and more disorder-induced states in the band gap, leading to gap closing at small $\bar{D}$. [4-6] The measured result shows two sharp vHS at both gap edges and a well-defined gap, indicating that the disorder strength is considerably reduced compared to the previous experiments on *h*-BN/BLG on SiO_2/Si and high-*k* Y_2O_3/BLG on SiO_2/Si devices where only one pronounced vHS was observed. [4, 6] The vHS observed were asymmetrical, which can be explained by the near-layer capacitance enhancement effect. [6]

C_Q at the Dirac point (C_Q@DP) can be used as a measure of the amount of disorder-induced states in the band gap. The C_Q@DP values for all-2D heterostructure and high-*k* Y_2O_3/BLG devices are plotted in **Fig. 8.2 (d)**. The result shows that for all-2D heterostructure device, C_Q@DP decreases rapidly even at small $\bar{D}$ and almost reaches zero compared to that in the high-*k* Y_2O_3/BLG device, [1] supporting that disorder was reduced in all-2D heterostructure. The other study also found that graphite top gate could further improve the resolution on integer quantum Hall states. [7] Since vHS are

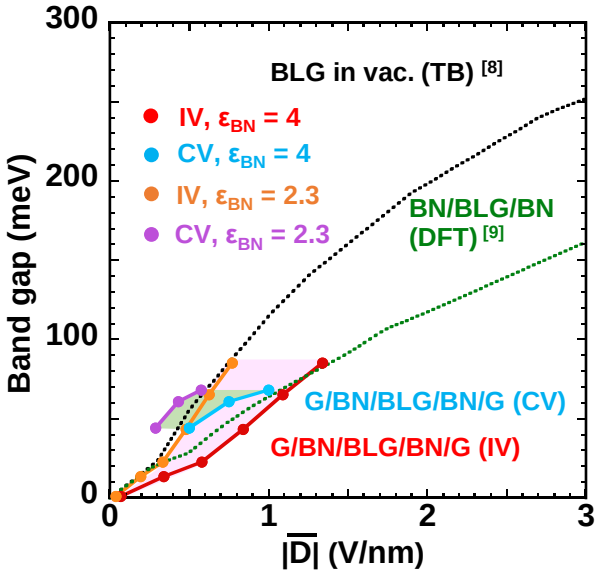

Figure 8.3 Band gap extracted from IV and CV measurements as a function of $|\bar{D}|$.

clearly observed, the size of the band gap opened at each $\bar{D}$ was evaluated by defining the band gap size as the energy difference between vHS at both sides. As shown in **Fig. 8.3**, the measured results from CV and IV in all-2D heterostructure devices are consistent even at low $\bar{D}$.

To investigate the behavior of disorder-induced states in the band gap, the temperature dependence of C_Q in the band gap of the all-2D heterostructure was observed in a different device as in **Fig. 8.2**. **Fig. 8.4 (a)** shows C_Q as a function of E_F measured at $\bar{D}$ = 1 V/nm at each temperature. At finite temperature, the C_Q of a 2D material is given by [10]

$$C_Q = q^2 g_{2D}\left[1+\frac{\exp(E_g/2k_BT)}{2\cosh(qV_{Ch}/k_BT)}\right]^{-1},$$

where $g_{2D} = g_s g_v m^*/2\pi\hbar^2$ is band-edge DOS, which was chosen from experimental value, and k_B is Boltzmann constant. g_s and g_v are spin and valley degeneracy factors, respectively, and m^* is effective mass. From the equation, temperature dependence of C_Q in band gap is expected. C_Q@DP is plotted as a function of temperature in **Fig. 8.4 (b)**. Only the data in the high temperature range could be fitted by equation for C_Q given above. The temperature dependence of C_Q@DP measured suggests contribution from a different mechanism at low temperature range. The transition in dominant mechanism in C_Q@DP seemed to be in the same temperature range as σ@DP. It was found that adding the NNH term using E_0 measured at the same $\bar{D}$ to equation for C_Q resulted in all the calculated values being fitting with the measured data well at all temperatures, as shown in **Fig. 8.4 (b)**. This indicates that a small amount of disorder-induced states still exists in the band gap.

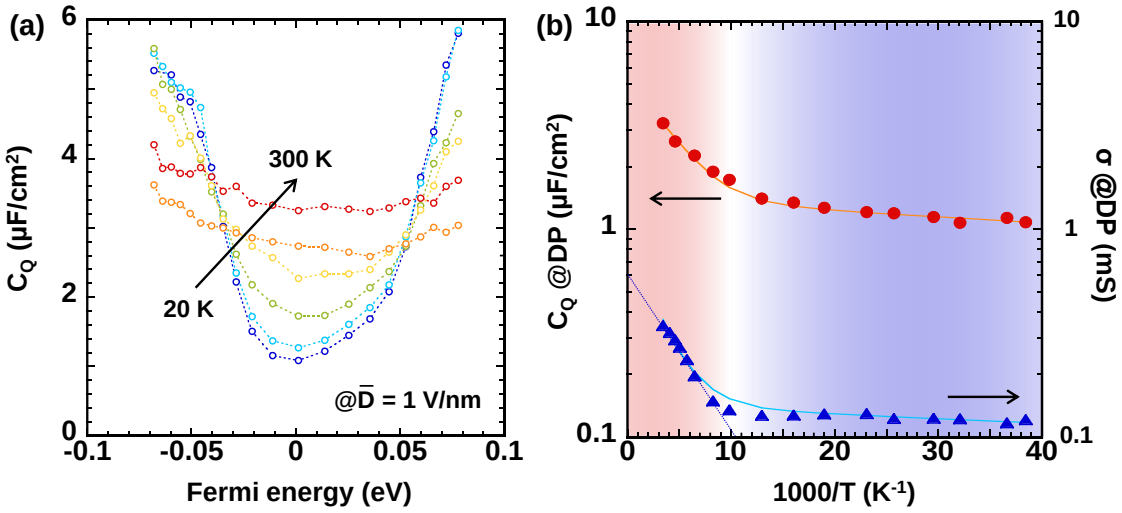

Figure 8.4 (a) C_Q measured at $|\bar{D}|$ = 1 V/nm as a function of Fermi energy from 20 K to 300 K.

(b) C_Q at Dirac point in **(a)** and σ at Dirac point of the same device at the same $|\bar{D}|$ as a function of inverse temperature. Solid lines are fits.

8.2 Conductance method

Temperature dependence of C_Q at Dirac point observed in **Fig. 8.4 (b)** suggests the presence of disorder-induced states in the band gap. Electrical response of disorder-induced states in the band gap in all-2D BLG FET can be investigated by conductance method. In conductance method [11] capture and emission process of mobile carriers trap levels in the band gap can be detected as a deviation from the ideal carrier response seen in frequency dependence of C_{Total}, allowing extraction of Gp/ω for determining D_{it}.

The frequency dependence of C_{Total} measured along the constant $\bar{D}$ = -1.25 V/nm (band gap ~ 90 meV) in a different device is shown in **Fig. 8.5**. Despite the hint of presence of disorder-induced states in the band gap, no frequency dependence of C_{Total} was observed in the frequency range of 10 kHz to 2 MHz. This suggests that D_{it} at 90 meV band gap is undetectable in the present frequency range, and *h*-BN/BLG interface in all-2D heterostructure is electrically inert. On the other hand, for all-2D heterostructure devices with bubbles in the BLG channel (**Fig. 8.6 (a)**), a frequency dependence in C_{Total} was clearly observed, as shown in **Fig. 8.6 (b, c)**. This indicates the possibility of detecting D_{it}. In parallel conductance extracted from the equivalent circuit, the left shoulder of conductance peaks was observed in the high frequency region as shown in **Fig. 8.6 (d)**, suggesting that the time constant is faster than the measurable range in this experiment. Therefore D_{it} could not be extracted quantitatively. However, the result shows the response of C_{it} which is consistent to the frequency response of C_{total}, supporting the interpretation of the data. The reason for fast time constant is probably due to the present band gap opened using *h*-BN as insulators being small compared to the maximum band gap of ~300 meV in high-*k* Y_2O_3/BLG device. [1] The clear observation of the mobile carrier response in devices with bubbles in the BLG channel validates the interpretation of the absence of a frequency dependence in **Fig. 8.5**.

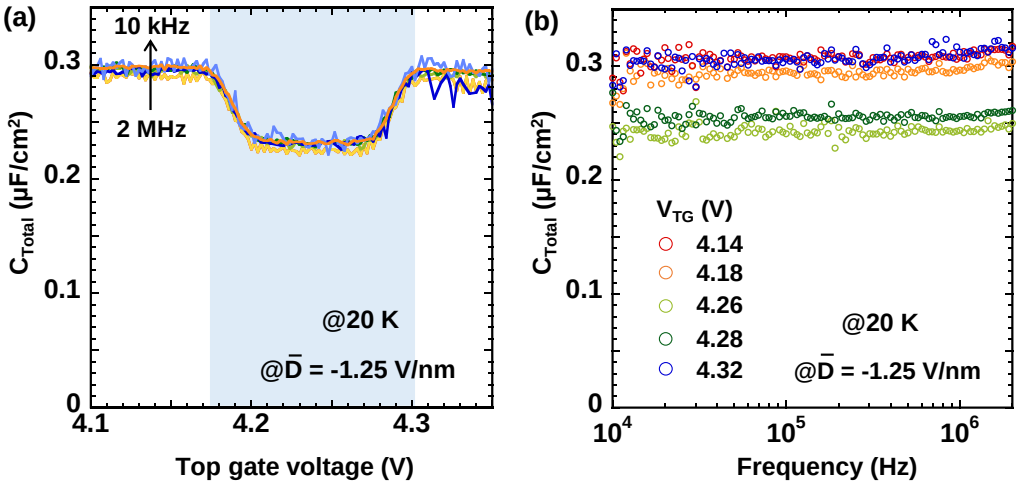

Figure 8.5 (a) C_{Total} as a function of V_{TG} measured at constant $\bar{D}$ = -1.25 V/nm at 20 K. It should be noted that VBG is also changed to maintain constant $\bar{D}$.
(b) C_{Total} as a function of frequency measured at each VTG in **(a)**.

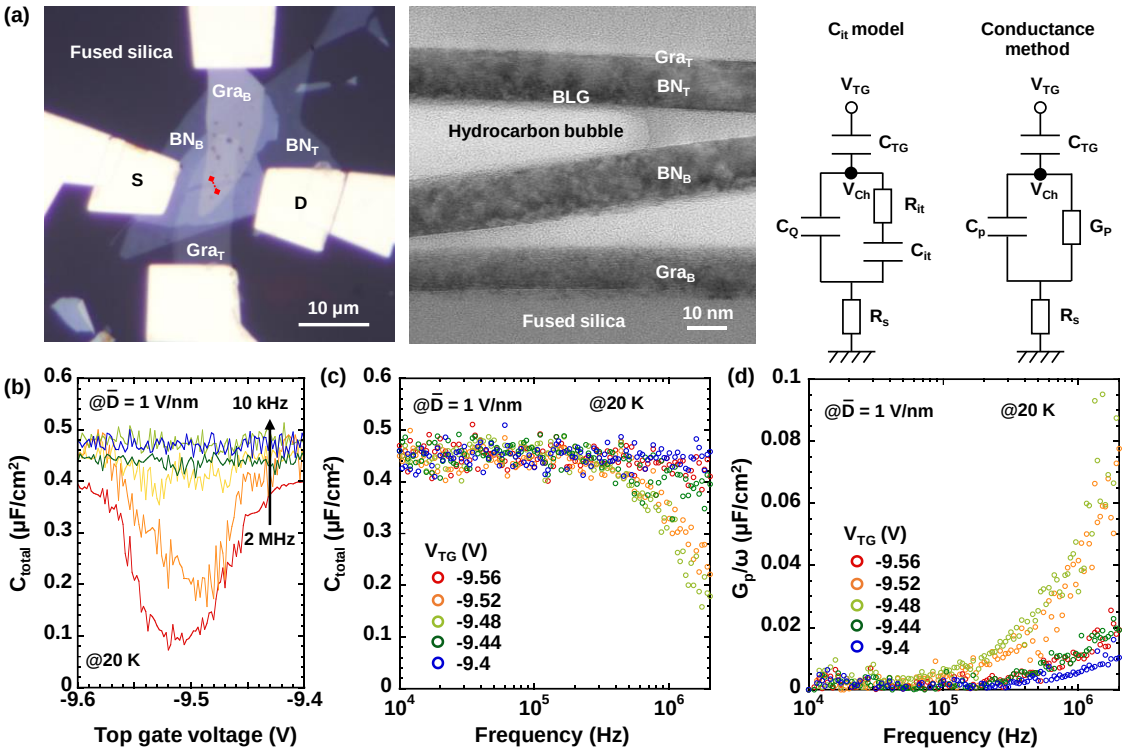

Figure 8.6 **(a)** Optical image of all-2D-heterostructure BLG-FET with bubbles in the channel area. A cross section TEM image taken along the red dotted line in (a) is shown in the right.

(b) C_{Total} as a function of V_{TG} measured at constant $\bar{D}$= 1 V/nm in **(a)** at 20 K. V_{BG} is also changed to maintain constant $\bar{D}$.

(c) C_{Total} as a function of frequency extracted from C_{Total} measured at each gate voltage in **(b)**.

(d) G_p/ω as a function of frequency extracted from total impedance measured at each gate voltage in **(b)** using equivalent circuits shown above.

8.3 Summary & discussion for FET application

Up until this point, it has been demonstrated that device properties can be significantly improved in all-2D heterostructure BLG-FETs compared to *h*-BN-encapsulated BLG on SiO_2/Si as well as high-*k* Y_2O_3/BLG/SiO_2. For the transfer characteristics at 20 K, I_{on}/I_{off} reached 4.6×10^5 with the off-state resistivity of ~5 GΩ even at band gap of 90 meV. For *h*-BN/BLG interface, nondetectable amount of D_{it} and two sharp vHS suggests that the 2D heterointerface is electrically inert. These significant results are mainly attributed to the drastic reduction of the potential fluctuation to ~0.5 meV and hence the spatial uniformity of E_G. This quite low potential fluctuations can be achieved only in all-2D heterostructure BLG-FETs, not in conventional semiconductor systems with high-*k* gate stacks. Therefore, all-2D heterostructure BLG-FET is suitable for FET application in BLG.

To obtain high I_{on}/I_{off} at room temperature, maximum band gap opening at $|\bar{D}|$ = 3 V/nm is required. Currently, $|\bar{D}|$ = 3 V/nm is achievable only with amorphous high-*k* oxide. On the other hand, maximum $|\bar{D}|$ achievable by *h*-BN is limited to 1.4 V/nm due to small dielectric constant. Although combining high-*k* amorphous oxide with *h*-BN can provide $|\bar{D}| \geq 3$ V/nm, potential fluctuations due to charged impurities in high-*k* amorphous oxide will deteriorate I_{on}/I_{off}. To apply $|\bar{D}| \geq 3$ V/ nm while keeping potential fluctuations low, gate stack structure needs to be reconsidered, such as by combining *h*-BN with high-*k* single-crystal nanosheets, [12, 13] in which potential fluctuations may be reduced due to crystal periodicity.

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Chapter 9 Photoresponse in all-2D BLG hetero-FET

Using spatially uniform band gap and I_{off} suppression at small band gap, photodetection can be considered as potential application for all-2D heterostucture BLG-FETs. In this study, theoretically predicted phototransistor action for BLG was investigated in all-2D heterostucture BLG-FETs.

9.1 Device structure

It should be noted that phototransistor action mechanism predicted for BLG-FETs is based on phototransistor action in bipolar transistors. As shown in **Fig. 9.1**, source, top gate and drain region correspond to emitter, base and collector respectively. In bipolar transistor, electrons and holes are generated from light absorption in base region. Electrons are swept out of base region but holes accumulates in base region due to potential wall resulted from band structure. This lowers potential barrier for electrons in emitter, allowing more electron diffusion to collector through base region. If the thickness of base is much more than electron diffusion length in base region, all electrons from emitter will be loss to recombination in base and the phototransistor action will be lost. [1] Carrier diffusion length can be estimated from

$$L_D = \sqrt{D\tau}$$

where L_D is diffusion length, D is diffusion constant and τ is carrier lifetime. In phototransistor regime all potential drops occur at junction depletion regions, therefore in base region electrons are transported by diffusion, not drifting. In this case, diffusion is limited by recombination, so τ should be taken as recombination time. L, D, τ in BLG have been measured by pump-probe technique, and were reported as $D \sim 4250$ cm²/Vs, $\tau \sim 4$ ps. [2, 3] Using the reported values, L_D is estimated to be ~1.3 μm. In general, D can also be calculated from Einstein relation

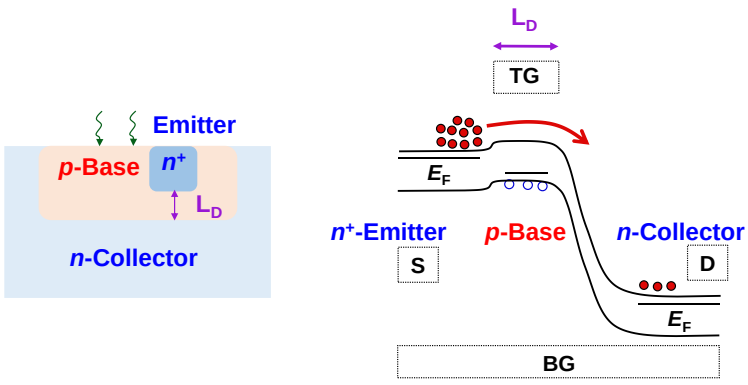

Figure 9.1 Phototransistor action in bipolar transistor. L_D denotes electron diffusion length in base region.

$$D = \frac{\mu k_B T}{q}.$$

Here, μ is carrier mobility, k_B is Boltzmann constant, T is temperature and q is elementary charge. In this case L_D is estimated to be ~83 nm at 10 K. In this study diffusion length estimated from pump-probe technique was used to compare with top gate length of BLG-FETs. Diffusion constant and recombination time measured in pump-probe technique was obtained in undoped BLG. In phototransistor regime, the electron diffusion length in BLG may be reduced due to hole accumulation under top gate region.

Halogen lamp with power of 150 W was used as a light source to observe photoresponse to visible light (**Fig. 9.2**). It was found that observation of time response in devices fabricated on fused silica was extremely difficult compared to devices fabricated on SiO_2/n^+-Si substrate despite similar transport characteristics. This suggests that optical heating can affect photoresponse. Therefore, fore photoresponse observation, devices were fabricated on SiO_2/n^+-Si substrate due to higher thermal conductivity compared to fused silica.

For optical transmission in top gate region, top gate electrode thickness has to be controlled. Transmittance of Ni and graphite for each thickness are shown in **Fig. 9.3 (a).** Transmittance was calculated from $T = \exp(-4\pi kt/\lambda)$ where k is extinction coefficient, t is thickness and λ is wavelength. Although Ni has lower optical transmittance than graphite of the same thickness, experimental control of thickness, position and gate length is easier for Ni. The measured thickness of Ni top gate electrode for each wire length (φ 0.5mm is used throughout this study) is plotted in **Fig. 9.3 (b)**. Ni thickness of 20 nm was chosen to allow optical transmission while maintaining electrical conductance.

BLG-FETs with Ni top gate and graphene top gate and varying top gate length were fabricated (**Fig. 9.4**). Devices with top gate length down to 1 μm shows I_{off} suppression at 10 K that is comparable to longer gate length (**Fig. 9.4 (a, b, d)**). Device with 0.25 μm long Ni top gate of shows higher I_{off} (degraded modulation) even when

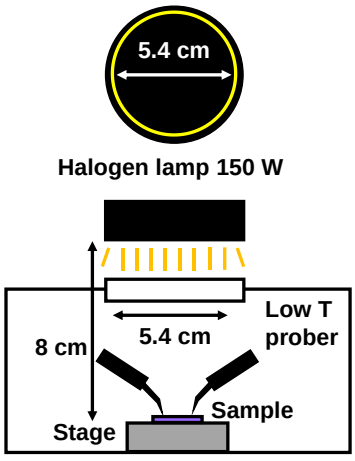

Figure 9.2 Measurement setup for observing photoresponse to visible light.

sufficient back gate voltage is applied to open band gap (**Fig. 9.4 (c)**). This could be because electrical conduction by NNH can occur more easily in short gate length, similar to current leakage in thin insulator. Moreover, the device with 0.25 μm long graphene top gate did not show I_{off} suppression (**Fig. 9.4 (e)**). This may be because the integrity of thin graphene created by top-down approach is difficult to determine with optical microscope. Although, phototransistor action is expected to be more prominent in devices with shorter top gate length with higher optical transmission, their I_{off} may be too large compared to the magnitude of photocurrent, making the results unreliable. High I_{off} also implies large disorder which may worsen the photoresponse. Therefore, photoresponse in devices with 5 μm long Ni, 1 μm long graphene, and 0.25 μm long Ni top gate will be discussed.

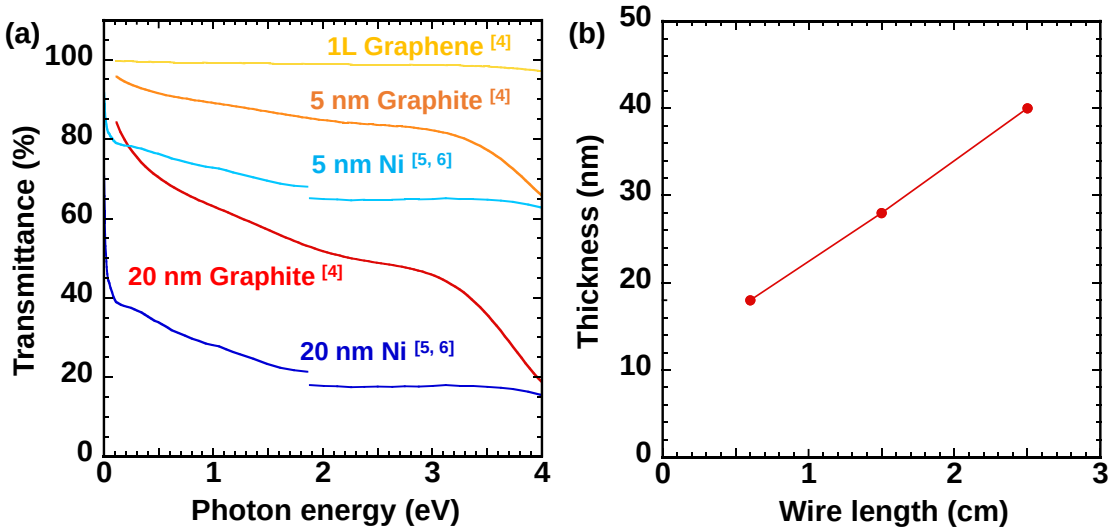

Figure 9.3 (a) Optical transmittance of graphene and Ni as a function of photon energy. **(b)** Ni top gate electrode thickness and wire length.

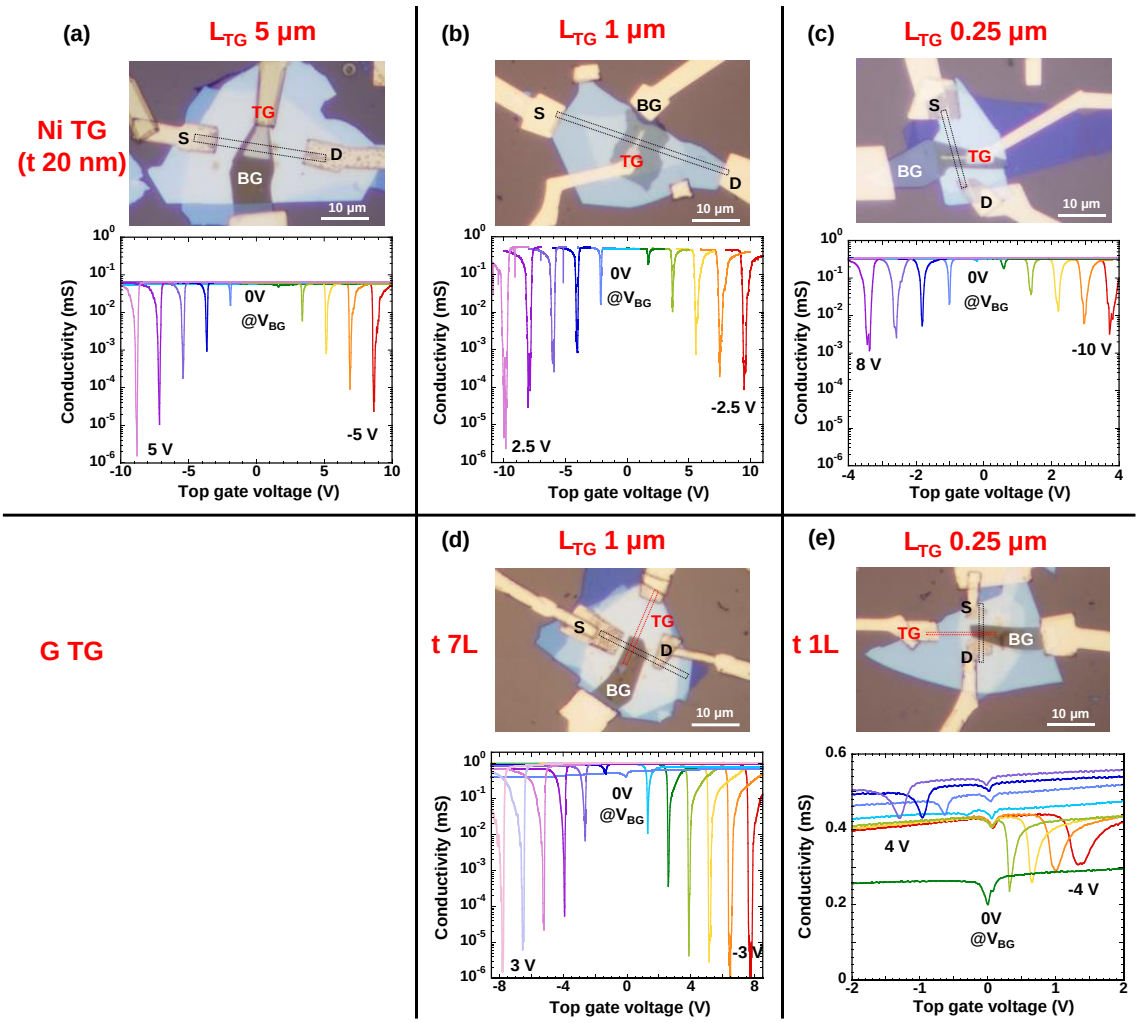

Figure 9.4 Optical images of devices with different top gate electrode material and length. Below each images are conductivity as function of top gate voltage measured at 10 K. Black dotted lines show outline of BLG. Red dotted lines show outline of graphene top gate. It should be noted that conductivity data of L_{TG} 0.25 μm GTG is in linear scale. Thickness of Ni top gate is 20 nm for all devices. Thickness of graphene top gate is shown on the left of optical image.

9.2 Basic photoresponse

First, basic photoresponse without phototransistor action in *h*-BN/BLG hetero-FETs was investigated in a device with Ni top gate with thickness of 20 nm and length of 5 μm (much longer than diffusion length) shown in **Fig. 9.4 (a)**. At 10 K photocurrent was generally observed in all top gate voltages (V_{TG}) for each back gate voltages (V_{BG}), but a distinct photoresponse was observed at Dirac point (DP) as shown in **Fig. 9.5 (a)**. In this condition, band gap is formed in top gate region, limiting total conductivity of the device. Moreover, in a device with Ni/Au (40 nm) top gate electrode with the same length, photoresponse at Dirac point for top gate region was not observed (**Fig. 9.5 (b)**). These results suggest that the observed photoresponse occurs in the top gate region, confirming optical transmission of top gate.

Next, the mechanism of the observed photoresponse will be discussed. The difference in conductivity when light was turned on (σ_{light}) and when light was turned off (σ_{dark}) for each V_{TG} and V_{BG} are plotted in **Fig. 9.6** along with color plot for conductivity in dark condition. When band gap is formed ($V_{BG} > 3$ V or < -3 V) $\sigma_{light} - \sigma_{dark}$ at some V_{TG} within band gap shows zero or negative value, denying the possibility for phototransistor action because phototransistor action should give positive photocurrent at all V_{TG} within band gap region. Color plot for σ_{light}-σ_{dark} is shown in **Fig. 9.7**. Unlike previous studies (**Fig. 3.1 (b), 3.2 (c)**) [7, 8], there was no symmetric photocurrent sign reversal about the DP, and at the boundary between pnp and ppp, suggesting that photovoltaic effect and photothermoelectric effect are not the dominant mechanism in present device. Moreover, photothermoelectric effect can only occur when there is sufficient thermal gradient, but in present study, light is illuminated uniformly on the device. This leaves only bolometric as only possible mechanism. To compare the results to previously reported bolometric effect in BLG-FET, [9] resistivity change and normalized values are plotted in **Fig. 9.8**. Unlike, previous research where photoresponse was measured as photovoltage by lock-

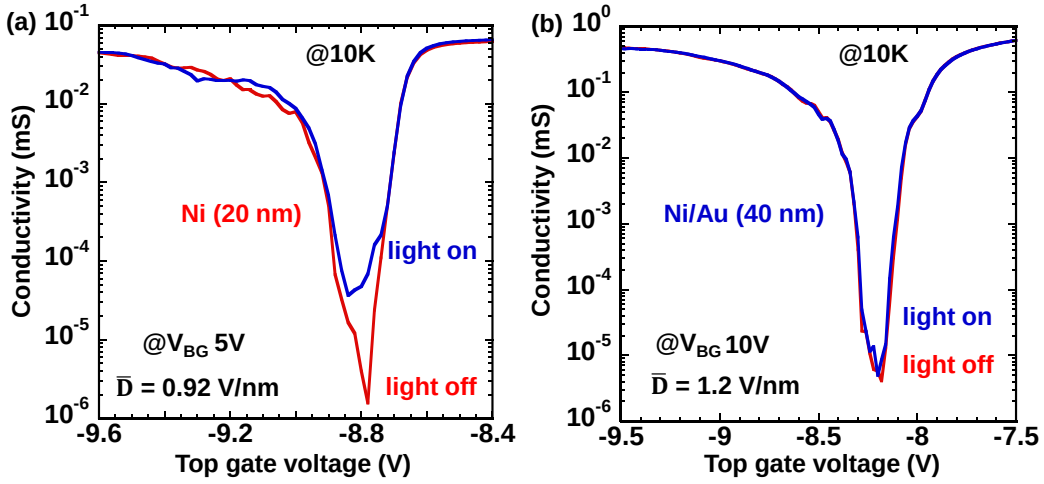

Figure 9.5 (a) Photoresponse of a device with Ni (20 nm) as top gate electrode.
(b) Photoresponse of a device with Ni/Au (40 nm) as top gate electrode.

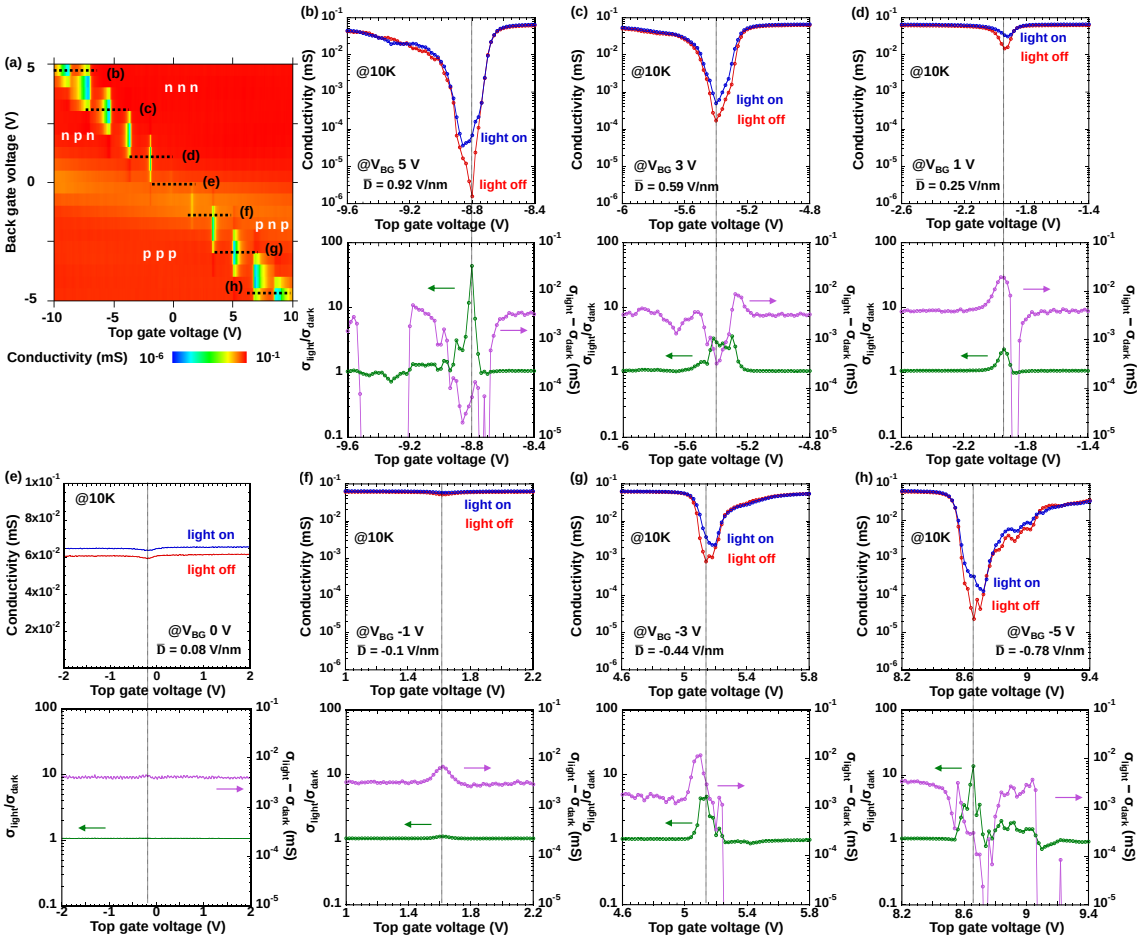

Figure 9.6 Photoresponse in device with 5 μm long Ni top gate. **(a)** Color plot for conductivity at dark state as function of V_{TG} and V_{BG}. **(b)-(h)** Conductivity with and without illumination, and their ratio and difference as a function of V_{TG} at V_{BG} from 5 V to -5 V shown as line cuts in **(a)**. $\bar{D}$ calculated at charge neutrality point for each V_{BG} is also shown.

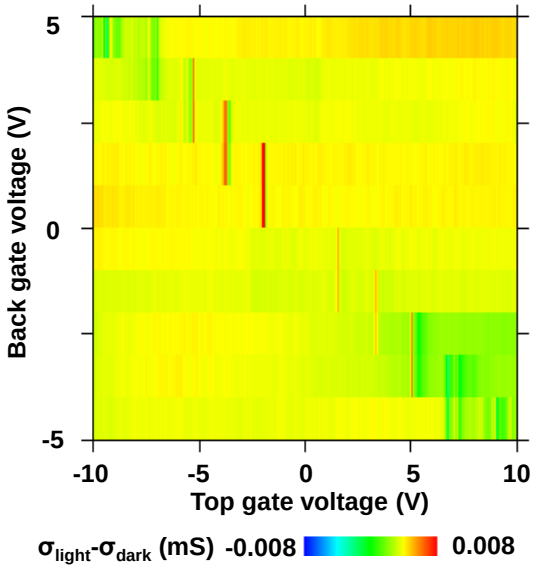

Figure 9.7 Color plot for conductivity difference in light and dark condition.

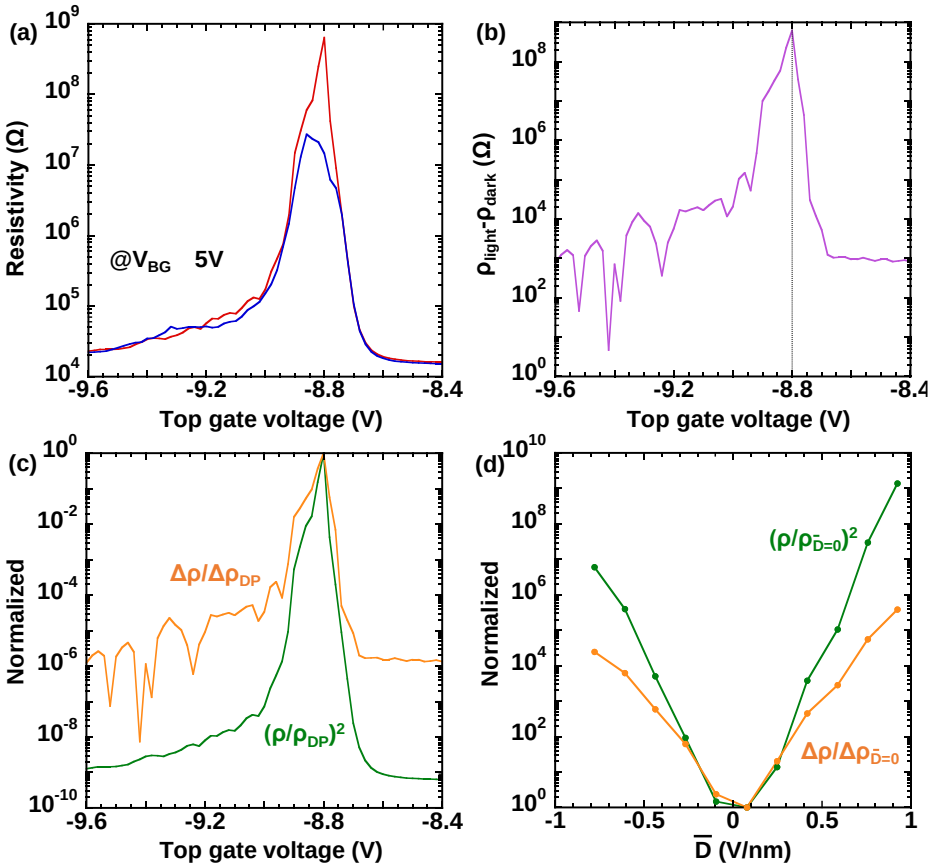

Figure 9.8 (a) Resistivity at 10 K as a function of top gate voltage.

(b) Resistivity change in **(a)** as a function of top gate voltage.

(c) Normalized resistivity and resistivity change taken from **(a)** & **(b)**.

(d) Normalized resistivity and resistivity change at DP as a function of $\bar{D}$.

in amp technique using AC voltage, photoresponse in this study was measured from DC current change at constant DC voltage. Therefore, photoresponse in this study was determined by resistivity change. The maximum change in resistivity was around DP (**Fig. 9.8 (b)**), which is similar to previous study (**Fig. 3.4 (b)**). On the other hand, normalized resistivity squared changed more rapidly than normalized resistivity change (**Fig. 9.8 (c, d)**), opposite to the trend in previous study but similarly suggesting that photoresponse was not photoconduction (**Fig. 3.4 (c, d)**).

Now, the bolometric response in the present device will be discussed and compared to previous study.[9] As shown in **Fig. 9.9 (a)**, resistivity change at DP increased as displacement field was increased. The change in resistivity was strongly dependent on temperature as shown in **Fig. 9.9 (b)** supporting that bolometric effect is dominant. Here, the resistivity change at DP for $\bar{D}$ = -0.65 V/nm, corresponding to V_{BG} = -4 V disappeared at 80 K, which is higher than in previous study (~15 K) shown in **Fig. 3.4 (e)**. This shows that the improvement in photoresponse can be a result of reduced charge impurities in *h*-BN/BLG heterostructure. Temperature dependence of resistivity at DP is shown in **Fig. 9.9 (c)**. The large change in resistivity in larger $\bar{D}$ can be describe by strong temperature dependence of resistivity at DP, especially at low temperature. At

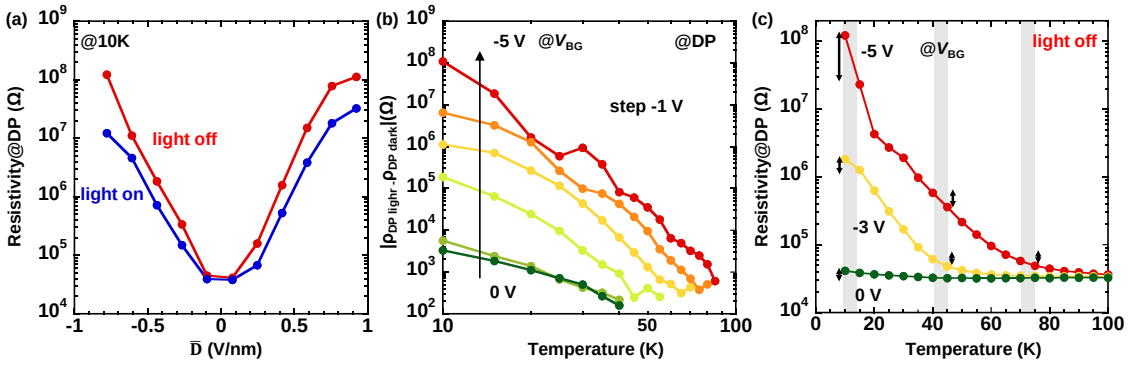

Figure 9.9 (a) Resistivity change at DP as a function of $\bar{D}$.

(b) Temperature dependence of resistivity change at DP.

(c) Temperature dependence of resistivity at DP.

low temperature, illumination from halogen lamp can increase the temperature of the sample as increase in stage temperature can be seen right after illumination. Temperature change is marked as grey hatched area and resulted the resistivity change is marked by arrows as shown in **Fig. 9.9 (c)**. At low temperature, the resistivity at DP became large and sensitive to temperature change. As temperature was increased, the resistivity at DP became lower and less sensitive to temperature change. This resulted in decreased resistivity change at higher temperature.

It should be noted that, $\sigma_{light} - \sigma_{dark}$ around DP is smaller than that at V_{TG} outside DP (**Fig. 9.6 (b, c, g, h)**). In fact, **Fig. 9.5 (a)** is an area denoted by orange dotted lines shown in **Fig. 9.10 (a)**. This is because the total conductivity of the device when V_{TG} is outside of DP is limited by ungated region (access region) and that means the observed photoresponse seen in range of V_{TG} in blue dotted lines in **Fig. 9.10** is from access region. $\sigma_{light} - \sigma_{dark}$ taken at V_{TG} where access region is dominant shows similar value to $\sigma_{light} - \sigma_{dark}$ taken at DP for $V_{BG} = 0$ V (**Fig. 9.6 (e)**).

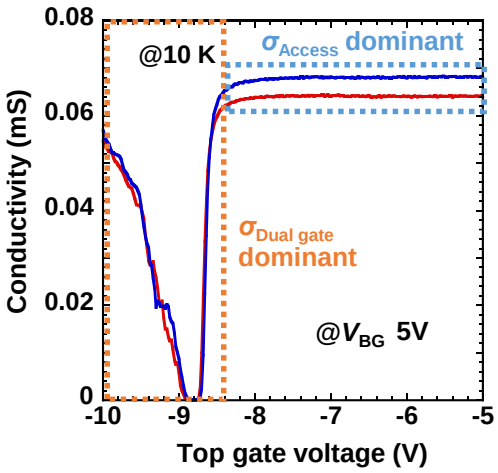

Figure 9.10 Conductivity as a function of top gate voltage in linear scale.

Interestingly, temperature dependence of σ_{light} - σ_{dark} at DP shows non-monotonous trend (**Fig. 9.11 (a)**). The trend of sensitivity of conductivity at DP to temperature change is similar to resistivity at DP (**Fig. 9.11 (b)**). However, the magnitude of conductivity change depends on the value of σ_{dark} at DP. At 10 K, σ_{dark} at DP for every V_{BG} is sensitive to temperature change. The condition that has largest σ_{dark} at DP shows largest σ_{light} - σ_{dark} at DP, i.e. σ_{light} - σ_{dark} at DP for V_{BG} = 0 V is larger than V_{BG} = -5 V. Around 40 K, σ_{dark} at DP for V_{BG} = 0 and -1 V loses sensitivity to temperature change, while σ_{dark} at DP for larger V_{BG} becomes higher, giving the rising trend of σ_{light} - σ_{dark} at DP seen in V_{BG} = -3 to -5 V. Around 80 K, only σ_{light} - σ_{dark} at DP for V_{BG} = -5 V is still sensitive to temperature change, showing σ_{light} - σ_{dark} at DP larger than at low temperature because σ_{dark} increased at higher temperature.

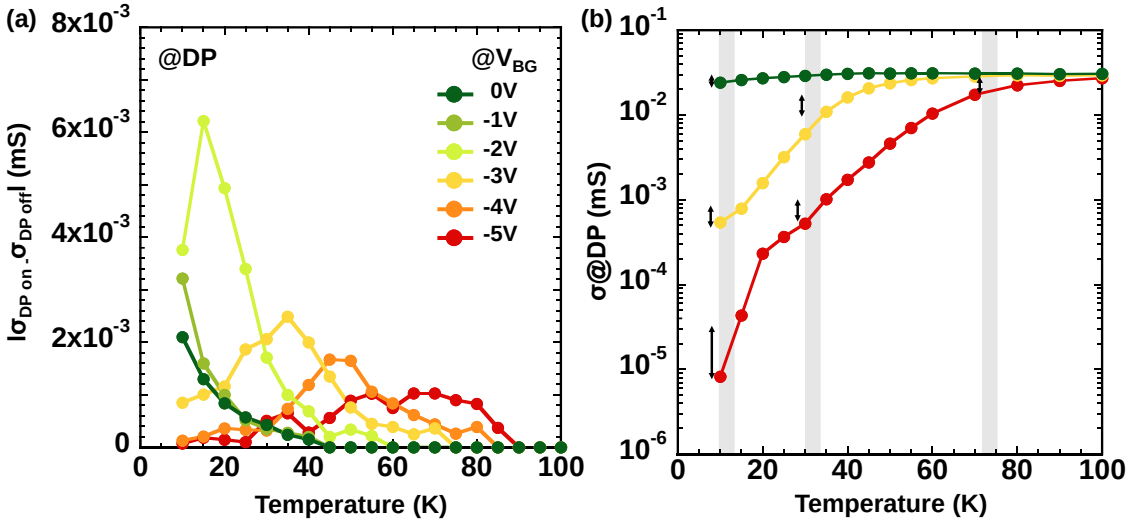

Figure 9.11 (a) Temperature dependence of conductivity change at DP. **(b)** Temperature dependence of conductivity at DP.

Time response at the DP for each V_{BG} was measured with time resolution of 20 ms (**Fig. 9.12**). Photoresponse curve was fitted with two time constants using

$$\sigma_{Rise} = \sigma_1(1 - \exp(-t/\tau_1)) + \sigma_2(1 - \exp(-t/\tau_2))$$

$$\sigma_{Fall} = \sigma'_1(\exp(-t/\tau_1)) + \sigma'_2(\exp(-t/\tau_2))$$

for rise time and fall time respectively. Here σ_1, σ_2, σ'_1, σ'_2 are prefactors, t is time τ_1, τ_2, τ'_1, τ'_2 are time constants. Similar time constants were observed in every back gate voltage (**Fig. 9.12 (a)**). Time constants for rising are 0.5 s, 3 s and for falling are 0.45 s, 3.41 s respectively. The faster time constant is considered as from bolometric response in device and the longer time constant can be considered as effect of temperature change of measurement chamber from optical heating.

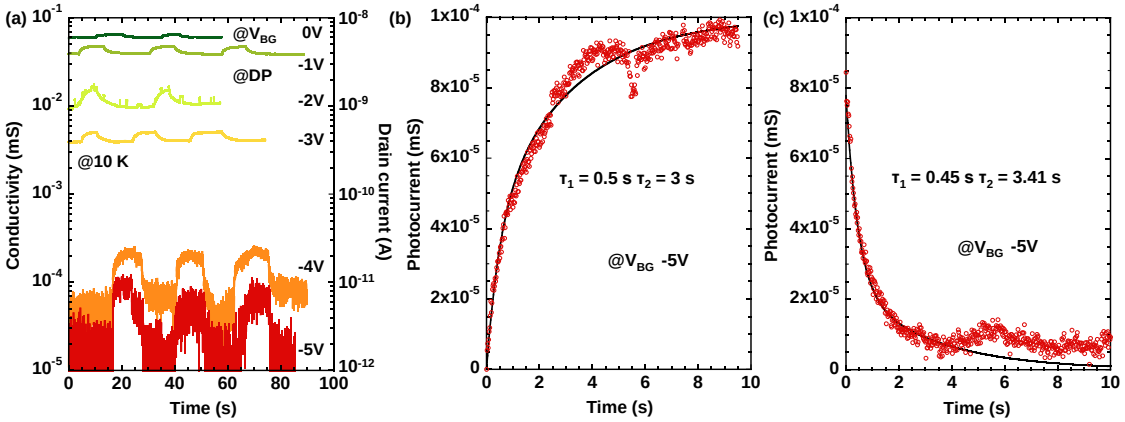

Figure 9.12 (a) Time response for conductivity at DP for each back gate voltage.

(b) Fitting for rise time in **(a)**.

(c) Fitting for fall time in **(a)**.

9.3 Photoresponse in 1 μm long Ni top gate

Photoresponse was investigated in devices with top gate electrode length comparable to diffusion length. Weak phototransistor action may manifest, resulting in different photoresponse behavior compared to bolometric response. First, photoresponse in device with 1 μm long Ni top gate electrode (**Fig. 9.4 (b)**) was investigated. Photoresponse results are shown in **Fig. 9.13**. Photocurrent in band gap region did not increase compared to bolometric response, and DP showed the most distinct response. However, unlike in device with gate length of 5 μm, (**Fig. 9.6 (b, c, g, h)**), continuous positive photocurrent was observed in V_{TG} within gapped region (**Fig. 9.13 (b, c, g, h)**). Maximum $\sigma_{light}/\sigma_{dark}$ were mostly at DP but for gapped BLG they appeared at V_{TG} slightly different from DP (**Fig. 9.13 (b, c, g, h)**). However, there were more than one DP at dark state (**Fig. 9.13 (b)**), possibly resulting in two peak of $\sigma_{light}/\sigma_{dark}$. Therefore, the observed $\sigma_{light}/\sigma_{dark}$ trend in this device was considered unreliable and will not be discussed further. Although temperature dependence of photoresponse in this device showed similar trend to the device with Ni top gate length of 5 μm, photoresponse was observed up to 100 K, which is slightly higher than bolometric response in device with Ni top gate length of 5 μm. Faster time constants for rise and fall compared to 5 μm long Ni top gate device were observed, as shown in **Fig. 9.14**, although the order of response time was considered to be too slow for quantum detectors. It is possible that optical transmission of 20 nm thick Ni top gate is still not enough to achieve phototransistor reaction. Therefore, photoresponse in a device with graphene top gate electrode with 1 μm length (**Fig. 9.4 (d)**), was also investigated.

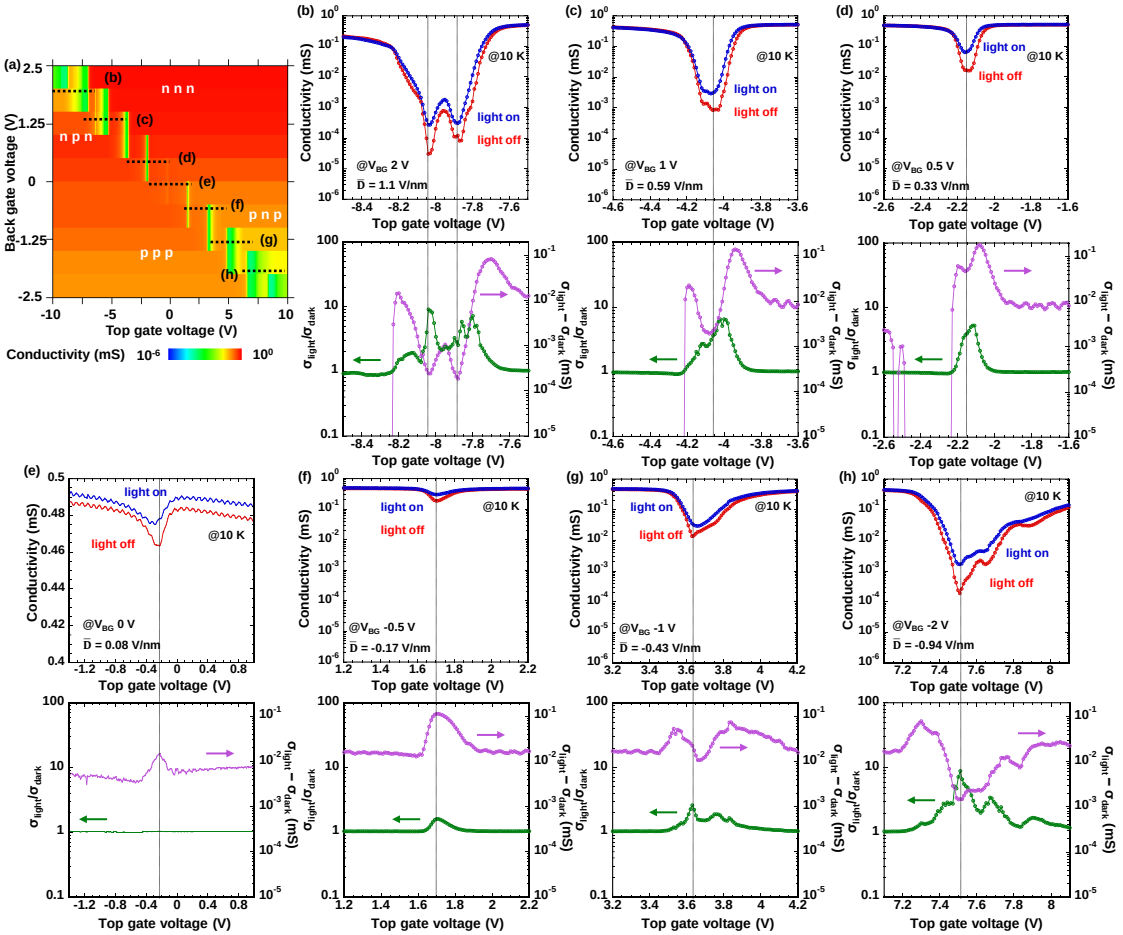

Figure 9.13 Photoresponse in device with 1 μm long Ni top gate. **(a)** Color plot for conductivity at dark state as function of V_{TG} and V_{BG}. **(b)-(h)** Conductivity with and without illumination, and their ratio and difference as a function of V_{TG} at V_{BG} from 2 V to -2 V shown as line cuts in **(a)**. $\bar{D}$ calculated at charge neutrality point for each V_{BG} is also shown.

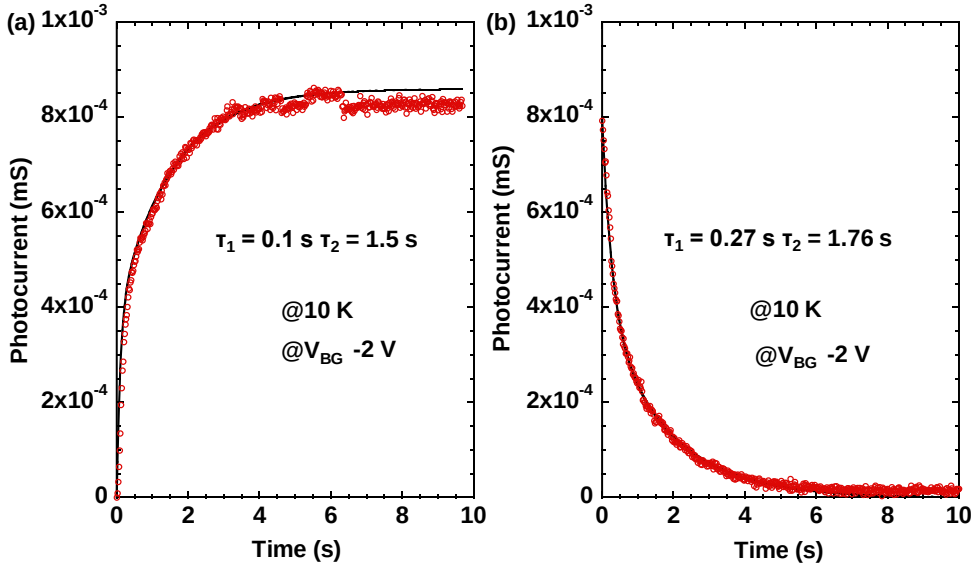

Figure 9.14 (a) Fitting for rise time.

(b) Fitting for fall time.

9.4 Photoresponse in 1 μm long graphene top gate

Although monolayer graphene has highest optical transmission, using monolayer graphene as top gate electrode can result in voltage drop in graphene due to quantum capacitance. Therefore, 7 layer graphene (estimated from optical contrast) with 1 μm width was used as top gate electrode. Heterostructure was fabricated by picking up 7 layer graphene by *h*-BN first, then picking up top gate *h*-BN, BLG, bottom *h*-BN and graphite, respectively. The fabricated device is shown in **Fig. 9.15**.

Photoresponse results are shown in **Fig. 9.16**. No significantly increased photocurrent in band gap was observed compared to 5 μm long Ni top gate device and 1 μm long Ni top gate device. However, photoresponse was observed up to 140 K with the same trend in temperature dependence of conductivity change as bolometric response (**Fig. 9.17**). Moreover, the response time was found to be faster than in 5 μm long Ni top gate device. Despite much shorter channel length and access region compared to 1 μm long Ni top gate device, similar time constants were observed, (**Fig. 9.18**). All response time measured at several V_{TG} within gap region were similar for every V_{BG}. Although minor differences were observed, markedly increase in photocurrent which is the main feature of phototransistor action was not observed. It can be concluded that photoresponse to visible light in devices with top gate length comparable to diffusion length are still dominated by bolometric effect.

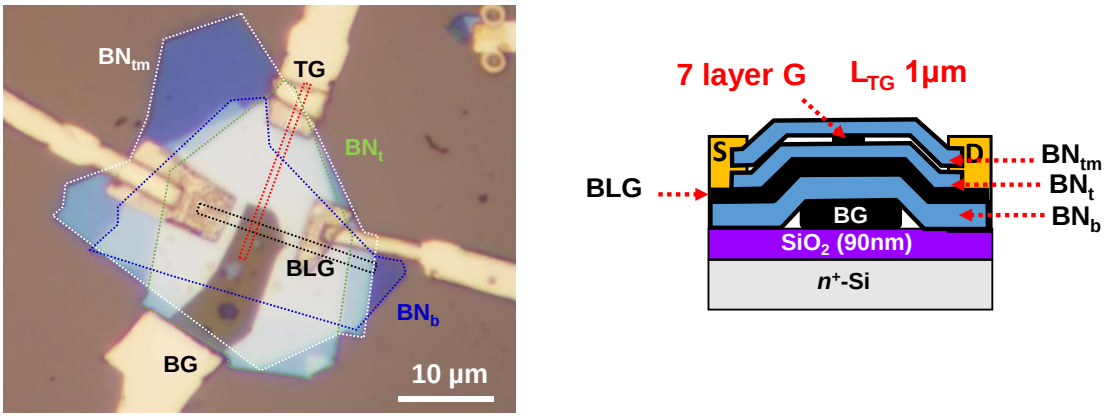

Figure 9.15 Optical image and schematic of a device with 1 μm long graphene top gate.

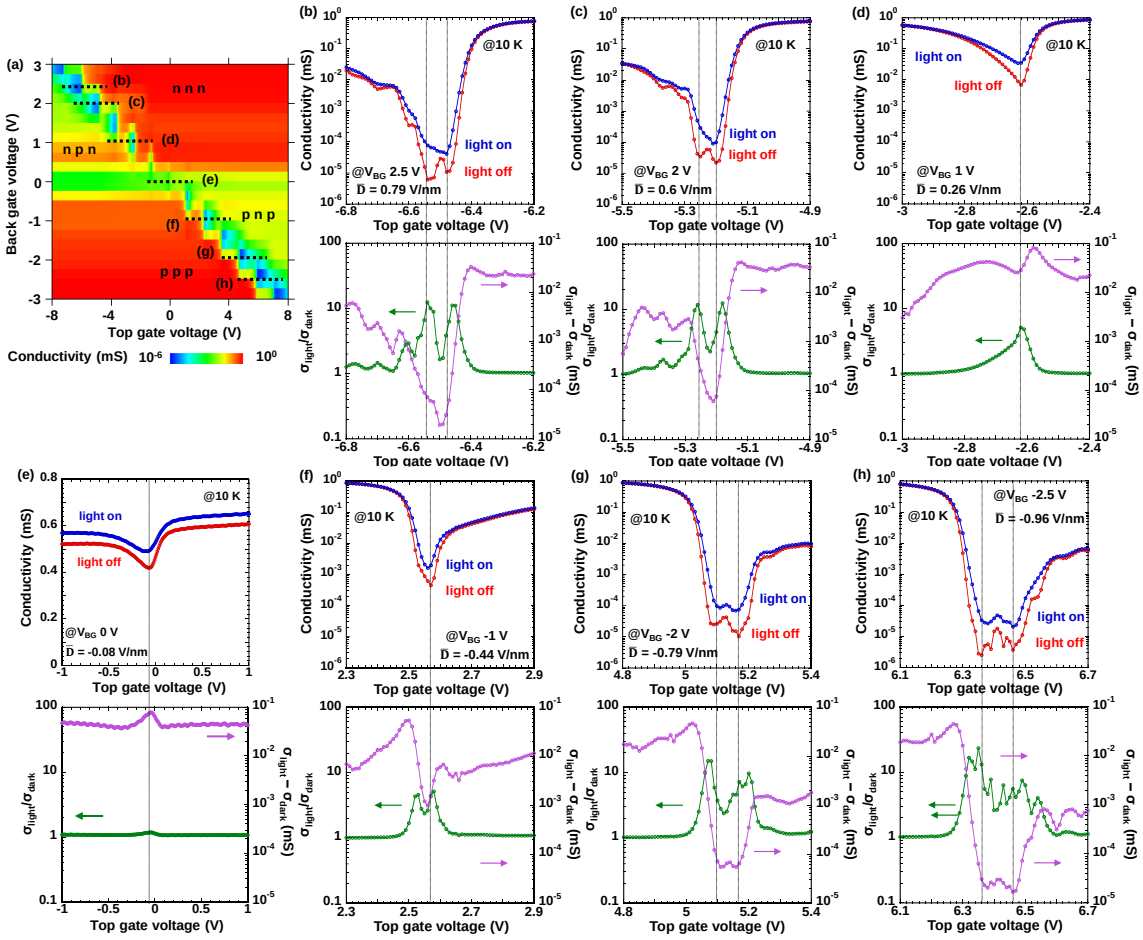

Figure 9.16 Photoresponse in device with 1 μm long graphene top gate. **(a)** Color plot for conductivity at dark state as function of V_{TG} and V_{BG}. **(b)-(h)** Conductivity with and without illumination, and their ratio and difference as a function of V_{TG} at V_{BG} from 2.5 V to -2.5 V shown as line cuts in **(a)**. $\bar{D}$ calculated at charge neutrality point for each V_{BG} is also shown.

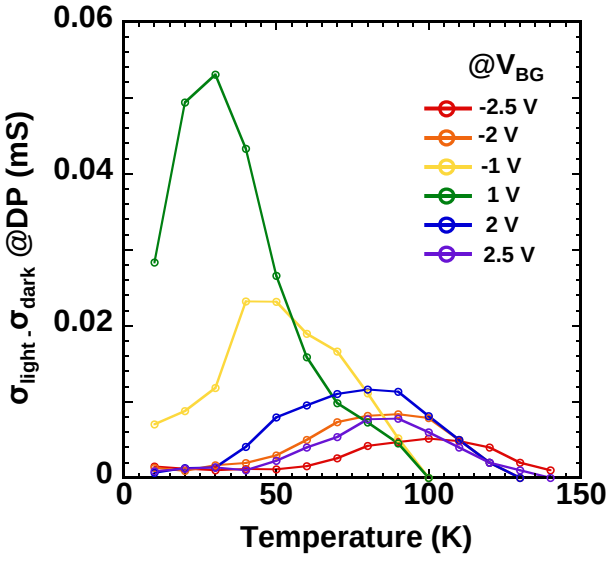

Figure 9.17 Temperature dependence of conductivity change at DP.

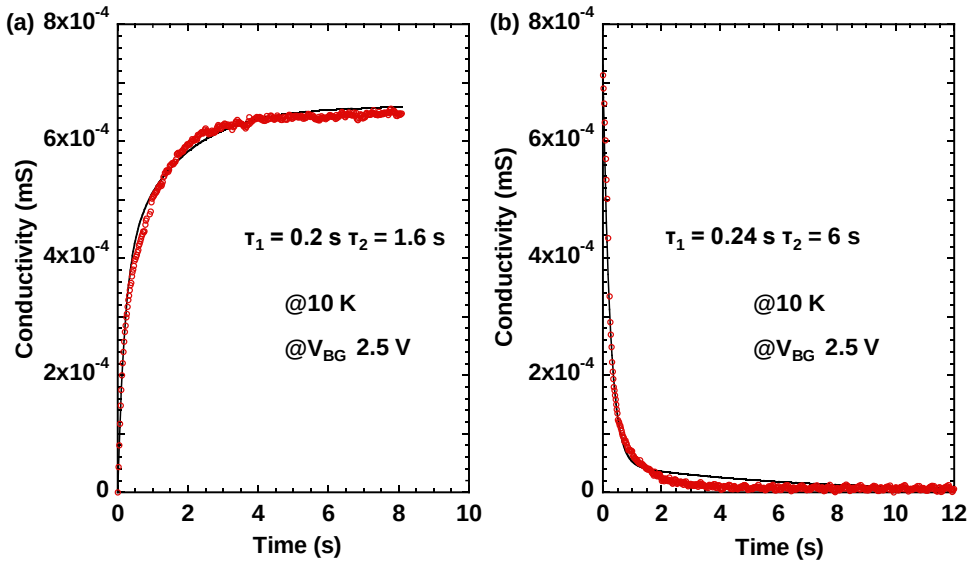

Figure 9.18 (a) Fitting for rise time.

(b) Fitting for fall time.

9.5 Infrared response in 1 μm long graphene top gate

It is possible bolometric response was observed due to optical heating caused by high intensity of halogen lamp. Moreover, wavelength dependence of photoresponse could not be investigated due to continuous wavelength of halogen lamp. In this study, blackbody furnace was attached to measurement chamber and infrared was illuminated on the device through band pass filter, which enables selection of wavelength. The setup is shown in **Fig. 9.19**. The temperature of blackbody was set to the maximum available, which is 1200℃ (1473 K). Four band pass filters were available; 1.54, 3.9, 10.6 and 12.84 μm. Spectral radiance of blackbody at 1473 K is shown in **Fig. 9.20**. Intensity of infrared at blackbody is obtained by integrating spectral radiance against wavelength. Intensity at a distance away from source can be calculated from inverse square law, given by

$$I = P/4\pi r^2.$$

Here, I is intensity, P is power and r is distance. Now, intensity at sample will be calculated while considering transmittance of ZnSe window and band pass filter. The total intensity at the sample without band pass filter is 83.61 W/m^2. Using top gate area of 1.85 μm^2, incident power at sample is 155 pW. For band pass 1.54 μm, incident power becomes 7.64 pW, which is 5% of total power with no filter. For 3.9, 10.6 and 12.84 μm, power is calculated to be 4.58, 1.65, 0.67 pW, respectively. The peak radiance at 1473 K is at 1.97 μm wavelength, therefore band pass filter 1.54 μm gives highest intensity for single wavelength incident light. It should be noted that the low temperature prober used in this experiment is different from one used to investigate response to visible light.

The temperature limit was down to 20 K and system was not designed for precise control of the probes temperature, which can result in larger temperature error.

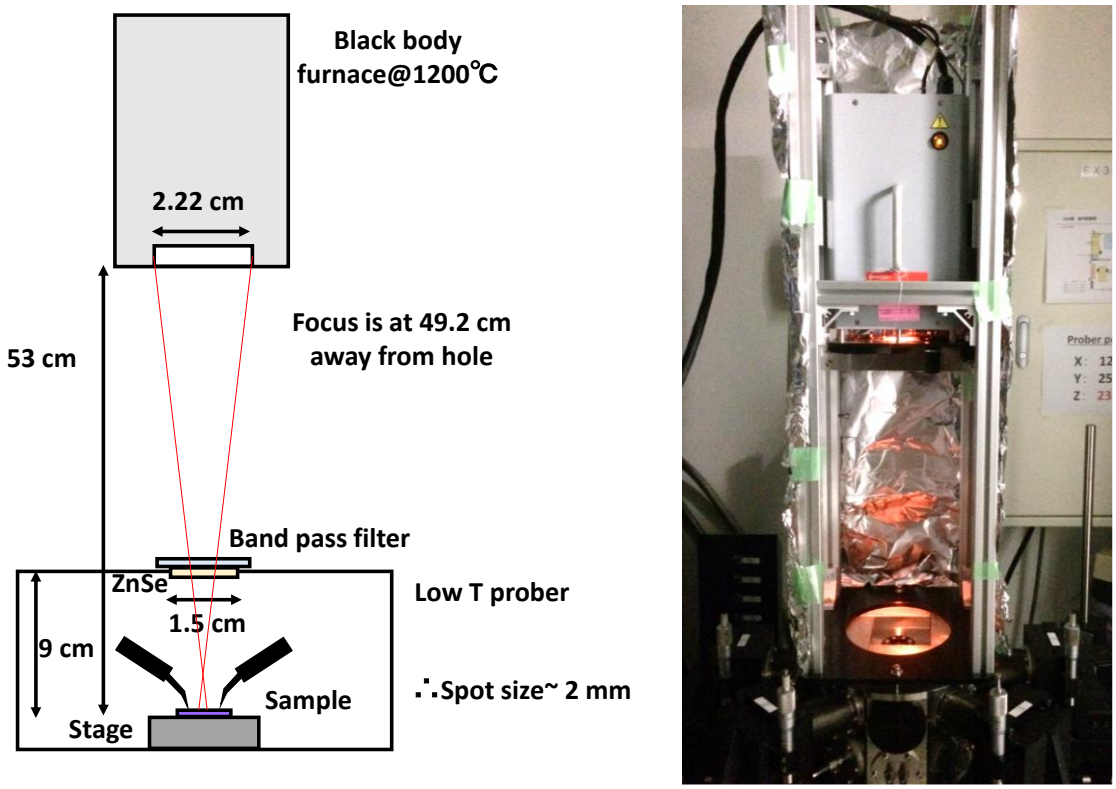

Figure 9.19 Setup for investigation of single wavelength infrared response using blackbody furnace.

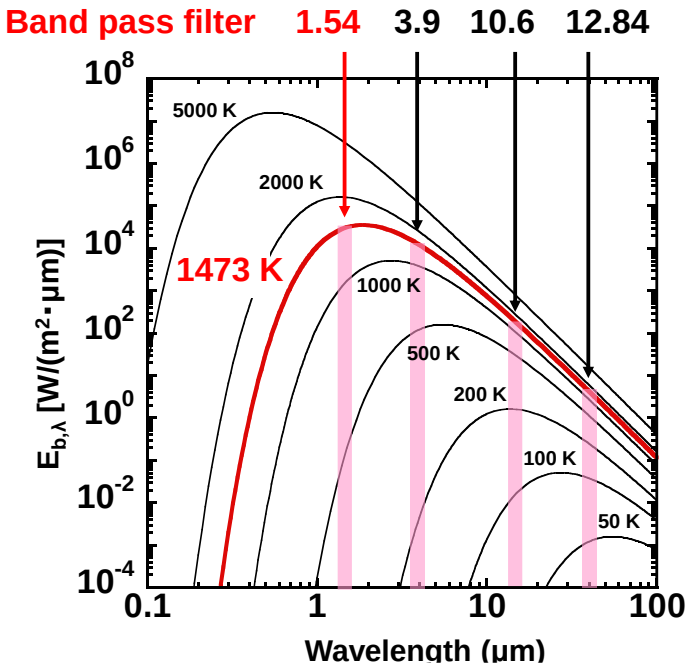

Figure 9.20 Blackbody spectral radiance and band pass filters.

Single wavelength infrared response was investigated in 1 μm long graphene top gate device. The photoresponse results are shown in **Fig. 9.21**. Photoresponse was observed only without band pass filter and with 1.54 μm band pass filter, although it would be ideal to be able to observe response with all band pass filters. This indicates that the incident power in this setup is quite low as no temperature change of sample stage is seen at the time of introducing infrared into the chamber. The response was very weak, but reproducible change was observed at DP (**Fig. 9.21 (a)**), confirming that devices with top gate length comparable or longer than diffusion length shows bolometric response to visible light and infrared, regardless of incident light power. Bolometric response taken as resistivity change at DP as a function of $\bar{D}$ was compared to bolometric response to halogen lamp (**Fig. 9.21 (b)**). It can be seen that resistivity change at DP was about one order of magnitude smaller, even disappearing at small V_{BG}. Temperature dependence of resistivity change at DP shows similar trend to bolometric response to halogen lamp but could only be observed up to 70 K due to smaller resistivity change (**Fig. 9.22**). Because photocurrent was extremely small, time response was noisy, and time constants could not be extracted.

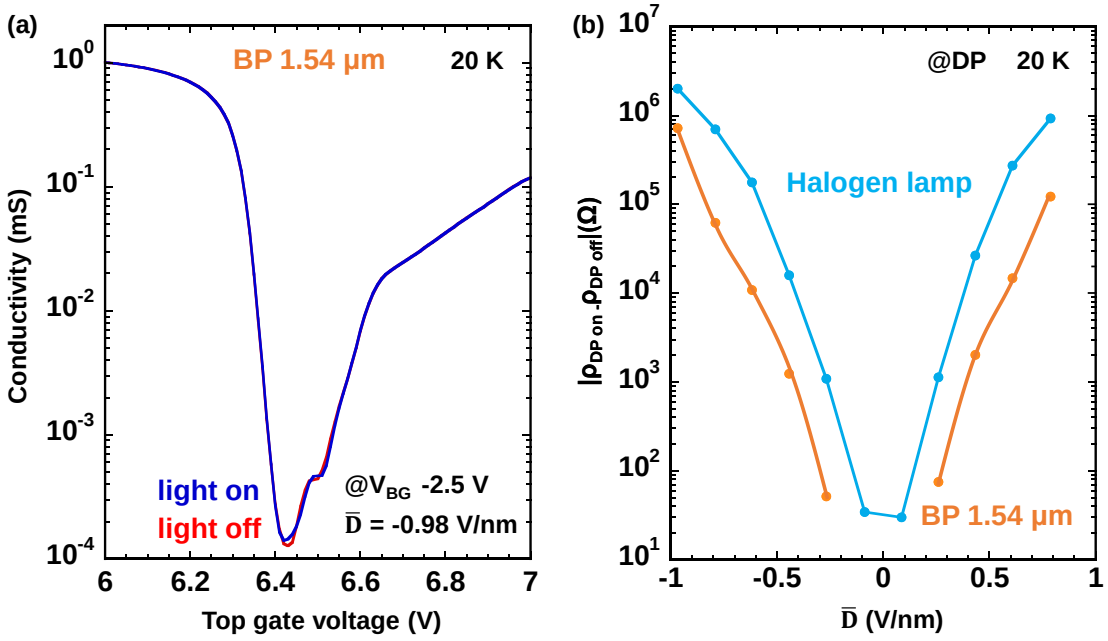

Figure 9.21 (a) Photoresponse to 1.54 μm infrared.
(b) Resistivity change at DP as a function of $\bar{D}$.

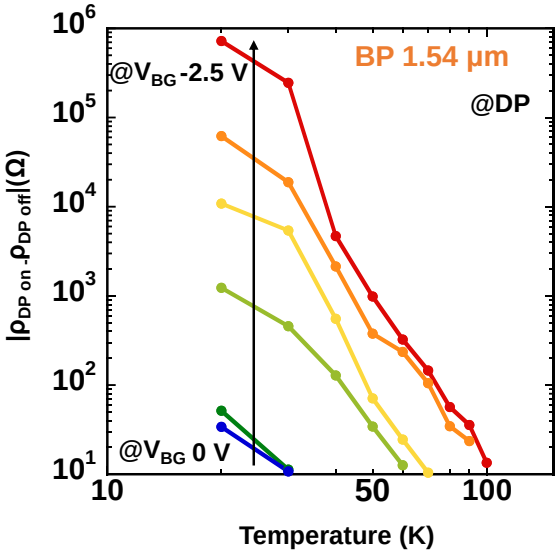

Figure 9.22 Temperature dependence of resistivity change at DP.

9.6 Photoresponse in 0.25 μm long Ni top gate

Photoresponse in 0.25 μm long Ni top gate device was investigated. Response to visible light was first observed. Photoresponse results for each V_{BG} are shown in **Fig. 9.23** and color plot for photocurrent is shown in **Fig. 9.24**. Significantly increased photocurrent can be seen on the right side of band gap region in boundary of npn and nnn (**Fig. 9.23 (b, c)**). Photocurrent in these areas is even larger than in access region (**Fig. 9.24**). As shown in color plot (**Fig. 9.24**), there was no photocurrent sign reversal at DP, denying the presence of photothermoelectric effect at pn-junction and photovoltaic effect at BLG/metal contacts. Therefore, the newly observed photocurrent was associated with phototransistor action. Although significantly increased photocurrent should be observed in all V_{TG} in gap region, the results show increased photocurrent only on the right side of band gap region in boundary of npn and nnn. This will be further discussed.

Band gap and Fermi level can be estimated from the value of V_{TG} and V_{BG} by calculating the value of $\bar{D}$ and δD. $\bar{D}$ and δD are band gap and Fermi level expressed as normalized V_{TG} and V_{BG}. Band gap for calculated $\bar{D}$ was taken from temperature dependence measured as well as from quantum capacitance measurement (**Fig. 8.3**). In CV measurement Fermi energy can be calculated from each V_{TG} and V_{BG}, therefore Fermi level for calculated δD was taken from Fermi level calculated at the same δD in quantum capacitance measurement (**Fig. 8.2 (c)**). First, band gap and Fermi level were separately estimated in region with only back gate and dual gate (**Fig. 9.25 (a)**). Then Fermi levels of the two areas were aligned and conduction band and valence band were joined. Potential barrier height was taken as the shown in **Fig. 9.25 (b)**. This way, the band structure and potential barrier in phototransistor regime in dual gate BLG-FET can be estimated.

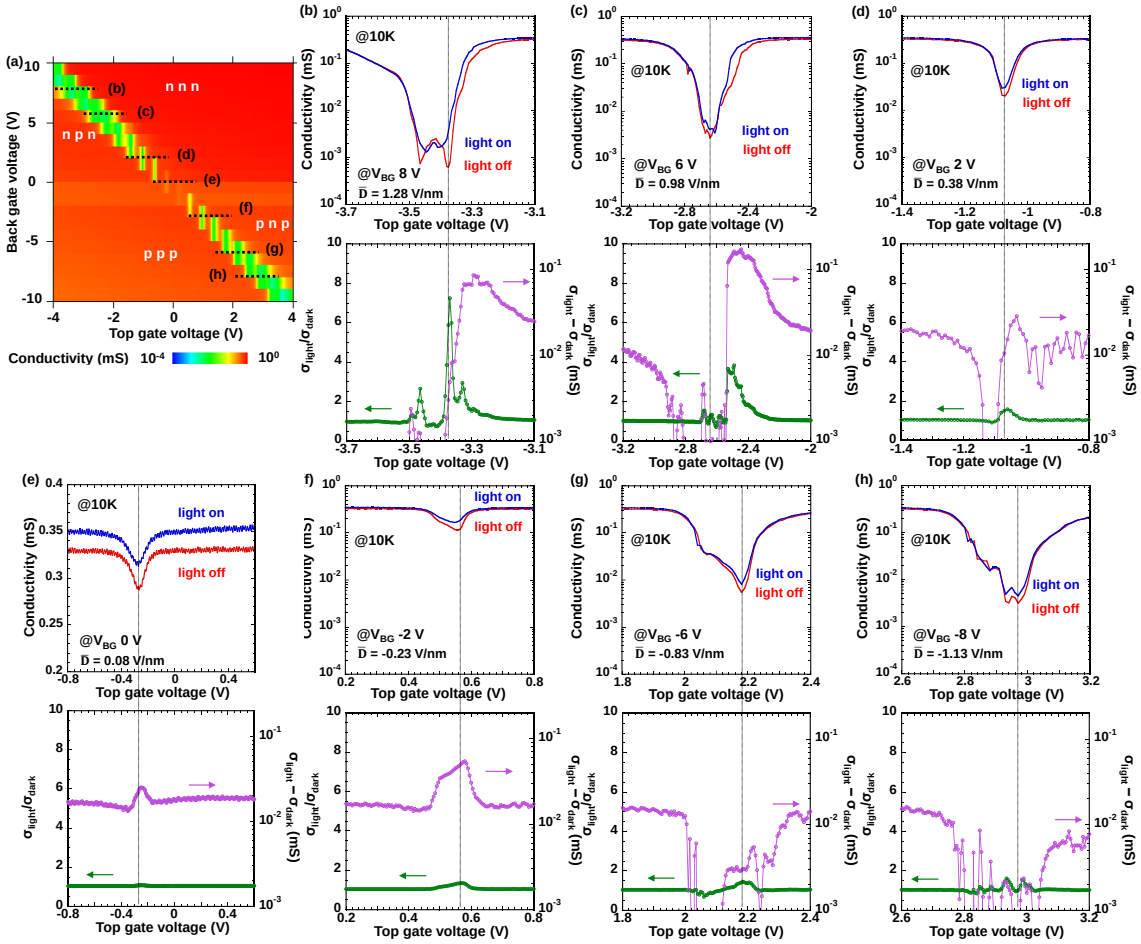

Figure 9.23 Photoresponse in device with 0.25 μm long Ni top gate. **(a)** Color plot for conductivity at dark state as function of V_{TG} and V_{BG}. **(b)-(h)** Conductivity with and without illumination, and their ratio and difference as a function of V_{TG} at V_{BG} from 8 V to -8 V shown as line cuts in **(a)**. $\bar{D}$ calculated at charge neutrality point for each V_{BG} is also shown.

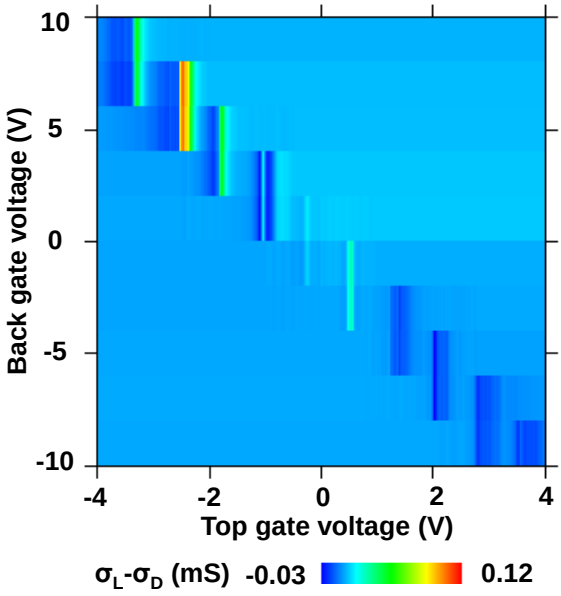

Figure 9.24 Color plot for conductivity difference in light and dark condition.

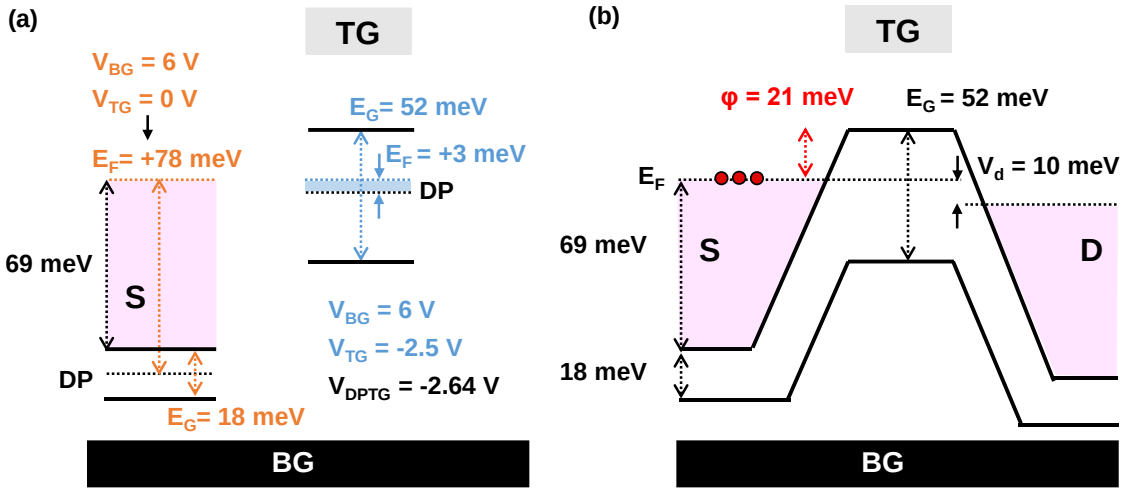

Figure 9.25 Estimation of band structure and potential barrier for phototransistor regime in dual gate BLG-FET. **(a)** Estimation of band gap and Fermi level in each area of the device. **(b)** Final band diagram of the device after aligning Fermi energy.

Now, potential barrier at different V_{TG} will be compared. V_{TG} that gives maximum σ_{light}-σ_{dark} for V_{BG} = 6 V (**Fig. 9.26 (a)**) corresponds to the situation where Fermi level is slightly above DP which makes potential barrier for carrier from source lower than the potential barrier when Fermi level is at DP (**Fig. 9.26 (b)**). This contradicts with theoretical prediction where higher potential barrier is expected to give higher responsivity. In this situation, dark current is lowest while barrier lowering by carrier accumulation under top gate region can amplify the photocurrent, giving the highest responsivity. [10] The result suggests that when V_{TG} = DP, the potential barrier was too high for carrier accumulation under top gate to lower the barrier to amplify photocurrent. On the other hand, when potential barrier is initially set to lower value, carrier accumulation under top gate can lower the barrier and amplify photocurrent. **Figure 9.27** shows that maximum photocurrent at V_{TG} marked by orange dot can be reproduced in dark condition by changing V_{TG} to the point marked by purple dot which gives the same conductivity. V_{TG} marked by purple dot corresponds to V_{TG} that gives lower potential barrier than V_{TG} marked by orange dot. Such behavior seems to be consistent with the mechanism of phototransistor action based on bipolar transistor.

Maximum photocurrent in V_{BG} = 8 V (**Fig. 9.23 (b)**) at similar position was smaller than in V_{BG} = 6 V. This similarly contradicts theoretical prediction where larger band gap which gives higher potential barrier should give higher responsivity. [10] From these observations, it is suggested that effect of potential barrier lowering by carrier accumulation in gate region may be too small for highest potential barrier in present device. Similar trend of photocurrent was not observed in negative V_{BG} (**Fig. 9.23 (g, h)**). This may be because their I_{off} was quite high compared to positive V_{BG} at the same $|\bar{D}|$. High I_{off} indicates more disorder which may have greatly diminished photoresponse in negative V_{BG}.

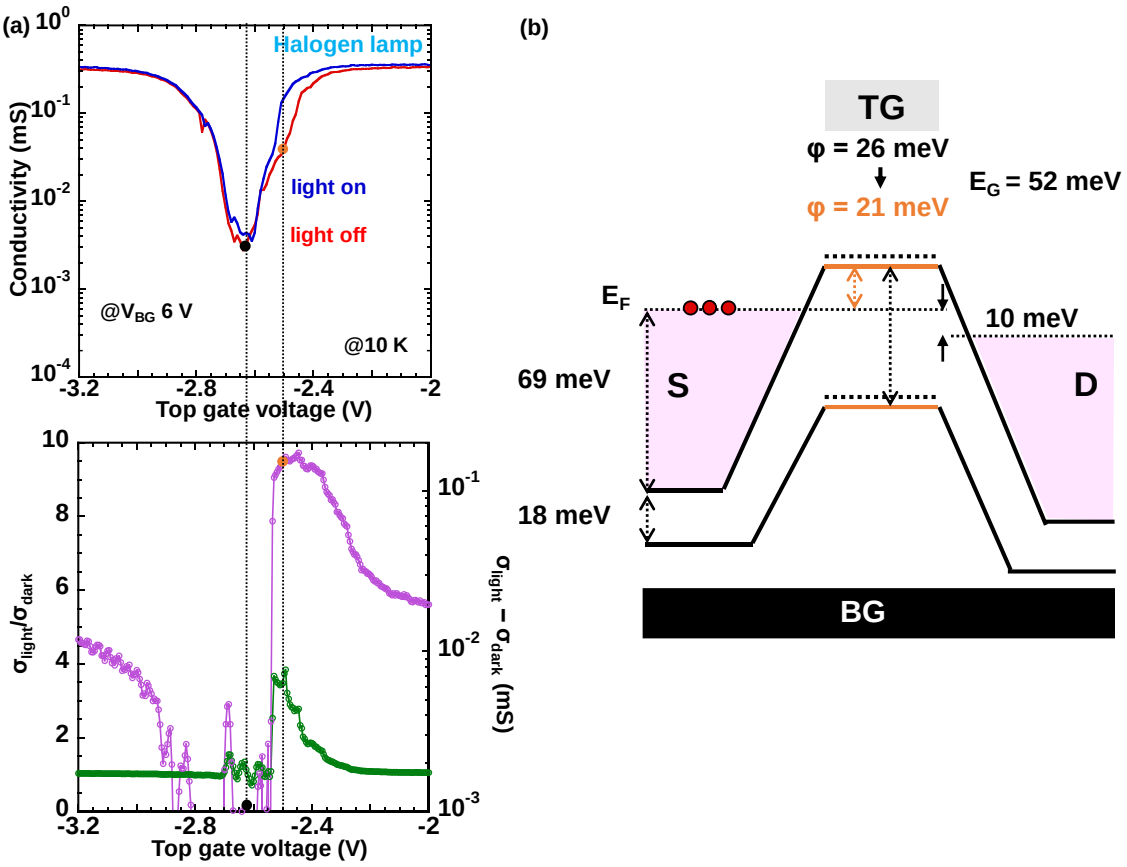

Figure 9.26 (a) Photoresponse results from **Fig. 9.23 (b)**.

(b) Potential barrier at maximum photocurrent (orange dot) and DP (black dot).

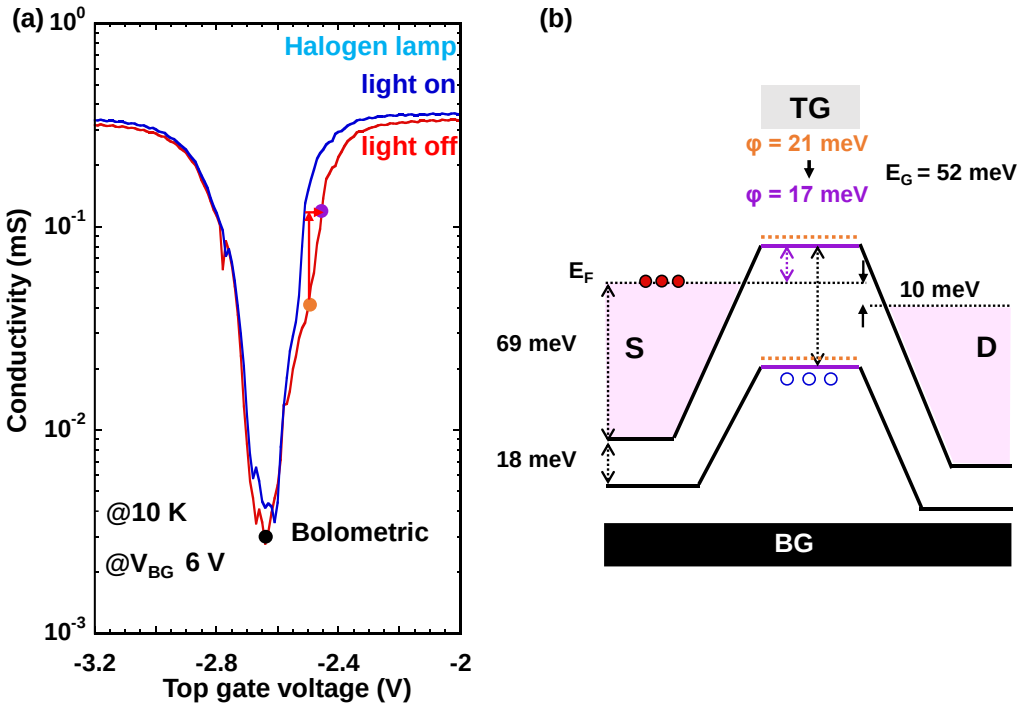

Figure 9.27 Reproduction of maximum photocurrent in dark condition.

(a) Photoresponse results from **Fig. 9.22 (b)**.

(b) Potential barrier at maximum photocurrent (orange dot) and equivalent conductivity in dark condition (purple dot).

Despite higher dark current compared to bolometric response, photoresponse at maximum photocurrent was observed up to 140 K (**Fig. 9.28**). Although the trend in temperature dependence is similar to bolometric effect, significantly increased photocurrent compared to bolometric response was consistently observed at every temperature. Higher temperature limit for photoresponse was expected in V_{BG} = 8 V due to largest band gap. However, the observed maximum photocurrent in V_{BG} = 8 V was smaller than in V_{BG} = 6 V in all temperature, implying that the potential barrier in V_{BG} = 8 V was too high for carrier accumulation in to gate region in present device to lower the potential barrier. The temperature dependence results also imply a possibility of phototransistor action where current amplification can overcome thermal noise at higher temperature than bolometric effect.

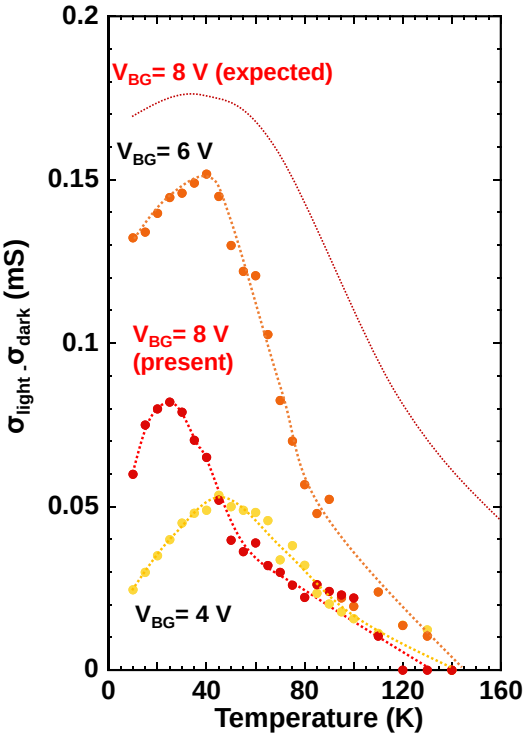

Figure 9.28 Temperature dependence of maximum photocurrent.

Time response was measured at the condition that gives maximum photocurrent. Although, the increased photocurrent suggests the possibility of phototransistor action, time constants were 0.2 s, 1.6 s for rise time and 0.5 s, 3.6 s for fall time (**Fig. 9.29**), which is about the same order of magnitude as bolometric response. This could be the limitation of time response to visible light in DC measurement, as time resolution was 10 ms and noise from temperature fluctuation could not be eliminated. Measurement with optimal optical power and better time resolution and smaller noise such as lock-in amp technique with AC current may give more accurate results.

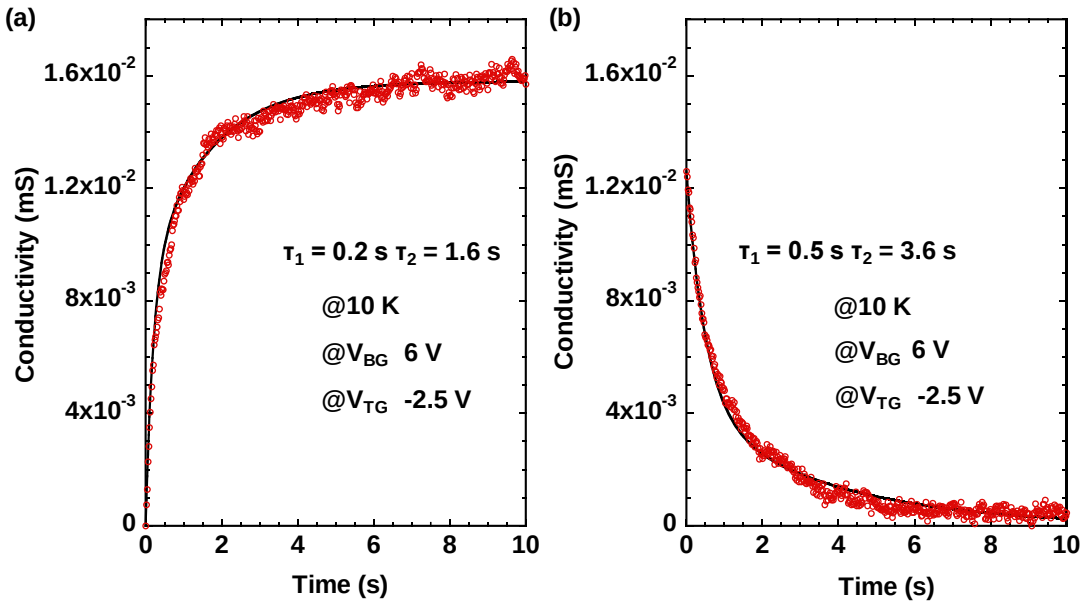

Figure 9.29 (a) Fitting for rise time.

(b) Fitting for fall time.

9.7 Photoresponse in FTPS

In order to investigate wavelength dependence of the newly observed photoresponse in 0.25 μm long Ni top gate device, FTPS measurement was attempted. The device was attached to copper substrate by thermal conductive glue and connected to pins through gold wire as shown in **Fig. 9.30**. The copper substrate was mounted onto aluminum sample holder which was then fixed to cryostat, and the pins were connected to measurement sockets. Cryostat was inserted into FRIR optical system (**Fig. 9.31**) and photocurrent spectra was measured. Unfortunately, top gate leakage occurred making

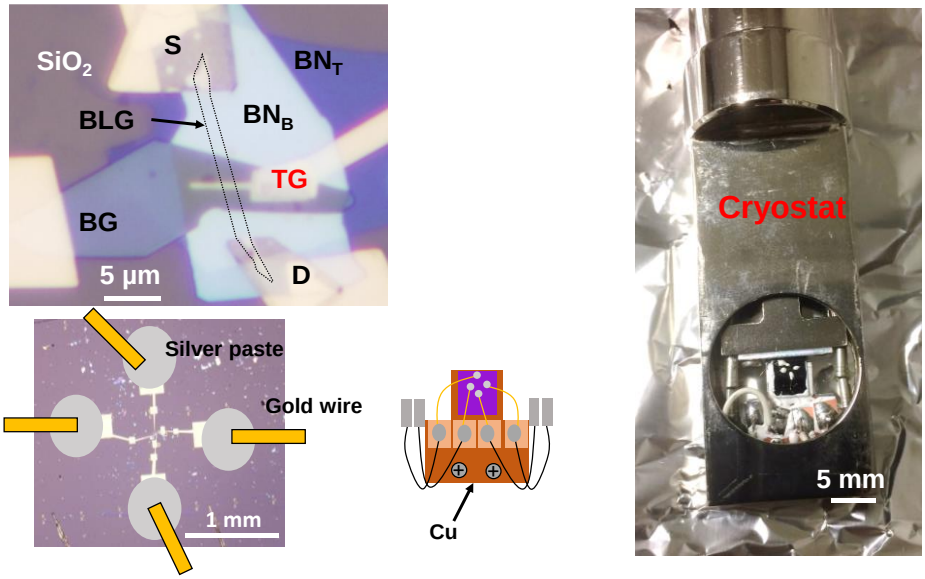

Figure 9.30 Sample set up for FTPS measurement.

independent tuning of Fermi energy and band gap difficult. The obtained spectra is shown in **Fig. 9.32**. Photocurrent spectra was not observed, but the measurement system and sample preparation procedure has been established.

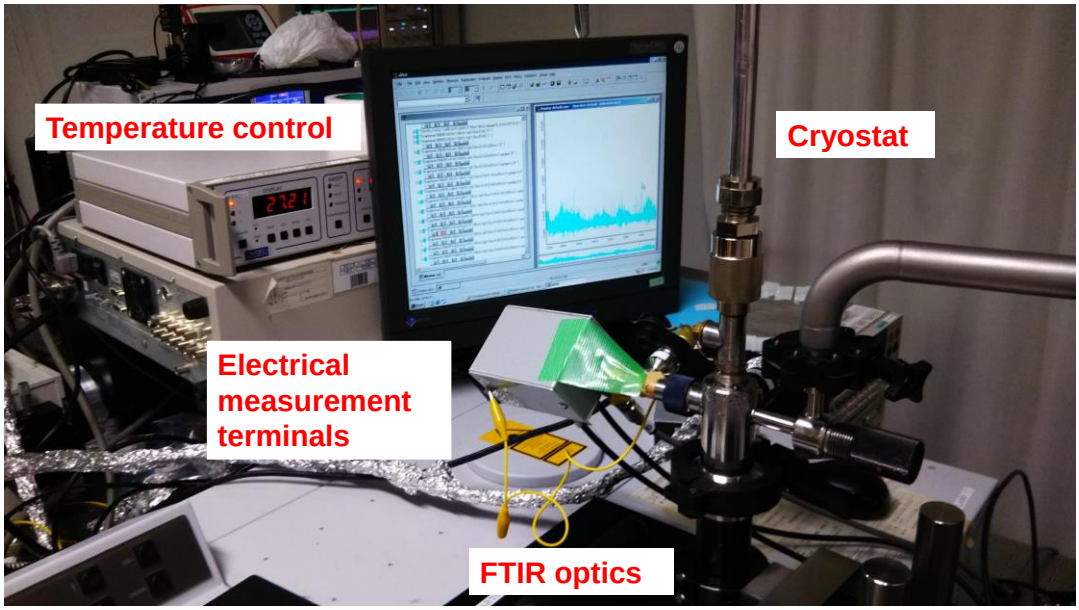

Figure 9.31 FTPS measurement system. Courtesy of Iwamoto lab at IIS.

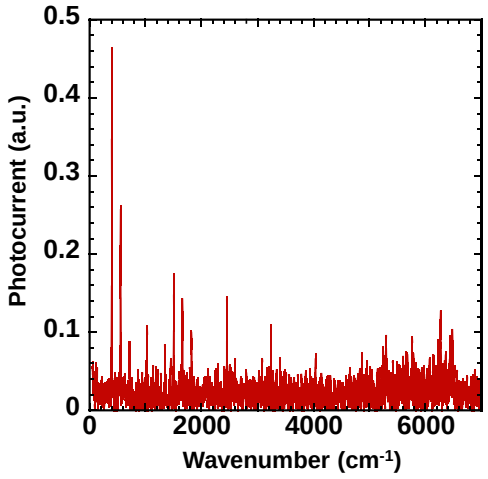

Figure 9.32 Photocurrent spectra of device in **Fig. 9.30**.

9.8 Summary and discussion for photodetector application

Photoresponse in all-2D layered heterostructure BLG-FETs was investigated. Gate length was considered as an important parameter in realizing phototransistor action in FETs because carrier diffusion through top gate region is required. If top gate length is much longer than carrier diffusion length which is calculated to be ~1.3 μm in BLG, the phototransistor action will be lost. Optical transmission of top gate electrode is also important. Devices with top gate length of 5, 1 and 0.25 μm with Ni and graphene as top gate electrode material were fabricated. First, basic photoresponse to visible light without phototransistor action was investigated in a device with 5 μm long Ni top gate. Distinct photoresponse was observed at DP and there was no consistent photocurrent sign change at DP. Therefore, photovoltaic effect and photothermoelectric effect are negligible. [7, 8] From strong temperature dependence of photoresponse, the basic photoresponse mechanism in BLG-FETs without phototransistor action was associated with the remaining possible mechanism: bolometric effect. Bolometric response taken as resistivity change at DP was observed up to 80 K which is quite higher than in previous study [9] (15 K), implying improvement in photoresponse by reducing potential fluctuations in BLG band gap.

Photoresponse to visible light in 1 μm long graphene also shows behaviors like bolometric effect, but photoresposne was observed up to 140 K. Photoresponse to infrared was also investigated in the same device. It was found that the device still showed bolometric response to low power infrared with wavelength of 1.54 μm.

Photoresponse to visible light in device with 0.25 μm long Ni top gate was investigated. Significantly increased photocurrent compared to bolometric response was observed on the right side of band gap region in boundary of npn and nnn. There was no photocurrent sign reversal at DP, denying the presence of photovoltaic effect at BLG/metal contacts. Therefore, the newly observed photocurrent was associated with phototransistor action. Although with phototransistor action, significantly increased photocurrent should be observed in all V_{TG} in gap region, the results show increased photocurrent only on the right side of band gap region in boundary of npn and nnn. Band structure and potential barrier in BLG in phototransistor regime were estimated at each V_{TG} and V_{BG}. It was found that potential barrier at V_{TG} that gives maximum photocurrent is lower than at DP. This contradicts with theoretical prediction where higher potential barrier is expected to give higher responsivity. The result suggests that when V_{TG} = DP, the potential barrier was too high for carrier accumulation under top gate to lower the barrier to amplify photocurrent. On the other hand, when potential barrier is initially set to lower value, carrier accumulation under top gate can lower the barrier and amplify

photocurrent. Such behavior seems to be consistent with the mechanism of phototransistor action based on bipolar transistor. It should be noted that maximum photocurrent at similar position in the largest band gap was smaller than in the second largest band gap. This similarly contradicts theoretical prediction where larger band gap which gives higher potential barrier should give higher responsivity. From these observations, it is suggested that effect of potential barrier lowering by carrier accumulation in gate region may be too small for conditions that give highest potential barrier in present device. Despite higher dark current compared to bolometric response, significantly increased photocurrent compared to bolometric response was consistently observed up to 140 K, implying a possibility of phototransistor action where current amplification can overcome thermal noise at higher temperature than bolometric effect.

To summarize, the results suggest phototranistor action in device with 0.25 μm long Ni top gate. However, non-ideal photocurrent behavior in large band gap suggests that effect of potential barrier lowering by carrier accumulation in gate region may be smaller than expected in present device. This may be due to insufficient optical transmission of top gate material or limitation by optical absorption of 2.3% per graphene layer. Hence, device with shorter top gate length and higher optical transmission that can suppress I_{off} is desirable. It can be seen that there is still room for improvement for all-2D layered heterostructure BLG-FETs as photodetectors.

9.9 References

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Summary & Outlook

The possibility for field-effect transistors (FETs) and photodetectors based on all-2D layered heterostructure bilayer graphene (BLG) was experimentally investigated.

In order to reduce potential fluctuations in BLG band gap, all-2D layered heterostructure BLG-FETs were fabricated. It was demonstrated that device properties can be significantly improved in all-2D layered heterostructure BLG-FETs compared to *h*-BN-encapsulated BLG on SiO_2/Si as well as high-*k* Y_2O_3/BLG/SiO_2. For the transfer characteristics at 20 K, I_{on}/I_{off} reached 4.6×10^5 with the off-state resistivity of ~5 GΩ even at band gap of 90 meV. For *h*-BN/BLG interface, undetectable amount of interface trap and two sharp vHS suggests that the *h*BN/BLG interface is electrically inert. These significant results are mainly attributed to the drastic reduction of the potential fluctuations to ~0.5 meV and hence the spatial uniformity of band gap. This quite low potential fluctuations can be achieved only in all-2D layered heterostructure BLG-FETs, not in conventional semiconductor systems with high-*k* gate stacks. Therefore, all-2D layered heterostructure BLG-FET is suitable for FET application in BLG.

Next, photoresponse in all-2D layered heterostructure BLG-FETs was investigated. Gate length was considered as an important parameter in realizing phototransistor action because phototransistor action requires carrier diffusion in top gate region. If top gate length is much longer than carrier diffusion length which is calculated to be ~1.3 μm in BLG, the phototransistor action will be lost. First, photoresponse mechanism without phototransistor action was investigated in a device with of 5 μm long top gate and was found to be bolometric effect. Bolometric response taken as resistivity change at Dirac point (DP) was observed up to 80 K which is quite higher than in previous study (15 K), implying improvement in phototresponse by reduction of potential fluctuations in BLG band gap.

In the device with 0.25 μm long top gate, significantly increased photocurrent compared to bolometric response was observed only in one part of band gap region. This region corresponds to potential barrier lower than the highest barrier, which, is expected to give highest responsivity in theory. Moreover, maximum photocurrent at similar position in the largest band gap was smaller than in the second largest band gap. This similarly contradicts theory where larger band gap which gives higher potential barrier should give higher responsivity. Therefore, it is suggested that effect of potential barrier lowering by carrier accumulation in gate region may be smaller than expected in present device. Despite higher dark current compared to bolometric response, significantly increased photocurrent compared to bolometric response was consistently observed up to 140 K, implying a possibility of phototransistor action where current amplification can overcome thermal noise at higher temperature than bolometric effect. The observed phototransistor action suggests possibility for photodetection application for BLG-FETs.

Outlook

FET application

The final goal for FET application for BLG is suppressing I_{off} at room temperature. This is extremely difficult for *h*-BN gate stack, because the maximum band gap attainable by *h*-BN gate stack is limited to 90 meV due to small dielectric constant. To open maximum band gap of ~250 meV for BLG, gate stack with larger dielectric constant is required for applying $|\bar{D}| \geq 3$ V/nm. This issue may be solved by combining *h*-BN with high-*k* single crystal nanosheet.

Photodetection

All-2D layered heterostructure BLG-FETs show potential for photodetection application as phototransistor action was observed in a device with 0.25 μm long top gate. The observed non-ideal photocurrent suggests room for improvement such as using top gate with shorter length and higher optical transmission.

Originality of this research

The originalities of this study are

1. Formation of surface contact to BLG channel by selective etching of top *h*-BN layer by CF_4 plasma. Edge contact has been used in most studies.
2. Quantum capacitance measurement of gapped BLG on fused silica substrate. Most CV measurements in graphene have been performed on Si/SiO_2 substrate where parasitics are large.
3. Measurement of interface trap density (D_{it}) at *h*-BN/BLG heterointerface by conductance method.
4. Investigation of bolometric response in all-2D layered heterostructure BLG-FETs.
5. Identification of theoretically proposed phototransistor action in BLG.

Publications

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(2) Uwanno, T., Taniguchi, T., Watanabe, K. & Nagashio, K. "Electrically Inert *h*-BN/Bilayer Graphene in All-Two-Dimensional Heterostructure Field-Effect Transistors" *ACS Appl. Mater. Interfaces* **10**, 28780-28788 (2018).

(3) Netsu, S., Kanazawa, T., Uwanno, T., Amemiya, T., Nagashio, K. & Miyamoto, Y. "Type-II HfS_2/MoS_2 heterojunction transistors" *IEIECE Trans. Electron.* **E101-C**, 338-342 (2018).

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