論 文 の 内 容 の 要 旨

論文題目　Study on Subthreshold Characteristics of Gate-All-Around Poly-Si Junctionless Nanowire Transistors
(ゲートオールアラウンド構造を有するポリシリコンジャンクションレスナノワイヤトランジスタにおけるサブスレッショルド特性に関する研究)

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Polycrystalline silicon (poly-Si) transistors have been considered as the key building elements for 3D integration due to their low thermal budget and simplicity of fabrication process with high scalability, which can offer high integrated density, rich functions, and low power consumption. However, unavoidable defects at grain boundaries (GBs) in poly-Si channel undermine the carrier transport and switching properties. These GB defects can be reduced by either several crystallization methods or passivation of GBs from hydrogen (H) and/or fluorine (F) treatments. In particular, in the F treatment more effectively suppress the GB defects because bonding energy of Si-F (5.73 eV) is stronger than that of Si-H (3.18 eV), which is driving force to improve the device performances of poly-Si transistor. Another effective way to minimize the GB defects is to shrink the dimension of poly-Si channel, which can significantly reduce the total number of GB defects (or increase the grain size) and improves the electrical performances of poly-Si transistor. Simultaneously, the adoption of gate-all-around (GAA) nanowire (NW) as the channel structure of the poly-Si transistor has been extensively studied because the surrounding gate on the whole channel can effectively control the electrostatic potential of the channel, and the total number of GBs can be dramatically reduced due to the nano scale small-size volume.

Meanwhile, the concept of junctionless (JL) transistors (or gated resistors) which consist of highly doped channel with a same polarity across the source (S), channel, and drain (D) have attracted much interest. The absence of S/D junctions enable to simplify the fabrication process and completely eliminate the diffusion of impurities owing to no doping gradient compared with the conventional inversion-mode (IM) transistor. In JL transistors, the channel is fully depleted by only gate bias in the turn-off state, which implies that the channel must be thin enough to allow fully depleted channel. In addition, the doping concentration of channel should be as high as possible to ensure high on-current and low series resistance in the turn-on state, because the current drivability of JL transistors strongly depends on channel

resistance. However, the electrical performances of JL transistors become worse as the doping concentration increases for various reasons including reduction of mobility, degradation of subthreshold slope (SS), severe device-to-device variations, and high level of off-state leakage current. As a result, these counteracting factors between high doping concentrations and undesirable effects have trade-off relationship.

Moreover, this JL scheme can be well matched with the poly-Si GAA NW transistor because the channel must be thin and narrow for full depletion in turn-off state. The channel structure and size have a strong influence on the subthreshold characteristics such as SS, threshold voltage (V_{th}) and off-current (I_{off}), which are key factors for low power applications. Among them, the steep SS is the most powerful factor so that the theoretical limit of SS ~60 mV/dec at room temperature is highly desired for low power logic applications. However, the poly-Si channel based transistors have severe restriction to achieve theoretical limit of SS due to the high density of GB defects.

Some studies had an effort to implement the steep SS near theoretical limit at room temperature by adopting small size poly-Si channel in only n-type devices, but few have addressed the p-type devices. In addition, the passivation kinetics of F implantation on the GB defects in poly-Si JL transistors have not been well studied and there have been no reports on the effect of F implantation on the poly-Si JL transistors yet.

Therefore, in this thesis, we experimentally demonstrated the effects of F implantation as a function of doping profiles of B and F ions on the electrical characteristics of planar p-type poly-Si JL transistors, for the first time. In addition, we successfully demonstrated the ideal SS of 60 mV/dec at room temperature in the GAA p-type poly-Si JL NW transistors with low I_{off} and high I_{on}/I_{off} ratio thanks to the ultra-thin and narrow poly-Si channel with highly suppressed GB defects as well as improved fabrication process.

First, we investigated the dependence of dopant types (P^+, B^+, BF_2^+) on the planar type poly-Si JL transistors and observed superior subthreshold characteristics in case of BF_2 doped channel thanks to B segregation as well as F effects. P^+, B^+, BF_2^+ ions were implanted at 35keV with dose of $3x10^{14}cm^{-2}$, for n-type and p-type channel. For thin poly-Si channel, local oxidation of silicon (LOCOS) process at 1100°C was conducted to thin down the channel to 10 nm, where the B ions were segregated. As a result, locally thinned active region with low concentration and thick S/D regions with high concentration were simultaneously formed. In this step, the average grain size in poly-Si film became larger from 130 to 230 nm owing to the high temperature process. As a results, we found that BF_2^+ implanted JL transistors have superior electrical characteristics (steep SS and high carrier mobility) as well as smaller device-to-device variations to P^+ and B^+ implanted JL transistors due to the effects of B segregation and F passivation, respectively. Therefore, it is expected that the passivation effect of F is remarkably effective even in the JL poly-Si transistors. However, it did not take into account that doping profiles of implanted B^+ and BF_2^+ ions would be different due to different atomic weights, which affects the some damages and defects in the poly-Si film produced by heavy ion implantation process. For more reasonable comparison, therefore,

comprehensive studies on the impact of F as a function of doping profiles on the poly-Si JL transistors is essential to achieve deep understanding of passivation effects and higher transistor performance.

Second, therefore, we focused on the effect of F in the p-type poly-Si JL transistors in order to more clearly verify the origins of performance enhancements of BF_2^+ implanted JL transistors in the 1st experiment. The fabrication process flows basically follow 1st experiment. Added to the two types of JL poly-Si transistors (by B^+ implantation and by BF_2^+ implantation), a new type of JL poly-Si transistors by co-implantation of B^+ and F^+ was fabricated with different two doping profiles (shallow and deep ion implantation) and compared based on experimental results. We found that the carrier mobility and SS characteristics are drastically enhanced by co-implanting the B^+ and F^+ compared to B^+ only implanted devices, and that effect is more prominent in case of deeper doping profiles with high ion energy. Therefore, it can be concluded that the electrical performances of poly-Si JL transistors are quite sensitive to the doping profiles of implanted ions even at same doping concentrations. In more details, it is observed that co-implantation of B^++F^+ is more effective way to achieve higher carrier mobility than single implantation of BF_2^+, while the SS characteristics are nearly similar. Hence, for higher carrier mobility, additional F implantation (co-implantation of B^++F^+) is essential. In contrast, there is no need to perform the co-implantation, only a single implantation such as BF_2^+ is acceptable to obtain steep SS because the co-implantation brings about additional process steps, which is not suitable for low thermal budget. As a results, we found that the F effects can play an important role to enhance the electrical characteristics of JL poly-Si transistors as well as conventional IM poly-Si transistors. Consequently, these findings can provide useful guidelines of fabricating high performance poly-Si JL transistors for future practical manufacturing and applications.

Finally, we fabricated the p-type GAA JL poly-Si NW transistors and clearly observed the ideal SS (theoretical limit) at room temperature thanks to the ultra-thin and narrow poly-Si channel with highly suppressed GB defects as well as improved process including segregation of B ion and effect of F ion. The fabrication process flows basically follow our previous works except for formation of NW channel. The NW pattern was defined by electron beam lithography and reactive ion etching, followed by wet-etching for suspending NW from the BOX layer. The actual nanowire width (W_{NW}) is 9.6nm. It clearly reveals that the poly-Si NW channel with thickness of 6.7 nm is surrounded by 7.1 nm thick gate oxide in this specific device. From the TEM images, the actual effective width (perimeter of NW, W_{eff}) of poly-Si NW can be calculated to the (9.6+6.7 nm) × 2 = 32.6 nm. As a results, we successfully demonstrated the ideal SS of 60 mV/dec in the GAA p-type poly-Si JL NW transistors with low I_{off} and high I_{on}/I_{off} ratio, based on the experimental results. The origins of superior subthreshold characteristics might originate from improved processes (B segregation and F effect) as well as reduced GB defects and GAA structure. In addition, it was found that the NW characteristics have relatively small device-to-device variations and good thermal stability. Therefore, it has great potential and is highly promising for 3D stacked ICs applications as well as future low power applications.