博士論文（要約）

Study on Subthreshold Characteristics of Gate-All-Around Poly-Si Junctionless Nanowire Transistors

(ゲートオールアラウンド構造を有するポリシリコンジャンクションレスナノワイヤトランジスタにおけるサブスレッショルド特性に関する研究)

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Min-Ju Ahn (安 珉柱)

Supervisor Prof. Toshiro Hiramoto

論 文 の 内 容 の 要 約

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(ゲートオールアラウンド構造を有するポリシリコンジャンクションレスナノワイヤトランジスタにおけるサブスレッショルド特性に関する研究)

氏　名　安 珉柱

In this dissertation, gate-all-around (GAA) polycrystalline silicon (poly-Si) junctionless (JL) nanowire (NW) transistors with superior subthreshold characteristics including ideal subthreshold slope (SS) at room temperature, low off-state leakage current, and high on/off current ratio, and small device-to-device variations are successfully demonstrated by improved fabrication processes with highly suppressed grain boundary (GB) defects in the poly-Si channel. The origins of these improvements are discussed based on the experimental results.

High quality of poly-Si channel can be obtained not only by segregation effects of boron (B) ions during channel thinning process, but also fluorine (F) passivation on GB defects during channel implantation process. The former can effectively increase the grain size owing to the high temperature annealing, and produce locally thin active region with low concentration which leads to small device-to-device variations. The latter can drastically reduce the GB defects, which enhances the subthreshold characteristics as well as carrier transports. In addition, the quality of poly-Si can be more improved by adopting small-size GAA NW structure with reduced GB defects as well as enhanced gate controllability.

For the JL transistor, the doping concentration of channel should be as high as possible to ensure high on-current, and carefully controlled. However, the highly doped JL channel significantly degrades the electrical performances of JL transistor, and suffers from some damages and defects during heavy ion implantation process, which shows trade-off relationship. In other words, the optimization of implantation conditions to determine the polarity of channel, as well as F passivation are essential for better understanding the electrical characteristics of JL transistor.

Some studies had an effort to implement the superior electrical characteristics such as steep SS near theoretical limit at room temperature by adopting small size poly-Si JL NW channel in only n-type devices,

but few have addressed the p-type JL devices. Moreover, the F passivation kinetics of GB defects in poly-Si JL transistors have not been well studied, and there have been no reports on the effect of F passivation on the poly-Si JL transistors yet.

Therefore, in this dissertation, we implemented the p-type GAA JL poly-Si NW transistors and clearly observed the ideal SS (theoretical limit) at room temperature thanks to the ultra-thin and narrow poly-Si NW channel with highly suppressed GB defects as well as improved processes including B segregation and F passivation. In addition, comprehensive studies on the impact of F passivation on the poly-Si JL transistors are carried out based on experimental results. As a results, nearly ideal SS of 60mV/dec at room temperature, small device-to-device variations, and negligible temperature dependence are observed in fabricated p-type GAA JL poly-Si NW transistors, indicating the device is promising for future three-dimensional (3D) integration.