論 文 の 内 容 の 要 旨

論文題目 Fabrication of (111) Ge-on-insulator n-channel MOSFETs by smart-cut process and the electrical characteristics
（スマートカットプロセスによる(111) Ge-on-insulator n-チャネルMOSFETの作製とその電気特性 ）

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In this dissertation, the well-behaved (111) Ge-on-insulator (GOI) n-channel metal-oxide-semiconductor field-effect transistor (nMOSFET) operation is demonstrated with smart-cut technology.

GOI structures has been received great attention as a promising platform for next-generation scaled complementary metal-oxide-semiconductor (CMOS) system owing to its high carrier mobility and high compatibility with the conventional Si-based platform. In particular, high-performance GOI pMOSFETs has been extensively reported because of high hole mobility. Whereas, study on electrical characteristics of GOI nMOSFETs is still insufficient in spite of its high electron mobility. Thus, a study on the performance enhancement of GOI nMOSFETs is strongly required. On the other hand, in developing Ge nMOSFETs, the surface orientation should be carefully considered because Ge has different effective mas depending on the surface orientation because of its anisotropic characteristics. As the (111) surface orientation has lower effective mass than the other surface orientations, (111)-oriented Ge is expected to improve the electrical properties. Although (111) GOI nMOSFETs have significant potential with these research issues, there is no report on (111) GOI nMOSFETs until now. This is mainly because of the difficulty in realizing (111) GOI substrates. Therefore, in this thesis, the physical and electrical properties of (111) GOI substrates fabricated by the smart-cut process are investigated focusing on the annealing temperature and hydrogen ion implantation (I/I) dose dependence. In addition, (111) GOI nMOSFETs are fabricated on the high-quality (111) GOI substrates and its electrical characteristics are studied compared with (100) GOI and bulk Ge nMOSFETs.

In the smart-cut process, the annealing process is indispensable to recover the defects in the transfer layer. Thus, to realize the high-quality GOI layer, physical and electrical characteristics of (111) and (100) GOI substrates fabricated by the smart-cut technology are examined with various annealing temperatures. The annealing effects on the surface roughness properties,

crystallinity and electrical properties of GOI layers are systematically studied by AFM images, Raman analysis, Hall measurements and back-gate GOI pMOSFETs operation. It is observed that the high-temperature annealing over than 550 ^{o}C causes the rough surface for both (111) and (100) GOI layers, attributed to desorption of GeO_X. High crystal quality of (111) and (100) GOI layers are realized with the annealing temperature of 550 ^{o}C. In addition, the annealing process at 550 ^{o}C effectively cure defects generated by the ion implantation process without thermal damages, leading to the improvement of electrical properties. The degradation in electrical characteristics are observed for annealed GOI samples at 600 ^{o}C due to the thermal damages. Fabricated back-gate (111) and (100) GOI p-channel MOSFETs (pMOSFETs) show the high effective mobility of around 350 $cm^{2/}Vs$, indicating the superior quality of fabricated GOI wafers.

Ion implantation is one of the most important process in the smart-cut technology because implanted hydrogen ions cause the splitting phenomenon and damages in GOI layers. Therefore, influence of hydrogen ion implantation dose on electrical and physical properties of GOI layers are investigated for (111) and (100) GOI substrates fabricated by the smart-cut process with two dose condition, 1×10^{17} cm^{-2} and 4×10^{16} cm^{-2}. High crystallinity GOI layers are obtained through the thermal annealing process at 550 ^{o}C, irrespective of the I/I dose. However, the reduction of Hall hole mobility is found for high dose GOI samples, implying the degradation in electrical characteristics. High Hall hole mobility of 2020 cm^2/Vs is achieved with low dose condition, suggesting the high quality of GOI layers. Whereas, the similar transfer characteristic curves and effective hole mobility are observed for high and low dose GOI devices under the back-gate pMOSFETs operation, indicating that there are almost no significant damages near the bonded interfaces.

(111) GOI nMOSFETs are prepared on high-quality GOI substrates fabricated by the smart-cut process. Here, the fabrication process for GOI nMOSFETs is carefully designed considering device performance in terms of gate stack condition, annealing method and sequence. To prevent the thermal damage of GOI substrates, n^{+}/p junction formation at a relatively low temperature of 550 ^{o}C is proposed with solid-state diffusion process from As-based spin-on-glass (SOG). As a result, the well-operated (111) GOI nMOSFETs are confirmed from the transfer characteristic curves, for the first time. In addition, it is found that the (111) GOI nMOSFET offer the higher on current compared to that of the (100) one. In particular, highest electron effective mobility of 943 cm^2/Vs is achieved for (111) GOI nMOSFETs among the reported GOI nMOSFETs. It is considered that the present (111) GOI nMOSFET fabricated by smart-cut technology is a promising template for future GOI CMOS logic circuits.