論 文 の 内 容 の 要 旨

論文題目　　Ferroelectric-HfO_2-based non-volatile memories for high density and low power applications

（強誘電体$Hf0_2$を用いた高密度・低消費電力不揮発性メモリ）

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Low power, high density non-volatile memories (NVMs) become a key component to achieve internet of thing (IOT) society. HfO_2 based ferroelectric NVMs including ferroelectric tunnel junction (FTJ) and ferroelectric field effect transistor (FeFET) have attracted more attentions due to low power consumption and good CMOS compatibility. However, because FTJ is a two terminal device and its relatively low read current, it is not clear if it has competitive scalability to other emerging memories. Even, 3D structure FeFET can significantly increase the density, the poly-Si channel of 3D structure FeFET has some challenges such as low mobility of very thin poly-Si channel, voltage loss and subthreshold slope (SS) degradation caused by low-k interfacial layer between poly-Si channel and gate oxide.

In chapter 2, first, the top electrode replacement process is proposed to achieve a symmetric coercive voltage and high remanent polarization of Metal-Ferroelectric-Insulator-Semiconductor (MFIS) type FTJ. Then, a numerical simulation framework is developed to investigate the scalability of HfO_2-based FTJ. The simulation framework consists of tunnel current calculator module using Non-Equilibrium Green Function (NEGF) method and potential calculator module using self-consistent method. The simulation framework is calibrated by experimental

results of MFIS type FTJ using top electrode replacement process. MFIS type FTJ has a higher TER than Metal-Ferroelectric-Insulator-Metal (MFIM) type FTJ while MFIS type FTJ has almost same read current as MFIM type FTJ due to the asymmetric screen length of top and bottom electrodes. High read current can be obtained by thinner ferroelectric and interfacial layers while high TER ratio and low depolarizing field are maintained by adjusting bottom semiconductor electrode property. Based on these results, we have shown the potential of MFIS type FTJ for scaling down to sub-20 nm diameter.

In chapter 3, ultrathin IGZO FeFET with top gate structure is proposed. Memory window exists with fixed body potential using top gate structure. The design guideline of ultrathin IGZO channel FeFET is proposed using TCAD simulation. HfZrO (HZO) capacitor with IGZO capping is fabricated and shows a large P_r and nearly symmetric coercive voltage. Thanks to nearly-zero low dielectric constant interfacial layer between HZO and IGZO layer, metal/HZO/IGZO/metal capacitor shows a good reliability. Asymmetric imprint effect of metal/HZO/IGZO/metal capacitor is observed due to the asymmetric structure. Ultrathin IGZO channel FeFET shows high mobility and nearly ideal steep slope (SS) with the use of back-end compatible process, thanks to junctionless FET operation, nearly-zero low-k interfacial layer between HZO and IGZO layer. Controllable memory characteristics are demonstrated with fixed body potential using top gate. IGZO channel FeFET will open a new path for high-density, low power consumption memory application.

In conclusions, FE-HfO_2 based memories including MFIS type FTJ and IGZO channel FeFET are investigated. We hope FE-HfO_2 based memories can contribute to the next generation low-power and high-density memories.