論 文 の 内 容 の 要 旨

論文題目　Operation Mechanisms and Intrinsic Performances of Non-volatile Memory Devices Based on Two-dimensional van der Waals Heterostructures
（二次元ファンデルワールスヘテロ構造からなる不揮発性メモリデバイスの動作機構と本質的なデバイス性能に関する研究）

氏　名　佐々木 太郎

It is no doubt that our society has been strongly supported by the remarkable progress of Si-based electronic devices. On the contrary, the emergence of new kinds of applications such as neuromorphic computing, and the predicted arrival of geometrical and economical limit of the device scaling have required the alternative strategy for future fertile society. In this context, two-dimensional (2D) materials have been increasing their prominence as a candidate for next-generation electronic material. As well as its field-effect-transistor (FET) applications, its non-volatile memory (NVM) applications have been aggressively studied. With the help of dry transfer technique, NVM devices based on 2D van der Waals heterostructures (2D heterostructured NVM devices) have been realized, and considered as promising candidates of next-generation NVM, since its dangling-bond free interfaces have potential to realize the interface trapped charge free NVM devices. In 2D heterostructured NVM devices, typically, transition metal dichalcogenides (TMDCs) are often used as channel materials, while hexagonal boron nitride (*h*-BN) and graphite or graphene are used as a tunneling barrier and floating gate (FG), respectively. In addition, because of the increasing attention of

2D materials-based FETs, future material compatibility can also be expected for 2D heterostructured NVM device. However, even though a lot of progress has been achieved from graphene channel device with non-2D materials to 2D heterostructured device, it has not been sufficiently supported by the understandings of their operation mechanisms, preventing further improvement and control of their performances as desired. The lack of understandings also leads to the invalid evaluation of their performances, that is, *intrinsic* performances of them are still unclear. Therefore, the objective of this study is to reveal the comprehensive operation mechanisms and their intrinsic performances. The study is conducted in bottom-up approach as follows.

First of all, new measurement technique called *floating gate voltage (V_{FG}) measurement* is proposed, for unveiling the operation mechanisms behind standard current–voltage (I–V) round sweep curves. Since V_{FG} measurement can be performed by just adding another electrode onto the FG, it is applicable to any 2D heterostructured NVM devices. Measured V_{FG} during I–V round sweep called *V_{FG} trajectory* can be explained by two regions, which are capacitive coupling region with tilted V_{FG} and feedback region with pinned V_{FG}. The principle has been confirmed by experimental results.

Next, for reasonable performance evaluation, the validity of memory window extraction method is investigated since there are two different extraction methods which strongly depend on the research field. While I–V round sweep is widely used in 2D research field, I–V single sweep after program and erase (P/E) operation is used in Si research field. Consequently, V_{FG} trajectory-based analysis has revealed that the memory window extracted by I–V round sweep is often overestimated. The criterion for the overestimation by I–V round sweep is also derived, and it is found that the criterion is easy to be satisfied. Therefore, as well as Si research field, I–V single sweep should be used for the extraction of memory window even in 2D research field.

Then, the V_{FG} measurement is applied for three kinds of 2D heterostructured NVM devices. Since bandgap of 2D channel material and metal/2D interface are considered as the keys of device operation, three different materials (MoS_2, WSe_2, $MoTe_2$) are used as the channels. On the other hand, all three devices have *h*-BN tunneling barrier and graphite FG. Interestingly, each device has inherent V_{FG} trajectory while their I–V round sweep curves are very similar as well as previous studies. By analyzing the trajectories, comprehensive understandings of their operation mechanism can be revealed, in terms of three tunneling current limiting paths. Moreover, the validity of understandings is confirmed by experimental controls of V_{FG} trajectory where the temperature, device structure, and sweeping rate are varied. Tunneling between

source/drain (S/D) metal electrode and FG are experimentally proved for the first time, while previous studies have claimed that the 2D heterostructure was tunneling path.

Finally, intrinsic performances of 2D heterostructured NVM device is reasonably investigated as mainly focused on the P/E speed. Remarkably, 50 ns ultra-fast P/E operation can be achieved by appropriately designed devices. To minimize the size of FG pad is the key for preventing the large tunneling current during fast P/E operation, which leads the *h*-BN breakdown. Although the superior 2D/2D interface seems to be the key, the controlled experiment revealed it is not the key. On the other hand, as compared with conventional SiO_2, *h*-BN possesses stronger breakdown strength under high-speed voltage pulse stress, suggesting that the larger tunneling current can be allowed for *h*-BN. Importantly, the ultra-fast nature of 2D heterostructured NVM device is in the range of storage class memory, which is now strongly desired. Retention and endurance characteristics are also investigated, and 10^5 s retention and 5×10^4 P/E cycles endurance can be achieved for the MoS_2 device with access region. Since the MoS_2 device has large FG pad for V_{FG} and tunneling current measurements, *h*-BN may be severely degraded due to large tunneling current as well as the speed test, suggesting that further improvement can be expected by the device with appropriately designed FG pad.

As the conclusion of this study, 2D heterostructured NVM device with graphite contact is proposed as a promising device structure. Although 2D/2D interface is not the key for the ultra-fast operation, it will be the key of great reliability.