博士論文（要約）

# Online Quantum Error Correction Using a Superconducting circuit

（超伝導回路を用いた
オンライン量子誤り訂正についての研究）

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# Abstract

Due to the low error tolerance of a qubit, detecting and correcting errors on it is essential for fault-tolerant quantum computing (FTQC). *Surface code* (SC) associated with its decoding algorithm is one of the most promising quantum error correction (QEC) methods. QEC needs to be very power-efficient since the power budget is limited inside a dilution refrigerator for superconducting qubits, by which one of the most successful quantum computers (QCs) is built. Moreover, real-time decoding is necessary because slow error correction leads to the accumulation of errors on qubits, resulting in logical failures. In this thesis, we proposed the concept of online-QEC, where both the measurement and decoding processes of QEC are performed simultaneously. Then, we proposed the decoding algorithms based on the concept and their hardware implementations with *SFQ*-based superconducting digital circuits to achieve a high-speed and low-power decoder.

First, we proposed an online-QEC algorithm named QECOOL with the capability to deal with measurement errors and its hardware implementation with SFQ-based superconducting digital circuits. We designed a key building block of the proposed hardware with an SFQ cell library and evaluated it by the SPICE-level simulation. Each logic element is composed of about 3000 Josephson junctions, and power consumption is about 2.78 $\mu$W when operating with 2 GHz clock frequency, which meets the required decoding speed. We simulated our decoder on a quantum error simulator for code distances 5 to 13, achieving a 1.0% accuracy threshold.

Second, we enhanced the QECOOL algorithm with a neural networks-based preprocessor to propose a new online decoding algorithm named NEO-QEC. The preprocessor decodes SCs utilizing richer information than the other algorithms based on graph matching problems, which leads to higher accuracy. We achieved high accuracy, low latency and low power of the decoding algorithm by reducing the computational cost required for neural networks with binarized neural network techniques. We designed a neural processing unit with an SFQ cell library to support the NEO-QEC algorithm and evaluated its circuit characteristics. We simulated our decoder on a quantum error simulator for code distances 5 to 13, achieving a 53% higher threshold than the original QECOOL.

Finally, we extended the QECOOL to propose a new online-QEC algorithm that supports logical operations between logical qubits with a practical decoder circuit, as well as a new FTQC architecture. We also showed that our architecture could process the merge-and-split operations required in the magic-state distillation protocols with reasonable latency and power consumption. We designed a key building block of the

proposed architecture with a hybrid of SFQ- and Cryo-CMOS-based digital circuits and evaluated it with a SPICE-level simulation. Each logic element includes about 2400 Josephson junctions, and power consumption is estimated to be 2.07 $\mu$W when operating with a 2 GHz clock frequency. We evaluated the decoder performance by a quantum-error simulator for an essential logical operation with code distances up to 11, and it achieves a 0.6% accuracy threshold.