

博士論文(要約)

**III-V/Si Hybrid MOS Optical Phase  
Shifters and Its Applications in Universal  
Photonic Integrated Circuits**

(III-V/Si ハイブリッド MOS 光位相シフ  
タおよびユニバーサル光集積回路への  
応用に関する研究)

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DOCTORAL THESIS

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**III-V/Si Hybrid MOS Optical  
Phase Shifters and Its Applications  
in Universal Photonic Integrated  
Circuits**

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UNIVERSITY OF TOKYO

# *Abstract*

Nano Physics and Device Technology  
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Doctor of Philosophy  
in Electronic Engineering

## **III-V/Si Hybrid MOS Optical Phase Shifters and Its Applications in Universal Photonic Integrated Circuits**

by Hanzhi TANG

Silicon (Si) photonics is the most promising technology for high-speed communication and networking for the next generation of interconnections. Recently, new paradigms of photonic information processing and analogue photonic computing are emerging in Si photonics. The computing process can be performed in programmable photonic integrated circuits (PICs) or nanophotonic processors, leveraging the interference of photons. One of the representative PICs for information processing, the universal PIC, can conduct arbitrary unitary matrix-vector operations and further cover arbitrary matrix-vector operation by singular-value decomposition (SVD). Driven by the great success of artificial intelligence and the lack of a powerful and efficient computing platform for deep neural networks, photonic neural networks (PNN) realized by universal PICs are attracting more attention. The encoded information can be transferred and processed with low loss at the speed of light, owing to less interaction between the photons and media. Combined with power-efficient Si photonic devices, the state-of-art photonic computing systems based on universal PICs outperform the advanced deep learning cluster composed of graphic processing units (GPUs) in the computation speed and power efficiency in the referring stage. However, the performance bottleneck of current universal PICs comes from the active programmable units in the circuit, named optical phase shifters. Low-loss, power-efficient and high-bandwidth optical phase shifters are strongly desired to unveil the mightiness of universal PICs over electronic counterparts.

The metal-oxide-semiconductor (MOS) optical phase shifter is a potential solution for universal PICs owing to low power consumption and a balance

between modulation efficiency and bandwidth. However, the free carrier accumulates in Si for phase modulation invokes extra loss simultaneously. This modulation loss leads to loss imbalance in each optical path and degrades the performance of universal PICs. In the past works, a III-V/Si hybrid MOS optical phase shifter was proposed and experimentally demonstrated, with a record-low  $V_{\pi}L$  down to 0.047 V·cm. Meanwhile, the modulation loss is down to 0.23 dB/ $\pi$ , approximately 10-fold smaller than all-Si MOS optical phase shifters. This novel phase shifter provides much lower static power ( $< 1$  nW) than the thermo-optic (TO) phase shifters (20 mW) and higher modulation speed (up to GHz) than microelectromechanical phase shifters (up to MHz). More promisingly, due to the demand for on-chip integrated light sources, III-V/Si heterogeneous integration process is now transferring from laboratory scale to foundry standard. III-V/Si hybrid MOS optical phase shifters will be accessible in process design kits (PDKs) with good uniformity, ready for large-scale PICs soon.

However, the influence of the modulation loss and insertion loss of III-V/Si hybrid MOS optical phase shifters to universal PICs is still unclear. In chapter 2, a numerical model of universal PICs is established by the transfer matrix model. The influences of the modulation loss and insertion loss in the phase shifters on the performance of the universal PICs are evaluated. A control method based on the simulated annealing is explored to compensate for the modulation loss for III-V/Si MOS optical phase shifters in universal PICs. However, with increasing scale of the universal PIC, the modulation loss leads to severer performance degradation even with optimization. This leads to the request of reduction of loss in III-V/Si MOS optical phase shifter for better scalability.

To reduce the loss of the phase shifters, in chapter 3, the low-doped III-V/Si hybrid MOS phase shifter is investigated. The simulation shows the absorption can be suppressed below 0.1 dB/mm with a lower doping profile in the hybrid waveguide, due to smaller free-carrier absorption with shallow doping. The phase shifter is also fabricated and evaluated. The modulation efficiency and modulation loss are matching well with the simulation result, while the insertion loss of the passive hybrid waveguide is higher than the expectation, which requires more investigation. Meanwhile, an improved coupling taper is proposed and fabricated. The coupling loss is reduced from 0.2 dB/facet to 0.01 dB/facet experimentally, which is favorable for application in universal PICs.

In chapter 4, a numerical simulation method is presented to evaluate the

parasitic capacitance between the III-V and Si slab. The characteristics of slab parasitic capacitance and the influence on RC bandwidth are elaborated. Experimentally, a high-speed III-V/Si hybrid MOS optical phase shifter is fabricated, with a low  $V_{\pi}L$  of 0.245 V·cm and a 3 dB modulation bandwidth of 10 GHz. 25 Gbps NRZ eye diagram and 40 Gbps 4-levels pulse-amplitude modulation (PAM-4) eye diagram are obtained without pre-emphasis.

During the scaling up of the universal PICs, the number of phase shifters increases quadratically with the size of the PIC, indicating a drastic increase of contacts. To reduce the number of contacts for large-scale PICs, a cross-bar wiring configuration with pulse control is proposed in chapter 5. As a partial demonstration, TO phase shifters with on-chip PN diode switches are fabricated by the standard foundry process. The selection function and pulse amplitude control are achieved with PN diode switches. The idea is then extended to III-V/Si MOS optical phase shifters. The selection function and the pulse amplitude modulation are also demonstrated using an external control circuit and a fabricated III-V/Si MOS optical modulator. The power consumption is reduced by 700 times compared with the TO phase shifter.

In chapter 6, we introduced the established measurement system and the control software for the universal PICs. With a simulated annealing algorithm, we experimentally demonstrate the robust control and the broadband operation with a 4x4 thermo-optic universal PIC chip. We also introduce current progress in the fabrication of the III-V/Si MOS optical phase and the issues we are facing in the planarization and wafer bonding process.

In summary, the application of III-V/Si MOS optical phase shifter in universal PIC is evaluated. Phase shifters with low insertion loss and high modulation bandwidth are explored to maximize the performance of the circuit. The combination of III-V/Si MOS optical phase shifters and universal PIC is expected to be a promising hardware for optical computing.



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## *List of publications*

### **As first author:**

#### **Journal (1 published):**

1. H. Tang, Q. Li, C. Ho, J. Fujikata, M. Noguchi, S. Takahashi, K. Toprasertpong, S. Takagi and M. Takenaka, "High-speed InGaAsP/Si Hybrid MOS Optical Modulator with a High Modulation efficiency", *Optics Express*, vol. 30, no. 13, pp. 22848-22859, June 2022. DOI: 10.1364/OE.457444
2. H. Tang, R. Tang, M. Okano, K. Toprasertpong, S. Takagi and M. Takenaka, "Broadband Robust Configuration of 4x4 Universal PIC with Simulated Annealing", In preparation

#### **Conference (5 peer reviewed, 1 accepted):**

1. H. Tang, R. Tang, J. Fujikata, M. Noguchi, S. Takahashi, K. Toprasertpong, S. Takagi and M. Takenaka, "Crossbar Wiring for III-V/Si MOS Optical Phase Shifters with Diode Selectors", European Conference on Optical Communication (ECOC), Basel, Switzerland, September 18-22, 2022. (Oral accepted)
2. H. Tang, R. Tang, K. Toprasertpong, S. Takagi, and M. Takenaka, "Numerical analysis of distributed slab capacitance in III-V/Si hybrid MOS phase shifter" ISPEC 2021 Poster session: P-17, Virtual, Dec. 2021.
3. H. Tang, S. Ohno, Y. Miyatake, K. Toprasertpong, S. Takagi, M. Takenaka, "Thermo-optic Mach-Zehnder Interferometer Integrated with Si PN Diode Switch for Bipolar Optical Phase Control" Optical Fiber Communication Conference 2021, Tu5B.5, Virtual, June 2021.
4. H. Tang, S. Ohno, Y. Miyatake, K. Toprasertpong, S. Takagi, M. Takenaka, "Bipolar thermo-optic Mach-Zehnder interferometer with pulse-height modulation", The 68th JSAP Spring Meeting 2021, 18a-Z18-3, Virtual, March, 2021.
5. H. Tang, S. Takagi, and M. Takenaka, "Numerical analysis of Waveguide coupled graphene thermal emitter," The 2019 International Conference on Solid State Devices and Materials, 2019, C000070, Nagoya University, Nagoya, Aichi, Japan, September 2019.
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#### **Journal (3 published):**

1. Q. Li, C. P. Ho, H. Tang, M. Okano, K. Ikeda, S. Takagi, and M. Takenaka, "Si racetrack optical modulator based on the III-V/Si hybrid MOS capacitor", *Optics Express*, vol. 29.5, pp. 6824-6833, 2021.

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3. T. Piyapatarakul, H. Tang, K. Toprasertpong, S. Takagi and M. Takenaka, "Numerical analysis of optical phase modulator operating at 2  $\mu\text{m}$  wavelength using graphene/III-V hybrid metal-oxide-semiconductor capacitor", *Japanese Journal of Applied Physics* 61, no. SC (2022): SC1031.

**Conference (6 peer reviewed):**

1. F. Boeuf, C. Barrera, A. Fincato, H. Tang, S. Guerber, S. Monfray, S. Ohno, D. Fowler, I. Charlet, L. Gianini, A. Simbula, L. Maggi, M. Shaw, K. Toprasertpong, S. Takagi and M. Takenaka, "Silicon Photonics Beyond Optical Interconnects" 2021 IEEE International Electron Devices Meeting (IEDM), Session 29-2-invited Dec., 2021.
2. M. Takenaka, H. Tang, S. Ohno, Y. Miyatake, K. Watanabe, K. Toprasertpong, S. Takagi, "Outlook for deep learning based on Si programmable photonic circuit", *The 68th JSAP Spring Meeting 2021*, 17p-Z08-7, Virtual, March, 2021.
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5. Z. Lin, T. Lee, H. Tang, K. Toprasertpong, M. Takenaka, S. Takagi, "Improvement of ferroelectric properties of TiN/Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub>/Si gate stacks by inserting Al<sub>2</sub>O<sub>3</sub> interfacial layers" *The 67th JSAP Spring Meeting*, 14p-A303-10, March 2019.
6. T. Piyapatarakul, H. Tang, K. Toprasertpong, S. Takagi and M. Takenaka, "Computational analysis of optical phase modulation using graphene/III-V hybrid MOS capacitor", *ISPEC 2021 Poster session: P-17*, Virtual, Dec. 2021.