博士論文

Study on effects of mechanical strain and MOS interface formation process on the characteristics of 4H-SiC MOSFET

（機械的歪みおよび MOS 界面形成プロセスが 4H-SiC MOSFET 特性に与える影響の研究）

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Doctoral Dissertation

Study on effects of mechanical strain and MOS interface formation process on the characteristics of 4H-SiC MOSFET

A DISSERTATION SUBMITTED

TO DEPARTMENT OF MATERIALS ENGINEERING

SCHOOL OF ENGINEERING

THE UNIVERSITY OF TOKYO

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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Abstract

Metal-oxide-semiconductor field-effect transistor (MOSFET) has become the most commonly used power devices in recent years, particularly in low voltage applications. When applied in high voltage region, power MOSFET based on silicon (Si) suffered great conduction loss from high on-resistance. As a wide band-gap semiconductor material, silicon carbide (SiC) is promising to replace Si in high-voltage applications, for not only wider band-gap minimizes on-resistance but also it owns higher breakdown electric field than Si. In addition, the unique capability of SiC among compound semiconductors to thermally grow oxide makes it possible to transfer well established Si technologies to SiC devices.

For further improvement of the device reliability, more accurate tuning and suppression of variability of the threshold voltage (V_{th}) are expected. One of the concerns in SiC device reliability is the impact of inevitably induced strain. The occurrence of strain in SiC devices could be process-induced, e.g., locally induced strain due to wafer process such as trench etching in trench structure MOSFET, and globally induced thermal strain due to high temperature process. Systematic study in the change of V_{th} in strained SiC MOSFET is necessary to achieve precise V_{th} control. What's more, SiC MOSFET has been suffering extremely low mobility as

a consequence of poor SiO_2/SiC interface with high density of interface traps (D_{it}). With decrease in D_{it}, not only mobility could be improved but a more direct tuning of V_{th} by doping concentration would become accessible due to suppression of Coulomb scattering. Previous researches predicted that, strain in SiC could shield defects responsible for scattering and lead to improvement in mobility. Therefore, systematic studies in the change of mobility in strained SiC MOSFET as well as D_{it} reduction in SiO_2/SiC interface are both necessary for device efficiency enhancement.

Compared to commonly used 4H-SiC (0001) Si-face devices, (1-100) m-face is less investigated despite its potential. It's reported that bulk mobility in m-face is higher than that in Si-face, suggesting a potential of higher channel mobility in m-face device. One of the applications in m-face is to form the trench channel in trench MOSFET, where challenge occurs due to different oxidation rate between m-face and Si-face during gate oxide formation. Identical oxidation ambient results in difference in not only oxide thickness but also MOS interface quality, on m-face and Si-face. A systematic study is important in order to precisely control channel and gate oxide properties in trench structure.

In this work, we will investigate on impact of MOS process and mechanical stress on SiC MOSFET. We will report on traps and charges distribution regarding MOS process. Particularly, we would compare impact of identical process on (1-100) m-face and on (0001) Si-face, to evaluate the potential of m-face. We will quantify relationship between process condition and m-face capacitor properties to

optimize the process conditions. Moreover, we will describe the relationship quantitatively between mechanical stress and induced electrical properties change, focusing mobility, threshold voltage and flat-band voltage (V_{fb}), because threshold voltage consists of flat-band voltage so their change should be highly related. Finally, we will investigate in possible mechanisms that causes flat-band change under mechanical stress, especially band alignment change and oxide charge change.

To investigate in reliability of SiC device with electrical stress, we focused on the time dependence of stress' impact as well as repeatability of stress application, to evaluate distribution of charges from interface to oxide. We also reported on traps and charges distribution regarding process conditions. Especially, we compared MOS process' impact on (1-100) m-face with that on (0001) Si-face, with variables controlled by estimation based on oxidation rate.

To systematically investigate in impact of mechanical stress on SiC MOSFET, we utilized wafer bending method, focusing on change of mobility and threshold voltage. To estimate value of mechanical stress induced in SiC device, we applied identical bending method on Si MOSFET as well and compared the mobility change in Si with that in SiC. By comparing change of threshold voltage with change of flat-band voltage, we concluded that V_{th} change is mainly attributable to V_{fb} change with stress. The repeatability of V_{th} was verified by being observed under repeatedly applied and released mechanical stress.

To discuss possible origins of device performance change with mechanical stress, we first investigated in electron barrier height change in SiO_2/SiC interface to discuss band alignment change. We measured and estimated leakage currents from Fowler-Nordheim tunneling and from Poole-Frenkel emission under low temperature and room temperature, then derived electron barrier height under wafer bending. By plotting V_{fb} change in relation to oxide thickness as a function of stress, we noticed the change of fixed oxide charges which was mainly attributable to V_{fb} change. We also observed change in dipole layer which was comparable to electron barrier height change and also contributed to V_{fb} change. A difference between oxidized and deposited oxide in the change of fixed charges and dipole layer was observed. We suggested that conduction band edge lowering with stress might be the physical origin of observed impact in SiC MOSFET.

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Chapter 1

Introduction

1.1 Development and Limits of Si Power Device

The electronics industry has become the largest industry since 20th century. By 2023, the sales volume of electronics industry shall reach 3.5 trillion dollars [15] and take up 3% of gross world product [16]. It can be foreseen that the electronics industry will remain to be the largest industry throughout 21st century. As the foundation of electronics industry, the semiconductor industry has surpassed the steel industry in the beginning of 21st century and took up 17% of the electronics industry in 2022 [15].

The invention of transistor back in 1947 is of particular importance for ushering the modern electronic era. In 1960, the metal-oxide-semiconductor field-effect transistor (MOSFET), based on a thermally oxidized silicon (Si) substrate, was invented [17] and has become the most important device for integrated circuits since then. Though MOSFETs have been scaled down to nanometer regime nowadays, the choice of Si and thermally grown SiO_2 used in the first MOSFET

remains to be the most important combination of materials. MOSFETs and related integrated circuits take up about 97% of the semiconductor device market in 2022 [18].

With the increasing dependence of modern society on electrical appliances, it is expected that the electricity consumption shall occupy around 60% of the used energy in the next 20 years. To achieve sustainable development, it is a crucial challenge to seek more energy-efficient technology. In recent years, power electronics has received attention because it motivates great advancement in power generation, power distribution and power management technologies. It is estimated that at least half of the electricity used in the world is controlled by power devices [19], which are important consisting parts for inverter operation in the circuits.

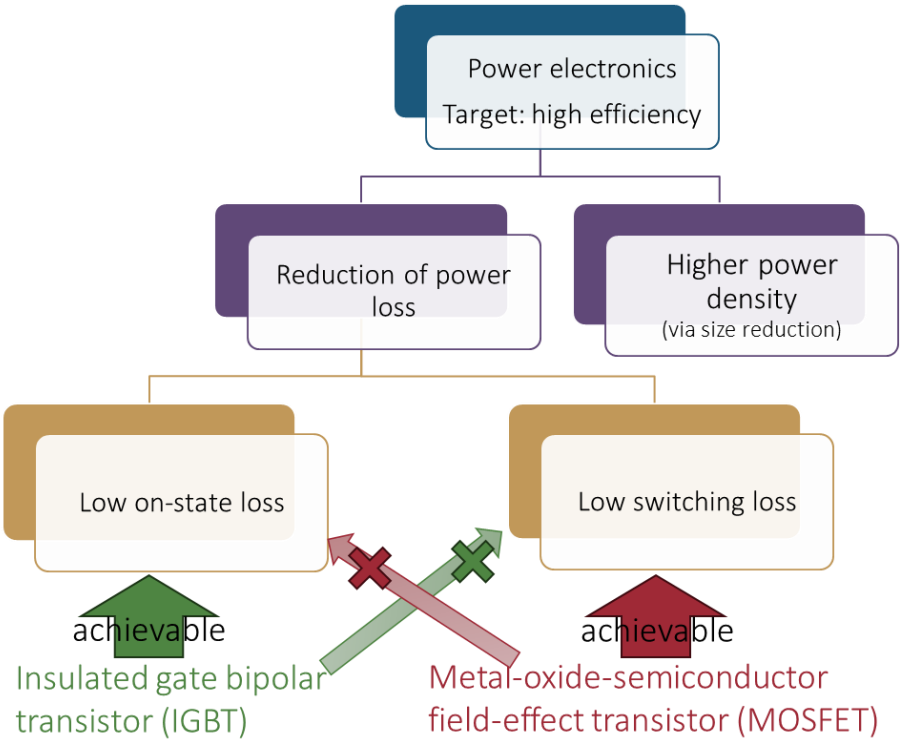

Figure 1.1 Major targets of power electronics and practical approaches.

The major targets of power electronics include higher power efficiency through the reduction of power loss and higher power density mainly through reduction of device size, as presented in **Fig. 1.1**. Power loss in power devices mainly consists of on-state loss and switching loss. The conventional application of power devices can be categorized into two classes [20][21]: 1) high-voltage and high-power system applications, and 2) low-voltage (<200V) and high-frequency switching application. Insulated Gate Bipolar Transistor (IGBT), commercially introduced in 1980s, has composed an important class in the first kind of application. Usually based on Si, IGBT is found to be the optimum solution to a broad range of systems that require operating voltages between 300 V and 3000 V and significant current handling capability. Yet, it has relatively slow switching speed and much switching loss, making it not a candidate as good as MOSFET for the second category. Limited by increasing on-resistance, Si-based MOSFETs are however not adopted by high voltage applications.

Ideally, all the resistances within device structure, apart from that of the drift region, are considered to be parasitic resistance that have been reduced to zero [22]. In this idealized case, the reduction of on-resistance has been simplified into reduction of the resistance of drift region, which is defined by [23]

$$R_{\mathrm{on-sp,ideal}} = \frac{4BV_{pp}^2}{\varepsilon_s \mu E_c^3}$$

Where BV_{pp} is the parallel-plane breakdown voltage, ε_s is the dielectric constant of semiconductor, μ is mobility, and E_c is the critical electric field for breakdown. This

resistance is referred as ideal specific on-resistance, and denominator of right side of equation $\varepsilon_s \mu E_c^3$ is referred as Baliga's Figure of Merit (BFOM), measuring inverse of specific on-resistance of the drift region. By calculation [23][24], it's predicted that there should be lower ideal specific on-resistance in wide band-gap semiconductor MOSFET devices; what's more, with wide band-gap material, it's promising for power devices to break the limit for conventional Si devices and have further application, even in high-voltage and high-power system.

1.2 Potential of SiC Power Device

Table 1.1 Electrical properties, physical properties and normalized BFOM for semiconductors at 300K.

Material	Si	4H-SiC [1]	GaN	β-Ga_2O_3
E_g (eV)	1.12	3.3	3.4	4.8 [25]
$\boldsymbol{\varepsilon}$	12	10 (⊥c-axis)	9 [26]	10 [27]
$\boldsymbol{\mu}$ (cm^2/Vs)	1450	1020 (⊥c-axis)	1000	100 [28]
E_C (MV/cm)	0.3	3.0 (⊥c-axis)	2.3	8 [29]
K (W/cmK)	1.6	3.7	1.3	0.1 [30]
BFOM	1	6×10^2	2×10^2	1×10^3

SiC is IV-IV compound semiconductor material containing silicon and carbon with ratio of 1:1. It has various crystal structures (polytypes) with their own unique electrical and optical properties [31][32]. The electric, physical properties and normalized BFOM of 4H-SiC are compared to that of Si and GaN and β-Ga_2O_3 in **Table 1.1**. SiC's wide band-gap E_g, high breakdown field E_C and high thermal conductivity K could lead to substantial performance improvement in many applications.

It can be read that gallium nitride (GaN) also shows potential to be applied for high-voltage application; however, at current stage, p-type GaN is difficult to be fabricated by ion implantation: magnesium (Mg), despite being a good acceptor,

cannot be activated by annealing. Moreover, growth and device fabrication technologies of SiC make it more suitable for mass production with lower cost in comparison. β-Ga_2O_3 also shows relatively larger band-gap and higher BFOM comparing to 4H-SiC, however, it has a very low thermal conductivity and low electron mobility, and lacks technologies for p-type device application. Therefore, we conclude that 4H-SiC is a promising candidate to replace Si in power devices. Successful application of SiC MOSFET for high-voltage purposes have been reported [33][34][35].

1.3 SiC Crystal Structure

The unit cell of SiC is tetrahedral, where each silicon atom is connected to exactly four carbon atoms and vice versa. SiC has more than 200 polytypes and can be divided into three basic crystallographic categories: cubic (C), hexagonal (H) and rhombohedral (R). Among the polytypes, 3C-SiC, 4H-SiC and 6H-SiC are most commonly investigated. 4H-SiC, particularly, owns wider band-gap and higher carrier mobility compared to other polytypes, which makes it to be the polytype choice for most SiC-based devices. **Fig. 1.2** shows schematic structures of popular SiC polytypes [1], where the silicon atoms labelled "h" and "k" denote the hexagonal sites and cubic sites, respectively.

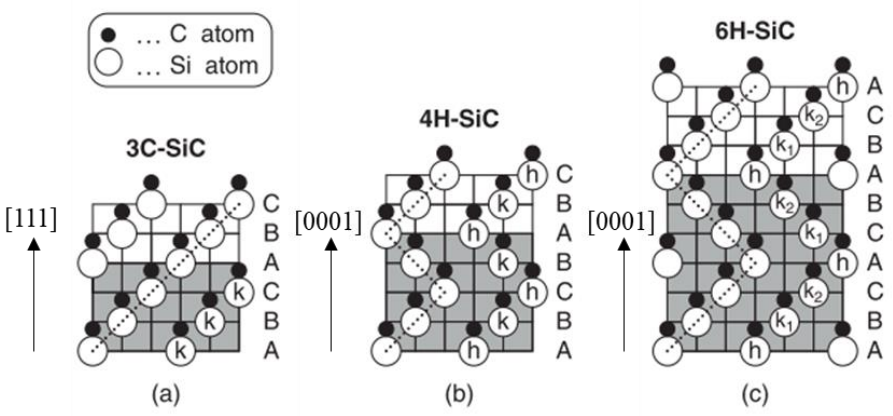

Figure 1.2 Schematic structures of SiC polytypes: (a) 3C-SiC, (b) 4H-SiC and (c) 6H-SiC [1].

Being a compound semiconductor, in SiC the valence electrons are slightly localized near carbon atoms, due to them being more electronegative than silicon atoms (C: 2.5, Si: 1.8). Then silicon atoms become partially positive charged and

carbon atoms become partially negative charged, resulting in polarity in SiC which is of particular importance in device design and fabrication.

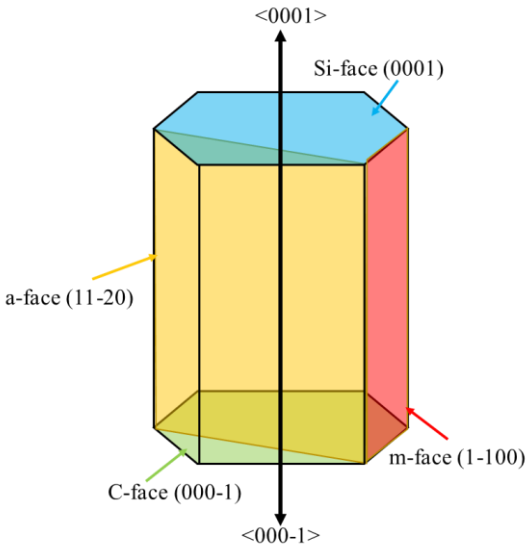

Figure 1.3 Definition of major planes in a hexagonal SiC polytype.

In a hexagonal structure, the (0001) face, where one bond from tetrahedrally bonded silicon atom is directed along the *c*-axis <0001>, is called Si-face, and the (000-1) face, where one bond from tetrahedrally bonded carbon atom is directed along the *c*-axis, is called C-face. **Fig. 1.3** illustrates several crystal faces in a hexagonal SiC polytype. Other than Si-face and C-face, the (11-20) face is called a-face and the (1-100) face is called m-face. The surface energy, chemical reactivity and electronic properties are reported to be significantly dependent on crystal orientations.

Si-face and C-face have been of the most investigated SiC crystal faces in past decades. Yet, along with the development of trench design MOSFET from late 1980s, m-face has drawn attentions for its application in this non-planar structure device. Trench design MOSFET (U-MOSFET), for example, is one of the non-planar structure devices designed to gain higher current density per area in high voltage application, due to its effective channel being larger than the projected area on chip. Compared to another common non-planar structure, vertical design MOSFET, the U-MOSFET has enabled significant reduction of resistance, which makes it more popular in commercial market.

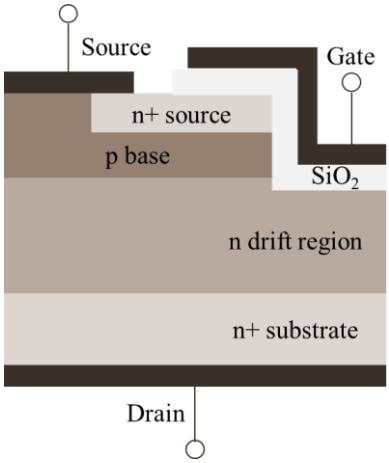

Figure 1.4 Trench-design MOSFET structure.

In trench design MOSFET, as shown in **Fig. 1.4**, the wall and bottom of trench are perpendicular to each other, corresponding with different crystal faces of SiC. For instance, when the bottom plane is formed by Si-face, then the trench wall could be m-face or a-face, etc. The anisotropy properties of crystal faces, including thermal oxidation rate, results in inadequate oxide thickness at the corner of the trench [36], and leads to potential failure in device as consequence.

In addition, it's also reported that m-face has potential to obtain higher mobility than Si-face, as shown in **Fig. 1.5** [2].

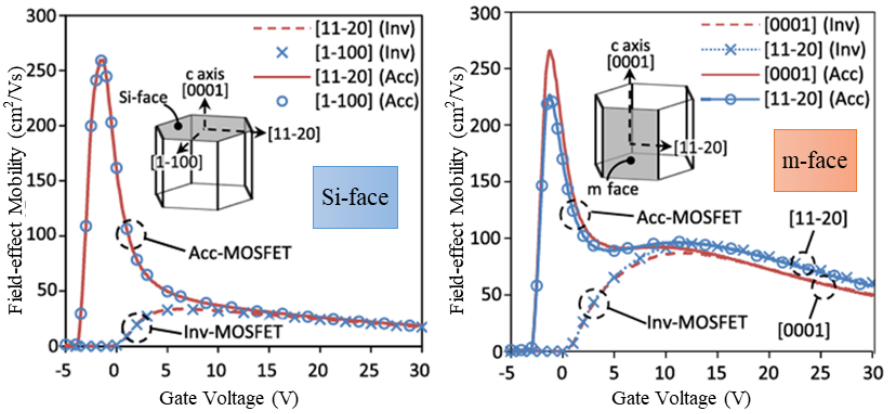

Figure 1.5 Field-effect mobilities on Si-face (left) and m-face (right) MOSFETs [2].

1.4 Oxidation of SiC

Besides the outstanding physical and electrical characteristics, there is another property of SiC that makes it unique as compound semiconductor [37]: the capability to form a native oxide insulator by chemical reaction with oxygen, as shown in following reaction

$$SiC + 1.5O_2 \rightarrow SiO_2 + CO$$

The amount consumed during thermal oxidation of SiC is calculated to be 46%, taking the SiC density in SiC into consideration [1], e.g., 46 nm of SiC will be consumed when growing 100 nm of SiO_2 on SiC. This value is close to the that for thermal oxidation of Si. During thermal oxidation, most of the carbon atoms in SiC are removed and diffuse as carbon monoxide (CO) molecules, while a small portion of carbon atoms diffuses into the SiC bulk region and lead to reduction of carbon-vacancy-related defects [38]. However, after thermal oxidation, there are still some carbon atoms remaining near the SiO_2/SiC interface, bringing difference into discussion of thermal oxidation of SiC.

1.4.1 Kinetics of Thermal Oxidation

This similarity to Si in ability to thermally grow oxide suggests the possibility that much of the technology and manufacturing processes shall be transferable. On

Si, it was well established that oxidation mechanism can be explained by Deal-Grove model [39] as

$$T_{ox}^2 + AT_{ox} = Bt$$

Here, T_{ox} is oxide thickness and t is the oxidation duration. B and B/A are called the parabolic rate constant and linear rate constant, respectively.

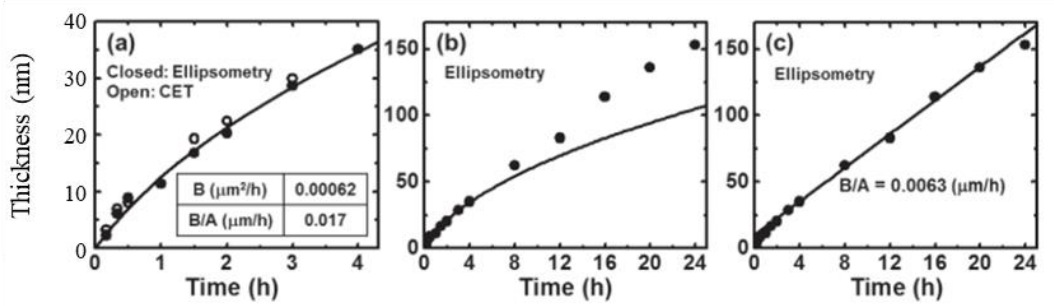

Figure 1.6 Oxide growth on 4H-SiC (0001) Si-face under dry O_2 ambient and 1150 °C. (a) Initial oxide growth within 4 hours where the solid line represents modified Deal-Grove fitting. (b) Results of prolonged dry oxidation up to 24 hours where solid line is extrapolated growth curve from the initial oxidation regimes shown in (a). (c) Validity of linear regression for a prolonged period from 4 to 24 hours, with a trustworthy linear rate constant estimated from the prolonged period [3].

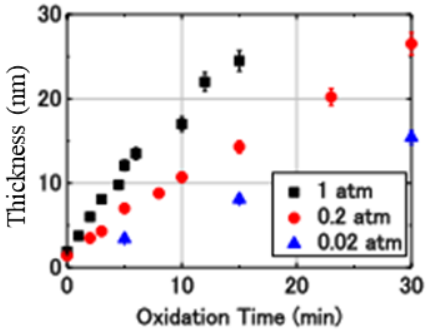

Figure 1.7 Oxide growth on 4H-SiC (0001) Si-face under ambients with various oxygen concentrations [4].

On SiC, a modified Deal-Grove model was developed to describe the oxidation kinetics [40], taking CO out-diffusion into consideration. **Fig. 1.6 (a)**

shows thickness growth over oxidation duration, measured by ellipsometry or estimated by oxide capacitance, with B and B/A extracted from modified Deal-Grove fitting. Comparison between **Fig. 1.6 (b)** and **(c)** leads to the conclusion that prolonged period (4 to 24 hours) corresponds to a real linear regime governed by interface reactions. Meanwhile, it is reported [4] that in very thin oxide, oxide growth is of linear relationship with oxidation duration, regardless of oxygen concentration in the ambient, as shown in **Fig. 1.7**.

A Si-C emission model is schematized in **Fig. 1.8**, where C, x, and D denote the concentration, distance from the interface and oxide thickness, respectively; R_1 and R_2 denote the reaction rate at the oxide surface and in the oxide, respectively [5]. This model has better explanation of oxide growth rate over entire thickness range for both C-face and Si-face, indicating that oxidation and emission of carbon and emission of silicon all need to be taken into consideration when describing the oxidation of SiC.

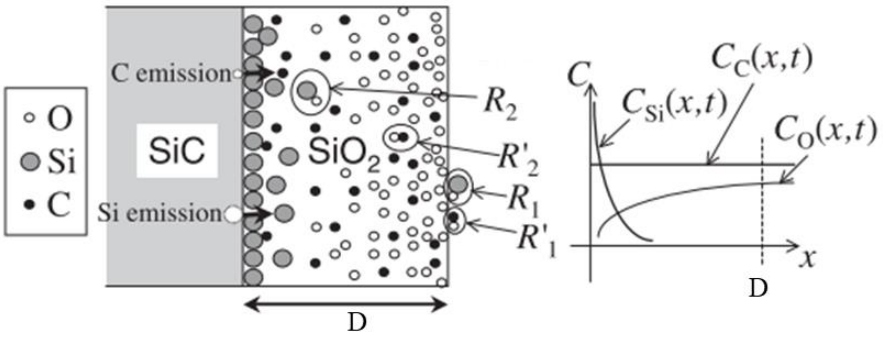

Figure 1.8 Schematic of the Si-C emission model [5].

1.4.2 Advanced MOS Fabrication Process

Despite the high expectations of SiC MOSFET, its practical performance doesn't exactly meet. One of the most serious problems in SiC MOSFET is the extremely low channel mobilities and high threshold voltage (V_{th}) instability. It's believed that those issues are mainly caused by carbon, the byproduct from thermal oxidation of SiC, which plays a detrimental role in the formation of high-quality oxide, associated to the generation of traps and charges in SiO_2/SiC interface and SiO_2 [35][41]. To improve the quality of oxide and SiO_2/SiC interface, optimized oxidation and related process in SiC MOS fabrication have been reported.

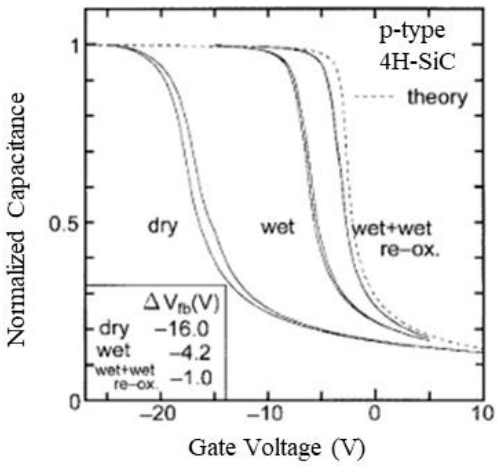

Figure 1.9 High frequency C-V curves of p-type 4H-SiC MOS capacitors measured under dark condition [6].

In addition to oxygen, water is also a commonly used oxidant which could produce wet thermal oxidation ambient [42]. Wet oxidation or annealing was reported to affect mobile charges, interface charges and fixed oxide charges near SiC MOS interface [6], as shown in **Fig. 1.9**, and suggesting the potential along with necessity to optimize wet oxidation or annealing condition to achieve better

device performance. In addition, it's reported that interface traps density (D_{it}) in MOS can be further reduced by replacing H_2O in ambient with H_2O_2 [43].

Surface etching with replacement of thermal oxidation with oxide deposition are also reported to be successful. Chemical vapor deposition (CVD) of SiO_2 without oxidation after hydrogen (H_2) etching of SiC surface greatly improves field-effect mobility (μ_{FE}) while not changing V_{th} for much [44].

In research above, nitridation with NO or N_2 was applied to passivate interface. Nitridation and post-oxidation annealing (POA) are two of popular methods for interface passivation. It's reported that POA in H_2O-containing or H_2-containing ambient is effective in suppressing D_{it} and improving field-effect mobility [45][6][46][47] by passivating defects on Si-face or C-face. It's noted that Hall mobility, however, isn't changed by nitridation or POA [48], indicating those processes don't have affect on drift velocity of carriers.

1.5 Strain in SiC MOSFET

For further improvement of the device reliability [49] of SiC MOSFETs, more accurate tuning and suppression of variability of the threshold voltage are expected [50][51]. A stable and relatively high V_{th} is important for high voltage power device, for the device can precisely switch between on and off status as system requires. For Si-based device, V_{th} can be adjusted by doping concentration in industrial application while maintaining the channel mobility. However, due to large amount of interface traps in SiC MOS structure, adjustment of doping concentration would not only change V_{th} but also affect channel mobility in SiC MOSFET, resulting in competition between a higher mobility and a sufficiently high V_{th} for operation [52].

Another concern in SiC device reliability is the impact of inevitably induced strain. The occurrence of strain in SiC devices could be process-induced, e.g., locally induced strain due to wafer process such as trench etching in advanced trench-channel MOSFETs [53][54], and globally induced thermal strain on the whole wafer due to high-temperature processes such as epitaxial layer growth, gate dielectric formation, contact formation, and so on [55]. Systematic study in the change of V_{th} in strained SiC MOSFET is necessary to achieve precise and uniform V_{th} control.

1.5.1 Developed Strain Engineering Technology in Si MOSFET

In n-type semiconductor, the electron mobility μ_e is determined by mean free time τ_C and effective mass of electron m_e^*

$$\mu_e = \frac{q\tau_C}{m_e^*}$$

The strain engineering can be applied on n-type Si to adjust carrier mobility by changing effective mass. There are six degenerate valleys in a bulk Si conduction band. Applied external stress shifts and splits these bands and result in repopulation of electrons. As shown in **Fig. 1.10** [7], tensile stress causes $\Delta 2$ subband energy to shift down and $\Delta 4$ energy to shift up, resulting in electrons repopulating from $\Delta 4$ valley to $\Delta 2$ valley. Due to conductivity effective mass in $\Delta 2$ valley (0.19 m_0) being smaller than that of $\Delta 4$ valley (0.315 m_0), the repopulation of electrons leads to decrease in average effective mass and increase in carrier mobility.

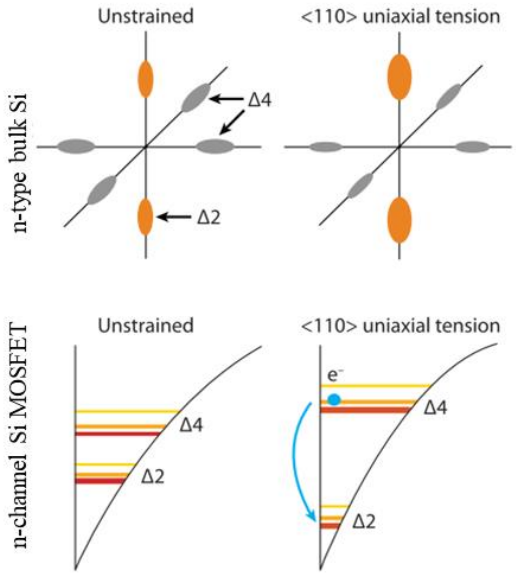

Figure 1.10 Simplified conduction band structure change under <110> uniaxial tensile stress for bulk n-type Si (above) and Si (100)-nMOSFETs (down) [7].

The strained Si n-MOSFETs, however, have distinct mobility enhancement factors from those in bulk Si. $\Delta 2$ and $\Delta 4$ valleys are non-degenerated in Si MOSFETs even for an un-strained one. For instance, the un-strained Si (100) n-MOSFET shown in **Fig. 1.10** has electrons predominantly occupy the lower-energy $\Delta 2$ valley, therefore effective mass change under stress would be different from that in bulk Si. Furthermore, while the dominant scattering mechanism in strained Si devices, intervalley phonon scattering, has lower scattering rate (due to smaller density of state) when subbands split and lead to higher mobility, however, the surface roughness scattering in commercial two-dimensional device makes current transport in Si n-MOSFET more difficult to be described in a predictable model.

The first Si MOSFET with biaxial stress induced by SiGe buffer layer was demonstrated in 1990s with 2.2-times enhancement in electron mobility and 1.5-times enhancement in hole mobility reported. After a while, the research focus has shifted to uniaxially stressed devices. In early 2000s, uniaxial stress was first introduced into MOSFET to successfully enhance its performance and has been experiencing innovations and industrial application since then.

1.5.2 Prediction of Strain's Impact in Bulk SiC

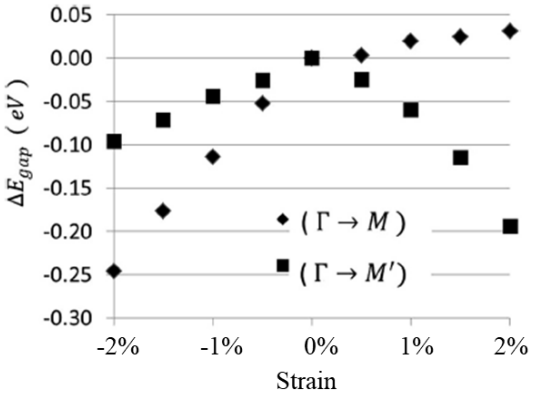

Figure 1.11 The change in the band-gap is reported as a function of percent lattice strain [8].

Despite well established in Si-based devices, strain engineering is still a novel technology for SiC. Density functional calculations were used to predict energy band and electron effective mass of strained bulk 4H-SiC, as presented in **Fig. 1.11** and **Fig. 1.12** [8], respectively.

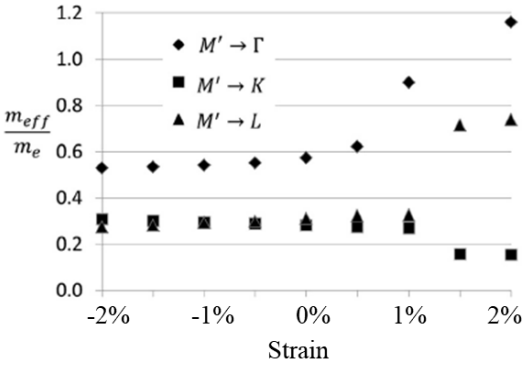

Figure 1.12 The effective masses (m_{eff}/m_e) are reported as a function of percent lattice strain [8].

In the aspect of band structure, for compressive strain, the band minimum transition is from Γ to M; for tensile strain, the transition is from Γ to M'. For both compressive and tensile strain, the band-gap lowers for ~0.2 eV at strain of 2%. Such band-gap reduction is suggested to be due to conduction band lowering,

and probably will work in shielding interface traps then improving mobility. The energy difference between two curves shows the intervalley splitting between the two minima and tensile strain results in a larger intervalley splitting than compressive strain. This intervalley slitting is assumed to reduce the intervalley electron scattering.

In the aspect of effective mass, minor change was observed under compression yet significant change appeared under tension. When un-strained, anisotropy is reported in 4H-SiC: in-plane mass along $M-\Gamma$ is of 0.6, twice higher than in-plane mass along $M-K$ and c-axial mass along $M-L$ [50]. Such anisotropy was also observed in mass change when strained. It was also noted that conductivity mass, which is more important for transport along channel of a MOSFET, decreased to half of that in unstrained bulk SiC with 1.5% of tensile strain. If strained SiC MOSFET has similar mobility enhancement factors as in strained bulk SiC, then those results suggest potential of mobility enhancement in SiC MOSFET with tensile strain.

1.6 Research Objectives

Advanced process is one of effective ways for the improvement of SiO_2/4H-SiC interface quality. Despite having potential to obtain higher mobility, the researches on m-face surface are so few. To reduce failure and improve efficiency in trench structure SiC MOSFET, the thermal oxidation mechanism and optimized process conditions on m-face should be investigated.

Strain engineering is a well-established technology for Si MOSFET but still novel to SiC device. The calculation of band-gap and effective mass in strained bulk SiC predicts the potential to apply strain engineering in SiC device for performance enhancement. Meanwhile, local or global strain is also reported to be induced by process and threats to the reliability of SiC device. To exclude variables introduced by different process, the mechanical stress should be introduced by a wafer bending method to show stress' solo impact on device. In addition, due to application of m-face in MOSFET is limited in wall of trench structure at current development stage, the mechanical stress is better to be applied on Si-face planar MOSFET in this study for simplicity and general discussion. Mechanical stress' impact on mobility and threshold voltage should be investigated and the possible origins of such impact should be discussed.

Therefore, the objectives of this research can be written as follows:

1) Investigation of the impact of MOS formation process on m-face SiC MOS capacitor performance.
2) Investigation of impact of mechanical stress on Si-face SiC MOSFET device performance.
3) Understanding of the possible origins of stress-induced performance change in Si-face SiC MOSFET

1.7 Outline of Thesis

Systematic study on impact of MOS formation process and mechanical stress, respectively, on the efficiency and reliability of 4H-SiC MOSFET are summarized in this thesis.

In **Chapter 1**, the physical properties of 4H-SiC, detailed explanation of thermal oxidation and annealing's impact on Si-face SiC MOS capacitor, strain engineering's application in Si MOSFET and previous study on introducing strain onto SiC are summarized. The motivation and detail of research objectives are also included in this chapter.

In **Chapter 2**, the details of fabrication methods and the electrical characterization technique are introduced. The fabrication methods include thermal oxidation and annealing. The characterization technique includes electrical characteristics measurement and grazing incident X-ray diffractometry.

In **Chapter 3**, we investigated the thermal oxidation mechanism on m-face surface and specified MOS formation process' impact on m-face MOS capacitor. The m-face was observed to be more reactive to oxygen than Si-face, resulting in faster oxide growth and more instable MOS characteristics.

In **Chapter 4**, we investigated the mechanical stress' impact on SiC MOSFET electrical characteristics. In addition to mobility change, we observed anomalous change of threshold voltage which was suggested to be attributable to change of flat-band voltage.

In **Chapter 5**, we investigated possible origins of observed stress-induced change in performance. Fixed oxide charge density change is considered to mainly contribute to the observed change of flat-band voltage, along with minor contribution from dipole layer change at SiO_2/SiC interface. Both fixed charges change and interface dipole layer change are affected by MOS formation process. The origin of fixed charges change is suggested to be conduction band lowering.

In **Chapter 6**, we summarized this study. We emphasized important points of m-face oxidation and annealing known from this study. Also, a systematic investigation of mechanical stress-induced performance change in SiC MOSFET and clarification of possible origins are summarized.

Chapter 2

Fabrication and Characterization Methods

2.1 Fabrication of SiC MOS Capacitor

2.1.1 Substrate Cleaning

(I) IPA cleaning (when necessary)

Samples are put into isopropyl alcohol (IPA), placed in running ultrasonic cleaner for 5 min, then rinsed in deionized water (DIW) for twice.

(II) RCA cleaning

SPM (sulfuric acid-hydrogen peroxide mixture) solution is produced by mixing concentrated sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in the volume ratio of 4:1. Samples are put into SPM solution and heated at 120 ℃ for 5 min to remove organic and metal contaminant, followed by rinsing twice in DIW.

HPM (hydrochloric acid-hydrogen peroxide mixture) solution is produced by mixing concentrated hydrochloric acid (HCl), DIW and H_2O_2 in the volume ratio of 1:6:1. Samples are put into HPM solution and heated at 80 ℃ for more than 6 min to remove metal contaminant, followed by rinsing twice in DIW.

The sequence of SPM and HPM refers to the Radio Corporation of America (RCA) cleaning.

(III) HF etching

Hydrofluoric acid (HF) with 5% concentration is utilized to remove oxide layer on SiC substrate. Etching rate of SiO_2 in this concentration is about 40 nm/min so 2 min is enough to remove naturally grown oxide layer on SiC.

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

Samples are rinsed in DIW at least twice then.

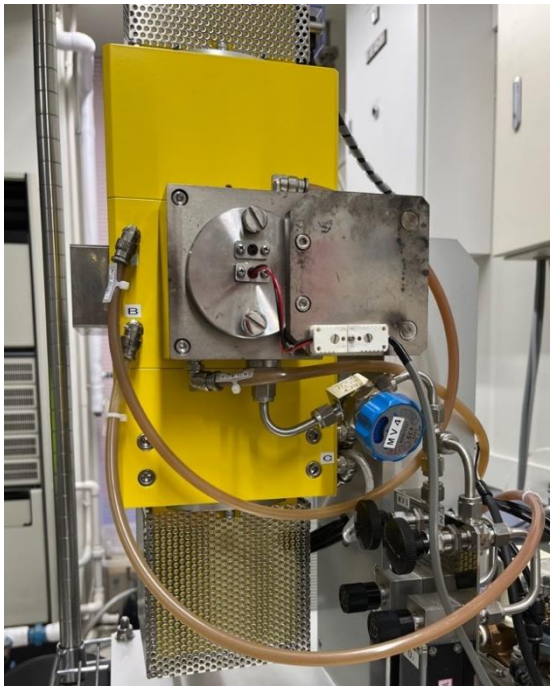

Figure 2.1 Advance Rico HT-RTA59HD as dry oxidation furnace.

2.1.2 Dry Oxidation

Dry oxidation process is done in High Temperature Rapid Thermal Annealing System produced by Advance Riko, HT-RTA59HD, as shown in **Fig. 2.1**. This system includes lamp-heating rapid thermal annealing furnace which could heat up to 1800 ℃ and temperature controller which could precisely control temperature in rapid heating or cooling process.

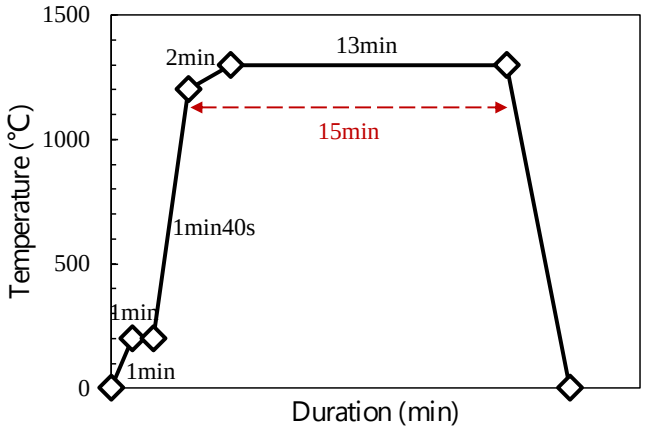

Figure 2.2 High-temperature oxidation process in HT-RTA59HD.

A common dry oxidation process is described in **Fig. 2.2**. We heated furnace from room temperature to 200 ℃ in 1 min and held the temperature for another 1 min to remove residual water from the wafer. We then increased the temperature in the speed of 10 ℃/min up to 100 ℃ lower than theoretical oxidation temperature and had a 2-min segment to increase the leftover 100 ℃. This 2-min segment was designed to prevent overheating, hence the duration of high-temperature oxidation process started from the beginning of this 2-min segment. After the high-temperature segment, the furnace started to cool down rapidly; if higher quality of SiO_2/SiC interface was required, the cooling down process could be adjusted into

much slower, with ambient shifted to pure nitrogen and temperature decrease speed set at 2 ℃/min. We took the sample out of furnace when temperature fell to 80℃.

2.1.3 Wet Oxidation/Annealing

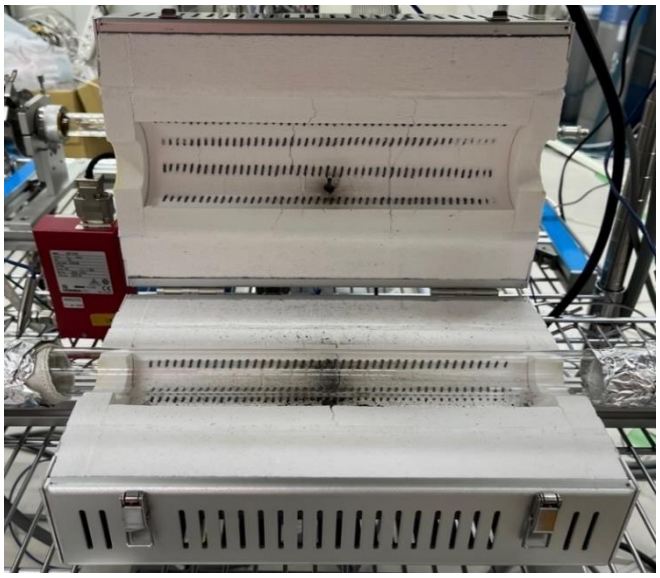

Figure 2.3 Quartz tubular furnace as wet oxidation furnace.

Wet (H_2O-containing) oxidation or annealing process is done in tubular quartz furnace, as shown in **Fig. 2.3**.

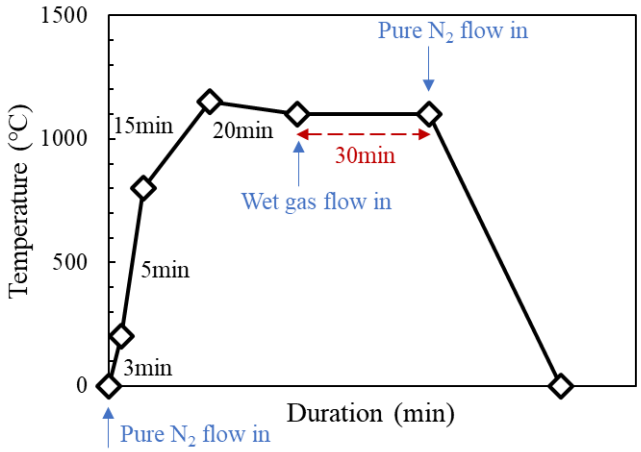

Figure 2.4 Oxidation process in tubular furnace.

A common wet oxidation process is described in **Fig. 2.4**. We heated furnace from room temperature to 200 ℃ in 3 min, then to 800 ℃ in 5 min. From here, we used 15 min to increase the temperature to 50 ℃ higher than theoretical oxidation temperature and had a following segment with comparable duration (this duration depends on segment's beginning temperature, e.g., if 1150 ℃, then 20min; if 1050 ℃, then 10 min) to decrease 50 ℃. These two segments were designed to speed up temperature rise. After the oxidation segment, the furnace started to cool down slowly. Note that wet gas was only flowed in during the oxidation segment; before and after this segment, we flowed pure N_2. SiC can hardly be oxidized in pure N_2 ambient under temperature as low as 1150 ℃, therefore possible oxide growth when not flowing wet gas could neglected.

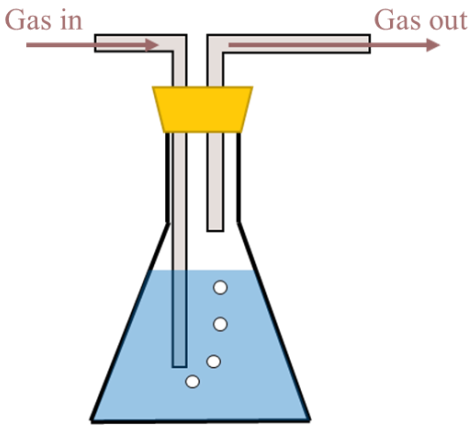

Figure 2.5 Bubbling method to produce wet ambient.

The wet ambient is produced by bubbling method, as shown in **Fig. 2.5**.

The partial pressure of water (pH_2O) in ambient should remain constant during the oxidation process. This can be achieved by taking control on water temperature [56], described in **Eq. 2.1**:

$$p = 6.1121\exp\left(\frac{17.123T}{234.95 + T}\right) \quad (2.1)$$

Here, p is equilibrium partial pressure of water in hPa and T is water temperature in Celsius. **Table 2.1** presents commonly used values of pH_2O and T_{H2O} in this research.

Table 2.1 Equilibrium partial pressure of water controlled by water temperature.

T_{H2O} (℃)	60	76	86	97
pH_2O (atm)	0.2	0.4	0.6	0.9

2.1.4 Electrode Deposition

For MOS capacitor characteristics measurement, we deposited gold (Au) and aluminum (Al) as gate electrode and substrate electrode. **Fig. 2.6** shows the turbomolecular pump (TMP) vacuum evaporator VE-2012 for metal evaporation. First, we used a mask to deposit Au on wafer surface with estimated layer thickness

of 80 nm; then we deposited Al layer on whole substrate back with estimated thickness of 50 nm.

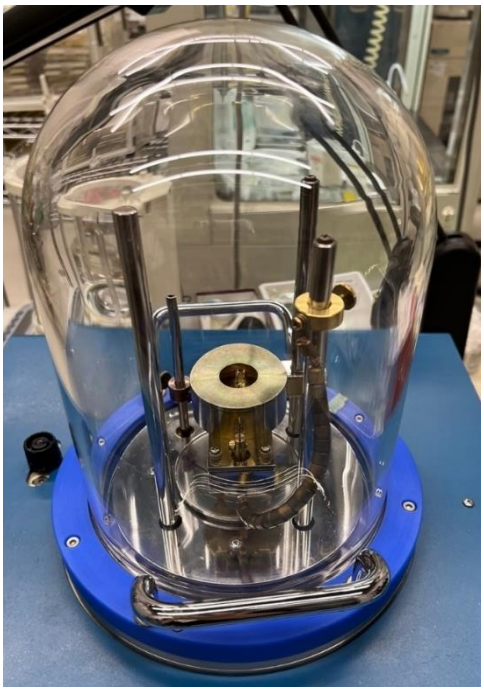

Figure 2.6 Metal evaporator for electrode deposition.

2.2 Characterization Methods

2.2.1 Capacitance-Gate Voltage Characteristics in Ideal MIS Capacitor

An ideal metal-insulator-semiconductor (MIS) capacitor is defined as follows [9]: *"(1) The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those, with an equal but opposite sign, on the metal surface adjacent to the insulator, i.e., there is no interface trap nor any kind of oxide charge; (2) There is no carrier transport through the insulator under dc biasing conditions or the resistivity of the insulator is infinite. Furthermore, for the sake of simplicity we assume the metal is chosen such that the difference between the metal function and the semiconductor work function is zero."*

Based on ideal MIS structure model above, we are capable to derive the capacitance-gate voltage (C-V) relationship. When the difference of work function is absent, the gate voltage applied will partly appear across insulator and partly appear semiconductor. Thus

$$V = V_i + \psi_s$$

where ψ_s is the surface potential on semiconductor, and V_i is the potential across insulator, given by

$$V_i = \frac{Q_g}{\varepsilon_i} d = \frac{Q_g}{C_i}$$

Q_g is the charges per unit on metal. For charge neutrality of system, it's required that

$$Q_g = -Q_s$$

where Q_s is the total charges per unit in the semiconductor.

Therefore

$$V = \frac{|Q_s|}{C_i} + \psi_s \tag{2.2}$$

The total capacitance C of system is a series combination of insulator capacitance

$$C_i = \frac{\varepsilon_i}{d} \tag{2.3}$$

and the semiconductor depletion-layer capacitance C_d

$$C = \frac{C_i C_d}{C_i + C_d} \tag{2.4}$$

For a given insulator thickness d, the value of C_i is constant and corresponds to the maximum capacitance of the system; however, C_d in semiconductor does not only depend on ψ_s, but also relates to the measurement frequency.

Here, we are going to obtain C_d under low measurement frequency, differentiating the total charges in semiconductor side Q_s with respect to its surface potential ψ_s

$$C_d = \frac{\mathrm{d}Q_s}{\mathrm{d}\psi_s} \tag{2.5}$$

With E_i being the intrinsic Fermi level, we define potential $\psi_p(x)$ as $E_i(x)/q$ with respect to the bulk of the semiconductor;

$$\psi_p(x) = -\frac{[E_i(x) - E_i(\infty)]}{q}$$

where ψ_p is positive when the band bends downward (as shown in **Fig. 2.7**). The electron and hole concentrations as a function of ψ_p are given by the following relationships:

$$n_p(x) = n_{po}\exp\left(\frac{q\psi_p}{k_BT}\right) = n_{po}\exp(\beta\psi_p)$$

$$p_p(x) = p_{po}\exp\left(-\frac{q\psi_p}{k_BT}\right) = p_{po}\exp(-\beta\psi_p)$$

n_{po} and p_{po} are the equilibrium concentrations of electrons and holes in p-semiconductor, respectively; $\beta = q/k_BT$.

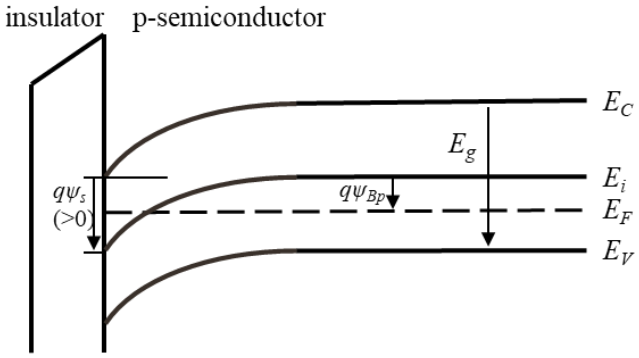

Figure 2.7 Band diagram at the surface of a p-type semiconductor in MIS structure.

At the semiconductor surface, $\psi_p(0) = \psi_s$; as mentioned before, ψ_s is called surface potential. The concentrations at the surface are

$$n_p(0) = n_{po}\exp(\beta\psi_s)$$

$$p_p(0) = p_{po}\exp(-\beta\psi_s)$$

By utilizing Poisson equation:

$$\nabla^2\psi = -\frac{\rho}{\varepsilon}$$

with total space-charge density $\rho(x) = q\left(N_D^+ - N_A^- + p_p - n_p\right)$ and the concentrations of ionized donors (N_D^+) and acceptors (N_A^-), we can obtain

$$\frac{d^2\psi_p}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q}{\varepsilon_s}\left(N_D^+ - N_A^- + p_p - n_p\right)$$

Consider somewhere in the semiconductor bulk, far away from its surface, in where the charge neutrality must exist. Therefore at $\psi_p(\infty) = 0$, we shall have

$$\rho(\infty) = q\left(N_D^+ - N_A^- + p_{po} - n_{po}\right) = 0$$

and

$$N_D^+ - N_A^- = -\left(p_{po} - n_{po}\right)$$

Therefore, the Poisson equation within depletion region can be expressed as

$$\frac{d^2\psi_p}{dx^2} = -\frac{q}{\varepsilon_s}\left(-p_{po} + n_{po} + p_p - n_p\right)$$

$$= -\frac{q}{\varepsilon_s}\left\{n_{po}\left[1 - \exp\left(\beta\psi_p\right)\right] - p_{po}\left[1 - \exp\left(-\beta\psi_p\right)\right]\right\} \qquad (2.6)$$

Now, integrate the left and right sides of the **Eq. 2.6**. For left side, by introducing the electric field $\mathfrak{E} = -d\psi_p/dx$, we have

$$\int_0^{d\psi_p/dx} \left(d\psi_p/dx\right) d\left(d\psi_p/dx\right) = \frac{1}{2}\left(d\psi_p/dx\right)^2 = \frac{1}{2}\mathfrak{E}^2 \qquad (2.7)$$

For the right side,

$$\int_0^{\psi_p} -\frac{q}{\varepsilon_s}\{n_{po}[1-\exp(\beta\psi_p)]-p_{po}[1-\exp(-\beta\psi_p)]\}\,d\psi_p$$

$$=\frac{q}{\beta\varepsilon_s}\{p_{po}[\beta\psi_p+\exp(-\beta\psi_p)-1]+n_{po}[-\beta\psi_p+\exp(\beta\psi_p)-1]\} \qquad (2.8)$$

Equate **Eqs. 2.7** and **2.8**,

$$\mathfrak{E}^2=\frac{2q}{\beta\varepsilon_s}\{p_{po}[\beta\psi_p+\exp(-\beta\psi_p)-1]+n_{po}[-\beta\psi_p+\exp(\beta\psi_p)-1]\}$$

$$=2\frac{1}{\beta^2}\frac{\beta p_{po}q}{\varepsilon_s}\left\{[\beta\psi_p+\exp(-\beta\psi_p)-1]+\frac{n_{po}}{p_{po}}[-\beta\psi_p+\exp(\beta\psi_p)-1]\right\}$$

From here, we introduce the extrinsic Debye length for holes

$$L_D=\sqrt{\frac{\varepsilon_s}{\beta p_{po}q}} \qquad (2.9)$$

and define a function for abbreviation as

$$F\left(\beta\psi_p,\frac{n_{po}}{p_{po}}\right)=\sqrt{[\beta\psi_p+\exp(-\beta\psi_p)-1]+\frac{n_{po}}{p_{po}}[-\beta\psi_p+\exp(\beta\psi_p)-1]} \qquad (2.10)$$

Then, the electric field can be written as

$$\mathfrak{E}(x)=\pm\frac{\sqrt{2}}{\beta L_D}F\left(\beta\psi_p,\frac{n_{po}}{p_{po}}\right)$$

the positive and negative signs correspond to $\psi_p>0$ and $\psi_p<0$, respectively.

At the surface, we have $\psi_p=\psi_s$ and the electric field

$$\mathfrak{E}_s=\pm\frac{\sqrt{2}}{\beta L_D}F\left(\beta\psi_s,\frac{n_{po}}{p_{po}}\right) \qquad (2.11)$$

By applying Gauss's law, we can obtain the total space-charge per unit area in this surface field

$$Q_s = -\mathfrak{E}_s \varepsilon_s = \mp \frac{\sqrt{2}\varepsilon_s}{\beta L_D} F\left(\beta\psi_s, \frac{n_{po}}{p_{po}}\right) \tag{2.12}$$

Now, we can derive the relationship between the semiconductor depletion-layer capacitance C_d and surface potential ψ_s by differentiating Q_s with respect to ψ_s (**Eq. 2.5**),

$$C_d = \frac{\mathrm{d}Q_s}{\mathrm{d}\psi_s} = \frac{\sqrt{2}\varepsilon_s}{\beta L_D} \frac{dF\left(\beta\psi_s, n_{po}/p_{po}\right)}{d\psi_s}$$

$$= \frac{\varepsilon_s}{\sqrt{2}L_D} \frac{[1 - \exp(-\beta\psi_s)] + n_{po}/p_{po}\,[-1 + \exp(\beta\psi_s)]}{F\left(\beta\psi_s,\ n_{po}/p_{po}\right)} \tag{2.13}$$

Eq. 2.13 describes depletion-layer capacitance's change with surface potential as free variable, except at $\psi_s = 0$, so-called as flat-band condition, since function F approaches zero. In this case, C_d could be obtained from **Eq. 2.13** by expanding the exponential terms into series.

Thus

$$C_d(\text{flatband}) = \frac{\varepsilon_s}{L_D} \tag{2.14}$$

The total capacitance C of MIS system can be obtained from **Eq. 2.4** once C_d and C_i are known. Particularly, C under flat-band condition ($\psi_s = 0$)

$$C_{fb} = \frac{C_i C_d(\text{flatband})}{C_i + C_d(\text{flatband})} = \frac{\frac{\varepsilon_i}{d}\frac{\varepsilon_s}{L_D}}{\frac{\varepsilon_i}{d} + \frac{\varepsilon_s}{L_D}} = \frac{\varepsilon_i \varepsilon_s}{\varepsilon_i L_D + d\varepsilon_s} = \frac{\varepsilon_i \varepsilon_s}{\varepsilon_i \sqrt{\varepsilon_s/\beta N_A q} + d\varepsilon_s} \tag{2.15}$$

To draw the ideal C-V curve, we also need to extract the relationship between gate voltage and surface potential. Based on the assumption that flat-band voltage $V_{fb} = 0$, **Eq. 2.2** can be applied for V-ψ_s relationship.

However, as in practical MIS structure where the oxide charges always exist, there should be a voltage shift due to the oxide charges' existence. According to Gauss' law

$$\Delta V = -\frac{1}{C_i}\left[\frac{1}{d}\int_0^d x\rho(x)dx\right]$$

$\rho(x)$ here is the charge density per volume.

Since this voltage shift is a fixed value for certain MIS structure, it should equal to the flat-band voltage shift when $\psi_s = 0$. When the insulator thickness d and concentration of acceptors N_A are known, system capacitance at flat-band condition C_{fb} can be obtained from **Eq. 2.15**. With measured C-V data, the corresponding V_{fb} can be determined by C_{fb}. Then **Eq. 2.2** is adapted into

$$V = \frac{|Q_s|}{C_i} + \psi_s + V_{fb} \tag{2.16}$$

By **Eqs. 2.5** and **2.16**, the ideal C-V relationship can be completely derived with the only independent variable ψ_s.

2.2.2 Interface Trapped Charges and Oxide Charges in Practical MIS Capacitor

The ideal C-V relationship discussed in last part is based on following assumptions: (1) Neither interface traps nor oxide charges exist; (2) Insulator resistivity is infinite; (3) No work function difference between semiconductor and metal. For a practical MIS capacitor, however, interface traps and oxide charges exist that will, in one way or another, affect the MIS characteristics.

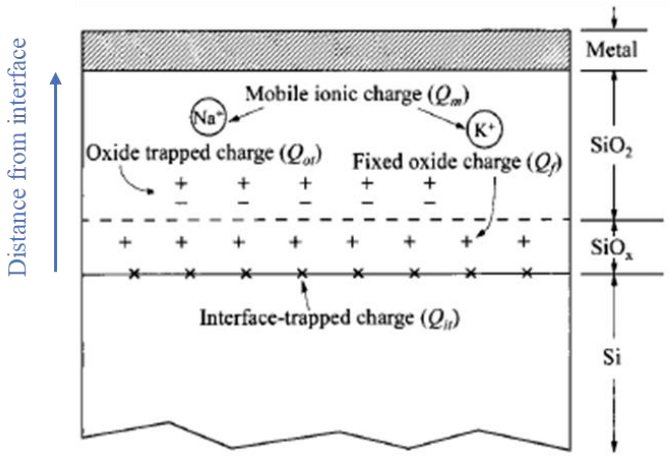

Figure 2.8 Terminology of charges associated with thermally oxidized Si [9].

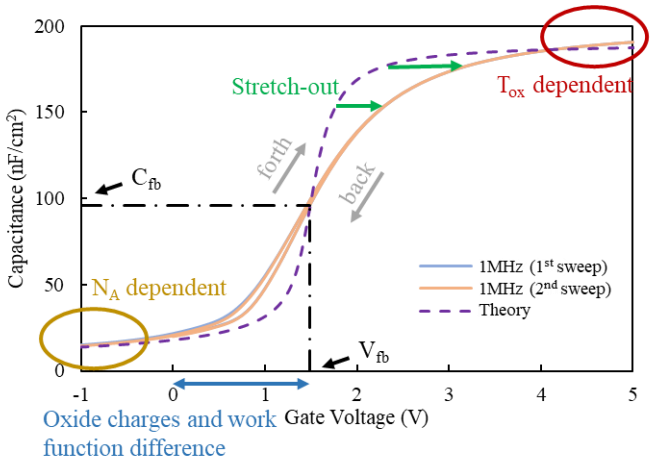

Figure 2.9 Measured C-V and ideal C-V on SiC MOS capacitor.

Fig. 2.8 shows the distribution of traps and charges in metal-oxide-semiconductor (in this research, gate material-SiO_2-SiC). Interface trapped charges Q_{it} locate in oxide/semiconductor interface with energy states within semiconductor band-gap, and can exchange charges with semiconductor in a short time. Oxide charges Q_{ox} locate in oxide or near interface and part of them would be mobile within oxide under bias-temperature stress conditions. The impact of traps and charges on C-V curve is shown in **Fig. 2.9**.

Various information can be implied from practical C-V curves. Compared with ideal (calculated) C-V, the existence of interface traps causes a significant stretch-out in the voltage direction. The hysteresis (a lag between curves swept from opposite polarities) can be observed when there are near-interface charges in MOS. The maximum capacitance refers to the insulator (oxide) capacitance $C_i = C_{ox}$, and is decided by oxide thickness T_{ox} (or electrically, capacitance equivalent thickness CET). The depletion region of C-V is related to doping concentration N as

$$N = -\frac{2}{q\varepsilon_s} \div \frac{d(1/C_d)^2}{dV} = -\frac{2}{q\varepsilon_s} \div \frac{d(1/C - 1/C_{ox})^2}{dV}$$

With known CET and N, capacitance under flat-band condition C_{fb} can be derived by **Eq. 2.15**. We can then read the corresponding flat-band voltage V_{fb} from the measured C-V by C_{fb}. Due to a common existence of hysteresis in C-V on SiC capacitor, in this thesis we read V_{fb} only from the back sweep. With existence of oxide charges and work function difference between metal and semiconductor, practical V_{fb} is usually non-zero.

Figure 2.10 E4980 for MOS capacitor characteristics measurement.

To evaluate the quality of an MIS capacitor, both the information of interface traps and of oxide charges are important. In the following two parts, we introduce

the electrical characterization methods of interface traps and oxide charges. Measurement in both sections were done through Precision LCR Meter produced by KEYSIGHT, E4980A, as shown in **Fig. 2.10**.

2.2.3 Evaluation of Interface Traps

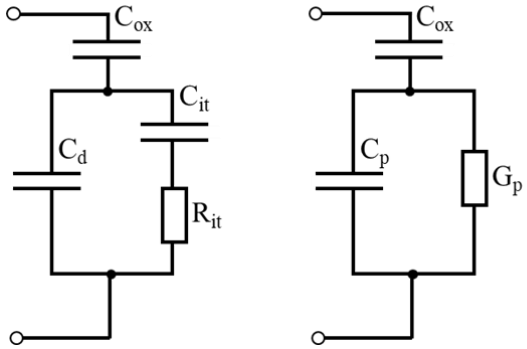

Figure 2.11 The equivalent circuits of MIS including interface-trap effects.

Fig. 2.11 (left) shows the equivalent circuits of MIS, with C_{it} and R_{it} being the capacitance and resistance related to interface traps. The product $C_{it}R_{it}$ is defined as the interface-trap lifetime τ_{it}, which determines the frequency behavior of the interface traps. The total terminal capacitance for low-frequency limit and high-frequency limit are

$$C_{LF} = \frac{C_{ox}(C_d + C_{it})}{C_{ox} + C_d + C_{it}} \tag{2.17}$$

$$C_{HF} = \frac{C_{ox}C_d}{C_{ox} + C_d} \tag{2.18}$$

The parallel branch of the equivalent circuit in **Fig. 2.11** (left) can be converted into a frequency-dependent capacitance C_p in parallel with a frequency-dependent conductance G_p, as shown in **Fig. 2.11** (right).

$$C_p = C_d + \frac{C_{it}}{1 + \omega^2 {\tau_{it}}^2} \tag{2.19}$$

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1 + \omega^2 {\tau_{it}}^2} \tag{2.20}$$

Either the measurement on capacitance or conductance can be used to evaluate density of interface traps. In general, conductance method gives more accurate result while capacitance method is easier to operate.

For n-type MOS capacitor, we usually plot D_{it} as function of energy level from the bottom of conduction band E_c-E in unit of eV, which can be obtained by

$$E_c - E = \left(E_c - E_f\right) - \psi_s$$

Here, $E_c - E_f$ is Fermi level from the bottom of conduction band, determined by temperature T, Debye length L_d and effective density of states in conduction band in 4H-SiC N_c, which is given by [57]

$$N_c = 3.25 \times 10^{15} \times T^{3/2}$$

Under room temperature, N_c=1.67×10^{19} cm^{-3} and $E_c - E_f = 0.19$ eV. In D_{it} research, we usually focus on energy level of $E_c - E = 0.2$ eV because it locates near to Fermi level.

High-Low Frequency Capacitance Method [9]

From **Eqs. 2.17** and **2.18**, the expression of C_{it} can be obtained.

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - C_d$$

$$= \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \quad (2.21)$$

Since interface-trap levels are distributed across the energy band-gap, we characterize them by an interface-trap density distribution:

$$D_{it} = \frac{1}{q}\frac{\mathrm{d}Q_{it}}{\mathrm{d}E} \quad (2.22)$$

E is energy level. The unit of D_{it} is number of traps/eV·cm^2. Since $\mathrm{d}E = q\mathrm{d}\psi_s$, then

$$C_{it} \equiv \frac{\mathrm{d}Q_{it}}{\mathrm{d}\psi_s} = q^2 D_{it} \quad (2.23)$$

Defining the capacitance gap $\Delta C \equiv C_{LF} - C_{HF}$, we can obtain the D_{it} for each bias point (voltage):

$$D_{it} = \frac{\Delta C}{q^2}\left(1 - \frac{C_{HF} + \Delta C}{C_{ox}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1}$$

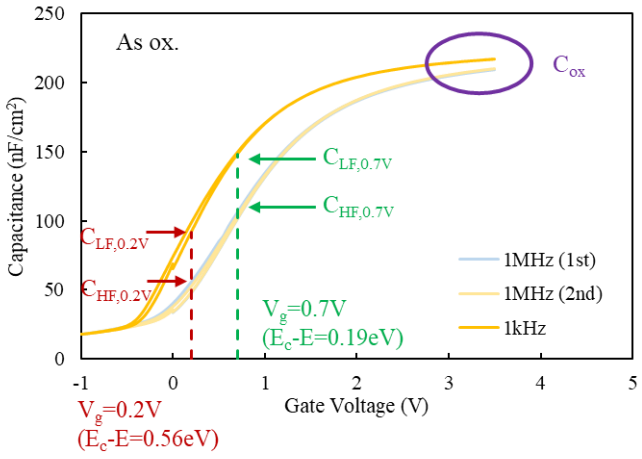

Figure 2.12 Determination of C_{ox}, C_{LF} and C_{HF}.

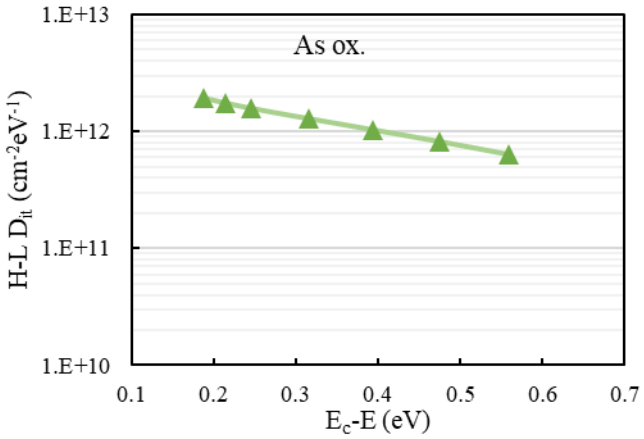

Figure 2.13 The energy distribution of D_{it}, evaluated by high-low frequency capacitance method.

In **Fig. 2.12**, the determination of C_{LF} and C_{HF} for each bias from measured C-V curve is shown. In **Fig. 2.13**, energy distribution of high-low (H-L) D_{it} is described.

Conductance Method [9]

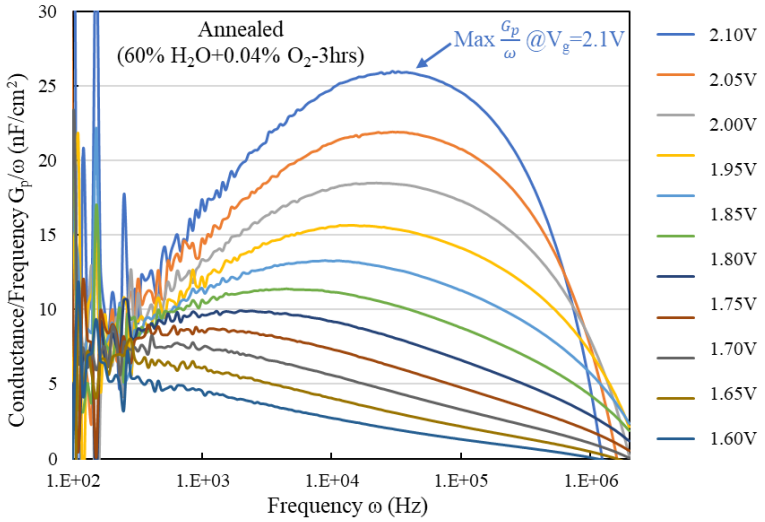

Figure 2.14 Determination of maximum G_p/ω.

At given bias, $\frac{G_p}{\omega}$ can be measured as a function of frequency. A plot of $\frac{G_p}{\omega}$ versus ω goes through a maximum when $\omega\tau_{it} = 1$. We use the relationship as

$C_{it} = 2.5\frac{G_p}{\omega}$ with the value of $\frac{G_p}{\omega}$ at maximum. Once C_{it} is known, the interface traps density can be obtained by **Eq. 2.23**.

Conductance is more sensitive than capacitance to frequency. When D_{it} is quite low (e.g., ~10^{10} $cm^{-2}eV^{-1}$ in Si MOS), conductance method would be more accurate.

In **Fig. 2.14**, the determination of maximum $\frac{G_p}{\omega}$ for each measured bias is shown. In **Fig. 2.15**, energy distribution of conductance-derived D_{it} is described.

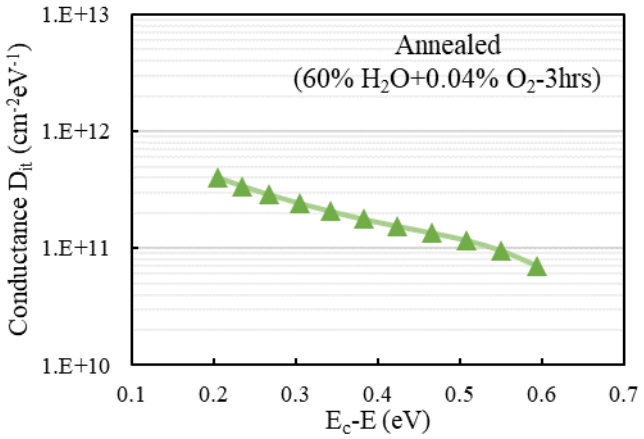

Figure 2.15 The energy distribution of D_{it}, evaluated by conductance method.

2.2.4 Evaluation of Oxide Charges

Oxide charges, different from those trapped in interface, can be categorized as the fixed oxide charge Q_f, the mobile ionic charge Q_m, and the oxide trapped charge Q_{ot}. They together cause a parallel shift in the gate-bias direction which contributes to V_{fb}. Among them, the mobile ionic charge can move back and forth through the oxide layer, depending on bias conditions and enhanced by elevated temperature, and thus give rise to voltage shifts.

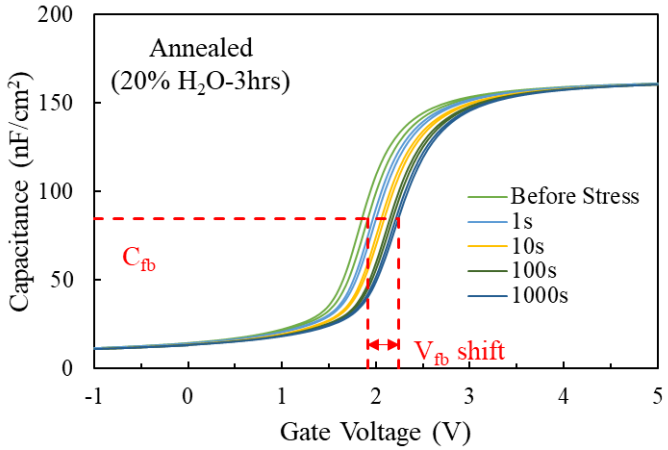

Figure 2.16 Practical C-V curves of SiC MOS capacitor under BTI test with electric field of 3MV/cm, measured under frequency of 1MHz.

By applying bias-temperature instability (BTI) test, we can evaluate change of oxide charges in MOS by the shift in flat-band voltage.

Fig. 2.16 shows a BTI result of H_2O annealed SiC MOS capacitor in our research. We apply external electric field as 3MV/cm on the sample and measure the C-V curve under 1MHz after fixed time interval (1s, 10s, 100s and 1000s). It needs to be noted that the breakdown electric field for SiO_2 is around 10MV/cm, so

3MV/cm is safe for the insulating layer. The impact of first sweep is excluded by setting a pre-measurement sweep (not shown in figure).

In Part 2.2.3, we have mentioned that under room temperature, $E_c - E_f \approx 0.19$ eV. With work function of Au being 5.38 eV [58] and electron affinity of 4H-SiC being 3.17 eV [59][60], we can estimate the work function between Au and 4H-SiC φ_{ms} to be 5.38-3.17-0.19≈2.0 eV. This should solely cause a 2.0 V positive shift in C-V curve. If we only consider contribution to non-zero V_{fb} from work function difference and oxide charges (practically, dipole layer may also contribute after nitridation [61]; yet we don't apply nitridation during our m-face MOS capacitor fabrication so we neglect it for now and will discuss it later in Chapter 5), then the oxide charges Q_{ox} could be evaluated by

$$V_{fb} = -\frac{Q_{ox}}{C_{ox}} + \varphi_{ms} \tag{2.24}$$

We could also make qualitative estimation of Q_{ox} out of **Fig. 2.16**. Before bias stressing, V_{fb} is smaller than 2.0 V, indicating existence of positive oxide charges; after applying bias for certain duration, V_{fb} shifts positively and eventually passes 2.0 eV, suggesting increase of negative oxide charges.

2.2.5 Determination of Threshold Voltage and Mobility

Threshold voltage V_{th} is one of the most important parameters in MOSFET. In traditional MOSFET, it's commonly regarded as the gate voltage that drives the

channel into strong charge inversion conditions. Under such definition, V_{th} could be given by

$$V_{th} = V_{fb} + 2\Phi_B + \frac{\sqrt{2\varepsilon_s N_A(2\Phi_B)}}{C_{ox}} \tag{2.25}$$

Here, ε_s is the dielectric constant of semiconductor and N_A is the doping concentration in channel region. Qualitatively, V_{th} is the gate bias beyond flat-band just starting to induce an inversion charge sheet and is given by the sum of voltages across the semiconductor ($2\Phi_B$) and the oxide layer (the last term of **Eq. 2.25**) [9].

However, such classical and simple definition may not suit in many modern MOSFETs, therefore "it is better to consider an operational concept of threshold, which applies in a more general sense to a wider range of devices and can be functionally described simply as the value of V_g needed for the transition from weak to strong source-drain conduction to take place in the MOSFET's channel [62]."

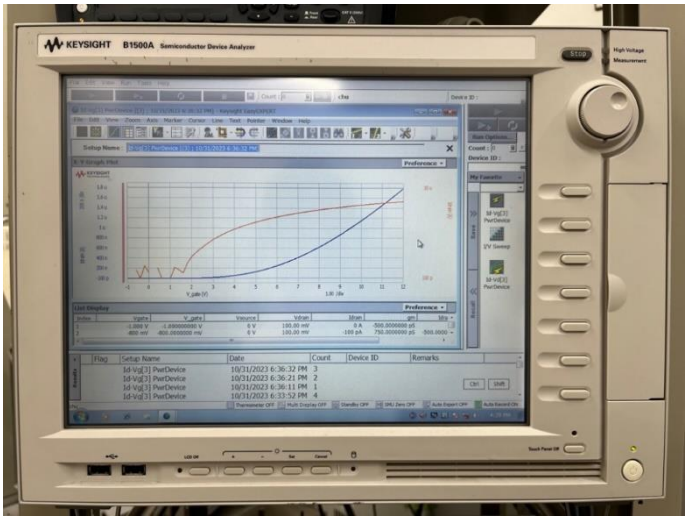

Figure 2.17 B1500A for MOSFET I_d-V_g characteristics measurement

Nowadays, there are numerous definitions and extraction methods of V_{th}, regarding MOSFET types and range of V_{th} value. In this work, we introduce two

extraction methods of V_{th}. Both are derived from drain current-gate voltage (I_d-V_g) characteristics, measured by Semiconductor Device Analyzer produced by KEYSIGHT, B1500A, as shown in **Fig. 2.17**. Drain voltage (V_d) during I_d-V_g measurement in this research was of constant value 0.1 V. Before each I_d-V_g measurement on SiC MOSFET, we had the device kept in dark environment for 2 min, then had pre-measurement sweep for twice to compensate for the charge-up effect. P-body was grounded during I_d-V_g measurement on n-MOSFET.

Extrapolation from linear region (LE) [9][63]

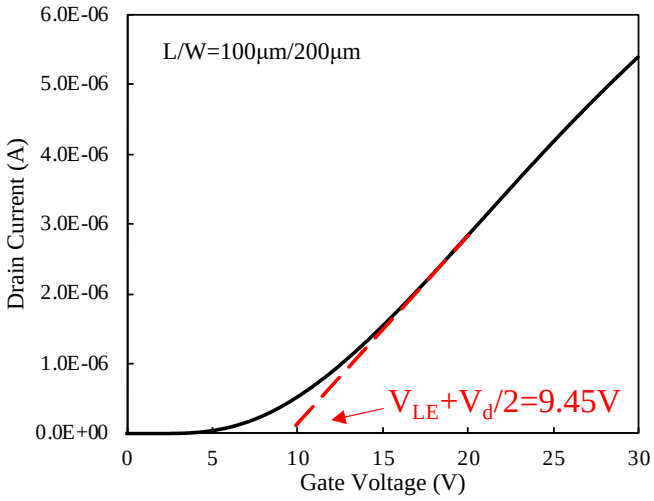

Figure 2.18 I_d-V_g plot with I_d in linear scale. V_{th} derived by LE method (V_{LE}) was decided to be of 9.40 V.

In LE method, we made extrapolation out of linear region (maximum transconductance region) of I_d-V_g curve and found its intercept with V_g axis which equaled to V_{LE}+V_d/2, as shown in **Fig. 2.18**. This method is commonly used in threshold voltage study; however, it has drawback as V_{LE} can be strongly influenced by parasitic resistance and mobility degradation effects [63].

Constant current level determination (CC) [63][64]

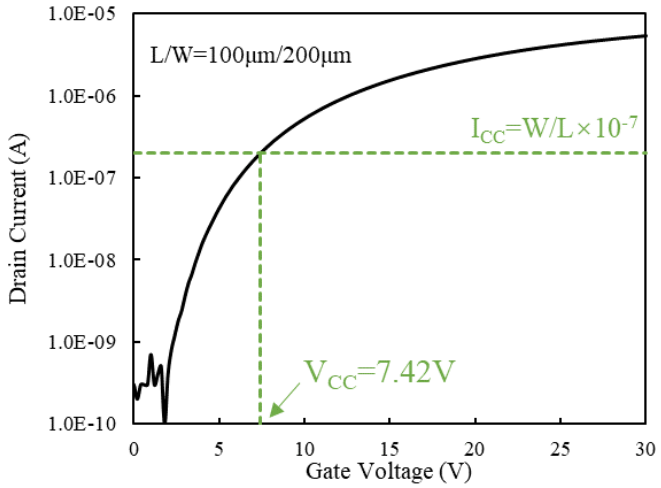

Figure 2.19 I_d-V_g plot with I_d in logarithmic scale. V_{th} derived by CC method (V_{CC}) was decided to be of 7.42 V.

In CC method, V_{CC} was determined as the corresponding V_g of an arbitrary and constant drain current level, as shown in **Fig. 2.19**. We used a popular definition for this constant current as I_{CC}=W/L×10^{-7} [64]. This method is quick however the results are highly dependent on choice of constant current I_{CC}. We chose this method because we only focused on stress-induced variation on same device, therefore this CC method was considered to provide consistent results to our device-to-device bend method.

Field-effect mobility

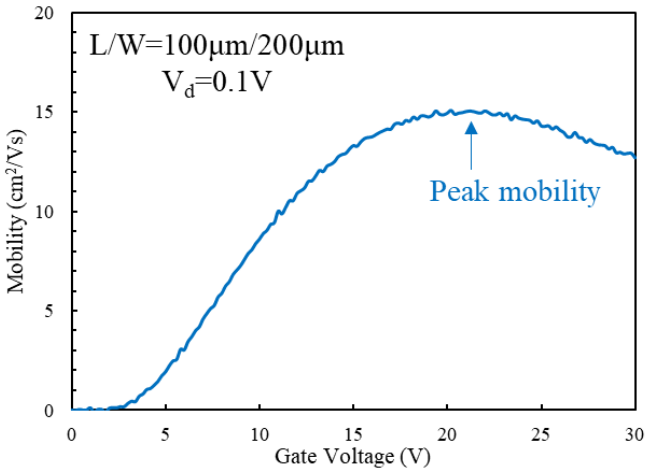

Figure 2.20 Field-effect mobility of SiC MOSFET.

There are various definitions of mobility in MOSFET, with the most common ones as Hall mobility μ_{Hall}, effective mobility μ_{eff} and field-effect mobility μ_{FE}. In this work, mobility μ refers to field-effect mobility derived from drain current-gate voltage (I_d-V_g) measurement

$$\mu = \frac{L}{WV_dC_{ox}}\frac{\partial I_d}{\partial V_g} \tag{2.26}$$

Here, L and W are channel length and width, respectively; V_d is drain voltage which is fixed at 0.1 V and C_{ox} is oxide thickness. **Fig. 2.20** shows a common measured mobility.

2.2.6 Measurement of Oxide Thickness

Electrical Measurement

By **Eq 2.3**, capacitance equivalent thickness CET of insulator in MIS system could be defined as

$$\mathrm{CET} = \frac{\varepsilon_i}{C_i}$$

and derived from C-V measurement. In this work, oxide thickness of electrical device, i.e., MOS capacitor and MOSFET, refers to CET.

Physical Measurement

X-ray diffraction (XRD) has been commonly used in investigating materials' structure. When X-ray passes through a crystal, it would scatter off the atom in the sample and then produce constructive interference at specific angle. In conventional X-ray diffractometers that based on Bragg-Brentano geometry [65], we define the incident angle between the X-ray source and the sample, the diffraction angle (2θ) between the incident beam and the reflect beam to the detector. Grazing geometry is required to increase the interaction of X-ray with the materials in the films when the films are very thin, and with such geometry shall the measurement be referred as grazing incidence XRD (GIXRD). With GIXRD, the effective X-Ray beam size on the sample surface is increased and the signal from a substrate is decreased [66]. In this work, oxide thickness of thermally oxidized SiC substrate refers to GIXRD-measured thickness.

Fig. 2.21 shows a typical GIXRD measurement result in our research. The X-Ray source is CuKα1 with λ=1.54Å. From the fitting software GlobalFit, we can obtain the fitting result as the SiO_2 (ρ=2.2 g/cm^3) thickness on SiC (ρ=3.24 g/cm^3) substrate is 8.47nm. The accuracy of fitting is limited by factors including interface roughness.

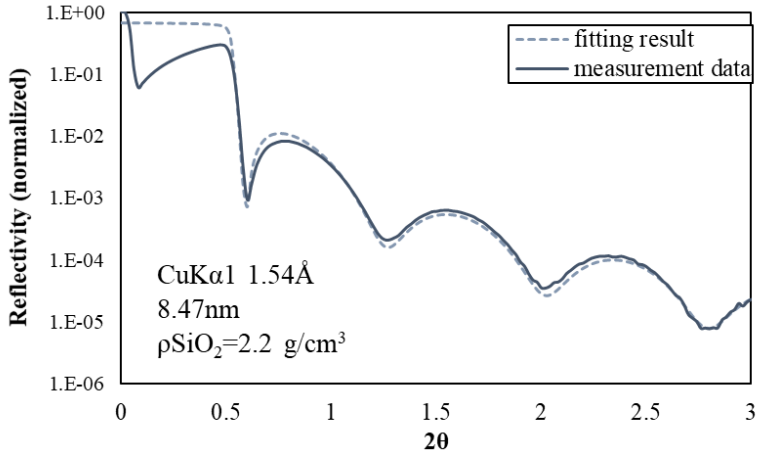

Figure 2.21 A GIXRD measurement result on SiO_2/SiC Si-face, along with fitting results.

Chapter 3

Impact of MOS Formation Process on MOS Capacitor Performance

Annealing, by its definition, is an oxidation process (usually after oxidation) resulting in oxide growth thinner than a few nanometers. In case that the oxide growth is around 10~100 nm, the process should be regarded as oxidation or re-oxidation instead.

Previously, both oxidation and annealing conditions were reported to have impacts on the C-face and Si-face SiC MOS interface quality [46][67]; our group also reported on the effect of wet re-oxidation on m-face, focusing on variables as temperature and pH_2O, as shown in **Fig. 3.1**. However, the oxide regrowth wasn't controlled within 1 nm, which leads the process to be about re-oxidation rather than annealing.

To systematically investigate on post-oxidation annealing's effect on m-face, we need to take a precise control of the oxide regrowth to distinguish the process from re-oxidation. Yet, few researches have reported on the oxidation on m-face, while the clear difference in reported oxide growth rate between Si-face and C-face

[68] suggests the possibility that m-face's oxidation rate differs from them. For further investigation in annealing's effect, we need to obtain the oxidation rate under different ambient on m-face first.

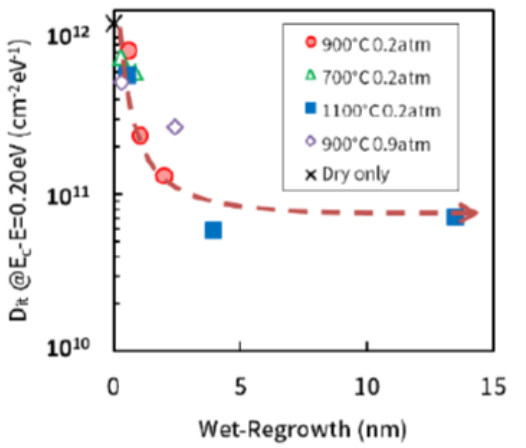

Figure 3.1 Interface traps density in wet-oxidized SiO_2/SiC m-face, with respect to wet-regrowth (Kuroyama, K, et al. JSAP, 2017 spring).

In this chapter, we report on the thermal oxidation rates under different ambient (O_2, $H_2O+O_2+N_2$, H_2O+N_2) on m-face SiC, and compare them with Si-face to discuss the impact of crystal orientation on oxidation. We also systematically investigate on annealing's impact on SiO_2/SiC m-face under different annealing ambient involved with H_2O, and discuss the phenomenon appears with evaluation of traps and charges in MOS.

3.1 Thermal Oxidation on m-face

3.1.1 Oxidation Under Dry O_2 Ambient

Oxidation Process

m-face (1-100) n-type 4H-SiC wafers from CREE research, with 10-μm-thick epitaxial layer (N_D=5×10^{15} cm^{-3}), was used in this research.

The m-face wafers are cleaned in RCA cleaning, followed by 5% HF solution to remove oxides. IPA cleaning would be done before RCA cleaning if necessary.

Dry O_2 ambient consists of 100% O_2.

Due to the commonly used temperature range for SiC, three oxidation temperature are chosen in this research: 1300 ℃, 1200 ℃ and 1100 ℃. For each temperature, more than three different oxidation durations are applied to better describe the thickness-duration relationship.

Oxidation Rate

The SiO_2 thickness on SiC is determined by GIXRD. The results for samples thermally oxidized under dry O_2 ambient are shown in **Fig. 3.2.** Insert graph shows offsets.

The thickness-duration relationship generally fits in linear approximation; however, the offsets (around 6-9 nm) in linearly approximated function are much larger than those on Si-face [4], which are only 2 nm on average.

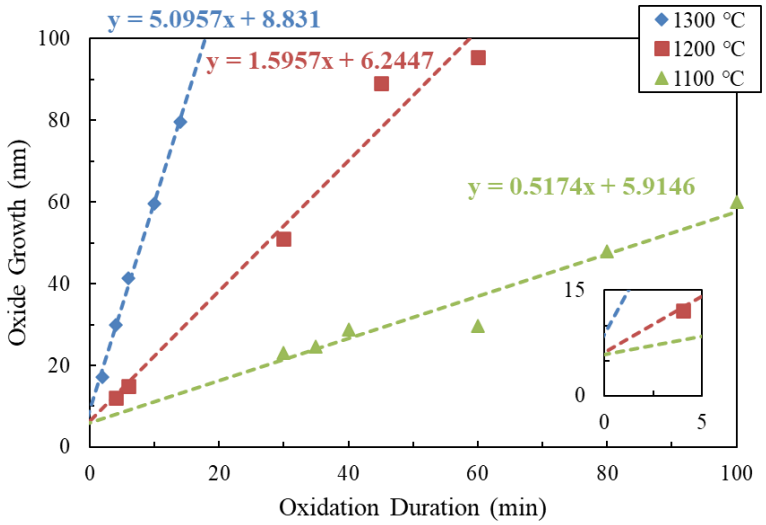

Figure 3.2 The oxide thickness grown over oxidation time under ambient of 100% O_2, at different oxidation temperatures.

According to the thermal oxidation kinetics of SiC surface based on modified Deal-Grove model [40], the oxide growth on SiC can be divided into two regimes: the interface-reaction-limited regime for thinner films and the diffusion-limited one for thicker films. This model suggests an early stage in oxide growth with linear function of the oxidation time and a later stage with parabolic function. The thickness of transition is not clear, though.

It should be noted that the Si-face research in reference [4] was designed to investigate only on the interface-reaction-limited growth, so that their oxide thickness was limited within 0-15 nm (to be precise, 2-15 nm because of existence of offsets), which is a range narrower than that of our research (12-100 nm).

There are a few possible explanations of the origin of such large offsets in our research: the thickness range has reached the transition between linear region and parabolic region, thus offset cannot be estimated accurately from linear approximation; or, though both researches utilize RTA furnace, the rise/fall rate of

temperature could still differ, which would result in additional growth during rise/fall time if our RTA process owns slower rate.

From the generally linear relationships between growth and duration, we can extract the activation energy of interface reaction by applying Arrhenius plot.

The Arrhenius equation is given by

$$k = A\exp\left(-\frac{E_a}{k_B T}\right) \tag{3.1}$$

here, k is reaction rate constant; A is pre-exponential factor; k_B is Boltzmann constant; T is oxidation temperature; E_a is activation energy of the reaction.

Eq. 3.1 can also be written as

$$\ln(k) = -\frac{E_a}{k_B T} + \ln(A) \tag{3.2}$$

With the reaction rate constant k (slope of linear approximation function) and corresponding T from **Fig. 3.2**, we are able to display ln(k), the logarithm of reaction rate, plotted against inverse temperature $1/T$ and determine activation energy E_a. Taking the length of atom bonds and atom radius in SiO_2 into consideration (e.g., 1.62 Å for Si-O and 0.65 Å for O), we take two decimal place accuracy of reaction speed in the unit of nm/min. As shown in **Table 3.1** and **Fig. 3.3**, the exponent of fitting function equals to $-\frac{E_a}{1000k_B}$. Taking Boltzmann constant k_B=1.38×10^{23} m^2·kg·s^{-2}·K^{-1} and elementary charge q=1.6×10^{-19} C into consideration, we can extract the activation energy E_a=2.12±0.004eV.

Table 3.1 Reaction rate constant *k* and inverse temperature 1000/*T*.

Temperature *T* (℃)	1300	1200	1100
1000/*T* (1000/K)	0.6357	0.6788	0.7283
Reaction rate *k* (nm/min)	5.10	1.60	0.52

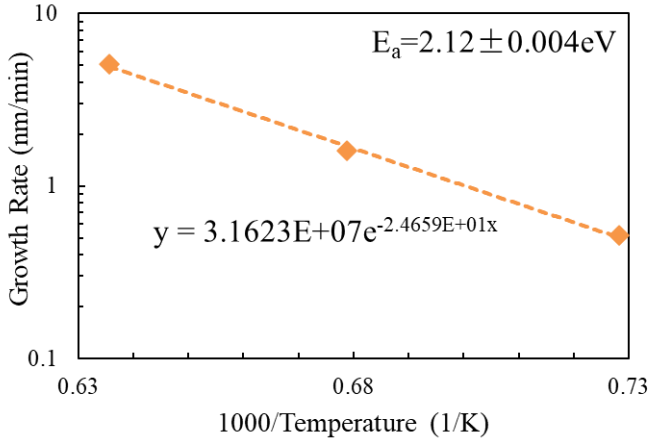

Figure 3.3 Arrhenius plot of the slopes observed in **Fig. 3.2.**

3.1.2 Oxidation Under H_2O-Containing Ambient

Oxidation Process

m-face (1-100) n-type 4H-SiC wafers from CREE research, with 10-μm-thick epitaxial layer (N_D=5×10^{15} cm^{-3}), was used in this research.

The m-face wafers are cleaned in RCA cleaning, followed by 5% HF solution to remove oxides. IPA cleaning would be done before RCA cleaning if necessary.

The H_2O-containing ambient is produced by bubbling method.

pH_2O of 0.6atm was chosen for previous research in our group when investigating on oxidation rate on m-face in H_2O+O_2 ambient. There is a reason for such choice: in the ambient of H_2O+O_2, the oxidation rate on Si-face reaches highest when the ratio of $pH_2O/(pH_2O+pO_2)$ is 0.6 [68]. Though such phenomenon has not been observed on m-face so far due to lack of sufficient oxidation rate data, our group has been using pH_2O as 0.6atm in m-face oxidation research regardless. In order to limit variables, we also use pH_2O=0.6atm in researches in this chapter.

Wet N_2 ambient consists of 60% H_2O and N_2.

Wet 2% O_2 ambient consists of 60% H_2O, 0.8% O_2 and N_2.

The oxidation process is done in quartz tubular furnace. Before furnace reaches the set heating temperature, we only flow dry gas in (pure N_2 or 2% O_2 + N_2). Because of low temperature (lower than 1100 ℃) and limited presence of oxidants in the ambient, this pre-oxidation process should only result in very thin additional growth. The flowing gas switches from dry gas to wet gas (H_2O-containing gas bubbled from heating water) instantly after the furnace reaches set heating temperature.

Due to that the quartz tubular furnace employed in this study can only reach heating temperature as high as 1150℃, we chose three different oxidation temperatures within reasonable range for ambient. For each temperature, at least three different oxidation durations are applied to better describe the thickness-duration relationship.

Oxidation Rate

① Wet N_2 ambient (60% H_2O)

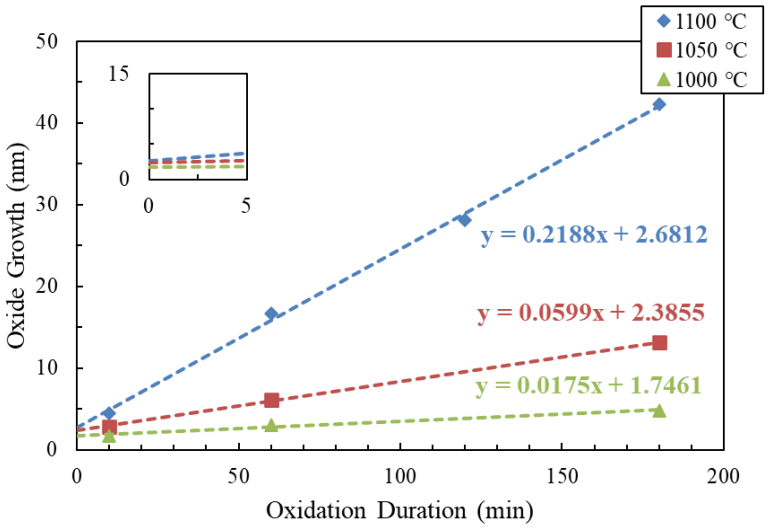

Figure 3.4 The oxide thickness grown over oxidation time under ambient of 60% H_2O and 40% N_2, at different oxidation temperatures.

The SiO_2 thickness on SiC is determined by GIXRD. The results for samples thermally oxidized under wet N_2 ambient are shown in **Fig. 3.4.** Insert graph shows offsets.

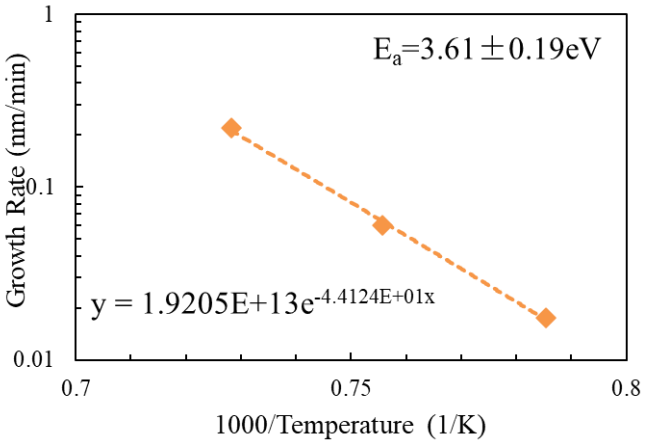

Figure 3.5 Arrhenius plot of the slopes observed in **Fig. 3.4.**

The growth over time fits in linear function very well, with much smaller offset (around 2 nm) than in dry O_2 oxidation (**Fig. 3.2**). Note that both thinner oxide

range and different heating furnace are applied in this research, so which factor is responsible for inducing large offsets is still not clear.

Arrhenius plot of the slopes is shown in **Fig. 3.5.** The activation energy E_a=3.61±0.19eV.

② Wet 2% O_2 ambient (60% H_2O+0.8% O_2)

The SiO_2 thickness on SiC is determined by GIXRD. The results for samples thermally oxidized under wet 2% O_2 ambient are shown in **Fig. 3.6.** Insert graph shows offsets.

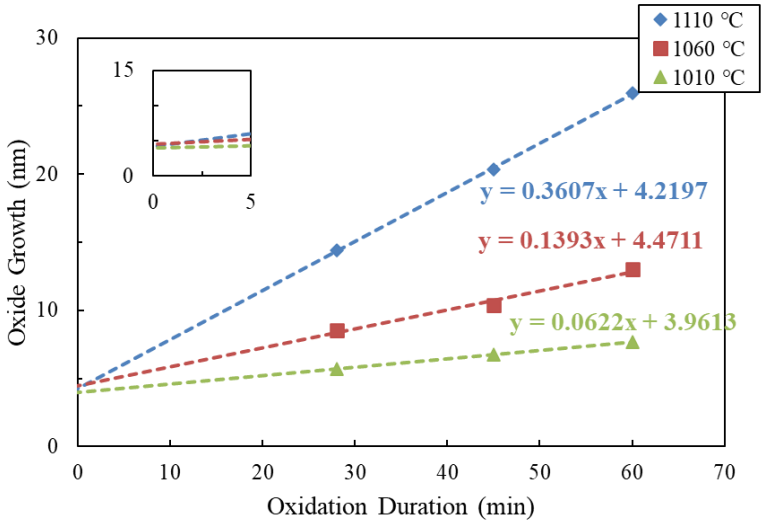

Figure 3.6 The oxide thickness grown over oxidation time under ambient of 60% H_2O, 0.8% O_2 and N_2, at different oxidation temperatures.

The growth over time also fits in linear function very well; however, the offsets (around 4 nm) are larger than that in wet N_2 ambient. This is likely due to the choice of growth range since no growth thinner than 5nm is obtained in the wet 2% O_2 ambient, which could cause error for approximation function.

Arrhenius plot of the slopes is shown in **Fig. 3.7**. The activation energy E_a=2.73±0.05eV.

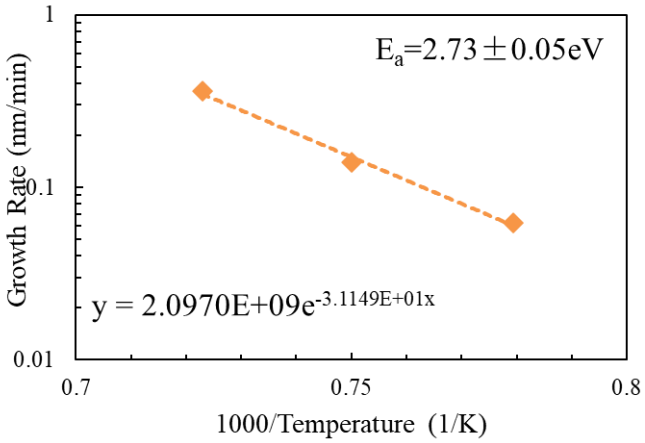

Figure 3.7 Arrhenius plot of the slopes observed in **Fig. 3.6.**

3.1.3 Similarity and Difference in Oxidation Rates between m-face and Si-face

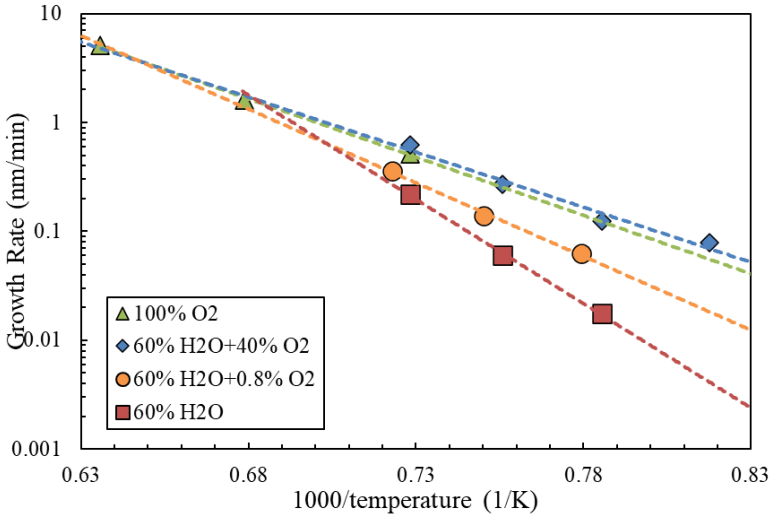

Figure 3.8 Arrhenius plot of the growth rates observed in m-face oxidation. The 60% H_2O+40% O_2 (blue diamond) data is from previous research in our group.

Arrhenius plots of the growth rates observed under different ambientes in m-face oxidation are shown in **Fig. 3.8** above. The activation energies from each plot are summarize in **Table 3.2**.

Table 3.2 Summary of activation energies from Arrhenius plots in **Fig. 3.8**.

Ambient	100% O_2	60% H_2O+40% O_2	60% H_2O+0.8% O_2	60% H_2O
E_a (eV)	2.12±0.004	2.00±0.006	2.73±0.05	3.61±0.19

Obviously, ambientes with pO_2 higher than 40% (blue diamond and green triangle) result in not only similar activation energies, but also close oxidation growth rates over temperature range. The 60% H_2O (red square) linear function

suggests a much higher oxidation rate than other ambientes in high temperature region (1000/T<0.73 1/K), which is possible yet has not been proven by experiment.

It needs to be noticed that only high temperature region (>1100 ℃) for dry ambient and low temperature region (<1100 ℃) for wet ambient, respectively, have been tested so far; meanwhile, previous researches on Si-face and C-face [69] present that there should be a transition of reaction kind at around 1100 ℃, which leads to different activation energy hence different Arrhenius plot in high and low temperature regions. This could be one of the inaccuracy factors when we compare the oxidation rates between dry and wet ambientes, before further researches are done.

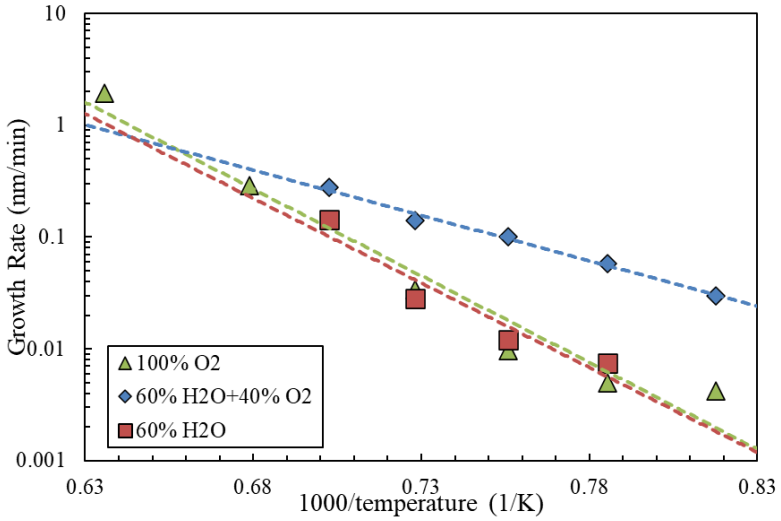

Figure 3.9 Arrhenius plot of the growth rates observed in Si-face oxidation. All data are from previous research in our group.

In order to discuss the similarity and difference in oxidation mechanism between Si-face and m-face, we introduce Si-face oxidation rates data from our group's previous researches, as shown in **Fig. 3.9**.

As mentioned above, there should be a transition of reaction at around 1100 ℃ (1000/T≈0.73) in Si-face oxidation. Such transition, presented as change in Arrhenius plot, can be clearly observed in 100% O_2 and 60% H_2O ambientes data. Despite, if we simplify the reaction model without transition and fit the logarithm of reaction rate ln(k) plotted against inverse temperature 1000/T in linear function, we can obtain the activation energy as shown in **Table 3.3**.

Table 3.3 Summary of activation energies from Arrhenius plots in **Fig. 3.9**.

Ambient	100% O_2	60% H_2O+40% O_2	60% H_2O
E_a (eV)	3.09±0.09	1.59±0.01	3.05±0.02

In **Fig. 3.9**, it's obvious that in Si-face, different from that in m-face, 100% O_2 ambient (green triangle) has not only similar activation energy but also close oxidation growth rate over temperature range, with 60% H_2O (red square) ambient.

We use pO_2 as variable to describe the relationship between oxidation rate and oxidizing ambient, at oxidation temperature of 1100 ℃, as shown in **Fig. 3.10**.

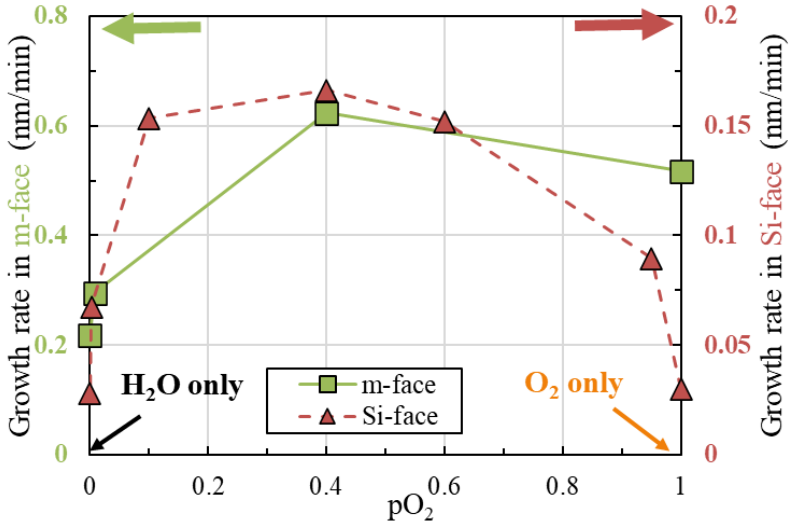

Figure 3.10 Growth rate at 1100 ℃ on m-face (green square) and on Si-face (red triangle), represented as a function of pO_2.

The right vertical axis in **Fig. 3.10** is based on our group's previous Si-face researches [68]. It's clear that the coexistence of O_2 and H_2O induces a significant enhancement of interface reaction, and reaches the fastest reaction rate when pO_2=0.4 ($pH_2O/(pH_2O+pO_2)$=0.6). When there is only one kind of oxidant in the ambient (100% O_2 or 60% H_2O), the reaction rate is closely slow regardless of the oxidant species.

The left vertical axis in **Fig. 3.10** is based on this m-face research. Apparently, at 1100 ℃, the oxidation rate on m-face is multiple times higher than that on Si-face, in all ambientes. A coexistence of O_2 and H_2O enhances the reaction on m-face as well as on Si-face. Though compared with 100% O_2 ambient, such enhancement is not large. Furthermore, the reaction rate in 100% O_2 ambient is several times higher than that of 60% H_2O ambient, indicating that m-face is more

reactive to O_2 than to H_2O. This might also explain why the enhancement in oxidation rate is not large even we increase pO_2 up to 0.4: that the ambient has reached its O_2 saturation for optimized reaction rate. If we compare the activation energies on both m-face and Si-face, the one of 60% H_2O on m-face is also the largest (3.8eV), suggesting the reaction on m-face under such O_2-absent ambient is hard to happen.

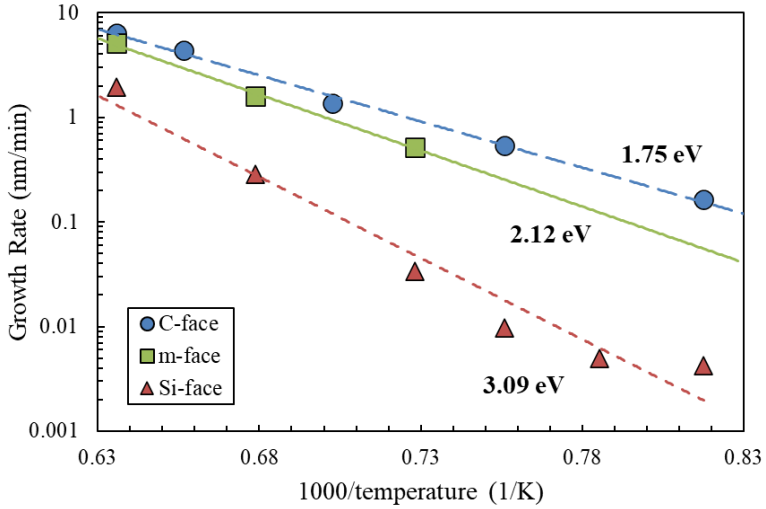

Figure 3.11 Thermal oxidation rates in 100% O_2 ambient on different crystal faces. The activation energy value estimated for reaction is indicated.

Oxide growth rates in 100% O_2 ambient on m-face have been often reported to be several times higher than that on Si-face [70]. When compared with the results on both Si-face and C-face, the dry oxidation rate on *m*-face in study is always between that of C-face and of Si-face, as shown in **Fig. 3.11**. This trend is consistent with the previously reported ones, but the specific activation energies of interface oxidation reactions estimated for those crystal faces at 1100−1300°C, i.e., 3.09 eV for Si-face, 2.12 eV for *m*-face, and 1.75 eV for C-face, seem significantly higher than the reported values, which were extracted from the ellipsometry data of much

thicker film growths assuming Deal-Grove formula [71]. The reason for the numerical discrepancy is not clear, but our results are based on the very thin films from several to tens of nanometer thickness region determined by GIXRD, which is regarded as more direct analysis of interface-reaction-limited growth with good accuracy [4].

3.2 H_2O-Annealing on m-face

3.2.1 Oxidation and Annealing Process

Process Design

m-face wafers are cleaned in RCA cleaning, followed by 5% HF solution to remove oxides. IPA cleaning would be done before RCA cleaning if necessary.

Dry oxidation process is done in lamp-heating RTA furnace. Wafers are oxidized in 2% O_2 ambient under 1300 ℃ for 15min, followed by slow cooling-down in the pace of 2 ℃/min under pure N_2 ambient for 5 hours. The oxide growth is around 18 nm.

H_2O-annealing process is done in tubular furnace. The H_2O-containing ambient is produced by bubbling method. Based on oxidation rate data from last section, the annealing temperature T is fixed at 900 ℃ to control oxide regrowth to be within 1 nm. We take various values on pO_2, pH_2O and annealing duration (t) to investigate their impact on annealing's effect.

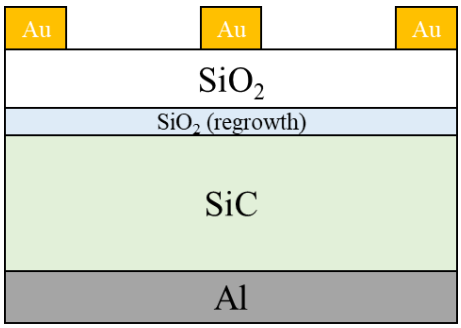

Figure 3.12 MOS capacitor structure.

Au and Al are deposited as top and bottom electrode, respectively, to fabricate the MOS capacitor, as shown in **Fig. 3.12**.

Annealing Condition

Partial pressure of H_2O is adjusted by water temperature during bubbling method.

Patial pressure of O_2 is adjusted by flowing dry gas with different composition (pure O_2, pure N_2, 0.1% O_2 + N_2 or 2% O_2 + N_2) into bubbling water. Oxidants in different ambientes are listed in **Table 3.4**.

Table 3.4 Oxidants in wet ambientes.

pH_2O (atm)	20%	20%	20%	20%	60%	60%	60%
pO_2 (atm)	80%	1.6%	0.08%	-	0.8%	0.04%	-

Ideally, when flowing pure N_2 into bubbling water, the produced ambient should not contain O_2. However, practically, decomposition reaction of water under high temperature (900 ℃) may result in non-negligible O_2 product in the ambient.

We estimated O_2 product from water decomposition as below.

$$2H_2O\,(g) = 2H_2\,(g) + O_2\,(g)$$

Start	n_B/mol	1	0	0
Equilibrium	n_B/mol	1-2α	2α	α

Here, n_B is the amount of substance of system which was set to be 1 mol at the start of reaction and α is equilibrium conversion rate at 900 ℃.

When equilibrium, total amount of substance

$$\sum n_B = 1 - 2\alpha + 2\alpha + \alpha = 1 + \alpha$$

And sum of stoichiometric coefficient

$$\sum \nu_B = -2 + 2 + 1 = 1$$

We regard total pressure in equilibrium as p^*=100 kPa=1 atm, then the equilibrium constant K^*

$$K^*(900\ ℃) = K_n \left(\frac{p}{p^* \sum n_B}\right)^{\sum \nu_B} = \frac{(2\alpha)^2 \alpha}{(1-2\alpha)^2} \frac{1}{1+\alpha} = \frac{\alpha^3}{\alpha^3 - \frac{3}{4}\alpha + \frac{1}{4}} \qquad (3.3)$$

Table 3.5 Standard enthalpy of formation, standard molar entropy and molar heat capacity at constant pressure under 25 ℃ and 100 kPa [14].

	H_2O	H_2	O_2
$\Delta_r H_m^*$ ($kJ \cdot mol^{-1}$)	-241.8	0	0
S_m^* ($kJ \cdot mol^{-1} \cdot K^{-1}$)	0.1888	0.1307	0.2051
$C_{p,m}$ ($kJ \cdot mol^{-1} \cdot K^{-1}$)	0.0336	0.0288	0.0294

Under 25 ℃ and 100 kPa, standard enthalpy of formation $\Delta_r H_m^*$, standard molar entropy S_m^* and molar heat capacity at constant pressure $C_{p,m}$ at reactant and products are listed in **Table 3.5**. $C_{p,m}$ is regarded as constant over temperature range from 25 ℃ to 900 ℃.

Molar heat capacity at constant pressure of the decomposition reaction at 25 ℃

$$\Delta_r C_{p,m} = -2C_{p,m}(H_2O) + 2C_{p,m}(H_2) + C_{p,m}(O_2) = 0.0198\ \text{kJ/(mol} \cdot \text{K)}$$

Enthalpy of the decomposition reaction at 25 ℃

$$\Delta_r H_m^*(25\ ℃) = -2\Delta_r H_m^*(H_2O) + 2\Delta_r H_m^*(H_2) + \Delta_r H_m^*(O_2) = 483.6\ \text{kJ/mol}$$

Enthalpy of the decomposition reaction at 900 ℃

$$\Delta_r H_m^*(900\ ℃) = \Delta_r H_m^*(25\ ℃) + \int_{T_1}^{T_2} \Delta_r C_{p,m}\, dT = 501.0\ \text{kJ/mol}$$

Entropy of the decomposition reaction at 25 ℃

$$\Delta_r S_m^*(25\ ℃) = -2S_m^*(H_2O) + 2S_m^*(H_2) + S_m^*(O_2) = 0.0889\ \text{kJ/(mol} \cdot \text{K)}$$

Entropy of the decomposition reaction at 900 ℃

$$\Delta_r S_m^*(900\ ℃) = \Delta_r S_m^*(25\ ℃) + \int_{T_1}^{T_2} \frac{\Delta_r C_{p,m}}{T}\, dT = 0.1160\ \text{kJ/(mol} \cdot \text{K)}$$

Gibbs energy of the decomposition reaction at 900 ℃

$$\Delta_r G_m^*(900\ ℃) = \Delta_r H_m^*(900\ ℃) - T\Delta_r S_m^*(900\ ℃) = 364.9\ \text{kJ/mol}$$

By the definition of equilibrium constant

$$K^*(900\ ℃) = \exp\left[-\frac{\Delta_r G_m^*(900\ ℃)}{RT}\right] \tag{3.4}$$

where molar gas constant $\text{R} = 8.31\ \text{kJ} \cdot \text{mol}^{-1} \cdot \text{K}^{-1}$

Equate **Eq. 3.3** and **3.4**, then we can obtain equilibrium conversion rate of the decomposition reaction at 900 ℃

$$\alpha = 2.42 \times 10^{-6}$$

When pH_2O=0.6 atm, pO_2=0.1453 Pa=1.453×10^{-6} atm.

When pH_2O=0.2 atm, pO_2=0.0484 Pa=4.84×10^{-7} atm.

3.2.2 Impact of H_2O-Annealing Process on C-V Characteristics

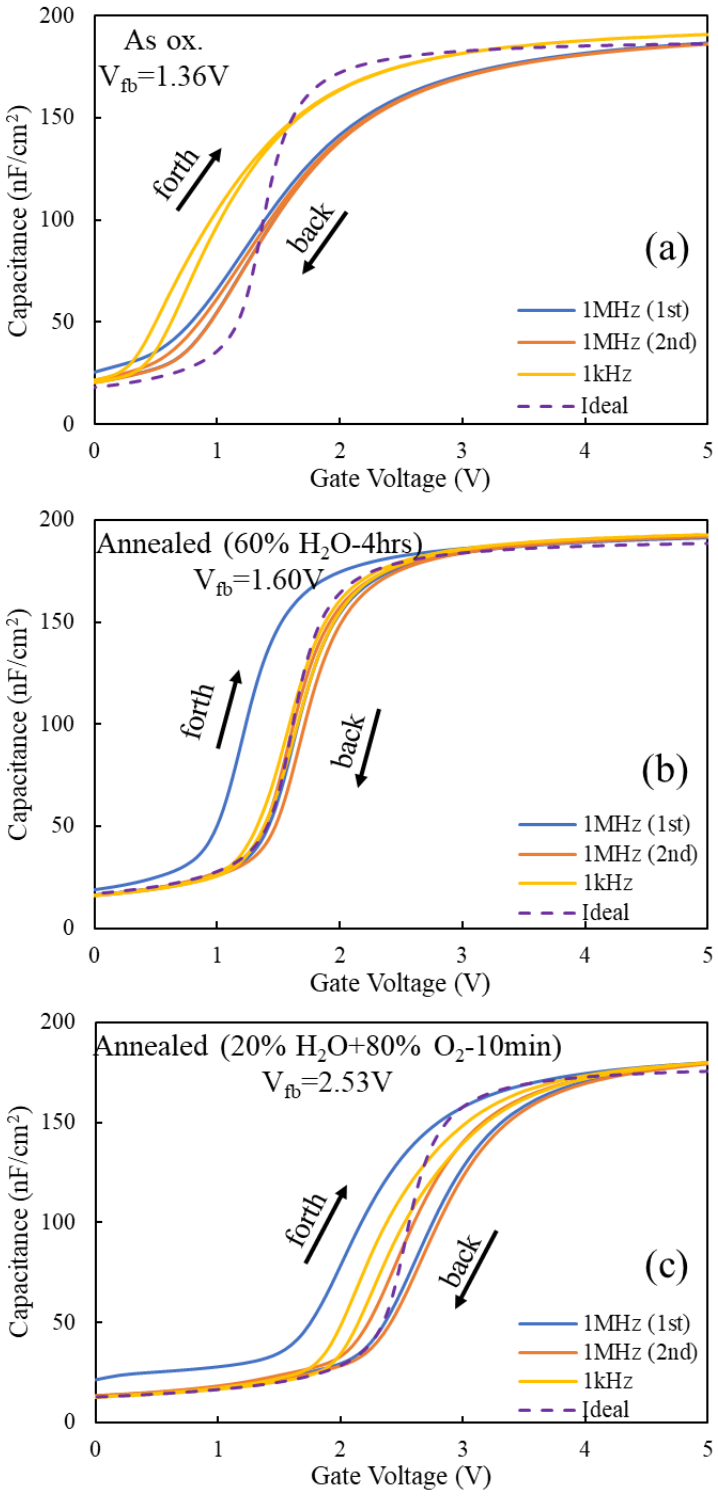

Figure 3.13 Frequency dispersions of C-V curve on samples (a) as oxidized (b) annealed under 60% H_2O ambient for 4 hours and (c) annealed under 20% H_2O with 80% O_2 for 10 min.

Fig. 3.13 shows bi-directional C-V characteristics of m-face MOS capacitors without and with H_2O-annealing process, under high (1 MHz) and low (1 kHz) frequencies, in comparison with theoretical curves. We sweep under the initial frequency (1MHz in this research) twice in the consideration of obvious first-sweep effect.

It is clear from **Fig. 3.13** (a) that with only dry-oxidation, frequency dispersion and first-sweep effect of C-V curves are quite significant. Yet after H_2O-annealing process was applied, the observed C-V curves fit more to the calculated one as shown in **Fig. 3.13** (b), indicating the reduction of D_{it} by low pO_2 H_2O-annealing. In addition, as we have calculated in Chapter 2 that the work function difference (between Au and 4H-SiC) in this system is 2.0 eV, by comparing V_{fb} with it we can qualitatively estimate change in oxide charges: the sample without H_2O-annealing has a negative shift of V_{fb}, suggesting existence of positive fixed charges, while the V_{fb} of sample with low pO_2 H_2O-annealing is much closer to ideal value, suggesting decrease of fixed charges during annealing process.

Nevertheless, when measurement was done on fresh annealed samples, a significant first-sweep effect was observed, suggesting the possibility that certain kind of slow carrier traps (other than interface traps) was induced during the annealing process as well. The density of such slow carrier traps is estimated to be ~10^{11} cm^{-2}, which will be discussed in detail later. From these results, the benefit of H_2O-annealing process is clarified for m-face MOS capacitors, although the

optimum annealing conditions are significantly different from Si-face in terms of the minimization of the interface trap density [72][69].

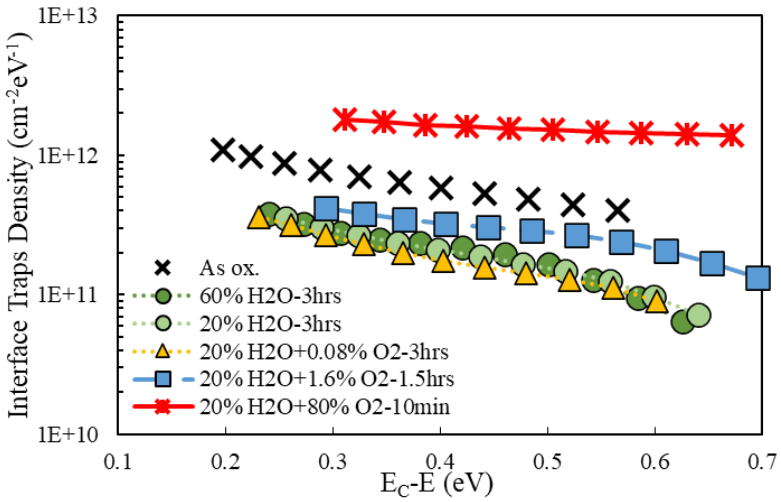

Figure 3.14 The energy profiles of D_{it}, estimated by the conductance method for the MOS capacitors fabricated with annealing ambient in various pH_2O and pO_2.

The D_{it} measured by conductance method for the capacitors fabricated with various H_2O ($+O_2$) annealing conditions is shown in **Fig. 3.14**. The energy levels are calculated based on theoretical curve with V_{fb} shift from 1MHz C-V data. It is clear that the highest pO_2 (80%) ambient results in the highest D_{it} which is even worse than the sample without annealing process, i.e., as dry oxidized, suggesting the generation of defects under high pO_2 ambient. In addition, the highest pO_2 ambient also leads to first-sweep effect in C-V curve, as presented in **Fig. 3.13** (c), and has a positive V_{fb} shift from 2.0 V. In contrast, when pO_2 is suppressed to sufficiently low (1.6% or lower), annealing works in efficient D_{it} reduction. D_{it} of sample with different pH_2O (60% and 20%) in the annealing ambient is also

compared, though impact of pH_2O was not as significant as of pO_2. Above results show the importance of annealing ambient in annealing impact.

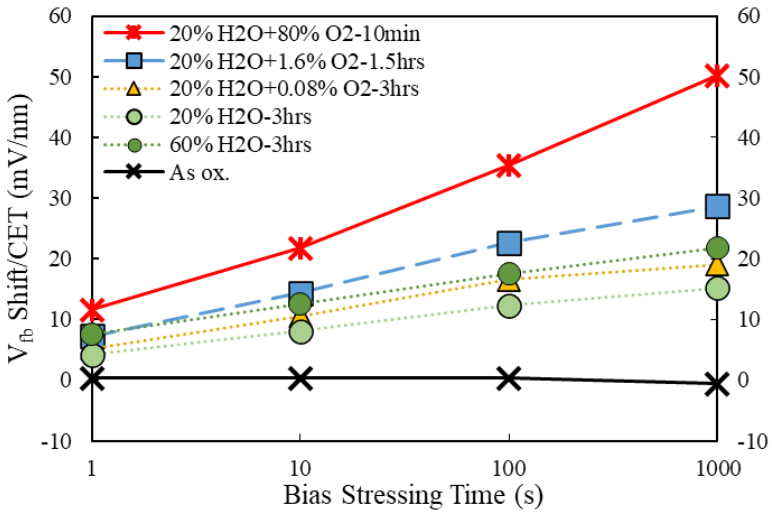

Figure 3.15 Flat-band voltage shift divided by CET over time, electrically stressed for the MOS capacitors fabricated with annealing ambient in various pH_2O and pO_2.

On the same group of samples discussed by **Fig. 3.14**, V_{fb} shift/CET over bias stressing time under BTI test with external electric field of 3 MV/cm is shown in **Fig. 3.15**. The high O_2 concentration (20% H_2O+80% O_2) results in a dramatic instability in V_{fb}. With its disadvantage in reduction of D_{it}, we suggest that high pO_2 in POA process is detrimental and should be avoided. Such sensitivity of m-face to pO_2 agrees with our conclusion from last section, that m-face is more reactive to O_2 than to H_2O during oxidation. What's more, we noticed that when first-sweep effect appears in C-V characteristics, the corresponding BTI result is also worse (more instable), indicating that first-sweep effect should be induced by similar origin as BTI (slower traps in oxide).

Contrast to its performance in D_{it}, the sample without POA process shows a very stable V_{fb} during bias stressing test. However, such stability of V_{fb} disappears after POA process is applied. Even preferable conditions for reduction of D_{it}, i.e., low pO_2 ambient, would induce a significant shift in V_{fb} under long time bias stressing. In addition, we noticed that sample with 1.6% O_2 in annealing ambient has slightly larger V_{fb} shift/CET than those samples annealed with even lower pO_2, while its impact in D_{it} decrease is also reported to be slightly less in comparison (**Fig. 3.14**). From here, we are going to discuss the impact of annealing ambient (pO_2 and pH_2O) and annealing temperature in detail, to decide the major factor in improving annealed MOS interface quality.

Impact of pO_2

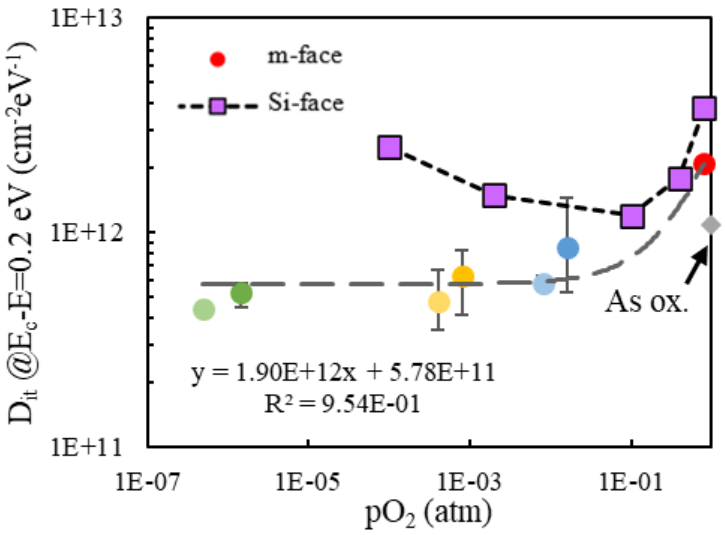

Figure 3.16 D_{it} in relationship with pO_2. Closed purple square refers to Si-face and open symbol in various colors refers to m-face.

D_{it} (by conductance method) as function of pO_2 is plotted in **Fig. 3.16**, from H_2O-annealed m-face and Si-face samples. m-face data is the average value of 2~4

samples with different annealing durations (pO_2=80% and as oxidized have only one duration), with linear approximation and error bar indicating D_{it} variation. Si-face data is from our group's previous research and is simply connected by broken lines.

It's obvious that lower D_{it} could be obtained on m-face with annealing process, compared to Si-face. In Si-face, the suppression of D_{it} is better with lower pO_2 in the ambient, until pO_2=0.1 atm; then the suppression becomes less effective with decreasing pO_2. This result shows that the optimized H_2O-annealing ambient in Si-face requires co-existence of both H_2O and O_2, which reminds us with the conclusion in Part 3.1.3 that highest oxide growth rate on Si-face is obtained with presence of both oxidants. In m-face, however, D_{it} suppression becomes more and more effective with decreasing pO_2 in annealing ambient. Linear approximation is applied to prove the monotonicity between D_{it} and pO_2.

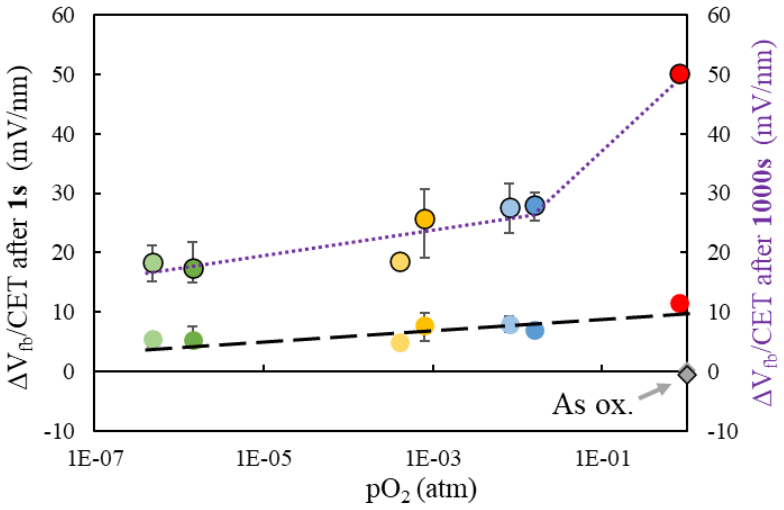

Figure 3.17 Flat-band voltage shift divided by CET after stressing time of 1s (open circle) and of 1000s (closed circle), in relationship with pO_2.

V_{fb}/CET shift after BTI duration of 1 s and of 1000 s as function of pO_2 is plotted in **Fig. 3.17**, from H_2O-annealed m-face and Si-face samples. Each datapoint is the average value of 2~4 samples with different annealing durations (pO_2=80% and as oxidized has only one duration), with error bar indicating V_{fb}/CET shift variation.

For as dry oxidized sample, bias stressing hardly causes any shift in V_{fb}, suggesting almost no existence of oxide trapped charges. Noting that D_{it} from this condition is as high as ~10^{12} $eV^{-1}cm^{-2}$ at E_c-E=0.2 eV and first-sweep effect observed in **Fig. 3.13 (a)** is insignificant, we conclude that during dry oxidation, traps are mainly generated at interface rather than in oxide and mobile oxide charges

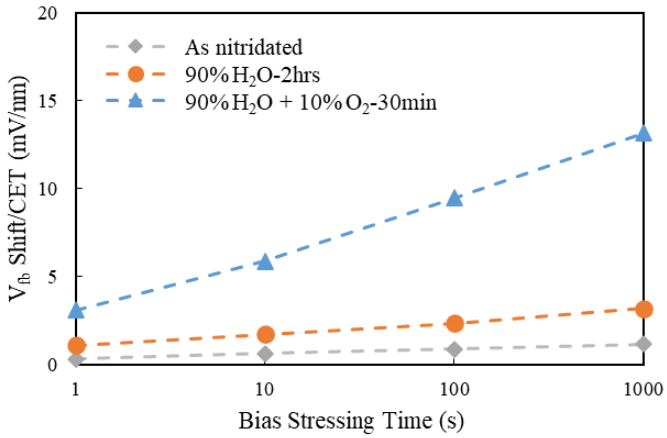

Figure 3.18 Flat-band voltage shift divided by CET on Si-face MOS capacitor [10].

are few.

After application of H_2O-annealing, shift of V_{fb} is induced under BTI test. In general, with more pO_2 in annealing ambient, V_{fb}/CET shift increases, suggesting the positive correlation between pO_2 and generation of oxide traps. The distribution of oxide traps is also affected by pO_2: according to **Fig. 3.15**, V_{fb}/CET shift

increases consistently when stressing time extends from 1 s to 1000 s, which says that the distribution of oxide traps in distance from interface is consistent, therefore amount of oxide traps multiples consistently at each distance with higher pO_2.

All the large V_{fb} shift observed from m-face samples above, is rarely to show up on Si-face MOS capacitor [10]. As **Fig. 3.18** shows, the V_{fb} shift induced from low pO_2 post-nitridation-H_2O-annealing is much smaller than that on m-face. With the introduction of oxygen, more V_{fb} shift is induced, but the value (especially after 1s) is still no larger than that of m-face.

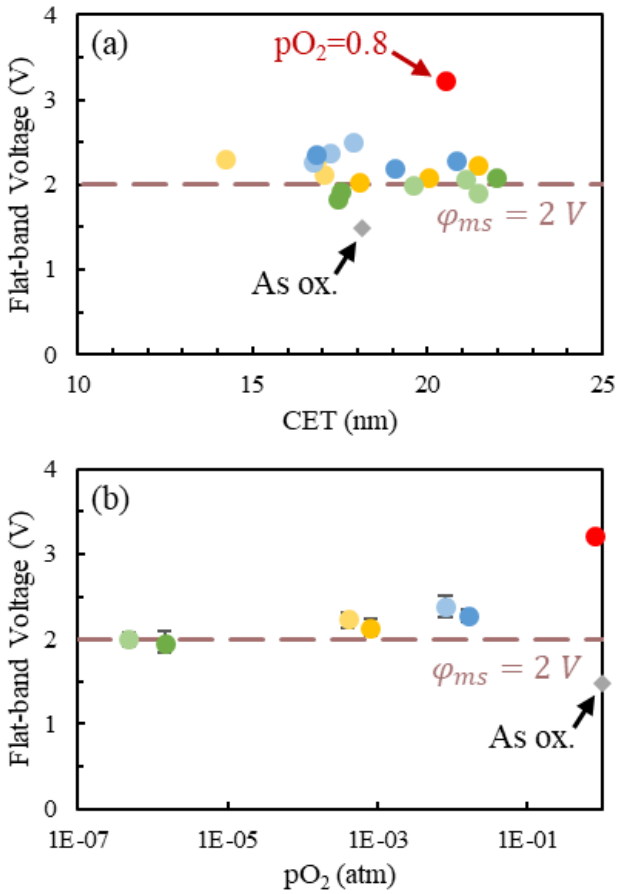

Figure 3.19 V_{fb} in relationship with CET (a) and with pO_2 (b). Different colors are for different pO_2. Work function of 2V in the system is marked with horizontal broken line.

Absolute value of V_{fb} is summarized in **Fig. 3.19**. We have reported in above part, that V_{fb} in as oxidized sample is lower than work function difference between Au and 4H-SiC $\varphi_{ms} = 2.0\,\mathrm{eV}$, suggesting existence of positive fixed oxide charges, and H_2O-annealing induces generation of negative fixed oxide charges which compensates the positive ones. In **Fig. 3.19 (a)**, we observed that V_{fb} on low pO_2 H_2O-annealed samples are not of clear CET dependence, but its value is close to $\varphi_{ms} = 2.0\,\mathrm{eV}$. (There might be a CET dependence, but CET variation is relatively too small to make a clear V_{fb}-CET plot; apparently this also proves that fixed oxide charges are relatively too few.) This result suggests that change of fixed oxide charges might only be related with annealing ambient.

In **Fig. 3.19 (b)**, the average value of 2~4 samples with different annealing durations (pO_2=80% and as oxidized has only one duration) is plotted to pO_2, with error bar indicating V_{fb} variation. It's clear that the V_{fb} is of pO_2 dependence, that higher pO_2 in annealing ambient induces negative fixed oxide charges hence positive shift in V_{fb}.

Impact of pH_2O

D_{it} (by conductance method) as function of pO_2 is plotted in **Fig. 3.20**, taking average value of 2~4 samples with different annealing durations and pO_2 (except for pO_2=80% and as oxidized which have only one datapoint each), with error bar indicating D_{it} variation.

We can suggest a vague relationship between D_{it} and pO_2 that D_{it} decreases with higher pH_2O in annealing ambient. However, this relationship only suits in when pO_2 is relatively low (<1.6%). Under high pO_2 ambient (red circle, pO_2=80% and pH_2O=20%), the D_{it} is even beyond error bar. This result suggests that despite pH_2O being effective in D_{it} depression, its impact is relatively smaller than that of pO_2.

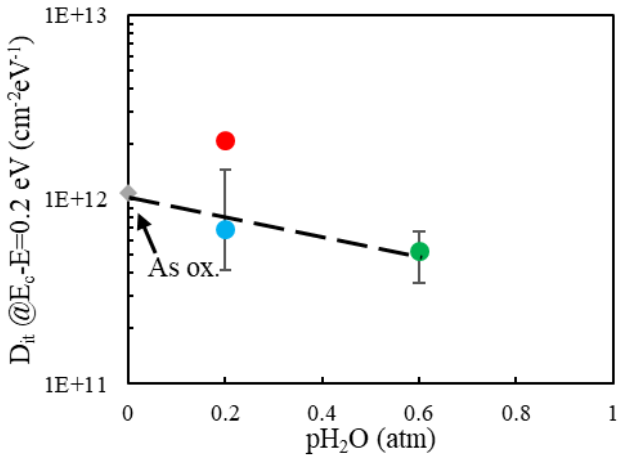

Figure 3.20 D_{it} in relationship with pO_2. Circle stands for H_2O-annealed sample and diamond stands for as oxidized sample.

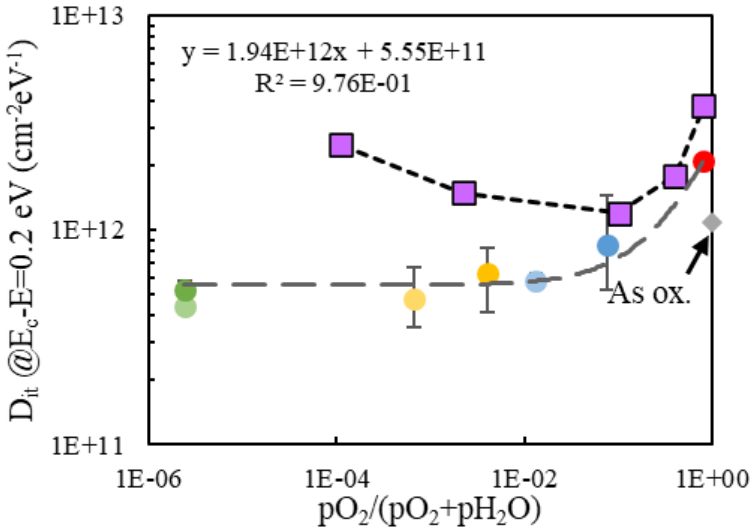

Figure 3.21 D_{it} in relationship with $pO_2/(pH_2O+pO_2)$. Closed purple square refers to Si-face and open symbol in various colors refers to m-face.

It would be a challenge to solely investigate in the impact of pH_2O when its impact is smaller. We replace the independent variable in **Fig. 3.16** from pO_2 to $pO_2/(pH_2O+pO_2)$, to describe the impact of coexistence of O_2 and H_2O in annealing ambient in **Fig. 3.21**.

We observed very similar relationships between **Fig. 3.16** and **Fig. 3.21**. After taking pH_2O into consideration, the R_2 of linear approximation of D_{it}-oxidants increases for a bit. Indeed, such relationship is not expected to be of linearity, yet the improvement in linear approximation suggests a better relativity between D_{it} and $pO_2/(pH_2O+pO_2)$ than between D_{it} and pO_2.

We also plot the dependence of $pO_2/(pH_2O+pO_2)$ on V_{fb}/CET shift under BTI and on V_{fb}, by replacing the independent variable with $pO_2/(pH_2O+pO_2)$ in **Fig. 3.17** and **Fig. 3.19 (b)** (those new figures would be presented together in next part) and observe almost no difference between the dependence of pO_2. These results show that pH_2O has minor impact on annealing effect.

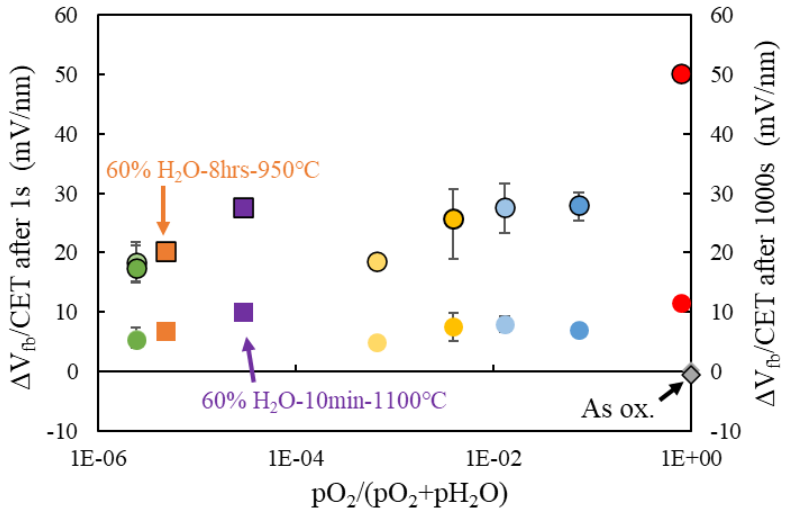

Figure 3.22 Flat-band voltage shift divided by CET after stressing time of 1s (open symbols) and of 1000s (closed symbols), in relationship with $pO_2/(pH_2O+pO_2)$.

Impact of Annealing Temperature and Duration

To investigate in the impact of annealing temperature and duration on annealing effect, we design two process conditions as 1) pH_2O=0.6 atm, t=8 hrs, T=950 ℃ and 2) pH_2O=0.6 atm, t=10 min, T=1100 ℃. Oxygen generated by water composition under 950 ℃ and 1100 ℃ would contribute to pO_2 of 2.9×10^{-6} atm and of 1.8×10^{-5} atm, respectively. V_{fb}/CET shift after BTI duration of 1 s and of 1000 s as function of $pO_2/(pH_2O+pO_2)$ is plotted in **Fig. 3.22**. Compared to process with close magnitude of $pO_2/(pH_2O+pO_2)$, higher T results in larger V_{fb}/CET shift and annealing duration has insignificant impact.

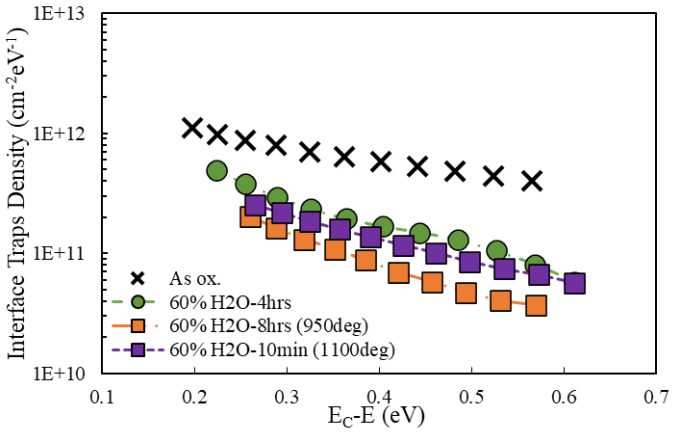

Figure 3.23 The energy profiles of D_{it}, estimated by the conductance method.

The D_{it} measured by conductance method is shown in **Fig 3.23**. We observe that with low pO_2 in the ambient, higher annealing temperature T leads to more suppression on D_{it}. The impact of annealing time t is minor.

Absolute value of V_{fb} is summarized in **Fig. 3.24**. In above part we came up with a suggestion that regardless not observing a clear relationship between V_{fb} and

CET on the given oxide thickness variation (8 nm), the CET dependence may still exist; now we can conclude that such suggestion does not work. With the thickness variation at the moment (16 nm), it's clear that V_{fb} has almost no CET dependence. This is certainly because of few fixed oxide charges after annealing.

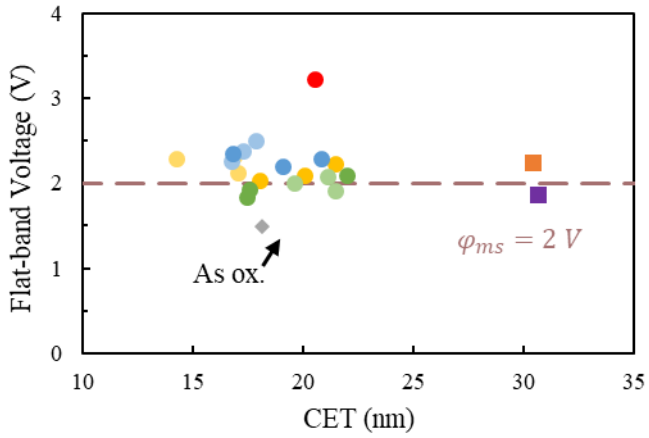

Figure 3.24 V_{fb} in relationship with CET. Work function of 2V in the system is marked with horizontal broken line.

3.2.3 Comparison of H_2O-Annealing Impact on m-face, Si-face and Si

Table 3.6 Oxidation and annealing conditions on SiC m-face, Si-face and Si wafers.

Name	Substrate	Dry oxidation			Wet-POA			
		T	pO_2	Duration	T	pH_2O	pO_2	Duration
m-face w/o POA	SiC m-face	1300℃	0.02atm	15min	(slow cooling for 5 hours after dry oxidation)			
m-face O_2-POA					950℃	0.6atm	0.4atm	15min
m-face N_2-POA					950℃	0.6atm		240min
Si-face w/o POA	SiC Si-face			40min				
Si-face O_2-POA					950℃	0.6atm	0.4atm	35min
Si w/o POA	Si	1100℃						
Si O_2-POA					500℃	0.6atm	0.4atm	10min

To compare impact of H_2O-containing post-oxidation annealing (wet-POA) on SiC and Si wafers, we made a series of capacitors following process conditions summarized in **Table 3.6**.

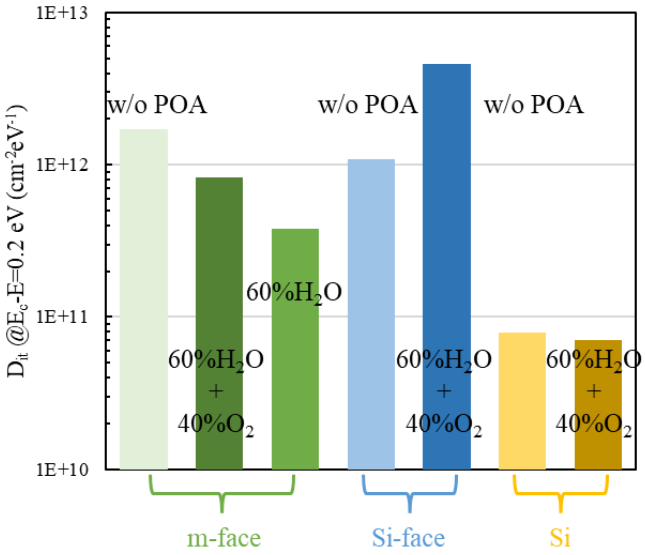

Figure 3.25 D_{it} at E_c-E=0.2eV (measurement in 2018).

D_{it} measured by conductance method is presented in **Fig. 3.25**. It is clear that by only H_2O-annealing, it is still challenging to obtain SiO_2/SiC interface with D_{it} as low as on SiO_2/Si; yet, compared to Si-face, lower D_{it} can be obtained on m-face.

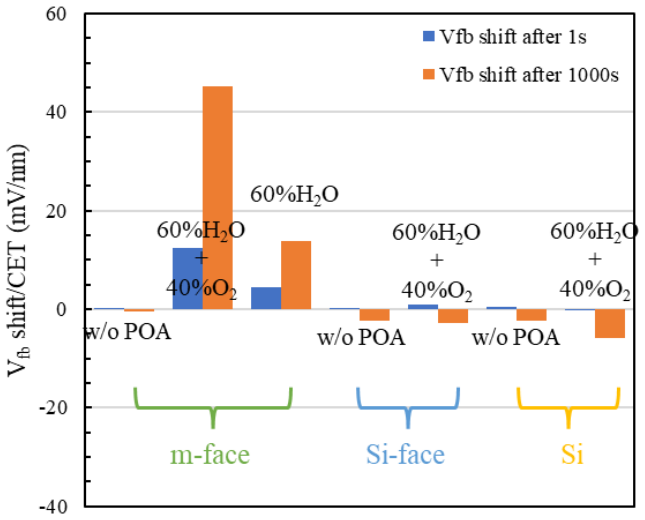

Figure 3.26 V_{fb}/CET shift under BTI test with electric field of 3MV/cm (measurement in 2018).

V_{fb}/CET shift under BTI test is presented in **Fig. 3.26**. Compared to Si-face SiC and Si, it is almost unique for m-face to have oxide traps generated during wet-POA, especially with higher pO_2 in the ambient.

Flat-band voltage is summarized in **Fig. 3.27**. We compared the value measured in the year of 2018 and 2023 to evaluate if the oxide quality can be considered as stable. Here, the work function difference in Au-SiC and in Au-Si system should be around 2 eV and 1 eV, respectively. We noticed an increase appeared commonly in V_{fb} for all capacitors after five years; considering the thickness of oxide layer is relatively thin (around 20 nm), this might be a result of natural oxidation in the air. Nevertheless, m-face capacitor with wet-POA showed the largest V_{fb} increase, suggesting the annealed oxide is more sensitive to oxygen.

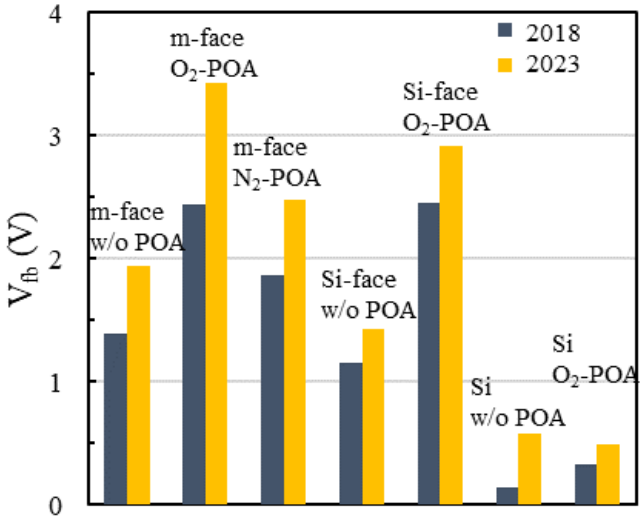

Figure 3.27 Flat-band voltage measured before and after interval of five years.

3.3 Summary

In this chapter, we first investigated on the reaction rate and activation energy of thermal oxidation reaction on m-face SiC and made the comparison with the case of Si-face; then, based on the oxidation rate data, we investigated on the impact of H_2O-annealing on m-face MOS characteristics, mainly regarding to interface traps (evaluated by D_{it}) and oxide charges (evaluated by V_{fb} value and V_{fb} instability).

In general, the reaction rate under same/similar ambient on m-face was significantly higher than that on Si-face. Coexistence of O_2 and H_2O enhanced reaction rate on both m-face and Si-face. On m-face, the reaction rate and activation energy were close when ambient consists of high oxygen components; on Si-face, the reaction rate and activation energy were close to each other when ambient consists of solo oxidant. It was suggested that m-face was more reactive to O_2 rather than H_2O in oxidation.

Based on the oxidation rate data, we were able to well limit oxide regrowth on SiC MOS from annealing process. The regrowth from POA process was limited within ~1nm utilizing oxidation rate data from above section. For H_2O-annealing, the effects of pO_2, pH_2O, annealing temperature and duration were studied. It was found that pO_2 was the most influential factor on m-face MOS characteristics: high pO_2 was detrimental for interface and oxide quality, while annealing with suppressed pO_2 helped to reduce D_{it}. It was also noticed that though it's inevitable to induce V_{fb} instability and first-sweep effect by H_2O-annealing, suppression of

pO_2 in annealing ambient can help controlling the instability at certain degree. In addition, as the regrowth is within 1 nm, the absolute value of V_{fb} is also decided by pO_2. Above results showed that on m-face, interface traps, oxide traps and oxide fixed charges were all affected by pO_2 in H_2O-annealing ambient. The impacts of pH_2O, annealing temperature and annealing duration were relatively insignificant.

In comparison with Si-face and Si, it was found that only on m-face that significant amount of oxide traps would generate during H_2O-annealing. The annealed oxide on m-face was also more reactive to oxygen in atmosphere and resulted in increase in number of fixed oxide charges.

Chapter 4

Anomalous Impact of Mechanical Uniaxial Stress on Threshold Voltage of 4H-SiC (0001) MOSFET

By definition, stress and strain are distinct from each other. Stress, usually in the unit of MPa, describes internal forces present during deformation while strain, in the unit of 1, evaluates the relative deformation by percentage change of the material's lattice constant.

Despite strain engineering has been well established and widely applied in Si-based devices, however, there is some uncertainty to decide whether strain is solely responsible for performance enhancement because many process flow parameters are changed when fabricating strained SiC MOSFETs, e.g., reduced external resistance [7]. To describe a direct relationship between strain and performance variation in MOSFETs, four-points wafer bending setup is utilized to apply external mechanical stress on and introduce strain into Si MOSFETs [73][74].

It was reported recently that in strained bulk SiC, significant change in band-gap and electron mass would be induced [8], suggesting the potential of transferring strain technologies to SiC device for performance enhancement such as mobility

improvement. The wafer bending setup we introduced above was utilized to study on performance enhancement in stressed SiC MOSFETs [11]. As presented in **Fig. 4.1**, the variation of mobility with the mechanical stress was successfully described. In addition to mobility enhancement, however, the study on the variation of threshold voltage with stress is also necessary for further discussion of strain's application in SiC MOSFETs.

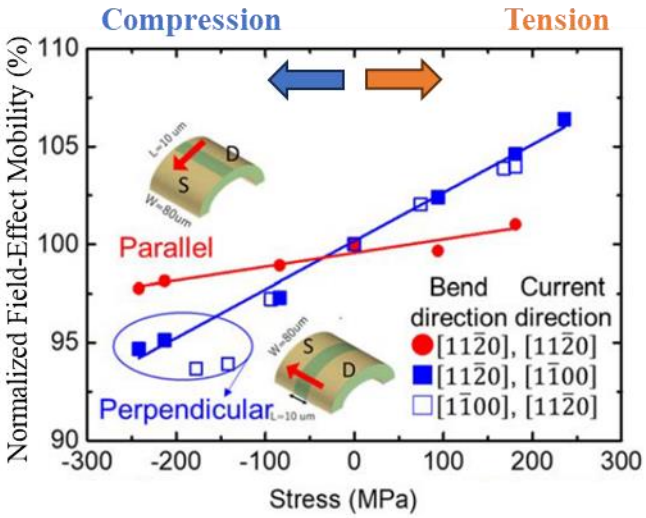

Figure 4.1 The variation of field-effect mobility with the stress [11].

In this chapter, we will utilize four-points wafer bending setup on SiC MOSFETs to study strain's impact on electrical characteristics, particularly mobility and threshold voltage. Process-induced strain will be estimated by Raman spectroscopy. Mechanical stress will be evaluated by comparison with Si MOSFETs in mobility variation.

4.1 SiC MOSFET Conditions

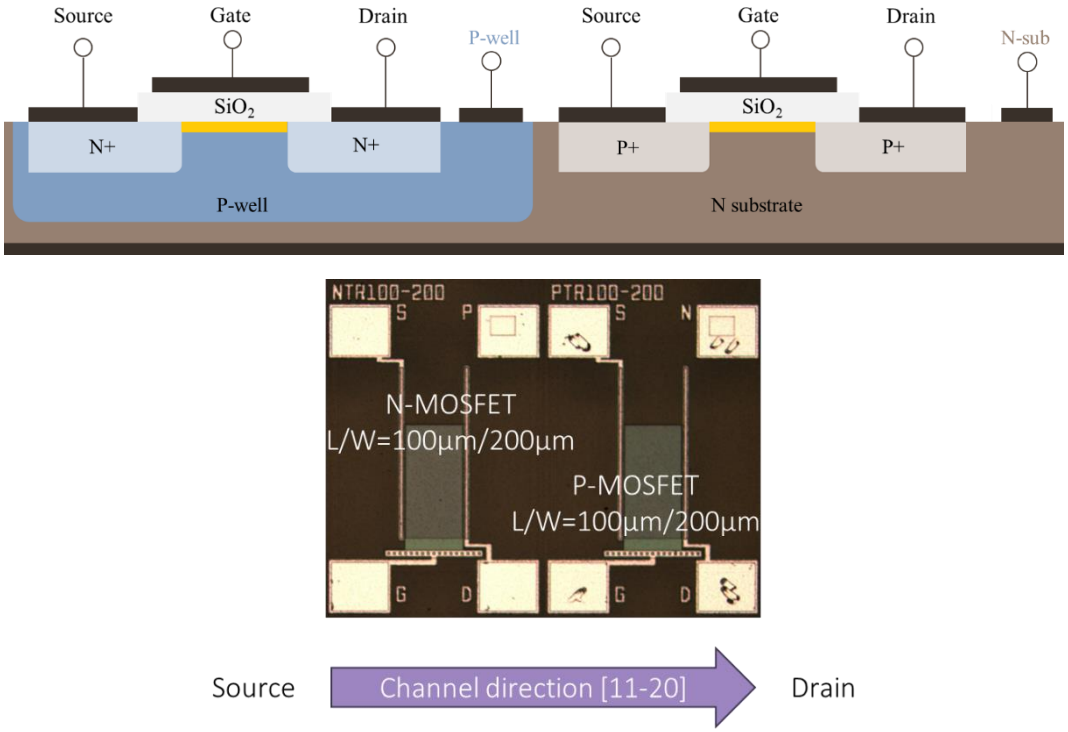

Figure 4.2 (Up) Structure of CMOS, (down) a pair of n-MOSFET and p-MOSFET with channels of L/W=100 µm/200 µm.

The N-channel MOSFET used in this chapter was fabricated on p-well with doping concentration $N_A=3.6\times10^{17}cm^{-3}$ on 4° off n-type 4H-SiC (0001) substrate; next to it, p-MOSFET was fabricated directly on substrate (epitaxial layer concentration $N_D=3.0\times10^{15}cm^{-3}$) to form complementary MOS (CMOS), as presented in **Fig. 4.2**. The channel direction was along [11-20], with various channel length and width. A 38nm-thick oxide was formed by chemical vapor deposition (CVD) followed by thermal oxidation. The MOS interface was passivated by conventional post-oxidation nitridation process.

I_d-V_g and I_d-V_d measurement was done on n-MOSFET.

C-V_g measurement was done on p-MOSFET; by contacting gate electrode and substrate electrode, marked as "G" and N" in **Fig. 4.2**, it worked as a n-MOS capacitor.

4.1 Mechanical Stress and Process-Induced Strain in SiC MOSFET

4.1.1 Deflection and Stress in Simply Supported Beam

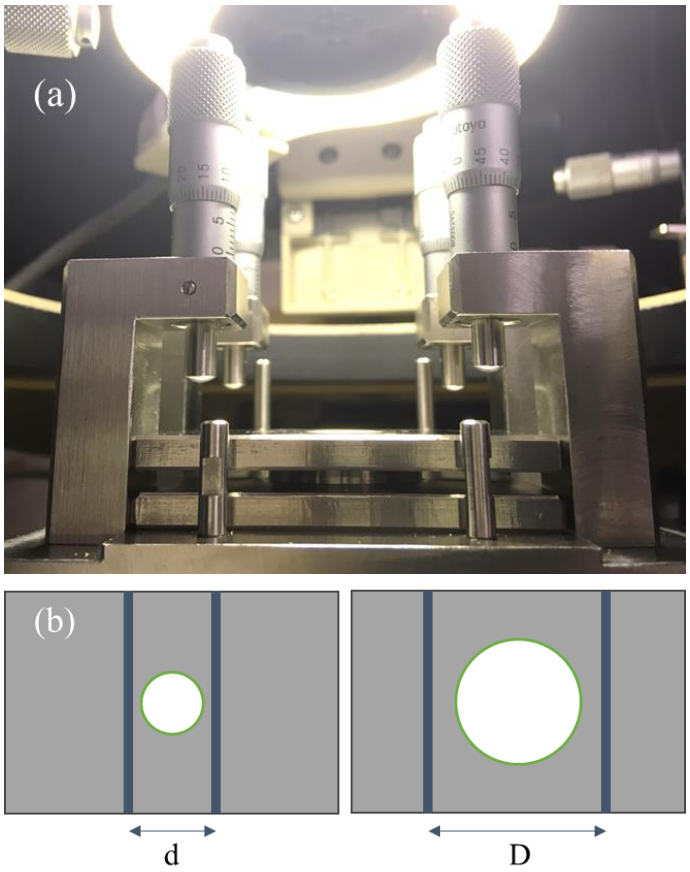

Figure 4.3 (a) Four-points wafer bending tool and (b) plates with parallel ridges.

The bending tool utilized in this research and two plates with pair of parallel ridges are shown in **Fig. 4.3 (a)** and **(b)**. With distance between ridges as d and D, the plates are placed above and under the wafer to apply uniaxial stress by rotating four Vernier scales. When d<D, compressive stress is applied on wafer surface; when d>D, tensile stress is applied. The hollow circle on plates is for probes to making electrical contact on devices on wafer surface.

In our research, distance between ridges d (or D) is no smaller than 10 mm, wafer thickness h is thicker than 350 μm and maximum displacement in the center of wafer δ_{center} is smaller than 150 μm, therefore we have d/h>10 and δ_{center}/d<0.1, which suggest that the wafer under bending could be regarded as simply supported beam, as described in **Fig. 4.4**.

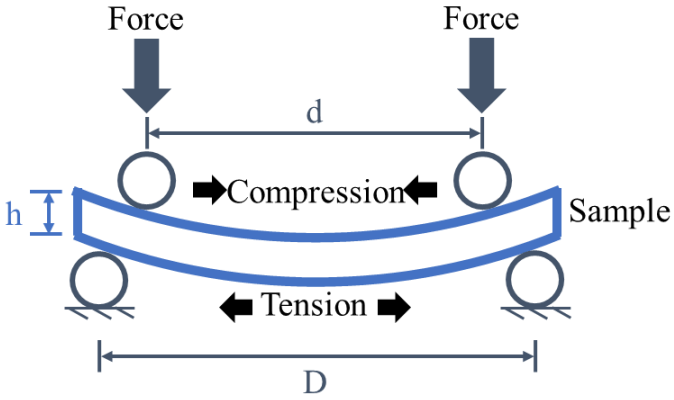

Figure 4.4 Schematic of simply supported beam model in wafer bending tool.

We can use either of the bottom supports as zero-point to build a deflection curve. The total length of the beam between supports equals to D. There are two off-center force F loaded on the beam, with distance from zero-point as (D-d)/2 and (D+d)/2, respectively. The bending moment in the beam M can be described as function of distance from zero-point x:

$$EI\delta_1^{(2)} = -M_1 = -2Fx, \quad x \in \left[0, \frac{D-d}{2}\right]$$

$$EI\delta_2^{(2)} = -M_2 = -F(D-d), \quad x \in \left(\frac{D-d}{2}, \frac{D+d}{2}\right)$$

$$EI\delta_3^{(2)} = -M_3 = 2F(x-D), \quad x \in \left[\frac{D+d}{2}, D\right]$$

Here, E is elastic modulus and I is area moment of inertia of cross section. With integration of above equations for two times and continuous conditions at x=0, (D-d)/2, (D+d)/2 and D, we have the deflection curved described as function of x:

$$EI\delta_1 = \frac{Fx}{3}\left(3\frac{D-d}{2}\frac{D+d}{2} - x^2\right), \quad x \in \left[0, \frac{D-d}{2}\right]$$

$$EI\delta_2 = \frac{F(D-d)}{6}\left[3x(D-x) - \left(\frac{D-d}{2}\right)^2\right], \quad x \in \left(\frac{D-d}{2}, \frac{D+d}{2}\right)$$

$$EI\delta_3 = \frac{F(D-x)}{3}\left[3\frac{D-d}{2}\frac{D+d}{2} - (D-x)^2\right], \quad x \in \left[\frac{D+d}{2}, D\right]$$

Deflection at the center of beam (x=D/2)

$$\delta_{center} = \frac{F}{3EI}\frac{D-d}{2}\left[3\left(\frac{D}{2}\right)^2 - \left(\frac{D-d}{2}\right)^2\right] = \frac{F}{12EI}\frac{D-d}{2}(2D^2 + 2Dd - d^2)$$

The stress induced on certain point in cross section of the beam [75]

$$\sigma = \frac{My}{I}$$

Here, M is the bending moment $M_{center} = F(D-d)$ and y is vertical coordinate of the point (horizontal axis is the neutral axis) $y_{surface} = h/2$. Then we have the stress on the surface and center of beam

$$\sigma_{center} = \frac{M_{center}y_{center}}{I} = \frac{\delta_{\text{center}}12Eh}{2D^2 + 2Dd - d^2} \tag{4.1}$$

Theoretically, with known δ_{center} which could be read from Vernier scales, the induced stress could be estimated by **Eq. 4.1**. However, we noticed a problem by this method which is caused by the design of bending tool. With four Vernier scales, it was difficult to find a status that all of them just started to apply stress

simultaneously. In other word, the "zero-point" for stress was not an ideal zero-point. This problem may greatly overestimate lower stress (around 20 MPa).

Nevertheless, the linear relationship between σ_{center} and δ_{center} we derived would be useful in following sections.

4.1.2 Evaluation of Mechanical Stress by Correction with Si MOSFET

Application of strain engineering in Si MOSFETs has been well established and quantitative relationship between I_d-V_g characteristics and stress was described in details, as shown in **Fig. 4.5** [12].

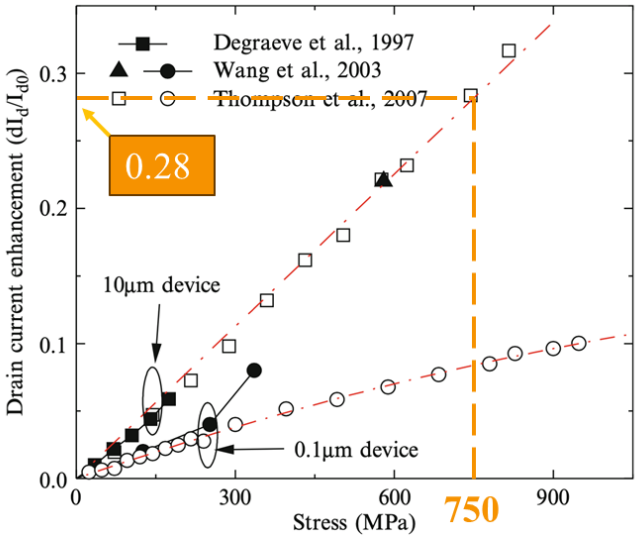

Figure 4.5 Drive current enhancement in uniaxial stressed n-MOSFETs [12].

On the Si device of 10 μm, with uniaxial tensile stress of 750 MPa, +28% enhancement in drain current was observed. Noted that much smaller enhancement on shorter channel device of 0.1 μm was due to parasitic resistance in source and

drain region R_{sd}. If R_{sd} was excluded from measurement, the mobility enhancement on devices with various channel length would be comparable [12].

We selected two Si (100) n-MOSFET devices of L/W=100 μm/100 μm and L/W=5 μm/50 μm to apply mechanical wafer bending; the devices are with 8-nm-thick oxide and channels along [110]. The field-effect mobility change regarding rotation of Vernier scales was recorded in **Fig. 4.6**, with data labels showing average value between devices. Here, R_{sd} was not excluded from mobility calculation by **Eq. 2.26** because its impact was relatively low when channel is in magnitude of 10 μm.

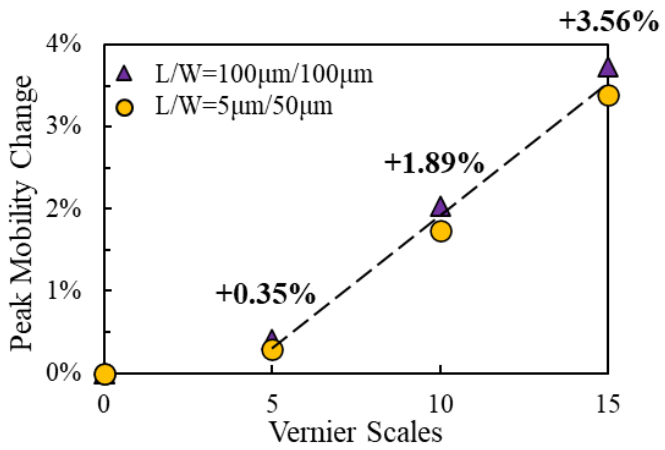

Figure 4.6 Mobility change in Si MOSFET regarding rotation of Vernier scales in wafer bending tool. The broken line is for the guide of eyes.

It can be clearly observed that, after rotating 5 scales from chosen zero-point, mobility increases linearly with more rotation of Vernier scales, demonstrating application of exact uniaxial tensile stress. Within first 5 scales, the stress in initial stage of wafer bending might not be uniaxial or uniformly distributed. This also confirmed our concern in Part 4.1.1 that lower stress would be overestimated if we used **Eq. 4.1** and count of Vernier scales to attempt direct calculation.

With measured mobility change, we can calculate corresponding stress in Si (100). If we control the wafer bending set up to be identical (wafer thickness difference was taken into consideration when setting zero-point for Vernier scales), then stress in SiC could be calculated by adapting **Eq. 4.1** into

$$\sigma_{SiC} = \sigma_{Si} \frac{E_{SiC} h_{SiC}}{E_{Si} h_{Si}} \tag{4.2}$$

Young's modulus and thickness of Si wafer and SiC wafer used in this chapter were summarized in **Table 4.1**.

Table 4.1 Young's modulus and thickness of Si wafer and SiC wafer.

	Si	SiC
Young's Modulus E	169 GPa	450 GPa [76]
Thickness h	570 μm	380 μm

Calculated stress in Si wafer and in SiC wafer were summarized in **Table 4.2**.

Table 4.2 Stress in Si wafer and in SiC wafer, regarding rotation of Vernier scales.

Vernier Scales	+5	+10	+15
Mobility Change	+0.35%	+1.89%	+3.56%
+28% mobility change → 750 MPa uniaxial tensile stress [12]			
Stress in Si (100)	9.3 MPa	50.5 MPa	95.4 MPa

$\sigma_{SiC} = \sigma_{Si} \frac{E_{SiC} h_{SiC}}{E_{Si} h_{Si}}$			
Stress in SiC (0001)	16.5 MPa	89.6 MPa	169.3 MPa

We expected error of 10% from this method, mainly introduced by the anisotropy of Young's modulus in SiC and extraction of quantitative relation between mobility change and stress from reference [12].

In this study, we regarded compressive stress as negative value and tensile stress as positive value. In addition, for displacement in opposite direction we took identical value with opposite sign, because the compression bending setting was exactly reverse to tension bending setting, e.g., the applied stress of 15 rotation of Vernier scales under compression bending was of -169.3 MPa.

4.2 Variation of Mobility with Stress

4.2.1 Impact of Parasitic Components on Mobilities

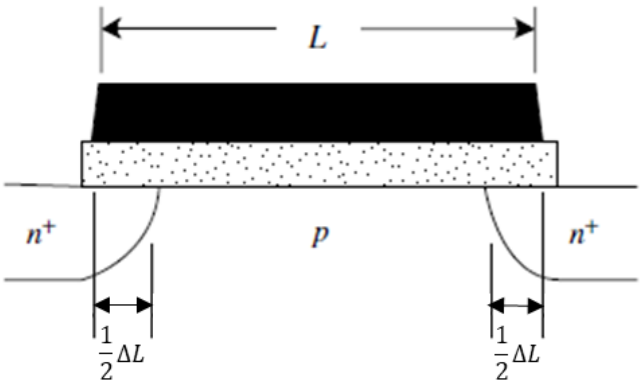

Figure 4.7 MOSFET device cross section showing actual gate length L and effective channel length difference ΔL [13].

The parasitic components, including source and drain resistance R_{sd} and effective channel length difference ΔL, as shown in **Fig 4.7**, are factors affecting accuracy of field-effect mobility and threshold voltage derived from I_d-V_g characteristics [77]. R_{sd} consists of "the source and drain contact resistance, the sheet resistance of the source and drain, the spreading resistance at the transition from the source diffusion to the channel, and any additional wire resistance" [13]. The difference between effective channel length L_{eff} and L originates from overlap between mask and source and drain region and usually leads to a shorter L_{eff}.

Because the activation process in fabrication of SiC MOSFET requires much higher temperature than in Si MOSFET, the conventional self-aligned process of gate material becomes unavailable, therefore a more significant overlap between mask and source and drain region is always induced in SiC MOSFET. It is necessary to decide whether R_{sd} and ΔL should be excluded from later researches on mobility and threshold voltage.

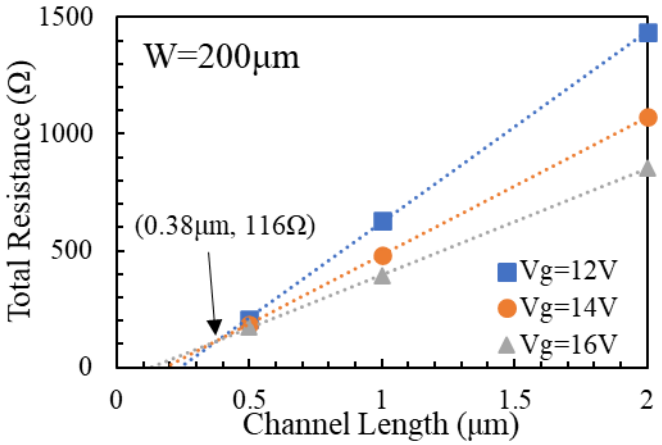

Figure 4.8 Total resistance versus channel length as a function of gate voltage. Intersect was marked.

Both R_{sd} and ΔL could be obtained by plotting total resistance-channel length relationship with different gate voltages and finding the intersect [13], as suggested by following equation:

$$R_{total} = R_{channel} + R_{sd} = \frac{L - \Delta L}{W_{eff}\mu_{eff}C_{ox}(V_g - V_{th})} + R_{sd}$$

The total resistance was extracted from drain current-drain voltage (I_d-V_d) characteristics as $R_{total} = V_d/I_d$. The relationship between total resistance and channel length on devices of W=200 μm was presented in **Fig 4.8**.

R_{sd} and ΔL on devices with various W was derived. We noticed that average value of ΔL was of 0.40±0.06 μm and independent from channel width. Relationship between R_{sd} and W was plotted in **Fig. 4.9**. R_{sd}-W plots on devices with thinner oxide layer, T_{ox}=16 nm and 28 nm, were also presented for comparison. It is obvious that R_{sd} decreased in channel with larger W, which was as expected because theoretically resistance is proportional to the reciprocal of channel's cross section area, $R \propto 1/W$. However, by plotting R_{sd}*W-W plot, we noticed that R_{sd}*W increased when W is larger than 400 μm. This phenomenon might be due to the parallel connection design of channels with larger width (W≥800 μm). In addition, we also observed comparable R_{sd} in devices with different T_o. but identical W. Those results demonstrated that parasitic components in our devices were only introduced during channel fabrication process, hence they were supposed to remain constant when measurement was on same device.

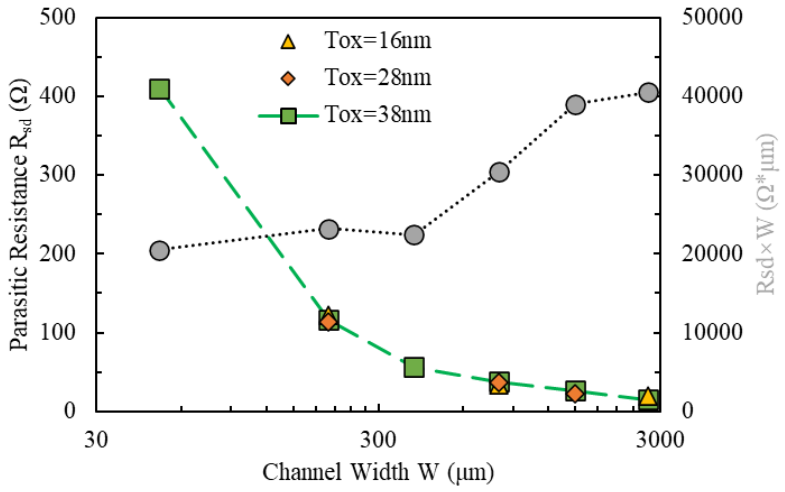

Figure 4.9 R_{sd} and R_{sd}*W as functions of channel width W.

With extracted parasitic components, we could correct the mobility by modifying **Eq. 2.26** into

$$\mu_{\mathrm{FE}} = \frac{L - \Delta L}{W C_{ox}(V_d - R_{sd} I_d)} \frac{\partial I_d}{\partial V_g} \tag{4.3}$$

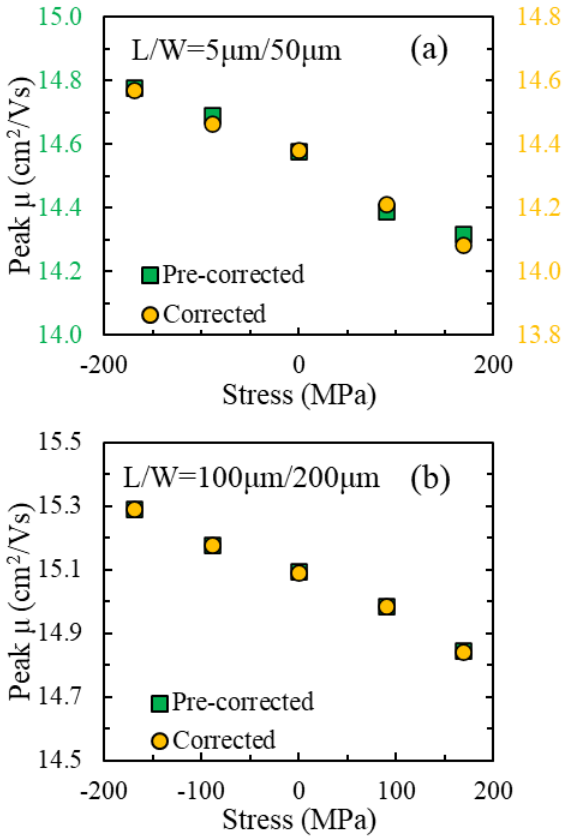

Figure 4.10 Pre-corrected and corrected mobilities on devices of (a) L/W=5 μm/50 μm and (b) L/W=100 μm/200 μm.

Pre-corrected and corrected mobilities with stress perpendicular to channel were plotted in **Fig. 4.10**. In a smaller channel (L/W=5 μm/50 μm), the exclusion of R_{sd} and ΔL caused averagely -0.3 cm^2/Vs difference on mobilities, as shown in **Fig. 4.10 (a)**, which meant that mobility was overestimated for 2% due to existence of parasitic components. However, we also noticed that the mobility variation with stress didn't change before and after the exclusion of parasitic components. In a

larger channel (L/W=100 μm/200 μm), almost no difference in mobility value or in mobility variation with stress was observed, as shown in **Fig. 4.10 (b)**. The stress-induced mobility variations in smaller and larger channels were also comparable. Those results indicated that existence of parasitic components didn't have impact in variation induced by stress. Therefore, we didn't exclude the parasitic components from mobility calculation in later researches.

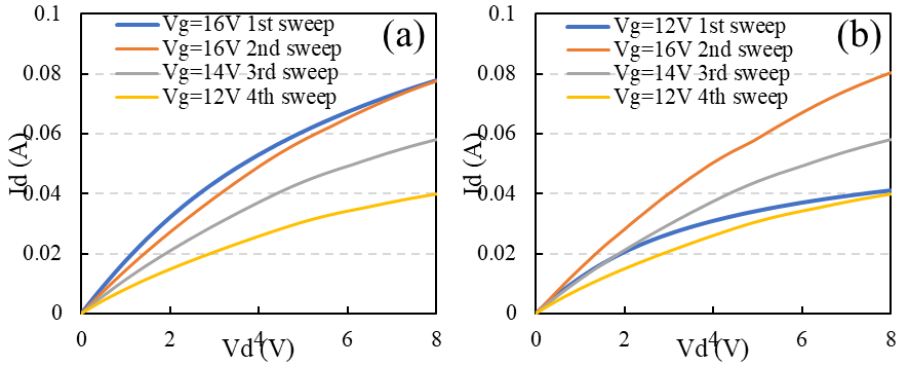

Figure 4.11 I_d-V_d characteristics on the same device with first sweep with (a) V_g=16 V and (b) V_g=12 V.

In addition, we noticed a first-sweep effect during I_d-V_d measurement on SiC MOSFETs. In **Fig. 4.11 (a)**, the first sweep with V_g=16 V showed averagely higher I_d than the second sweep with V_g=16 V; in **Fig. 4.11 (b)**, the first sweep with V_g=12 V showed averagely higher I_d than the fourth sweep with V_g=12 V. Therefore, we concluded that the appearance of such first-sweep effect was not due to gate voltage value; this phenomenon was probably caused by p-body not grounded during measurement. To reduce the error, we had a pre-measurement sweep before each I_d-V_d measurement on SiC MOSFETs.

4.2.2 Variation of Mobility with Stress

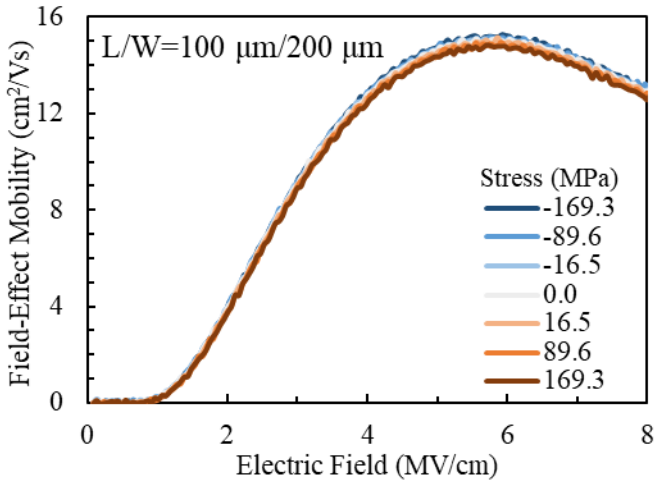

Figure 4.11 Mobility under electric field with stress.

Fig. 4.12 shows a typical series of mobility with stress perpendicular to channel. It can be clearly observed that mobility increased with compressive stress and decreased with tensile stress, which were consistent to previous reports [11].

Fig. 4.13 summarizes mobility variation with stress on SiC [11-20] devices and Si [110] devices. We chose channels of two sizes (L=5 μm and L=100 μm) and applied bending perpendicular and parallel to channels on both SiC and Si devices. On Si devices, parallel bending induced mobility variation a bit more than perpendicular bending, and compression induced mobility decrease while tension induced mobility increase. Compared to Si, the mobility variation on SiC with comparable stress was much less. Mobility variation with perpendicular stress of 170 MPa was of 1.5%, while with parallel stress it was even less. We also noticed that the variation on different size channels was very close to each other, on both

SiC and Si, which suggested that peripheric conditions of channel had no impact in stress-induced mobility variation.

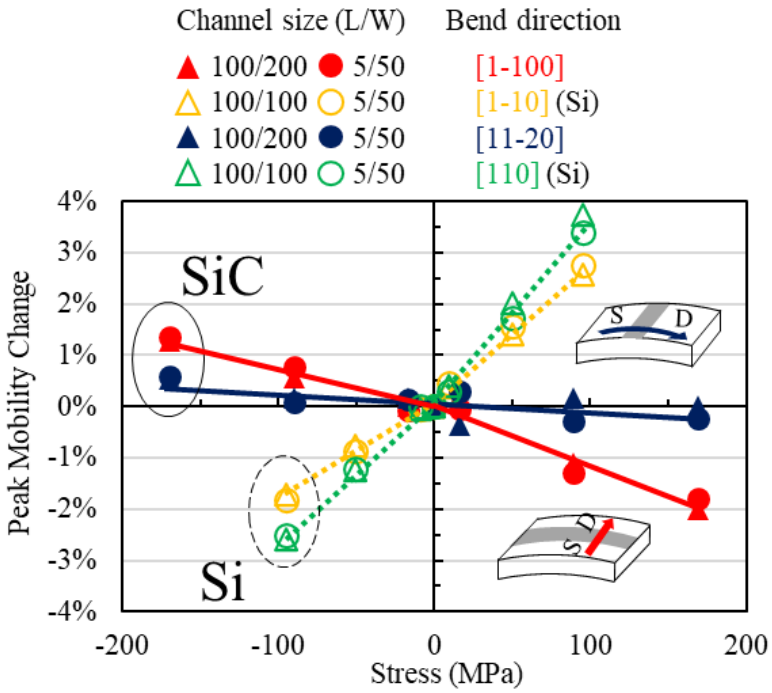

Figure 4.13 Variation of mobility under bending.

Our observed trend that perpendicular bending induced more variation than parallel bending on SiC was consistent to previous report [11], yet mobility variation was relatively less. Such difference might be due to fabrication process conditions.

4.3. Threshold Voltage Change with Stress

4.3.1 Relationship between Change of Linear Extrapolation Threshold Voltage and Change of Flat-Band Voltage

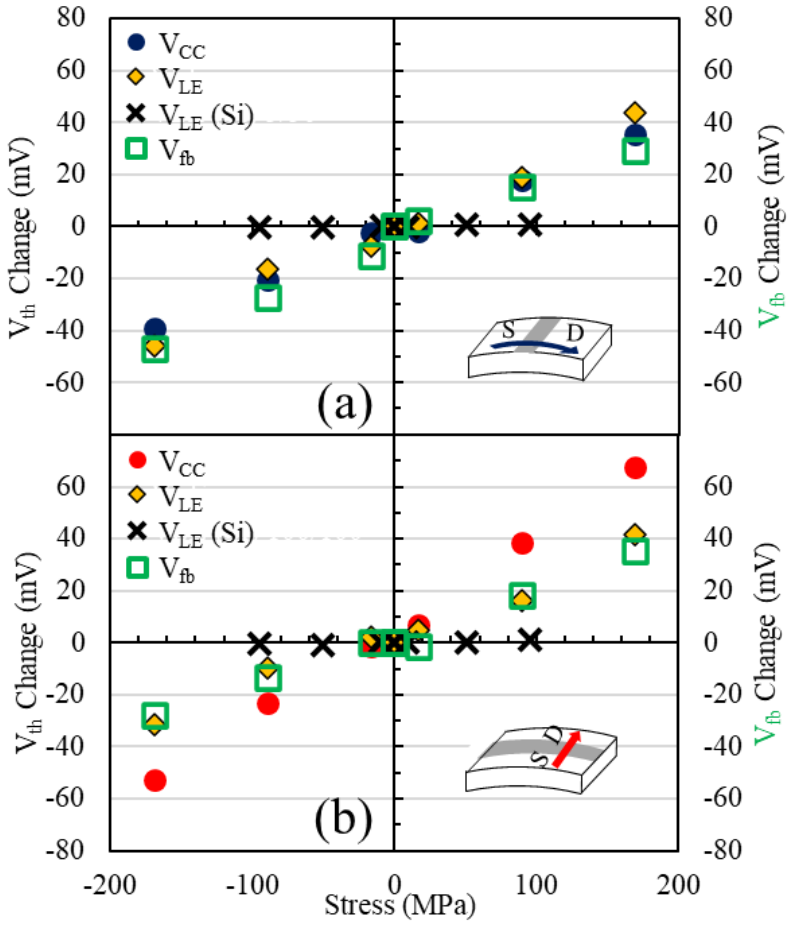

Figure 4.14 Variation of V_{th} and V_{fb} under stress in SiC device of L/W=5 μm/50 μm, in comparison to Si device, when bending is (a) parallel or (b) perpendicular to channel.

In **Fig. 4.14**, we summarized change of V_{LE} and V_{CC} on SiC n-MOSFET, V_{LE} on Si n-MOSFET, and V_{fb} on n-type SiC MOS capacitor of L=5 μm with stress. **Fig. 4.14 (a)** shows the results when the bending was parallel to the current. As we observed that V_{LE} change on Si MOSFET was less than 1 mV (which is consistent to previous report on Si device [78]), however, V_{LE} change on SiC MOSFET with

stress of 170 MPa was as high as 40 mV, which is compliant to previous reports [79][80]. We also noticed that the magnitude of V_{fb} change on SiC was very close to that of V_{LE} change, suggesting that V_{LE} change is mainly attributable to V_{fb} change in SiC.

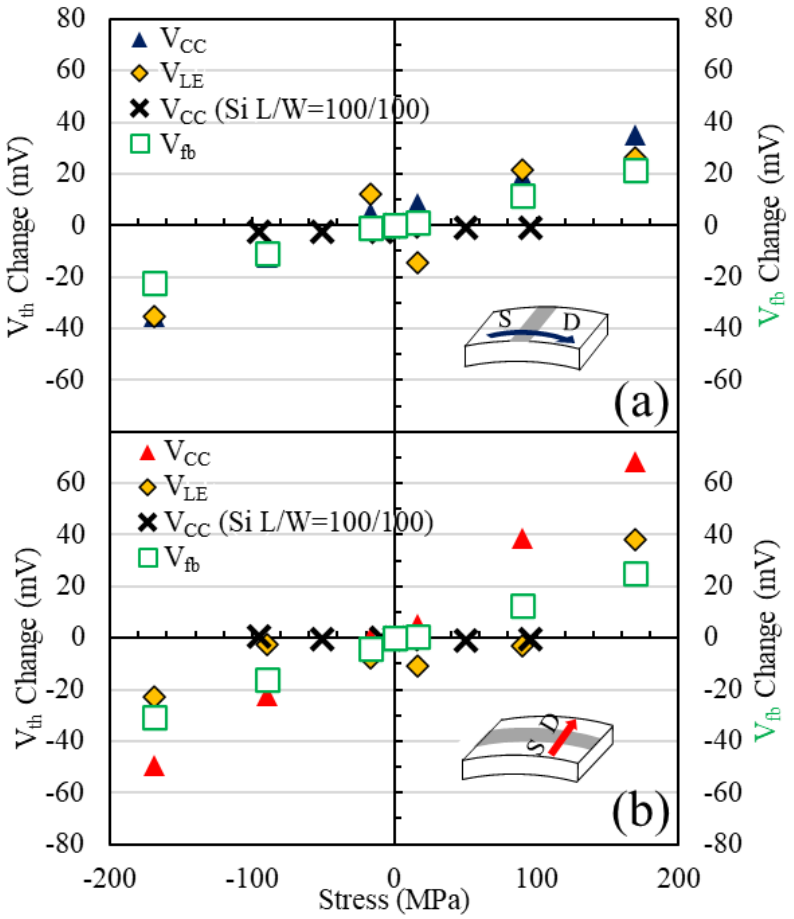

Figure 4.15 Variation of V_{th} and V_{fb} under stress in SiC device of L/W=100 μm/200 μm, in comparison to Si device, when bending is (a) parallel or (b) perpendicular to channel.

While under parallel bending V_{CC} change was also close to V_{LE} change, however as shown in **Fig. 4.14 (b)**, under perpendicular bending V_{CC} change was twice larger than V_{LE} change. Though no clarification so far, we assumed this additional V_{CC} change could be related with more significant mobility variation

under perpendicular bending. What's more, change in V_{LE} and V_{fb} under parallel or perpendicular bending were all close to each other, whereas V_{CC} change of Si MOSFET under perpendicular bending was still less than 1 mV.

Study in **Fig. 4.14** was applied on devices of L=100 μm as well, as shown in **Fig 4.15**. Despite some fluctuation, we obtained results in same magnitude, suggesting that peripheric conditions of channel had no impact in stress-induced V_{th} change either.

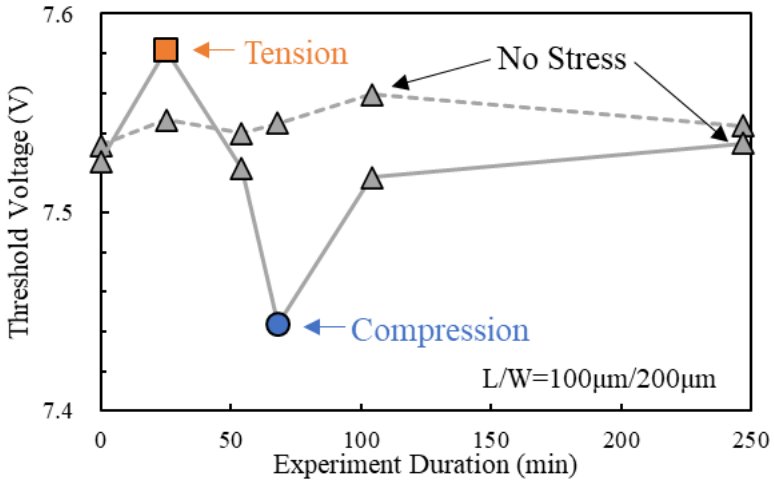

Figure 4.16 Variation of V_{CC} measurement with stress of 170 MPa, in comparison to sequence without stress.

To confirm such anomalous V_{th} change in SiC device was not due to measurement error or mis-operation, we applied a repeatability test. As described in **Fig. 4.16**, we measured V_{CC} before, during and after applying stress of 170 MPa, and did alternate measurement sequence without stress application for comparison. We observed that stress-induced V_{CC} change recovered immediately after stress was released. By comparing V_{CC} fluctuation (±13 mV) in each measurement sequence, we considered that such fluctuation was not due to measurement duration or stress

application but because of bias sweeping effect. This test confirmed the reliability of our measured V_{th}, and suggested that there was no destructive change being responsible for observed stress-induced variation, hence the origin of such variation was not generation of defects.

Despite we concluded that V_{fb} change is main cause of V_{th} change with stress, the physical origin of V_{fb} change remains unclear so far. Here are two major assumptions regarding it. The first one is change in band alignment, which might be induced by change in dipole layer, in work function of gate material [81] or in Fermi level of SiC. The dipole layer magnitude at SiO_2/SiC was reported to be introduced by the formation of N-Si bonds aligned on SiC surface [82][61] and it might be affected by mechanical stress. The conduction band offset between SiC and SiO_2 should induce change as well in this case. The other assumption is change in near-interface fixed charge density, for non-zero V_{fb} originates from fixed charges, and it is possible that their instable density at nitridated interface [83] is affected by mechanical stress. Both assumptions would be further studied in following chapter.

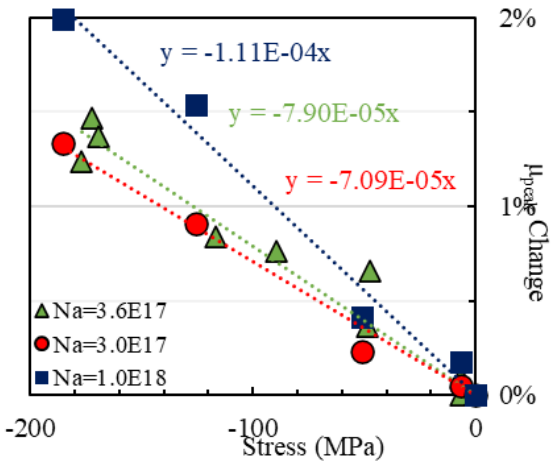

Figure 4.17 Peak mobility change as a function of stress in different device series.

4.3.2 Change of Constant-Current Threshold Voltage

We came up with the assumption in above part that the significant change of V_{CC} with stress perpendicular to channel should be related with stress-induced mobility change. From here, we are going to quantitatively describe V_{CC} as a function of stress.

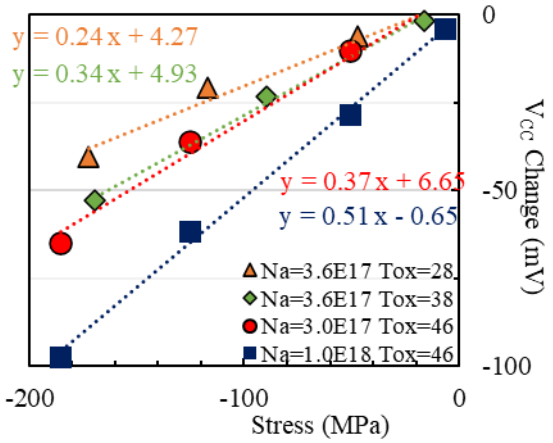

Figure 4.18 V_{CC} change as a function of stress in different device series.

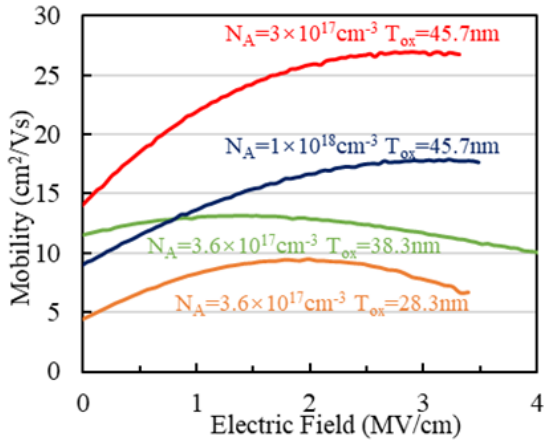

Figure 4.19 Field-effect mobility on different device series.

When the doping concentration in channel is identical, it's observed in **Fig. 4.17** that the mobility change is not of T_{ox} dependence (green triangles represent

data with different T_{ox}). It needs to be noted that μ change with stress is positively related with N_A however not so with the un-stressed mobility value, as indicated between **Fig. 4.18** and **Fig. 4.19**.

In **Table 4.3**, we slope of μ change-stress plot K_1, slope of V_{fb} change-stress plot K_2, slope of V_{CC} change-stress plot K_3, and coefficient K defined as $K_3 = K_2 K_1 K$. Calculated K is of average value of -1.8×10^4 with acceptable error of 10%, which confirms the linear relationship between V_{CC} change-μ change and between V_{CC} change-V_{fb} change. The empirical formula of V_{CC} change is

$$\Delta V_{CC} = -1.8 \times 10^4 \cdot \Delta V_{fb} \cdot \Delta \mu$$

It is inferred that V_{CC} change could be used to evaluate μ change indirectly.

Table 4.3 K_3, K_2, K_1 and K from various plots with stress.

K_3 ($mV \cdot MPa^{-1}$)	K_2 ($mV \cdot MPa^{-1}$)	K_1 (MPa^{-1})	K (MPa)
0.37	0.29	-7.09E-05	-1.8E+04
0.51	0.29	-1.11E-04	-1.6E+04
0.24	0.17	-7.90E-05	-1.8E+04
0.34	0.22	-7.90E-05	-2.0E+04

4.4 Summary

Uniaxial mechanical stress' impact on electrical characteristics of SiC MOSFET has been systematically studied. We estimated mechanical stress value by comparison with Si MOSFET. We reported on variation of field-effect mobility with stress and concluded that existence of parasitic resistance didn't affect such stress-induced variation. We observed change in V_{th} of around 40 mV with stress of 170 MPa; by comparing V_{th} change with V_{fb} change, we concluded that the V_{th} change with stress was mainly attributed to change in V_{fb}. We suggested that change in band alignment change and change in fixed oxide charge density are possible origins of V_{fb} change with stress.

Chapter 5

Investigation on Origins of Mechanical Stress-Induced Device Performance Change

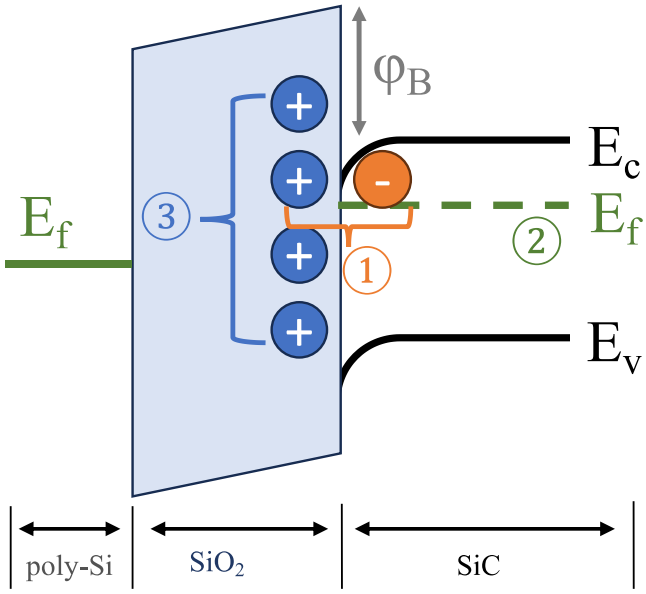

Figure 5.1 Distribution of origins of non-zero V_{fb} in SiC MOS: 1) dipole layer, 2) work function difference and 3) fixed oxide charges.

As introduced in Chapter 2, non-zero V_{fb} in practical SiC MOS capacitor is usually caused by work function difference and inevitable occurrence of fixed oxide charges. In addition, with application of post-oxidation nitridation process, it was

reported that dipole layer, induced by Si-N bond, would form at SiC/SiO_2 interface [61]. With considerations above, **Eq. 2.24** adapts into

$$V_{fb} = \varphi_{dipole} + \varphi_{ms} - \frac{Q_{ox}}{\varepsilon_{ox}} T_{ox} \tag{5.1}$$

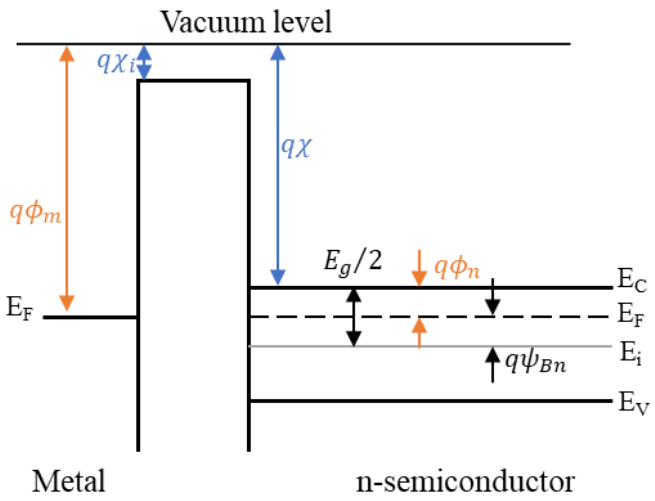

Figure 5.2 Energy band diagrams of ideal MIS capacitors at equilibrium (V=0).

Each term in the right of **Eq. 5.1** is presented in **Fig. 5.1**. Nitridation-induced dipole layer is decided by nitridation condition and crystal orientation [61]. Work function difference between gate material and semiconductor is decided by work function of gate material φ_m, electron affinity of semiconductor χ_s and the energy difference $E_C - E_f$ from Fermi level to bottom of conduction band, as presented in **Fig. 5.2** and defined by $\varphi_{ms} = \varphi_m - q\chi_s - (E_C - E_f)$. Dipole layer change or Fermi level change may cause band alignment shift in this system, and electron barrier height φ_B change might happen as consequence, inducing V_{fb} change. Fixed oxide charges refer to those near-interface fixed charges which are attributable to oxidation and annealing process.

In Chapter 4, we concluded that the change of V_{LE} with stress was attributed to change of V_{fb} and suggested that the change of V_{CC} might be related with significant mobility change. In this chapter, we would investigate in the origin of V_{fb} change with stress perpendicular to channel, mainly considering band alignment shift and fixed oxide charges change. We would also study in impact of mobility on threshold voltage.

5.1 SiC MOSFET Conditions

Table 5.1 Series of SiC MOSFET.

Sample Series	**A**			**B**			**C**		
P-well $N_A/10^{17}$ cm^{-3}	3.6			3.6	1.0	0.6	3	10	30
CVD thickness by design/nm		20	35	8			50		
Thermally oxidized thickness by design/nm	10	5	10						
Actual CET/nm	15.5	28.3	38.3	9.5			46		
Gate electrode	n+ poly-Si			p+ poly-Si			p+ poly-Si		
Epitaxial $N_D/10^{14}$ cm^{-3}	30			7			30		
φ_{ms}/eV	0.66			1.74			1.78		

Three sets of SiC MOSFET devices with various process conditions were used in this chapter, as summarized in **Table 5.1**. Post-oxidation nitridation process is of identical condition and was applied on every series.

Series A devices were identical to those used in Chapter 4, with two more different thickness of oxide layer.

Series B devices were of CMOS similar to series A, except for the oxide was solely formed by CVD process.

Series C devices were of only n-MOSFET and their oxide were solely formed by CVD process as well.

To estimate work function difference between gate material and semiconductor, we took values as followed: work function of p-doped poly-silicon (p+ poly-Si) 5.17 eV [84] and work function of n-doped poly-silicon (n+ poly-Si) 4.05 eV [84].

I_d-V_g measurement was done on n-MOSFET.

I_d-V_g and C-V_g measurement was done on p-MOSFET.

5.2 Shift of Band Alignment

5.2.1 Fowler-Nordheim Tunneling and Poole-Frenkel Emission

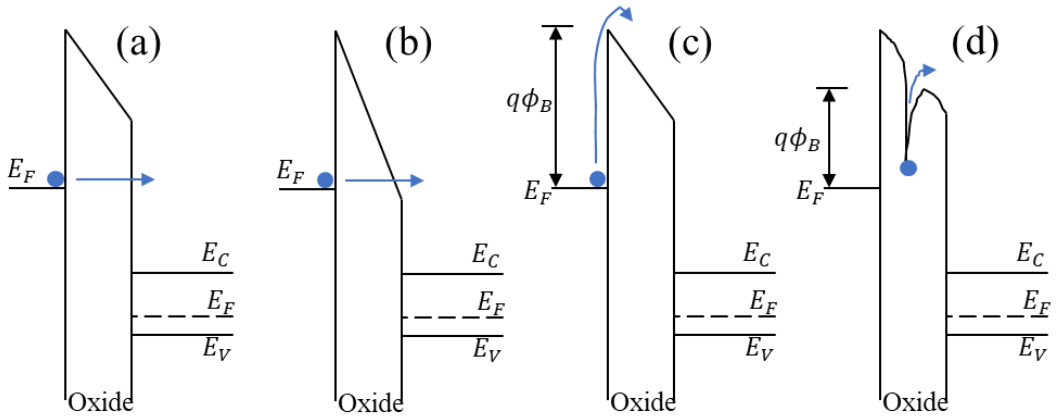

Figure 5.3 Energy band diagrams showing (a) direct tunneling, (b) F-N tunneling, (c) thermionic emission and (d) P-F emission.

In SiO_2/Si system, the current leakage mechanism is a perfect Fowler-Nordheim (F-N) tunneling [85], as shown in **Fig. 5.3 (b)**. In SiO_2/4H-SiC system, however, the interface is much worse due to defects [86] and the transition layer is with unneglectable thickness [87]. It was reported that, despite F-N tunneling dominates leakage current in SiO_2/4H-SiC system when temperature is lower than 0 °C, Poole-Frenkel (P-F) emission, as shown in **Fig. 5.3 (d)**, also contributes under room temperature [88][89].

Electron barrier height φ_B could be determined from F-N current J_{FN}, as [61]

$$J_{FN} = \frac{q^3 m_{sc}}{8\pi h m_{ox} \varphi_B} E_{ox}^2 exp\left(-\frac{4\sqrt{2m_{ox}\varphi_B^3}}{3qhE_{ox}}\right) \quad (5.2)$$

Here, h is Planck's constant, E_{ox} is oxide electric field, m_{sc} and m_{ox} are effective mass in the semiconductor (0.29 m_e) and in the oxide (0.42 m_e) [88].

To extract F-N current from measured total current, we need to first exclude P-F current. In ideal design, F-N current should be measured with stress under low temperature to directly derive electron barrier height with stress. However, the low temperature in our research is produced within a vacuum chamber, making it difficult to apply mechanical stress via wafer bending method. Therefore, to extract F-N current with stress under room temperature, we divided the measurement into multiple steps, details described as below. Note that this measurement was based on the assumption that P-F emission was not affected by mechanical stress.

1) Measure leakage current under low temperature (≤-50 ℃). At this temperature, total current is regarded as pure F-N current.

2) Estimate F-N current under room temperature (RT) by known temperature dependence of F-N current. This dependence can be described by functions below [88][89]:

$$J_{FN} \propto \int n(E)T_c(E)\,d(E)$$

$$n(E) = N(E)F(E) = M_c \frac{\sqrt{2}m_{de}^{3/2}(E-E_c)^{1/2}}{\pi^2\hbar^3} \frac{1}{1+\exp\left(\frac{E-E_f}{kT}\right)}$$

$$N_D \approx N_C \exp\left(-\frac{E_c - E_f}{kT}\right)$$

$$T_c(E) = \exp\left\{-\frac{4\sqrt{2m_{ox}\left[\varphi_B - (E-E_f)\right]^3}}{3\hbar q E_{ox}}\right\}$$

Here, M_c is the number of equivalent minima in the conduction band, m_{de} is the density-of-states effective mass for an electron and k is Boltzmann constant.

3) Measure leakage current under RT. The measured current is sum of F-N current and P-F current.

4) Estimate P-F current under RT by excluding estimated F-N current under RT from measured current under RT.

5) Measure leakage current under RT with stress.

6) Estimate F-N current under RT with stress by excluding estimated P-F current under RT from measured current under RT with stress.

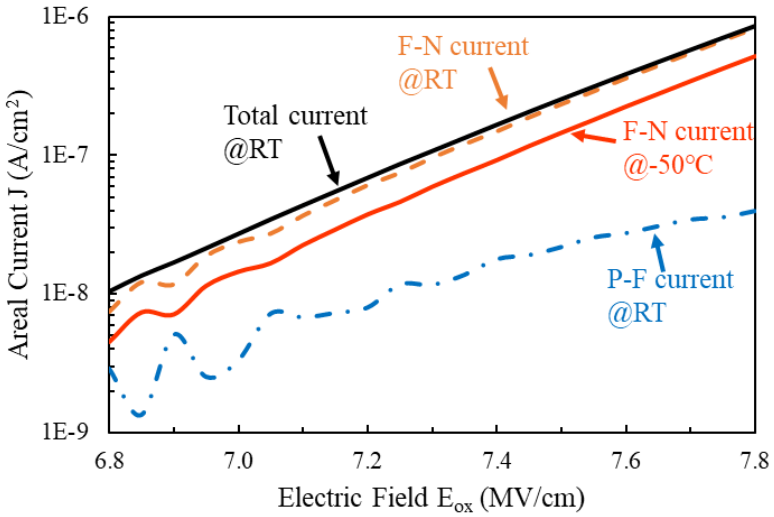

Figure 5.4 Measured and estimated currents on series A device of L/W=100 μm/200 μm.and T_{ox}=38 nm.

Fig. 5.4 shows currents measured or estimated from step 1 (red solid line), 2 (orange broken line), 3 (black solid line) and 4 (blue broken line).

5.2.2 Change of Electron Barrier Height

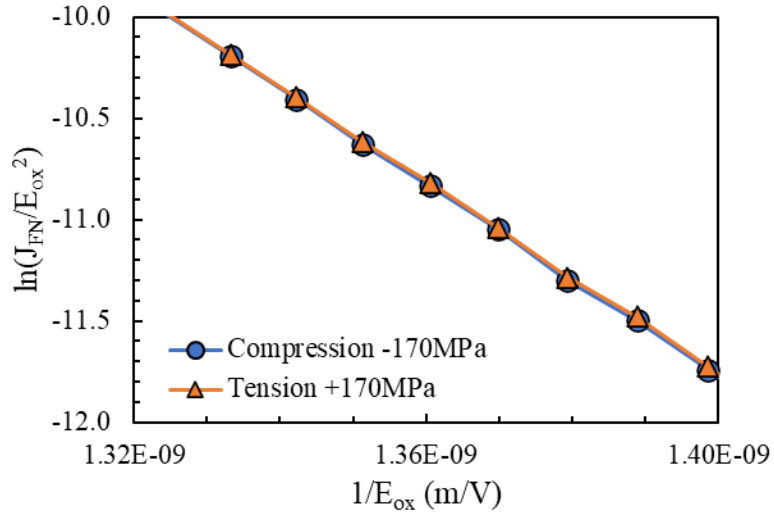

Figure 5.5 Plots of $\ln(J_{FN}/E_{ox}^2)$ versus $1/E_{ox}$ with compressive or tensile stress, on same device as in **Fig. 5.4**.

Consider **Eq. 5.2** with F-N current under RT: by plotting $\ln(J_{FN}/E_{ox}^2)$ versus $1/E_{ox}$, the linear approximation should give slope as $-4\sqrt{2m_{ox}\varphi_B^3}/3qh$, where φ_B can be derived. **Fig 5.5** shows the plots with compressive or tensile stress of 170MPa where we observed insignificant difference between them.

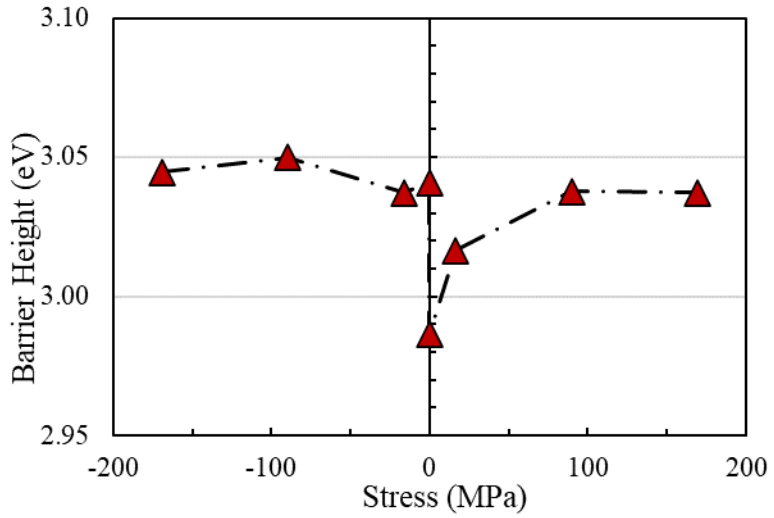

Figure 5.6 Variation of barrier height with stress, on same device as in **Fig. 5.4**.

Fig. 5.6 shows barrier height change with stress. We noticed that, despite the change between -170 MPa and +170 MPa is relatively small (as indicated in **Fig. 5.5**), yet the change with increasing tensile stress in significant.

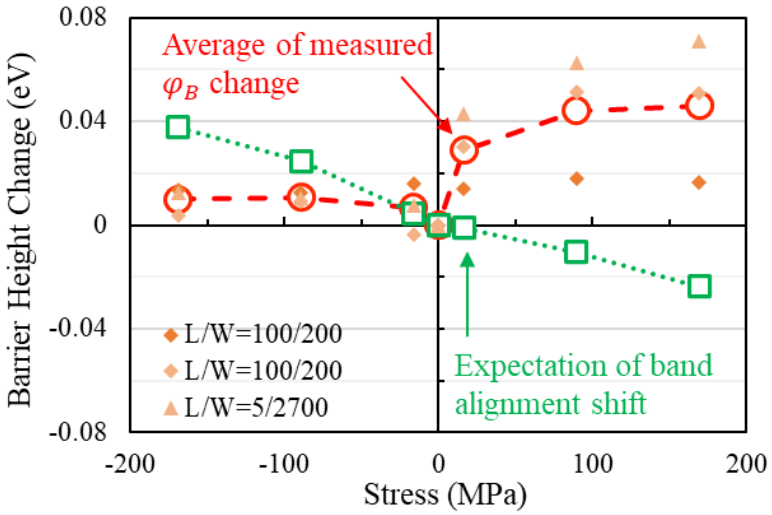

Figure 5.7 Barrier height change on series A device of T_{ox}=38 nm.

Fig. 5.7 shows φ_B change on devices of identical conditions but sizes, with average value of φ_B change (red circle with broken lines). It's noted that measurement on two identical devices of L/W=100 μm/200 μm shows great difference with tensile stress, indicating large measurement error under tension. On the other hand, with compressive stress, the φ_B change is in good agreement. Under compression of 170 MPa, around +0.01 eV was induced in φ_B. Nevertheless, if we assume band alignment shift being the only cause of V_{fb} change, then the φ_B change induced under compression of 170 MPa should be as high as +0.04 eV (green square with dotted line). Therefore, we concluded that band alignment shift is not the only cause of V_{fb} change with stress.

5.3 Change of Fixed Oxide Charges

5.3.1 In Thermally Grown Oxide Layer

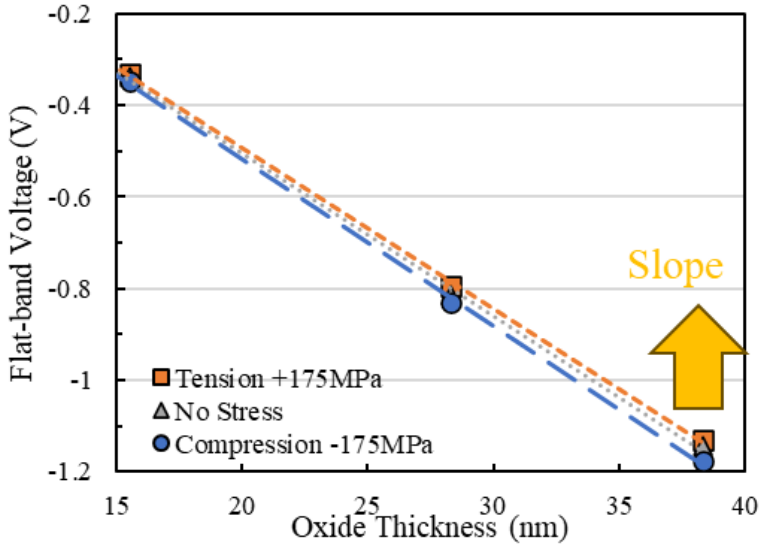

Figure 5.8 Plot of flat-band voltage versus oxide thickness as a function of stress, on series A device of L/W=100 μm/200 μm.

In addition to band alignment shift, the change of fixed oxide charges with stress was also studied. **Fig. 5.8** shows plots of V_{fb} versus T_{ox} with compression or tension of 175 MPa. According to **Eq. 5.1**, the slope of the plot equals to $-qN_{ox}/\varepsilon_{ox}$, and offset is the sum of φ_{dipole} and φ_{ms}. It's observed that the slope changes, increasingly or decreasingly, when compressive or tensile stress was applied, indicating increase or decrease in fixed oxide charges. In following discussion, we assume that $\Delta\varphi_{ms} = 0$ and dipole layer change solely contributes to offset change.

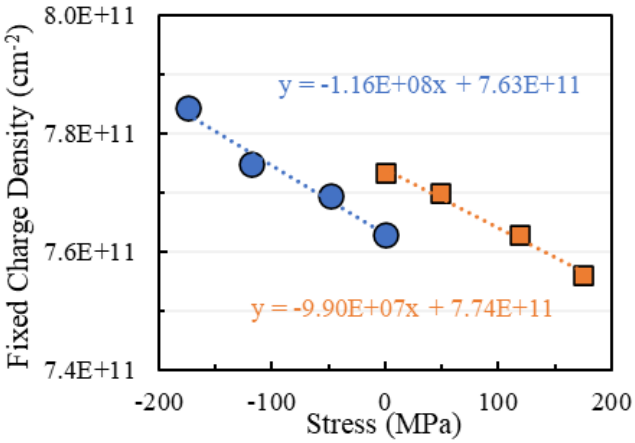

Figure 5.9 Fixed oxide charge density in relationship with stress, on series A device of L/W=100 μm/200 μm.

Fig. 5.9 shows fixed oxide charge density N_{ox} in relationship with applied stress. Around 3% change of N_{ox} was observed, with compression or tension of 170 MPa. It's also noted that compressive stress induced more change; by linear approximation, it's confirmed that compression induced nearly one more time of N_{ox} change compared to tension.

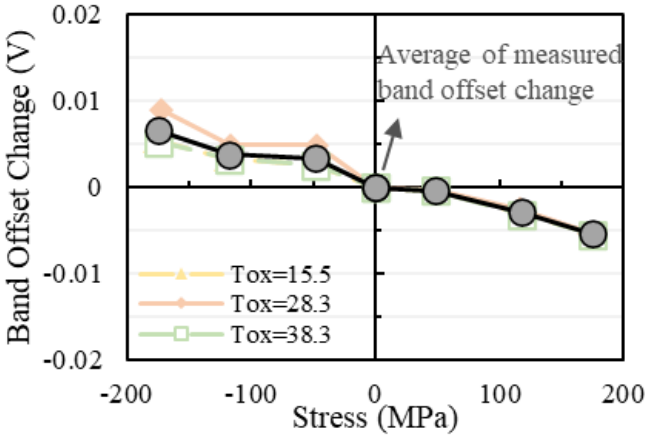

Figure 5.10 Dipole change derived from V_{fb}-T_{ox} plot with stress, on series A device of L/W=100 μm/200 μm.

Fig. 5.10 shows dipole layer change (derived from V_{fb}-T_{ox} plot) in relationship with stress. It's noticed that the measurement under compression had smaller variation between devices of different oxide thickness. By taking average value of

offset change, we observed +0.01 V change under compression of 170 MPa. Note that this is a close value to barrier height change observed in **Fig. 5.7**, confirming the reliability of both measurements with compressive stress.

5.3.2 In CVD Oxide Layer

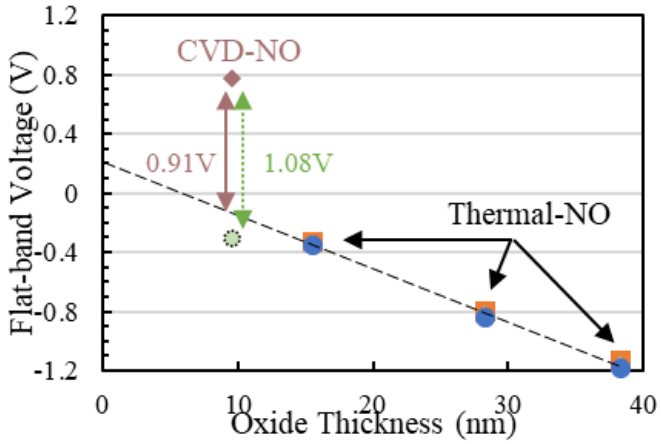

Figure 5.11 V_{fb}-T_{ox} with stress, on series A and series B device of L/W=100 μm/200 μm. The broken line is for the guide of eyes.

Despite the V_{fb}-T_{ox} plot in **Fig. 5.8** shows good agreement among series A devices, however, it seems that series B device didn't fit in the plot well, as presented in **Fig. 5.11**. A gap of estimated 0.91 V was observed between practical and expected V_{fb} of series B device, noting that the difference between φ_{ms} on series A and B is 0.66-1.74=-1.08 eV, which indicates that series B still falls out of

series A plot with a considerable gap of 0.91-1.08=-0.17 V even if we take φ_{ms} into consideration.

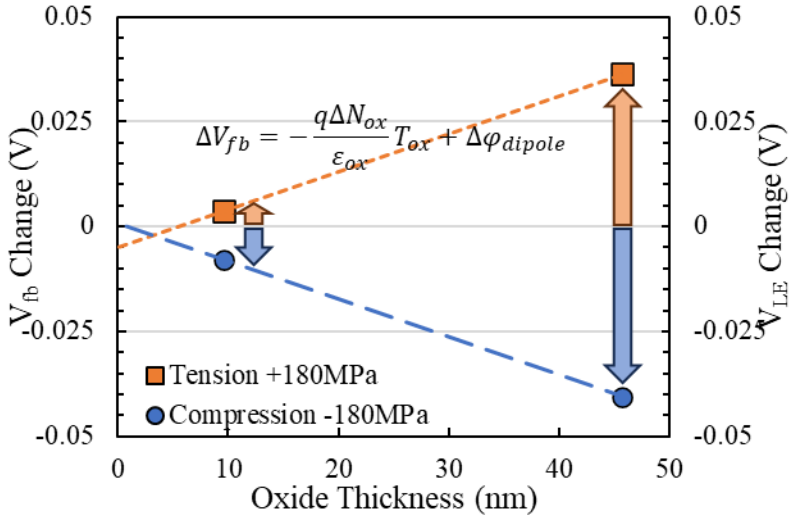

Figure 5.12 V_{fb} change with stress on series B and V_{LE} change with stress on series C.

In addition to φ_{ms} difference, as presented in **Table 5.1**, the oxide layer formation is also different between series A and B. In series A, SiO_2/SiC interface formed with thermal oxidation or post-CVD thermal oxidation; in series B and C, the interface formed with CVD process. Despite identical post-oxidation nitridation process was applied on every device (which was reported to produce identical dipole layer on interface formed by thermal oxidation [61]), it's indicated in **Fig. 5.11** that dipole layer and near interface fixed oxide charges density may be different when the oxidation process is of different approach, hence the change of N_{ox} and dipole under stress could also be different.

As stated in Section 5.1, series C contains only n-MOSFET and no MOS capacitor, making it challenging to directly derive V_{fb} from capacitance-gate voltage characteristics. However, as concluded in Section 4.3 that V_{LE} change in n-

MOSFET with stress should be solely attributable to V_{fb} change on n-type substrate, we considered that V_{LE} change on series C could be regarded as comparable to V_{fb} change on series C. Based on **Eq. 5.1** and the assumption that $\Delta\varphi_{ms} = 0$, we have

$$\Delta V_{fb} = \Delta\varphi_{dipole} - \frac{\Delta Q_{ox}}{\varepsilon_{ox}} T_{ox} \tag{5.3}$$

V_{fb} change with stress on series B was plotted along with V_{LE} change with stress on series C in **Fig. 5.12**, to describe the relationship between V_{fb} change and T_{ox} with compression or tension of 180 MPa. The slope of linear approximation equals to $-q\Delta N_{ox}/\varepsilon_{ox}$.

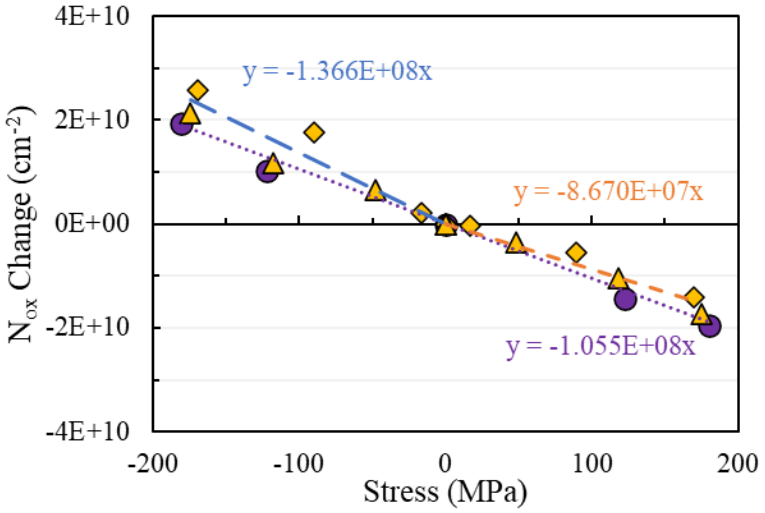

Figure 5.13 Fixed charge density change with stress in thermal oxide or CVD oxide. Thermal oxide devices of two sizes (triangle as L/W=100 μm/200 μm and diamond as L/W=20 μm/1500 μm) were plotted.

The comparison of N_{ox} change with stress in thermal oxide or CVD oxide is described in **Fig. 5.13**. While in thermal oxide the N_{ox} change under compression was larger than under tension, it's noticed that in CVD oxide the N_{ox} change under

compression and under tension were even and in the medium of the N_{ox} change in thermal oxide.

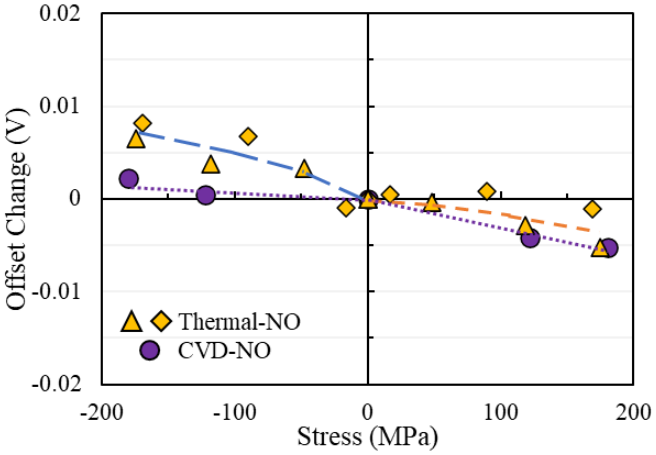

Figure 5.14 Dipole change with stress in thermal oxide or CVD oxide. Thermal oxide devices of two sizes (triangle as L/W=100 μm/200 μm and diamond as L/W=20 μm/1500 μm) were plotted.

The comparison of dipole change with stress in thermal oxide or CVD oxide is described in **Fig. 5.14**. It's observed that dipole in thermal oxide is more sensitive to compression and less sensitive to tension, compared to dipole in CVD oxide.

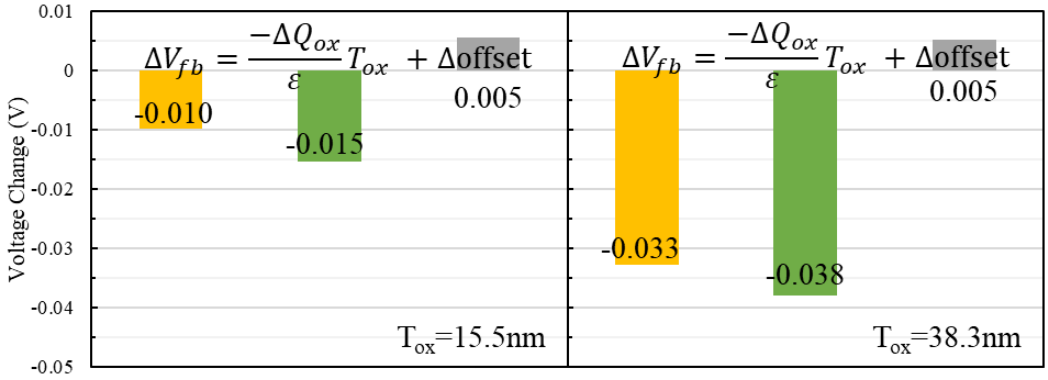

Figure 5.15 V_{fb} change (yellow) and sum of fixed charges change (green) and dipole change (gray), in thermal oxide of 15.5 nm (left) and 38.3 nm (right), with stress of 175 MPa.

V_{fb} change and sum of fixed charges change and dipole change, in thermal oxide with compression, are compared in **Fig. 5.15**. It can be seen that the sum of fixed charges change and dipole change can almost explain the induced V_{fb} change.

At this stage, we could give the assumption that observed fixed charges change and dipole change are induced by lowering of conduction band edge. Based on previous theoretical calculation in bulk SiC [8], energy gap is expected to lower for around 0.2 eV with tensive strain of +2%; by estimation, energy gap should lower for 4 meV with tensile stress of 180 MPa. Though we don't have profile of fixed charges yet, we can make a rough comparison based on D_{it} distribution, for both interface traps and fixed charges locate near to interface. In series A, Fermi level locates 0.18 eV lower than conduction band edge. At a given energy level 3 meV away from Fermi level, the D_{it} would be around 3% different from that at Fermi level. Assuming near interface fixed charges share similar distribution, then this 3% difference can exactly fit in the fixed oxide charge change we observed when applying stress near to 180 MPa. With acceptable error, our assumption that stress-induced lowering of conduction band edge can well explain our observation and calculation.

5.4 In Comparison with p-MOSFET

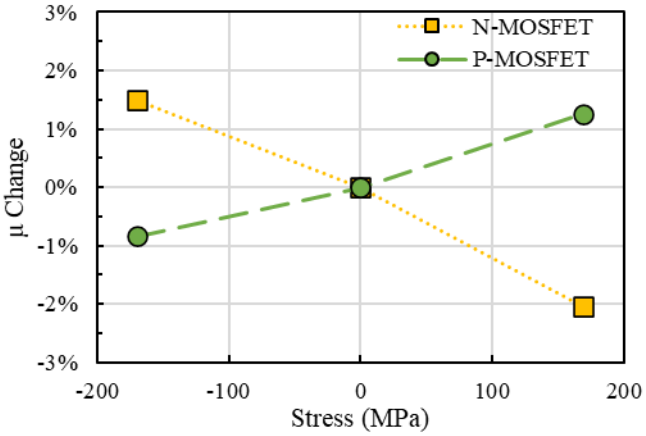

Figure 5.16 Peak mobility change with stress in n-MOSFET and p-MOSFET on series A device of T_{ox}=38.3 nm.

Comparison of mobility change with stress in n-MOSFET and p-MOSFET is plotted in **Fig. 5.16**. The percentage of mobility change is smaller in p-MOSFET, likely due to lower carrier concentration in n-type epitaxial layer compared to highly doped p-well. The exact opposite trend of mobility change by same kind of stress in n-MOSFET and p-MOSFET suggests that the possible origin as conduction band edge lowering with stress.

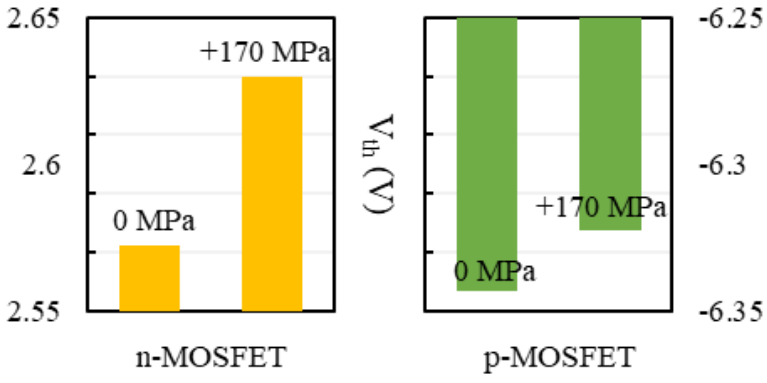

Figure 5.17 V_{th} change with stress of 170 MPa on n-MOSFET (left) and p-MOSFET (right), in the series A device of T_{ox}=38.3 nm.

We also measured V_{th} change on p-MOSFET. The V_{th} change with stress on n-MOSFET and p-MOSFET, derived by channel capacitance measurement [13][90], is compared in **Fig. 5.17**. A positive change of V_{th} change was observed on both devices, despite the difference in amount of change which is likely due to different carrier concentration in p-well and in n-type epitaxial layer. This result confirms that the trend of V_{th} change with stress is not related with substrate type and should be mainly attributed to fixed oxide charges change.

5.5 Estimation of Process-Induced Stress via Raman Spectroscopy

Raman spectroscopy was reported to be a very useful and direct method to determine stress distribution in SiC power devices [91][92][93]. Significant change in frequency can expected to be around 1.0 cm^{-1} in E_2 peak with uniaxial stress of 320 MPa [11].

The Raman spectroscopy system available for this research was with minimum frequency step of 0.4 cm^{-1} which was decided by limited number of gratings. We made an attempt in decreasing minimum frequency step down to 0.1 cm^{-1} by scanning for four times, with the scan starting from frequency at x cm^{-1}, (x+0.1) cm^{-1}, (x+0.2) cm^{-1} and (x+0.3) cm^{-1}, respectively. There were two methods to take estimate peak frequency: a simpler one is to take linear average of peak frequencies from four scans directly; the other one is to first do parabolic approximation of three or four datapoints with highest intensity, then take linear average of symmetry frequency in each approximation.

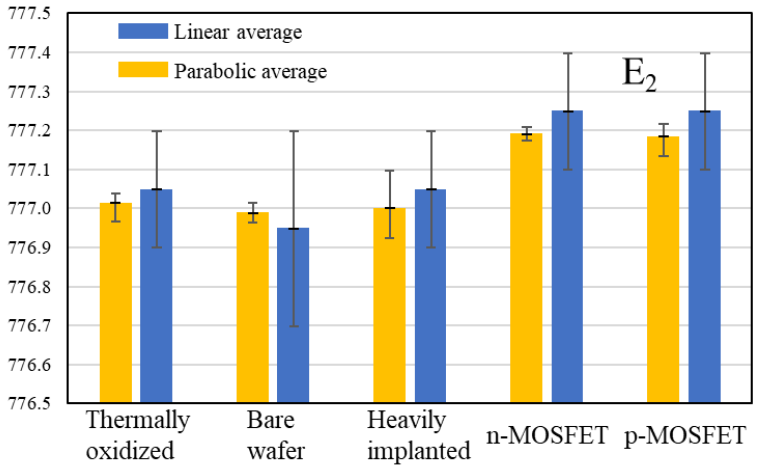

Figure 5.18 Estimated E_2 peak Raman frequencies by linear average method (blue bar) or by parabolic average method (yellow bar).

We selected five 4H-SiC (1000) based wafer to apply Raman spectroscopy and the above peak frequency estimation methods on: 1) thermally oxidized with thickness of over 100 nm, 2) bare wafer as purchased, 3) heavily implanted with doping concentration around 10^{18} cm^{-3}, 4) n-MOSFET and 5) p-MOSFET. The estimated E_2 peak frequencies were presented in **Fig. 5.18**.

It's clearly observed in error bars that, with comparable frequencies, the parabolic average estimation method suppressed error by a lot. Nevertheless, both estimations showed around +0.2 cm^{-1} difference between MOSFETs and other wafers, which suggested existence of compressive stress of around 60 MPa [11]. Since we can exclude oxidation process and implantation process from possible origin of such stress, the most possible origin would be other MOSFET fabrication process including nitridation. Much larger compressive strain was reported on nitridated SiC surface before [94] hence we consider the stress value we observed to be normal phenomenon.

With results above, we may expect common existence of process-induced stress within MOSFET which can induce threshold voltage change of as much as -15 mV.

5.6 Summary

We observed change of electron barrier height with stress via extracting F-N tunneling current under room temperature. By plotting V_{fb} change with stress in relationship to oxide thickness, we found that fixed oxide charges change with stress is the major cause of V_{fb} change with stress. The dipole layer also changed with stress. The impact of stress on fixed oxide charges and dipole are affected by species of oxide. The origin of mobility change with stress could be conduction band edge lowering.

Chapter 6

Conclusions

For the perspective of process' impact on 4H-SiC MOS capacitor, we found that the m-face was more reactive to O_2 than Si-face. This is not only indicated by much faster thermal oxidation rate, but also proved by the induction of oxide traps during H_2O+O_2 annealing process with various pO_2. High pO_2 was detrimental for interface and oxide quality, while annealing with suppressed pO_2 helped to reduce D_{it}. It was also noticed that though it's inevitable to induce V_{fb} instability and first-sweep effect by H_2O-annealing, suppression of pO_2 in annealing ambient can help controlling the instability and first-sweep effect at certain degree. In addition, as the regrowth is within 1 nm, the absolute value of V_{fb} is also decided by pO_2. Above results showed that on m-face, interface traps, oxide traps, oxide mobile charges and oxide fixed charges were all affected by pO_2 in H_2O-annealing ambient.

For the perspective of mechanical stress' impact on 4H-SiC MOSFET, we reported on variation of field-effect mobility with stress. We also observed anomalous change in V_{th} at around 40 mV with stress of 170 MPa and compared V_{th} change with V_{fb} change to prove that the anomalous V_{th} change with stress was

mainly attributed to change in V_{fb}. We suggested that change in band alignment change and change in fixed charge density are possible origins of V_{fb} change with stress.

To investigate the origin of mechanical stress-induced device performance change, first we observed change of electron barrier height with stress via extracting F-N tunneling current under room temperature. By plotting V_{fb} change with stress in relationship to oxide thickness, we found that fixed oxide charges change with stress is the major cause of V_{fb} change with stress. The dipole layer also changed with stress. The origin of mobility change with stress could be energy band lowering.

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Publications

A. **Original papers for the journal with peer review**

1) **Q. Chu**, M. Noborio, S. Shimizu and K. Kita, "Influences of Coexisting O_2 in H_2O-annealing Ambient on Thermal Oxidation Kinetics and MOS Interface Properties on 4H-SiC (1-100)", *Mater. Sci. Semicond.* **116**, 105147 (2020).

2) **Q. Chu**, M. Masunaga, A. Shima and K. Kita, "Comparative Study of Mechanical Stress-Induced Flat-Band Voltage Change in MOS Capacitor and Threshold Voltage Change in MOSFET Fabricated on 4H-SiC (0001)", *Jpn. J. Appl. Phys*, to be published.

3) **Q. Chu**, M. Masunaga, A. Shima and K. Kita, "Mechanism of Mechanical Stress-Induced Flat-Band Voltage Change in 4H-SiC MOS Structure", in preparation.

B. **Proceedings for the international conferences with peer review**

1) **Q. Chu**, M. Noborio, S. Shimizu and K. Kita, "Influences of Coexisting O_2 in H_2O-annealing Ambient on Thermal Oxidation Kinetics and MOS Interface Properties on 4H-SiC (1-100)", 8th International Symposium on Control of Semiconductor Interfaces (ISCSI-VIII), FA1-3 (November 2019, Tohoku University, Sendai, Japan).

2) **Q. Chu**, M. Masunaga, A. Shima and K. Kita, "Anomalous Impact of Mechanical Uniaxial Stress on Threshold Voltage of 4H-SiC (0001) MOSFET", 2023 International Conference on Solid State Devices and Materials (SSDM 2023), N-5-03 (September 2023, Nagoya Congress Center, Nagoya, Japan).

3) **Q. Chu**, M. Masunaga, A. Shima and K. Kita, "Possible Origins of Mechanical Stress-Induced Anomalous Impact on Threshold Voltage of 4H-SiC (0001) MOSFET", 2023 International Workshop on Dielectric Thin Films for Future Electron Devices (2023 IWDTF), S6-6 (October 2023, Kanazawa Chamber of Commerce and Industry, Ishikawa, Japan).

C. **Proceedings for the domestic conferences with peer review**

1) **Q. Chu**, M. Masunaga, A. Shima and K. Kita, "Mechanism of Mechanical Stress-Induced Flat-Band Voltage Change in 4H-SiC MOS Structure", 2024 JSAP Spring Meeting (March 2024, Tokyo).

Award

- **Young Award**

  2023 International Workshop on Dielectric Thin Films for Future Electron Devices (2023 IWDTF), S6-6 (October 2023, Ishikawa, Japan).

Acknowledgment

It has been a fascinating journey for me to spend the years in doctoral program. Due to pandemic, it has taken some while longer to complete than I supposed to, yet it may take forever if not because of warm help from many people.

First of all, I would like to express my sincere appreciation to my supervisor, Prof. Koji Kita, for his continuing support and encouragement through our researches. I would like to thank him for giving me the opportunity to work with him, and for his patience, enthusiasm, and immense knowledge. With his helpful guidance, I was able to adventure in attractive researches and finish thesis and journal papers.

I would like to thank my doctoral dissertation committee members, Prof. Ken Uchida, Prof. Kosuke Nagashio, Prof. Takashi Kondo and Dr. Mitsuru Sometani, for their precious time and valuable comments for my doctoral research.

I would like to thank Prof. Ken Uchida, Prof. Kosuke Nagashio and Dr. Tomonori Nishimura for allowing me to use the facilities and tools in their lab, especially for the 4-points wafer bending tool and Raman Spectroscopy system.

I would like to express my appreciation to members in Kita Research Group for the help and kindness I have received ever since joined.

I would like to thank Dr. Masahiro Masunaga and Dr. Akio Shima of Hitachi R&D Group for their support and helpful discussion for the research, especially for the MOSFETs studies.

I would like to thank Dr. Sumera Shimizu and Dr. Masato Noborio of DENSO corporation for their helpful discussion and comments for this study, especially for the research about m-face of 4H SiC.

I would like to give my sincere thanks to my families and friends in China, for their financial and mental support of my study life in Japan.