Master Thesis

Sensitivity of CMOS Image sensor and Scaling

CMOSイメージセンサの感度特性と評価

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Abstract

This thesis focuses on the sensitivity characteristics of CMOS image sensors and scaling trends. We address the sensitivity characteristics of CMOS image sensor in advanced processes. Sensitivity characteristics, espacially spectral sensitivity and quantum efficiency, is measured. We scaled the sensitivity trends in advanced processes, also.

In this paper, we show the sensitivity of CMOS image sensor using standard CMOS 0.35μm, 0.6μm, 90nm process technologies. Particularly, the spectral sensitivity and the quantum efficiency are measured. The spectral sensitivity exhibits the relation between the radiant sensitivity and the wave length of the incident light. The quantum efficiency chracterizes the transformation of the incident light on the photodiode sensor into electrical charges. These sensitivity characteristics represent the performance of an image sensor using a standard CMOS process technology.

We scaled the trends of sensitivity with advanced processes, also. The sensitivity characteristic of below a 90nm CMOS process technology is scaled by the relationship between the process technology generation and the junction depth.

In advanced process, CMOS process technology is hardly use only for image sensor. However, recognization of sensitivity characteristics of image sensor in advanced processes is helpful for technical chip, not for just image sensor. We can also show the roadmap for optimum pixel configuration of image sensor with downscaled processes by modeling the trends of sensitivity.

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Chapter 1

Introduction

1.1 Background

Recently, complementary metal-oxide-semiconductor(CMOS) based imagers offer significant advantages over charge-coupled devices(CCDs) such as low voltage, low power consumption, and lower cost. The prediction of market stream of CCD/CMOS cameras is shown in the fig. 1.1 [1]. At this time of CMOS technology's rapid downscale, small pixel size, low dark current, high fill factor, and low noise are required for high-resolution imagers [3, 6]. While 0.18μm, 0.35μm, 0.6μm CMOS technologies are mainly used for designing image sensors recently, 90nm or 65nm CMOS technologies will be used. Change of technologies causes to change of size of readout circuit and photodiode. Accordingly, sensitivity characteristics will be changed. For designing a high performance image sensor, we need to model sensitivity characteristics with a standard CMOS process technology's downscaling.

Sensor's characteristics have an effect on performance characteristics, as well. However, organized data of sensitivity characteristics is not disclosed in general. Moreover, a standard CMOS process technology is not for only image sensor [8]. Accordingly, there is only a limited choice of photodetector devices in the standard CMOS process. If characteristics of CMOS image sensor were disregarded, the sensor could be fabricated by general-LSI process. Therefore, researchers, also students, can design a high performance image sensor using a standard CMOS process technology at a low price and, easily.

1.2 Previous researches

Various studies are performed for analysis for sensitivity characteristics. However, studies for image sensors using a standard CMOS process technology is not performed. Studies for

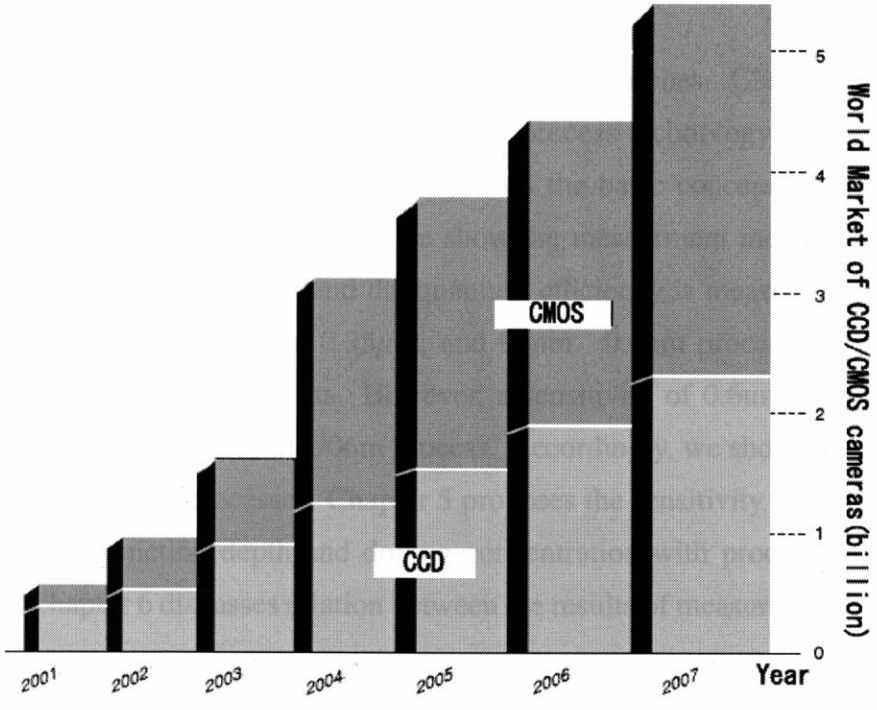

Figure 1.1 Prediction of Market of CCD/CMOS cameras.

the CMOS technology's downscaling is not performed , as well. For instance, an analysis of the shape of photodiode effect on CMOS active pixel sensor(APS) sensitivity was performed [4, 5, 6]. This group's work is mainly photoresponse analysis for pixel shape optimization. In particular, optimum pixel area and pixel perimeter are proposed through experiment of CMOS image sensor using a standard CMOS 0.5μm, 0,35μm process technology. However, this experiment results cannot apply to the other technologies. In [7], sensitivity of CMOS image sensor with different pixel circuits which have a standard photodiode, pinned photodiode, and photodate is estimated. The three-dimensional (3-D) integration for light sensitivie detector, another architectures to improve sensitivty, also estimated. However, a standard CMOS process technology cannot make modificated pixel configuration such as a pinned photodiode and a photogate, a 3D integration architecture, also. In [11], quantum efficiency of CMOS image sensor is measured by test structure. This study represents quantum efficiency for different kinds of Nwell/Pepi diode. The impact of the design (different Nwell geometries) and two reading nodes(CMOS and NMOS) are also studied. However, CMOS process technology used measurement is not disclosed. Eventually, these research didn't showe the estimation about the change of sensitivity from a standard CMOS process technology's downscaling.

1.3 Organization of Thesis

In this chapter, we explained background and previous researches. Chapter 2 shows the advantages of image sensor using a standard CMOS process technology. We explain the detailed target of this research, also. Chapter 3 shows the basic concept of image sensor and sensitivity characteristics. In chapter 4, we show the measurment methods and results of sensitivity. The spectral sensitivity and the quantum efficiency is measured, mainly. We use 3 process technologies of 0.6μm, 0.35μm, and 90nm. 0.6um process technology for Image sensor is an old-fasioned process. However, a sensitivity of 0.6um image sensor is compared with front-process, 0.35μm, 90nm process. Accordingly, we show the roadmap of sensitivity with downscaling processes. Chapter 5 proposes the sensitivity trends by scaling. Relationship between junction depth and doping concentration with process generation is used for scaling. Chapter 6 discusses relation between the results of measurement and scaling trends.

Chapter 2

Prospect of CMOS based imagers

2.1 Advantages of CMOS based imagers

What is the main advantage of image sensors using a standard CMOS process technology? The real advantage of CMOS imager is the high level of on-chip logic, memory, and signal processing function integration, and random access capability, which cannot be easily accomplished by the CCD. In the near-past, there is a proliferation of activity to modify baseline processes to optimize cost-performanxe as well as to integrate traditionally "seperate" functions on the same chip to build what has been called "system-on-a-chip"(SOC). For requirement of high-performance, CMOS image sensors are changed, however. For instance, one-pixel can have not only source follower as a readout part, but also ADC or the other functional circuit [2]. This group suggests that the image pixel circuit including column sense amplifier circuit and comparator/latch pair in fig. 2.1.

The challenge to the CMOS imager community is to determine where the cost-performance trade-offs are, how far CMOS technology has to be modified to accommodate the imaging function, and to use imaging-specific technologies judiciously without compromising its capability for system integration. Conventional CCD product differentiation is mostly found at the device and process design level. For CMOS imagers, product differentiation will increasingly be found in the circuit design, chip architecture, and system integration.

As a result, CMOS imagers is not just imagers. They have many performances with imaging function.

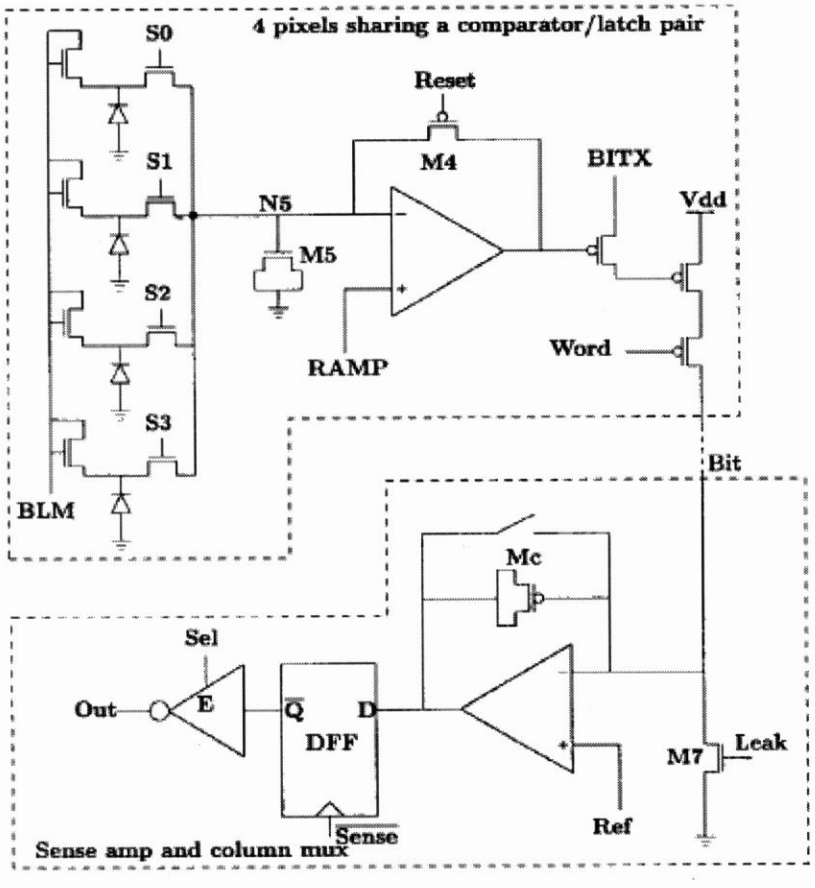

Figure 2.1 Example of CMOS image senor's pixel block and column sense amplifier circuit

2.2 CMOS Image sensors in Deep sub-micron technology

CMOS technology has been downscaled in deep sub-micron technology in past years. Downscaled technologies cause to a small pixel size in fig. 2.2. As CMOS technologies evolve at the unabated pace of 0.7x of the minimum feature size, certain important device characteristics do change as the technology us scaled. While the industry standard CMOS technology has been developed to optimize the power-delay, reliability, and cost-performance of logic and memory circuits, some device characteristics that are germane to the imaging application have not benn addressed as the technology evolves; and it is not so clear that CMOS imagers will continue to benefit from device scaling.

Pixel Size

The scaling of the CMOS imager pixel size is shown in Table. 2.1. The pixel size as a function of the minimum feature size reported by various researchers is plotted in fig. 2.2.

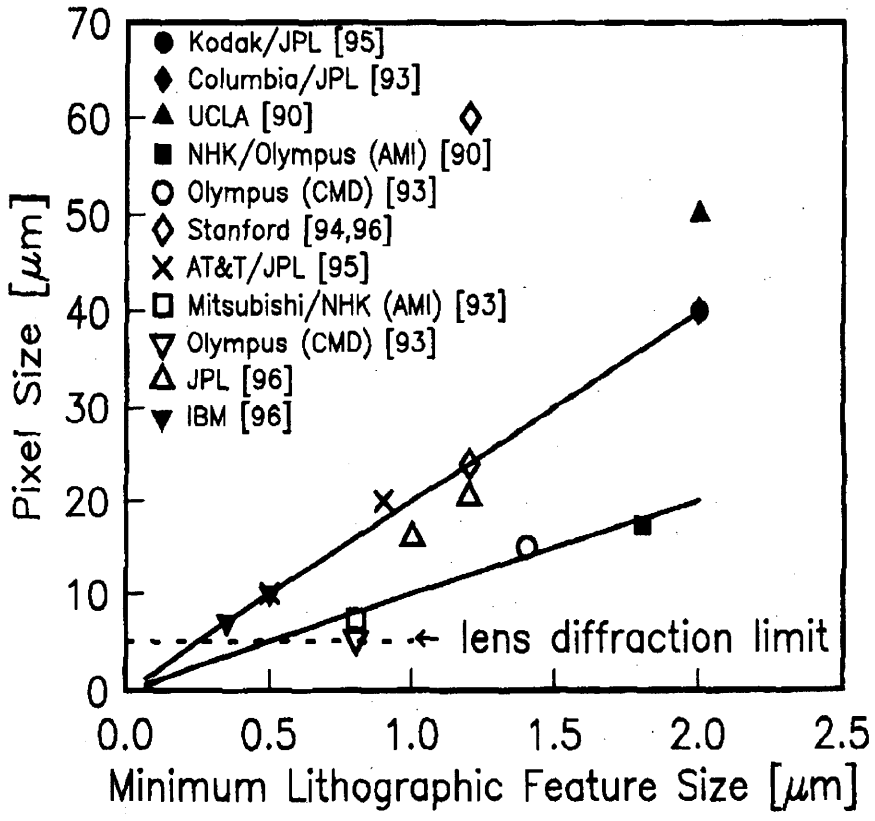

Figure 2.2 Scaling trend of CMOS imager pixel size. Symbols are experimental data reported in the lietrature. The line represents linear scaling. The upper solid shows pixel size scaling as $20Lg$(typical of 4-transistor photodate designs), the lower solid line shows pixel size scaling as $16Lg$(typical of 3-transistor photodiode designs), Lg is the minimum lithographic feature size.[16]

The trend basically follows the profections of Table. 2.1. Fig. 2.3 illustrate two layouts using 0.5μm and 0.35μm technology. The pixel size and the photosesitivite fill-factor scale linearly with the minimum feature size. Pixel design cleverness is not expected to provide more than a 50% improvement in pixel size or fill-factor. It has been generally acknowledged that further decrease in the pixel size much beyond 5μm x 5μm is not needed because of the diffraction limit of the camera lens. Therefore, CMOS iamgers will benefit from further scaling after the 0.25μm generation only in terms of increased fill-factor and/ or increased signal processing functionality within a pixel[16].

Sensitivity

The spectral sensitivity of the MOS photogate and the pn junction of the photodiode are largely determined by the gate electrode and junction materials and technologies, respec-

Table 2.1 Principal Wafer Fabrication Characteristics. The Information is adapted from the SIA Roadmap and Various CMOS logic technologies across the industry[16]

Minimum lithographic feature size (0.7x/generation)	2	0.7	0.18	0.13	0.1	0.07
CMOS imager pixel size (0.7x/generation) [$x\mu m x x \mu m$]	40	14	5(3.5)	5(2.45)	5(1.72)	5(1.2)
CMOS imager fill facter [%]	25	25	53(25)	82(25)	91(25)	96(25)

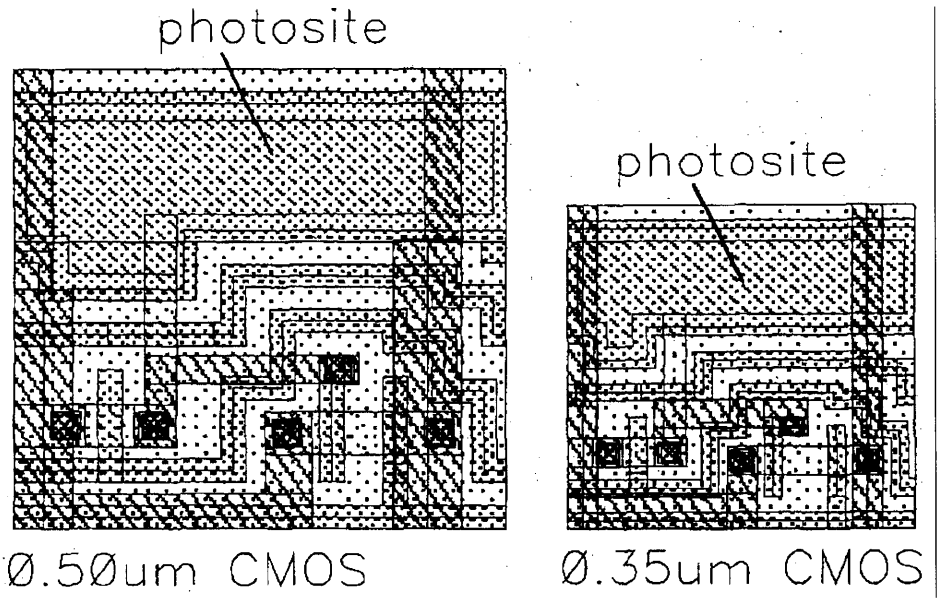

Figure 2.3 Example layout for a 0.5μm technology (10μm pixel) and 0.35μm technology (7μm pixel).

tively. From [23], substrate doping concentration is larger, and source/drain junction depth is thiner according to downscaling technology. Therefore, sensitivity of CMOS image sensors get worse with downscaling technology. (The concept of sensitivity of CMOS image sensor explained next chapter.)

2.3 Purpose of our research

As the mentioned above, image sensors fabricated by CMOS process technologies have benefit and non-benefit in downscaled technologies. For high performance CMOS image sensors, we aim to measure the sensitivity characteristics in real world, not predict that from parameters. We used ,for measurment, CMOS image sensors fabricated by standard CMOS 90nm, 0.35μm, 0.6μm process technolgies, which we can use for designing image sensor now. We aim to scale the sensitivitiy chatacteristics of CMOS image sensor in advanced

process which we cannot use for designing at now. For designing the high-performance image sensor, our research will be stem of that. We aim to suggest the way for the optimum readout circuit or the same level circumstanse for high sensitive and high performance CMOS image sensor.

Chapter 3

Sensitivity of CMOS Image Sensor

3.1 Concept of CMOS image sensor

This section introduces the basic concept, pixel configuration and operation, of CMOS image sensor, used for measurement [12]. Also, the principle of sensitivity of CMOS image sensor will be introduced.

3.1.1 Pixel Configuration

The basic CMOS image sensor, as known as an active pixel sensor (APS), employs a photodiode as a photodetector and a readout circuit of three transistors: a photodiode reset transistor (*RSTi*), a row select transistor(*SELi*), and a source-follower transistor. The scheme of this pixel configuration is shown in Fig. 3.1(a). This pixel configuration is used image sensors measured for sensitivity. This pixel readout circuit is the typical configuration among the image sensors having a photodiode.

3.1.2 Pixel Operation

In this CMOS image sensor, the pixel area in constructed of two functional parts. The first part, which has a certain geometrical shape, is the sensing element itself: the active area that the illumination energy within it and turns that energy into charge carriers. This part impacts on sensitivity characteristics. The second part is the control circuitry required for readout of this charge. Pixel operation is described in fig. 3.1(b). A photodiode reset transistor (*RSTi*) is on for preparing readout. For integration time, electrons are generated by photons. If a select transistor(*SELi*) is on, photocarriers are read out through output signal(*VALj*).

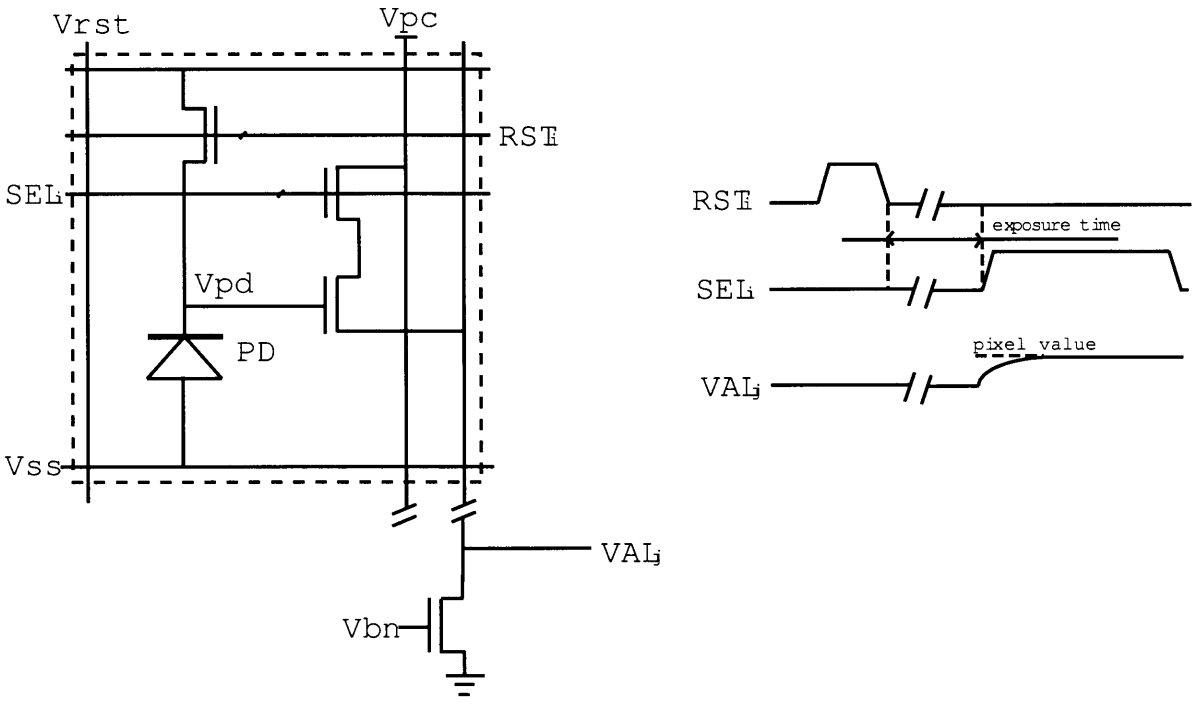

Figure 3.1 Pixel Circuit and Readout operation[12]

3.2 Sensitivity characteristics

This section introduces the main sensitivity characteristics of image sensor [11].

Spectral Sensitivity

The spectral sensitivity exhibits the relation between the radiant sensitivity and the wave length of the incident light. For example, the spectral sensitivity of a pinnned photodiode imagers is shown in fig. 3.2 [7].

In front of the explaining of the spectral sensitivity, the concept of photoelectric transformation is introduced.

The photoelectric transformation, one of the principle of readout operation, means that electrons are generated by incident photon. In other words, states of electrons, changed by taking a photon energy could be free by putting the electric field. This photoelectric transformation has two types: the external and the internal photoelectric effect. The external photoelectric effect exhibits emitting of outside of solid-state electrons by photon energy. This external photoelectric effect is shown in fig. 3.3(a). At this time, work function correspond to difference between valence band and vaccum state is necessary. In the other side, the internal photoelectric effect, shown in fig. 3.3(b), describes that electrons with low energy among

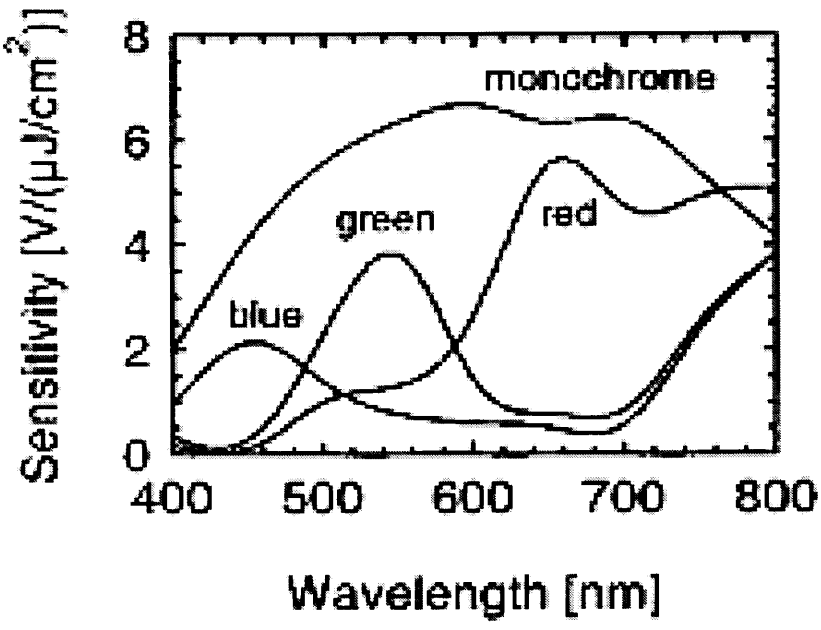

Figure 3.2 Monochrome and color sensitivity of a PPD imager[7]

inside of solid-state electrons are raised up by photon energy [9].

During absorption of light in the photodiode, energy of photon turns into energy of electron, as mentioned above. This operation has an effect on the spectral sensitivity. A silicon(Si) single-crystal using for the image sensor absorbs gradually the incident light. This operation showed in fig. 3.4. The incident light in Si single-crystal moves onward x vertical axis by zero of a substrate surface. I and x indicate light intensity and depth from silicon substrate, respectively. Besides, dx and dI describe the distance of a light and changed the light intensity. dI would be proportioned to dx and I. The formula is

$$dI = -\alpha \, \mathrm{I} \, \mathrm{dX} \tag{3.1}$$

where α is an absorption coefficient. An absorption coefficient with a photon energy, which is oppsition to wave length, shows in fig. 3.5. This equation could be changed as below,

$$I = I_0 \, e^{-\alpha x}. \tag{3.2}$$

This equation describes that the distribution of a light intensity(I) is showed by an exponential function. We recognize also that a high α value means the absorbtion in near device surface and a low α means deep absorption from eq. 3.2 and fig. 3.5.

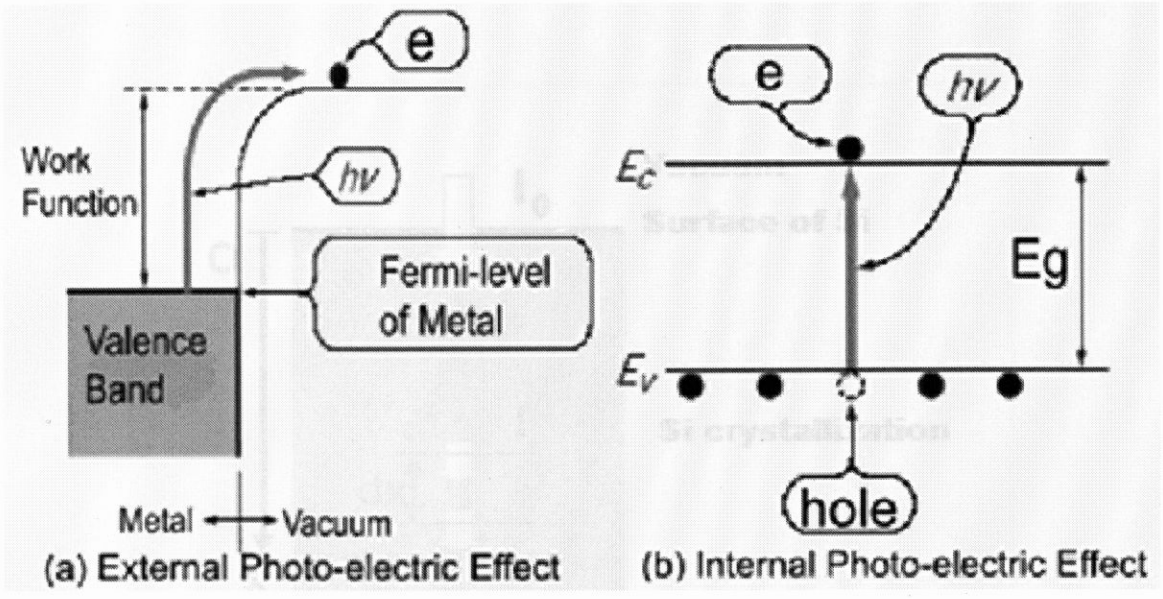

Figure 3.3 Photoelectric Effect

Red light, with wavelength, $\lambda \sim 0.6\ \mu$m for instance, has a relatively small absorption coefficient, which means more of the photocarriers can be generated outside the depletion region(p-type substrate in our case). These carriers diffuse to the original imaging site or th a nearby site where they are collected, before they are lost to the bulk recombination process. The imagers lose resolution as the result of this diffusion process.

Besides, blue photons, with wavelength $\lambda \sim 0.4\ \mu$m, tend to be absorbed near the device surface. Image sensors having typicel photodiode and pixel circuit, used measurement, have better sensitivity in the short wave length than in long wave length from eq. 3.2. However, a very short wavelength, 400nm, has the worse sensitivity because of a film for protection Si surface in real world. Moreover, the high doping density in this region strongly reduces the carrier lifetime such that most of the minority carriers recombine immediately, causing, therefore, low photodiode sensitivity for a short wavelengths illumination.

As a results, the architecture of photodiode rely on the sensitivity following the wave length during this photoelectric transformation. The depth of photodiode has a great effect on the spectral sensitivity, especially a long wavelength, as well.

Quantum Efficiency

The Quantum Efficiency(Q.E.) characterizes the transformation of the incident light on the photodiode sensor into electrical charges. For instance, Q.E. of CCD imagers is shown in fig.

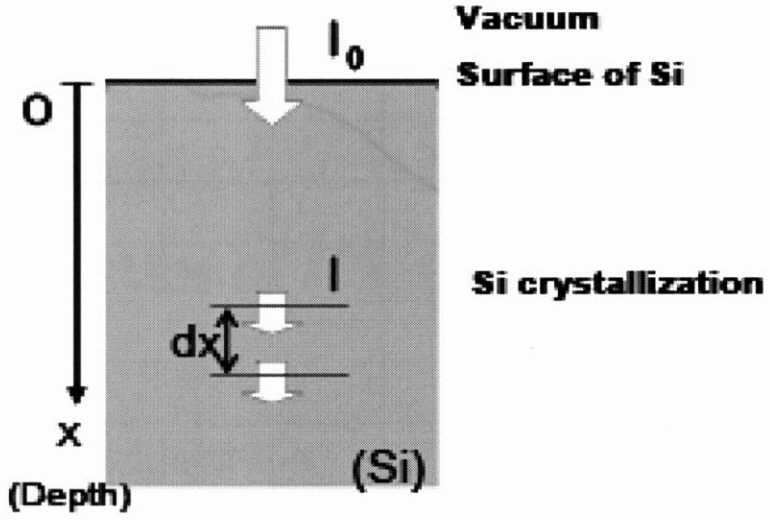

Figure 3.4 State of light absorbtion

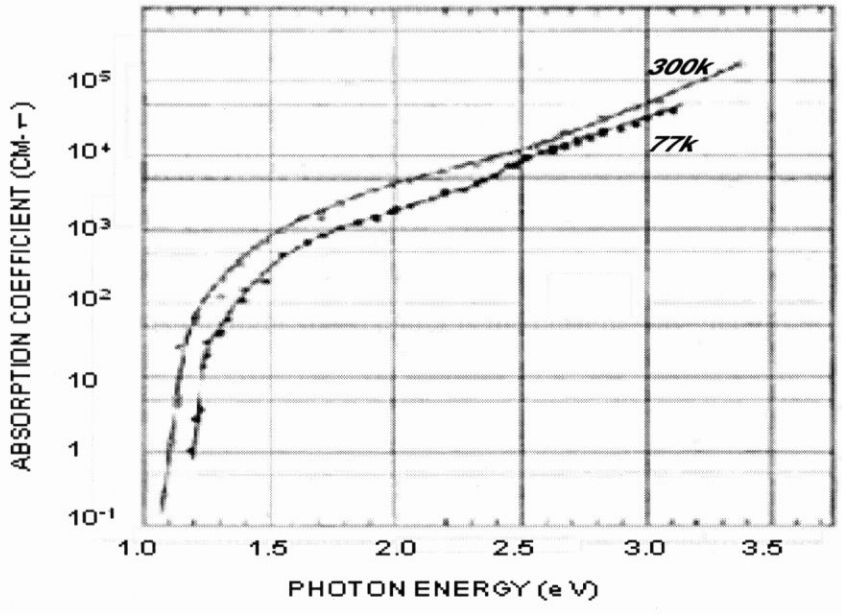

Figure 3.5 Absorption Spectra of single-crystal silicon at 77K and 300K[10]

3.6 [18].

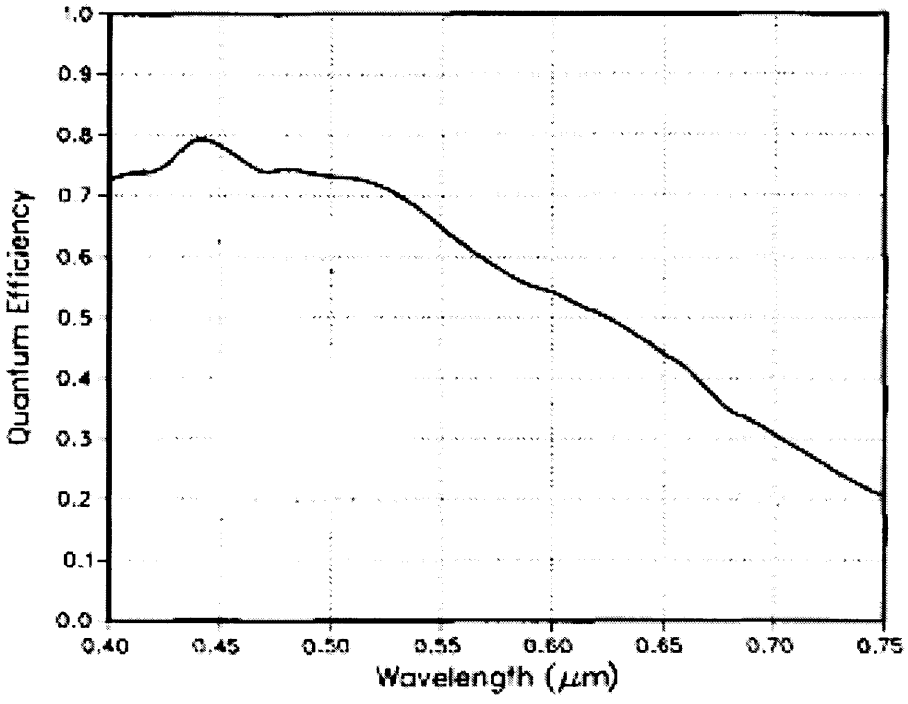

Figure 3.6 Quantum Efficiency of CCD[18]

Q.E. is the ratio of the number of photogenerated electrons captured by a pixel to the number of photons incident upon the pixel during a period of time[11]. Q.E. is expressed in electrons per photon. The number of electron generated in the photodiode is: $\frac{Idiode}{q}$

Where *Idiode* is the current of the diode and Q(1.602E-09q) is the electronic charge. The number of photon hitting the silicon can be expressed as the optical power in watt divided by the energy of one photon: $\frac{P}{\frac{hc}{\lambda}}$

P is the optical power measured by the photo detector, h is Plank constant (6.626E-34m^2Kg/s), c(3E8m/s) is the light speed and λ is the current wave length.

The formula is

$$QE = \frac{Idiode \text{ x} h \text{ x } c}{q\text{x } P \text{ x } \lambda} \text{x}\alpha \tag{3.3}$$

where α is the ratio between the optical power measured on the photo detector and the power actually hitting the sample(about 1).

Chapter 4

Measurement of Sensitivity characteristics of CMOS Image Sensor

4.1 Sensor configuration

We used image sensors using three process technologies, 0.35μm, 0.6μm, 90nm, for measurment. We explain configuration of these sensors in this section.

4.1.1 CMOS image sensor using 0.35μm, 0.6μm process technologies

In fig. 4.1, readout circuit showed[12, 13]. Mentioned above chapter 3.1.1, this pixel has two fuctional parts. The incident light turns into charge carriers in the first part-photodiode area. In the second part, this charge is readouted. Pixel specification is showed in table. 4.1. The ratio between the active area and the total pixel area is referred to as the fill factor(FF), which in an APS is less than 100%.

Table 4.1 Specification

Process	0.35 μm 2P3M CMOS	0.6μm 3M2P
Pixel resolution	1024 X 768 pixels(XGA)	640 X 480 pixels(VGA)
# FETs	3.2M transistors	1.12M transistors
Pixel size	8.4μm X 8.4μm	12μm X 12μm
Pixel configuration	1PD + 3 FETs	1PD + 3 FETs
Fill factor	29.02%	29.54%

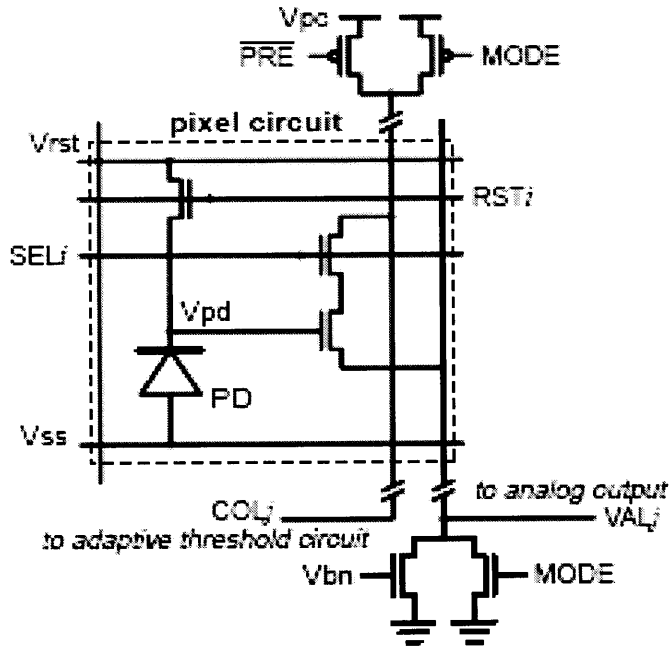

Figure 4.1 Readout Circuit Configuration

4.1.2 Photodiodes using a 90nm process technology

We designed photodiodes of a 90nm process technology. Types of photodiodes show in tab. 4.2.

4.2 Measurement of Spectral Sensitivity

4.2.1 Measurement Set

Spectral sensitivity depends on a detector (photodiode), grating (dispersion), and a light source. Our equipment is shown in fig. 4.2. We make a focus of light source, having a visible spectrum, by pinhole. The light source is 150W halogen lamp (JCR15V150WH5). The relative spectrum intensity of this lamp is shown in fig. 4.4. We used a convex lens and two dispersion equipments for producing a parallel beam of light and dispersing the incident light. For reliable measurement, we used and compared two dispersion eqipments, a prism and a diffraction gratings. For calibration, we use narrow band pass interference filters, LEDs, and laser diodes. we measured the position of three wave lengths using laser diodes and laser pointer whose wave reponse is 532nm, 655nm, and 785nm, respectively. When we calculate the relation between wave length and position, we used the snell's law

Table 4.2 Photodiodes Specification

Type	area(μm X μm)	Type	area (μm X μm)
N-diff/P-Well	1 X 50	N-diff/HVP-Well	1 X 50
N-diff/P-Well	2.5 X 10	N-diff/HVP-Well	2.5 X 10
N-diff/P-Well	5 X 5	N-diff/HVP-Well	5 X 5
N-diff/P-Well	2.5 X 10 (silicide)	N-diff/HVP-Well	2.5 X 10(silicide)
N-diff/P-Well	5 X 5 (silicide)	N-diff/HVP-Well	5 X 5 (silicide)
P-diff/N-Well	1 X 50	P-diff/HVN-Well	1 X 50
P-diff/N-Well	2.5 X 10	P-diff/HVN-Well	2.5 X 10
P-diff/N-Well	5 X 5	P-diff/HVN-Well	5 X 5
P-diff/N-Well	2.5 X 10 (silicide)	P-diff/HVN-Well	2.5 X 10(silicide)
P-diff/N-Well	5 X 5 (silicide)	P-diff/HVN-Well	5 X 5 (silicide)
P-well/Deep-N-Well	2.5 X 10	P-well/Deep-N-Well	5 X 5

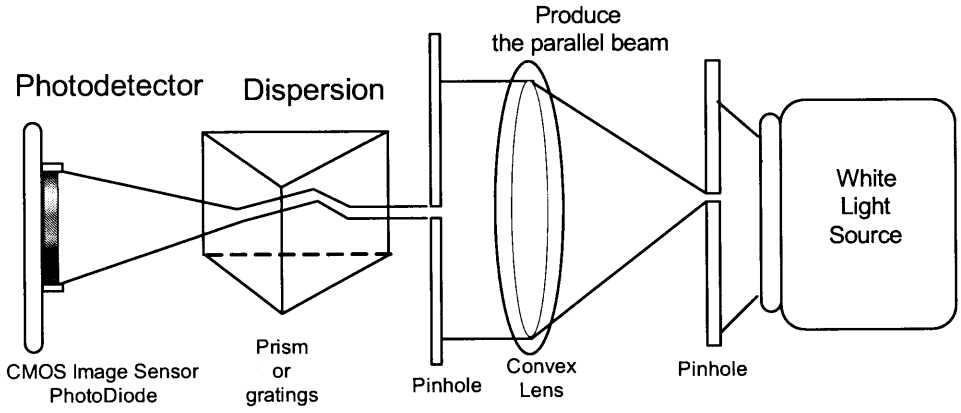

Figure 4.2 Optical system(in the case of a prism)

and the principle of prism and a linear approximation. Narrow band pass interference filters, whose wave reponse is from 400nm to 1064nm at 50nm intervals, used and compared for measurement as the same of a prism and a diffraction gratings for reliable measurement.

4.2.2 Measurement Method

Firstly, we measured the position of three wave lengths using laser diodes. We calibrated the relation between the incident light of light source and position of wave length. Secondly, the spectrum intensity per area of light source is measured. We can measure the light source's photocurrent by photodiode (Hamamatsu, S1087-01, fig. 4.5). The spectral respose range

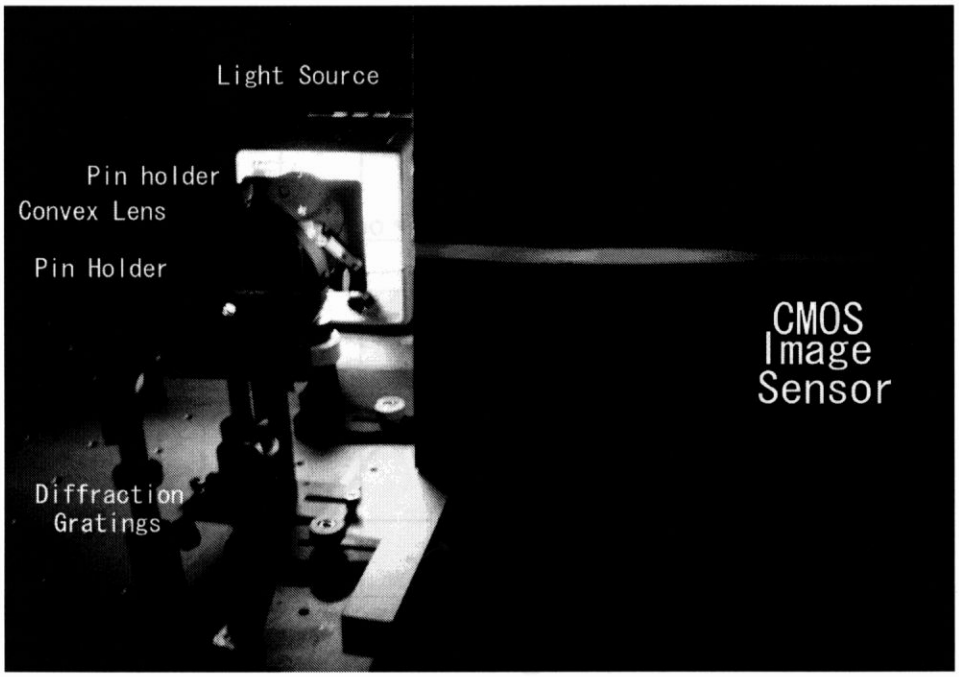

Figure 4.3 Optical system(in the case of a gratings)

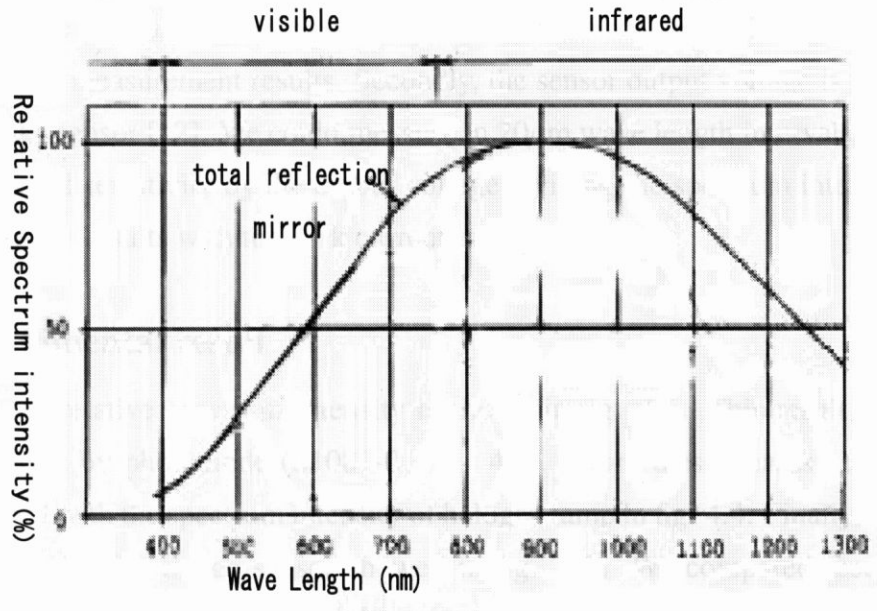

Figure 4.4 Relative Spectrum Intensity of Halogen Lamp JCR15V150WH5

of this photodiode, as a photodetector is 320nm~1100nm. The spectrum intensity which indicates a light power, is calculated by dividing photocurrent and photodiode's sensitivity

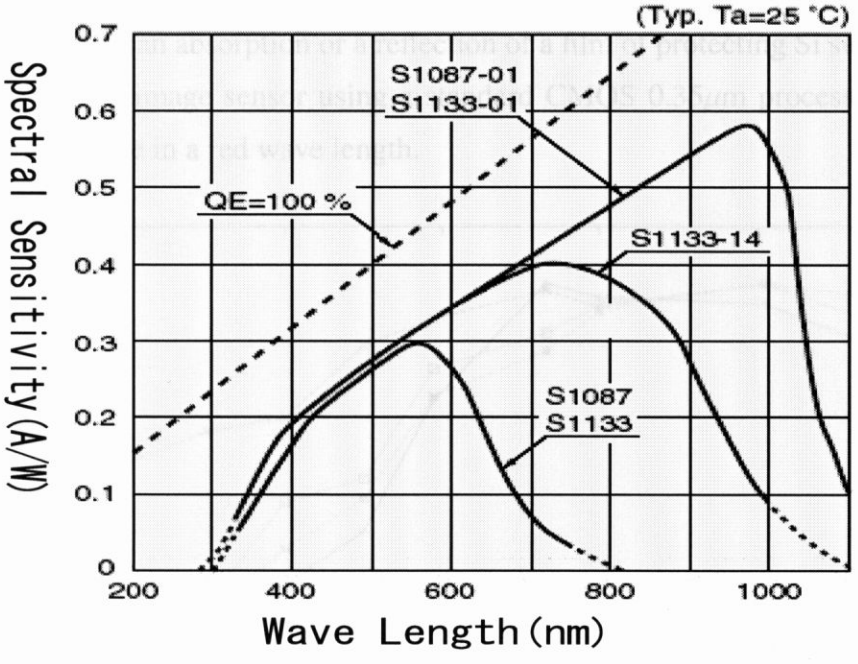

Figure 4.5 Spectral Sensitivity of photodiode(S1087-01)

(A/W). For reliable measurement, we compared the light source's relative spectrum intensity in fig. 4.4 with the measurement results. Secondly, the sensor output voltage is measured by the CMOS image sensor [12]. We could measure in 20μm wave length intervals. Finally, we can get the spectral sensitivity by the output voltage dividing the spectrum intensity. We do doublesampling the results with the dark current in all data.

4.2.3 Experimental result

First of all, the relative spectrum intensity is shown in fig. 4.6. This result is measured the dispersed light by photodiode (S1087-01,fig. 4.5). From these results, detected light intensity matched with the spectrum intensity of halogen lamp in fig. 4.4. Finally, the spectral sensitivity of the CMOS image sensor showed in fig. 4.7. We compared results by two dispersion equipments, a prism and a diffraction gratings. The results using a prism and a diffraction gratings are matched. Maximum of the spectral sensitivity is 2.5 (V/(μm/mm^2)) in the 780nm wave length, both.

This results in long wave length prove the principle commented in section 3.2. However, the spectral sensitivity in a very long wave length decreases drastically, because of an absorption coefficent decreasing rapidlly in this wavelength. Moreover, the spectral sensitivity

in a short wave length is lower than in a long wave length. We could expect that the spectral sensitivity is affected by an absorption or a reflection of a film of protecting Si surface. From this results, the CMOS image sensor using a standard CMOS 0.35μm process technology have a goon performance in a red wave length.

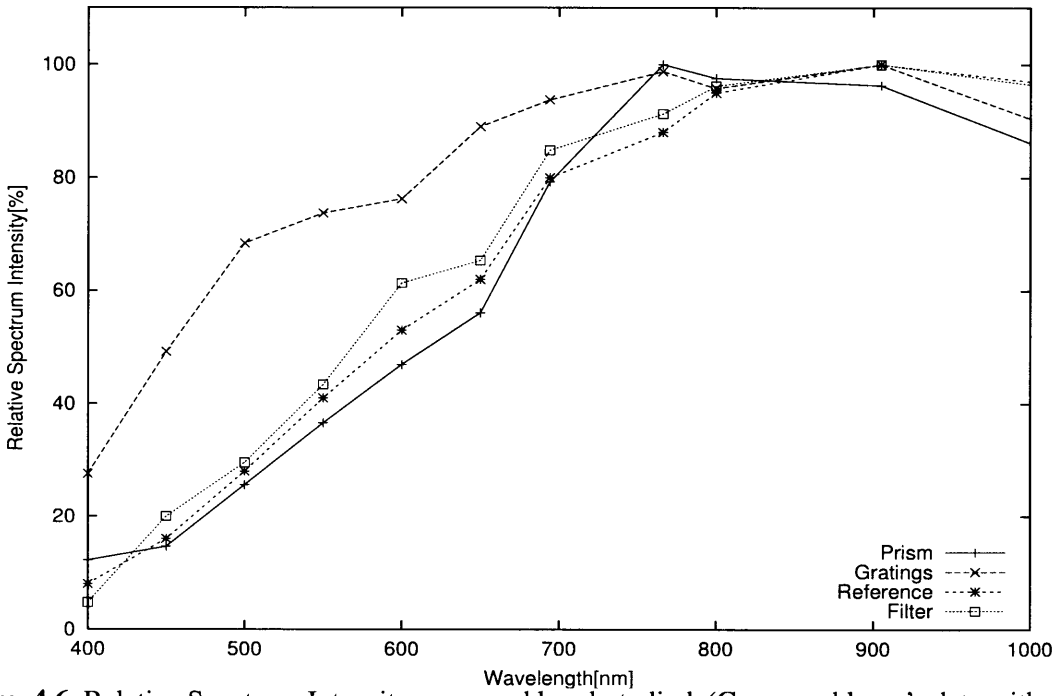

Figure 4.6 Relative Spectrum Intensity measured by photodiode(Compared lamp's data with results using filter and prism)

4.3 Measurement of Quantum Efficiency

4.3.1 Quantum Efficiency of CMOS Image sensors using 0.35μm, 0.6μm process technologies

Measurement set and method

For the estimation of the Quantum Efficiency, we use narrow band pass interference filters as a diversion equipment, which have wave length from 400nm to 1064nm at 50nm intervals. We used the principle as the photocurrent of photodiode could be calculated by the relation between capacitance and voltage. Firstly, the photodiode's capacitance of image sensor is calculated by the simulation of pixel circuit. We use equation for calculation of capacitance [14]. The formula is

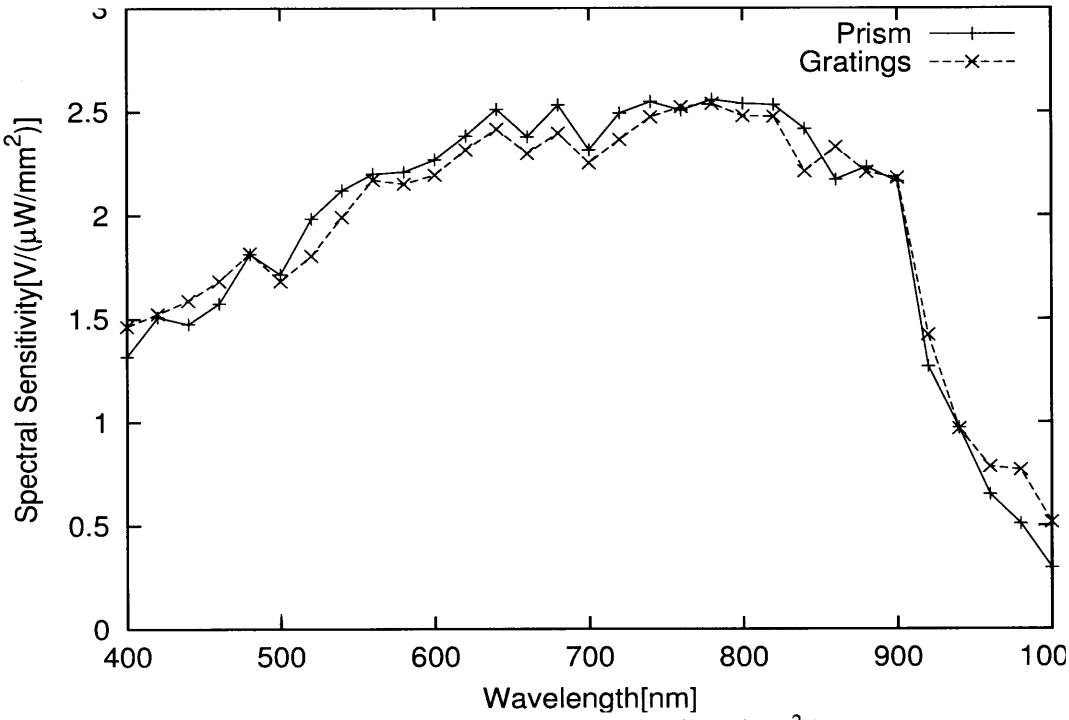

Figure 4.7 Spectral Sensitivity (V/(μW/mm^2))

Table 4.3 Parameters

Parameter	0.35μm process technology	0.6μm process technology
A_{deff}	2.05e-11	4.25e-11
P_{deff}	1.92e-05	2.76e-05
C_{jd}	3.67e-04	5.005e-04
C_{jswd}	1.05e-09	4.14e-14
M_{jd}	3.14e-02	3.46e-01
M_{jswd}	5.12e-01	1.13e-01
P_{bd}	9.66e-02	7.21e-01
P_{jswd}	8.82e-01	5.18e-01

$$C = A_{deff} \times C_{jd} \left(1 + M_{jd} \frac{V_{bd}}{P_{bd}} \right) + P_{deff} \times C_{jswd} \left(1 + M_{jswd} \frac{V_{bd}}{P_{jswd}} \right) \tag{4.1}$$

A_{deff} shows an area of photodiode and P_{deff} shows a length of periphery of photodiode. Parameters are shown in the tab. 4.3, respectively 0.35μm, 0.6μm process technologies.

We calculated the junction capacitances of photodiodes with these parameters and bias voltages from 0 to 5. Results of calculation of relation between bias voltages and capacitance

show in fig. 4.8, fig. 4.9.

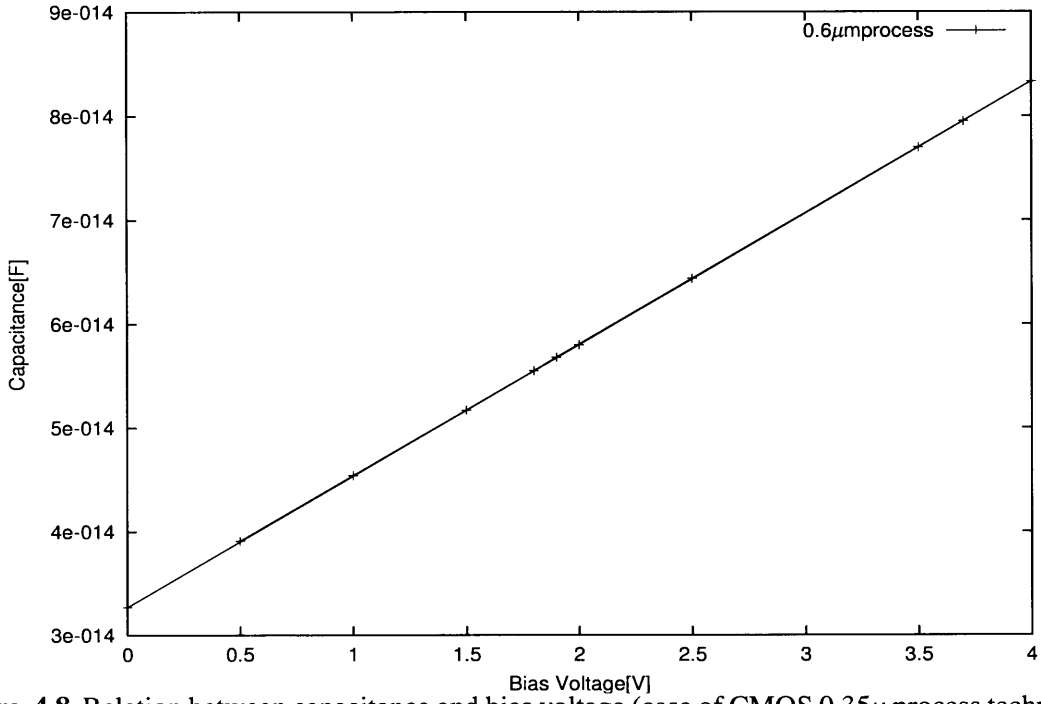

Figure 4.8 Relation between capacitance and bias voltage (case of CMOS 0.35μ process technology)

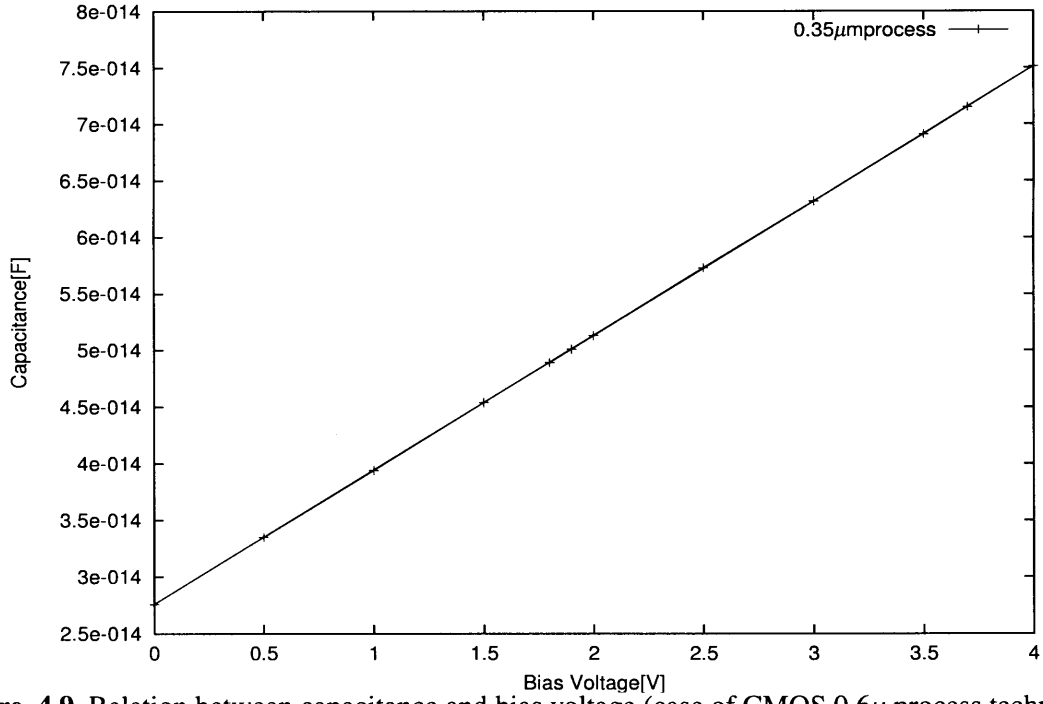

Figure 4.9 Relation between capacitance and bias voltage (case of CMOS 0.6μ process technology)

Secondly, we measured the relation between voltage of *RSTi* and voltage of *VALj* with no

light. Voltage of *VALj* measured with continuous on state of *RSTi* and *SELi* in fig. 4.10(a). Results of relation between voltage of *RSTi* and voltage of *VALj* show in fig. 4.11, and 4.12 ,respectively.

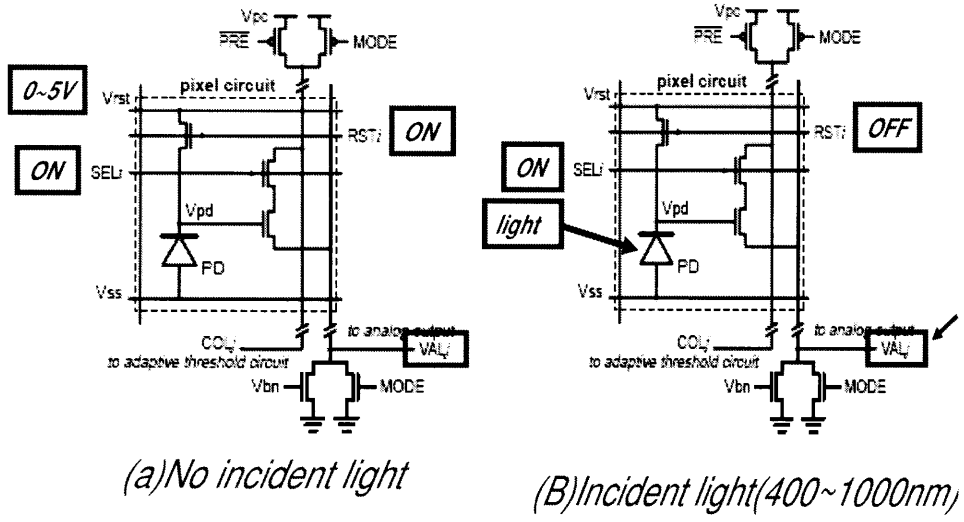

Figure 4.10 Measurement of Vrst and Vval

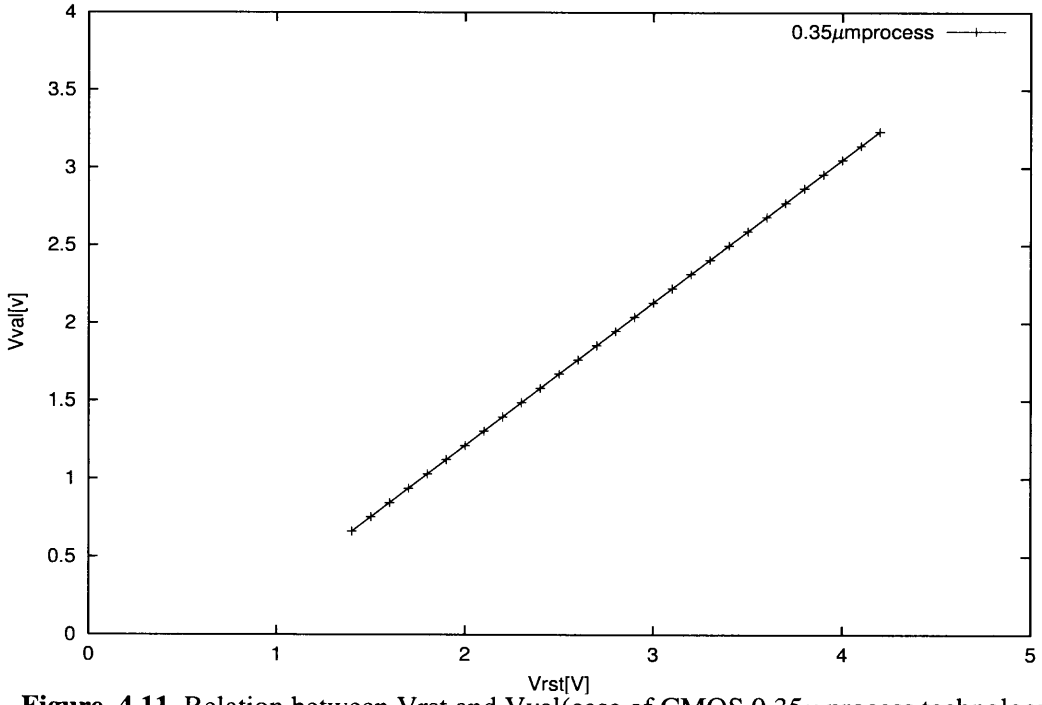

Figure 4.11 Relation between Vrst and Vval(case of CMOS 0.35μ process technology)

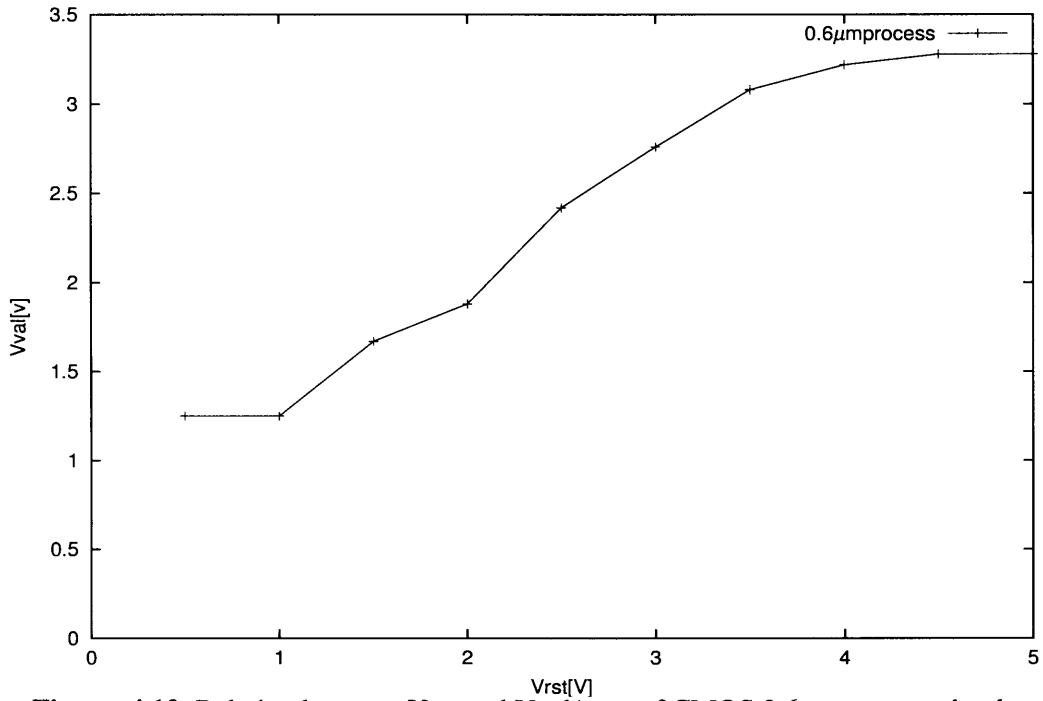

Figure 4.12 Relation between Vrst and Vval(case of CMOS 0.6μ process technology)

Thirdly, voltage of *VALj* with the on-state of *RSTi* in the fig. 4.10(b) is measured. Voltage of *VALj* converts to photodiode voltage from relation between voltage of *RSTi* and voltage of *VALj*.

Forthly, we use the capacitance of photodiode ,mentioned above, to calculate generated carriers. Bias voltage in fig.**??** changes photodiode voltage in this case. We obtain the carriers, Q(F), from integration of photodiode voltage and capacitance. The photocurrent would be calculated by the electrical charge dividing the integration time, nextly. When measurement of 0.35μ process technology, we adapt the integration time per wavelengths. When the maximum value outputed in adaptable time, we use that integration time. Fig. 4.13 shows the integration time having the maximum output, each wavelengths. Variation of Vval means that large variation of Vval is high sensitivity.

Finally, we could get the quantum efficiency from Eq. 4.10, using the photocurrent and the spectrum intensity. This spectrum intensity is the same data in the spectral sensitivity.

Experimental results

The result of the quantum efficiency is shown in fig. 4.14 and fig. 4.15. Max values of quantum efficiency are 0.26(e-/photon) at 450nm wavelength in a 0.35μ process technology and 0.664(e-/photon) at 430nm wavelength in a 0.6μ process technology, respectively.

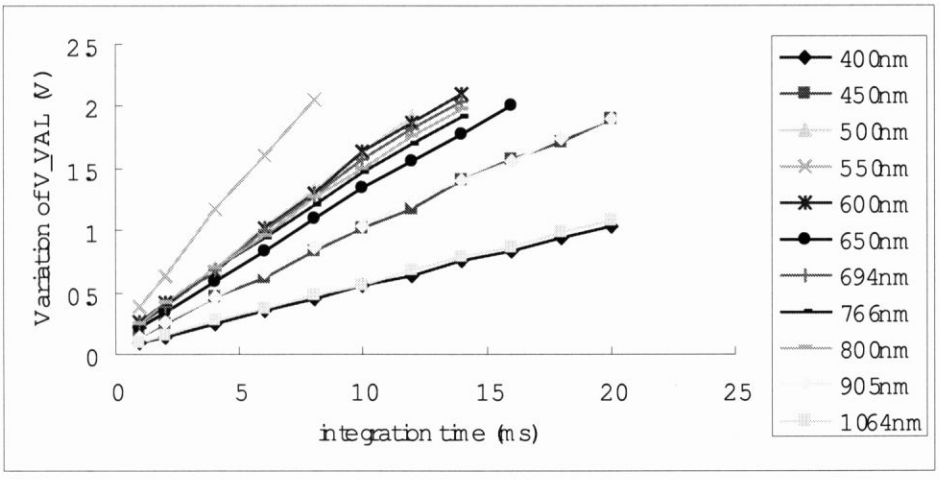

Figure 4.13 Variation of Vval per integration time[*ms*](case of CMOS 0.35μ process technology)

Min values are 0.08(e-/photon) at 1046nm wavelengths in a 0.35μ process technology and 0.158(e-/photon) at 800nm wavelengths in a 0.6μ process technology, respectively. The incident light generates well in short wavelengths by photoelectric conversion operation, as mentioned above.

4.3.2 Quantum Efficiency of photodiodes fabricated by CMOS 90nm process technology

Measurement Set and Method

We measure with the same optical set of different process technologies. We use DC source (HP4142B) for readout the photocurrent of photodiodes, also. We input bias voltage to photodiodes, and we measure the photocurrent 100 times per 1 measurement by HP4142B. These data are averaged for using the estimation of quantum efficiency.

Experimental Results

We failed measurement with all of photodiodes, eventually. We show the result of one case, P-diffusion/high voltage N-well sub, in fig. 4.16. The result of quantum efficiency is too big. We guessed the reason that all of photodiode is affected each other or the junction length is bigger then design size. In the future work, we try again to measure.

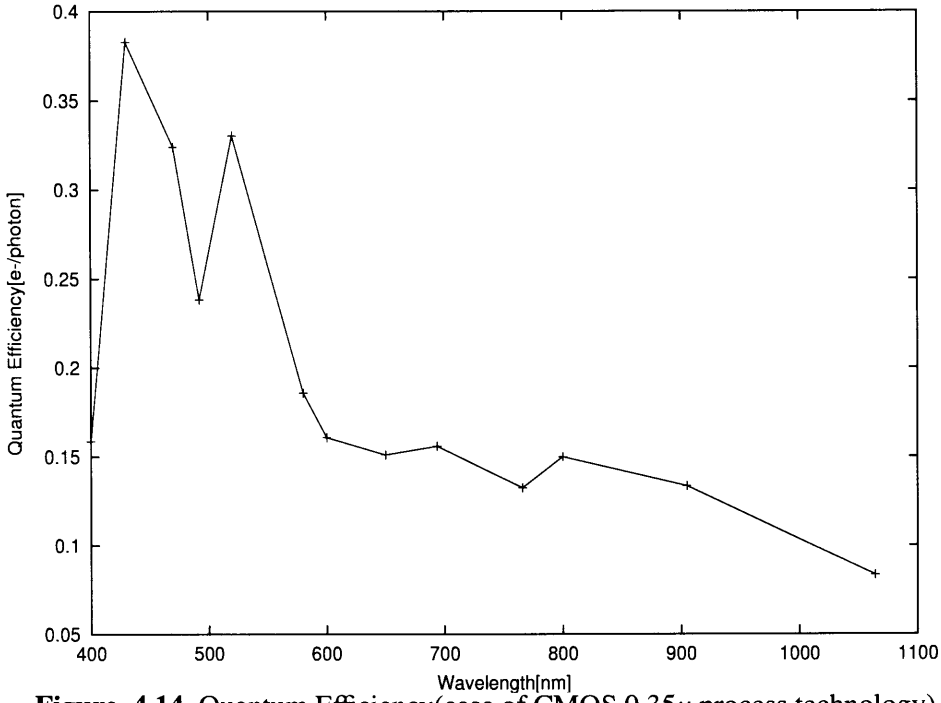

Figure 4.14 Quantum Efficiency(case of CMOS 0.35μ process technology)

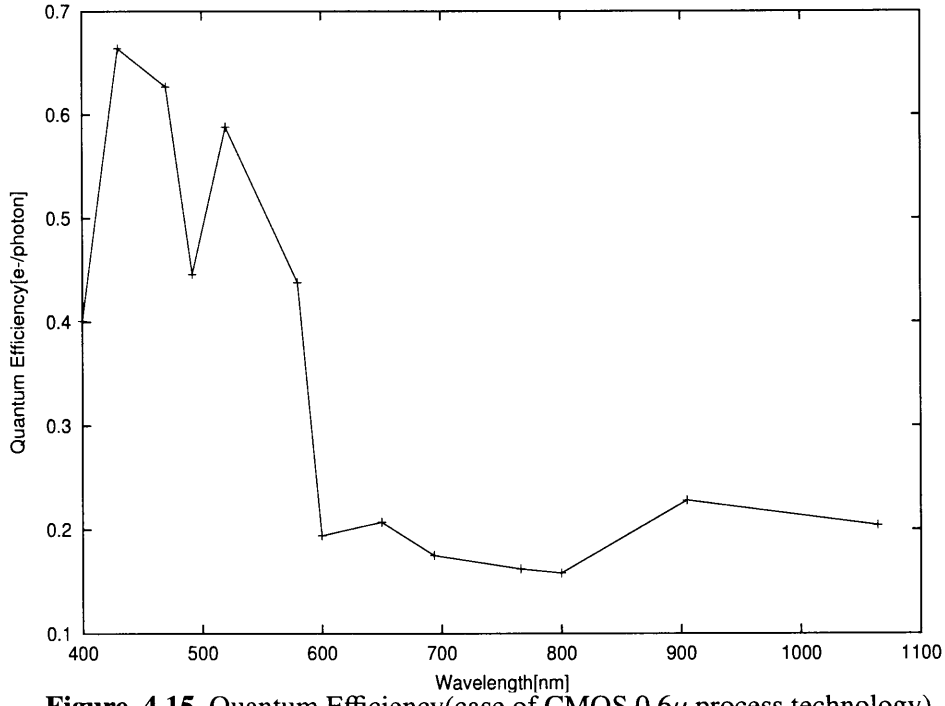

Figure 4.15 Quantum Efficiency(case of CMOS 0.6μ process technology)

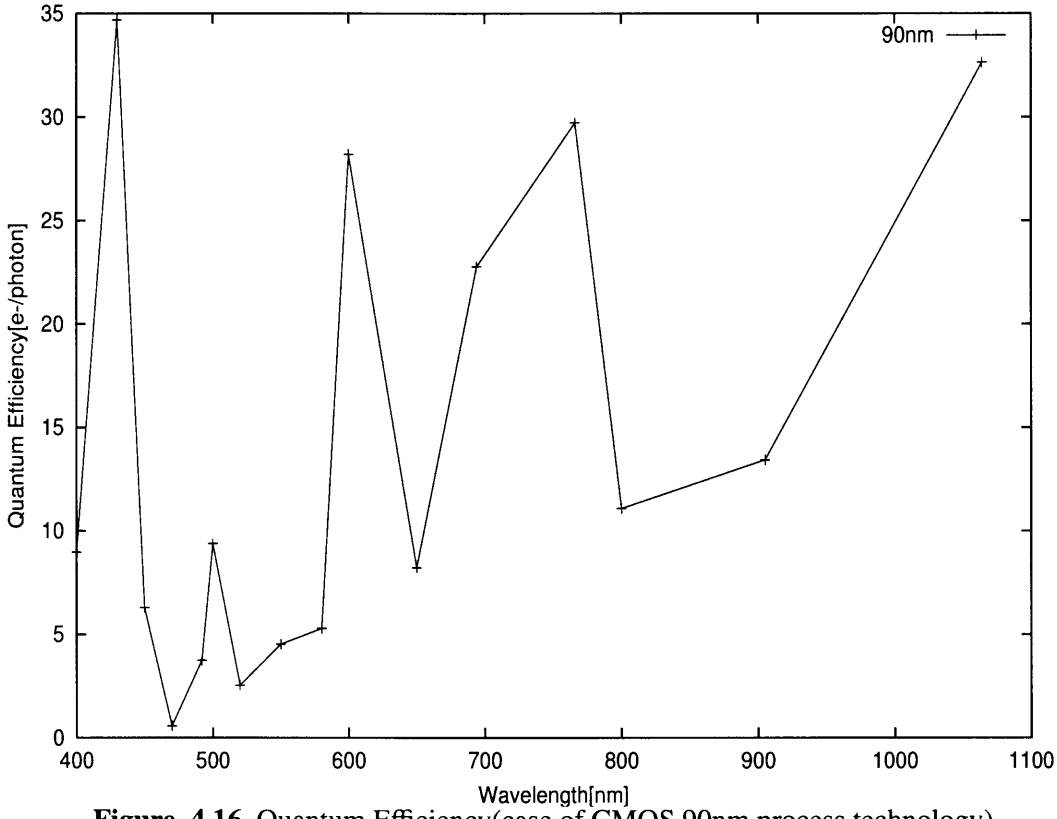

Figure 4.16 Quantum Efficiency(case of CMOS 90nm process technology)

Chapter 5

Scaling of Sensitivity trend

5.1 Concept of Photoelectric conversion

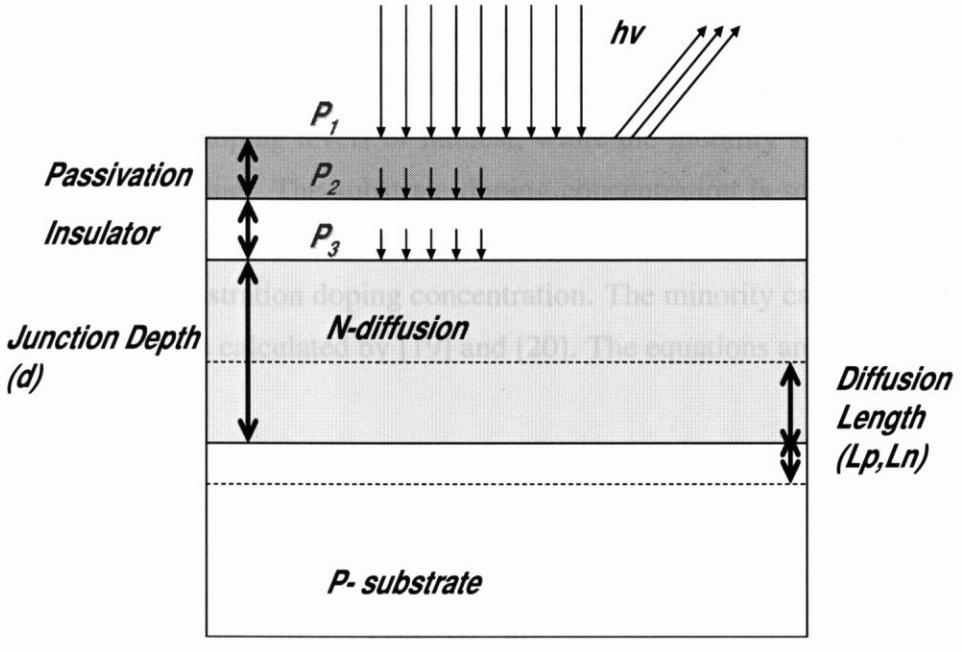

Figure 5.1 Concept of photoelectric conversion

This chapter explains how photons are converted into electrons. Appearance of photon absorbed in photodiode is shown in fig. 5.1. Firstly, the incident light absorbed or reflected in passivation layer and Insulator, repectively. The incident photons extinct in this operation. Secondly, the incident light absorbed or reflected in deletion layer and diffusion layer.

5.2 Trends of Sensitivity inside Photodiodes

5.2.1 Trends of Quantum Efficiency

In this section, we explain scaling trends of quantum efficiency. Carriers generated by photons within the depletion region are collected completely by the sensing element. Typically the depletion layer of a PN junction is thin, so photon absorption is assumed to be uniform over the depletion layer. So, carriers generated by photons in the neutral bulk semiconductor are collectred by the sensing element via diffusion of the minority carrier, which is characterized by the diffusion length, $L_{diff} = \sqrt{D_\tau}$, where D is the diffusion constant and τ is the carrier life time. So, we need to scale the trends of diffusion length, mobility, and minority carrier lifetime in front of scaling trends of the quantum efficiency.

Both the mobility and the minority carrier lifetime decrease with scaling due to the increase of the substrate doping. Fig. 5.2 shows the minority carrier diffusion length as a function of device technology generation. The minority carrier lifetime is inversely proportional to the substrate doping at the doping levels of interest, while the mobility slowly decreases with increasing substrate doping. The substrate doping concentration is scaled by [16, 23]. In fig. 5.2, points are from [23] and line represents results of matching data from [23] and calculation results of substration doping concentration. The minority carrier lifetime and the mobility (fig. 5.3, 5.4) is calculated by [19] and [20]. The equations are

$$\tau_n^{-1} = 3.45\ x\ 10^{-12}\ N_A + 0.95\ x\ 10^{-31}\ N_A^2\ s^{-1} \tag{5.1}$$

$$\tau_p^{-1} = 7.8\ x\ 10^{-13}\ N_D + 1.8\ x\ 10^{-31}\ N_D^2\ s^{-1} \tag{5.2}$$

$$\mu_n = 232 + \frac{1180}{(1 + (\frac{N_A}{8\ x\ 10^{16}})^{0.9})}\ cm^2\ V^{-1}\ s^{-1} \tag{5.3}$$

$$\mu_p = 130 + \frac{370}{(1 + (\frac{N_D}{8\ x\ 10^{17}})^{1.25})}\ cm^2\ V^{-1}\ s^{-1} \tag{5.4}$$

eq. 5.1 and eq. 5.2 show the lifetime of electrons and hole, repectively. Eq. 5.3 and eq. 5.4 show the mobility of electrons and hole, repectively. Diffusion length, $L_{diff} = \sqrt{D_\tau}$, where

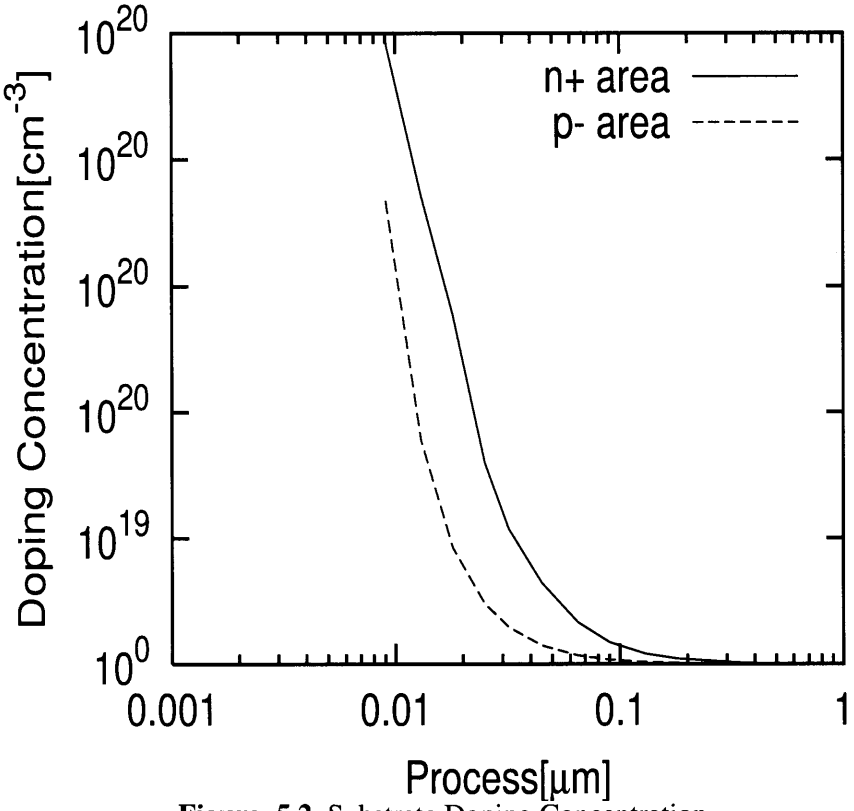

Figure 5.2 Substrate Doping Concentration

D is the diffusion constant and τ is the carrier life time is scaled by 5.3, 5.4, also. Diffusion length shows in fig. 5.5.

CMOS technologies, used to build image sensors, needs to pay attention to the location and depth of the photodiode junctions and the depth o the depletion region of the photodate since they determine the spectral sensitivity of the image sensor. Fig. 5.7 plots the edge of the depletion region (junction depth plus the depletion depth of a source/drain diode at V_DD reverse bias for a photodiode, and the gate induced depletion depth for a photogate) versus the minimum feature size. Comparing Fig. 5.7 with the absorption length of visible light in silicon (Fig. 5.8) [22], it is apparent that for CMOS imagers, most photo-carriers are not generated in the depletion region but rather in the neutral region, and most photo-carriers are collected via carrier diffusion, allowing for the possibility of cross-talk[16].

The quantum efficiency is defined a function of the wave length of the incident light[15, 21]. To derive the quantum efficiency, we use the simple one-dimension geometry shown in Fig. 5.9 where d is the junction depth, and Ln and Lp are the minority diffusion length in the P side and n side repectively.

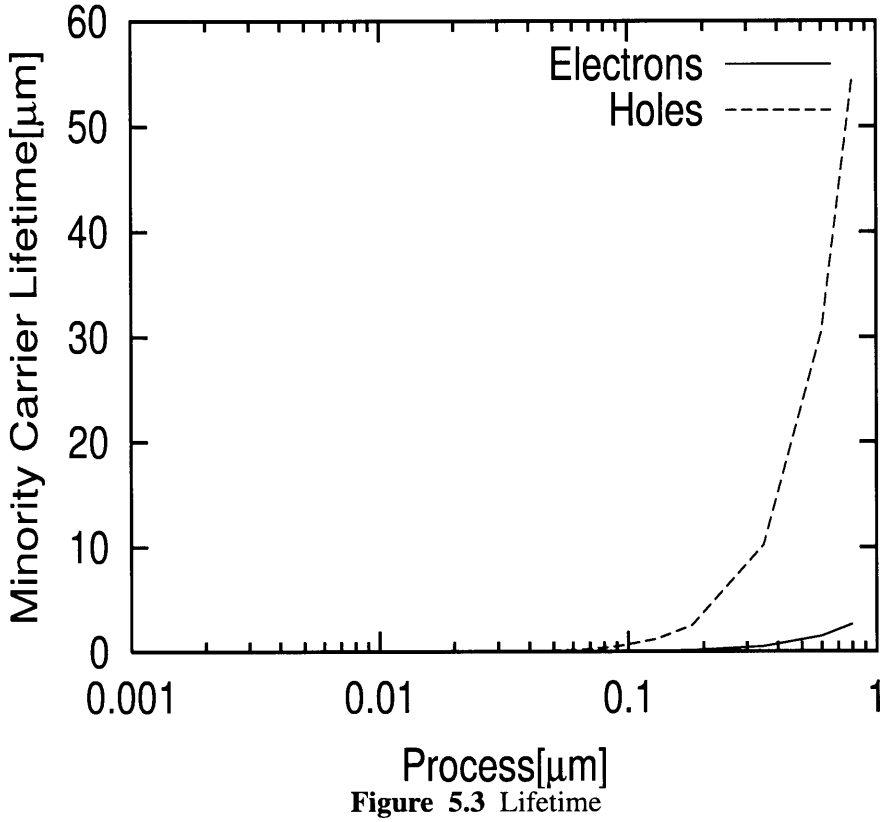

Figure 5.3 Lifetime

We assume that the depletion width of the junction is much smaller that *Ln* or *Lp*. For incident photons with energies in excess of the energy gap ($hv \geq$ Eg), the density of the photons in the semiconductor varies as $\Phi = \Phi_0 exp(-\alpha x)$ where Φ is in the units of photon/sec-cm^2 and α is the absorption coefficient which is a function of wave length. The hole-electron generation rate by photons is given by

$$G(x) = \Phi_0 \, \alpha \, e^{-\alpha x} \tag{5.5}$$

In the *n* side the minority carriers (holes) created at a distance *x* will have a fraction proportional to $exp[-(d - x)/Lp]$ diffuse to the junction. The total number of minority carriers reaching the junction due to creation of hole-electron pairs in the *n* side is given by

$$N = \int_0^d \Phi\alpha \, exp(-\alpha \, x \,) exp[-\frac{|d - x|}{L_p}] dx \tag{5.6}$$

$$= \frac{\Phi_0 \, \alpha}{\alpha - \frac{1}{Lp}} [exp\left(\frac{-d}{Lp} - exp\,(-\alpha d)\right)] \tag{5.7}$$

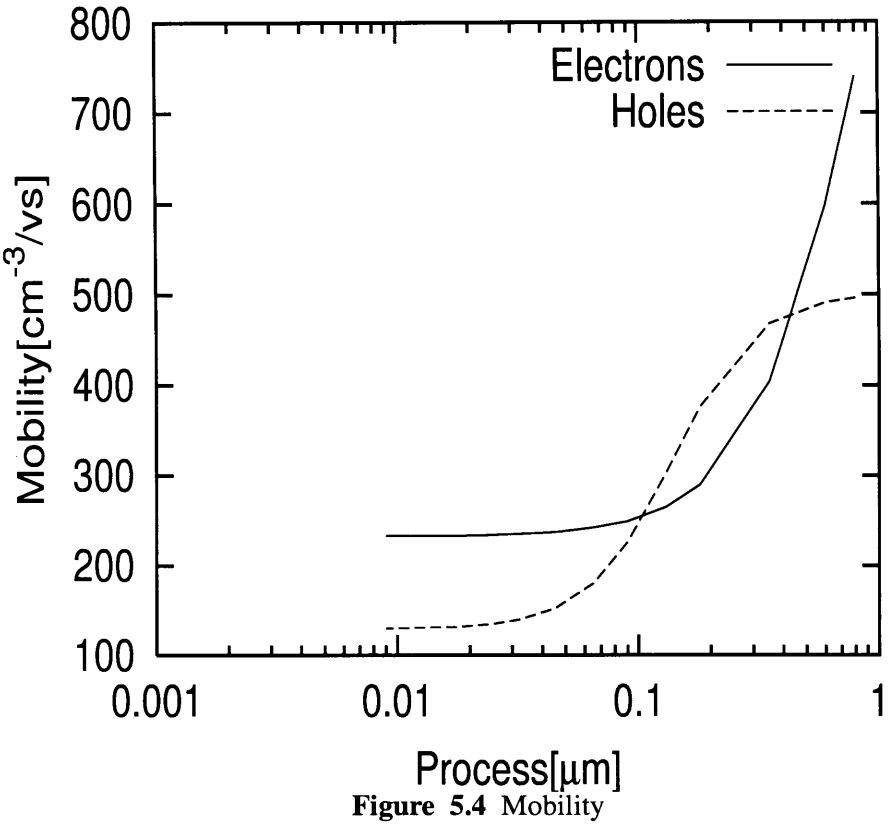

Figure 5.4 Mobility

Similarly, the number of minority carriers (electrons) reaching the junction as a result of the creation of hole-electron pairs in the *p*-region is the integral of Eg. 5.7 from $x = d$ to $x = \infty$ with Lp replaced by Ln. Thus the total number of carriers crossing the *p-n* junction is

$$N_T = \frac{\Phi_0 \alpha}{\alpha - \frac{1}{Lp}}\left[exp\left(\frac{-d}{Lp} - exp\right)(-\alpha d)\right] + \frac{\Phi_0 \alpha exp(-\alpha d)}{(\alpha + \frac{1}{L_n}} \tag{5.8}$$

In the steady state the current throught the cell is a constant, hence it is proportional to N_T. For an equal-energy spectrum, the photon density is proportional to the wavelength of the incident light, since the energy of an individual photon is proportional to frequancy. Therefore Φ_0 itself is proportional to wavelength for an equal-energy spectrum. The current per unit wavelength is then given from Eq. 5.8[15]:

$$I \sim \alpha \lambda\{ \frac{Lp}{1 - \alpha Lp}[exp(-\alpha d) - exp\left(\frac{-d}{Lp}\right)] + \frac{Ln\, exp(-\alpha d)}{1 + \alpha Ln}\} \tag{5.9}$$

The above equations are for *n*-on-*p*. For *p*-on-*n* , we have only to replace the quantity Lp with Ln.

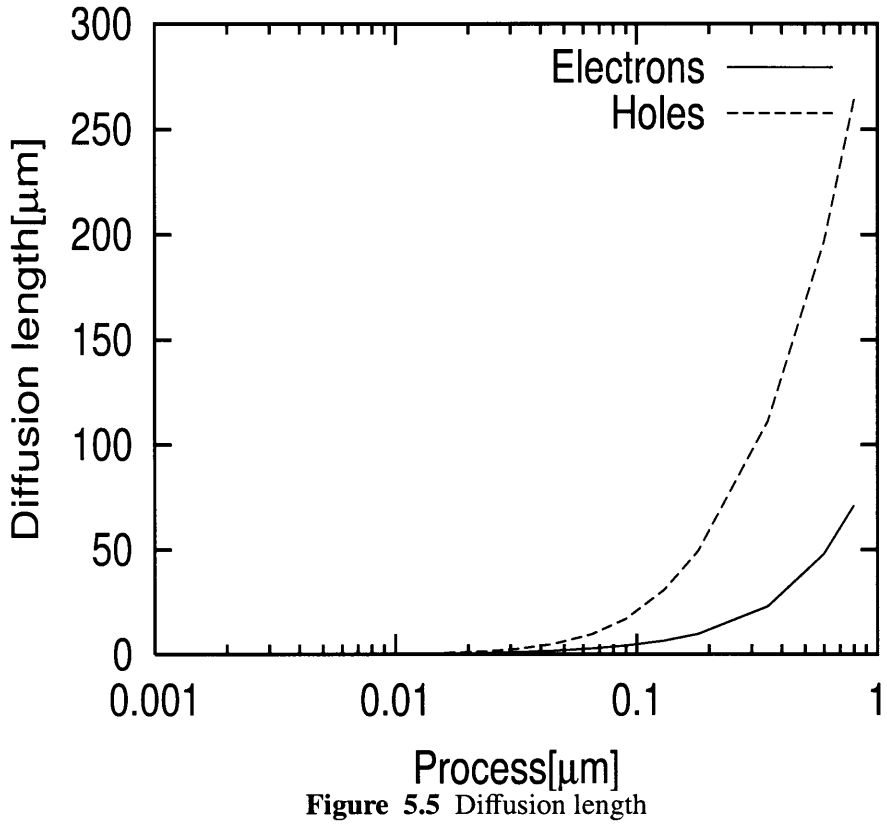

Figure 5.5 Diffusion length

Scaling effect shows in fig. 5.10. Quantum efficiency shift left to short wave lengths. The Peaks of quantum efficiency shows in fig. 5.11. We show the comparsion results of measurement with the theoretical value in fig. 5.12, 5.13.

5.3 Trends of Spectral Sensitivity

The spectral sensitivity is different from quantum efficiency. The spectral sensitivity contains not only photodiode's characteristics of generated photocurrent, but also readout conversion gain, which is affected with the process technology. In this section, we scale the trends of spectral sensitivity with concepts from [7]. The spectral response SR(λ)is related to the quantum efficiency according to the equation

$$SR\,(\lambda) = \frac{\lambda\, q}{h\, c_0} \cdot QE(\lambda) \tag{5.10}$$

with q representing the elementary charge and hc_0 the product of Plank's constant and the vaccum speed of light.

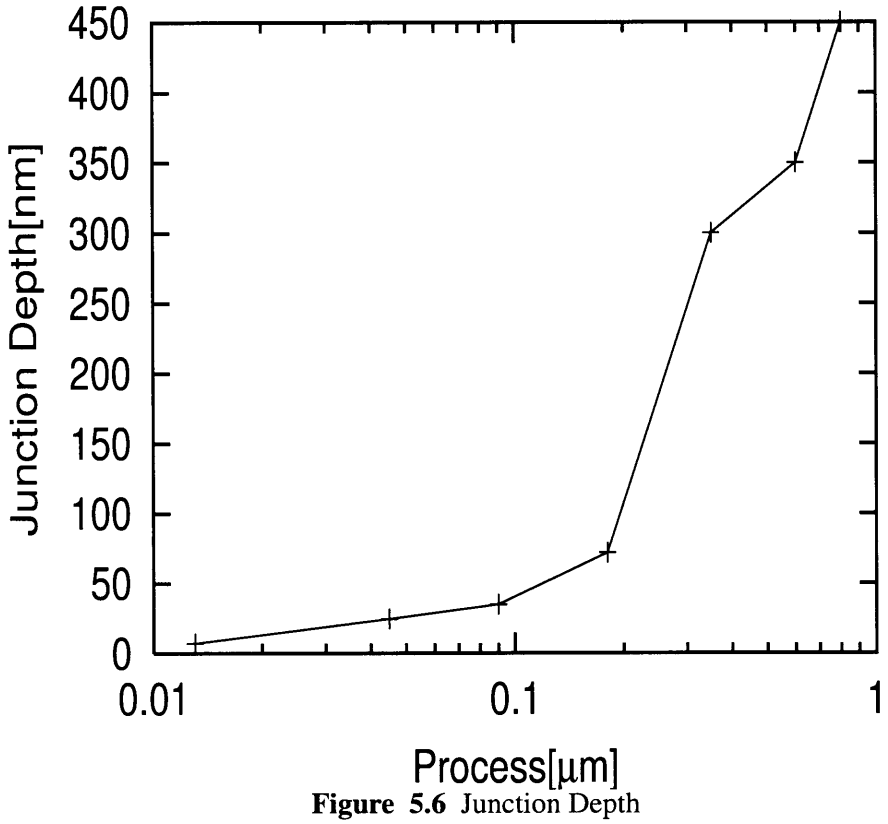

Figure 5.6 Junction Depth

If a photodiode is exposed to a spectral power density $\Phi(\lambda)$(in W/cm^2nm) the collectrd photocharge Q can be expressed as

$$Q = A_{eff} \cdot T_{int} \cdot \int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda \tag{5.11}$$

with A_{eff} denoting the effective photoactive area of a pixel and T_{int} the integration time. Illumination is assumed to be constant during the exposure time.

The photoactive region is determined by the effective optical fill factor FF of the device that describes the portion of the pixel area A_{pix} which contributes to photosensitivity

$$FF = \frac{A_{eff}}{A_{pix}} \tag{5.12}$$

The spectral response and the quantum efficiency data used in this treatise are referred to the photoactive area rather than to the complete pixel area.

The voltage swing V that is obtained from the collected photocharge is inversely proportional to the integration capacitance C_{int}, as follows:

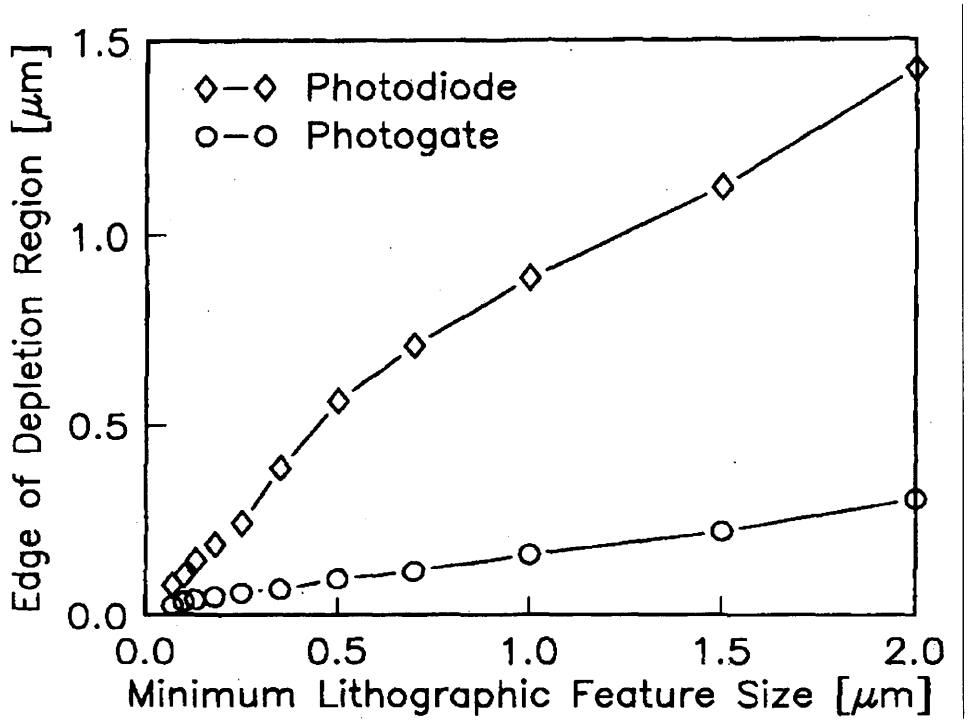

Figure 5.7 The location of the edge of the depletion region as a function of *Lg*

$$V = \frac{Q}{C_{int}} = \frac{FF \cdot A_{eff} \cdot T_{int}}{C_{int}} \cdot \int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda \tag{5.13}$$

The following sensitivity considerations are all referred to the pixel input. Additional amplification in the pixel or system electronics is ignored and can be applied in all CMOS based imaging technologies. However, any circuitry creating gain reduces the effective fill factor in a CMOS pixel.

In order to calculate the sensor sensitivity the integrated photovoltage has to be divided by the optical energy impinging on the pixel during the integration time:

$$S_W = \frac{FF \cdot A_{pix}}{C_{int}} \cdot \frac{\int SR(\lambda) \cdot \Phi(\lambda) \cdot d\lambda}{\int \Phi(\lambda) \cdot \lambda}. \tag{5.14}$$

Integration extends over the relevant wavelength interval in which $SR(\lambda)$ exhibits values different from zero. The quantity defined by equation (5.14) is designated as radiometric sensitivity [in $V/(\mu J/cm^2)$].

We derive the spectral sensitivity from Eq. 5.14 and Eq. 5.10. $QE(\lambda)$ is scaled as forechapter. Φ, the incident light intensity assumed the constant, also. The spectral sensitivity

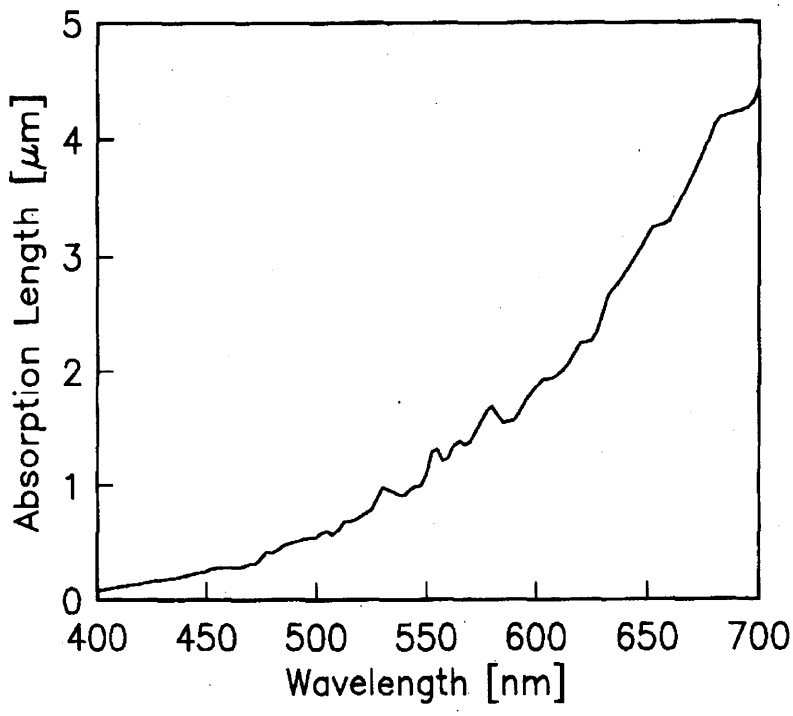

Figure 5.8 Light absorption length in silicon. Data from E.Palik [22]

is calculated as an effective value at the pixel readout node C_{FD}. It depends on effective integration capacitance, pixel area and fill factor. Finally, we calculate the spectral sensitivity as belowed.

$$S_W(\lambda) = \frac{FF \cdot A_{pix}}{C_{FD}} \cdot \frac{\lambda q}{hc_0} \cdot QE(\lambda). \tag{5.15}$$

The capacitance of the high impedence node(C_{FD}) that converts the signal charge to a voltage determines the charge conversion gain (Gain = C_{FD}^{-1}). In photodiode architectures the readout diode is either in parallel with or the same as the imaging diode.

The capacitance of the high impedence node (C_{FD}) scales with the minimum feature size (Fig. 5.14). This is because both the areal($C_{ox}xA_{gate}$ and $C_{junction}xA_{junction}$) and overlap($C_{ov}xW_{gate}$) capacitances scale with the minimum feature size. As a result, high charged to voltage conversion gain(conversion gain = $1/C_{FD}$)(Fig. 5.15) can be obtained as technology advances. The C_{FD} for the case of a combined imaging and readout diode increase again at small feature size after the pixel size ceases to decrease because the fill-factor increasing the total capacitance of the imaging diode[16].

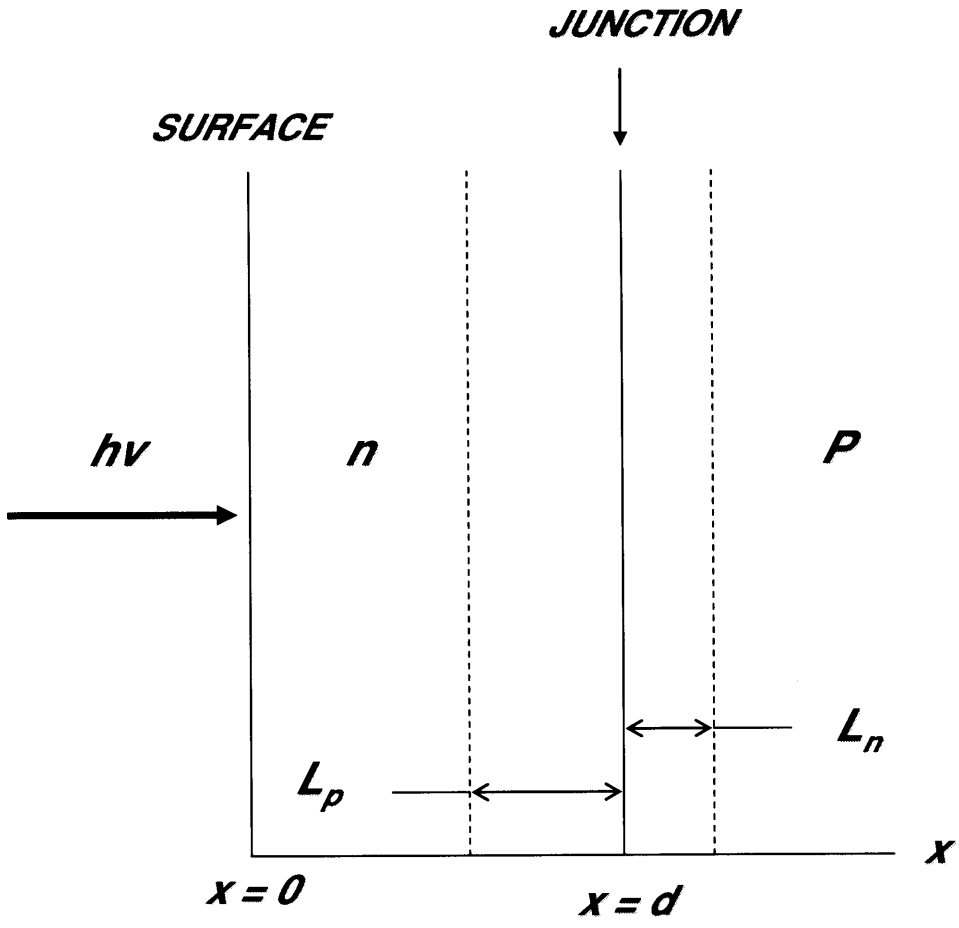

Figure 5.9 One-dimensional geometry with junction depth d and minority carrier diffusion lengths Ln and Lp for the P side and n side [15, 21]

We scaled the spectral sensitvity for two ways. The one is assumed that the FF stays constantly with improvement of process technologies. In this case, we assumed that the FF is 25%, which is specificated from [16]. The area of pixel is also represented in table. 2.1. Firstly, Fig. 5.16 shows the scaling trends of spectral sensitivity in advanced technologies. The peaks movements of spectral sensitivity is shown in Fig. 5.17, also.

The other one of scaling way is that we scale with fixed conversion gain in the downscaling technologies. With downscaling process technologies, if the pixel area does not need to change, the conversion gain is fixed. So, we scale the trend of spectral sensitivity with fixed the conversion gain. The results is shown in Fig. 5.18. As a result, sensitivity of CMOS image sensor decrease with downscaling technologies with fixed conversion gain. We assume that the conversion gain is not main effect of sensitivity charactersitics.

Finally, we compared the results of scaling with results of measurement. From quantum

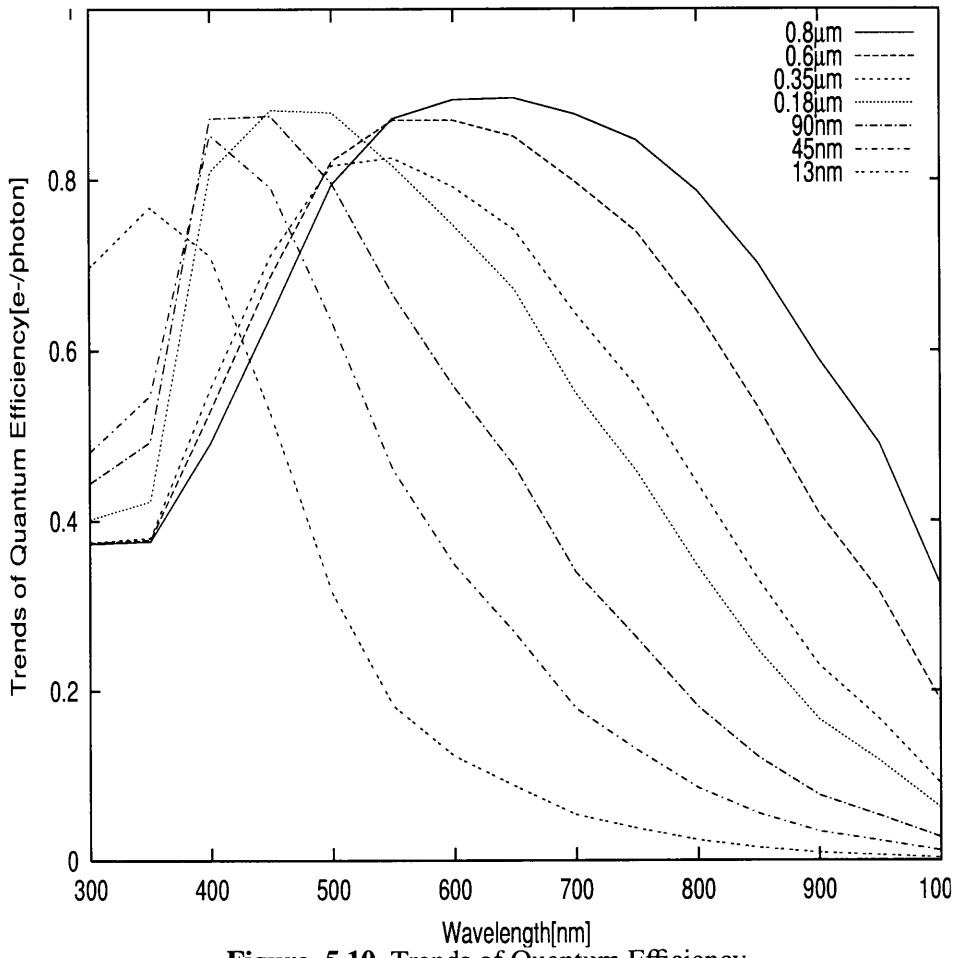

Figure 5.10 Trends of Quantum Efficiency

efficiency results of measurement in $0.6\mu m$ technologies, we calculate the spectral sensitivity with Eq. 5.14. From comparison, the results of measuremet are smaller than theoretical values. We guess the reason that the theoretical formula doesnot consider the effect outside photodiode, photodetect region. So, we consider the effect of light loss of multilayer interconnects in the next chapter. The measurement error cause to the difference of two results, as well. We consider this measurement error as future work.

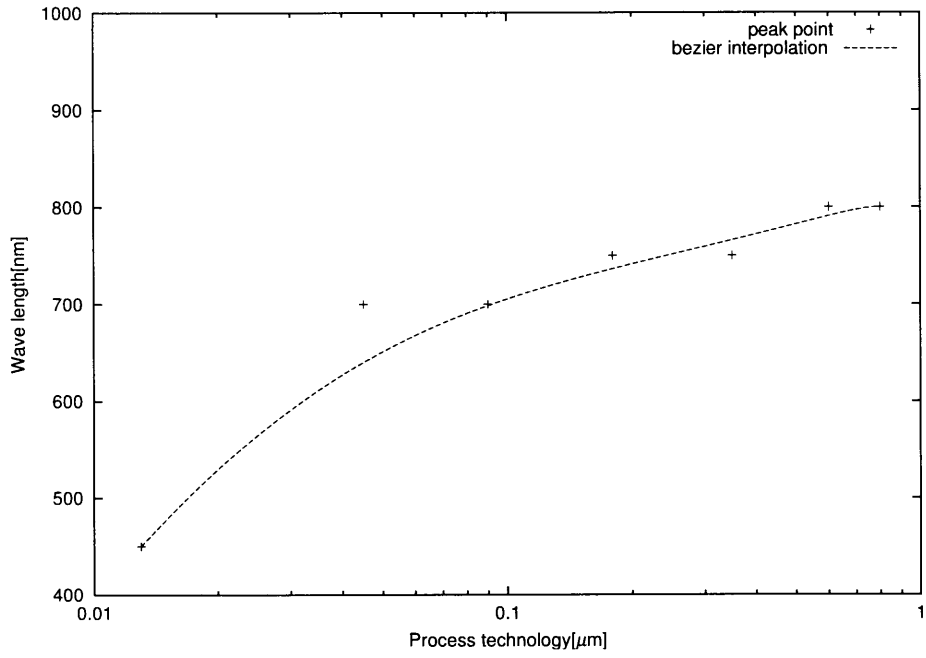

Figure 5.11 Movement of peak value

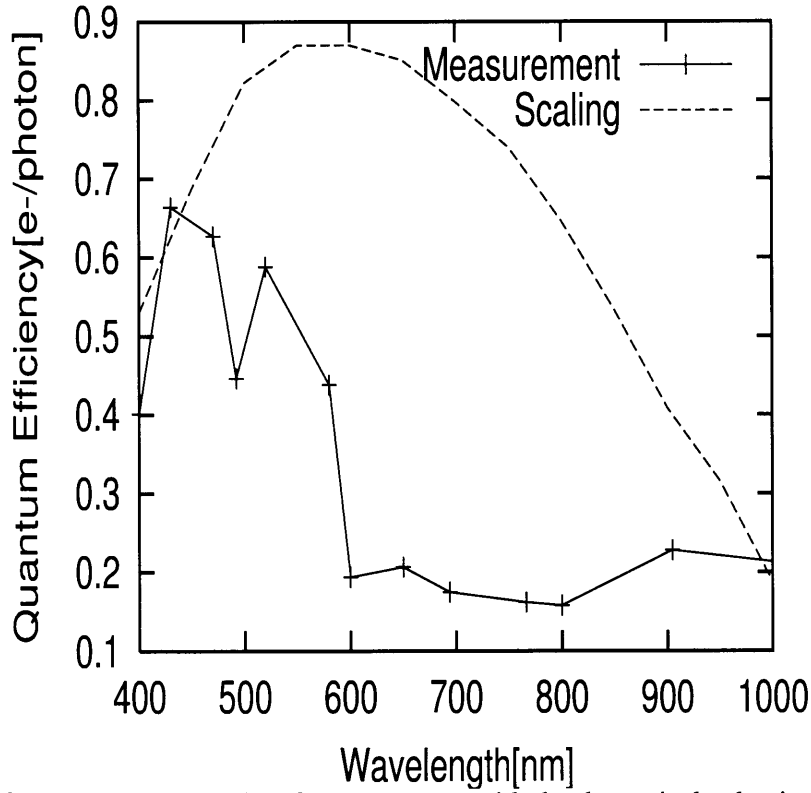

Figure 5.12 Comparison Results of measurement with the theoretical value in 0.6μm process

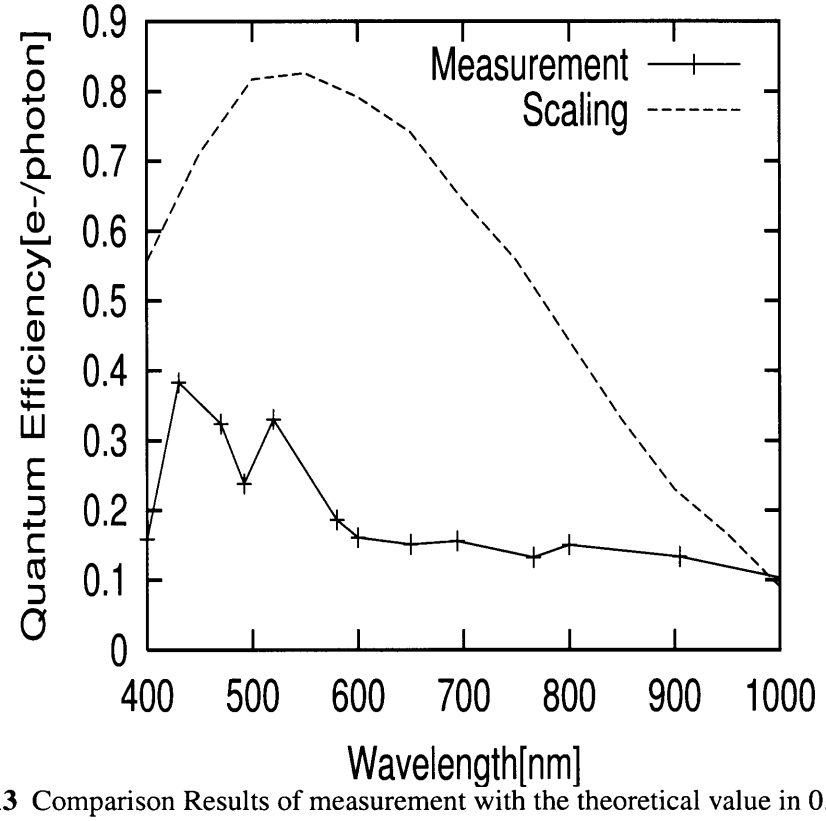

Figure 5.13 Comparison Results of measurement with the theoretical value in 0.35μm process

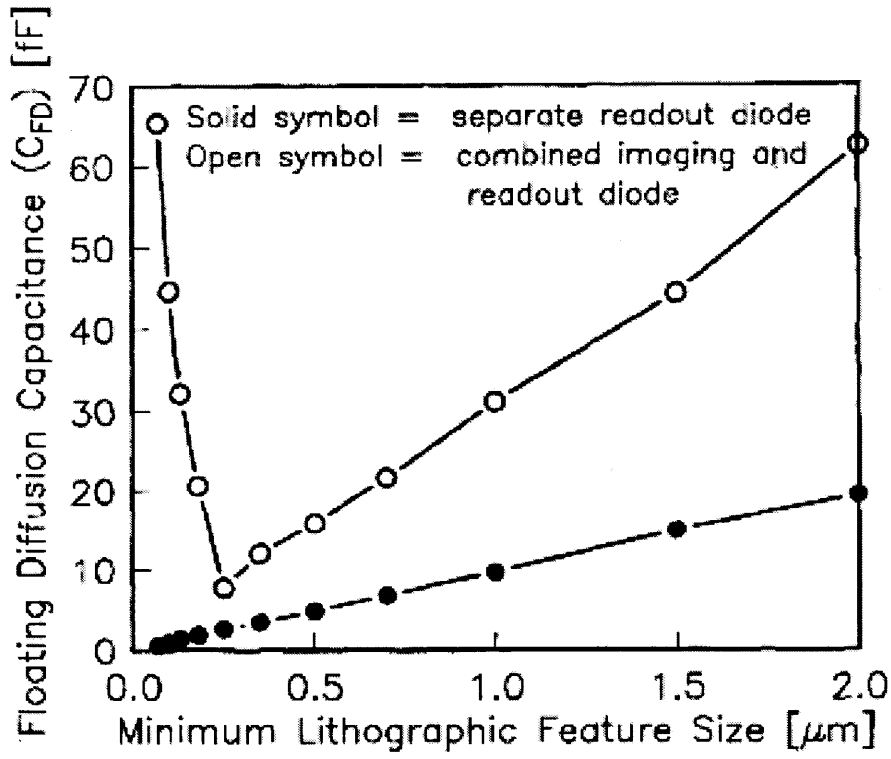

Figure 5.14 Floating Diffusion node capacitance as a function of the minimum feature size[16].

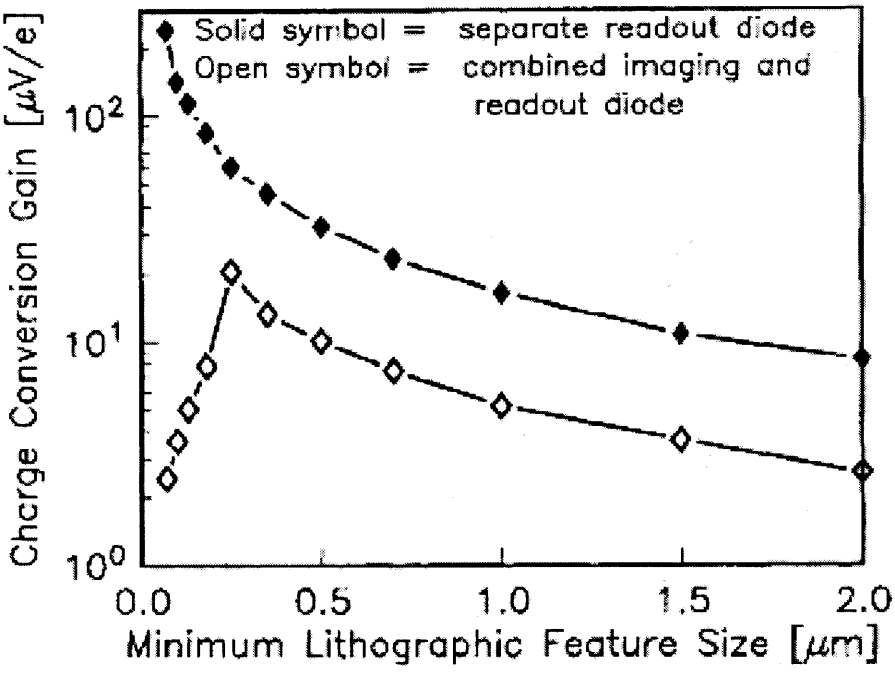

Figure 5.15 Charge to voltage conversion gain as a function of the minimum feature size[16].

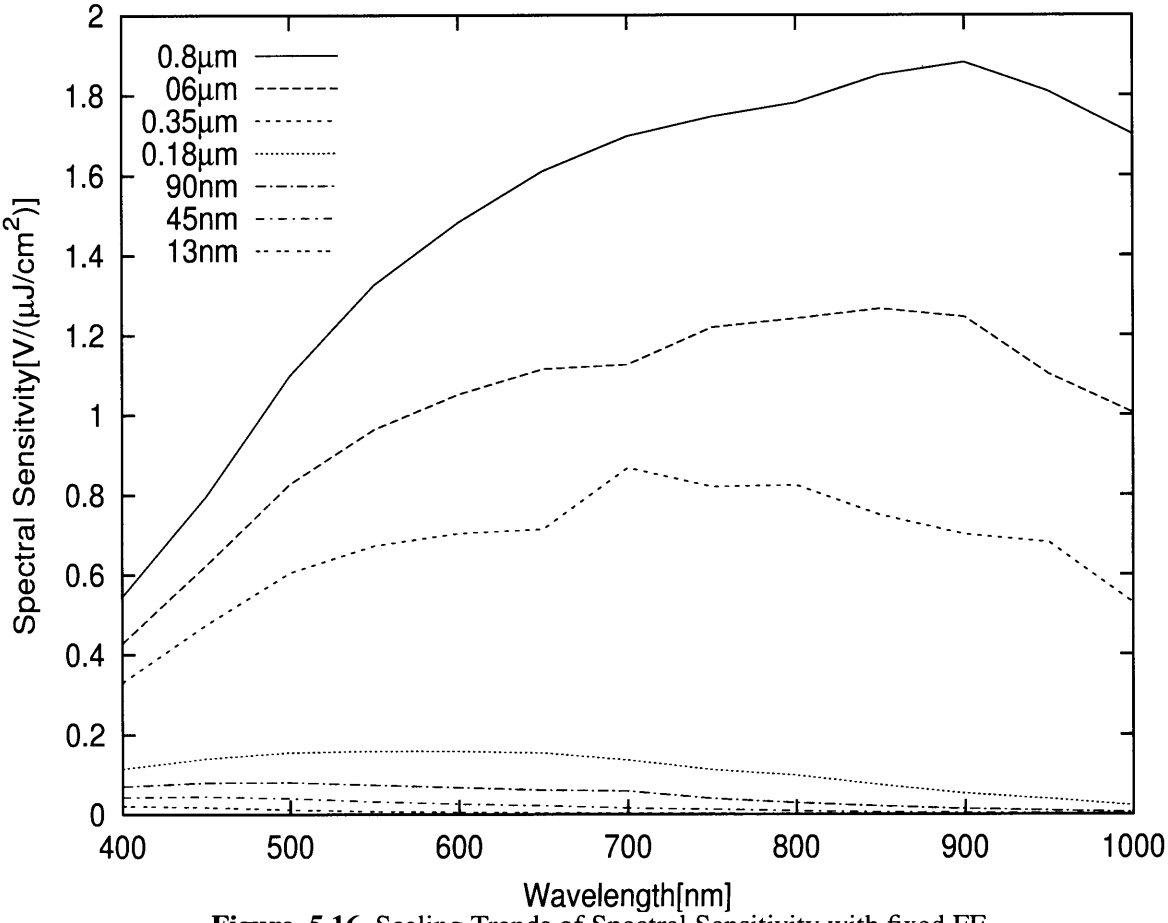

Figure 5.16 Scaling Trends of Spectral Sensitivity with fixed FF

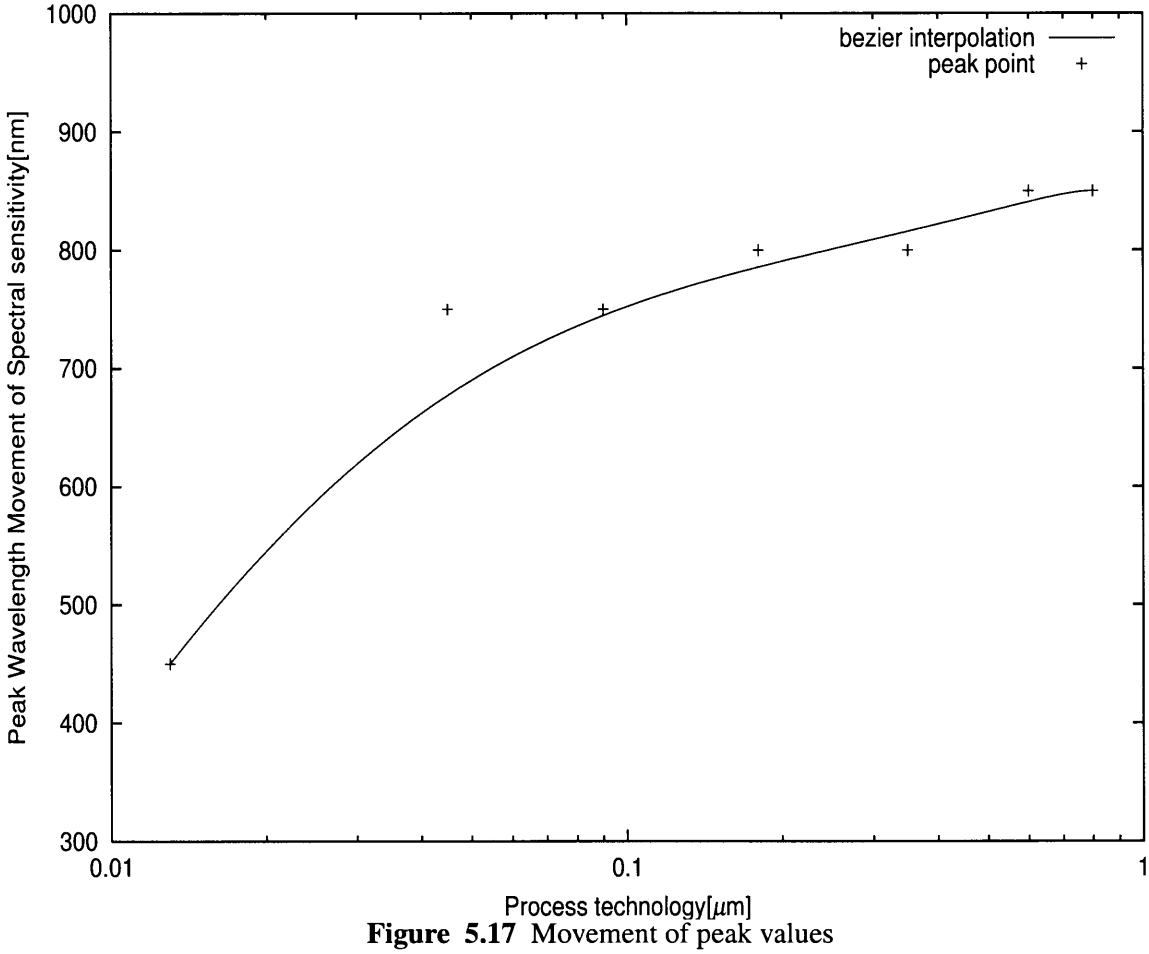

Figure 5.17 Movement of peak values

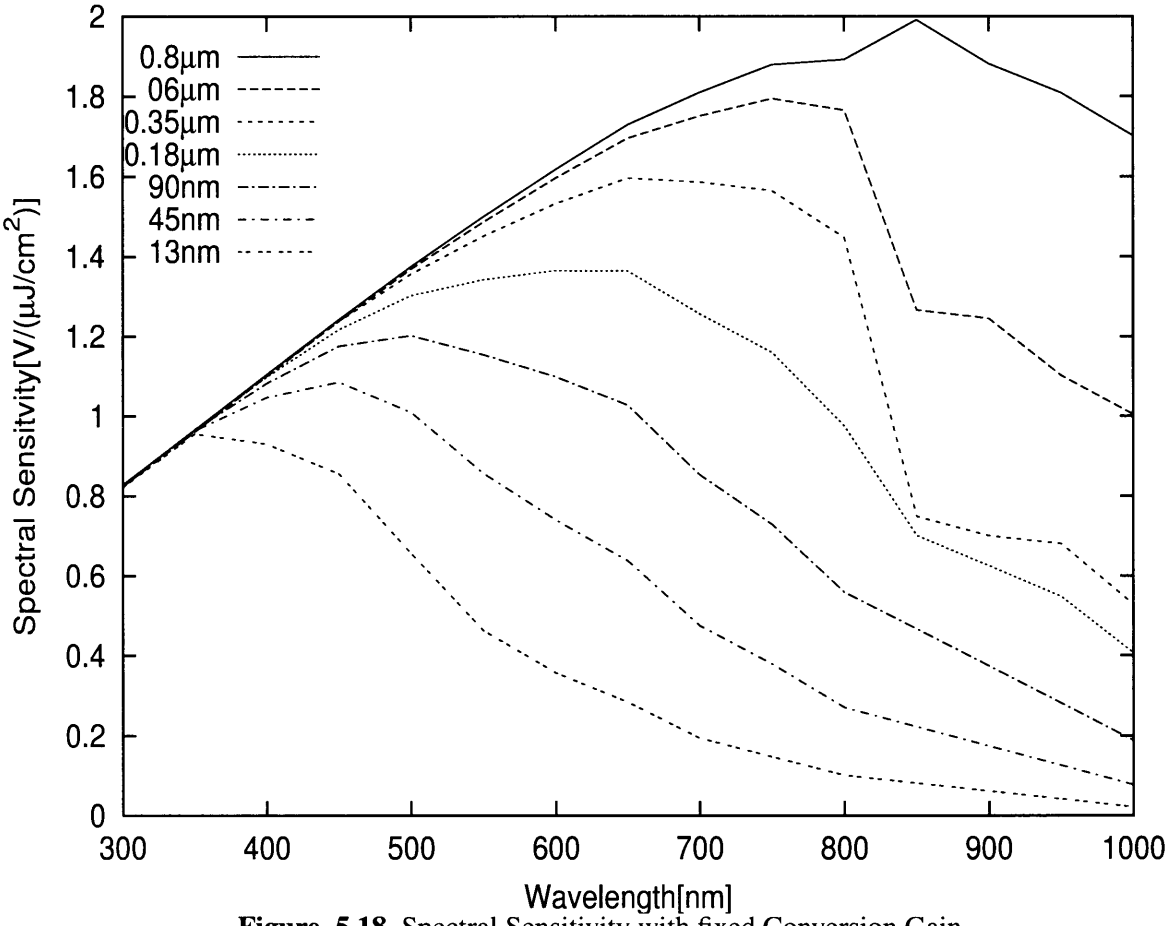

Figure 5.18 Spectral Sensitivity with fixed Conversion Gain

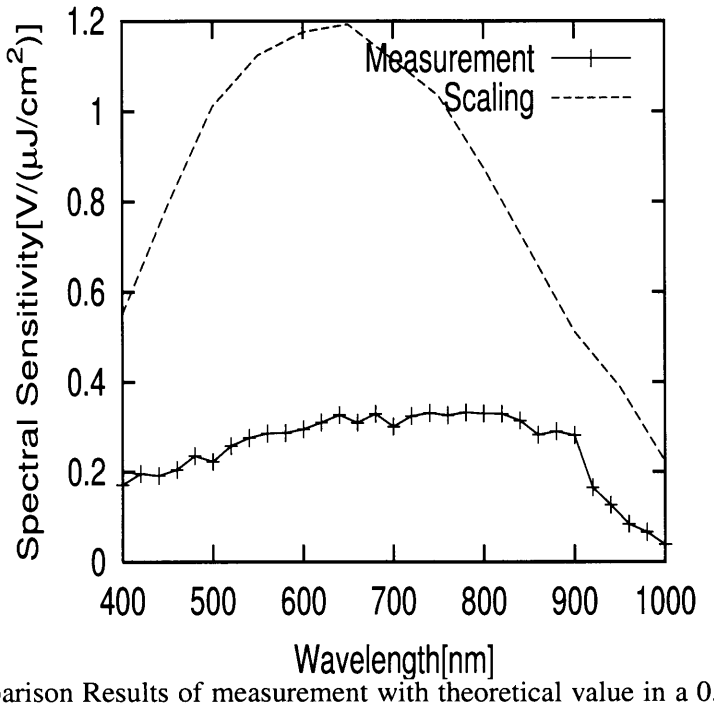

Figure 5.19 Comparison Results of measurement with theoretical value in a 0.35μm process technology

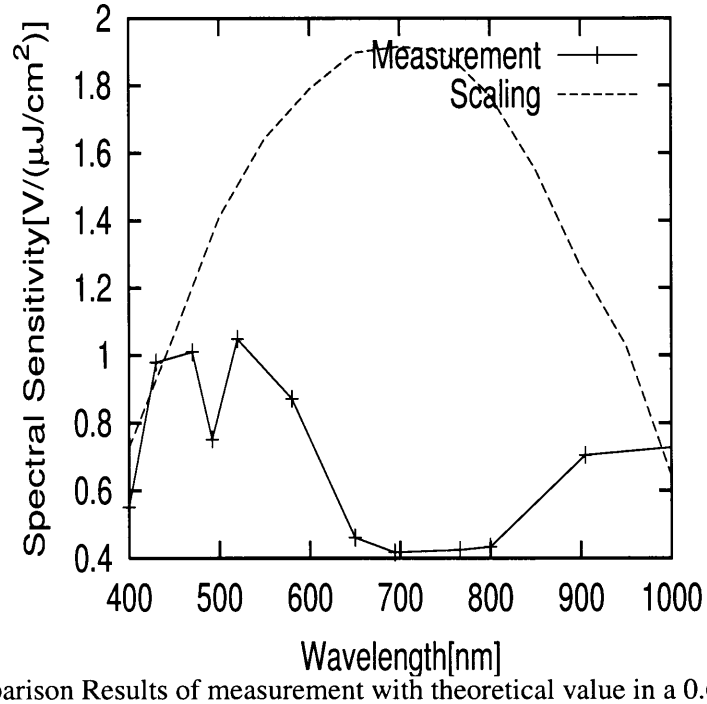

Figure 5.20 Comparison Results of measurement with theoretical value in a 0.6μm process technology

Chapter 6

Effect of Optical path loss for multilayer interconnects

6.1 Trends of Optical path loss for multilayer interconnects

In this section, we scale the trends of effect outside the silicon division. We need to consider the absorption and the extinction of photons outside silicon parts. Firstly, we consider absorption and extinction of photon in an insulator layer, SiO_2. The depth of an insulator layer affect the sensitivity of photodiode, directly. So, we scaled photocurrent remained with the depth of an insulator layer.

For scaling, the refractive index and the extinction coefficient are used for estimation of absorption and reflection in an insulator layer. Before addressing the refractive index, *n(E)* and the extinction coefficient, *k(E)*, we explain the concept of these elements [24]. The fraction of light lost to scattering and absorbtion per unit distance in a participating medium. Extinction coefficient is the sum of the absorption coefficient and the scattering coefficient. The refractive index of a material is the factor by which the phase velocity of electromagnetic radiation is slowed in that material, relative to its velocity in a vacuum.

The refractive index, *n(E)*, and the extinction coefficient, *k(E)*, are related by the Kramers-Krong dispersion relations. These relations are a consquence of the analytic behavior of the complex index of refraction, $N(E) = n(E) - ik(E)$. In turn, the analytic behavior of N(E) stems from the principle of casuality, which states that no signal can be transmitted through a medium at a speed greater than that of light in vaccum. Based on concepts of two elements, we calculated the refractive index, *n(E)*, and the extinction coefficient, *k(E)* [24]. Results shows in tab. 6.1.

Secondly, we consider the lambert law, who indicates the linear relationship between absorbance and concentration of an absorping species. The lambert law shows the relationship

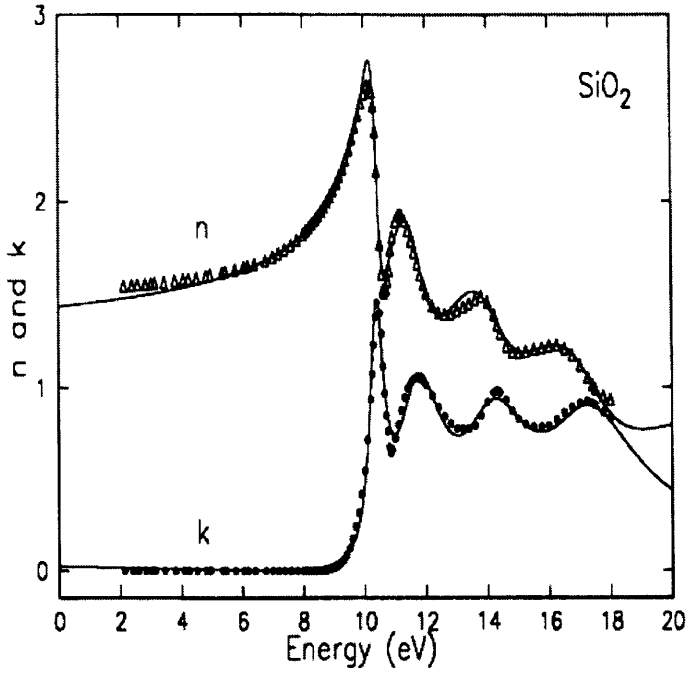

Figure 6.1 Infractive index and Extinction coefficient(SiO_2)

Table 6.1 Optical properties of insulator layer(SiO_2)[22, 24]

Wave length(nm)	Energy(eV)	*k(E)*	*n(E)*
400	3.07	0.00251	1.2479
450	2.73	0.00270	1.2493
500	2.46	0.00285	1.2505
550	2.23	0.00297	1.2514
600	2.05	0.00307	1.2522
650	1.89	0.00314	1.2529
700	1.75	0.00321	1.2534
750	1.64	0.00326	1.2539
800	1.53	0.00331	1.2543
850	1.44	0.00335	1.2547
900	1.36	0.00339	1.2550
950	1.29	0.00342	1.2553
1000	1.23	0.00345	1.2556

between the incident light and the tranferred light, in other word. For using the lambert law, it is required to calculate the absorption coefficient, $\beta(\lambda)$, of SiO_2, and the reflection coefficient, R. The formula of equation for the absorption coefficient and the reflection coefficient is

$$R = \frac{(n-1)^2 + k^2}{(n+1)^2 + k^2} \tag{6.1}$$

$$\beta(\lambda) = \frac{4\pi k(\lambda)}{\lambda} \tag{6.2}$$

Results of the absorption coefficient and the reflection coefficient show in fig.**??**

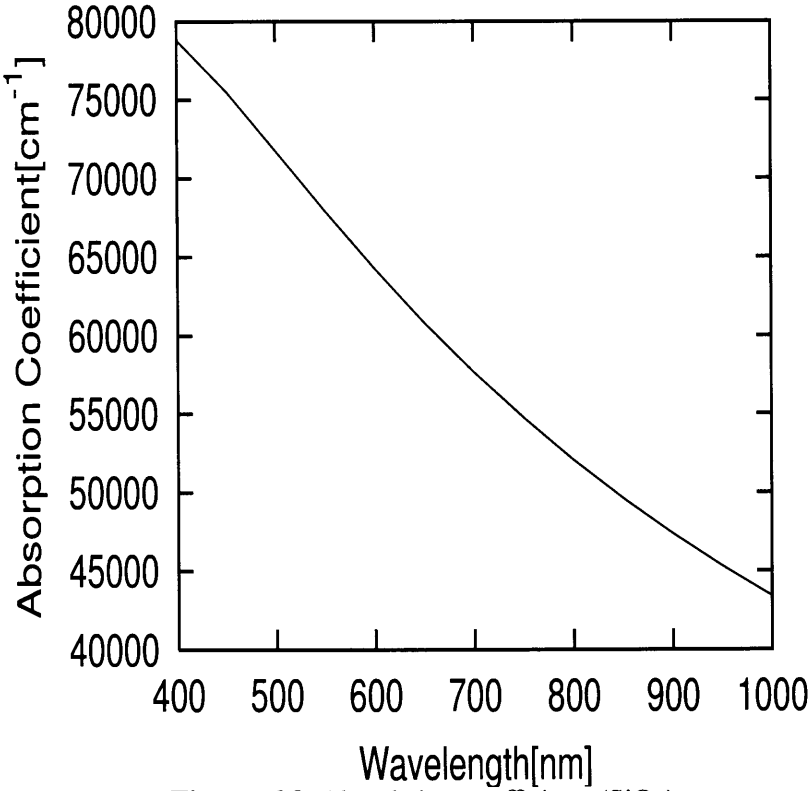

Figure 6.2 Absorbsion coefficienct(SiO_2)

Finally, we scale the effect in the insulator layer by the lambert law 6.3. Result of scaling shows in fig. 6.4. We assumed an insulator depth from $1\mu m \sim 10\mu m$. The thicker insulator layer, the lower photocurrent(sensitivity) in short wave length area.

$$I\lambda = I(\lambda)(exp(-\beta(\lambda)L) - R) \tag{6.3}$$

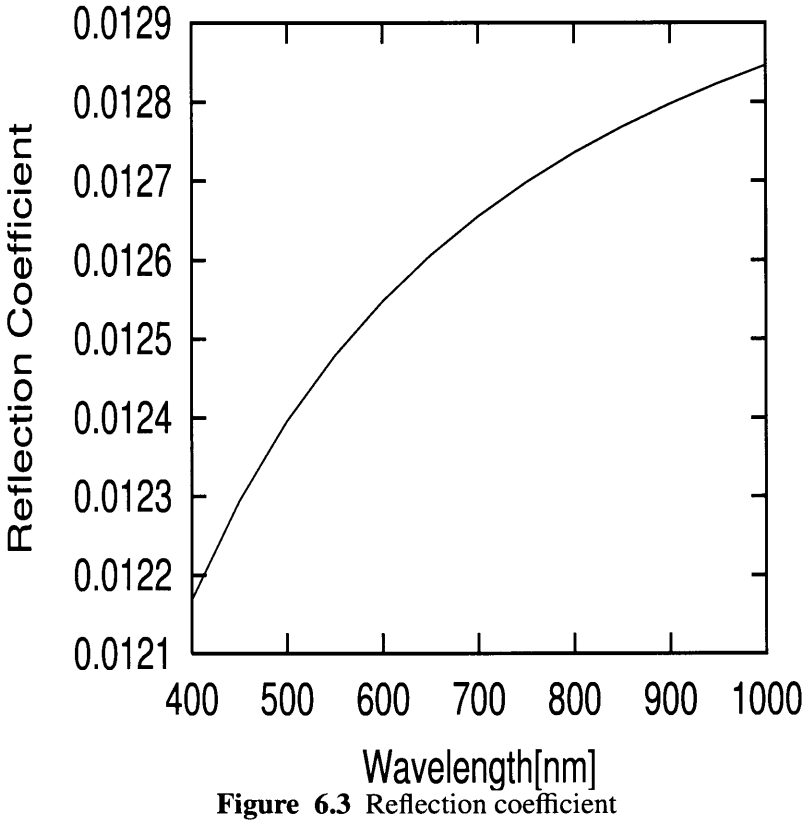

Figure 6.3 Reflection coefficient

On the other hand, we scaled effcet of an insulator layer using real parameter of the CMOS 90nm process technology. In this process, about 20 layers, 6-metal layer, 5-via layer, pad-metal layer, pad-via layer, contact, and poly layer, locate above the silicon. So, we assumed the extinction coefficient is zero in this multi-insulator layers. We calculate the refractice index and the reflection coefficient using the equations as below.

$$n = \sqrt{K_e}. \tag{6.4}$$

$$R = \frac{(n-1)^2}{(n+1)^2}. \tag{6.5}$$

The parameters for scaling is shown in Tab.**??**. Thickness of insulator layer and dielectric constant is given by 90nm process technology. For scaling, we use the concept of tranmission line. As fig. 6.5 shows, we consider that the incident light goes to mult-layer having uniform infractive index each insulator layer.

Thickness of insulator layer and dielectric constant(ϵ) is given by 90nm process technology. We scaled the effect of multi insulator layers by the Eq. 6.3. The results is shown in fig. 6.6.

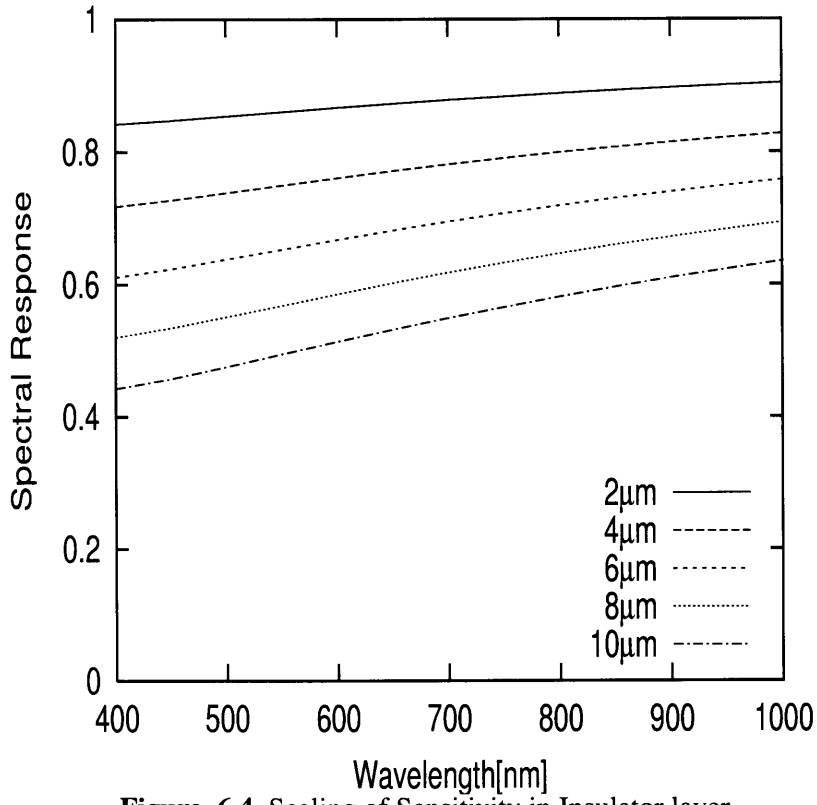

Figure 6.4 Scaling of Sensitivity in Insulator layer

We compared this result with the original spectral sensitivity. From this comparison, multi insulator layers have a considerable effect for sensitivity characteristics.

Table 6.2 Optical properties of 90nm pocess technology

Thickness	Dielectric Constant	n(refractive index)	R(reflection coefficient)
6.4	2.9	1.7029	0.0676
1	6	2.4494	0.1765
0.12	4.4	2.0976	0.1255
1	4.4	2.0976	0.1255
0.12	4.9	2.2135	0.1426
0.7	4.4	2.0976	0.1255
0.1	4.9	2.2135	0.1426
0.1	4.4	2.0976	0.1255
0.5	4.4	2.0976	0.1255
0.1	4.9	2.2135	0.1426
0.05	4.4	2.0976	0.1255
0.2	2.9	1.7029	0.0676
0.05	4.9	2.2135	0.1426
0.02	4.4	2.0976	0.1255
0.2	2.9	1.7029	0.0676
0.05	4.9	2.2135	0.1426
0.15	4.1	2.0248	0.1147
0.05	4.9	2.2135	0.1426
0.05	4.3	2.0736	0.1220
0.35	4.3	2.0736	0.1220
0.05	7	2.6457	0.2037
0.25	4.1	2.0248	0.1147

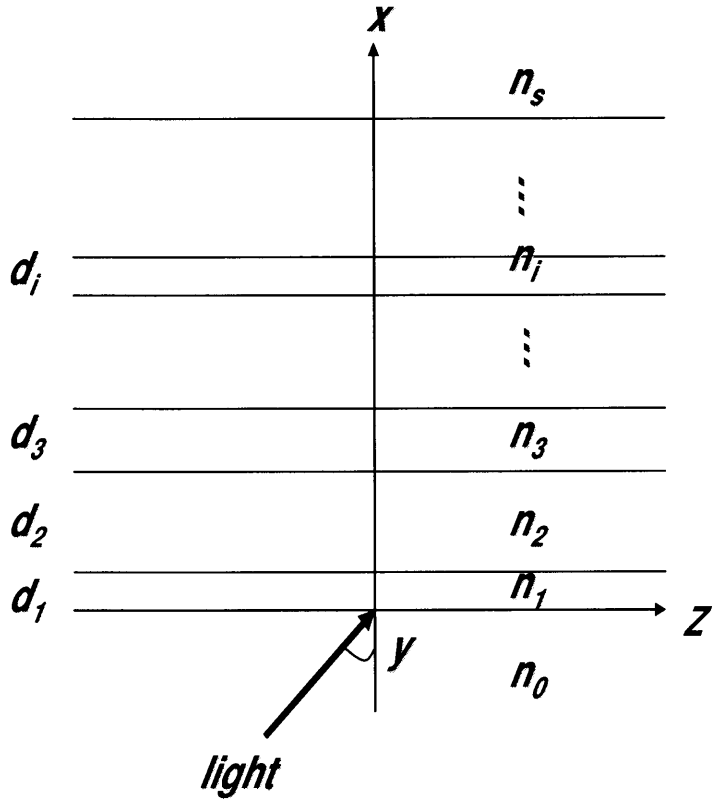

Figure 6.5 Sample configuration of the multi insulator layers

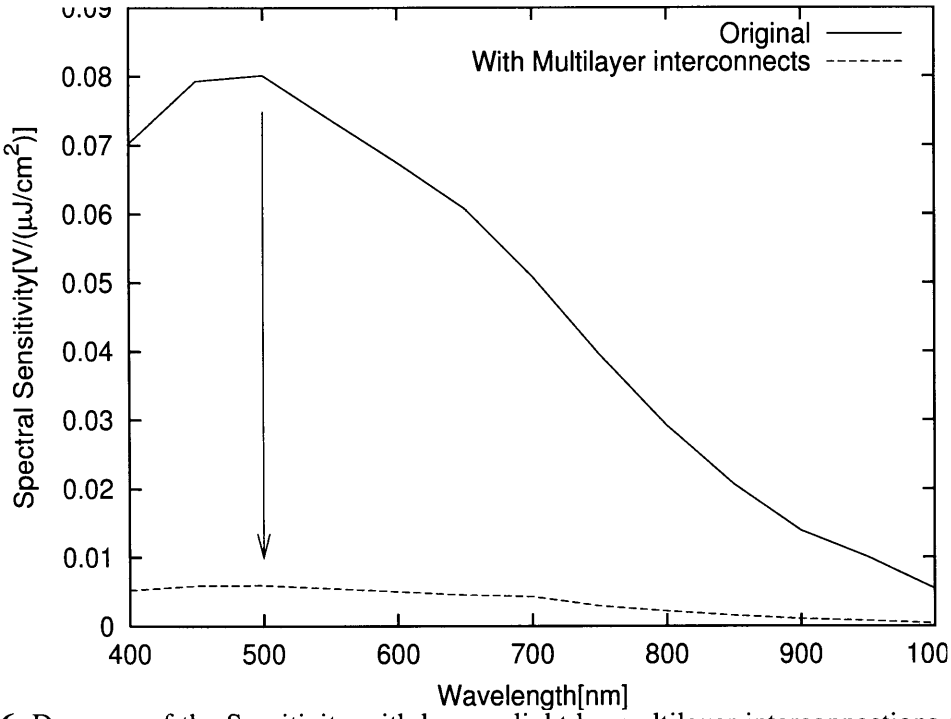

Figure 6.6 Decrease of the Sensitivity with loss og light by multilayer interconnections and low-k layers

Chapter 7

Conclusions

In this research, we estimate the sensitivity chatacteristics of CMOS image sensors for high sensitivity imagers fabricated by deep sub micron technologies.

Firstly, we measured the Sensitivity characteristics, the spectral sensitivity and the quantum efficiency, of image sensors using a standard CMOS 90nm, 0.35μm, 0.6μm process technologies. The spectral sensitivity is measured with an image sensor of a CMOS 0.35μm process technology. In case of the spectral sensitivity, two dispersion equipments, a prism and a diffraction gratings, are used. The results of two dispersion equipments are compared for the reliable measurment. From the result, the image sensor using a standard CMOS 0.35μm process technology have a good performance in red wavelength. The quantum efficiency(Q.E.) is measured by short band pass interference filters, also. In case of the Q.E., three process technologies, which are 90nm, 0.35μm, and 0.6μm technologies, are used. Eventually, photocurrents in the short wave length(about 400nm~500nm) are generated more than in the other wave lengthes.

Secondly, we showed the trends of the sensitivity characteristics in deep sub micron technologies. We divided two parts of sensitivity. One is the photoelectric conversion in photodiode. The other is the reflection and extinction operation outside photodiode, silicon. Additionally, the photoelectric conversion is divided by the spectral response and the quantum efficiency. We scaled the trends of these three operation. The quantum efficiency indicates how many photons converts to electrons. In other side, the spectral sensitivity contains the quantum efficiency and readout gain(conversion gain). As a results, the highest response shifts to short wavelengths. In other words, the spectral response gets worse in visible sight. It is because photocurrent is generated in short wave length having high absorption coefficients. As advanced process, doping concentration is higher, junction depth is thiner. So, long wavelengths hardly absorb in photodiode, as well. We compare the scaled trends with

measurement results. Results of 0.35μm,0.6μm, 90nm process technologies have a large margin. We guess the reason that the theoretical formula doesnot consider the effect outside photodiode, photodetect region. So, we considered the effect of light loss of multilayer interconnects. The measurement error cause to the difference of two results, as well. We consider this measurement error as future work.

We scaled the trends of spectral sensitivity with fixed conversion gain. As a result, sensitivity of CMOS image sensor decrease with downscaling technologies with fixed conversion gain. We assume that the conversion gain is not main effect of sensitivity charactersitics.

The effects of the reflection and extinction outside photodiode showed, also. We show the effect by thickness of insulator. From the results, long wave length does not effect outside photodiodes, since the absorption length is long. Meanwhile, short wave length, especially 400nm~500nm, is affected well, since absorption coefficient is low and absorption legnth is short.

On the other hand, we scaled effcet of an insulator layer using real parameter of the ASPLA 90nm process technology. In this process, about 20 layers, 6-metal layer, 5-via layer, pad-metal layer, pad-via layer, contact, and poly layer, locate above the silicon. Eventually, the multi-insulator layer have an large effect on sensitivity. In this 90nm process technology, the difference between non-multi insulator layer and multi-insulator layer was about 0.07 which is 7 times of the max value in multi-insulator layer.

Through measurement and scaling of sensitivity, we recognize the need to optimize the pixel circuit for a high sensitivity image sensor. Since sensitivity gets worse in short wave length of visible sight, we need to increase the sensitivity of photodiode by optimizing pixel configuration, as the future work. For perspective of CMOS image sensors, increasing sensitivity will be the one of key in advance tehnologies.

References

[1] *2007年　世界CCD/CMOSカメラ市場推移予測と分析*, Yano Research institute, June, 2005

[2] "A 640 X 512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC," *IEEE Journal of Solid-State Circuits*,, Vol.34, Np.12, Dec, 1999

[3] O. Yadid-Pecht and R. Etienne-Cummings, *CMOS Imagers: From Phototransduction to Image Processing* , KLUWER ACADEMIC Pub.

[4] I. Shcherback, and O. Yadid-Pecht, "Photodresponse Analysis and Pixel Shape Optimization for CMOS Active Pixel Sensor," *IEEE Transactions on Electron Devices*,, vol. 50, no.1, pp.12 - 18, 2003

[5] I. Shcherback, and O. Yadid-Pecht, "Prediction of CMOS APS Design Enabling Maximum Photoresponse for Scalable CMOS Technologies," *IEEE Transactions on Electron Devices*,, vol. 51, no.2, pp.285 - 288, 2004

[6] T. Danov, I. Shcherback, and O. Yadid-Pecht, "Study of CMOS APS Responsivity Enhancement: Ring-Shaped Photodiode," *IEEE Transactions on Electron Devices*,, vol. 52, no.1, pp.126 - 129 2005

[7] T. Lule, S. Benthien, H. Keller, F. Mutze, P. Rieve, K. Seibel, M. Sommer and M. Bohm, "Sensitivity of CMOS Based Imagers and Scaling Perspectives," *IEEE Transactions on Electron Devices*,, vol.47, no.11, pp.2110 - 2122, 2000

[8] S. Ito, S. Kawahito, H. Takashima, and M. Sakakibara, "Characteristics of CMOS Image sensor using a standard CMOS process technology," *ITE Technical Report*,, 2002, pp.69-73

[9] T. Yonemoto, "Application of CCD and CMOS image sensors," CQ Pub.

[10] W. C. Dash and R. Newman , "Intrinsic Optical Absorption in Single-Crystal Germanium and Silicon at 77 • and 300 • ," Physical Review, Vol.99, No.4, pp.1151~1155, 1955

[11] F. Odiot, J Bonnouvrier, C. Augier, J.M. Raynor, "Test stucture for Quantum Efficiency characterization for silicon image sensor," Microelectronic Test Structures, pp.3 - 33, 2003

[12] Y. Oike, M. Ikeda and K. Asada, "A 1024 X 768 High Speed and High Accuracy 3D Image sensor," *Proceedings of the 5th Biannual World Automation Congress (WAC)*, pp. 417 - 422, Jun. 2002.

[13] Y. Oike, M. Ikeda and K. Asada, "640 X 480 Real-Time Range Finder Using High-Speed Readout Scheme and Column-Parallel Position Detector," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*,, pp.153 -156, Jun. 2003

[14] C. Hu, A. Niknejad, X. Xi, W. Liu, X. Jin, K.M. Cao, M. Dunga, J. Ou,

BSIM4.5.0 Manual chap.10,http://www-device.eecs.berkeley.edu/ bsim3/get.html

[15] Sze. S. M., *Physics of Semiconductor Devices*, New York: Wiely, 1981.

[16] Hon-Sum P. Wong, "Technology and Device Scaling Consideration for CMOS Imagers," *IEEE Transactions on Electron Devices*,, Vol. 43, Issue 12, pp.2131 - 2142, Dec 1996

[17] Hon-Sum P. Wong, "CMOS Image Sensors - Recent Advances and Device Scaling Considerations," *International Electron Devices Meeting, Technical Digest.*,, Technical Digest., pp.201 - 204, 1997

[18] E. G. Stevens, B.C. Burkey, D.N. Nichols, Y.S. Yee, D.L. Losee, T-H. Lee, T.J. Tradwell, and R.P. Khosla, "A 1-Megapixel, Progressive-Scan Image Sensor with Antiblooming Control and Lag-Free Operation," *IEEE Transactions on Electron Devices*,, Vol. 38, No.5, pp.981 - 988, 1991

[19] J. del Alamo, S. Swirhun, and R. M. Swanson, "Simultaneous Measurement of Hole Lifetime, Hole Mobility and Bandgap Narrowing in Heavenly Doped n-Type Silicon", *International Electron Devices Meeting, Technical Digest.*,, Vol.32, pp.290 - 293, 1985.

[20] S. Swirhun, Y.-H. Kwark, and R. M. Swanson, "Measurement of electron lifetime, electron mobility, and band-gap narrowing in heavily doped P-Type Silicon", *International Electron Devices Meeting, Technical Digest.*,, Vol.32, pp.24, 1986.

[21] L. M. Terman, "Spectral Response of Solar Cell Structures", *Solid-State Electronics*, 2, 1, 1961.

[22] E.Palik, *Handbook of Optical Constants of Solid*, New York: Academic, 1985.

[23] Semiconduct. Ind. Assoc., "International Technology Roadmap for Semiconductors," 2003

[24] A. R. Forouhi, "Optical properties of crystalline semiconductors and dielectrics," Physical Review B, Vol. 38, No. 3, pp.1865-1874, July 1988.

[25] D. E. Aspnes and A. A. Studna, "Dielectric functions and optical parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV," Physical Review B, Vol. 27, No. 2, pp.985 - 1009, Jan 1983.

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1. Y. K. Kim, M. Ikeda, and K. Asada, "Sensitivity of CMOS Image Sensor and Scaling," *ITE Technical Report*, Sep. 2006. (Submitted)

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