Chapter 4

Measurement Results

4.1 Performance Evaluation

The fabricated chip is measured using T2000 logic tester, with 250MHz digital module using the open Architecture Test System Test Programming Language (OTPL) (Fig. 4.1). Measurement results reveal that the microcontroller functionally works correctly, and the waveform obtained from the logic tester is shown in Fig. 4.2. The microcontroller nicely demonstrates the two properties that we want to exploit in the design of microcontroller, namely the average-case performance and performance adaptation to the physical properties. From the measurement results, the microcontroller achieves an average speed performance of 23.3ns for evaluation time, and it needs 2.2ns for precharge time at nominal power supply voltage of 3.3V.

4.2 Average-Case Performance

The microcontroller senses when a computation has completed, allowing it to exhibit average-case performance regardless of propagation delay variations due to instruction dependency, data dependency and inter-chip variability.

4.2.1 Instruction Dependency

In the synchronous circuits, the circuits must be clocked to accommodate the longest evaluation time among its instruction set, resulting in worst-case performance. In contrast, the proposed microcontroller could sense when a computation has completed, allowing it to exhibit average-case performance. Fig. 4.3 and Fig. 4.4 show a portion of the instruction evaluation times of the microcontroller. As could be expected, the arithmetic and logical instructions possess a longer evaluation time if compared to the load instruction as shown

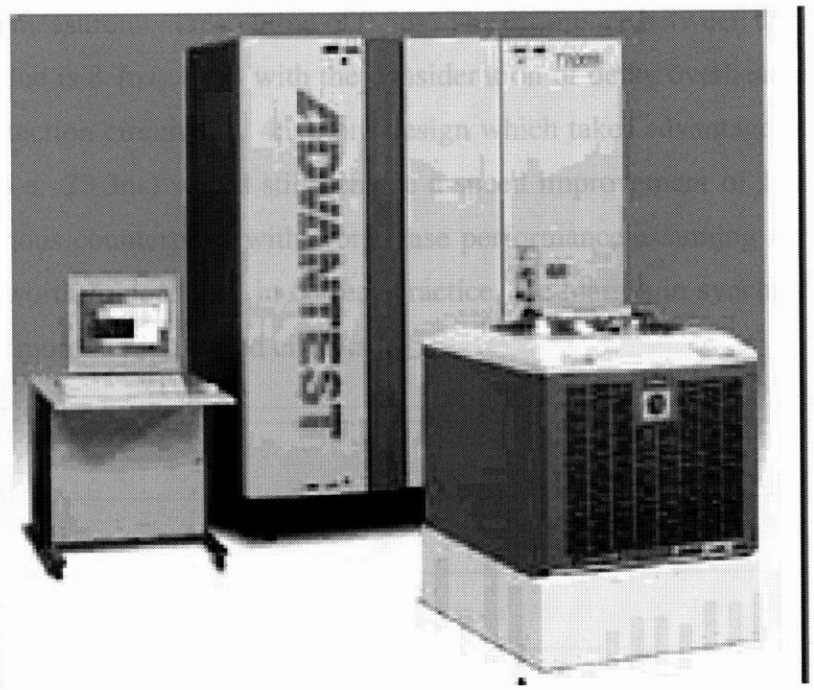

Fig. 4.1: T2000 with 250MHz digital module.

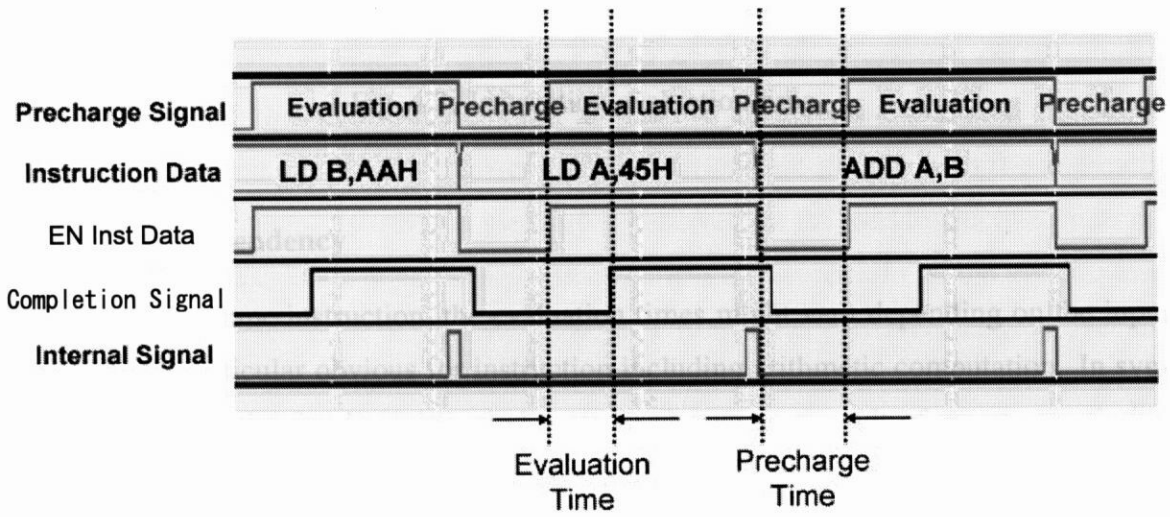

Fig. 4.2: Waveform result from logic tester.

in Fig. 4.4. The evaluation times vary depending on their respective computation paths, and are ranging from 14.5ns till 32.0ns with an average value at 23.3ns at power supply voltage of 3.3V with a measurement resolution of 0.5ns. The difference between the maximum and the average value is 8.7ns. Even with the consideration of delay overhead incurred in the completion detection circuit (i.e. 4ns), our design which takes advantage of average-case performance (i.e. 23.3ns) would still achieve a speed improvement of 17% if compared to its synchronous counterparts with worst-case performance assuming zero margin (i.e. 28.0ns). It is worth to note that, in current practice, the margin in synchronous design is often 100% or more in high-speed circuits [4].

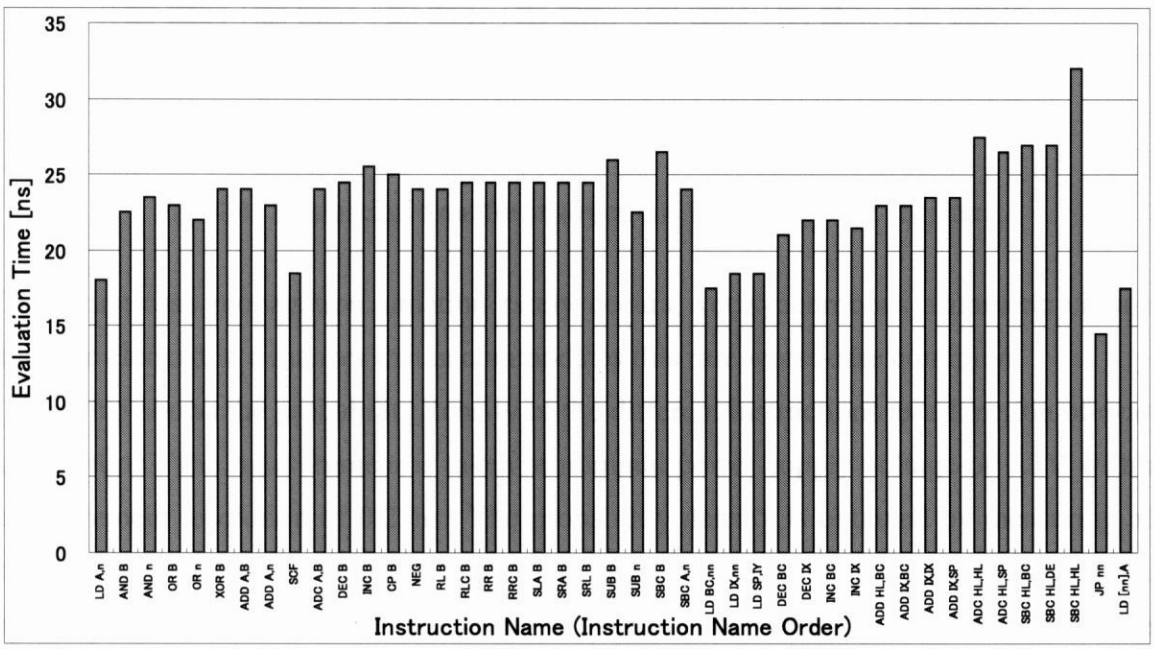

Fig. 4.3: Instruction evaluation time.

4.2.2 Data Dependency

Even for the same instruction, the evaluation times might vary depending on the input data. This is particular obvious for instruction including arithmetic computation. In synchronous circuit, the fixed clock period must be chosen as a result of worst-case timing analysis. It is not adaptive and therefore does not take advantage of average- or even best-case computational situations. Again, there is an opportunity for performance enhancement in the proposed microcontroller if the difference between the worst-case and average-case latencies is significant. Arithmetic circuits provide a good example. Arithmetic circuit performances are typically dominated by the propagation delay of carry or borrow signals.

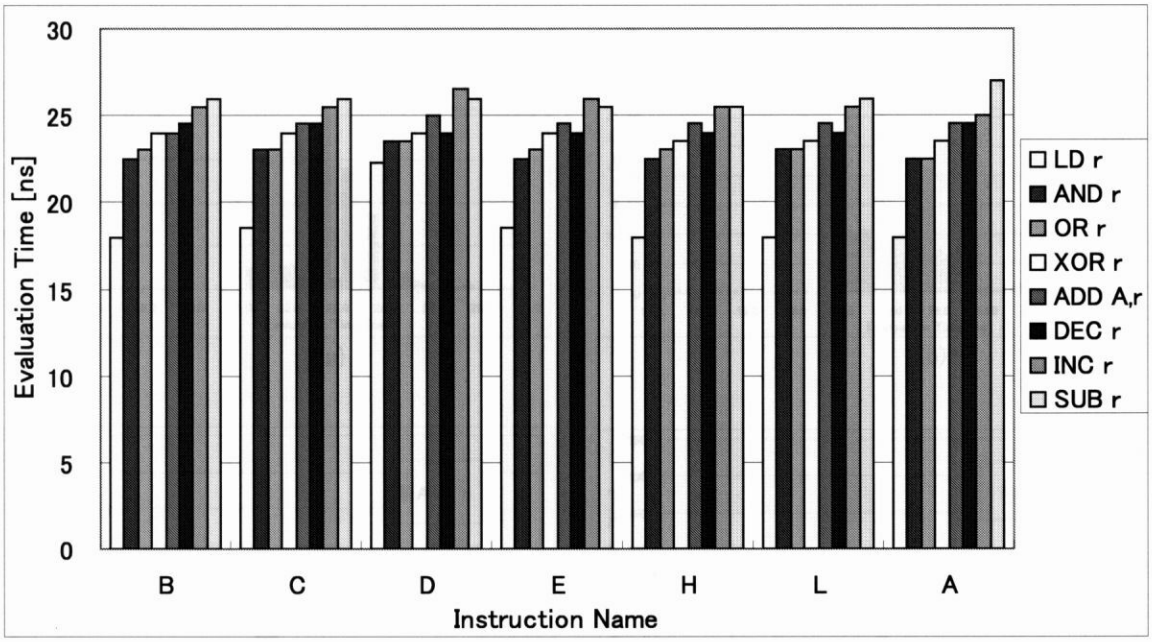

Fig. 4.4: Evaluation time for instructions involving 8-bit registers.

The worst-case propagation situation rarely occurs, yet synchronous arithmetic circuits must be clocked in a manner that accommodates this rare worst-case condition.

Fig. 4.5 shows the probability density of the different instructions as a function of evaluation time. The measurement is taken at nominal power supply voltage of 3.3V with a measurement resolution of 0.25ns. The probability density is obtained by measuring all the possible combination of input data. For example, a total of 65,536 input data combination is possible for instruction involving 8-bit register such as ADD A,n. From the figure, the arithmetic instruction such as addition (ADD A,n) or the subtraction (SUB n) has a broader evaluation time distribution if compared to the logical instruction such as AND or OR. It is interesting to note that the worst-case situations are rare for both the arithmetic and logical instructions. No obvious variance is observed for the load instruction, meaning that it is free from the data dependency. Measurement results reveal that the average-case performance achieves 1.17, 1.17, 1.02, 1.04, and 1.00 times performance gain over the worst-case performance with the addition (ADD A,n), subtraction (SUB n), AND (AND n), OR (OR n), and load (LD A,n) instruction, respectively (Table 4.1).

4.2.3 Inter-Chip Variability

The synchronous microcontroller's maximum clock frequency (FMAX) distribution is significantly influenced by the magnitude of critical path delay deviations resulting from

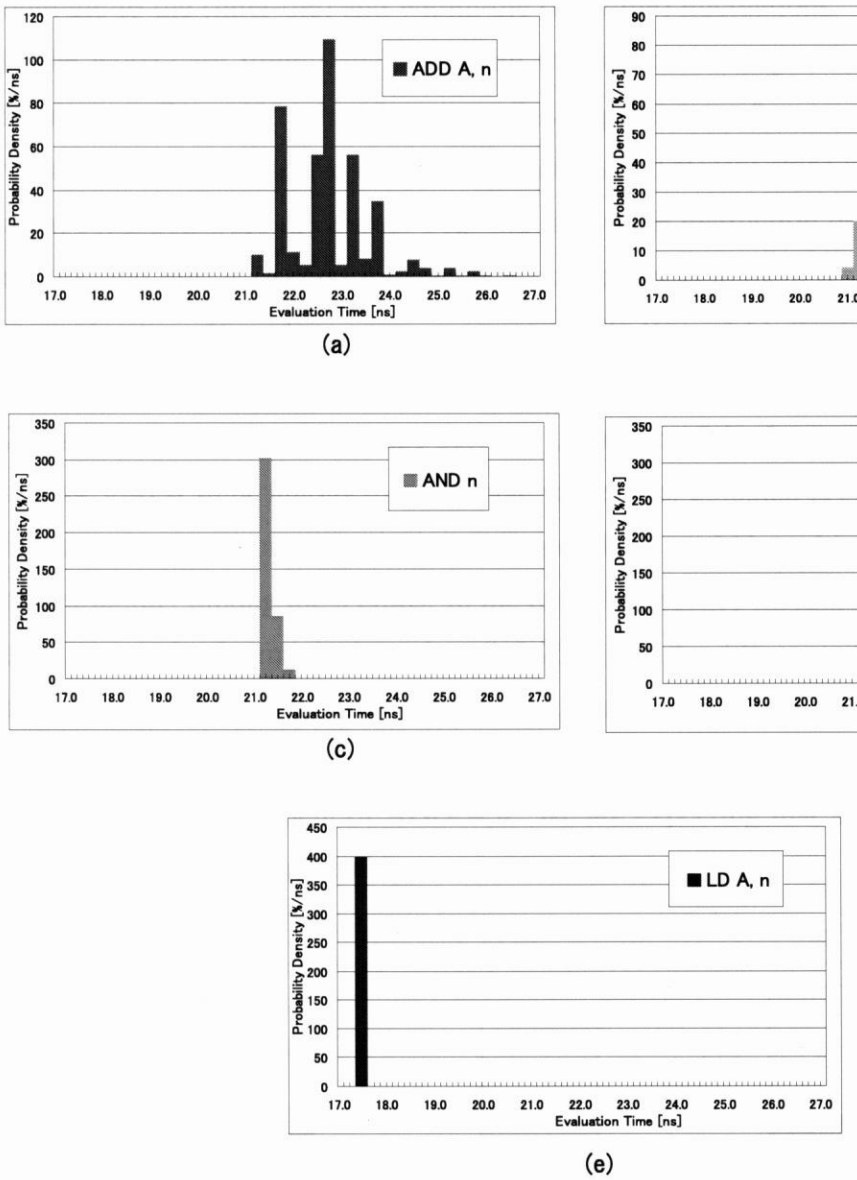

Fig. 4.5: Probability density of instructions due to data dependency.

Table 4.1: Measurement results due to data dependency.

Instruction Name	Evaluation Time [ns]			Ratio(=Max/Average)
	Min	Max	Average	
ADD A,n	21.25	26.50	22.68	1.17
SUB n	20.50	26.25	22.43	1.17
AND n	20.25	21.75	21.26	1.02
OR n	21.25	22.50	21.72	1.04
LD A,n	1.75	17.50	17.50	1.00

both die-to-die (inter-die) and within-die (intra-die) fluctuations. The FMAX must be set to the worst-case timing analysis of all the fabricated chips. In contrast, the proposed microcontroller could take advantage of average-case performance in the midst of all the variations. To evaluate the inter-chip variability, 3 different chips under the same measurement condition were measured. Fig. 4.6 shows the instruction dependency measurement results, and Fig. 4.7 shows the data dependency measurement results of ADD A,n. From the instruction dependency measurement results (Fig. 4.6), the largest difference among the maximum values is between chip-2 (i.e. 31.5ns) and chip-3 (i.e. 33.5ns), which is 2.0ns. In contrast, the difference between the mean of the 3 average values (i.e. 23.56ns) and the lowest value among the 3 average values (i.e. 23.03ns) is only 0.53ns. This implies that a performance improvement of 1.47ns or 4.4% could be achieved by only considering the variability among the 3 chips. In the data dependency measurement, the largest difference among the the maximum values is 1.25ns, and the difference between the mean of the average values and the lowest value among the average values is 0.45ns. In a similar way, we can conclude that a performance gain of 0.8ns or 2.9% could be achieved in the data dependency measurement of ADD A,n. We are expecting that a larger performance gain would be obtained if more chips are measured.

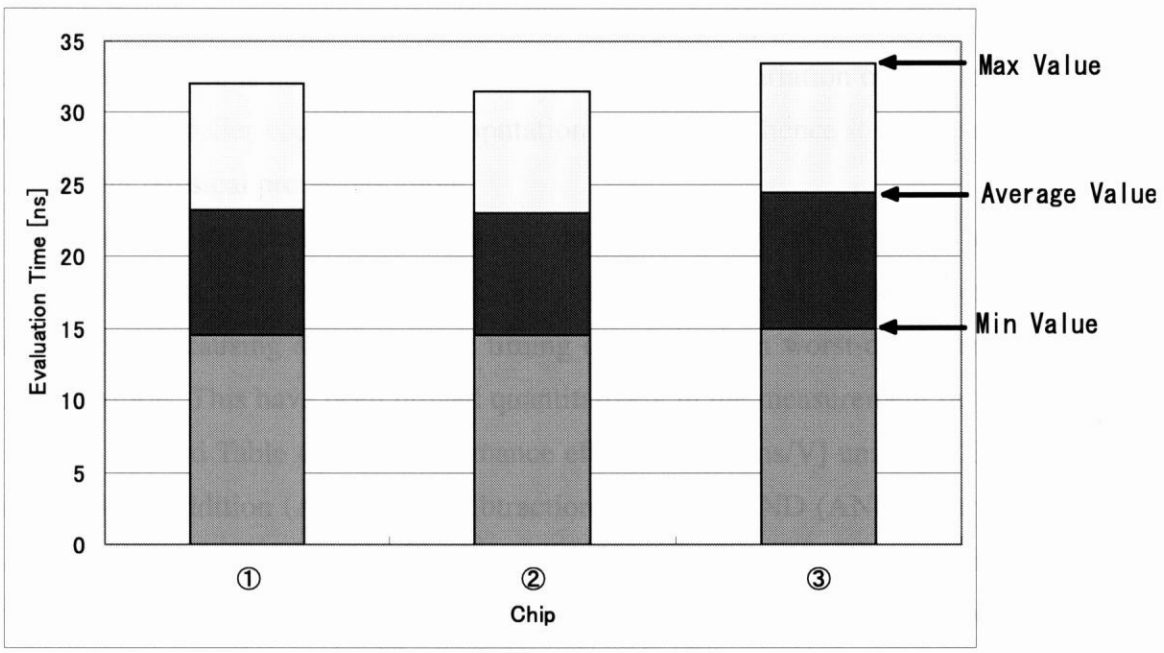

Fig. 4.6: Instruction dependency measurement in 3 different chips.

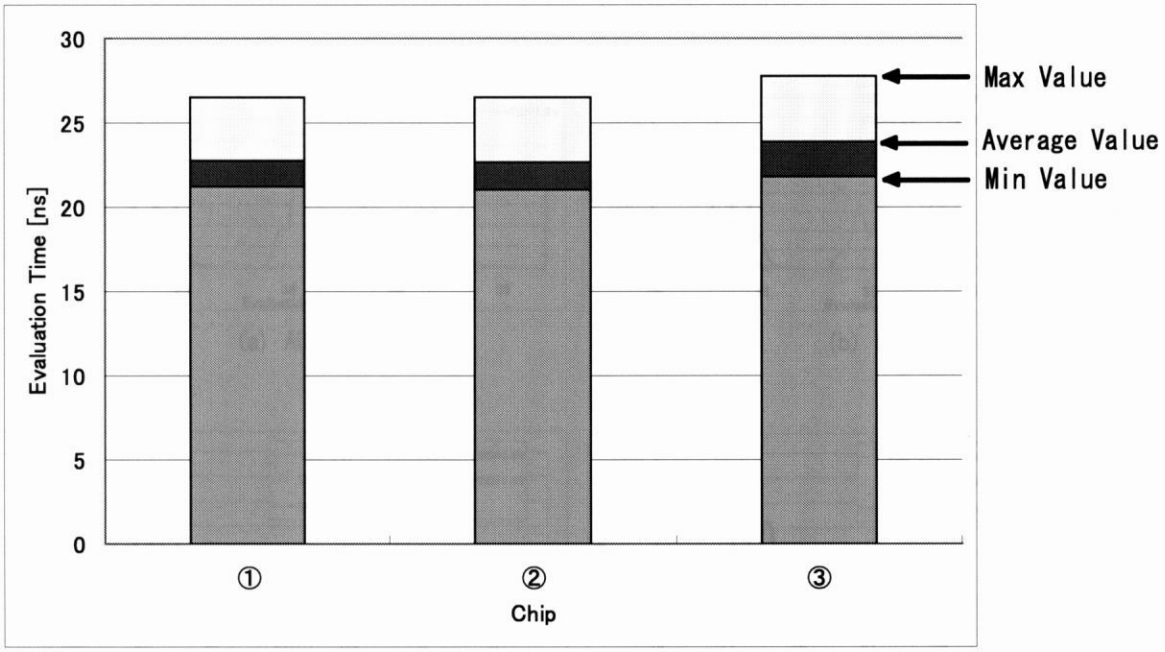

Fig. 4.7: Data dependency measurement of ADD A,n in 3 different chips.

4.3 Performance Adaptation

The performance adaptation property to the power supply voltage of the proposed microcontroller is shown in Fig. 4.8. It is easier to vary power supply voltage in the microcontroller, since there is no need to coordinate simultaneous variation of the clock frequency. The microcontroller could sense computation completion; hence it will run as quickly as the current physical properties allow.

As could be expected, the performance depends linearly on the power supply voltage (Fig. 4.9). Also, the performance variation increased rigorously as the power supply voltage is scaled, causing a more severe timing degradation in worst-case than the average-case situation. This have been proved quantitatively in the measurement results, as shown in Table 4.2 and Table 4.3. A performance efficiency (in [ns/V] unit) of 2.31, 1.99, 1.05, and 1.74 for addition (ADD A,n), subtraction (SUB n), AND (AND n), and OR (OR n) is achieved in average- if compared to worst-case timing analysis, respectively. We can hence conclude that the microcontroller with average-case performance would perform better than its synchronous counterparts when operating in low power supply voltage.

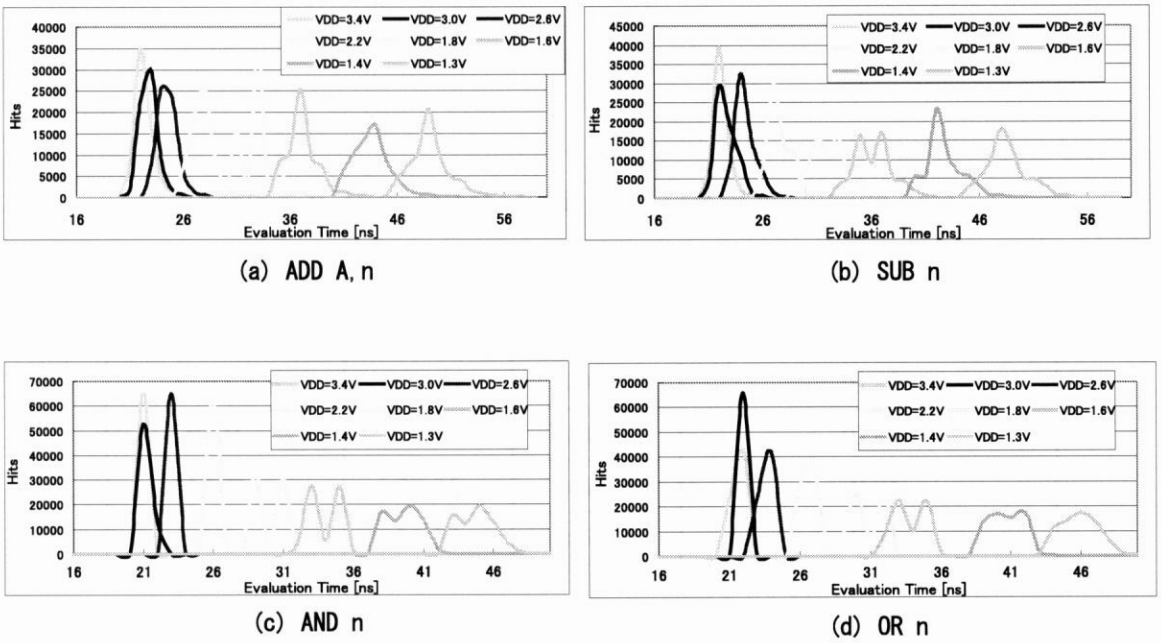

Fig. 4.8: Distribution curves of evalution time.

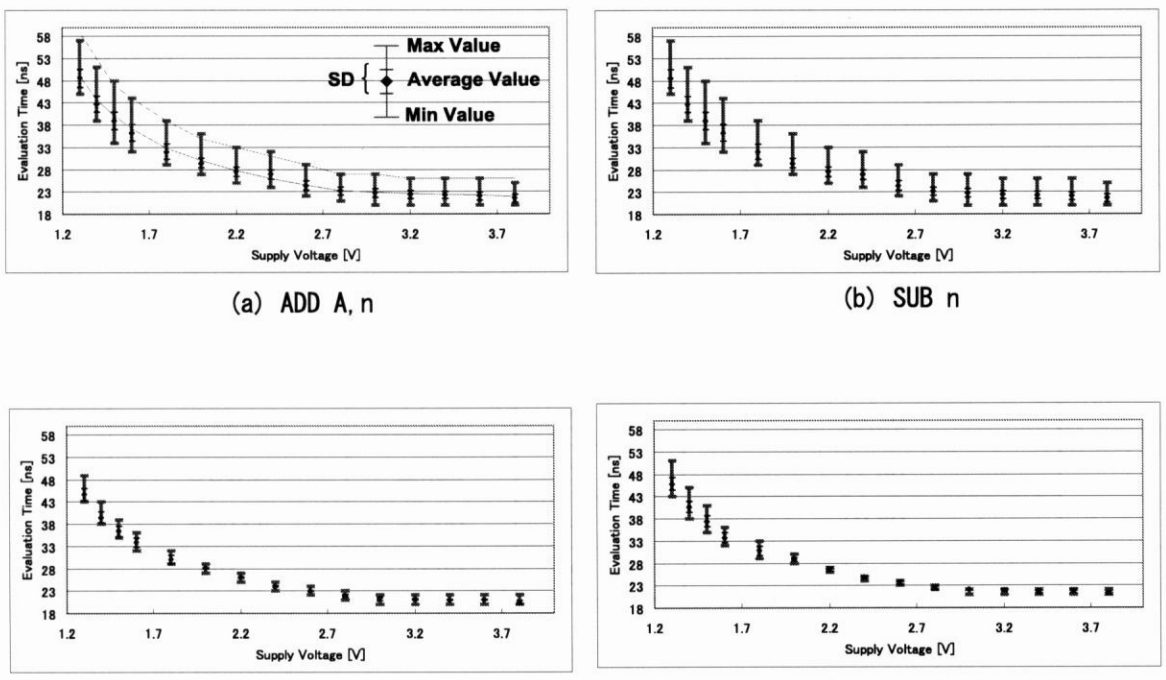

Fig. 4.9: Evaluation time as a function of power supply voltage.

Table 4.2: Average-case timing analysis of evaluation time.

Instruction Name	Evaluation Time [ns]		Ratio(Δ E.T./ Δ Vdd) [ns/V]
	Vdd@3.8V	Vdd@1.3V	
ADD A,n	21.90	49.12	10.89
SUB n	21.56	48.58	10.81
AND n	20.36	44.73	9.75
OR n	21.23	45.89	9.86

Table 4.3: Worst-case timing analysis of evaluation time.

Instruction Name	Evaluation Time [ns]		Ratio(Δ E.T./ Δ Vdd) [ns/V]
	Vdd@3.8V	Vdd@1.3V	
ADD A,n	26.00	59.00	13.20
SUB n	25.00	57.00	12.80
AND n	22.00	49.00	10.80
OR n	22.00	51.00	11.60