CHAPTER THREE

Fabrication of patterned SiO_2/GaAs substrates for selective growth

3.1 Introduction

The control of the positioning of the InAs/GaAs quantum dots (QDs) formation is of great importance for the fabrication of single photon emitters and for investigating solid-state cavity quantum electrodynamics phenomena. The Stranski-Krastanow (SK) growth mode is the most widely used approach for the fabrication of quantum dots, but it results in random positioning of the quantum dots. Several methods have been used to define the nucleation sites, and in particular those focused on the regrowth on nano-patterned substrates [26-46]. In this chapter, the fabrication of patterned SiO_2/GaAs substrates for selective growth is introduced. The patterning structure consists of a SiO_2 layer sputtered on a (100) GaAs substrate, in which a hole array is subsequently fabricated by electron beam lithography and wet etching processes. The hole diameter is ~100 nm.

3.2 Procedure of selective area growth

To fabricate the patterned SiO_2/GaAs substrates, many procedures are required as shown in Fig.3-1. These experiments were carried out by the following procedure:

1. Sputtering: Deposition of SiO_2 on GaAs substrates by sputtering system. The thickness of SiO_2 is about 20nm. (Fig.3-1(a))
2. Resist: Spin-coating pf resist on the sample surface. (Fig.3-1(b))
3. EB: Fabrication of patterns onto resist using electron beam lithography system.(EB) (Fig.3-1(c))

4. Development: Developing to transfer patterns into resist layer. (Fig.3-1(d))
5. Wet etching: Transfer of patterns into SiO_2 mask using wet etching. (Fig.3-1(e))
6. Removal of resist: Removing resist on the SiO_2 mask completely. (Fig.3-1 (f))

Specific explanations and optimizations of these procedures will be introduced as follows.

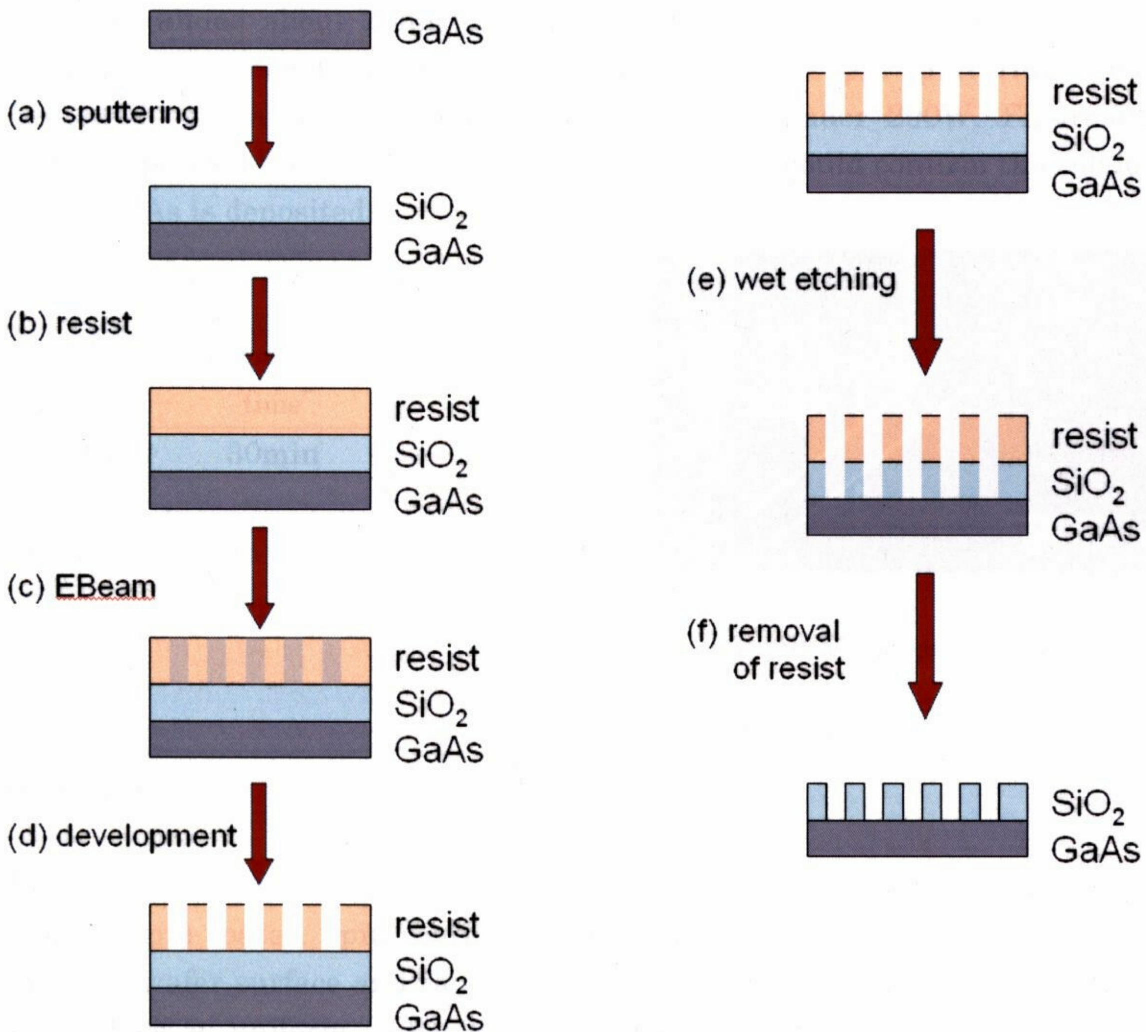


Fig.3-1 schemes of procedures for fabrication of patterned substrates

(a) Sputtering

First, we deposited SiO_2 onto a GaAs substrate using sputtering system. We prepared a (100) GaAs substrate which had cleaned up with Acetone and Methanol using ultrasonic. Putting the sample inside sputtering system, we evacuated the system with a pump until the pressure reached ~10^{-4}Torr. Then we generated the plasma of SiO_2 under high voltage acceleration. The main factors which determine the thickness and quality of deposited SiO_2 are RF power and pre-sputtering time. The growth rate of SiO_2 is increased with increasing RF power. And pre-sputtering which refers to the plasma exposure before sputtering, enable to stabilize the condition of deposition. Since we aimed about 20nm thick SiO_2 deposition, we selected sputtering conditions as shown in Table.3-1. After 30 minute pre-sputtering, SiO_2 deposited onto a GaAs substrate for 2 minutes under 200W. Figure.3-2 shows deposited SiO2 mask on GaAs substrate. We could confirm that about 20nm GaAs is deposited.

RF power	Pre-sputtering time	Sputtering time
200W	30min	2min

Table.3-1 Growth conditions of sputtering

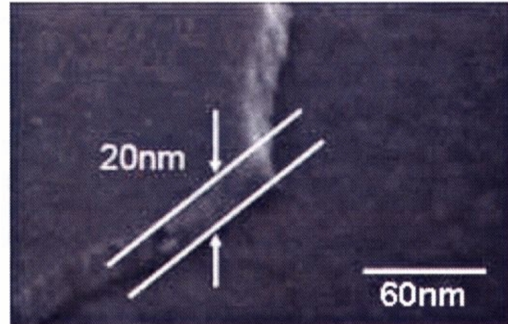


Fig.3-2 SEM image of SiO2 mask.

(b) Resist

Resist was coated over the surface of a SiO_2/GaAs substrate homogeneously using a spin coater. Spin coating consists of dispensing the resist solution over the wafer surface and rapidly spinning the wafer until it becomes dry. It enables a uniform, adherent, and defect-free resist film of correct thickness over the wafer. In this study, we used ZEP520 (ZEON corporation) as a resist solution. ZEP520 is a positive-tone electron-beam resist with comparable resolution to polymethylmethacrylate (PMMA).

It is composed of alternating copolymer of α-chloromethacrylate and α-methylstyrene as shown in Fig.3-3(a). It improves sensitivity and etch resistance compared with PMMA and thus has been widely used for device fabrication. On the other hand, ZEP520 has a disadvantage of poor adhesion. In the process of wet etching which refers to the SiO_2 etching process, we found that we could not transfer the patterns onto SiO_2 without pre-priming process. Hence we added pre-priming process before spin coating for enhancing the adhesion properties. Pre-priming process was performed by evaporation. A few drops of primer solution were deposited onto the SiO_2/GaAs substrate under the high temperature. As a primer, we used HMDS which ties up the molecular water on a hydroxylated silicon dioxide surface with a portion of the complex molecule and bonds the ends of the resist molecule with the other portion of the HMDS molecule as shown in Fig.3-3(b).

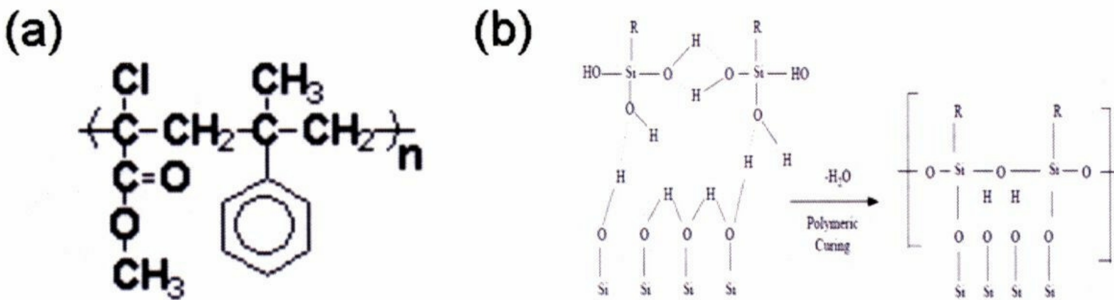


Fig.3-3 (a) Formula of ZEP520 (b) Schematic reaction of HMDS

After pre-priming, spin coating was subsequently carried out using ZEP520. We dropped 2 or 3 drops of ZEP520 over the wafer surface, and then rotated the wafer rapidly. Specific spinning condition was 500 rpm for 10s followed by 6000 rpm for 60s. Finally, the sample was baked at 190°C for 4 minutes in order to:

1) drive away the solvent from the spun-on resist
2) improve the adhesion of the resist to the wafer
3) anneal the shear stresses introduced during the spin-coating.

(c) Electron Beam lithography

After a wafer has been coated with resist and subjected to soft baking, it has to undergo exposure that will produce the pattern image on the resist. To make pattern on the resist, we used Electron Beam Lithography (EB) which refers to a lithographic process that uses a focused beam of electrons to form the circuit patterns in contrast with optical lithography which uses light for the same purpose. Electron lithography offers higher patterning resolution than optical lithography because of the shorter wavelength possessed by the 10-50 keV electrons that it employs. First, we designed the pattern with CAD and the designed structure is subsequently patterned onto the sample according to a computer controlled signal on the scan coils. Figure.3-4 shows the schematic illustration of the designed pattern and Table.3-2 shows the parameters of them. It was decided considering the combination with photonic crystals after InAs QD growth in the future. As introduced in chapter.1, photonic crystals lead to high efficient single photon emitters.

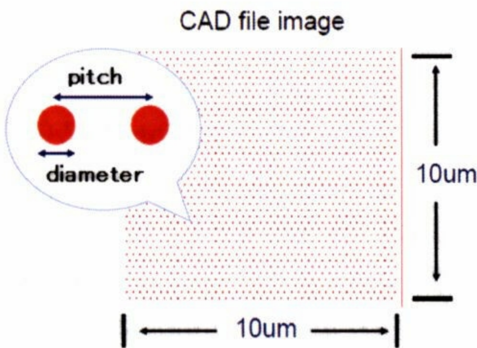


Fig.3-4 Schematic illustration of the pattern

	diameter	pitch
Design (1)	60nm	280nm
Design (2)	60nm	340nm

Table.3-2 Parameters of designed patterns

(d) Development

Development, which is the process step that follows resist exposure, was done to transfer the designed pattern into resist. The patterned area which was attacked by electron beam got dissolved in the developer. In this study, we used ZEP-N50 and ZMD-B as developing solution and rinse solution, respectively. We should make sure that the designed patterns can be transferred into resist with good accuracy. Otherwise we cannot transfer the designed patterns into SiO_2 mask pattern. By optimizing the developing

temperature and developing time as 20°C and 140s, we could transfer the patterns precisely. The diameter of patterned holes became about 90nm. The cross-sectional SEM image of pattern-transferred resist sample is shown in Fig.3-5(b).

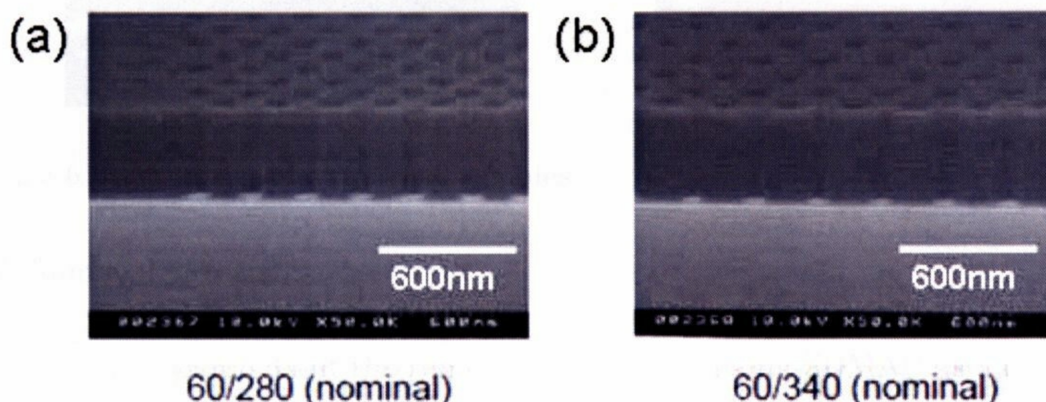
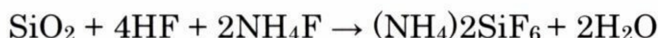


Fig.3-5 SEM images of developed samples. (a) 60/280 (nominal diameter/pitch) (b) 60/340

(e) Wet etching

Next, we transferred the designed patterns into SiO_2 mask using BHF solution. BHF (Buffered Hydrogen Fluoride) solution is made by adding NH_4F to HF solution. Adding NH_4F to HF solution enables to control the pH value, and to replenish the depletion of the fluoride ions to maintain stable etching performance. For BHF etching, the overall reaction is:



$$SiO_2 + 4HF + 2NH_4F \rightarrow (NH_4)2SiF_6 + 2H_2O$$

Since we had only 20nm thick SiO_2, we diluted BHF solution by 4 times of water and cooled down to the 0°C to decrease the etching rate. Then we put the sample into the solution for 50s and washed with large amount of water. Figure.3-6 shows the SEM images of wet-etched samples. We could confirm that the diameters of top and bottom of SiO_2 are different because etching advanced isotropically.

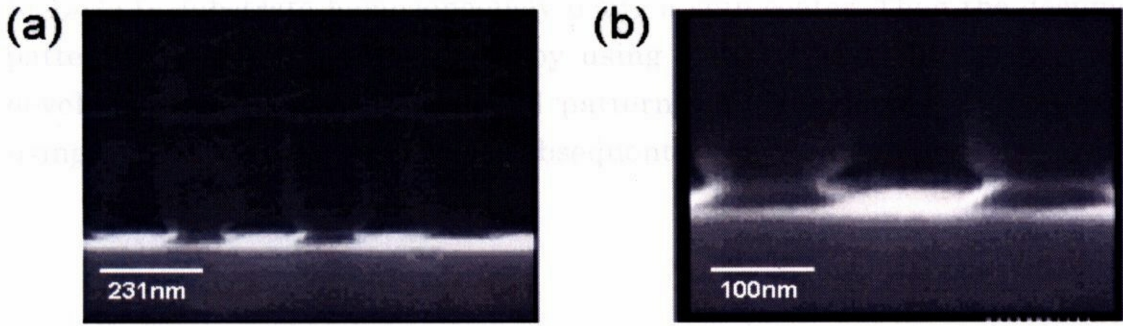


Fig.3-6 SEM images of wet etched samples

(f) Removal of resist

Finally, we carried out the removal of resist by using ZDMAC as a remover. All the resist got dissolved into the remover. In order to make sure that there would be no resist on the SiO2, we put the samples into the ZDMAC for one night. The SEM image of the sample after removal of resist is shown in Fig.3-7. GaAs exposed holes are observed clearly.

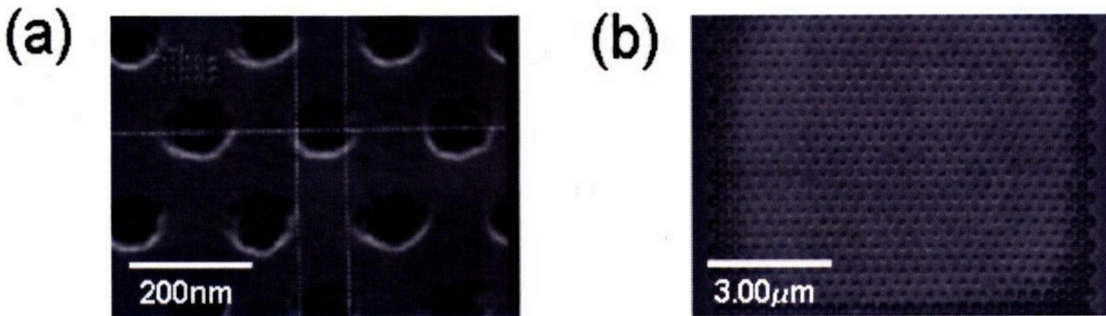


Fig.3-6 SEM images of the sample after removal of resist

3.3 Conclusion remarks

In this chapter, the fabrication of patterned SiO_2/GaAs substrates for selective growth was introduced. First, SiO_2 mask was deposited by using sputtering system. After sputtering, resist was coated over the surface of a

SiO_2/GaAs substrate homogeneously using a spin coater. Then the designed pattern was transferred to resist by using electron beam lithography and development. Finally, the designed pattern was transferred to SiO_2 mask using wet etching and resist was subsequently removed by removal.