Chapter 5

Proposed Circuit Design Techniques to Improve the Noise Margins of the Dual-Rail PLA

Techniques to improve the noise margin of the dual-rail PLA are proposed in this chapter.

5.1 A One-Side Virtual Ground Structure (1-side VG)

To enlarge the noise margins of the dual-rail PLA, we propose a one-side virtual ground (1-side VG) structure, which is showed as Figure 5.1. The voltage of *BL* remains as Vdd when all the input signals are low, or is pulled down to ground level when at least one of the input signals is high because *BL* is directly connected to ground through logic cells, and the voltage of $\overline{BL}$ is always pulled down to about Vdd/2 by charge sharing with VG through a reference cell. This scheme enlarges Vdiff and thus improves the noise margins of the dual-rail PLA. Figure 5.2 shows the variations of Vdiff of the 1-side VG structure with one input when input=1 and input=0 along with process scaling. Compared to Figure 4.6, one can see that Vdiff is enlarged, which means noise margins are improved. Note that Vdiff decreases gradually in time at 32nm process due to large leakage current.

Figure 5.3 gives the profiles of Voff and Vdiff of the 1-side VG PLA when input=1 and input=0. They are histograms with an interval of 5mV. Vdiff is measured at 300ps. For both cases, the space between the Voff and Vdiff profiles is enlarged, which means the noise margin is improved.

The trend of noise margins of the 1-side VG dual-rail PLA for both input=1 and input=, with and without Vdd noise is shown in Figure 5.4. Vdiff is measured at 300ps. Compared to Figure 4.7 and Figure 3.11, a 1-side VG dual-rail PLA not only increases the noise margins

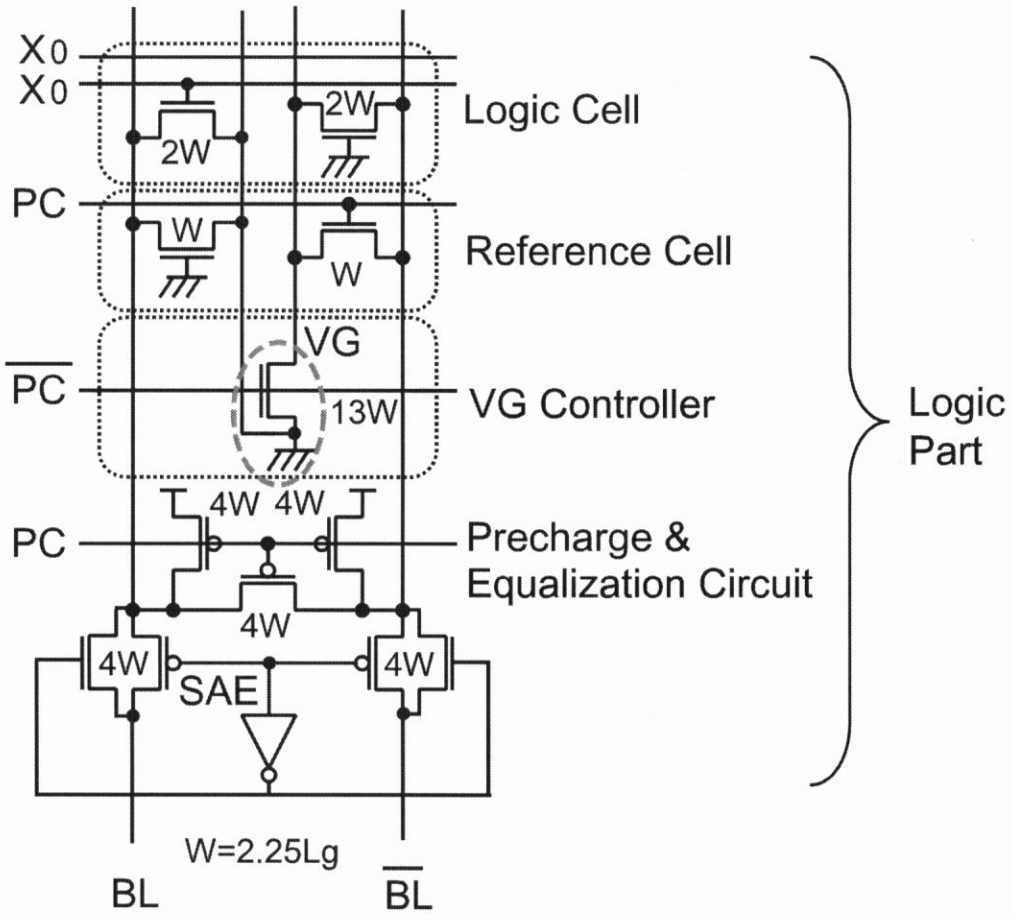
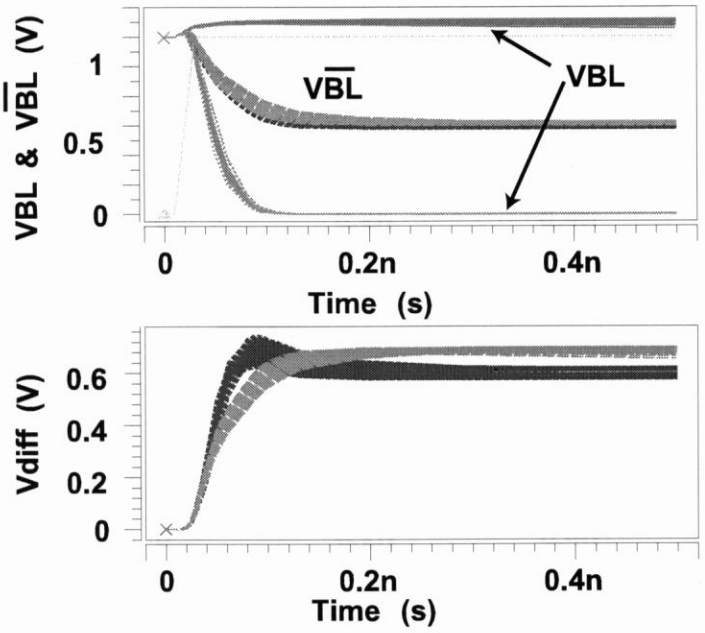
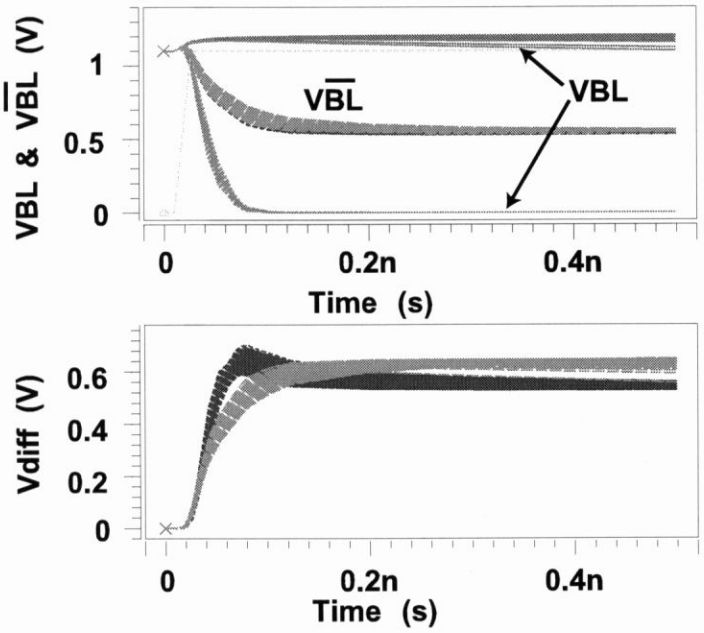


Figure 5.1 A one-side virtual ground structure proposed in this paper to enlarge the differential voltage generated between bit lines to improve the noise margins of the dual-rail PLA (Figure 4.1)

of the original dual-rail PLA, but also has larger noise margins than those of the random CMOS at each process, which means this improved PLA works more reliably along with process scaling.


VBL & $\overline{VBL}$ (V)
1
0.5
0
$\overline{VBL}$
VBL
0
0.2n
0.4n
Time (s)
Vdiff (V)
0.6
0.4
0.2
0
0
0.2n
0.4n
Time (s)

90nm


VBL & $\overline{VBL}$ (V)
1
0.5
0
$\overline{VBL}$
VBL
0
0.2n
0.4n
Time (s)
Vdiff (V)
0.6
0.4
0.2
0
0
0.2n
0.4n
Time (s)

65nm

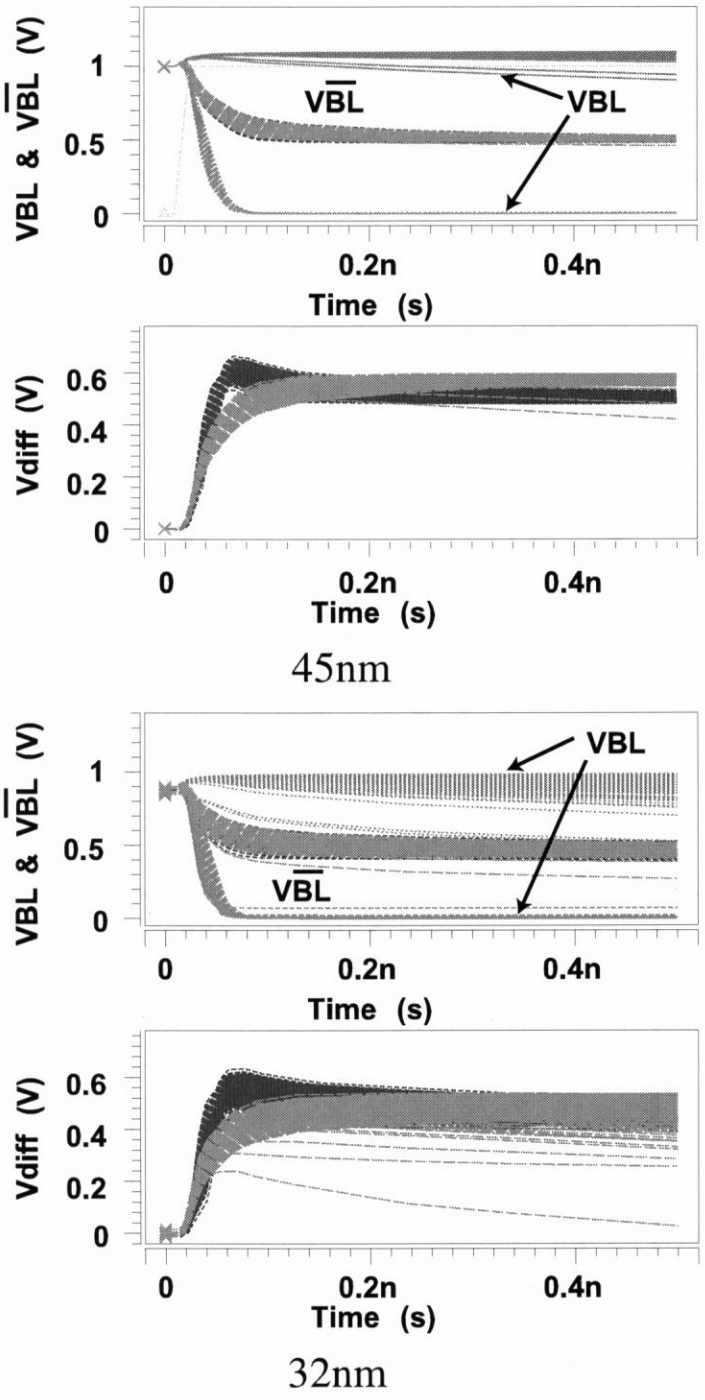
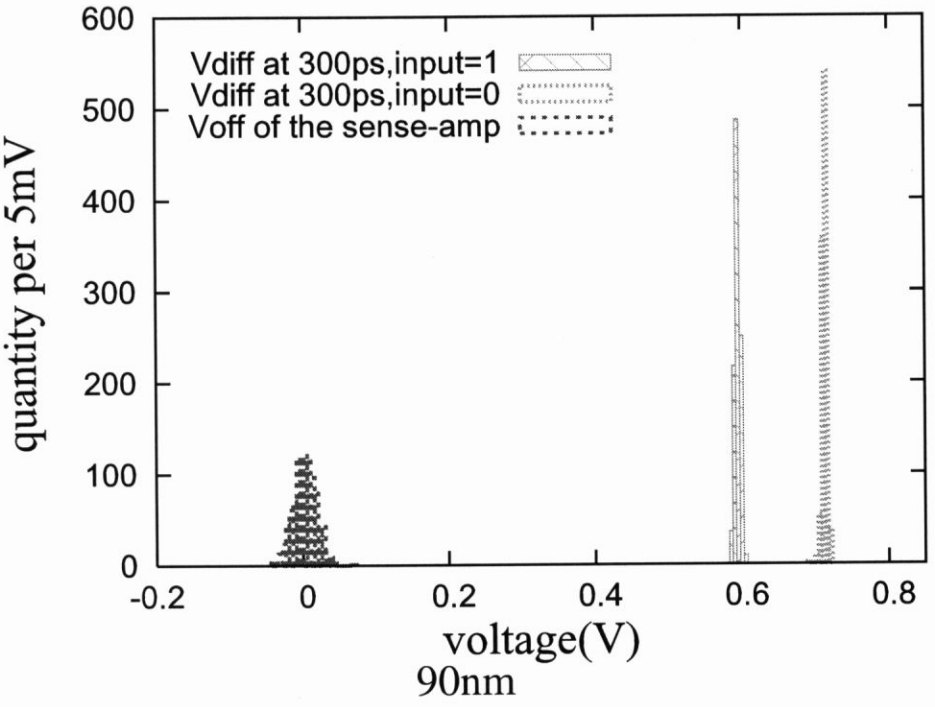
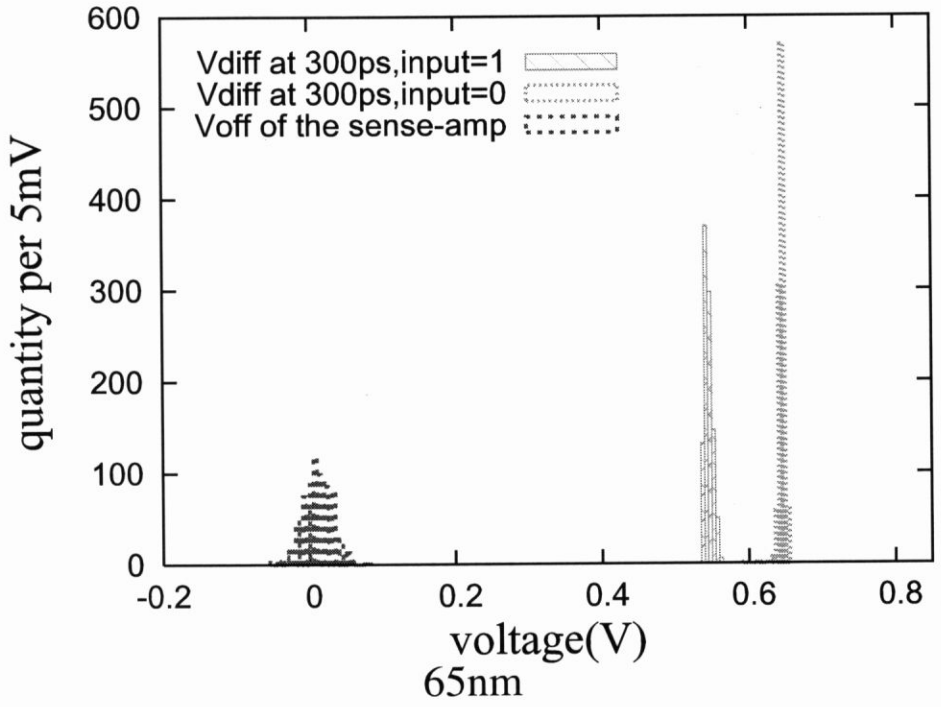


Figure 5.2 Variations of Vdiff of the one-side virtual ground structure with 1 input (Figure 5.1). Of each process, the upper graph shows the voltage potential of BL and $\overline{BL}$ (V_{BL}=Vdd when input=0 or V_{BL}=0 when input=1, because BL is directly connected to ground through a logic cell, and $V_{\overline{BL}}$ is always pulled down to about Vdd/2 by charge sharing with VG through a reference cell.). The lower graph shows Vdiff: $V_{\overline{BL}} - V_{BL}$ for input=1 and $V_{BL} - V_{\overline{BL}}$ for input=0


Vdiff at 300ps,input=1
Vdiff at 300ps,input=0
Voff of the sense-amp
quantity per 5mV
voltage(V)
600
500
400
300
200
100
0
-0.2
0
0.2
0.4
0.6
0.8

90nm


Vdiff at 300ps,input=1
Vdiff at 300ps,input=0
Voff of the sense-amp
quantity per 5mV
voltage(V)
600
500
400
300
200
100
0
-0.2
0
0.2
0.4
0.6
0.8

65nm

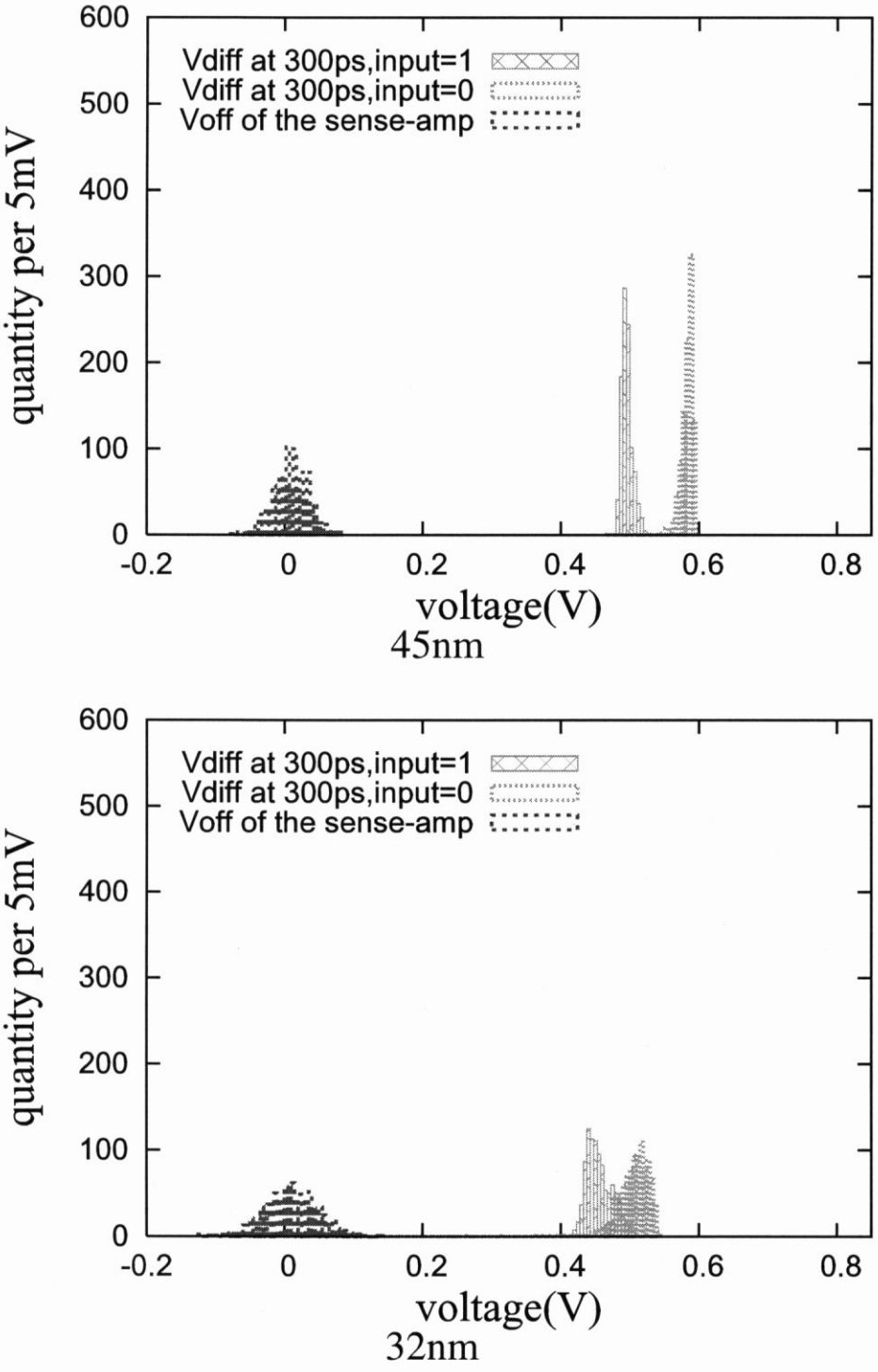


Figure 5.3 The profiles of Voff and Vdiff of the 1-side VG PLA when input=1 and input=0. They are histograms with an interval of 5mV. Vdiff is measured at 300ps. For both cases, the space between the Voff and Vdiff profiles is enlarged, which means the noise margin is improved.

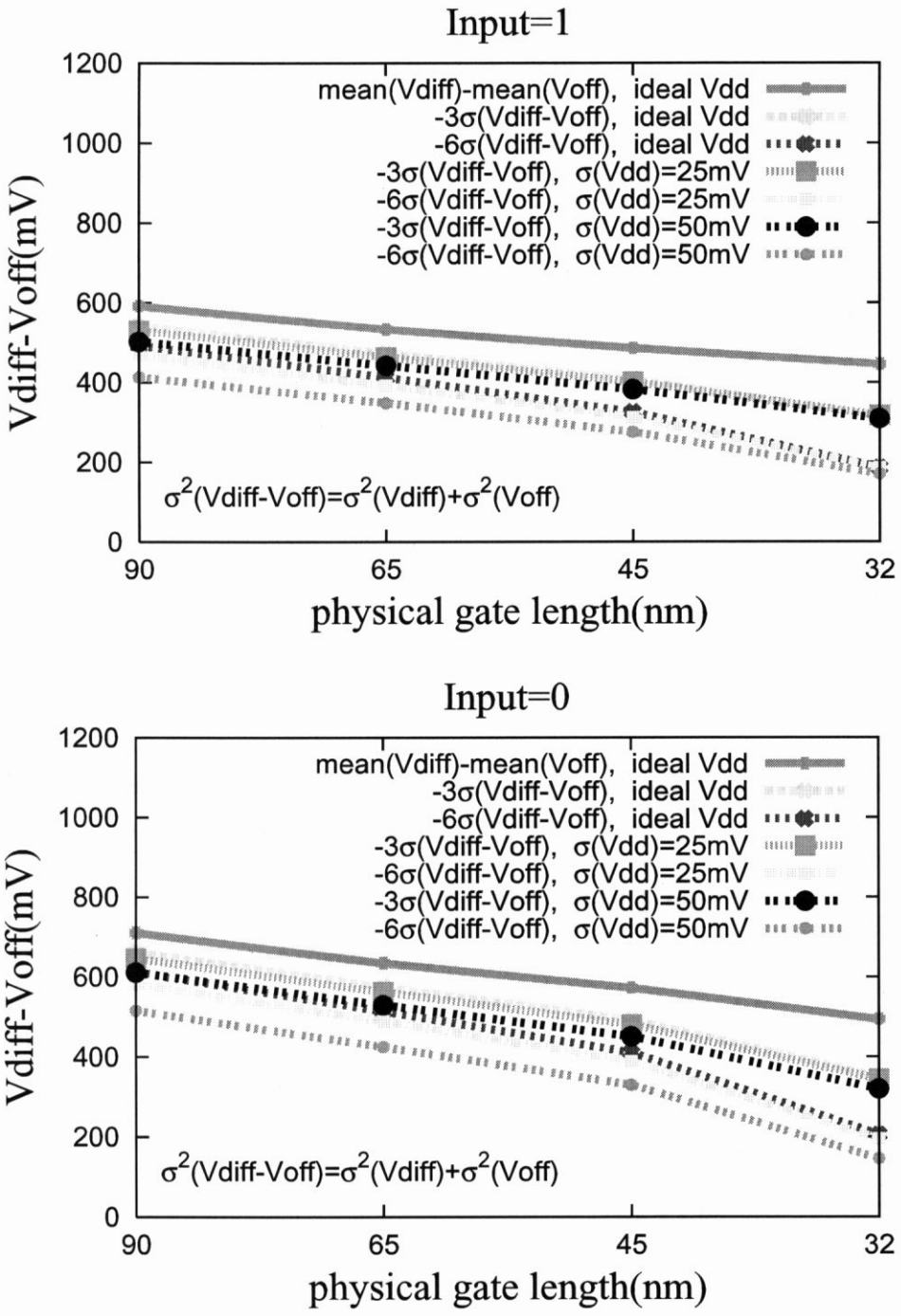


Figure 5.4 The trend of noise margins of the 1-side VG dual-rail PLA. Vdiff is measured at 300ps. Compared to Figure 4.7 and Figure 3.11, a 1-side VG dual-rail PLA not only increases the noise margins of the original dual-rail PLA, but also has larger noise margins than those of the random CMOS at each process, which means this improved PLA works more reliably along with process scaling.

5.2 An Input Offset Voltage Canceling Sense Amplifier

To further increase the noise margins of the dual-rail PLA, we propose input offset voltage canceling technique to suppress the variation of Voff of the sense-amp. Figure 5.5 shows a conventional input offset voltage canceling sense-amp [20]. The operations are as follows

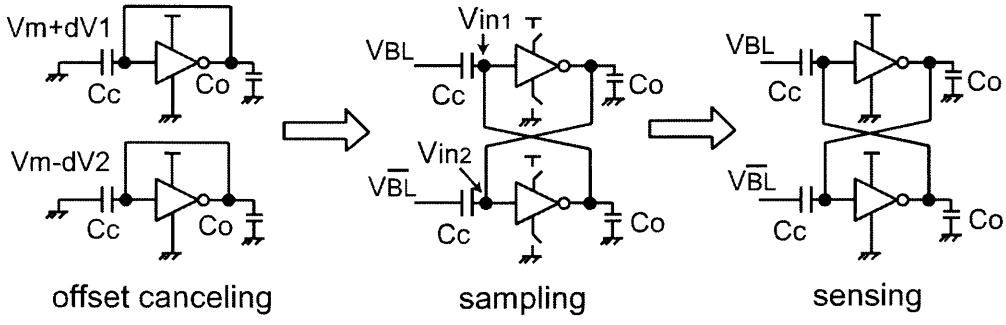


Figure 5.5 Conventional input offset voltage canceling sense-amp [20]

- offset canceling: Inputs and outputs of the 2 INVs are shorted. Hence the switching threshold of each INV is stored in each coupling capacitor (Cc).
- sampling: Inputs and outputs of the 2 INVs are crossed and the 2 INVs are separated from Vdd and Gnd. Meanwhile, input signals can be sampled.
- sensing: The 2 INVs are connected back to Vdd and Gnd. Input signals are amplified.

According to redistribution of charge, the following equations can be listed:

$$\begin{aligned}
V_{in1} - V_{BL} &= (V_m + dV_1)\frac{Cc}{Cc+Co} + (V_m - dV_2)\frac{Co}{Cc+Co} \\
V_{in2} - V_{\overline{BL}} &= (V_m - dV_2)\frac{Cc}{Cc+Co} + (V_m + dV_1)\frac{Co}{Cc+Co} \\
suppose\ V_{BL} &= V_{\overline{BL}} \\
then\ \Delta V_{in} &= V_{in1} - V_{in2} = (dV_1 + dV_2)(\frac{Cc-Co}{Cc+Co}) \\
define\ V_{off} &= V_m + dV_1 - (V_m - dV_2) = dV_1 + dV_2, \\
and \quad x &= \frac{Cc}{Co} \\
we\ get\ \frac{\Delta V_{in}}{V_{off}} &= \frac{x-1}{x+1}
\end{aligned} \tag{5.1}$$

Voff is the input offset voltage of sense-amp and ΔV_{in} is the amount of how much input offset voltage can be canceled. Therefore, Eq. (5.1) indicates the ability to cancel the input offset voltage, which depends on Cc/Co.

Based on the above discussion, we propose an improved input offset voltage canceling sense-amp as shown in Figure 5.6. The difference to the conventional one is that after the switching threshold of each INV is stored in each Cc, the two outputs of the INVs are connected to equalize the voltage potential before crossing the inputs and outputs. Again, according to the redistribution of charge, the following equations can be listed:

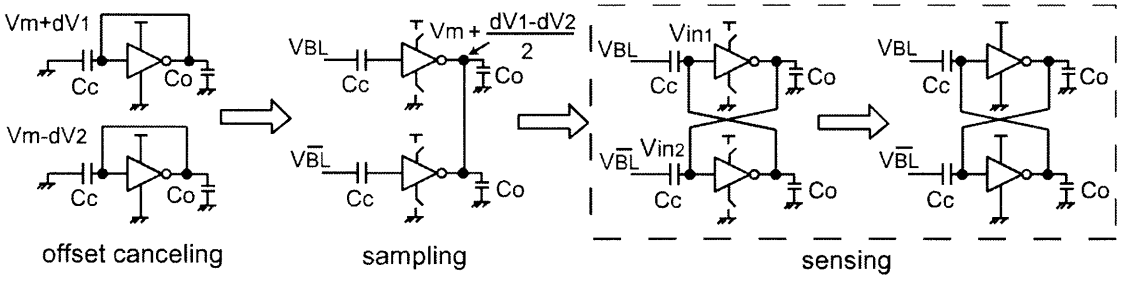


Figure 5.6 Proposed input offset voltage canceling sense-amp

$$
\begin{aligned}
V_{in1} - V_{BL} &= (V_m + dV_1)\frac{Cc}{Cc+Co} + (V_m + \frac{dV_1 - dV_2}{2})\frac{Co}{Cc+Co} \\
V_{in2} - V_{\overline{BL}} &= (V_m - dV_2)\frac{Cc}{Cc+Co} + (V_m + \frac{dV_1 - dV_2}{2})\frac{Co}{Cc+Co} \\
suppose\ V_{BL} &= V_{\overline{BL}} \\
then\ \Delta V_{in} &= V_{in1} - V_{in2} = (dV_1 + dV_2)(\frac{Cc}{Cc+Co}) \\
define\ V_{off} &= V_m + dV_1 - (V_m - dV_2) = dV_1 + dV_2, \\
and\quad x &= \frac{Cc}{Co} \\
we\ get\ \frac{\Delta V_{in}}{V_{off}} &= \frac{x}{x+1}
\end{aligned}
\tag{5.2}
$$

Eq. (5.1) and Eq. (5.2) are plotted in Figure 5.7. From it one can understand that Eq. (5.2) cancels Voff better than Eq. (5.1) for the same Cc/Co. Actually the value of Cc itself impacts how much voltage can be transfered through it, which is showed in Figure 5.8. Hence, Cc should be decided as

$$Cc = max(xCo, Cc_{min}) \tag{5.3}$$

In this experiment, $Co = 5Cinv$, where $Cinv$ is the input capacitance of the inverter in Chapter 3. If 90% offset canceling and 80% voltage transfer ability are required, from Eq. (5.2) we get x=9 and from Figure 5.8 we get the minimum value of Cc. At last from Eq. (5.3) Cc can be calculated. From 90nm to 32nm, $Cc = 90fF, 51fF, 35fF$ and $25fF$, respectively.

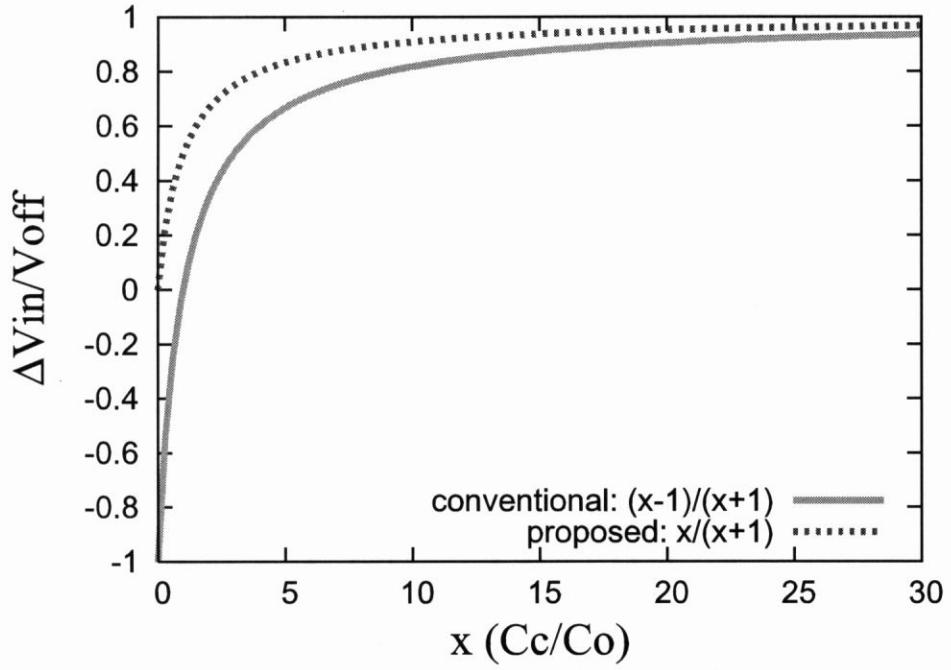


Figure 5.7 Offset canceling comparison. The proposed offset canceling sense-amp cancels Voff better than the conventional one.

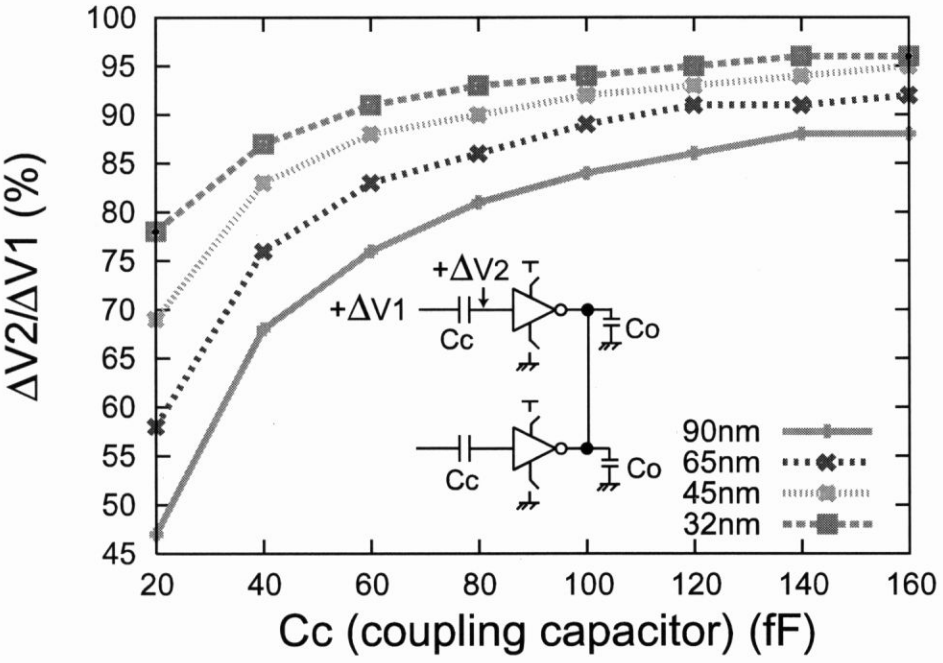


Figure 5.8 Voltage transfer ability. The value of coupling capacitor (Cc) impacts how much voltage can be transfered through it.

Figure 5.9 shows the transistor structure. Cc is implemented by transistors, which means variations of Cc are introduced by variations of transistors.

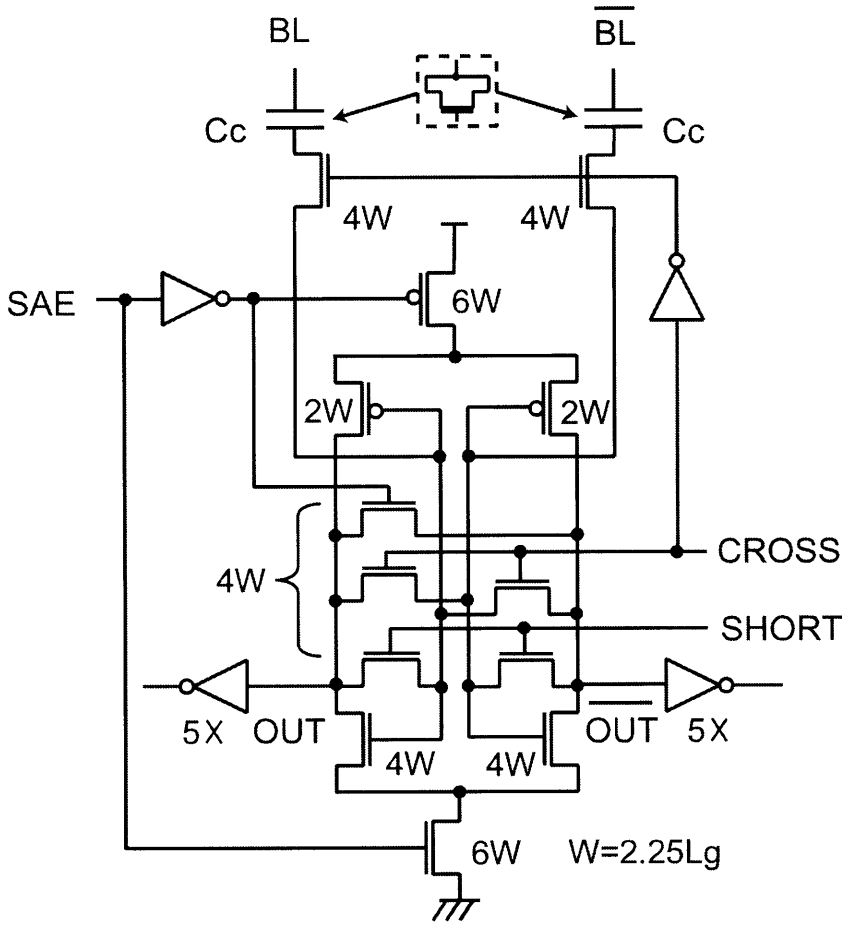
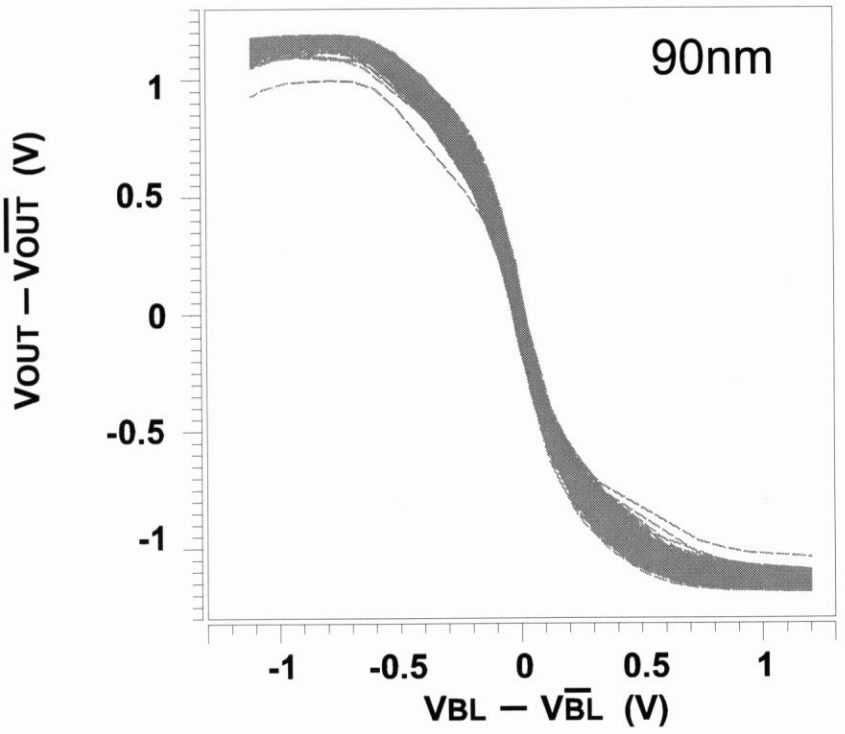
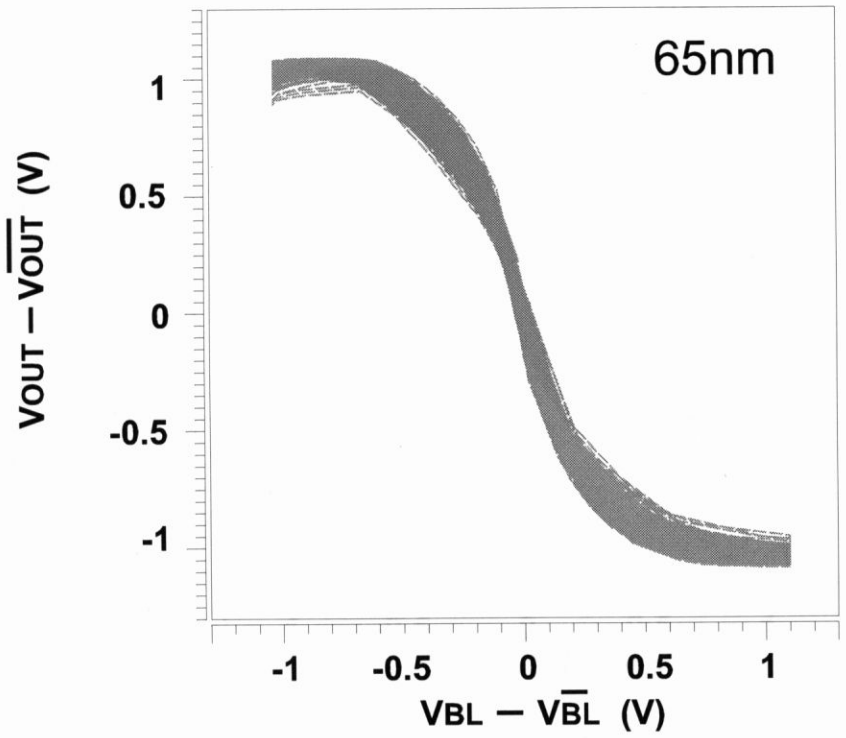


Figure 5.9 The transistor structure of the proposed input offset voltage canceling sense-amp. Cc is implemented by transistors, which means variations of Cc are introduced by variations of transistors.

Again, we change Figure 5.9 into open loop and estimate Voff, which is plotted in Figure 5.10. The comparison of Figure 5.10 and Figure 4.5 is showed in Figure 5.11, from which one can understand using the proposed offset canceling sense-amp, Voff can be suppressed efficiently.


90nm
1
0.5
0
-0.5
-1
VOUT — VOUT (V)
-1
-0.5
0
0.5
1
VBL — VBL (V)


65nm
1
0.5
0
-0.5
-1
VOUT — VOUT (V)
-1
-0.5
0
0.5
1
VBL — VBL (V)

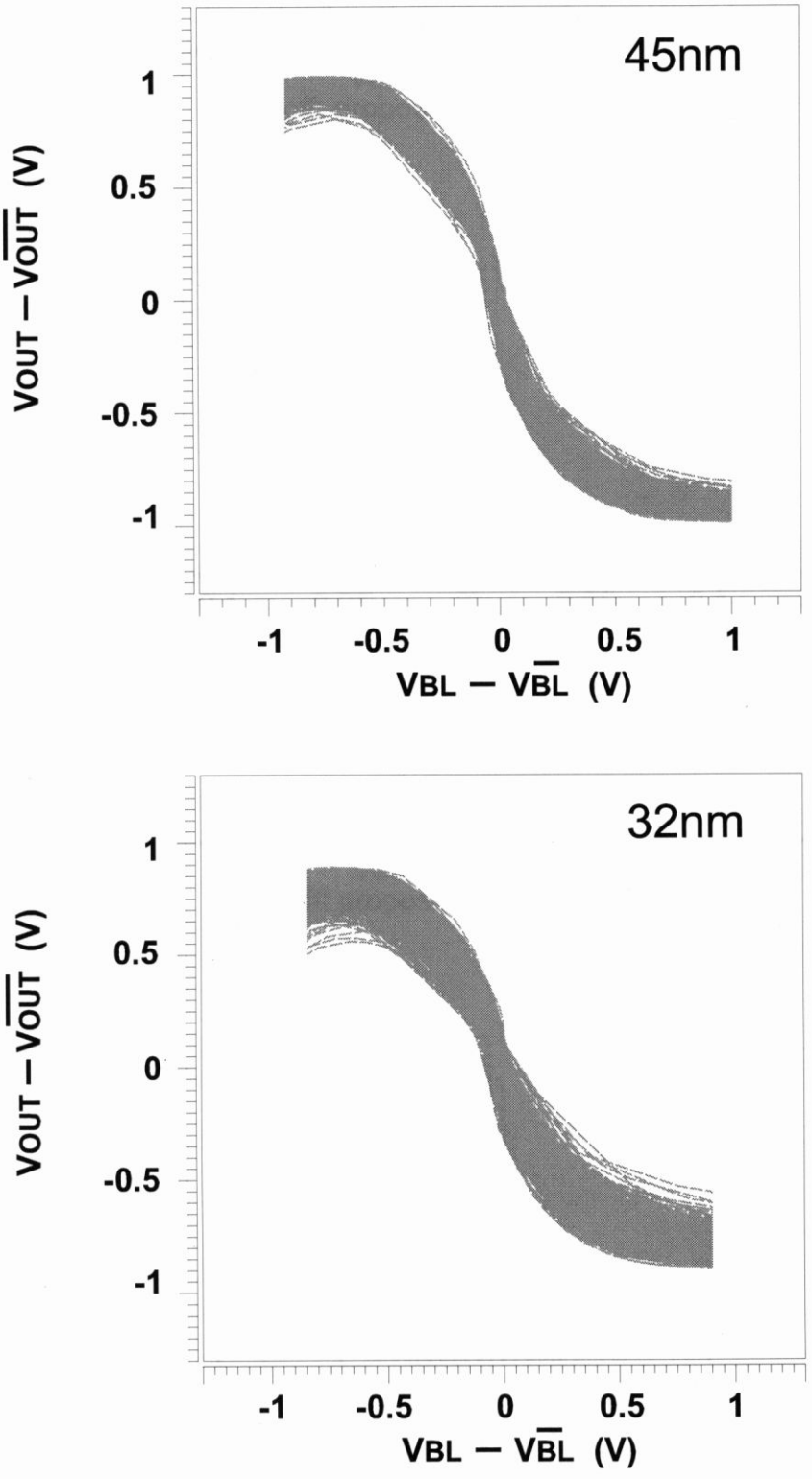
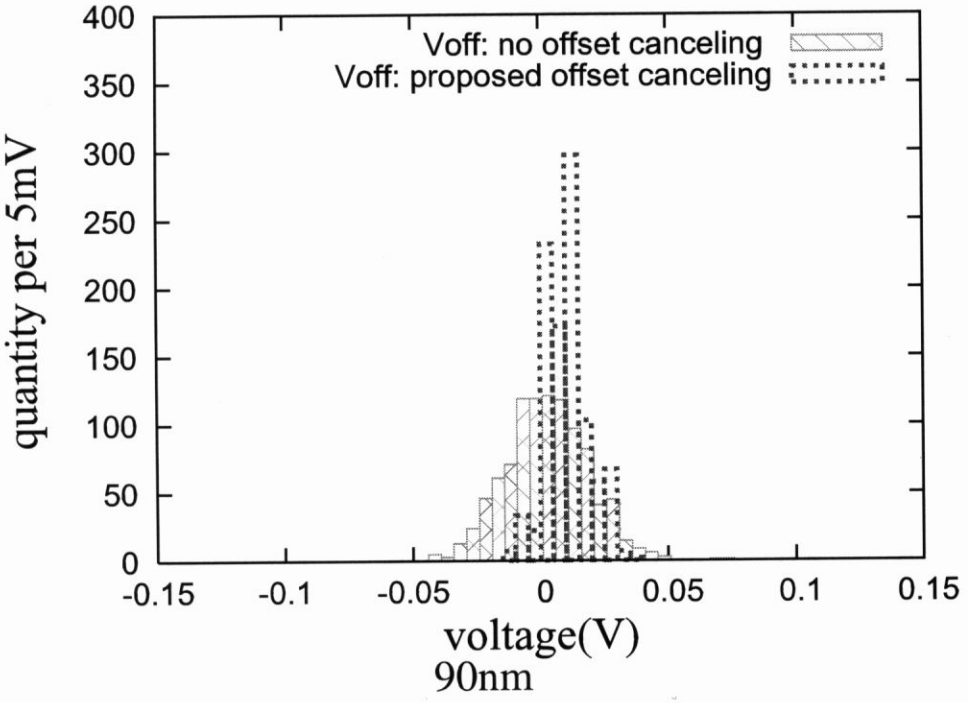
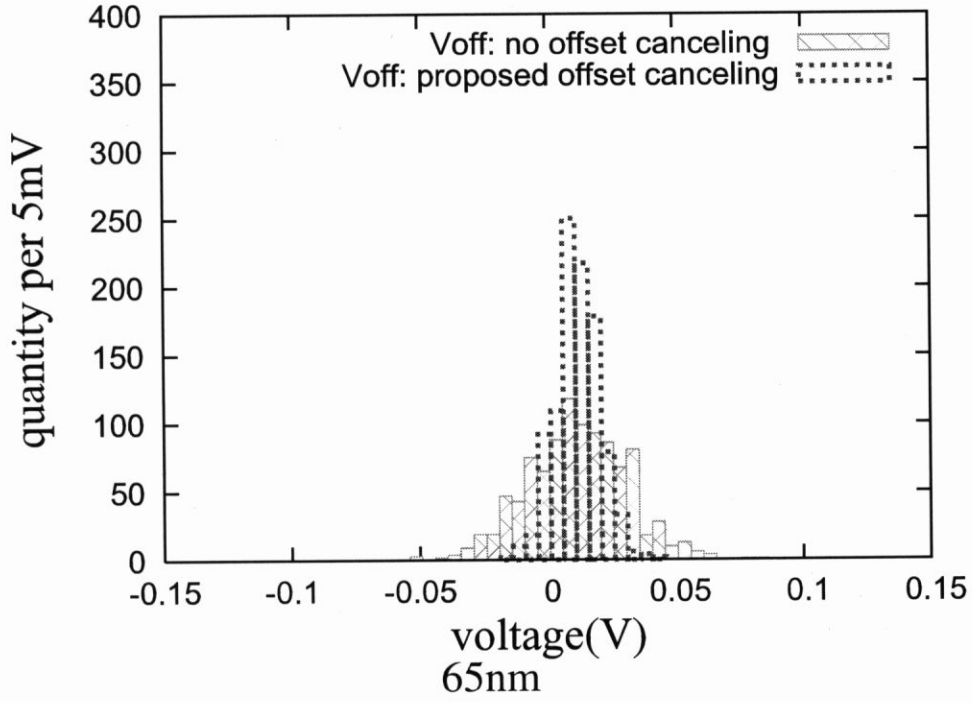


Figure 5.10 Input offset voltage variations of sense-amp


Voff: no offset canceling
Voff: proposed offset canceling
quantity per 5mV
400
350
300
250
200
150
100
50
0
-0.15
-0.1
-0.05
0
0.05
0.1
0.15
voltage(V)
90nm


Voff: no offset canceling
Voff: proposed offset canceling
quantity per 5mV
400
350
300
250
200
150
100
50
0
-0.15
-0.1
-0.05
0
0.05
0.1
0.15
voltage(V)
65nm

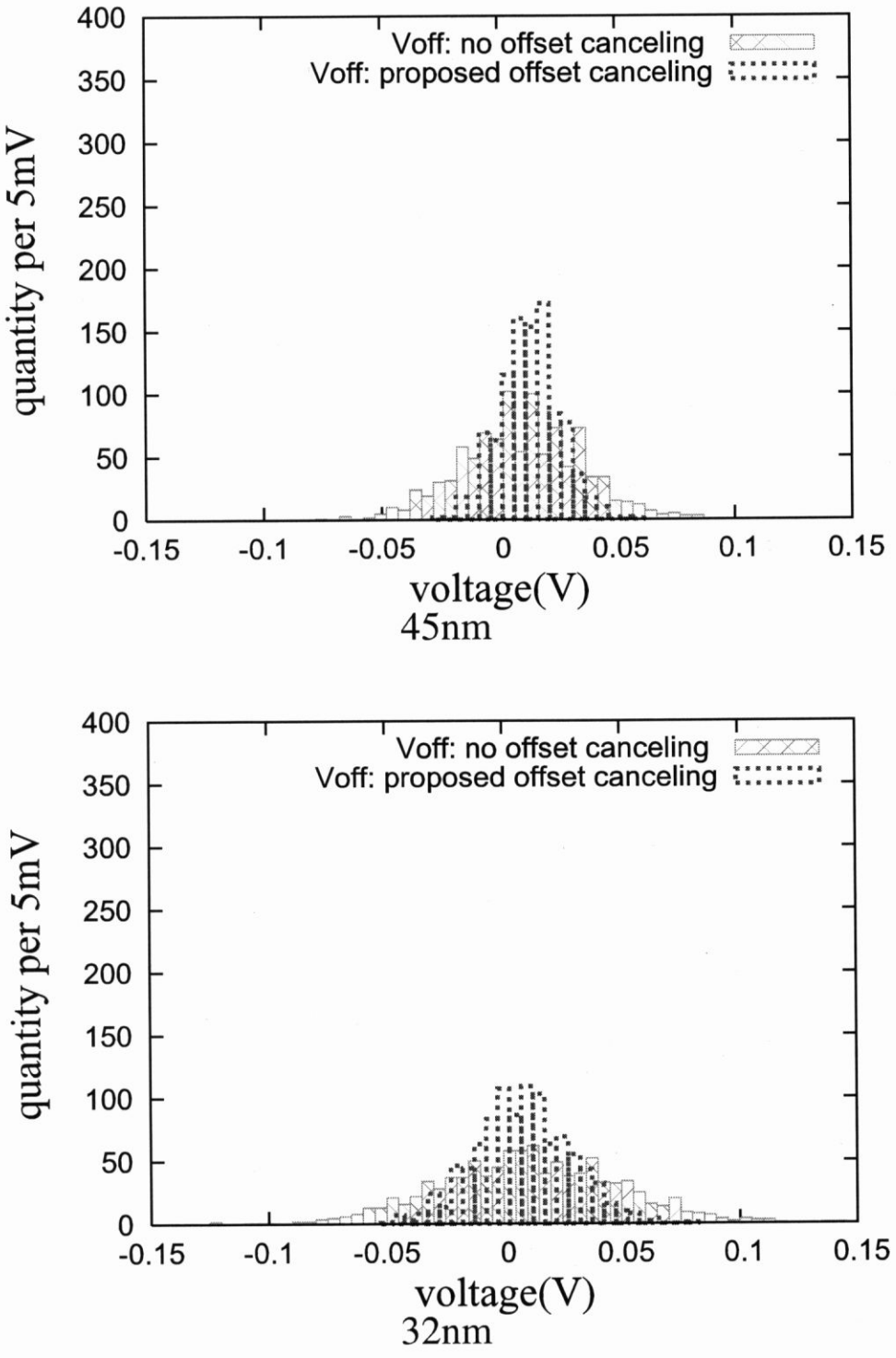


Figure 5.11 Input offset voltage variations of sense-amp comparison. By using the proposed offset canceling sense-amp, Voff is suppressed efficiently.

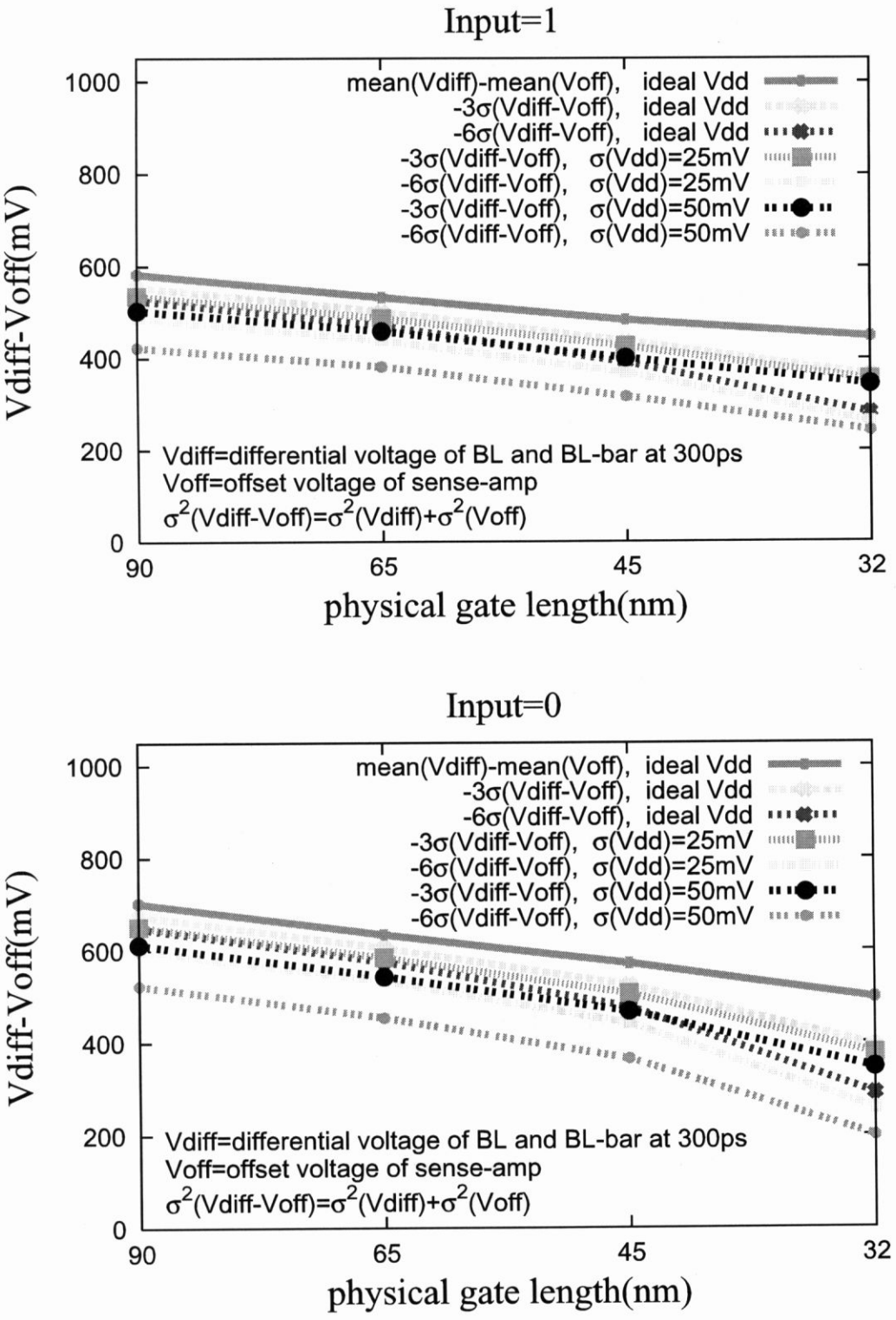


Figure 5.12 Trend of noise margins of PLA with 1-side VG and offset canceling sense-amp

Trend of the noise margin of PLA using the 1-side VG and proposed offset canceling sense-amp for both input=1 and input=0, with and without Vdd noise is plotted in Figure 5.12, in which $\sigma_{Vdd} = 0mV$, $25mV$ and $50mV$, respectively. Compared to Figure 5.4, noise margins can not be increased very obviously because from $\sigma_{V_{diff}-V_{off}} = \sqrt{\sigma^2_{V_{diff}} + \sigma^2_{V_{off}}}$, $\sigma_{V_{off}}$ is reduced by using offset canceling sense-amp even with Vdd noise but $\sigma_{V_{diff}}$ increase due to Vdd noise.

5.3 Parameter Sensitivity Analysis of the Dual-Rail PLA with Proposed Techniques

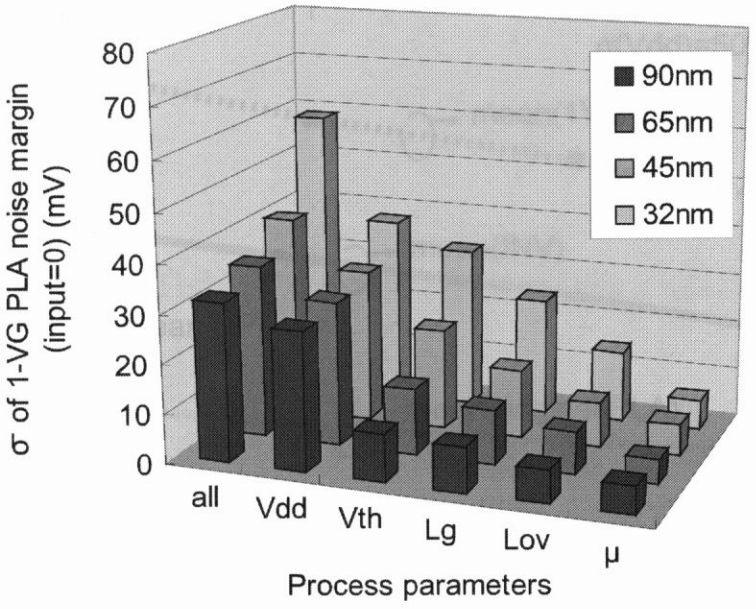
Instead of varying all the parameters simultaneously, we vary one parameter for one time to estimate the sensitivity of each parameter to the dual-rail PLA with proposed techniques. Results are shown in Figure 5.13. It shows how sensitive the σ of noise margins of the dual-rail PLA with proposed techniques is to individual parameter. V_{dd}, V_{th}, L_g, L_{ovs} and L_{ovd}, μ affect the σ of noise margins obviously.

Compared to the original PLA in Figure 4.9, the 1-side VG PLA in Figure 5.13 (a) and the 1-side VG PLA with offset canceling sense-amp in Figure 5.13 (b) both suppress the sensitivity of parameter variations efficiently.

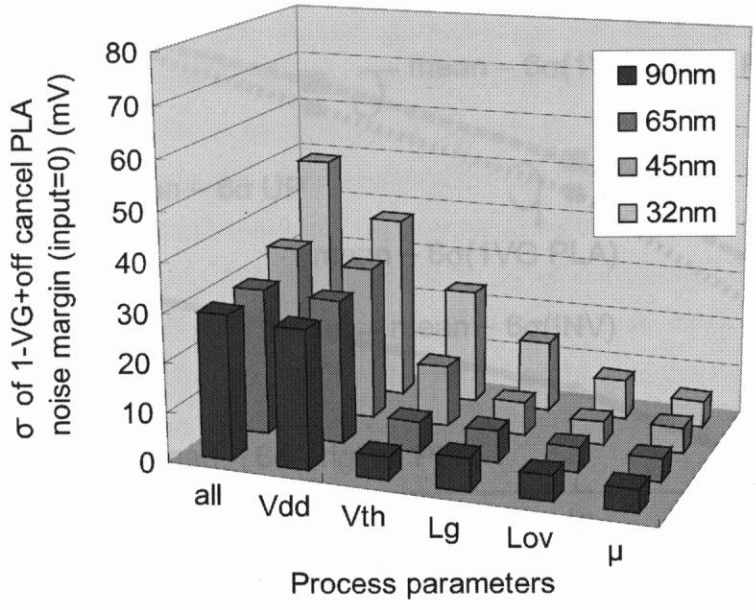
Compared to Figure 5.13 (a), Figure 5.13 (b) suppresses the sensitivity of variations of all the other parameters expect V_{dd}. This is because the variation of the Vdiff, which is in the logic part, increase greatly due to Vdd noise. This also explains why the offset canceling sense-amp can not further increase the noise margin of the 1-side VG PLA very much when with $\sigma_{V_{dd}} = 50mV$.

5.4 Comparison of the Results of Chapter 3, 4 and 5

At last, The trend of noise margins of a CMOS INV (NM_H), the original dual-rail PLA, the PLA only using the 1-side VG, and the PLA using both the 1-side VG and offset canceling sense-amp are compared as Figure 5.14. While there is no noise margin left for 6σ assurance for the random CMOS from 32nm process and for the original dual-rail PLA from 90nm process, the improved dual-rail PLA with 1-side VG is shown to work down to 32nm process with keeping a sufficient operational margin of 150mV, and the 1-side VG dual-rail PLA with offset canceling sense-amp adds 50mV in addition to the operational margin to 200mV at 32nm process.



(a) 1-side VG PLA



(b) 1-side VG offset canceling PLA

Figure 5.13 Parameter sensitivity analysis of the dual-rail PLA with proposed techniques. V_{dd}, V_{th}, L_g, L_{ovs} and L_{ovd}, μ affect the σ of noise margins of the PLA obviously. Compared to the original PLA in Figure 4.9, (a) (b) both suppress the sensitivity of parameter variations efficiently. Compared to (a), (b) suppresses the sensitivity of variations of all the other parameters expect V_{dd}.

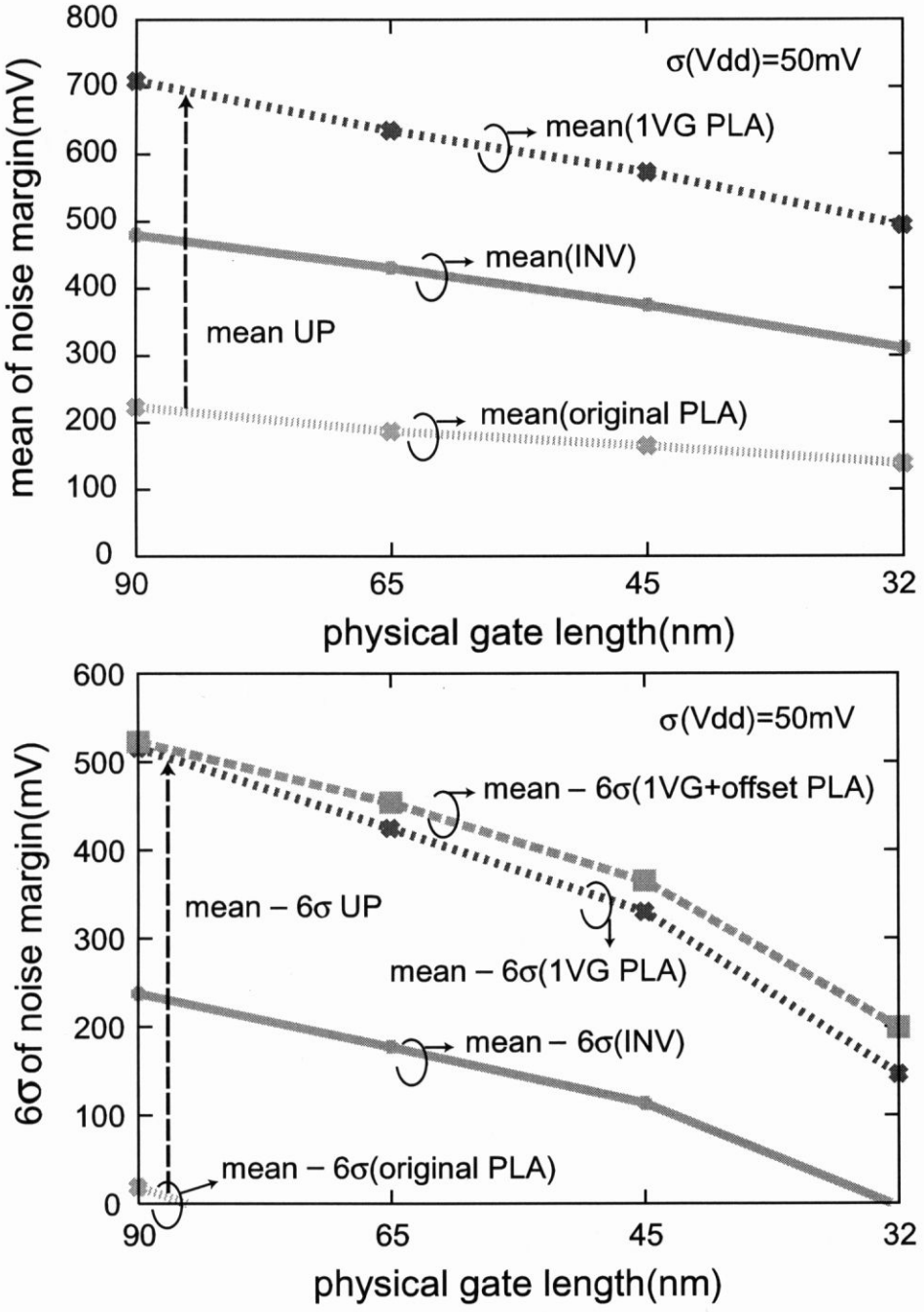


Figure 5.14 The trend of noise margins of a CMOS INV (NM_H), the original dual-rail PLA and the improved dual-rail PLA. While there is no noise margin left for 6σ assurance for static CMOS from 32nm process and for the original dual-rail PLA from 90nm process, the improved dual-rail PLA with 1-side VG is shown to work down to 32nm process with keeping a sufficient operational margin of 150mV, and the 1-side VG dual-rail PLA with offset canceling sense-amp adds 50mV in addition to the operational margin to 200mV at 32nm process.

Chapter 6

Speed and Energy Dissipation Analysis

In this section, we will analyze the trend of speed and energy dissipation of the random CMOS and the dual-rail PLA with proposed techniques along with process scaling.

6.1 Speed and Energy Dissipation analysis of Random CMOS Along with Process Scaling

We measure the propagation delay and energy dissipation of the same inverter in Chapter 3 per switching transition along with process scaling to analyze the performance trend of the random CMOS. Figure 6.1 shows the details. We measure the average of the rise transition case and the fall transition case, from the output of the input buffer to the input of the load buffer. We use the switching threshold of the inverter to be the start point and end point, which is Vdd/2 as described in Chapter 3. A step input signal is assumed in this study.

The results are showed as Figure 6.2 and Figure 6.3, which indicate that process parameter variations deteriorate the performance of the inverter. Especially to the speed, one or even two generation of performance gain can be lost due to process parameter variations.

6.2 Speed and Energy Dissipation Analysis of Dual-Rail PLA with Proposed Techniques Along with Process Scaling

We measure the propagation delay and energy dissipation of one column circuit of the dual-rail PLA with proposed techniques along with process scaling. Figure 6.4 shows the details. We measure the average of the input=1 case and the input=0 case, from the output of the

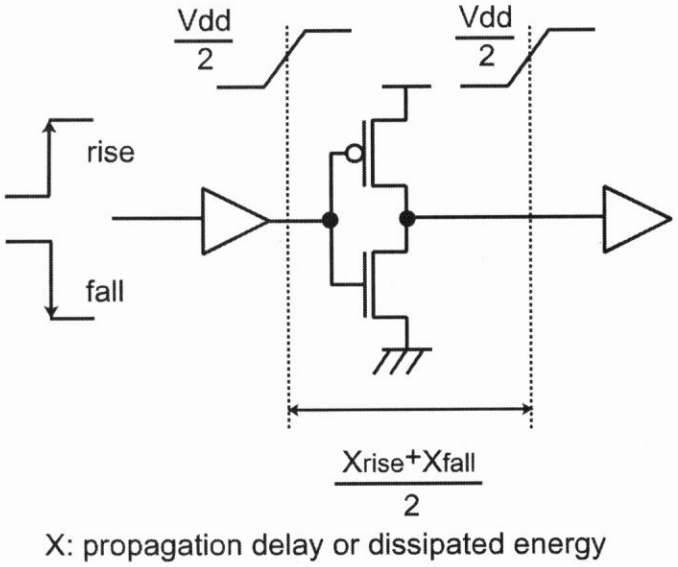


Figure 6.1 The same inverter in Chapter 3 to measure the propagation delay and energy dissipation. We measure the average of the rise transition case and the fall transition case, from the output of the input buffer to the input of the out buffer. We use the switching threshold of the inverter to be the start point and end point, which is Vdd/2 as described in Chapter 3. A step input signal is assumed in this study.

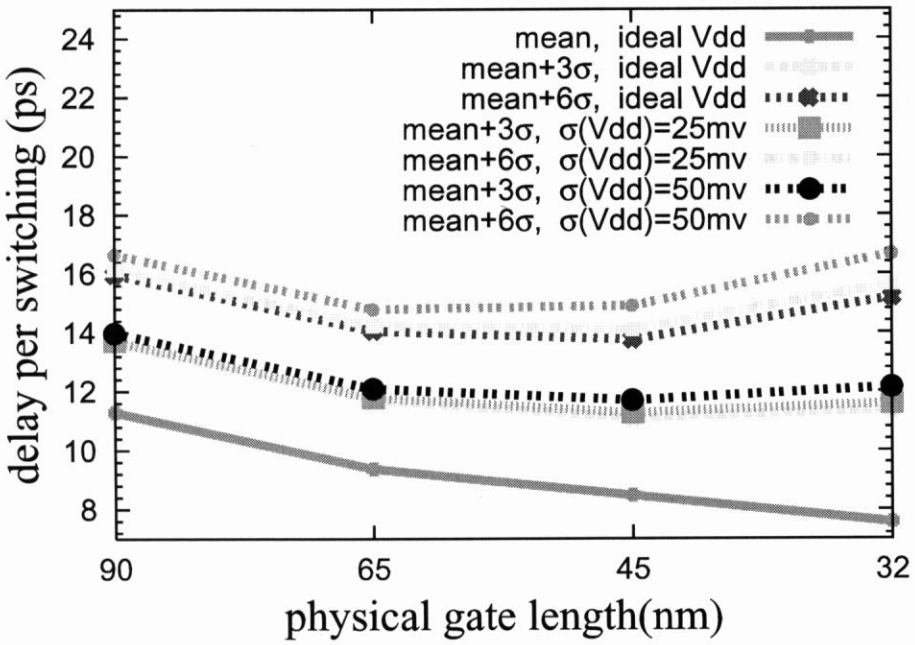


Figure 6.2 The trend of delay per switching transition of an inverter along with scaling

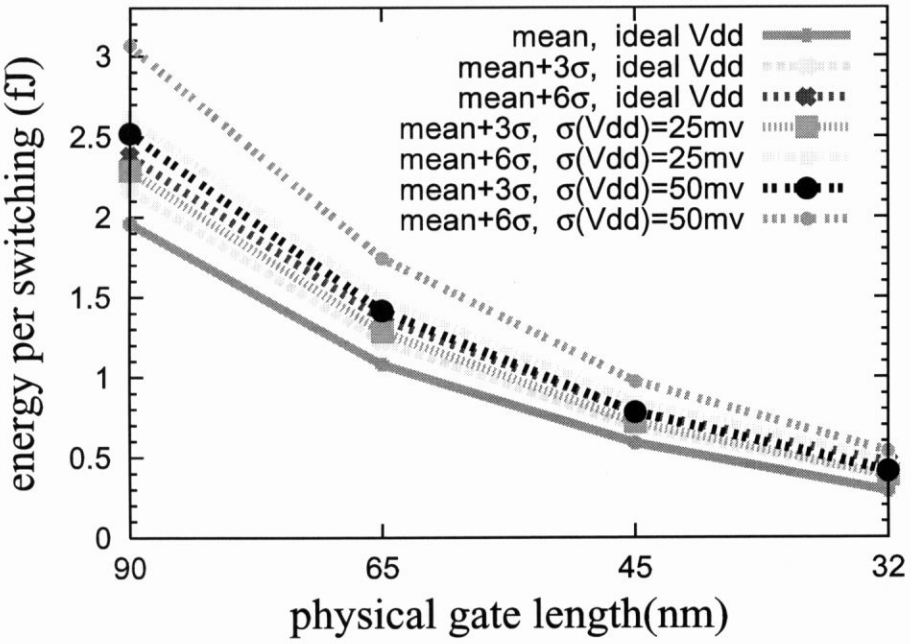


Figure 6.3 The trend of dissipated energy per switching transition of an inverter along with scaling

PC buffer to the input of the load buffer. Vdd/2 is chosen as the sign of start point and end point. The propagation delay is measured during the evaluation phase and on the other hand, the energy dissipation is measured during the pre-charge and evaluation phase. Step input signals are assumed too in this study.

The dual-rail PLA with 1-side VG is estimated. The results are showed as Figure 6.5 and Figure 6.6, which are similar to the random CMOS (refer to Figure 6.2 and Figure 6.3). They indicate that process parameter variations deteriorate the performance of the dual-rail PLA with 1-side VG. Especially to the speed, the same as the random CMOS, one or even two generation of performance gain can be lost due to process parameter variations.

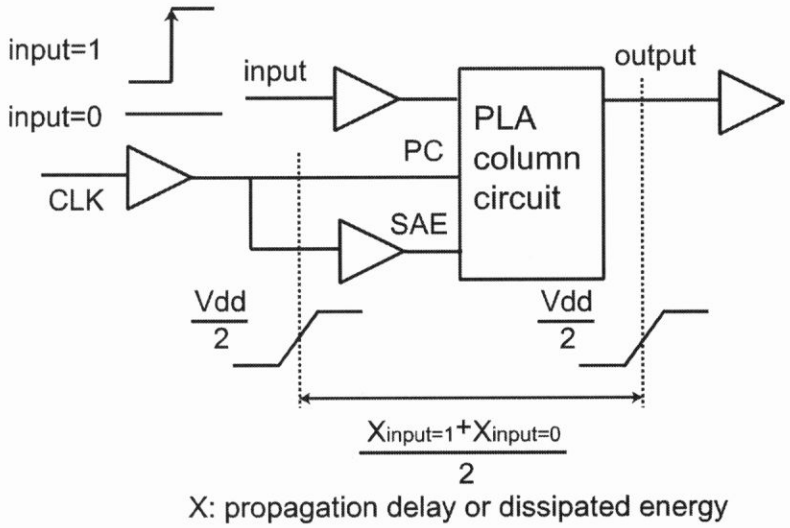


Figure 6.4 One column circuit of the dual-rail PLA with proposed techniques to measure the propagation delay and energy dissipation. We measure the average of the input=1 case and the input=0 case, between the output of the PC buffer and the input of the load buffer. Step input signals are assumed too in this study.

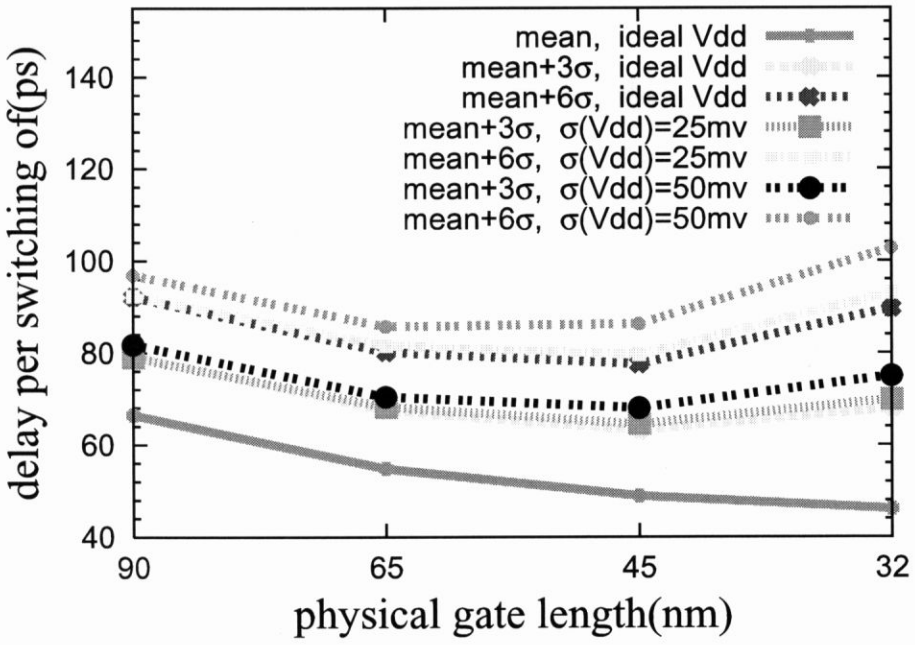


Figure 6.5 The trend of delay per switching transition of the dual-rail PLA with 1-side VG along with scaling

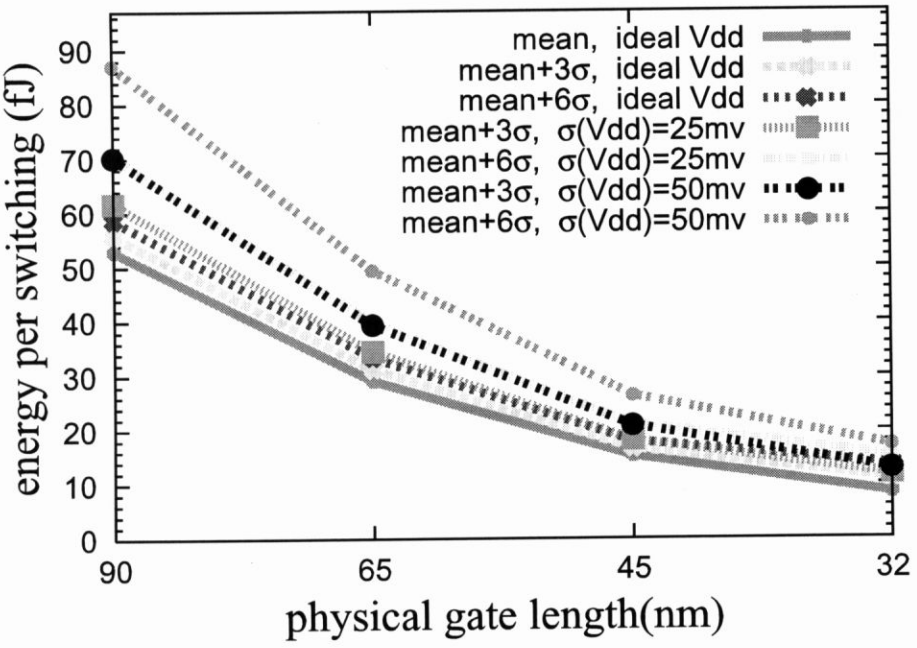


Figure 6.6 The trend of dissipated energy per switching transition of the dual-rail PLA with 1-side VG along with scaling

Chapter 7

Conclusions

This thesis focused on the prediction of the trend in VLSI circuit's reliability under process parameter variations in sub-100nm technology. We have mainly addressed the noise margin issue in the random CMOS and the dual-rail PLA design methodology and proposed new architectures for the dual-rail PLA.

In Chapter 2, we described an approach to estimate the impact of process parameter variations on the random CMOS and the PLA. This approach was built on accurate variation modeling, published data including ITRS, PTM, and Monte Carlo analysis. The difference of the characteristic of the random CMOS and the PLA parameter variations lay in the within die, systematic layout pattern-dependent component. This component was uncorrelated for the random CMOS because the layout was undecided in the early design stage. However, it was correlated and small in magnitude for the PLA because the layout was regular and decided.

In Chapter 3 and Chapter 4, the trend of the noise margin of a CMOS inverter and a column circuit of the dual-rail PLA were respectively analyzed. With the scaling of MOSFETs, the ever increasing process parameter variations posed a challenge to the random CMOS from 32nm and to the dual-rail PLA from 90nm process due to insufficient noise margins. Hence new circuit design methodologies that suppress the impact of process parameter variations should be investigated.

In Chapter 5 techniques to improve the noise margin of the dual-rail PLA were proposed. A 1-side VG structure could enlarge the differential voltage of bit lines by connecting one bit line - BL directly to ground but leaving the other bit line - $\overline{BL}$ connecting to virtual ground. Hence, this structure improved the noise margin of the original dual-rail PLA efficiently. An improved offset canceling sense amplifier scheme was also proposed to cancel the input offset voltage to improve the noise margin of the PLA further. The improved dual-rail PLA with

1-side VG was shown to work down to 32nm process with keeping a sufficient operational margin of 150mV, and the 1-side VG PLA with offset canceling sense-amp added 50mV in addition to the operational margin to 200mV at 32nm process.

In Chapter 6, we analyzed the trend of speed and energy dissipation of the random CMOS and the dual-rail PLA with the 1-side VG structure along with process scaling. Process parameter variations posed similar impact on the two design approaches. Especially to the speed, one or even two generation of performance gain can be lost due to process parameter variations.

As can be seen from the above results, designs with consideration to alleviate the impact of process parameter variations are necessary in future nanometer technology. The techniques proposed in this thesis are viable and efficient in future VLSI designs.

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List of Publications

Proceedings of International Conferences

1. Z. Liang, M. Ikeda, and K. Asada, "Analysis of Circuit Faults Based on Noise Margins Due to Device Parameter Variations in Sub-100nm CMOS Technology," *The 10th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, April 2007*, sumitted.

Proceedings of Domestic Conferences and Meetings

1. Z. Liang, M. Ikeda, and K. Asada, "A Monte-Carlo Analysis of Static CMOS and Dual-Rail PLA for Sub-100nm Parameter Variations," *IEICE General Conference, March 2007.*

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