Chapter 3

On-Chip Transmission Lines

In the previous chapter, the described on-chip inductor can effectively provide required inductances at low frequency up to several gigahertz. At higher frequencies, it cannot be used due to its associated parasitic capacitances and transmission lines are employed instead. An advantage of using transmission lines is the higher quality factor (Q-factor) that can be achieved, compared to the on-chip inductor. However, the Q-factors of conventional CMOS on-chip transmission lines are still low with a typical value of approximately 5.0 [37]. To effectively exploit CMOS at high frequency, transmission lines with high Q-factor are required. High Q lines are characterized by a low attenuation that can reduce power consumption in a circuit. It is also desirable to have lines with high phase constant, β, to reduce the phase velocity of the waves in the lines. The resulting slow wave has low dispersion as described in [38]. An implementation of the slow-wave transmission line in the form of the coplanar waveguide has been reported [39] by using a floating shield. This method of reducing losses is very useful because it requires no additional processing steps. It is therefore useful to further develop new transmission line structures with slow-wave characteristics though layout innovations. Currently, there are several issues that need to be addressed regarding on-chip transmission lines.

- Less lossy lines with superior performance at high frequency are required. Specifically, lines with high Q for low loss, high β for lower phase velocity of the wave, and high obtainable impedance for easy matching are required.
- Proper characterization is necessary for accurate circuit simulations. Accurate models that

can explain the physical phenomenon of the structure are required. The attenuation, phase constant as well as characteristic impedance of the line should be correctly predicted.

- In advanced CMOS processes, stringent design rules require minimum metal densities and limited distances between planar metals. Therefore, the loop inductance of a coplanar waveguide (CPW) cannot be large, thus resulting in low impedance lines. This makes it difficult to use transmission line matching at high frequency.

3.1 History of Slow-Wave Phenomenon

The fundamental principle on which the improved transmission line designs are based on in this work is the slow-wave phenomenon. In 1971, the relationship between the wave propagation frequency and the resistivity of the silicon substrate on which a Si-SiO_2 system were reported [38] as summarized in Fig. 3.1. According to the measured characteristics, a slow-wave mode of propagation was identified which has desirable characteristics such as lower dispersion and losses.

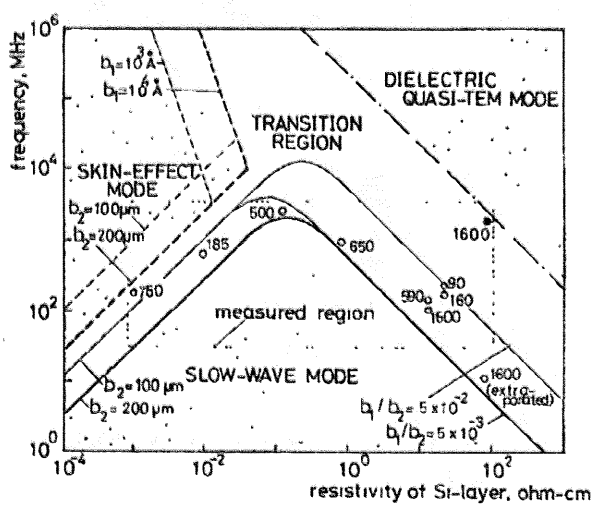


Fig. 3.1 Three propagation modes were identified experimentally in 1971 [38].

It is, however, useful and important to achieve the slow-wave mode by using innovative layout techniques on an available process. This is possible since the structure of the transmission lines determines the effective permittivity, and therefore the propagation velocity.

3.2 Realizing Slow-Wave Transmission Lines (SWTL)

3.2.1 SWTL Structure

We present a new slow-wave transmission line (SWTL) structure that satisfies the above requirements. The lines are fabricated using a six-metal 90nm CMOS process. Figure 3.2 shows the basic structure of the transmission line. The features and physics of this structure are explained in detail in the following sections.

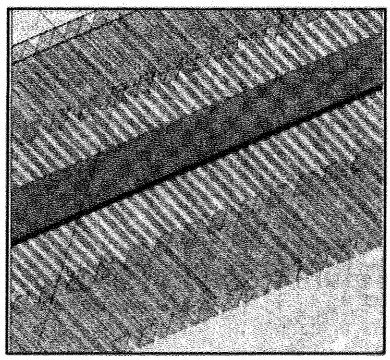


Fig. 3.2 New composite high-Q transmission line structure for advanced CMOS designs.

Figure 3.3 describes the structure which includes ground metals at both sides of the signal line. Each of the ground metal structure consists of extended metal fingers orthogonal to the direction of current flow and they are connected together at a distance w_g from the signal conductor. Figure 3.4 shows the cross-section of the structure.

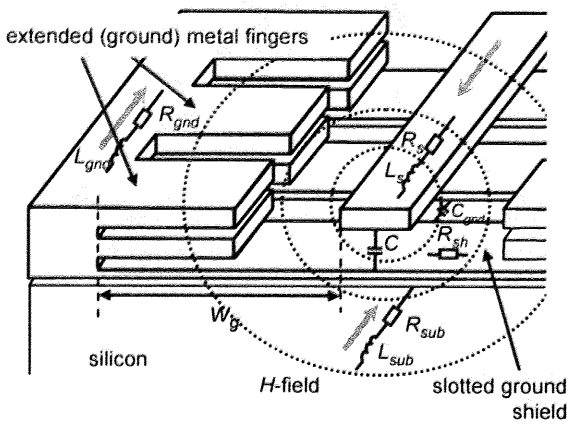


Fig. 3.3 Structure of the slow-wave transmission line with the currents flowing through it.

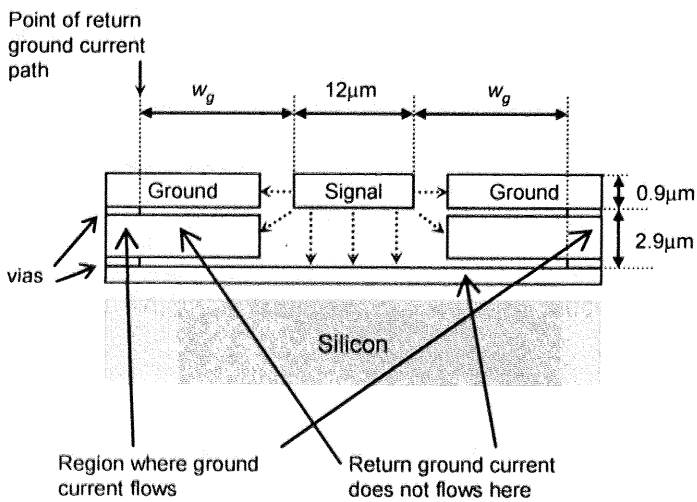


Fig. 3.4 Simplified cross-section of the slow-wave transmission line. The electric field from the signal line will terminate at the side grounds and the bottom shield located 2.9μm below it.

No return current flows along these finger structures but will flow at a farther distance w_g from the signal conductor at where the fingers join. In this way, the return ground current flows at a distance farther away in order to increase the inductance while satisfying the density rules. The typical density requirement for advanced CMOS processes is between 20% and 60% within the given size of a checking area, depending on the metal layer. This checking area is stepped through the layout. Hence, the required condition in the design of the finger structures is to

fulfill these requirements by determining the most appropriate distance between the fingers and the signal line. This region will not contain any metal and will, therefore, reduce the total metal density of the checking area. The most stringent requirements can be considered with more than one CPW in the same checking area, which can be satisfied by the proposed method while maintaining proper characterization of the complete structure. In this structure, the effects of extended metal fingers can be considered as a minor reduction in the inductance of the signal lines due to eddy current in the fingers. However, due to the narrow width of each finger, the eddy current in the extended metal fingers is small and can be reasonably neglected.

The ground conductors extend towards the silicon substrate and are connected to a slotted ground shield laid underneath the signal conductor. The ground shield prevents the electric field from entering the substrate while its slotted structure minimizes return current from flowing thereby allowing w_g to be the principal parameter to determine the inductance. Figure 3.5 demonstrates how the inductance, L can be affected by w_g.

$$L = \frac{\partial B}{\partial t} \cdot A = \frac{\partial B}{\partial t} \cdot w_g \cdot l$$

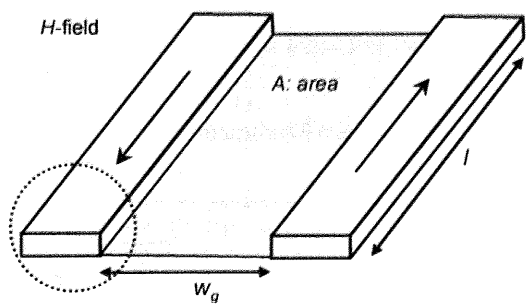


Fig. 3.5 The inductance L is determined by the area enclosing the magnetic field which is a function of w_g.

The proximity of the shield, further, reduces the distance of the signal line to ground potential and this result in a larger capacitance. The approximate lossless relationship between the phase velocity, v_p and the unit inductance, L and capacitance, C is shown as

$$v_p = \frac{1}{\sqrt{LC}} \quad . \tag{3.1}$$

It can be deduced that a lower phase velocity can be achieved when the unit inductance and capacitance are high. In general, the propagation constant γ is related to L and C by

$$\gamma = \alpha + j\beta = \sqrt{(G + j\omega C)(R + j\omega L)} \quad . \tag{3.2}$$

The real part of γ, α corresponds to the attenuation of the line, and the imaginary part, β is the phase constant. G and R is the unit leakage conductance from signal to ground and the unit series resistance of the signal line respectively. Consequently, the extended metal fingers and slotted ground shields changes α and β. This is verified by the measurement results in the next section.

3.2.2 Measurement of Fabricated Structures

Test structures are fabricated with line length, l=900μm and different values of w_g. Large values of w_g are included to characterize its effect on the performance of the SWTL. Table 3.1 summarizes the dimensions of the fabricated test structures. Table 3.2 lists the dimensions of the common parameters.

Table 3.1 Summary of Dimensions of Fabricated SWTL Structures.

	w_g [μm]	w_{finger} [μm]	L_{finger} [μm]	s_{finger} [μm]
#1	14.0	4.0	0.0	8.125
#2	24.0	4.0	10.0	8.125
#3	34.0	4.0	20.0	8.125
#4	44.0	4.0	30.0	8.125
#5	84.0	4.0	70.0	8.125

Table 3.2 Dimensions of Other Common Parameters.

Signal conductor width, w	12.0μm
Signal conductor to finger distance	14.0μm
Signal conductor to shield distance	2.9μm
Shield metal thickness, t_{shield}	0.25μm
Shield slot spacing, s_{slot}	0.25μm
Shield slot width, w_{slot}	0.25μm

w_{finger} and L_{finger} are the width and length of the metal fingers at the top metal layers, s_{finger} is the space between the fingers. For comparison, a coplanar waveguide (CPW) structure of Fig. 3.6 with signal-to-ground gap of 14μm is also fabricated on the same chip.

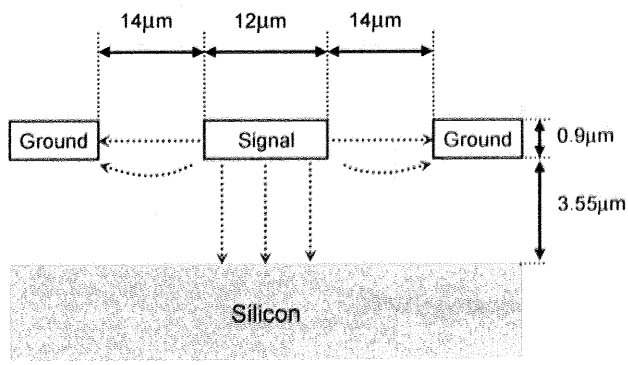


Fig. 3.6 Cross-section of the reference CPW structure.

For measurements, an Anritsu ME7808 vector network analyzer with Anritsu 3742A-EW Transmission-Reflection modules is used on an on-wafer probe station. The Transmission-Reflection modules extend the measurement frequency from 65 GHz to 110 GHz. Figure 3.7 is a micrograph of a fabricated transmission line for w_g=44μm. The lines are measured with G-S-G probes on the pads at the two ends of the lines and de-embedded.

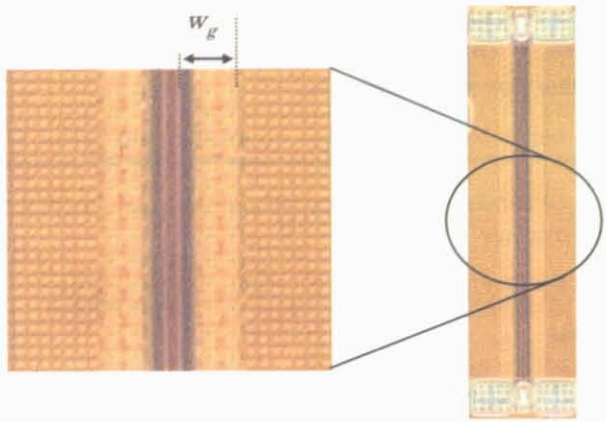


Fig. 3.7 Micrograph of the fabricated structure.

De-embedding employs the open-short-through method. From the de-embedded S-parameters obtained from measurements, Eq. (3.3) and (3.4) are then used to obtain the propagation constant, γ [40].

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1}, \tag{3.3}$$

where

$$K = \left\{ \frac{\left(S_{11}^2 + S_{21}^2 + 1\right)^2 - \left(2S_{11}\right)^2}{\left(2S_{21}\right)^2} \right\}^{\frac{1}{2}} \tag{3.4}$$

and l is the length of the fabricated SWTL.

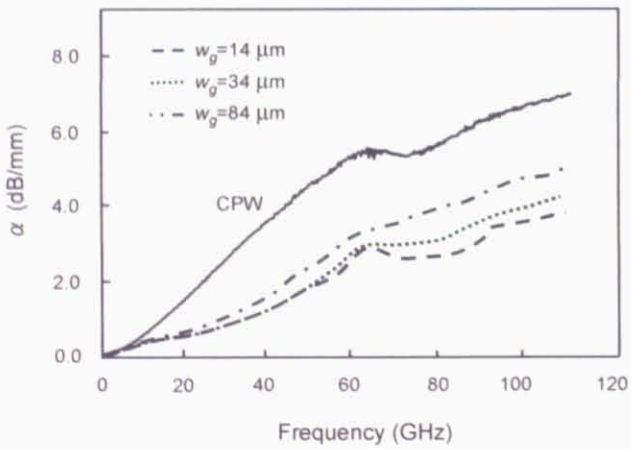


Fig. 3.8 Real part of the propagation constant, α plotted for structures of different w_g. α corresponds to the attenuation of the lines. The plot for CPW is included for reference.

Figure 3.8 plots the measured values of α for three of the representative SWTL as well as the conventional CPW. The results show that lower attenuations are achieved for the SWTL when compared to the CPW. Up to 60 GHz, the attenuations of these lines are approximately only 50% of the reference CPW line. The higher attenuations of some lines at 65 GHz are a result of measurement errors due to employing the Transmission-Reflection modules at the switch-over frequency of 65 GHz.

Comparing the SWTL of different w_g, there is relatively small variations at low frequency. However, at high frequencies, lines with smaller w_g perform significantly better with lower α with up to 20% reduction in attenuation at 100 GHz between the narrowest (w_g=14μm) and the widest structure (w_g=84μm). Lines with large w_g have stronger magnetic field penetrating the substrate underneath the shield at high frequency that induces a current to flow. Further increasing w_g results in attenuations which approaches that of a CPW. The high frequency effect of the signals on the CPW is manifested through the substrate parasitic as the signal line of the CPW is exposed to the silicon underneath. Some of the electric field lines terminates on the semi-conducting substrate and can induce a weak return current to flow.

The plot of Fig. 3.9 shows that the slow-wave transmission lines have high phase constants β. The phase velocity of the wave is related to the phase constant by

$$v_p = \frac{\omega}{\beta}. \tag{3.5}$$

Slow-wave transmission lines have high β that result in the lowest phase velocity. Figure 3.9 also shows that reducing w_g will result in a value of β closer to that of the CPW. This variation with w_g is different from that of α as described earlier.

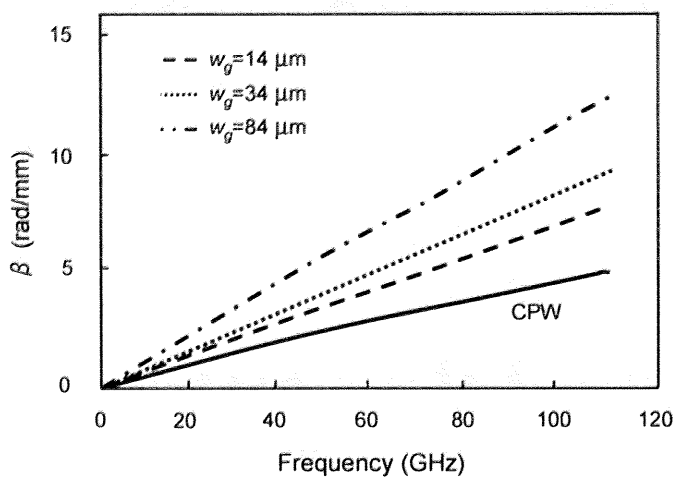


Fig. 3.9 Imaginary (β) component of the propagation constant for structures of different wg. β is the phase constant of the lines. The plot for CPW is included for reference.

For transmission line resonators that are commonly used in filters, oscillators and tuned amplifiers, the resonant cavity Q is derived [41] to be

$$Q = \frac{\beta}{2\alpha}. \tag{3.6}$$

This definition takes into account of the average energy stored, including both magnetic energy and electric energy. Figure 3.10 plots the values of Q obtained using Eq. (3.6). From Fig. 3.10, the Q-factors of all the slow-wave transmission lines are higher than the conventional CPW. The definition of Q in Eq. (3.6) can also be understood as the inverse relationship of attenuation per phase constant. In contrast to the attenuation per physical length, given simply by α as in Fig. 3.8, Q describes the power loss in a given phase. Since the length of a transmission line is determined by the required number of wavelengths in a RF design, it is meaningful to consider the loss in a given phase. To understand the mechanism of the Q-factor variation, it is useful to consider the inductive quality factor and the capacitive quality factor [42] that limits the attainable value of Q. In the case of SWTL, it is the low inductive quality factor that prevents the structures from high values of Q.

For the CPW which has a larger signal-to-ground distance, the capacitive quality factor is lower and the value of Q is affected by both types of quality factor. It can be seen that all SWTL have higher Q-factors when compared with the CPW.

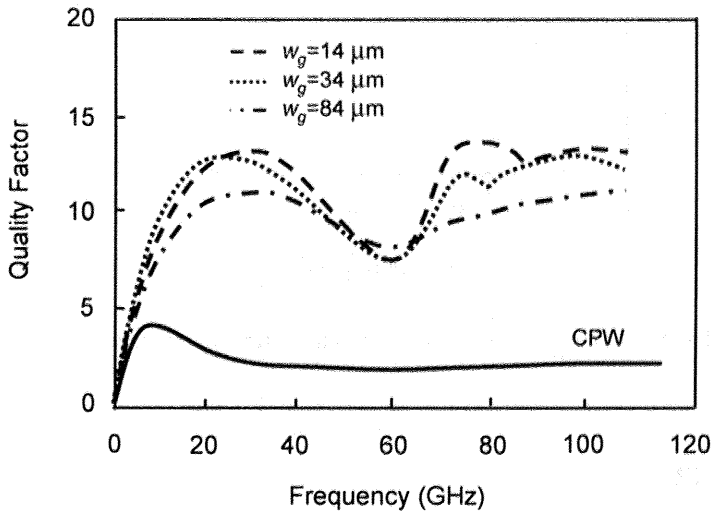


Fig. 3.10 Quality factors of the measured new transmission lines have higher values as compared to the Q-factor of the measured CPW fabricated under the same process conditions.

The characteristic impedances of the lines are obtained from the de-embedded S-parameters according to

$$Z_C = Z_0 \frac{(1+S_{11})^2 - S_{21}^{\ 2}}{(1-S_{11})^2 - S_{21}^{\ 2}}. \tag{3.7}$$

Results are shown in Fig. 3.11 with values in the range of 30-50 Ω. It can be seen that lines with larger w_g has higher impedances. For the simplified lossless case approximation,

$$Z_C = \sqrt{\frac{L}{C}}. \tag{3.8}$$

Since lines with larger w_g have a higher L, lines with larger w_g will result in higher Z_C.

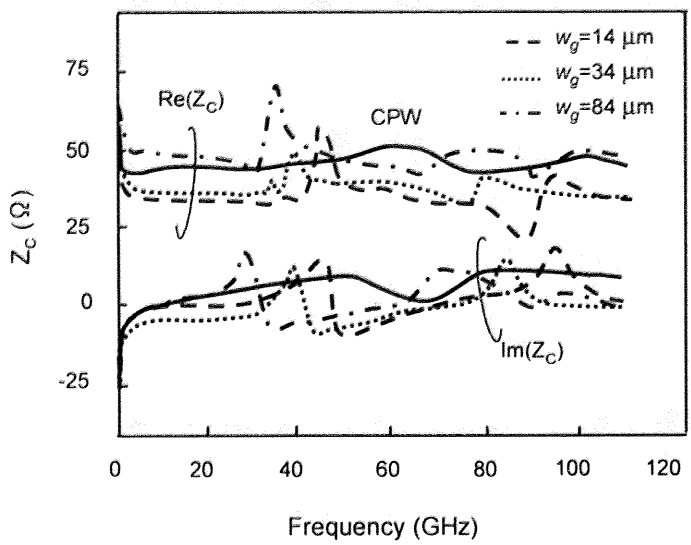


Fig. 3.11 Real and imaginary components of the characteristic impedance of the lines.

3.3 Modeling SWTL

3.3.1 Equivalent Circuit Model

To employ the new transmission line structure in circuit designs, an accurate model for circuit simulations is required. The proposed model of Fig. 3.12 considers the physics of the SWTL structure. A magnetic field loops around the current-carrying conductor and penetrates the closely located silicon substrate. Hence, substrate current is induced that results in parasitic inductance and resistance. As the operating frequency increases, this substrate effect increases and becomes substantial. The electric field that originates from the signal line terminates at ground potential located at the same metal plane and at the slotted ground shield underneath the signal line. Therefore, the return current due to the electric field in the silicon substrate is significantly reduced. The electric field lines also terminate at sidewalls of the ground metals. In this structure, the return current flows primarily along the coplanar metals at a distance w_g from the signal line, which also develops an inductance and resistance along its path. The return current cannot effectively flow through the slotted ground shield dividing the signal line and the

substrate because of the slot spaces that prevents the flow of the return current. However, due to capacitive coupling between the slotted metals of the shield, a small current exists at high frequency. With a description of the physical processes in the structure, an equivalent distributed circuit model is developed. The model of Fig. 3.12 takes into account the important effects of the substrate and ground parasitic by using simple lumped equivalent circuit elements.

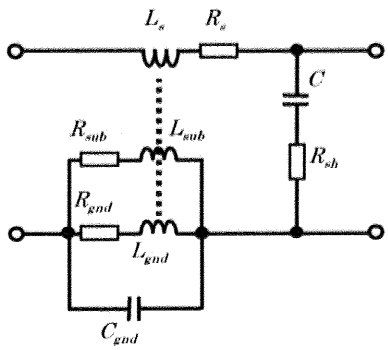


Fig. 3.12 Distributed circuit model of the slow-wave transmission line.

In the model, the series inductance and resistance are represented by L_s and R_s respectively. The parasitic components include the substrate resistance R_{sub}, substrate inductance L_{sub}, resistance of the ground metal along the return current path R_{gnd}, the associated inductance in the ground metal L_{gnd}, as well as the capacitance of the slot spaces in the shield metal C_{gnd}. The substrate and ground inductances are coupled to the line inductance. In addition, the capacitance between the signal line and the ground metals is considered with the capacitor C. R_{sh} represents the resistance of the metal slots of the shield structure.

This model is transformed into an equivalent model of Fig. 3.13. This model has fewer components and it explicitly demonstrates the effect of the substrate parasitic on a shielded transmission line. The resonance loop models the increasing effects of the substrate at higher frequency. In addition, this equivalent-circuit model has kept its simplicity for the purpose of practical implementation. The proposed elements R_{ext}, L_{ext}, M, C_{gnd}, and R_{sh} in this equivalent

circuit are described. Eq. (3.9)-(3.13) provides guidance to the value of the parameters used in the model. For Eq. (3.9)-(3.11), fitting is made to the numerical parameters of k_1, k_2, k_3 and k_4. Approximations of the other parameters can be obtained by conventional analysis of the Telegrapher's *RLGC* model. R_{ext} is approximated to the substrate resistance through which the substrate current flows.

$$R_{ext} = k_1 \frac{R_{\square,Si}}{w} \tag{3.9}$$

$R_{\square,Si}$ is the sheet resistance of the silicon underneath the signal line and w represents the width of the signal line. L_{ext} is a result of the magnetic field generated by the signal line and is approximated by a fraction of L_s.

$$L_{ext} = k_2 \cdot L_s \tag{3.10}$$

The magnetic coupling coefficient is approximated by the parametric equation

$$M = 1 - e^{-k_3 (w_g / w)^{k_4}} . \tag{3.11}$$

C_{gnd} and R_{sh} are small due to the low values of the series capacitances linking the gaps between the slotted metals in the shield and the parallel resistances of the slotted metal, respectively. The values can be approximated by

$$C_{gnd} = \varepsilon_{ox} \frac{t_{shield} w}{m \cdot s_{slot}} \tag{3.12}$$

$$R_{sh} = R_{\square,slot} \cdot \frac{2w_g + w}{2m \cdot w_{slot}} \tag{3.13}$$

ε_{ox} is the effective dielectric permittivity, m is the number of metal slots per meter in the shield and $R_{\square,slot}$ is the sheet resistance of the slot metal in the shield. This model of Fig. 3.13 has been simulated in 80-stage cascade to evaluate the performance. To ensure the distributed characteristics of the model, the elemental stage is ensured to have a length significantly less than a wavelength of the maximum measurement frequency. Results of the modeling are explained in the next section.

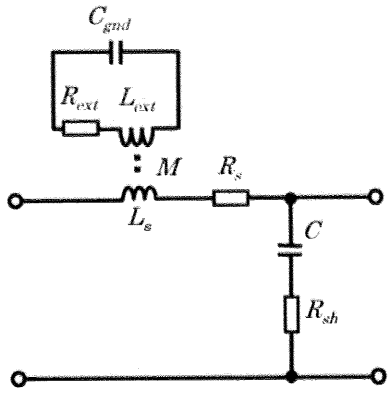


Fig. 3.13 Equivalent model with the substrate and ground effects externally modeled.

3.3.2 Modeling Results

Table 3.3 shows the fitted parameters used in Eq. (3.9)-(3.11).

Table 3.3 Values of the Fitting Parameters.

k_1	k_2	k_3	k_4
0.56	0.02	0.36	0.42

The new parameters of the distributed model of Fig. 3.13 are calculated by the Eqn. (3.9)-(3.13). Tables 3.4(a) and 3.4(b) provide a summary of all the parameters used in the SWTL model.

Table 3.4(a) Parameters of the Proposed Model for Different Test Structures.

w_g	R_s [kΩ/m]	L_s [nH/m]	C [pF/m]	R_{sh} [nΩ/m]
14.0 μm	2.0	379	335	4.98
24.0 μm	2.0	459	335	7.48
34.0 μm	2.0	542	335	9.97
44.0 μm	2.0	586	335	12.5
84.0 μm	2.0	819	335	22.4

Table 3.4(b) Parameters of the Proposed Model for Different Test Structures (Continue).

w_g	C_{gnd} [fF/m]	R_{ext} [kΩ/m]	L_{ext} [nH/m]	M
14.0 μm	4.11×10^{-6}	5.29	9.7	0.39
24.0 μm	4.11×10^{-6}	5.29	10.1	0.41
34.0 μm	4.11×10^{-6}	5.29	10.8	0.43
44.0 μm	4.11×10^{-6}	5.29	12.8	0.46
84.0 μm	4.11×10^{-6}	5.29	13.2	0.46

Since all the test structures have the same length, the values of R_s, C, C_{gnd} and R_{ext} do not change, according to the physical equations that describe them. L_{ext} which is a result of the coupled inductance from the signal line is shown to have a value that is only a fraction of L_s with slight increases in the coupling coefficient M. A larger M results from a larger area being coupled with increasing w_g. The model characteristics, using the calculated values, are then verified with the measured results in this frequency range. The objective is to show that the proposed model can be used to represent the fabricated structures.

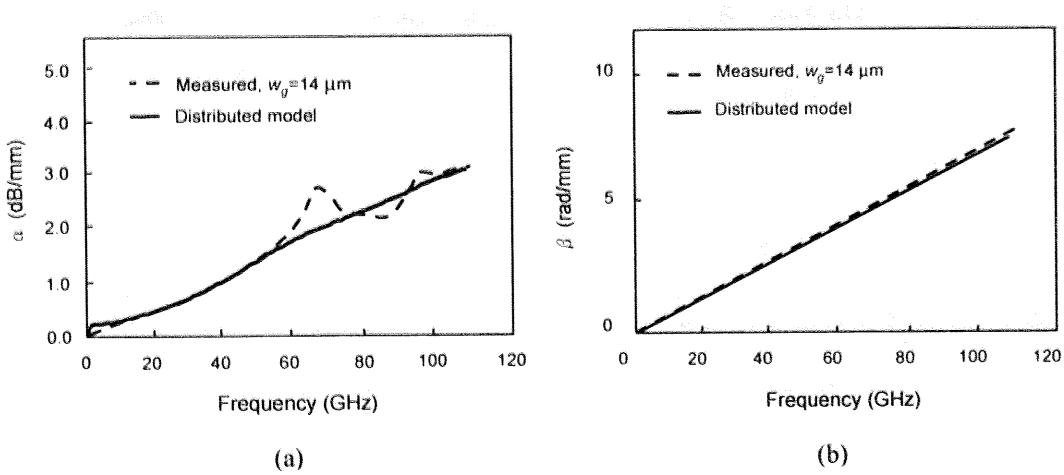


Fig. 3.14 Comparison of (a) real (α) component of the propagation constant of a sample measured line to the simplified distributed model of Fig. 3.12; (b) comparison of imaginary (β) component of the propagation constant of a sample measured line to the model.

Figures 3.14(a) and (b) show the comparison of the attenuation and the phase constant of the fitted model and measured sample transmission line with w_g=14μm. The simulated results of the distributed model generally agree well with the measured results, especially at low frequency. However, excessive attenuation is not accounted for by the model at 65 GHz due to the switching-over of the Transmission-Reflection modules of the measurement setup as described earlier. Figure 3.14(a) shows the results of the fitted model with a sample line w_g=14μm, which has the worst-case 65 GHz peaking among the results of Fig. 3.8. Figure 3.14 (b), however, shows the excellent agreement of the phase constant of the model and measured results.

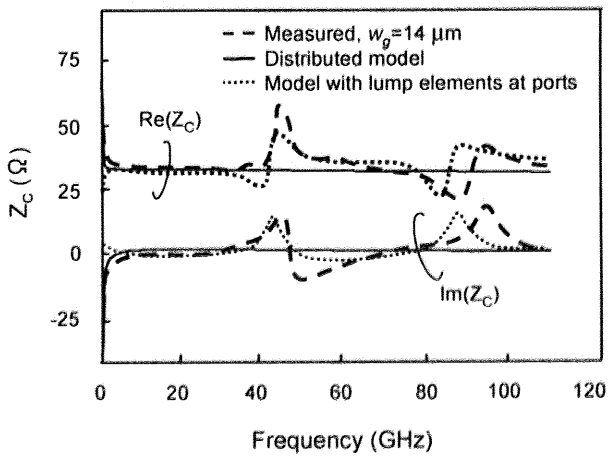


Fig. 3.15 Comparison of real and imaginary components of the characteristic impedance of a sample measured line to the model.

Figure 3.15 shows the simulated impedance of the lines using the proposed model and the measured results. The peaks and troughs are not due to measurement problems but are simply caused by the length of the line which reaches half a wavelength at this frequency [43]. This can be seen by the S11 of the measured SWTL showing minimum return losses and zero phases at frequencies corresponding to the half-wavelength in Figs. 3.16(a) and (b) respectively. Alternatively, this effect can be modeled by lumped circuit elements at the two ports. This results in a good fit as shown in Fig. 3.15 as well. The proposed model can be used in

simulations to characterize the high-Q transmission lines.

The peak occurrences of the characteristic impedance at half-wavelength can be verified by the phase velocity v_p of the wave through the 900μm SWTL. This can be calculated at f=46.0 GHz according to Eq. (3.14).

$$v_p = f \cdot \lambda \tag{3.14}$$

where the half-wavelength, $\lambda/2$=900μm. According to Fig. 3.9 and Eq. (3.5), an equivalent value can be obtained for the sample line w_g=14μm.

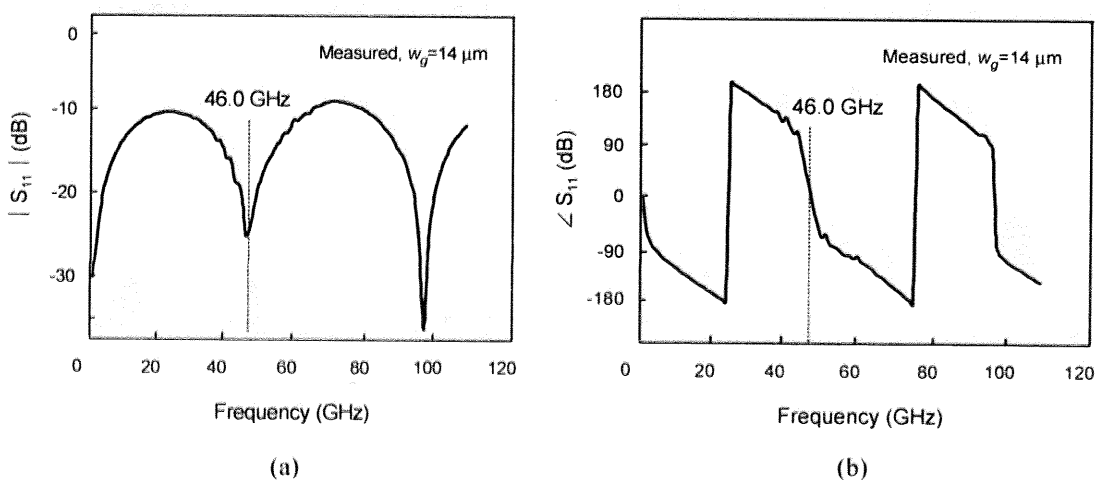


Fig. 3.16 (a) Magnitude of S11 of the sample transmission line showing the high return loss at 68 GHz; (b) The corresponding phase of S11 of the sample transmission line showing the changes in phase.

3.4 Chapter Summary

A new slow-wave transmission line structure for improving the Q-factor has been fabricated and characterized. This structure uses slotted ground shields for preventing the electric field from entering the substrate. The extended ground metal fingers of the transmission line allow higher

inductances to be achieved while enabling the design to satisfy the stringent density requirements of advanced CMOS processes. The quality factor achieved is higher than 10 at 110 GHz, which is four times that of the conventional coplanar waveguide. The current induced in the silicon substrate by the magnetic field is modeled by the proposed distributed circuit model. This model also accounts for the leakage return current along the reverse signal path in the ground shield. The model can be employed in circuit simulators to design the circuits used in the millimeter-wave transceiver.

Chapter 4

Asymmetric Coaxial Waveguide

In this chapter, another structure for the transmission line is proposed. As the scaling of CMOS processes advances to sub-100nm, it is realized that MOSFET perform better with higher cut-off frequencies beyond 100 GHz. The performance of the passive devices, however, needs to be improved to exploit the performance of the MOSFET. In particular, further new transmission line structures should be developed as it is the fundamental building block to realize other passive devices such as baluns and impedance transformers. To measure the performance of the transmission lines, the quality factor (Q-factor) is typically considered as a figure of merit. Another useful figure of merit is the required physical length to realize a given wavelength of the propagating signal. It is thus desired to achieve a shorter length which would allow a smaller circuit size. In order to achieve such performances, the most practical method is to employ new designs at the layout by exploiting the slow-wave phenomenon of propagating waves in the structure. This design method allows the slow-wave CPW (S-CPW) [39] and slow-wave transmission line (SWTL) structures to exhibit high quality factors. First, a detailed description of the new asymmetric coaxial waveguide (ACW) structure is made. This is followed by a detailed explanation of how the Q-factor is analyzed with respect to conventional transmission lines. A brief review of the preceding work on SWTL is made for performance comparisons. These comparisons will be made with measured results in section 4.3.

4.1 The ACW Structure

This structure shown in Fig. 4.1 is designed with the pad metal as part of the ground structure which encloses a signal conductor. The signal conductor of our test structure is designed with a width of 12μm surrounded by ground metals on the sides as well as its top and bottom. The side ground metals are at w_g=44μm from the signal conductor. The top pad metal is designed with slot patterns and grounded. This thick top pad metal layer is not suitable to be used as the signal line due to Design For Manufacturability (DFM) constraints. The bottom metal is a slotted ground shield that prevents the electric field from penetrating the conductive silicon substrate. All the ground metals are connected together using inter-metal vias. Designed for our six-metal 90nm CMOS process, dummy ground metal strips are inserted between the signal line and the coplanar ground metal. No return current flows in these dummy ground metal strips because they are not connected together in the direction of the signal flow.

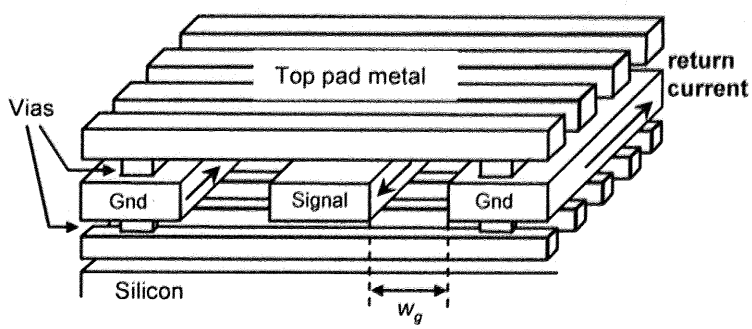


Fig. 4.1 The structure of the ACW.

The capacitance is determined by the distance between the signal and ground potential which increases with reducing distance. The inductance is determined by the distance between the signal path and the return current path which increases with increasing distance. Therefore, a trade-off exists between increasing the inductance and capacitance of the coplanar waveguides (CPW) and the microstrip line to decrease the phase velocity, v_p given in Eq. (4.1) to achieve

short wavelengths.

$$v_p = \frac{1}{\sqrt{LC}} . \tag{4.1}$$

Equation (4.1) is considered for a lossless case to emphasize the relation between the phase velocity and the line reactances. Through innovative designs, the return current does not necessarily have to flow in the closest metal of ground potential. The ACW achieves this by keeping the capacitance large with closely-located slot metals at the top and bottom where the return current cannot effectively flow. Instead, the return current is forced to flow at a farther distance at the sides. This results in a large inductance, as illustrated in Fig. 4.2.

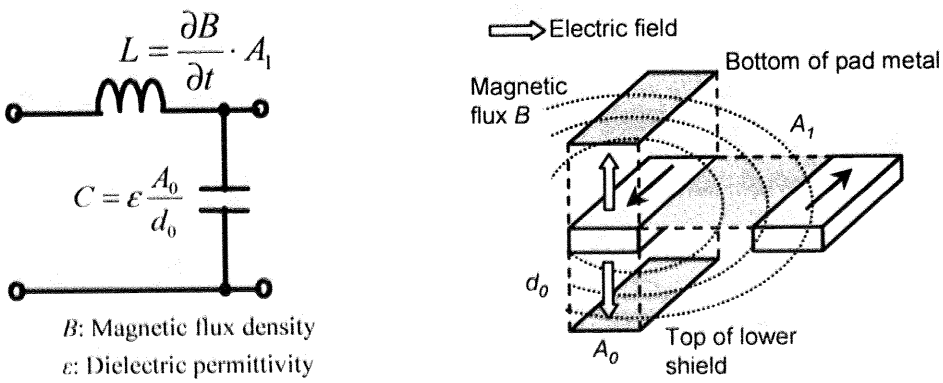


Fig. 4.2 Concept of the ACW. Increased area A_1 enclosed with farther side ground metals results in a larger inductance. d_0 is the decreased distance between the signal line and ground potential which allows larger capacitance to be achieved.

The wavelength of the signal wave is related to the phase constant:

$$\lambda = \frac{2\pi}{\beta} . \tag{4.2}$$

where λ is the wavelength and β is the phase constant. Hence, a large β results in a small λ and this corresponds to a shorter physical length to achieve a given fraction of the wavelength. Therefore, devices such as filters that require a determined wavelength can be fabricated using

this structure to occupy a smaller the area on the chip. This concept has been used in the design of the SWTL. The SWTL structure is fundamentally similar to the S-CPW except for the use of grounded shields instead of floating shields. Compared to the ACW, it also does not use a top pad metal layer.

4.2 Analysis of Inductive and Capacitive Quality Factors in Transmission Lines

A useful measure of characterizing the transmission line is to describe its quality factor (Q-factor). Different transmission line structures result in different Q-factors. For integrated circuits, transmission lines implemented in the form of CPW and microstrip lines are commonly used. The Q-factor of a transmission line can be calculated from the propagation constant to give $Q = \beta/2\alpha$, where α is the attenuation constant and β is the phase constant. Another useful measure of defining the Q-factor is obtained from the distributed model of the telegrapher's equations where the series resistance R and inductance L along with the parallel conductance G representing the leakage and capacitance C are defined. This leads to the definitions of Q_L and Q_C.

$$Q_L = \frac{\omega L}{R} \qquad \text{and} \qquad Q_C = \frac{\omega C}{G}. \tag{4.3}$$

Here, ω is the angular frequency. Transmission lines store mostly magnetic energy to resonate with the intrinsic capacitance of transistors. Thus, Q_L is crucial in determining the loss of the lines. Nevertheless, Q_C dominates under certain conditions. In commonly used CPW, Q_C is affected by the coupling to the substrate and is the limiting mechanism of the Q-factor. In general, the Q-factor can be calculated from Eq. (4.4).

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C}. \tag{4.4}$$

Therefore, to increase Q, it is necessary to increase both Q_L and Q_C.

Using the electromagnetic simulator, the 2D Extractor by Ansoft, values of the Q-factor, Q_L and Q_C of the CPW are obtained at 60 GHz. Fig. 4.3(a) shows the variations in these values of the CPW when the distance between the center signal line and the coplanar ground line w_g changes. This distance w_g between the center signal line and the two lateral ground lines determines the inductance L. Therefore, to increase L, w_g should correspondingly increase, thereby also increasing Q_L. However, if w_g is increased, the signal capacitance to ground C reduces and the leakage conductance G will be increased, leading to a lower Q_C. Therefore, increasing w_g will result in an increase in the Q-factor up to the point where the Q_L and Q_C curves will intersect and it will then decrease with increasing w_g.

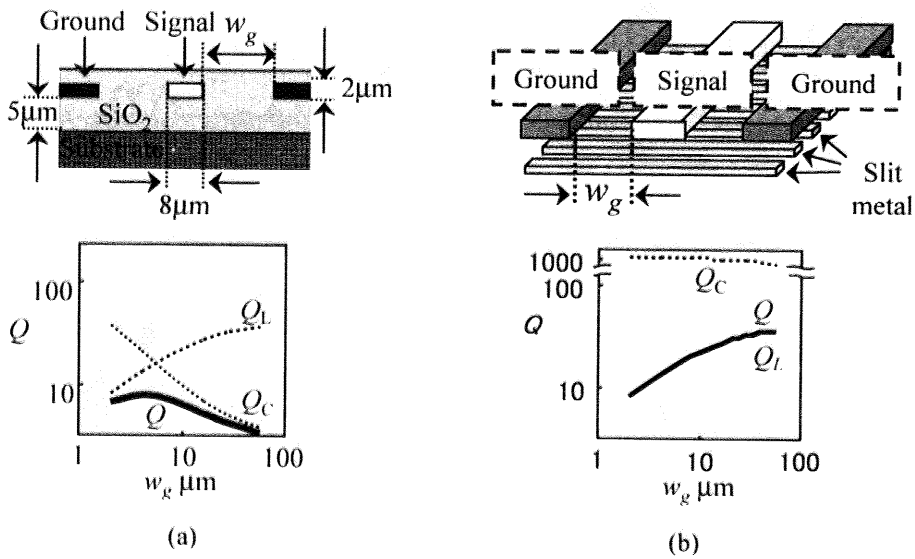


Fig. 4.3 (a) CPW cross section and its Q-factor; (b) S-CPW structural cross section and its Q-factor.

To evaluate the effects of the slot shield underneath the signal line, as for the case of the ACW and SWTL, an approximate floating shield structure is used for simulations. This structure is the S-CPW in Fig. 4.3(b) which is designed with a slot metal shield underneath the signal line. This slot metal shield cuts perpendicular to the flow of current in the signal line above; thus, this shield is able to effectively lower the induced current in it. The shield also reduces substrate

losses because it can effectively reduce the electric field entering the silicon substrate.

Having the advantages of the shield, the coplanar ground can be spaced further apart for a larger inductance without increasing substrate losses. This results in a capacitance per unit length C similar to that of the microstrip line. This follows then, that the wave speed and wavelength are lower with S-CPW, and such devices will use a smaller chip area. Also, the signal conductor is wider for the given characteristic impedance, thereby reducing copper losses. Figure 4.3(b) shows the simulation results of the Q-factor; the inductive and capacitive components Q_L and Q_C of S-CPW plotted as functions of w_g. It can be seen that the S-CPW can achieve a high Q_C because of the shield. A high Q_L is also achieved which is similar to the CPW because of the higher inductive coplanar grounds.

4.3 Experimental Results

The ACW is measured up to 110-GHz with Anritsu ME7808 with transmission- reflection modules. The micrograph of the ACW is shown in Fig. 4.4. Figure 4.5 shows a high phase constant that results in a short wavelength as described by Eq. (4.2). Compared to the conventional CPW and the microstrip line, its value is approximately 3.3-times higher. In addition, the ACW has a higher quality factor (Q-factor), compared to the conventional lines, as shown in Fig. 4.6. The Q-factor of the ACW, however, is not clearly better than that of the SWTL since it is expected that the Q-factors of substrate-shielded coplanar structures are similar since the Q-factor of both structures are not limited by any improved Q_C. The attenuations α, of the different structures are shown in Fig. 4.7. α partially determines Q since it is determined by Eq. (4.5).

$$Q = \frac{\beta}{2\alpha} \tag{4.5}$$

The higher measured attenuation of the ACW is due to the increased capacitance with the pad metal layer, which explains why the quality factor of the ACW is not significantly higher despite a high phase constant. There is thus a trade-off for high phase constant to achieve length reduction with attenuation. However, despite higher attenuation, the quality factor improves, as shown for the case of the ACW over the microstrip line and the CPW. All the lines are fabricated using the same process with a signal line width of 12μm and characteristic impedances between 20 and 50 ohms, shown in Fig. 4.8. As a result of employing ACW, circuits such as oscillators can achieve a significant area reduction as illustrated in Fig. 4.9.

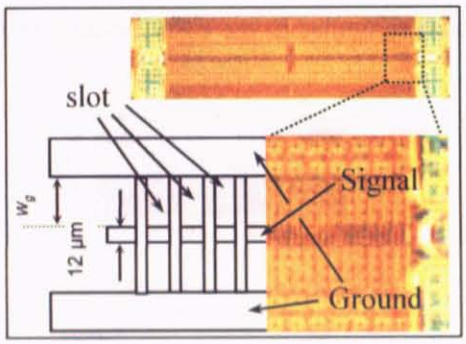


Fig. 4.4 Micrograph of the ACW.

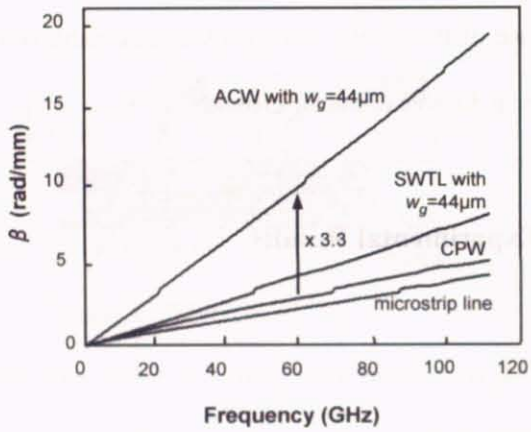


Fig. 4.5 Measured phase constant of the transmission lines.

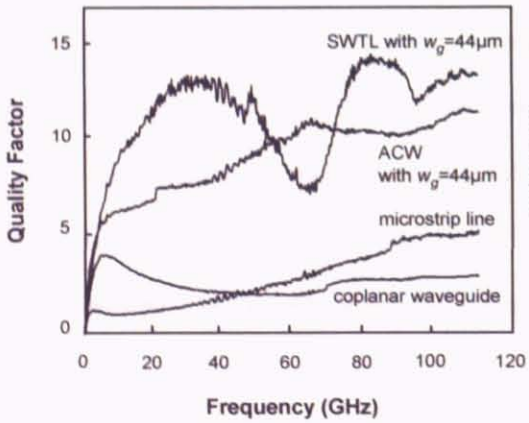


Fig. 4.6 Quality factor of the transmission lines.

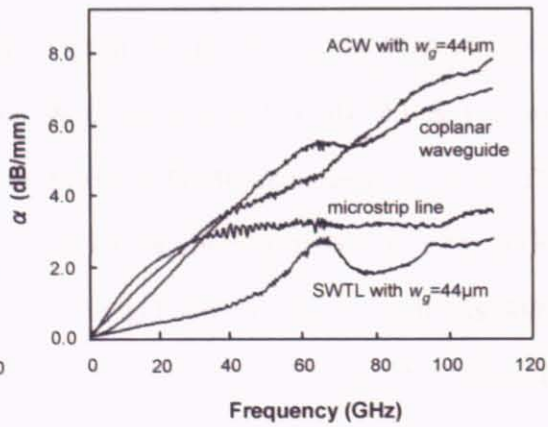


Fig. 4.7 Attenuation of the transmission lines.

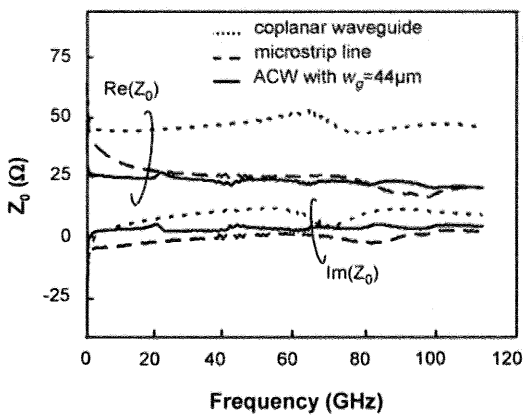


Fig. 4.8 Characteristic impedance of the transmission lines.

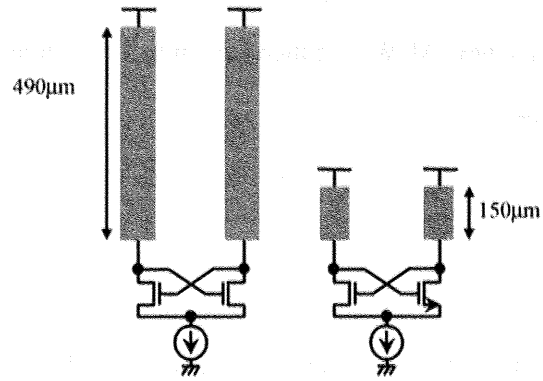


Fig. 4.9 Comparison of 60-GHz oscillators with quarter-wavelength transmission lines.

4.4 Chapter Summary

An ACW structure that uses the slow-wave concept is then presented for advanced CMOS processes which consist of a signal line surrounded by ground metals. This design increases the Q-factor and reduces the phase velocity for short wavelengths through large capacitance and inductance when compared to conventional CPW and microstrip lines. Using 2-D electromagnetic simulations, the Q-factor of the CPW and substrate-shielded S-CPW is evaluated for its inductive and capacitive components Q_L and Q_C. From the results, it is observed that the Q_C of the S-CPW with a slot metal shield is high as the shield suppresses the capacitive coupling to the substrate and thus minimizes the loss. In addition, the S-CPW also shows a high Q_L. Similar to the CPW, the high Q_L of the S-CPW is obtained because the ground can be placed farther from the return current path, thereby increasing the inductance per unit length. Applying this concept to the ACW, the inductance and capacitance can be varied almost independently of each other as the coplanar ground spacing controls the inductance while the shield affects capacitance. The high measured value of the phase constant confirms the short

wavelength of the signal propagating in the ACW structure. Up to 110-GHz, the physical length of the new ACW is reduced down to 30% while achieving the same wavelength as conventional lines.

Chapter 5

On-Chip Balun

This chapter continues the development of passive devices for the millimeter-wave transceiver circuits. The balance-unbalanced (balun) converter is a device that interchanges between a single-ended unbalanced signal and differential balanced signals. This function is frequently needed in balanced mixers and differential amplifiers in the transceiver circuit. Hence, on-chip CMOS baluns have been reported in recent works [44], [45]. On-chip balun offer high levels of integration for cost-savings and develop less parasitic due to shorter interconnections to devices. As a result, they are suitable for high frequency applications. It is, however, a challenge to obtain good performances with low losses when designing a passive balun on standard lossy silicon substrates. In addition, the balun should occupy a small area and maintain design simplicity. In this work, due to the broadband nature of the Marchand-type balun used, the design parameters can be easily estimated without complex calculations or time-consuming simulations. Section 5.1 describes the balun structure and design considerations. Section 5.2 reports the measurement results of the work.

5.1 Balun Design

The objective of the design is to realize a feasible balun structure that can be implemented in a high frequency circuit. For rapid simulations and high design error tolerance, a wideband, passive Marchand-type balun is used. Figure 5.1 shows the design of the balun. The shape of the balun is optimized to reduce occupied area and minimizes the distance between the differential

ports. The desired distance between the differential ports is closely affected by the layout requirements of the circuit that uses the balun. In general, a balun connects to the active devices through a minimum of interconnections, especially at high frequency. Therefore the differential ports are located close to the MOSFETs and to each other. Typical reported works of balun test structures occupy large area without an efficient shape for realization in a circuit [45].

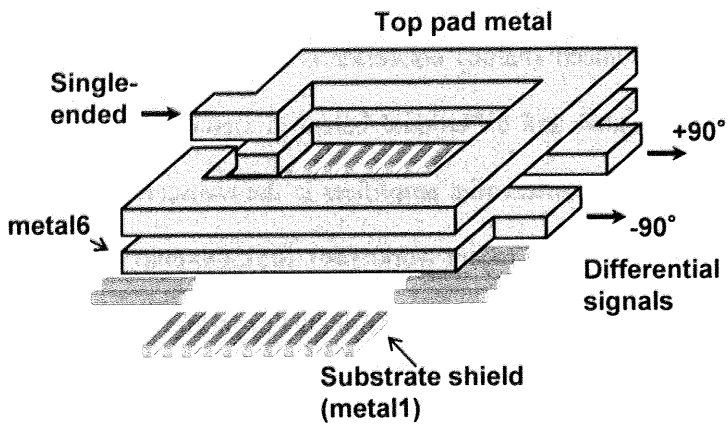


Fig. 5.1 Structure of the stacked on-chip balun includes the use of the top pad metal layer and two conductors on metal layer 6 with slotted shields placed below the metal.

This Marchand-type balun uses a thick top pad metal strip of half-wavelength. The single-ended port is at one end while the other end is left open-circuited. Two metal strips are located immediately under the top pad metal strip in the next highest metal layer. One end of each lower metal strip is connected to ground while the other end connects to each of the differential ports. This stacked structure allows the use of the thick top pad metal layer available in the process technology in a useful way, which normally is not suitable for carrying signals that are directly connected to the gate of the MOSFET, in order to satisfy the antenna rules. In addition, this stacked structure provides optimal inductive coupling, as compared to planar layout of the lines on the same metal layer. In this stacked design, all lines have the same width. Slotted ground shields are laid underneath the metal structures to prevent the electric field from penetrating the silicon substrate to induce substrate eddy currents.

The design of the balun requires determining of the length of the top pad metal strip and the width. Each of the two lower metal strips has half the length of the top pad metal to be at a quarter-wavelength long, less the gap distance between the differential port outputs. Determining the length requires an estimate of the effective permittivity. The effective permittivity is related to the wavelength of the propagating signal according to Eq. (5.1).

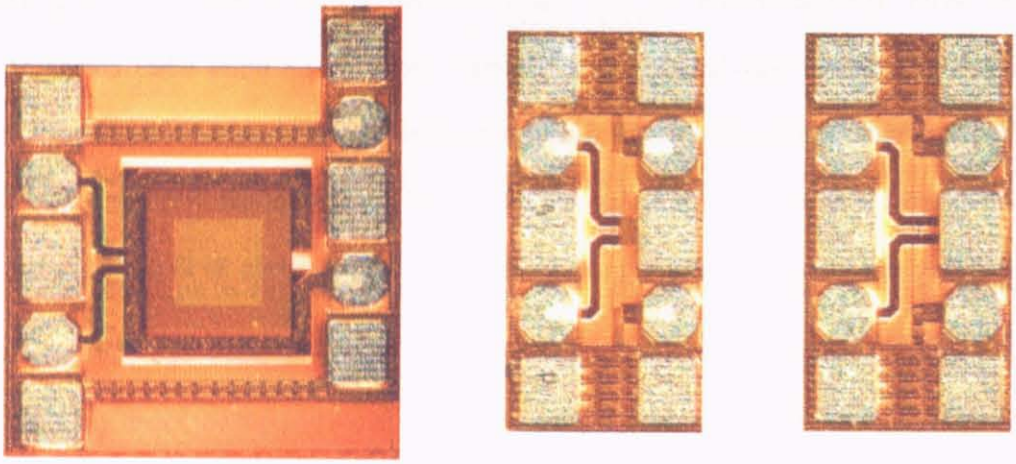
$$\lambda = \frac{c}{f\sqrt{\varepsilon_r}} \tag{5.1}$$

The value of the effective permittivity depends strongly on the structure of the transmission lines that forms the balun. For conventional microstrip line structure, the value is taken approximately at 4.0, using SiO_2. Transmission line structures using slow-wave designs are developed which has an effective relative permittivity of up to 15, according to its wavelength reduction factor. The lines used it this work has an effective relative permittivity of 7.6 and this corresponds to a shorter wavelength with a reduction factor of 2.8 times when compared to conventional microstrip lines. Due to the broadband nature of the Marchand balun, Eq. (5.1) is sufficient to provide an estimate for design and further EM simulations can determine the width for the required impedance. In this design, the widths are 12μm to obtain 50 Ω port impedances for measurements.

Finally, the position of the differential ports is determined by the gap distance required between them. It is necessary to consider the trade-off between placing them closely to minimize phase imbalance and placing them apart to reduce the parasitic capacitance. This design choice also considers the layout requirements of the circuit employing this device. In this design, a value of 10μm is selected that is able to maintain good phase balance as well as amplitude balance as shown in the results in the next section.

5.2 Experimental Results

The test structure is fabricated using a CMOS 90nm 6M1P process connected to two GSGSG pads for measurements using Anritsu 37397D vector network analyzer with a SM6000 four-port test set. This setup results in one dummy port that is not used. Nevertheless, standard 4-port open-short-through calibration can be performed with the existing calibration structures without any loss of accuracy. The open-short de-embedding method is then employed to remove the effects of the pads and the additional lengths that connect to the balun ports. Ignoring the measurements of the dummy port, the 3-port S-parameter matrix of the balun is obtained. Figure 5.2 shows the balun micrographs, including the open and short structures for de-embedding.



(a) (b) (c)

Fig. 5.2 (a) Micrograph of balun; (b) open structure (c) short structure.

Figure 5.3 shows the transfer characteristics of the balun. Port 1 of the scattering matrix refers to the single-ended port. Ports 2 and 3 refer to the differential balanced ports. Accordingly, |S21| and |S31| are the measured attenuations through ports 2 and 3 respectively.

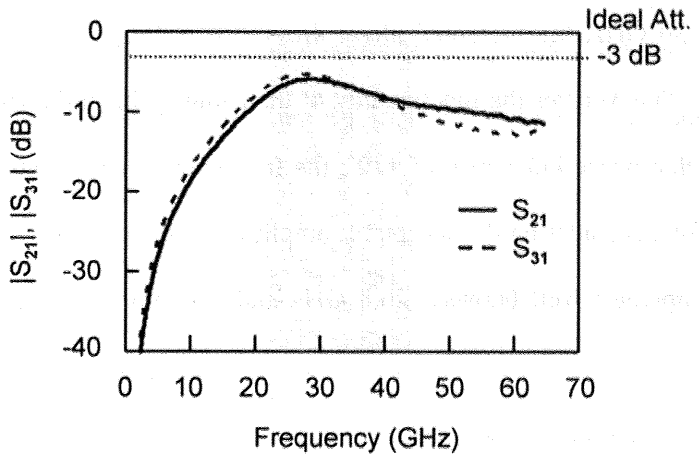


Fig. 5.3 Transfer characteristics of the balun. Port 1 refers to the single-end port. Ports 2 and 3 the differential balanced ports.

The theoretical values of |S21| and |S31| of an ideal balun are -3 dB, since each differential port divides to half of the power at the single-ended port. At 30 GHz, the measured values of |S21| and |S31| are -6.5 dB and -6.0 dB respectively. This calculates to an amplitude imbalance of 0.5 dB. Within an acceptable amplitude imbalance of ±1dB, the frequency range is between 22.4 GHz and 44.4 GHz. This large bandwidth indicates a good broadband amplitude balance. Figure 5.4 shows the measured phase difference between the differential ports after de-embedding.

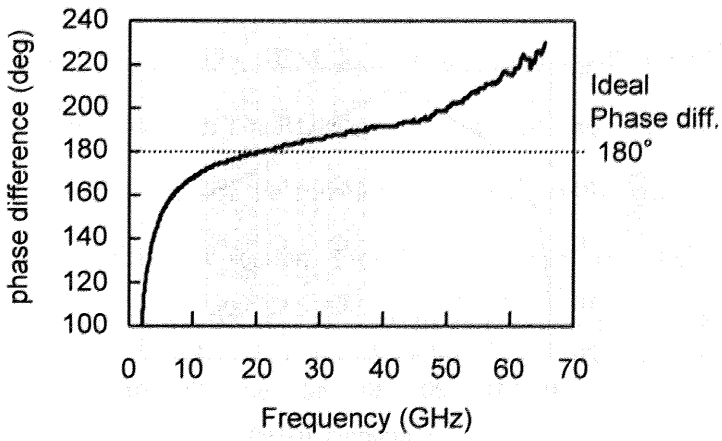


Fig. 5.4 Phase difference between the differential ports of the balun. At 30 GHz, the phase imbalance between the two ports is below 5 degrees.

For the proper functioning of the balun, the desired phase difference between the differential ports is 180°. At 30 GHz, the measured phase difference is 185°. This calculates to a phase imbalance of 5.0°. This verifies the functionality of the balun at the millimeter-wave frequency. Within an acceptable phase imbalance of ±10°, the frequency range is between 11.6 GHz and 37.3 GHz. Therefore, considering the acceptable amplitude imbalance of ±1dB in this frequency range, the balun operates well between 26.8 GHz and 37.3 GHz, confirming its broadband characteristics.

In order to analyze the use of the balun as an 180° power splitter, the common mode rejection ratio (CMRR) is calculated according to Eq. (5.2) [46], and shown in Fig. 5.5.

$$\mathrm{CMRR} = \left|\frac{S_{dm}}{S_{cm}}\right| = \left|\frac{S_{31} - S_{21}}{S_{31} + S_{21}}\right| \tag{5.2}$$

S_{dm} and S_{cm} denote the differential-mode and common-mode S-parameters respectively. Eq. (5.2) gives a single measure of the effects of both magnitude and phase imbalance in a splitter that can be readily calculated from measured data. At the desired frequency band, the differential-mode response is larger than the common-mode response to give a large value of CMRR. In the operating frequency band, the 180° power splitter has approximately 25.0 dB CMRR. The minimum measured CMRR is 21.0 dB.

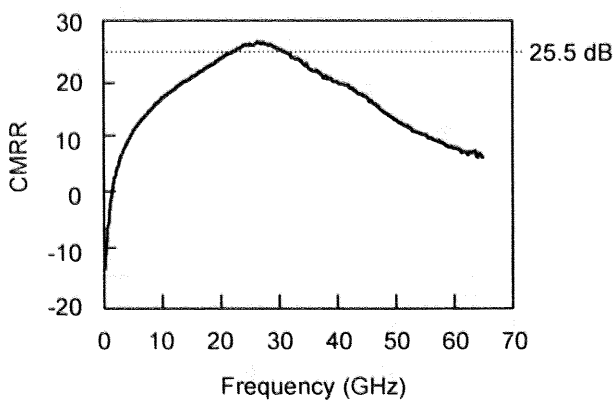
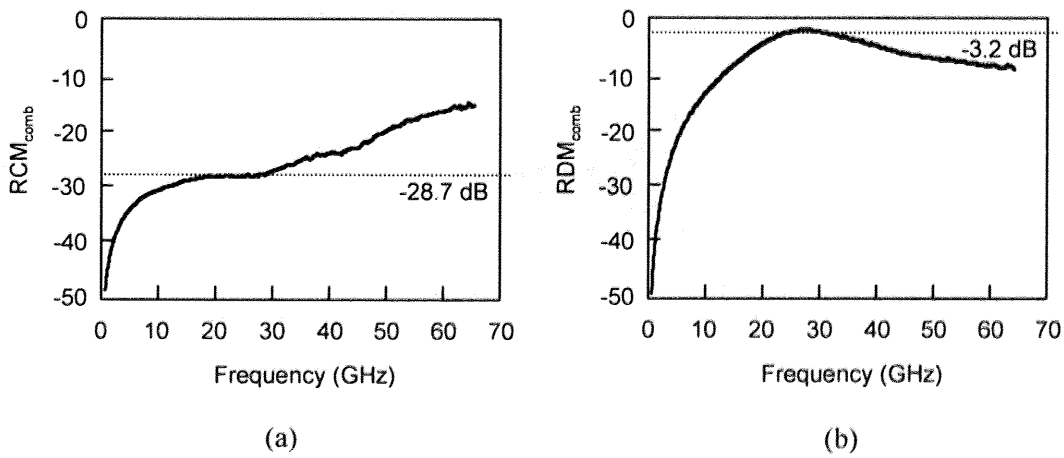


Fig. 5.5 CMRR of the balun when operating as a splitter.

When the balun is analyzed as an 180° power combiner, a rejection ratio cannot be directly applied. However, a common-mode response ratio (RCM_{comb}) and a differential-mode response ratio (RDM_{comb}) are defined by Eq. (5.3) and Eq. (5.4), plotted for the measured results in Fig. 5.6.

$$RCM_{comb} = \frac{1}{\sqrt{2}}|S_{12} + S_{13}| \tag{5.3}$$

$$RDM_{comb} = \frac{1}{\sqrt{2}}|S_{12} - S_{13}| \tag{5.4}$$



(a) (b)

Fig. 5.6 (a) Common-mode response; (b) differential-mode response of the balun operating as a power combiner.

The common-mode signal, measured by RCM_{comb}, is undesired and will affect the output of the combiner when there is an imbalance. The RDM_{comb} is the desired response of the combiner. Eq. (5.3) and Eq. (5.4) are amendments of the equations provided in [46]. The derivations for the equations are provided in the next section. From the measurements, the RCM_{comb} of the fabricated balun is -28.7 dB and the RDM_{comb} is -3.2 dB and these values can be verified using the identity given in Eq. (5.5).

$$CMRR = \frac{RDM_{comb}}{RCM_{comb}} \tag{5.5}$$

The measurement results compare well with works on reported baluns. In [44], the balun operates from 25 GHz to 40 GHz designed for 0.24μm SiGe BiCMOS and occupies 285μm×1333μm. In [45], the balun operates from 800 MHz to 2.5 GHz designed for 0.18μm CMOS and occupies 250μm×250μm.

5.3 Derivations for RCM_{comb} and RDM_{comb}

The derivations for RCM_{comb} and RDM_{comb} shown below are amendments to [46].

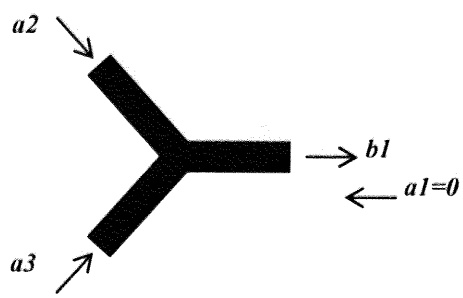


Fig. 5.7. The output of the combiner is labeled as port 1. The inputs of the combiner are identified as ports 2 and 3.

Note the relationship $\begin{pmatrix} b_1 \\ b_2 \\ b_3 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \end{pmatrix}$, where $b_1 \neq 0, a_2 = a_3 \neq 0$ for this case.

Hence, $b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3$, $a_1 = 0$

Define $a_{cm} = \dfrac{|a_2 + a_3|}{\sqrt{2}}$ and $a_{dm} = \dfrac{|a_2 - a_3|}{\sqrt{2}}$. When $a_{dm} = 0$, $a_2 = a_3$.

The basic definition of RCM_{comb} is $\left|\dfrac{b_1}{a_{cm}}\right|_{a_{dm}=0}$, therefore

$$
\begin{aligned}
\mathrm{RCM}_{\mathrm{comb}} &= \left| \frac{b_1}{(a_2 + a_3)/\sqrt{2}} \right|_{a_{dm}=0} \\
&= \sqrt{2} \left| \frac{S_{11}a_1 + S_{12}a_2 + S_{13}a_3}{a_2 + a_3} \right|_{a_2=a_3} \quad \text{(Remember that } a_1 = 0\text{)} \qquad (5.6) \\
&= \sqrt{2} \left| \frac{S_{12} + S_{13}}{1+1} \right| \\
&= \frac{1}{\sqrt{2}} |S_{12} + S_{13}|
\end{aligned}
$$

The basic definition of $\mathrm{RDM}_{\mathrm{comb}}$ is $\left| \frac{b_1}{a_{dm}} \right|_{a_{cm}=0}$, therefore

$$
\begin{aligned}
\mathrm{RDM}_{\mathrm{comb}} &= \left| \frac{b_1}{(a_2 - a_3)/\sqrt{2}} \right|_{a_{cm}=0} \\
&= \sqrt{2} \left| \frac{S_{11}a_1 + S_{12}a_2 - S_{13}a_3}{a_2 + a_3} \right|_{a_2=-a_3} \qquad (5.7) \\
&= \sqrt{2} \left| \frac{S_{12} - S_{13}}{1+1} \right| \\
&= \frac{1}{\sqrt{2}} |S_{12} - S_{13}|
\end{aligned}
$$

5.4 Chapter Summary

An on-chip stacked Marchand balun has been realized using CMOS 90nm process technology for potential applications in the millimeter-wave frequency band. The balun structure has been optimized for the process design rules by employing the top pad metal and thin slotted ground metal shields. As a result, it consumes a small area of 229μm×229μm. At 30 GHz, the measurements show an amplitude imbalance of 0.5 dB and a phase imbalance of 5.0°. The balun operates within an amplitude imbalance of ±1dB and a phase imbalance of ±10° between 26.8 GHz and 37.3 GHz. To evaluate the balun as a power splitter, the CMRR is calculated to be 21.0

dB at 30 GHz. For evaluation as a power combiner, the expressions for RCM_{comb} and the RDM_{comb} are derived. They are then calculated from measured results to have a value of -28.7 and -3.2 dB, respectively. This balun design has been successfully employed in the up-conversion mixer circuit, described in chapter 6.

Chapter 6

20-26 GHz Up-Conversion Mixer

This chapter begins the details on the active circuits in the transceiver. For the ultra-wide band (UWB) vehicular radar transceiver operating in the 22-29 GHz frequency range, up-conversion mixers above 20 GHz are required. Until recent years, CMOS has not been able to achieve this operating frequency and it is necessary to employ compound semiconductors. CMOS technology, besides consuming less power, has the potential to integrate with digital technology. In addition to the design for low power consumption, it is necessary that the mixer circuit does not suffer excessive conversion losses. With advances in filtering technology [47], [48] in recent years, allowing up to 30 dB attenuations at 20 GHz with high Q, a review of the use of the up-conversion mixer topology is necessary.

A double-balanced Gilbert mixer has been widely used in analog and RF circuits to implement mixers because of excellent port-to-port isolation. The single-balanced mixer can be used to reduce power consumption because less number of active devices is employed. The separate feeding ports for IF and LO in a single-balanced mixer provides good isolation between IF and LO ports. However, excellent IF-RF and LO-RF port-to-port isolation can be achieved only if a double-balanced Gilbert mixer is fed with balanced IF and LO signals and the output RF signals are taken differentially. Nevertheless, the LO-RF isolation of the single-balanced mixer is still superior to the isolation provided by a single transistor mixer. In fact, the common-mode rejection provided by the biased current source in a conventional double-balanced Gilbert mixer deteriorates rapidly at high frequency [49]. Therefore, at high frequency, it is practical to

challenge the single-balanced topology for gain and reduced power consumption at high gigahertz bands while reducing the LO with advanced filtering techniques.

The single-balanced topology, as used in this work, can also achieve moderate gain and a low noise figure. Less chip area is required since a balun is not required for the IF input, compared to that of the double-balanced mixer. However, this topology has low 1-dB compression point and high input impedance. To our knowledge, existing implementations on CMOS have achieved 24 GHz with high gain at a power consumption of 12.5mW [50], as at the time of this writing, with the current-reuse technique [51] to provide more current to the transconductance FETs. In this work, a fully integrated 20-26 GHz broadband up-conversion mixer with on-chip baluns is demonstrated on 90nm CMOS technology. The maximum power consumption is 11.1mW from a 1.2V dc supply.

6.1 Up-Conversion Mixer Design Methodology

The mixer topology used for this work is shown in Fig. 6.1 which uses the single-balanced design. The input and output power are transferred using the impedance match of the on-chip baluns.

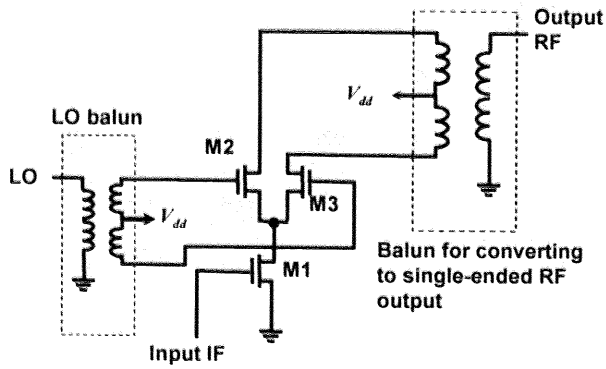


Fig. 6.1 Schematics of the up-conversion mixer circuit.

The differential output RF signal is converted to a single-ended output using a substrate-shielded Marchand-type balun. The balanced LO signal is also provided through another balun. Common-mode noise produced by the switching transistors and LO-port is rejected at the differential output. However, there remains a direct noise current path between the output terminals during a time interval around the zero-crossing of the LO voltage. Since the noise scales with the size of the M2 and M3, the transistors should not be large. Furthermore, LO signals need to be sufficiently high to fully switch the transconductance current to flow through either of M2 or M3. At low supply voltages, special considerations are necessary. M1 is usually biased in the strong inversion and saturation to achieve conversion gain, good linearity and low noise. With V_{gs} for the optimum transconductance g_m at about 0.65V and a threshold voltage of 0.3V for the technology used, the minimum voltage required to turn the switching transistors on is near to 1V. Therefore, possible voltage headroom required by de-generation resistors is avoided. Since the configuration is optimized for gain with low power, rather than linearity, inductive de-generation is not applied. Furthermore, the conventional method of operating M2 and M3 in saturation also requires significant voltage headroom, reducing the headroom available for any resistive load with broadband operations and hence limiting the achievable conversion gain. A finite external load will further reduce this limit. This problem is overcome in this design by allowing the single-ended output signal to be drawn by the capacitive coupling of the balun which appears as high impedance to the output of the mixer core.

6.2 Stacked Marchand Balun Design

Passive baluns do not consume any power and topologies such as the Marchand-type balun provide broadband response with low losses at the pass-band. This section describes the implementation of the on-chip balun, as described in chapter 5, for the mixer circuit. The

Marchand balun provides single-ended signal to differential signal conversion by using coupling across a half-wavelength line. Signal is input into the half-wavelength line at port 1 as shown in Fig. 6.2 and output is taken from the ends of two quarter-wavelength lines at ports 2 and 3.

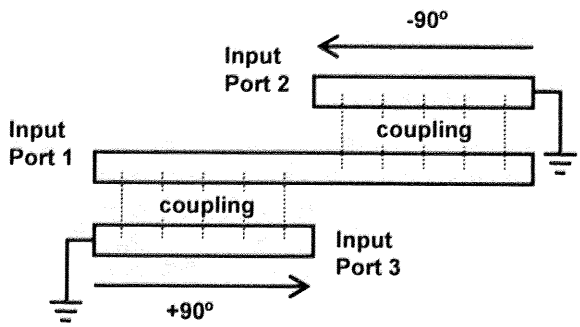


Fig. 6.2 Operating principle of the Marchand balun.

The opposite ends of the quarter-wave lengths lines are connected to a common ground potential, hence the outputs at ports 2 and 3 have a phase difference of 180 degrees. To ensure amplitude balance, the two quarter-wave lines are placed at the same distance away from the half-wavelength line. For sufficient power to be transferred to both the coupled lines at the LO input and the load at the RF output, sufficiently strong coupling is required. In the conventional implementations of the Marchand balun on thick dielectrics [52], [53], coupling between the coplanar half-wavelength and quarter-wavelength lines are significantly stronger than the leakage capacitance across the dielectric. However, for implementations on CMOS, large capacitive losses results from the thin dielectric between the conducting metal and the ground metal underneath (~2.9μm). This distance is significantly smaller than the distance between the coplanar half-wavelength and quarter-wave length lines on the same metal layer. Therefore, to achieve the strong coupling required, the coupling is increased by reducing the distance between metals through stacking. Stacking is achieved by using the pad metal for the half-wavelength line and the next highest metal layer for the quarter-wavelength lines. As illustrated in Fig. 6.3, the single-ended signal is input into thick pad metal and capacitive-coupled to the two lines on

metal 6 below where the signal exits differentially.

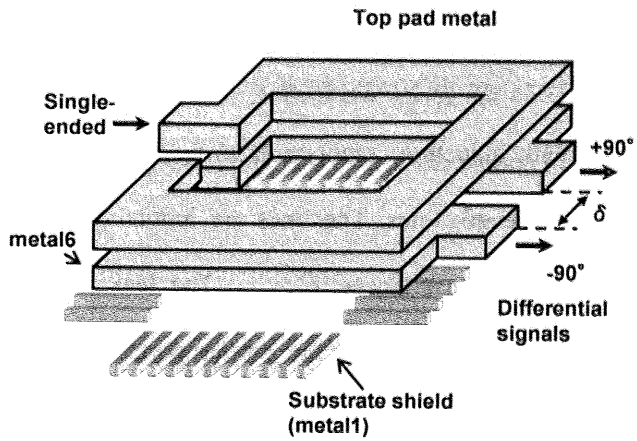


Fig. 6.3 Multi-layer stacked balun design with substrate shield.

The loss in the structure can further be reduced with substrate shielding. The substrate shield is realized with slotted shield structures are placed underneath the balun. This shield reduces the speed of the propagating wave and results in a shorter physical length that corresponds to the required wavelengths. The shield also prevents the electric field from penetrating the conductive silicon substrate. To ensure sufficient power transfer from the coupled quarter-wave lines to the input/outputs of the balun, sufficiently high impedance for matching is desired. In this implementation, the ground slot shield is located nearest to the coupled lines and thus determines the capacitance to ground. The line inductance is determined by the distance of the signal line to the return ground current, which are located further away. Thus, the inductance and the capacitance can be controlled fairly independently to achieve the required impedances, similar for the case of the slow-wave transmission lines (SWTL) as described in chapter 3.

The shape of the balun is constructed in the form of a square to minimize required chip area and to allow the differential ports to be located closely. It is necessary to locate the ports closely since they connect to the switching transistors that need to be well matched. Any extra length on the layout for the interconnections between the balun and the transistors will affect the transfer

characteristics. However, due to physical layout constraints, the differential ports cannot fully couple to half the length of the half-wavelength line and leaves a gap with a distance of δ. This distance δ between the terminals of the differential ports must be spaced closely to achieve good anti-phase. The coupling effects are illustrated by a simplified lossless model in Fig. 6.4. This model describes the balun with inductive components along the length of the half-wavelength line and the two quarter-wavelength lines. The lines are inductively coupled together with a coupling coefficient k and have capacitances, $C_{coupling}$. The leakage capacitive losses to the ground are through C_{loss}. The space between the output ports is represented by a parasitic capacitance C_{gap}.

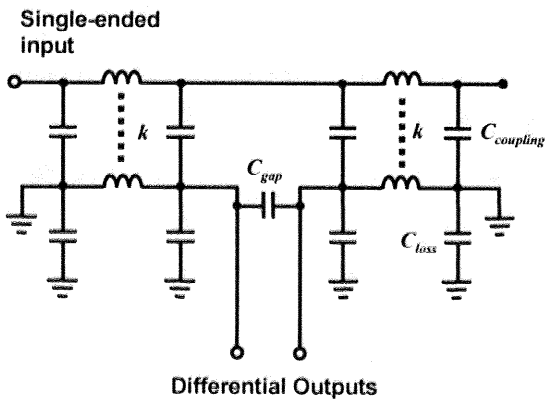


Fig. 6.4 Simplified stacked Marchand balun equivalent circuit ignoring resistive losses illustrating the capacitive coupling and losses.

From Fig. 6.4, it can be seen that the capacitive losses through C_{loss} should be minimized and the $C_{coupling}$ maximized. However, since the width of the metal lines affects the required impedance as well as the desired capacitances for coupling, an optimized value should be used. For the case of the coplanar implementation described previously, more capacitive losses occur since both the half-wavelength line and the quarter-wavelength lines suffer capacitive losses. For the case of the stacked implementation, only the quarter-wavelength lines are directly coupled to the ground. The half-wavelength line couples to the quarter-wavelength lines through a short inter-dielectric layer distance of only 1.12μm.

Fig. 6.5 shows the simulation results of the output balun using the proposed circuit model of Fig. 6.4 and comparing it to the results generated by 2.5-D layout simulator ADS Momentum. Port 1 refers to the single-ended, while ports 2 and 3 refer to each of the differential ports. The two sets of simulation results agree fairly well. Both show an insertion-loss of less than 6 dB at the pass-band from 20 GHz to 24 GHz while the phase difference is within 5 degrees from the desired value of 180 degrees.

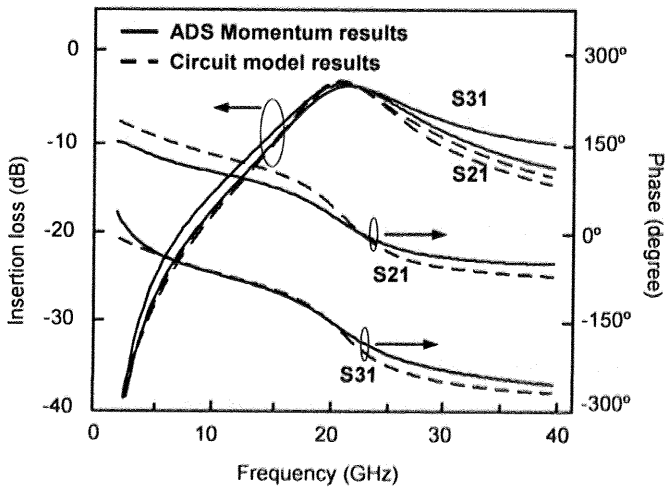


Fig. 6.5 Simulation results of the output RF balun.

Table 6.1 Balun Design Parameters.

Widths	12 μm
Gap distance, δ	10 μm
Effective wavelength	1716 μm (LO balun) 1460 μm (RF balun)
Elemental shield width	1 μm

Table 6.1 shows the summary of the design parameters used. The width of the balun is designed to match the LO and RF ports of the mixer to the pads for measurements. Table 6.2 shows the simulated port impedances. The pads are modeled with an impedance 45-j3.1Ω at the center frequency of 22 GHz.

Table 6.2 Mixer Design Parameters at 22 GHz.

Simulated impedance at each differential LO port	12.6-j131Ω
Simulated impedance at each differential RF port	30.3-j0.1Ω

6.3 Experimental Results

The up-conversion mixer was designed and fabricated using a six-metal 90nm CMOS process. The additional pad metal layer available is utilized as one of coupled lines of the baluns for the single-ended input/output. On-wafer measurements are performed because the fabricated circuit allows a GSG single-ended IF input, a GSG single-ended RF output and the LO supplied through another GSG single-ended input. The LO frequency is varied between 17.3 GHz and 23.3 GHz. This allows an RF output of 20-26 GHz using a 2.7 GHz IF. Figure 6.6 shows the micrograph of the fabricated chip. The size is 650μm×570μm.

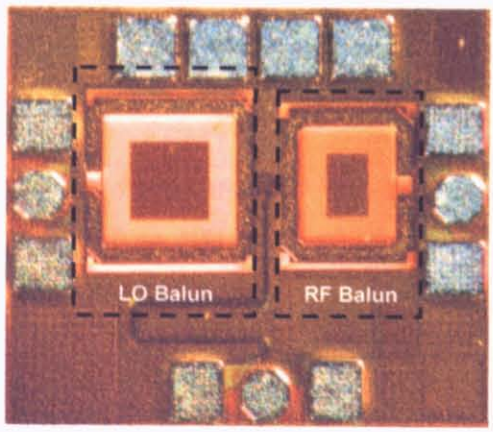


Fig. 6.6 Micrograph of mixer with on-chip baluns.

The circuit has a large matching bandwidth for the LO and RF output at where the baluns are

used. *S*-parameter measurements are taken with the circuit bias voltages. The input and output of the network analyzer are used to probe the LO and output RF ports to evaluate the balun matchings.

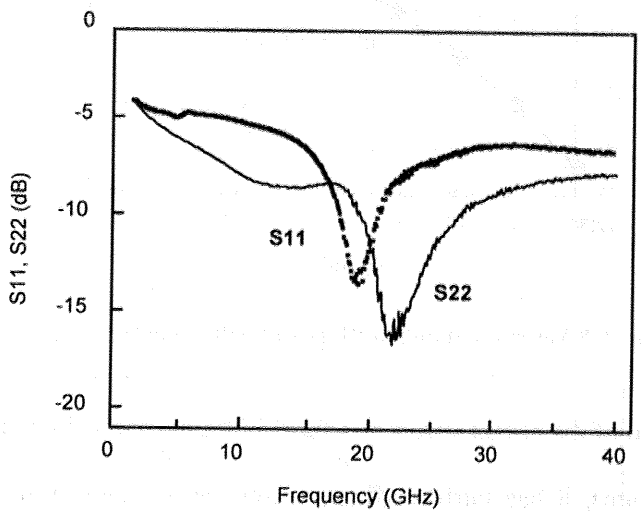


Fig. 6.7 Measured S11 for LO balun matchings and S22 RF output balun matchings.

From Fig. 6.7, the output matching, S22 has a return loss better than 10 dB for frequencies from 20 GHz to 26 GHz. The matching to LO, S11 achieves a minimum of -14.0 dB at 19.4 GHz. Small signal S-parameters are used to determine the range of the operating frequency for low power conditions. For large power levels, linear assumptions of the S-parameter measurements do not hold. Therefore, direct power measurements are taken to verify the characteristics. In addition, since the output impedances at the drain of the switching transistors are a function of the gate voltage of the switching transistors M2 and M3, and S22 is a measure of the degree of impedance matching at the output (to 50Ω), S22 should be measured while the LO signal is being applied.

Power measurements were taken across the frequency band of interest. Figure 6.8 shows the measured output power at the center RF frequency of 22.1 GHz with an input IF signal at 2.7 GHz. The up-conversion mixer exhibits a conversion gain of 2 dB and achieves an input-referred 1-dB compression point of -14.8 dBm.

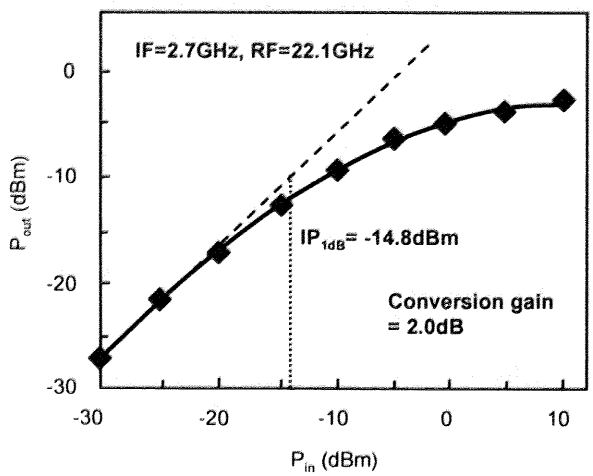


Fig. 6.8 Variation of output RF power with input IF power.

The power consumption of the circuit varies as a function of the applied voltage and LO power. For each set of conditions, it has fairly constant power consumption at low input IF power. Conversion gain decreases as the applied voltage or LO power decreases. Figure 6.9 shows the conversion gain variations with the output frequency. The input IF is maintained at 2.7 GHz and the LO frequency is varied between 17.3 GHz and 23.3 GHz. The results show a conversion gain with a minimum of -3 dB across the 20-26 GHz band.

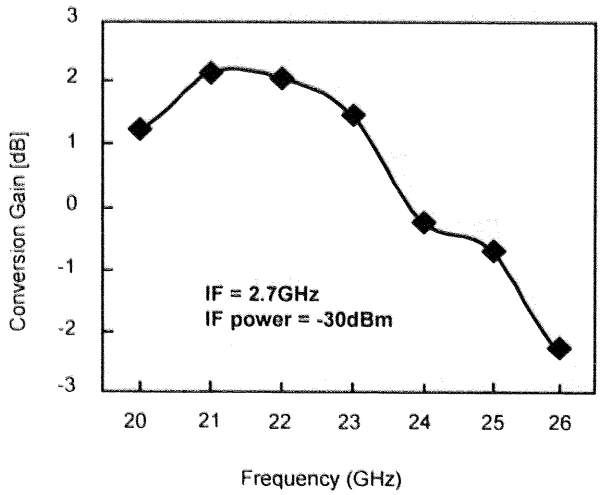


Fig. 6.9 Plot of conversion gain variations with RF frequency.

Figure 6.10 plots the IF-RF isolation at an input IF power of -30 dBm. The result shows a

minimum of 10 dB isolation up to 26 GHz. At the designed balun frequency of 22 GHz, an isolation of 18 dB is obtained. Reduction in isolation can be caused by fabricated balun imbalances as well as poor transistor matching. It is reasonable for a narrowband power amplifier to increase the output power from the output RF signal of the mixer so that it will further increase the IF-RF isolation at the transmitter output. For vehicular radar applications, FCC limits emission to -60 dBm below 22 GHz and -40 dBm from 22 GHz onwards. It will be satisfactory if all signals keep below these limits even under weak IF-RF isolation performances.

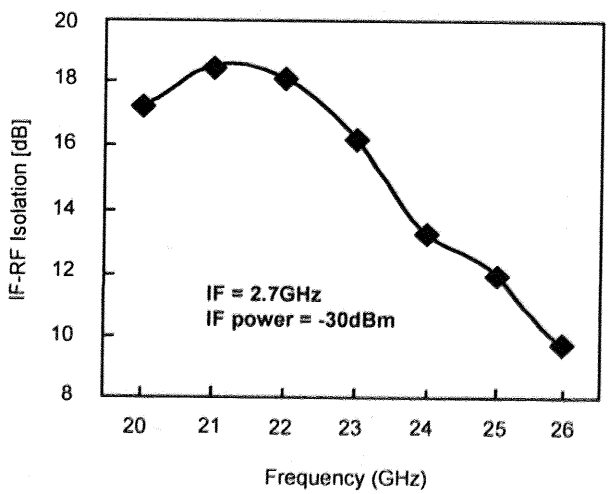


Fig. 6.10 Plot of IF-RF isolation variations with RF frequency.

Figure 6.11 shows the 1-dB compression point of the mixer. Across the measured band, the minimum value is obtained at 25 GHz corresponding to a -16.5 dBm input power. Considering the low emission limit of -41.3 dBm/MHz in the required bandwidth of 500 MHz for the automotive radar application [54], high 1-dB compression points are not required.

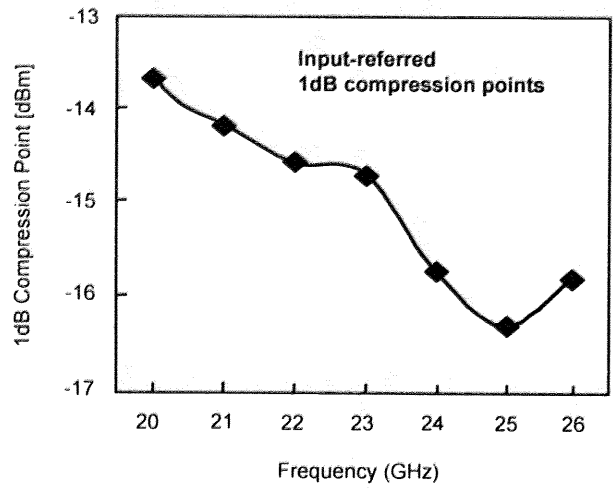


Fig. 6.11 Plot of 1-dB compression point variations with RF frequency.

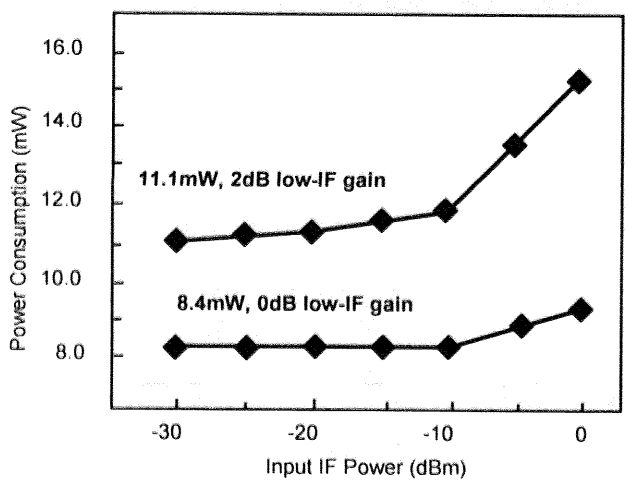


Fig. 6.12 Power consumption with varying IF input power.

As shown in Fig. 6.12, the mixer circuit consumes 11.4mW at low input IF when the voltage supply V_{dd} is at 1.2V using an LO output of 5 dBm. This produces a conversion gain of 2 dB before compression. At a reduced V_{dd} of 1.0V and LO output of 3 dBm, the gain obtained is 0 dB. When such a gain level is acceptable, the required power is only 8.4mW. The region of high input IF power corresponds to saturated output power region and does not provide any gain.

Table 6.3 Up-Conversion Mixer Measurements.

Matched RF Frequency	20-26 GHz
IF Frequency	2.7 GHz
Max. Power Gain	2 dB@22.1 GHz
Max. Power Dissipation	11.1mW
IF-RF Isolation	18 dB@22.1 GHz
Input 1-dB Compression Point	-14.8dBm@22.1 GHz

Table 6.3 summarizes the performance of the broadband mixer circuit. With emphasis on low power consumption, the performance is comparable to up-conversion mixers fabricated on other semiconductor technologies. Figure 6.13 makes a comparison.

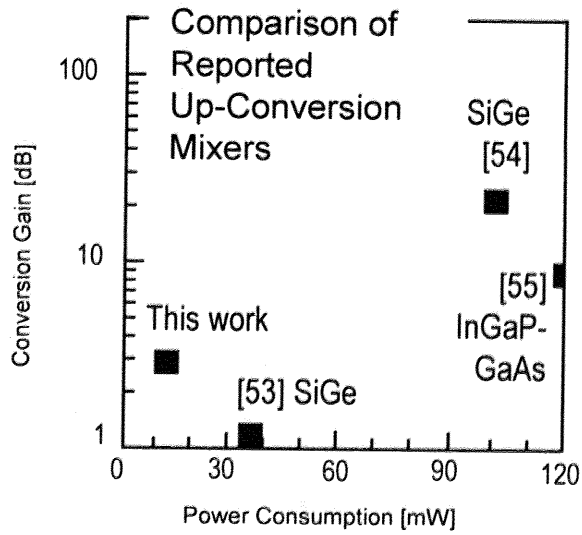


Fig. 6.13 Comparison of conversion gain and power consumption with other reported works.

6.4 Chapter Summary

With the advancement in filtering technology, the single-balanced mixer is reviewed for use in up-conversion mixing. This work demonstrates a fully integrated broadband up-conversion single-balanced mixer with on-chip baluns to enable a single-ended input and a single-ended

output. The baluns are constructed with the top pad metal and the next highest metal layer for increased coupling and they provide impedance matching to improve conversion gain. Slotted substrate shields are laid under the balun structures to reduce substrate losses and provide reduced physical lengths. The occupied areas of the baluns are 229μm×229μm and 182μm×212μm for the LO feed and the RF output, respectively. The total die size is 650μm×570μm. At 22.1 GHz, the integrated mixer achieves a conversion gain of 2 dB with a maximum power dissipation of 11.1mW from a 1.2V dc power supply at LO power of 5 dBm. These results are comparable to mixer circuits fabricated using high-performance semiconductor processes. Input referred 1-dB compression point is -14.8 dBm. The LO and RF return loss are better than 10 dB for frequencies from 20-26 GHz.