Chapter 7

60 GHz Down-Conversion Mixer

The 57-64 GHz licensed-free band in the United States and 59-66 GHz in Japan has driven the development of 60 GHz systems in recent years. This includes the development of the receiver on digital CMOS technology with potential applications in wireless HDMI and WPAN. The feasibility of the CMOS transceiver has been studied and works on its building blocks are reported [58]. One of these blocks is the frequency down-conversion mixer which forms a critical part of the receiver. The down-conversion mixer converts a high radio-frequency (RF) signal at the input to an intermediate frequency (IF) at the output through the use of a local oscillator signal (LO).

Among the important figures of merit to consider in the design of the mixer is the linearity. The linearity is important because the mixer is the first block in the receiver to handle large power, being located immediately after the low-noise amplifier (LNA). Determining the 1-dB compression point, it gives rise to the dynamic range of the mixer. A higher 1-dB compression point allows a larger input power range, which is the difference between this point and the noise floor. A higher 1-dB compression point will also result in a higher IM3 intercept, whose value can be approximated to 10 dB above the 1-dB compression point [59]. Therefore, the IM3 intercept is an alternative way to evaluate the mixer's signal handling capability.

High linearity can be achieved with passive mixers. However, its obvious drawback is the associated high conversion loss because the mixer's zero power consumption cannot boost the strength of the frequency-converted signal. Minimizing the loss of the signal is important

because sufficiently high power may be needed to drive the subsequent stages in the receiver. In fact, it is a challenge to obtain high gain at 60 GHz in the preceding LNA due to the limits in the f_T of the process. It is thus necessary to provide minimum conversion loss in the subsequent down-conversion mixer stage to reduce the burden on the LNA. Thus, we focus on the design of a mixer that achieves linearity while having minimal conversion loss. In addition, designing on advanced CMOS processes can allow integration with high speed digital circuits. However, RF design on advanced CMOS processes has been challenging. One of the issues is the high cost of the chip area. This translates to a need to reduce the design area for achieving a specific function under certain performance requirements. Small chip area can be realized by using slow-wave transmission lines for impedance matching instead of using conventional microstrip lines. Simple test structures utilizing the slow-wave phenomenon have been reported in earlier works [60]. In this work, SWTL is employed to realize a mixer with high linearity, low loss and small chip area.

7.1 Mixer and Slow-Wave Transmission Lines

The down-conversion mixer consists of the core mixer and a buffer stage. Figure 7.1 shows the schematics of the mixer circuit using on-chip transmission line for impedance matching. The core mixer is a cascode stage which is made up of a transconductance (g_m) stage, M1 and a switching MOSFET, M2 which performs the frequency mixing. M1 is therefore biased to obtain a high g_m while M2 is biased near threshold to enable effective switching.

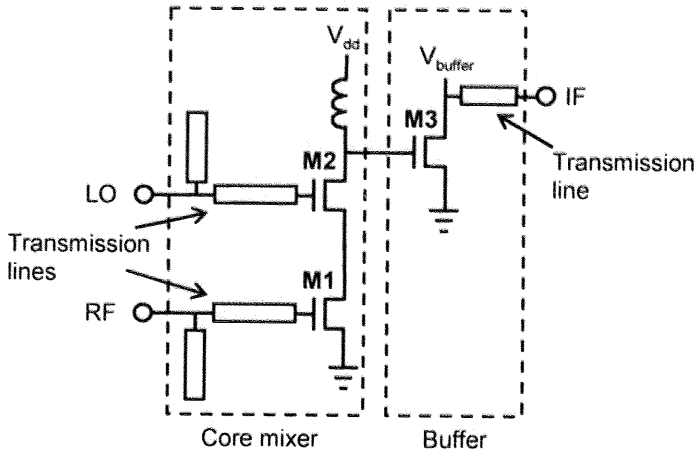

Fig. 7.1 Schematics of down-conversion mixer circuit using transmission lines for impedance matching.

The advantage of using a cascode topology is that it allows the RF input and the LO signal to be fed into two different MOSFET gates, avoiding the need for area-consuming power combiners. Since the LO and RF rejections at the IF output are not so critical due to the large spectral differences, this topology can be employed instead of Gilbert mixers and thus avoiding the use of lossy baluns. The common-source output stage M3 in the circuit boosts the output gain while providing impedance match to the output ground-signal-ground (GSG) pad and the IF signal port. In principle, the necessity or design of this stage depends on the impedance of its subsequent stage in the receiver module. In this work, the mixer circuit is connecting directly to the GSG pads.

The modeling of the MOSFET has been performed by capturing the extrinsic high frequency parasitics using on-wafer S-parameter measurements up to 65 GHz. These parasitic components are added to the BSIM model obtained by the low-frequency parameters. The slow-wave transmission line (SWTL) is used for implementing the matching networks between the pads and the mixer inputs/output. Analysis of this structure is described in chapter 4. Figure 7.2 shows the structure of the SWTL.

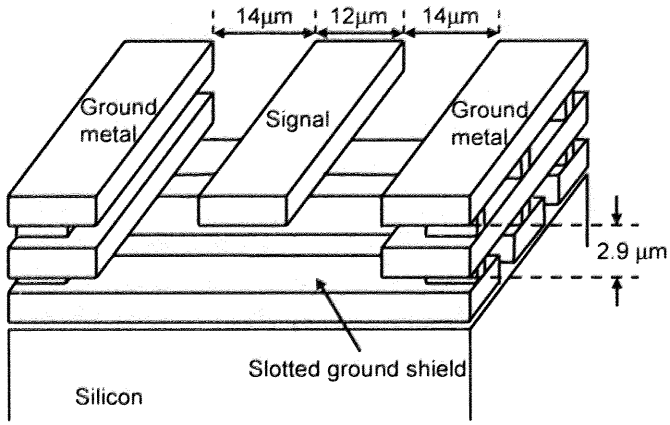

Fig. 7.2 Simplified structure of the slow-wave transmission line used in the circuit.

The structure of the SWTL consists of slotted ground shields underneath the signal line which are laid orthogonal to the direction of the current flow. This structure results in the propagating wave having a lower phase velocity. Therefore, the corresponding wavelength at a given frequency reduces. In the design of the matching circuit requiring a given number of wavelengths, shorter physical lengths can be realized on the layout.

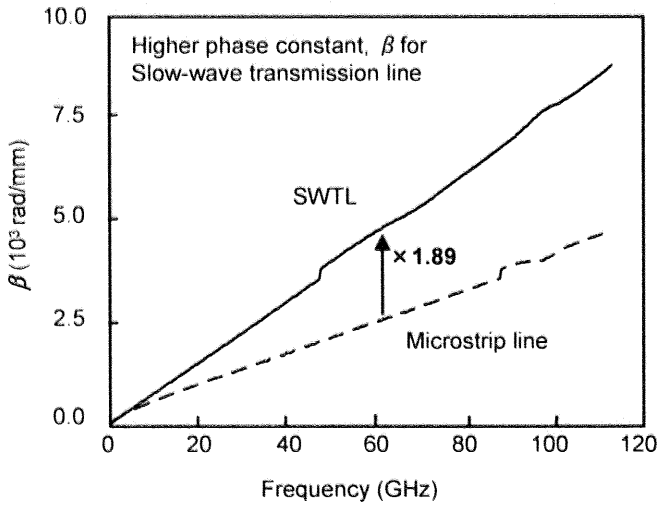

Fig. 7.3 De-embedded S-parameters of the measured slow-wave transmission line and microstrip line. Both have lengths of 900μm and widths 12μm, fabricated on the same chip.

Figure 7.3 shows the increase in the phase constant, β of the SWTL as compared to the microstrip line (MSL) to result in a shorter wavelength, λ as given in Eq. (7.1).

$$\lambda = \frac{2\pi}{\beta} \tag{7.1}$$

To use these lines in the mixer circuit, test structures were fabricated. They are measured and modeled. Figure 7.4 shows the measured and modeled results up to 60 GHz.

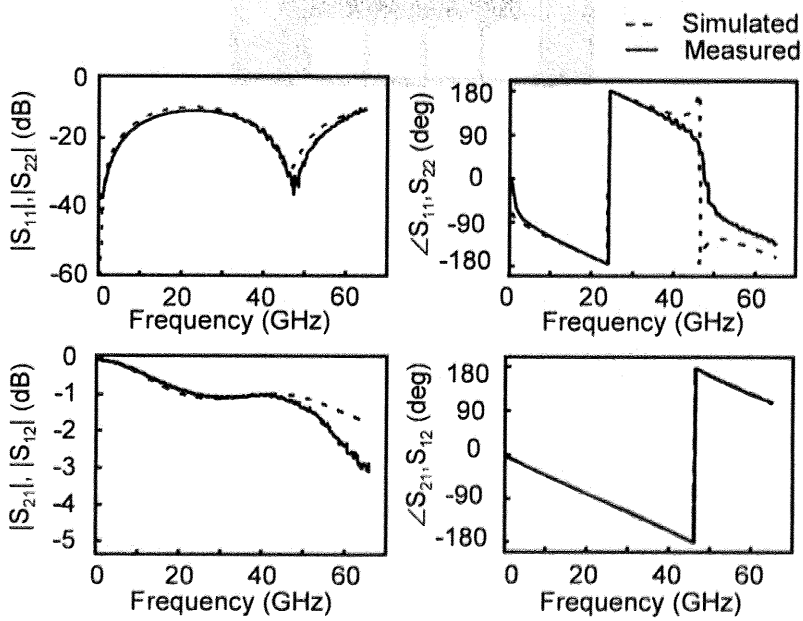

Fig. 7.4 S-parameters of the measured slow-wave transmission line test structures and the extracted distributed model lengths of 900μm and widths 12μm.

7.2 Chip Layout

The down-conversion mixer was designed and fabricated using a six-metal 90-nm CMOS process. Figure 7.5 shows the micrograph of the fabricated chip. The size is 0.61mm by 0.80mm including the D.C. and GSG pads.

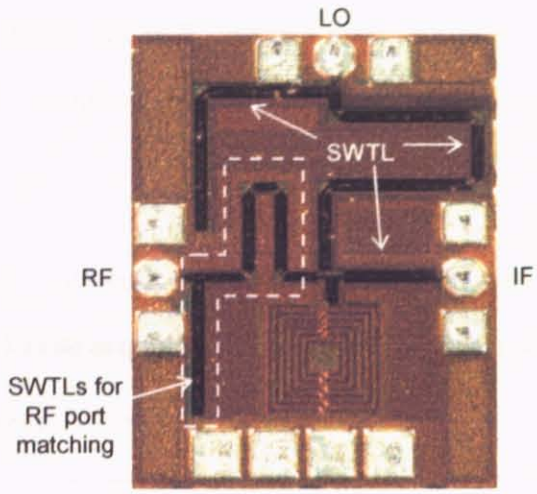

Fig. 7.5 Micrograph of the down-conversion mixer circuit.

To demonstrate the advantage of the length reduction for area conservation, consider the input RF signal port matching. A simple matching network consisting of one series and one parallel open stub is used. The required length of the transmission lines for the design can be represented by $m\lambda$ and $n\lambda$ for the series and the parallel stubs, respectively, where λ represents one wavelength of the propagating RF signal. According to the results of Fig. 7.3 and Eq. (7.1),

$$1.89\lambda_{\mathrm{SWTL}} = \lambda_{\mathrm{MSL}} . \tag{7.2}$$

When SWTL is used, $\lambda = \lambda_{\mathrm{SWTL}}$ (7.3)

When MSL is used, $\lambda = \lambda_{\mathrm{MSL}}$ (7.4)

From design of the fabricated circuit where SWTL is used, the series stub is 564μm and the parallel stub is 245μm. Therefore,

$$m\lambda_{\mathrm{SWTL}} = 564\ \mu\mathrm{m}$$

$$n\lambda_{\mathrm{SWTL}} = 245\ \mu\mathrm{m} .$$

If MSL is used instead,

$$m\left(\frac{\lambda_{\mathrm{MSL}}}{1.89}\right) = 564\ \mu\mathrm{m} \Rightarrow m\lambda_{\mathrm{MSL}} = 1066\ \mu\mathrm{m}$$

$$n\left(\frac{\lambda_{\mathrm{MSL}}}{1.89}\right) = 245\ \mu\mathrm{m} \Rightarrow n\lambda_{\mathrm{MSL}} = 436\ \mu\mathrm{m}$$

The longer required lengths of the MSL will occupy a larger area on the chip. Similarly, the lengths of the LO and IF matching transmission lines are reduced using SWTL.

7.3 Experimental Results

Using the line lengths determined for the matching to RF, LO and IF ports, the circuit was fabricated and measured. On-wafer measurements are performed on the fabricated circuit through a GSG single-ended RF input, a GSG single-ended IF output and the LO supplied through another GSG single-ended input. Scattering parameters are obtained using an Anritsu ME7808 vector network analyzer. In particular, the impedance match of the RF input port to 50Ω is important because minimal power loss of the input RF signal is critical and it is unlike the LO and IF ports which are often not 50Ω terminations for connecting to the phase-locked loop (PLL) output and the IF filtering. Figure 8.6 shows the comparison between the measured and simulated return loss of the RF input port. It has a return loss better than 10 dB for frequencies at 45-64 GHz.

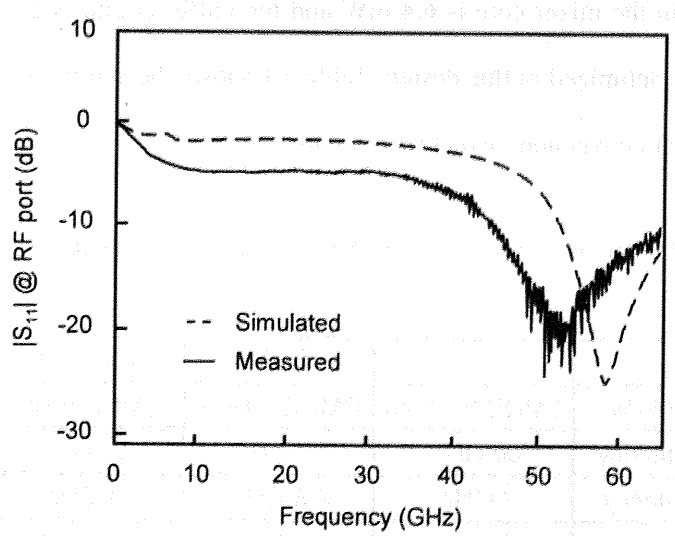

Fig. 7.6 Measured and simulated return loss of the RF input port.

From Fig. 7.6, it can be seen that the model overestimates the matching frequency by less than

10%. Fluctuations in the measured readings at high frequency occur due to imperfect calibration. The return loss at 60 GHz achieved is -13 dB. Figure 7.7 shows the measured output power at RF frequency of 60 GHz and IF of 4 GHz. The down-conversion mixer exhibits a conversion loss of 1.2 dB and achieves an input-referred 1-dB compression point of 0.2 dBm.

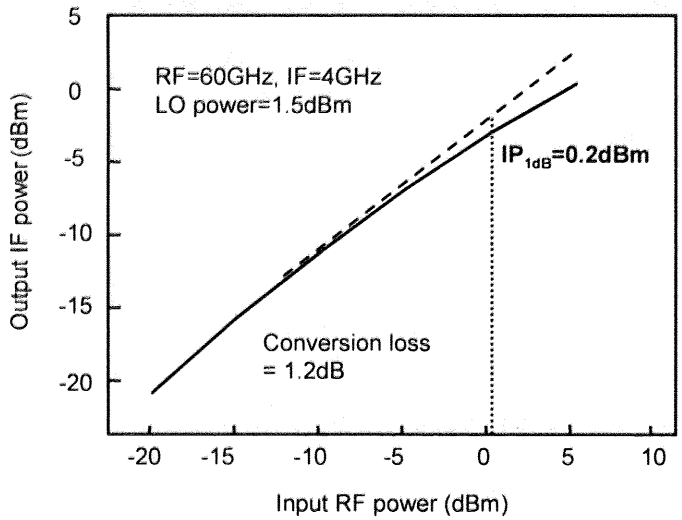

Fig. 7.7 IF output power at 4-GHz plotted against the RF input power at 60-GHz.

The power consumed in the mixer core is 6.4 mW and the buffer circuit is 23.0 mW although the buffer has not been optimized in this design. Table 7.1 shows the summary of performances of 60-GHz CMOS down-conversion mixers reported to date.

Table 7.1 Comparison of Reported CMOS Down-Conversion Mixers.

	[61]	[62]	This work
Technology	CMOS 0.13 μm	CMOS 90 nm	CMOS 90 nm
RF frequency	60 GHz	60 GHz	60 GHz
IF frequency	2 GHz	2-6 GHz	4 GHz
Conversion Gain	-2.0 dB	-11.6 dB	-1.2 dB
1 dB c.p.	-3.5 dBm	6.0 dBm	0.2 dBm
Area	1.6 × 1.7 mm^2	2.0 × 2.0 mm^2	0.61 × 0.8 mm^2

7.4 Chapter Summary

A linear 60-GHz CMOS active mixer implemented with SWTL has been achieved. The mixer employs a cascode topology with IF output boosting and is fabricated on standard digital 90-nm CMOS process. The SWTL allows physical length reductions of 47% when compared to a microstrip line of an equivalent wavelength. The resulting circuit measures only 0.61mm×0.80mm. At a RF of 60 GHz, IF of 4 GHz and LO of 1.5 dBm, the conversion loss is 1.2 dB and an input-referred 1-dB compression point of 0.5 dBm is measured. The return loss at the RF input port is better than 10 dB between 46 GHz and 64 GHz. Performance is comparable to other reported works of CMOS 60-GHz down-conversion mixers while achieving a smaller occupied area.

Chapter 8

50 GHz Variable Gain Amplifier

This chapter presents the high frequency variable gain amplifier using CMOS. CMOS circuits operating at high gigahertz frequency have been reported frequently in recent years [63]. The developments are driven by the availability of the 60 GHz license-free band as well as applications in the high-gigahertz bands below 50 GHz such as the automotive radar system operating at 22-29 GHz. High frequency signal amplification is necessary to realize the front-end transceiver in these applications. However, for CMOS amplifiers to achieve high gain at high frequency with low power consumption, advanced CMOS processes with high f_T is used but requires circuit design techniques to handle the low supply voltage. A VGA is necessary to control the gain so that it is sufficient for the purpose of its application in order to minimize power consumption. In addition to these design considerations, designing at high frequency requires considerations such as accurate active device modeling and passive device optimizations. Available on-chip gain tuning from the variable gain amplifier (VGA) to compensate for modeling non-idealities will be useful.

Figure 8.1 illustrates an applicable architecture involving a control voltage to tune the gain of the VGA and feedback which can be directed by a digital signal processor (DSP) [64], [65], as well as the circuit schematic of the VGA. In this work, a gain-boosting technique is implemented on a single CMOS cascode amplifier stage to realize a VGA.

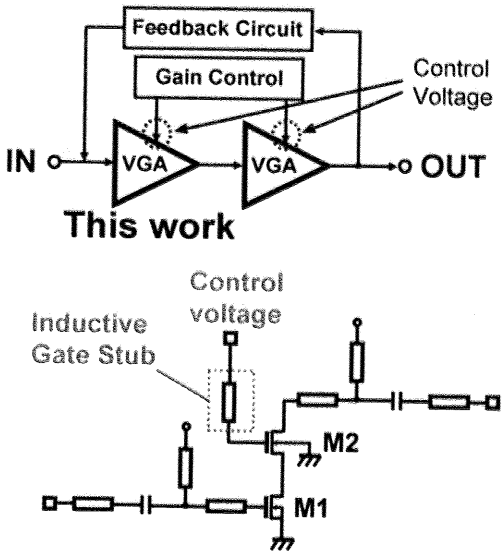

Fig. 8.1 Applicable architecture and circuit schematic of the VGA.

8.1 VGA Design

The VGA is implemented with a cascode topology that includes a common-source stage M1 and the MOSFET M2. The cascode configuration improves stability and reduces the Miller effect. The cascode transistor improves the reverse isolation and minimizes the gate-drain capacitance of M1's effect on the bandwidth. At maximum gain, M1 is biased at saturation of V_{gs}=0.67V where maximum transconductance G_m is achieved for the process employed. It is desired for G_m to be at a high value when maximum gain is desired for a given load impedance. However, using the biasing at M1 for maximum G_m would be accompanied by a large drain current which results in large power dissipation. When a high gain is not required or when low-noise attenuation is desired, M1 does not have to be operating in the saturation region. Therefore, a control of the operating region of M1 between saturation and triode will allow a variable gain. The method employed in the circuit is through the use of a control voltage to provide the gate voltage bias for M2. The important advantage in doing so is to maintain the input and output impedance matching of the circuit.

8.2 Gate-Inductive Gain Boosting Technique

To improve the gain at high frequency, it is proposed to utilize M2 to increase the G_m of the cascode configuration. In a conventional cascode topology, M2 is in a common-gate configuration and M1 determines the G_m. However, in this case, it is made possible by inserting an inductance at the gate of M2 to resonate with its gate-source capacitance C_{gs} as shown in Fig. 8.2.

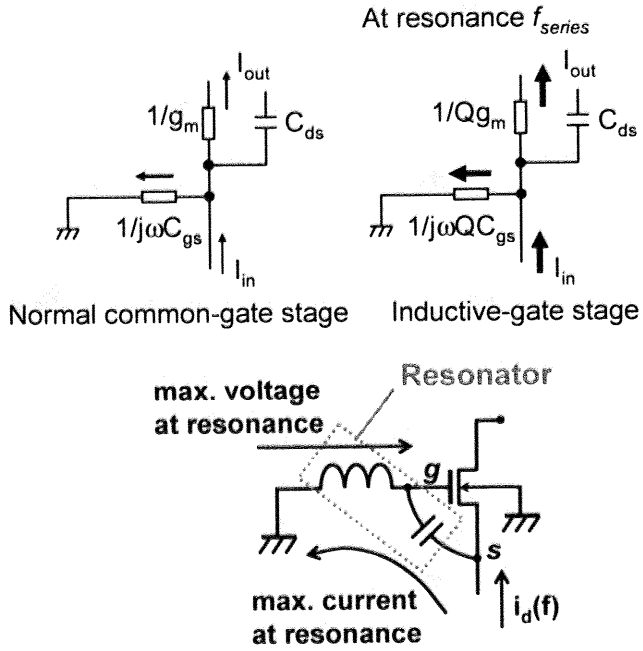

Fig. 8.2 V_{gs} is maximized at the resonant frequency that is determined by values of L_g and C_{gs}.

The inductance forms a series resonator with C_{gs} and presents a low impedance of $1/j\omega QC_{gs}$ at the source of M2 at resonance where Q is the quality factor of the resonator and ω is the angular frequency. Current flows through the inductor and the capacitor C_{gs} which leads to a high potential across the inductor, resulting in a high gate voltage, and thus a high v_{gs} as seen from the peaking of v_{gs} in the simulation results of Fig. 8.3.

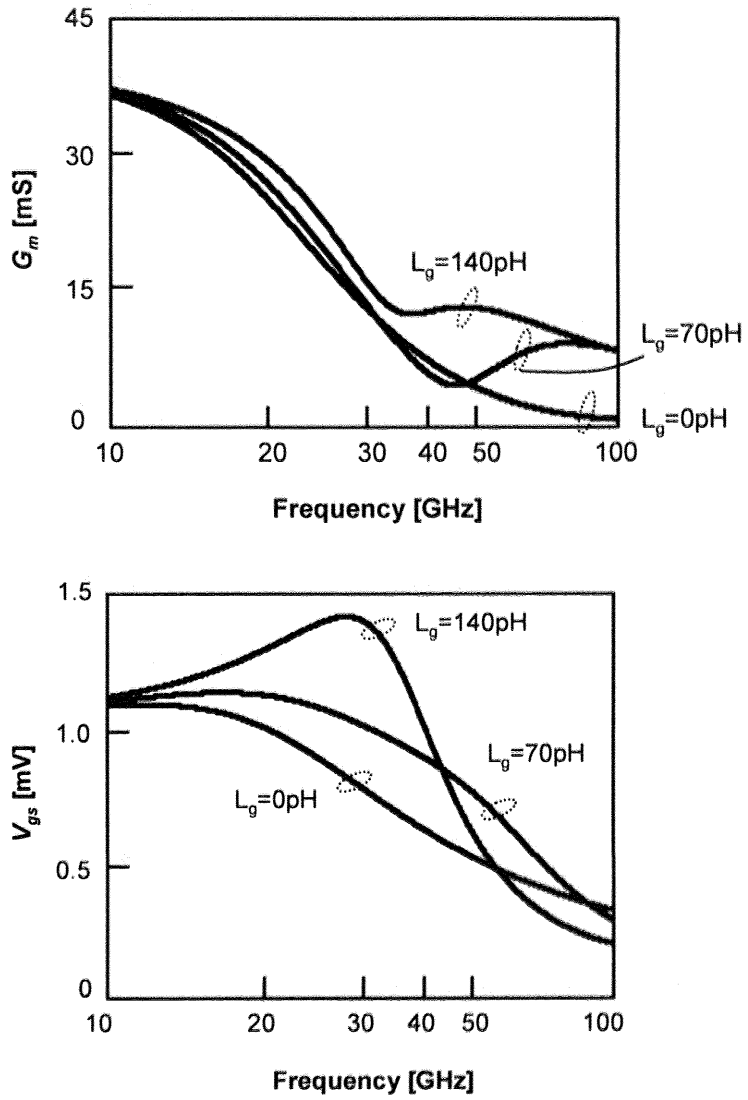

Fig. 8.3 The transconductance G_m peaks due to the increase of V_{gs} caused by the resonator.

Through the transconductance of M2, the output current I_{out} increases as a result of increased v_{gs}. This resonance occurs at a frequency f_{series}. However, the resonance frequencies of of v_{gs} and G_m do not coincide because a parallel tank resonator is also presented to the source node of M2 through the connection of the M2 drain-source capacitor C_{ds} which results in high impedance at resonance of the parallel tank. At this frequency $f_{parallel}$, the potential at the source node increases. Since the series resonator forms part of the parallel resonator, $f_{parallel} > f_{series}$ and has

been verified through simulations by plotting the peaks of the M2 gate node voltage and M2 source node voltage. Nevertheless, an increase of v_{gs} of M2 due to series resonance can be employed to obtain an increase in the transconductance G_m of the cascode stage for gain at high frequency. The gain-boosting technique is feasible for high frequency operation because of the practical impedance values from L_g and C_{gs} obtainable at high frequency. In addition, since high frequency operations require the use of high-f_T advanced CMOS processes, it therefore also facilitates the integration with digital logic circuits, including the gain control logics for the VGA. This gain-boosting technique which is applied to the M2 gate complements the implemented gain-tuning by applying the control voltage at the other end of the inductive stub line. This allows the inductive stub line to be used as the dedicated metal feed to the gate contact of the cascode transistor on the layout to reduce high frequency parasitic into the gate to improve stability. Furthermore, this technique of applying the inductive stub at M2 gate does not dissipate any dc power since dc current does not flow through the MOSFET gate under normal operating conditions.

8.2.1 Analytical Expressions for the Gate-Inductive Cascode G_m

An expression for the transconductance G_m of the cascode amplifier with the gate-inductance is derived as a function of the gate inductor. This relationship enables us to understand how the gain is varied according to the inductance value. Consider the small-signal voltage gain of a typical cascode topology using a model as shown in Fig. 8.4.

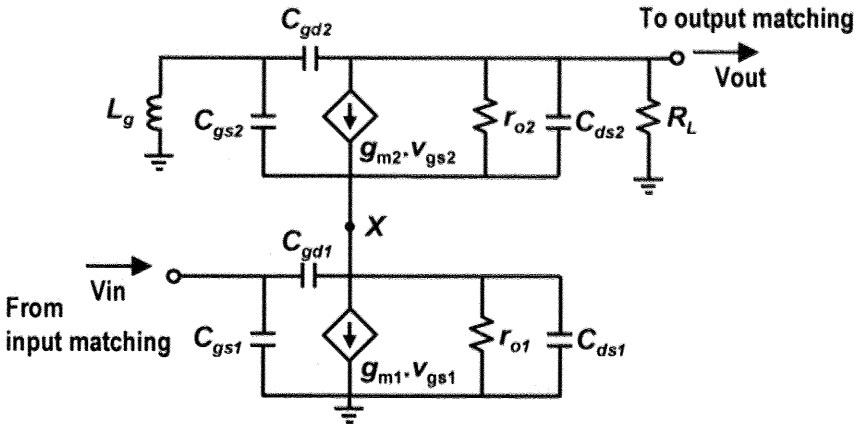

Fig. 8.4 Small-signal model of a cascode amplifier.

Applying Miller's theorem on C_{gd1} and C_{gd2}, new equivalent capacitance values of C'_{gs1}, C'_{ds1}, C'_{gs2} and C'_{ds2} are obtained. This is a result of replacing C_{gd1} with an equivalent combination of C'_{gd1} at the gate-source nodes and C''_{gd1} at the drain-source nodes. Similarly, C_{gd2} is replaced with C'_{gd2} and C''_{gd2} respectively. Relating the voltage-current relationships in the circuit and applying Kirchoff's current law to node X, Eq. (8.1) can be obtained for an infinitely large R_L.

$$A_v = \frac{g_{m1}r_{o2}\cdot H_2(\omega)}{\dfrac{1}{g_{m2}r_{o2}\cdot\dfrac{H_2(\omega)}{G(\omega)}+1}\left[-r_{o2}\left(j\omega C'_{gs2}+g_{m2}\right)\cdot\frac{H_2(\omega)}{G(\omega)}-\left(1+\frac{r_{o2}\cdot H_2(\omega)}{r_{o1}\cdot H_1(\omega)}\right)\right]+1} \tag{8.1}$$

where

$$H_1(\omega)=\frac{1}{1+j\omega C'_{ds1}r_{o1}} \qquad C'_{ds1}=C_{ds1}+C''_{gd1}$$

$$H_2(\omega)=\frac{1}{1+j\omega C'_{ds2}r_{o2}} \qquad C'_{ds2}=C_{ds2}+C''_{gd2}$$

$$G(\omega)=1-\omega^2 L_g C'_{gs2} \qquad C'_{gs2}=C_{gs2}+C'_{gd2}$$

Note that $G(\omega)$ is a function of L_g. This provides the relationship between A_v and L_g. Eq. (8.1)

reduces to a well-known expression for the voltage gain of a cascode topology at low frequency in Eq. (8.2).

$$A_v = -g_{m1}\left(g_{m2} \cdot r_{o1} \cdot r_{o2} + r_{o1}\right) \tag{8.2}$$

Since $G_m = \frac{I_{out}}{V_{in}} = A_v \cdot \frac{1}{R_L}$, The expression for G_m as a function of L_g can be obtained.

$$G_m = \frac{g_{m1} r_{o2} \cdot H_2(\omega)}{\frac{R_L}{g_{m2} r_{o2} \cdot \frac{H_2(\omega)}{G(\omega)} + 1}\left[-r_{o2}\left(j\omega C'_{gs2} + g_{m2}\right) \cdot \frac{H_2(\omega)}{G(\omega)} - \left(1 + \frac{r_{o2} \cdot H_2(\omega)}{r_{o1} \cdot H_1(\omega)}\right)\right] + R_L} \tag{8.3}$$

8.3 SWTL Implementation

As discussed, the gain-boosting technique can be improved by using an inductive gate stub with high quality factor (Q-factor). In order to realize high-Q inductive gate stub as well as other impedance matching lines, the slow-wave transmission line (SWTL) structures are used. SWTL has shown to improve the quality-factor and uses less area as a result of the shorter wavelength of the propagating signal. This structure consists of a signal-carrying conductor at the center and coplanar ground metals at the sides. Slotted ground shields are placed between the signal line and the silicon substrate. In order to perform circuit simulations for the design, a distributed electrical model of the SWTL has been developed and is accurate to within 10% of the measured results. The wavelength reduction allows the SWTL to achieve a physical length reduction factor of 1.89 as have been shown in Fig. 7.3.

8.4 Experimental Results

A chip micrograph of the CMOS VGA with the cascode gate stub is shown in Fig. 8.5 where a 90nm CMOS process with six metal layers is used.

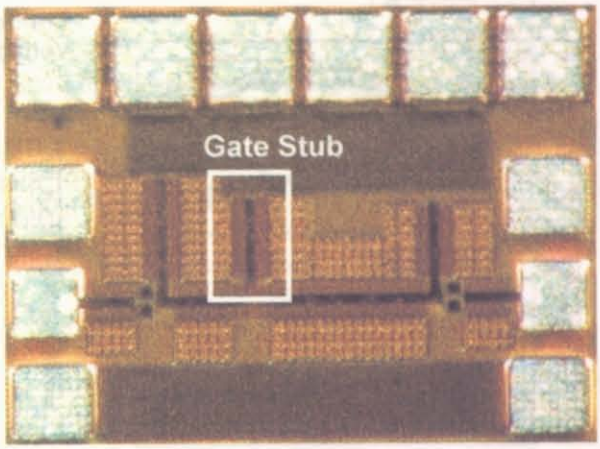

Fig. 8.5 Chip micrograph of VGA.

At the maximum gain control voltage, the return losses at the input and output ports are -10 dB at 50 GHz, as shown in Fig. 8.6. The corresponding S21 has a value of 4.8 dB. The feedback is better than -20 dB across the entire measured frequency band. Figure 8.7 shows the variation of the S21 at different applied gate control voltages. The gain can be varied from -10 dB to 4.8 dB by tuning the control voltage from 0.5V to 1.0V.

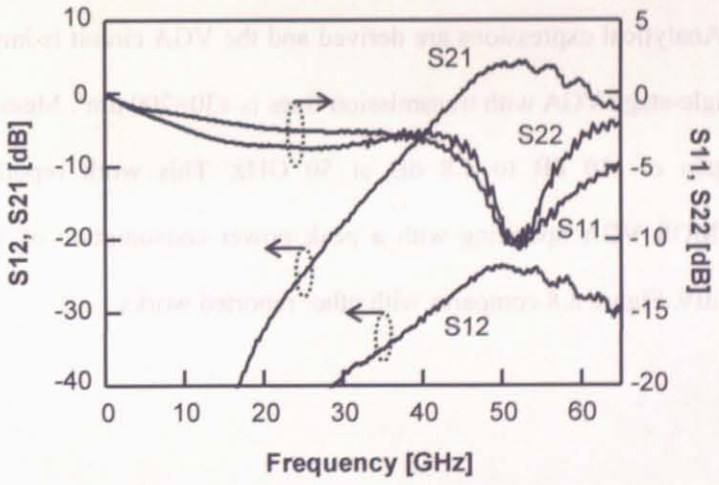

Fig. 8.6 Measured scattering parameters of the VGA at maximum control voltage.

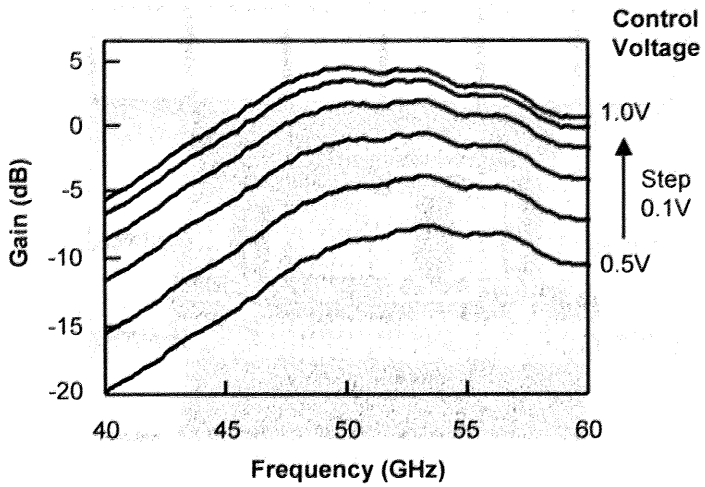

Fig. 8.7 Gain of the VGA at different control voltages.

8.5 Chapter Summary

A new gain boosting technique has been introduced that exploits the resonance of the gate-source capacitance of the MOSFET. The component values of the resonator are suitable for implementation of millimeter-wave frequency amplifier circuit by using 90nm CMOS process that has a high f_T. Analytical expressions are derived and the VGA circuit is implemented. The core size of this single-stage VGA with transmission lines is 430×200 μm^2. Measurement results show a tunable gain of -10 dB to 4.8 dB at 50 GHz. This work reports on the first millimeter-wave CMOS VGA operating with a peak power consumption of 7.6mW using a supply voltage of 1.0V. Figure 8.8 compares with other reported works.

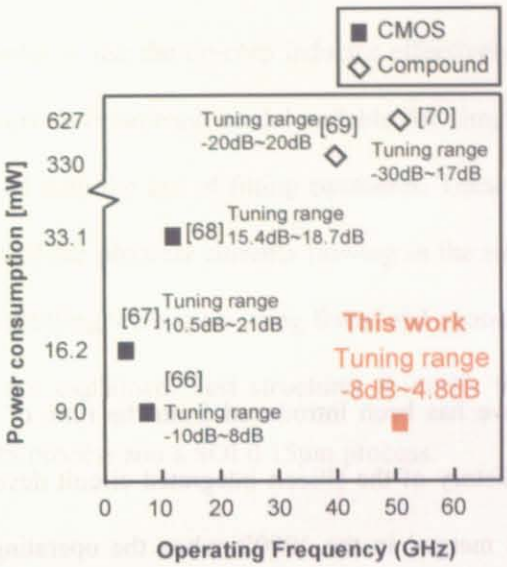

Fig. 8.8 Performance comparison with other tunable amplifiers.

Through the design of the variable gain amplifier, up-conversion and down-conversion mixers as well as passive devices that are explained in the previous chapters, the principal building blocks of the transceiver are presented. These high frequency devices and circuits verify the possibility of realizing millimeter-wave transceiver.

Chapter 9

Conclusion

The history of millimeter-wave has been introduced from the time of Maxwell's predictions with his famous equations. History of the silicon integrated circuit developed separately from the 1960's. These two fields merged in the 1990's when the operating frequency of silicon circuits reached high gigahertz to make possible CMOS millimeter-wave circuits today. This research focuses on the use of CMOS 90nm process technology to implement millimeter-wave circuit building blocks for the wireless transceiver.

The high frequency analog portion of the wireless transceiver consists of the amplifiers, mixers and oscillators, each performing a specific function according to their roles in either the transmitter or receiver. The design of each block is not trivial, considering the frequency and power requirement objectives for CMOS implementation. In addition, the interconnections will severely affect the performance of the devices. Therefore, simply interconnecting working devices are not trivial. In order to accomplish the research work, designs are made with the help of various software, including the high frequency simulation software, Hewlett Packard's Advanced Design System (HP ADS). Chip layout for mask design is made with the Cadence's Layout Editor software together with its verification tools. Measured results are obtained with the carefully-calibrated use of various chip measurement equipments, including a 110-GHz vector network analyzer. Each of the transceiver's building blocks have been explained with some of the most important ones fabricated and measured.

In certain parts of the transceiver that operates at lower gigahertz frequency, the on-chip spiral

inductor is used. In order to use the on-chip inductor effectively, accurate and efficient models are needed. In this work, a broadband model suitable for simulation beyond the self resonant frequency is introduced with the use of fitting equations. These fitting equations are generated through an evaluation of the physical currents flowing in the substrate and at different parts of the inductor. Important fitting techniques using linear and geometric programming on nonlinear monomial equations are explained. Test structures to verify the model have been measured using a 0.35μm CMOS process and a SOI 0.15μm process.

The transmission line is another integral part of the transceiver which has to operate up to very high frequency. New low loss transmission lines up to 110 GHz have been developed. The development of these structures is based on the slow-wave propagation characteristics in the SiO_2-Si interface. However, instead of relying on material properties (substrate resistivity) to obtain slow waves, we used innovative layout designs to achieve it. The design of the slow-wave transmission line (SWTL) and an asymmetric coaxial waveguide (ACW) are described, fabricated and measured. Both structures are able to obtain a high quality factor and length reduction. Measurement results show that, SWTL achieves a higher quality factor, while the ACW is able to achieve a higher length reduction factor.

The idea of the slow-wave phenomenon is extended to the design of an on-chip broadband balun operating from 26.8 GHz to 37.3 GHz. This balun has been tested and characterized for the use in a 20-26 GHz up-conversion mixer. The balun can also be used as a power combiner or a power splitter. Analytical expressions to describe the combiner have been derived to correct errors in existing known equations and are verified by experimental data. Consequently, a 20-26 GHz up-conversion mixer is realized for the automotive radar application that employs two such baluns operating at different frequencies. This demonstration of a fully integrated single-balanced mixer fabricated on CMOS 90nm process has a measured power consumption

of 11.1mW. The results obtained are comparable to mixer circuits fabricated using high performance semiconductor processes.

The down-conversion mixer is the fundamental device in the wireless receiver. A down-conversion mixer is realized for operation in the 60 GHz license-free band. Due to oxygen attenuation at 60 GHz, wireless devices at the frequency are suitable for secure short-range applications. An important concern in realizing such circuit is the chip area consumption as chip area translates to manufacturing and material cost. This circuit employs the SWTL to reduce the chip size area. The mixer employs a cascode topology with IF output boosting and is fabricated on CMOS 90-nm process. The SWTL allows physical length reductions of 47% when compared to a microstrip line of an equivalent wavelength.

To boost the signal to a sufficient level in the transceiver chain, gain amplifiers are used. A 50 GHz variable gain amplifier has been realized using the CMOS 90nm process by employing an innovative gate resonance technique on a popular cascode circuit configuration to improve the gain. Gain at high frequency is difficult to achieve because the operating frequency for amplification should only be a fraction of f_T. This technique is implemented without additional current consumption through a series resonance by using the MOSFET gate-source capacitance with an inductive element at the gate. The inductive element is realized with a transmission line that fits well on the physical layout. The dependence of the cascode transconductance on the gate has been analytically derived and simulated. As a result, this technique can be used to boost gain of the CMOS amplifier at high frequency.

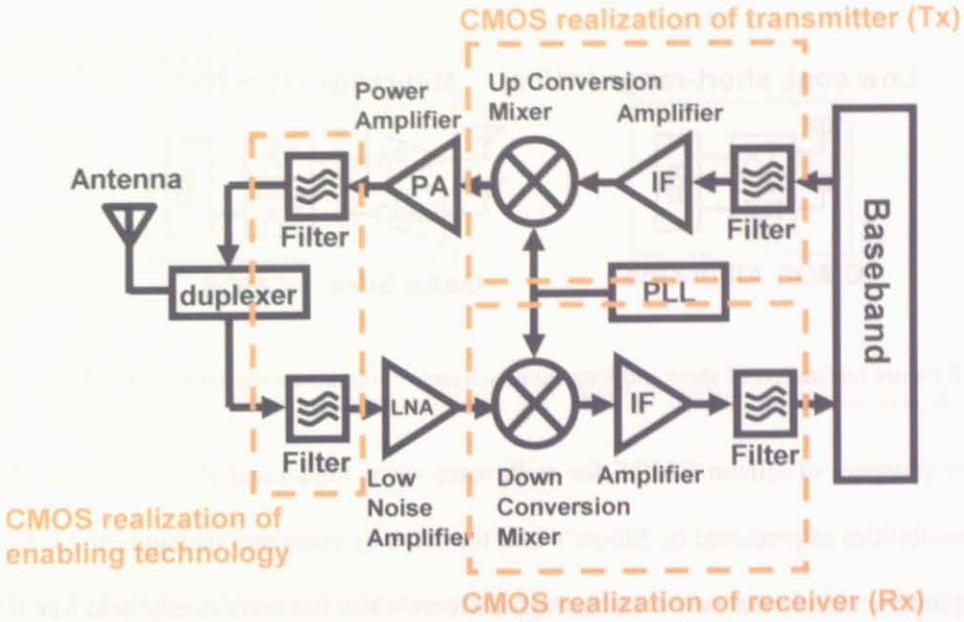

Fig. 9.1 The main building blocks in the RF transceiver design for the millimeter-wave band are realized.

Recall that the receiver or transmitter will almost always be realized as a string of operations where each operation is either one of these three frequency domain operations:

- *a filter*, for the suppression of signals outside the wanted channel;
- *an amplifier*, to adjust the signal level;
- *a mixer*, to change the center frequency.

In this research, the critical building blocks of the millimeter-wave wireless transceiver are accomplished. Future realization of low cost, short range (< 10m) transceivers can be fully integrated using CMOS. Mid-range transceiver (10~20m) requires high power transmission and is therefore suitable to be integrated with compound semiconductors or SiGe amplifiers. Future work is therefore expected to include the integration of the compound semiconductor technology in addition to the continuing developments of CMOS processes and circuits.

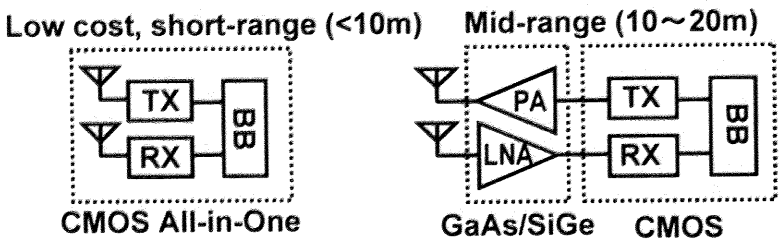

Fig. 9.2 Future realization of short and long range wireless communication building blocks.

The future prospect of silicon CMOS for millimeter-wave fundamentally depends on further scaling possibilities as predicted by Moore's law, the drive by consumer demands and initiatives in developing the circuits for new breakthroughs. Moore's law has consistently held true for the past 30 years and will likely continue to persist for the next decade. Process developments had overcome various obstacles and will continue to do so to sustain the infrastructure of the silicon industry. Demand for bandwidth has pushed applications to operate at a higher frequency. Hence, we can only expect the millimeter-wave frequency band uses to increase. As a start, the 60-GHz license free band is a very attractive option for consumer electronics. This will drive CMOS for millimeter-wave applications. Therefore, it is imperative to continue the development of this technology at the circuit level to meet the needs of the next decade.

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