SFQ Data Processing with Set/Reset Information

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Abstract—We propose a new class of SFQ logic circuits. In this new approach, an SFQ pulse represents the transition between "zero" and "one". By using these two bits of information, a one-to-one correspondence between input and output can be realized. Since the correspondence is then the same as in semiconductor circuits, this method permits logic design without clock elements. In order to carry out this logic, we propose the most fundamental element, a new DC/SFQ converter. A computer simulation and low-speed test were performed. Both results showed that this converter operates correctly with a wide margin. Moreover, this converter also provides the basis for many other logic elements such as AND, OR, and XOR.

I. Introduction

Single flux quantum (SFQ) logic is highly promising for computer systems. Its main features are low power consumption and ultra-high-speed switching. Several types of SFQ logic have been proposed [1]-[3]. In particular, much research has been carried out using RSFQ logic, and excellent results have been demonstrated.

However, an operation in an SFQ circuit is far different from that in a CMOS circuit. A major difference between CMOS and SFQ is that the former uses static data processing with 'voltage-level coding', whereas the latter uses dynamic data processing with 'voltage-pulse coding'. In the former, only the input voltage levels determine the output voltage levels, and no clock is required in CMOS combinational logic. In an SFQ system, in contrast, input voltage pulses determine the next output voltage pulses. Therefore, a conventional SFQ system invariably requires a local clock with every logic element. In this case, it is possible that a circuit may introduce an error due to the delay in a clock signal. In order to prevent this problem, several methods based on dual-rail asynchronous logic have been proposed [4],[5], which eliminate the need for an external clock. However, some internal timing lines, such as a delay line or a feedback line, are still necessary for each logic module. In a CMOS circuit, the module is typically a combinatorial logic circuit with many logic gates. In SFQ circuits, however, the module is typically only a single gate. Therefore, whatever class of system, synchronous or asynchronous, the circuit design for an SFQ system becomes rather complicated. The reason is that data processing in an SFQ circuit is based on pulse coding, and a one-to-one correspondence between input and output cannot be achieved.

Manuscript received September 14, 1998
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From this viewpoint, we had earlier proposed non-latching single flux quantum logic (NSFQ) [6]. NSFQ is based on a threshold device and is very similar to CMOS, except that the former is based on "flux level", and the latter is based on voltage level. Though all basic logic elements, i.e. AND, OR, and NOT, can be realized, it became clear that NSFQ had a problem with signal propagation. However, a one-to-one correspondence between input and output is a very desirable feature.

In this paper, we propose a new data processing concept and design its most fundamental device, in order to eliminate the timing problem, and permit the straightforward construction of combinatorial circuits similar to the case of CMOS. In other words, we propose a method in which output corresponds to input. In order to carry out such a method, set and reset information are used, as explained in the next section. In addition, a new DC/SFQ converter is proposed and simulated in Section III. In Section IV, we show experimental measurements of this circuit.

II. Set and Reset Information

Fig. 1 shows the relation between DC input and SFQ output using a conventional DC/SFQ converter. It is clear that this converter generates an SFQ pulse only when input is set, i.e., when input changes from low to high. This means that the timing of the "reset" is meaningless, and time information of the input signal is lost in the conversion. Therefore, a one-to-one correspondence between input and output is impossible, and a combinational circuit in which the output is determined uniquely only by the state of the input, without any clock elements, cannot be realized. Moreover, a combination of the conventional DC/SFQ converter and a SFQ/DC converter creates a problem, in which a cycle of DC

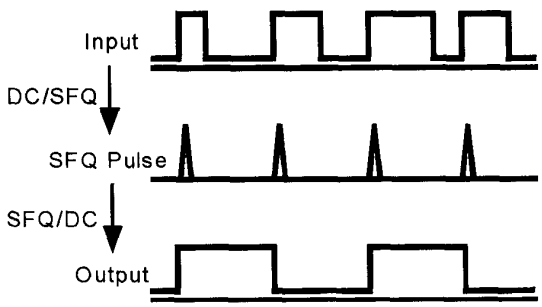

Fig. 1. Relation between input and output when a conventional DC/SFQ converter and a SFQ/DC converter with T flip-flop is used. Output frequency is longer than input frequency. It is because input generates a SFQ pulse only when the signal is set.

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output voltage becomes longer than the DC input current. In order to eliminate these problems and enable SFQ circuits to retain such time information, we propose a new picture for SFQ data processing.

Fig. 2 shows this new picture. Here, an SFQ reset pulse is provided in addition to the set pulse. In this system, the SFQ pulse does not function as a single bit in itself, but rather indicates the transition between "zero" and "one". The time span between two SFQ pulses corresponds to the duration of the "zero" or "one" state. An SFQ pulse that carries zero-to-one information is called the "set SFQ", and that for one-to-zero is called the "reset SFQ". It is clear that one-to-one correspondence between input and output can be achieved. Since data zero and data one are then equivalent, and there is no reason to give zero-to-one conversion special treatment, this method seems to be natural. By using these two SFQ pulses, no special timing element for synchronization in a

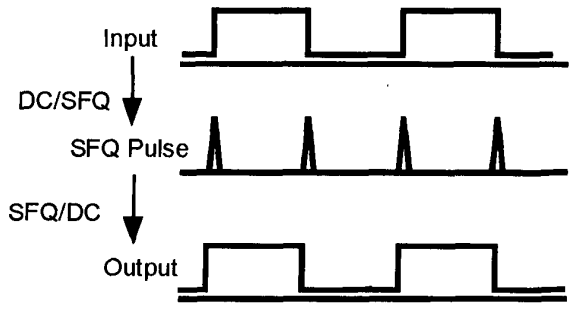


Fig. 2. Relation between input and output when a set pulse and a reset pulse are used. Output frequency is the same as input and output corresponds with input. This operation is perfectly the same as semiconductor circuit. It also means that logic device like AND, OR can be realized without clock elements.

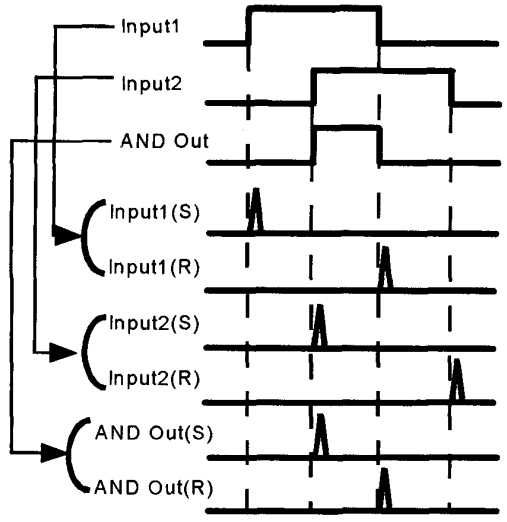


Fig. 3. Input/output representation of SFQ pulses using set/reset information. This is an example of AND. Other logic devices are also represented by the same way. Inverter can be realized by exchanging set and reset pulses.

combinational logic circuit is necessary, and the circuit structure becomes simpler. In this way, a semiconducting circuit can be more easily translated into an SFQ circuit.

One example of the input/output relations for a logic element based on this principle is shown in Fig. 3. The input/output relation of other logic elements can be represented in the same way. As can be easily seen, an inverter can be obtained by exchanging a set SFQ and a reset SFQ. By using a confluence buffer and a T-flip-flop, these two pulses can be transmitted on the same transmission line. Therefore, this is not a simple dual-rail system. The only requirement is that a set pulse and a reset pulse must be present in alternation.

III. Proposal of New DC/SFQ Converter

In order to realize this set/reset system, a conventional DC/SFQ converter is not sufficient. A new DC/SFQ converter that generates both a set SFQ and a reset SFQ is necessary. We propose a circuit shown in Fig. 4 as such a converter, with operation as follows.

Initially, there is no SFQ stored in any SQUID loop. Bias current flows through J1 and J2 to ground. If input current is added, a part of the current flows to ground through inductance L1, and the rest flows up through J1. If L3 is large enough, the current flows to ground through L2 and J2. Because of added bias and input, J2 switches earlier than J1. Two SFQ pulses of opposite signs are generated on each side of J2. The SFQ on the left crosses J4 and is sent out as the "set SFQ". In contrast, the SFQ on the right cannot cross J1 because input current is flowing up, and opposes the current bias of J1. Therefore, this SFQ is trapped in the SQUID loop defined by J1, J2, and L2. However, if the input is removed in this state, the trapped SFQ can cross J1, and then can cross J3, and is sent out as the "reset SFQ".

A computer simulation of this new DC/SFQ converter is shown in Fig. 5, where the solid line is the "set output" and the dotted line is the "reset output". The expected results are obtained, namely that the set and reset SFQ pulses are generated when the input current changes. In this simulation,

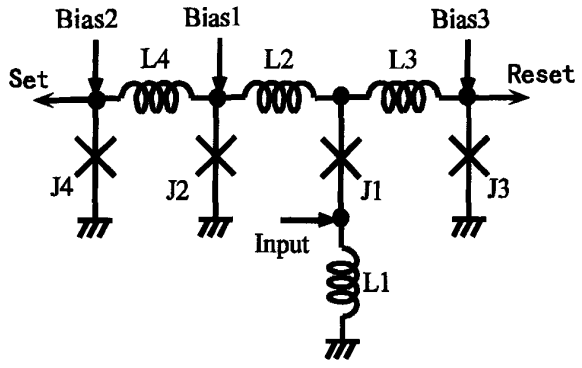


Fig. 4. Schematic of a new DC/SFQ converter. If input is added, J2 breaks first and a SFQ of left side is outputted as a set SFQ. A SFQ of right side can not break J1 because input works as opposite bias of J1. The SFQ breaks J1 when input is removed and it is outputted as a reset SFQ.

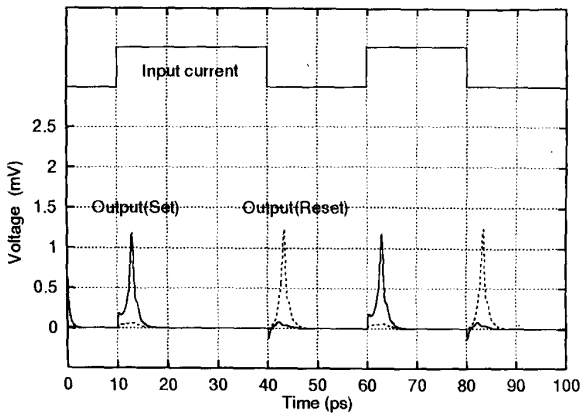
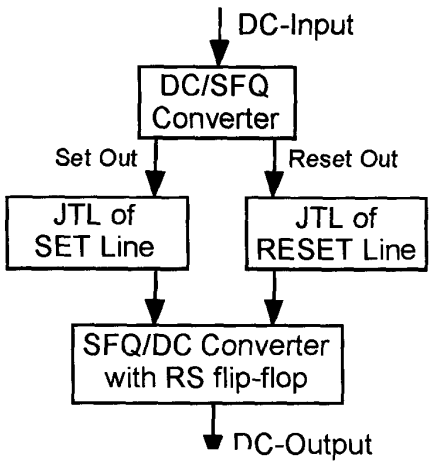
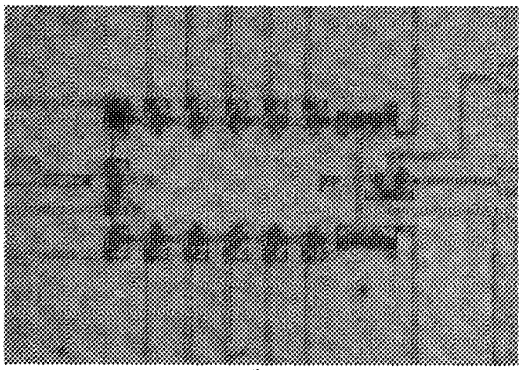


Fig. 5. Simulation of a new DC/SFQ converter. In this simulation, JTL of ten gates are connected to both output terminals. The value of each parameter: Ic1=Ic3=Ic4=0.2 mA, Ic2=0.14 mA, L1=1.5 pH, L2=1.1 pH, L3=8 pH, L4=5 pH, Bias1=0.18 mA, Bias2=0.16 mA, Bias3=0.11 mA. The narrowest margin of bias current is 36% of Bias3.



(a)



(b)

Fig. 6. (a) Block diagram of a test circuit. The test circuit is composed of three parts, i.e. a DC/SFQ converter, two JTL lines of set and reset, and a SFQ/DC converter with RS flip-flop. (b) Photograph of a test circuit. Left side of this circuit is a DC/SFQ converter and right side is a SFQ/DC converter with RS flip-flop. An upper 5-gate JTL is a reset line and a lower 5-gate JTL is a set line.

in order to simulate a real circuit, a ten-stage Josephson transmission line (JTL) is connected to each of the output terminals. Values used in this simulation are given in the caption to Fig. 5. Although we have not yet optimized the parameters, the margins of bias current are +/-36%, which is sufficient for this converter to be used in a real circuit.

IV. Measurement of New Converter

We designed, fabricated, and measured the new converter. The test circuit is composed of the new DC/SFQ converter and two JTLs, together with the standard SFQ/DC converter with the RS/flip-flop of [1]. Fig. 6(b) is a photograph of this circuit, fabricated by NEC Corporation. Device parameters are the same as those given in Fig. 5. The critical current of the JTL is 0.2 mA.

The measured result is shown in Fig. 7. Despite some high-frequency noise, this clearly operates correctly and shows the characteristics of a threshold device. In other words, the one-to-one correspondence between input and output has been achieved, just as for a semiconductor circuit. Adjusting the proper threshold value permits this to function as a logic element such as AND or OR. The DC bias margin of Bias3 is +/- 70%, which is much higher than the simulation. We think that this may be because the measurement is performed in a low-speed mode (on the kHz scale), whereas the time axis of the simulation (Fig. 5) is the order of picoseconds, corresponding to operation at tens of GHz.

A result that is more interesting, shown in Fig. 8, is obtained by increasing the input. When the input exceeds a second threshold, the DC output disappears, indicating that a reset pulse has been generated. This can be understood as follows. If input current increases, the current through L3 and J3 also increases. When this exceeds the critical current of J3, the SFQ crosses J3 and a reset pulse is generated.

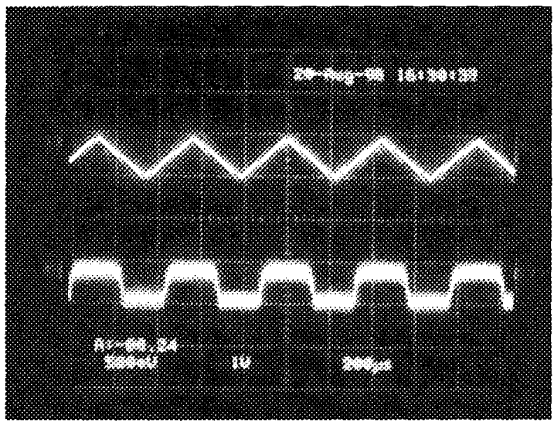


Fig. 7. Measurement of test circuit. When input current exceeds a threshold value, a set pulse is generated and DC output voltage appears. Oppositely, input falls below the threshold, a reset pulse is generated and DC output disappears. This operation is perfectly the same as semiconductor and one-to-one correspondence between input and output is achieved. By using this characteristic and adjusting proper threshold, fundamental logic devices like AND, OR are realized. Input : 0.2 mA/div, Output : 50 μV/div, Time : 200 μs/div.

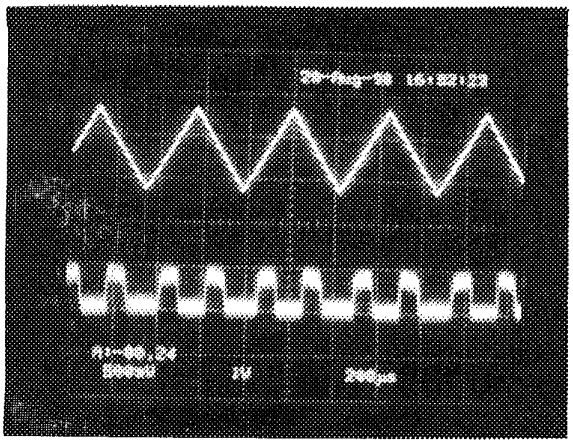


Fig. 8. Measurement when input increases. When input exceeds "second threshold", a reset pulse is generated and DC output voltage disappears. When input falls below the second threshold, J1 is broken and two SFQ of both sides of J1 recouple and vanish. After that, J1 is broken again and set pulse is outputted. By using this characteristic and adjusting a proper threshold, this circuit has a possibility to realize XOR. Input : 0.2 mA/div, Output : 50 μV/div, Time : 200 μs/div.

However, J1 is not crossed because the large input acts as an opposite bias for J1. When the input is then decreased, the critical current of J1 is exceeded, and the two SFQs on both sides of J1 recombine and vanish. After recombination, a set pulse is generated and the output DC voltage appears again. This result indicates that a functional logic gate such as XOR can be easily realized by proper adjustment of parameters.

V. Conclusion

We propose a new data processing picture for SFQ circuits. In this picture, an SFQ pulse represents the transition between "zero" and "one". By using set and reset SFQ pulses,a one-to-one correspondence between input and output can be realized, and a circuit structure similar to that in semiconductors can be obtained. Therefore, one can easily create combinational logic circuits in which the output is generated from the input without any clock elements. In order to demonstrate this method, a new DC/SFQ converter that produces both a set SFQ and a reset SFQ was proposed. This circuit was simulated, fabricated, and measured at low frequencies. These results showed correct operations with wide parameter margins. This circuit functions as a perfect threshold device, and shows the possibility of many useful logic elements, including AND, OR, and XOR, by proper adjustment of parameters.

Acknowledgement

The authors would like to thank Dr. Shuichi Tahara of NEC Corporation and his research group for circuit fabrication. One of the authors (H.K) would like to thank Dr. Yoshihisa Soutome of Hitachi Limited for useful discussion and encouragement.

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