Abstract

As the size of very large scaling integration (VLSI) scales down into deep sub-micron regime, conventional device scaling concept loses its effect and new physics turn to dominate device performance. Although we have achieved performance enhancement during the device scaling down, it is obvious that there is a limit at the end of scaling down and we can not just diminish the device size forever. Accordingly, in ITRS, three different but related concepts are proposed: “More Moore”, “More than Moore”, and “Beyond CMOS”. Until now, we still have no concrete image that what will happened in “Beyond CMOS”, but it is clear that we need to achieve further performance enhancements in Si-based devices before we enter into “Beyond CMOS” era.

Nanowire is a one-dimensional structure that owns two-dimensional quantum confinements that plays an important role in “More Moore”. As a promising candidate in future VLSI technology, nanowire has attracted more and more attention in recent years. Carrier mobility is an important factor that dominates the device transport performance, such as the drive current and operation speed. To understand more details about nanowire transport characteristics and figure out effective methods to obtain performance enhancement, it is necessary to investigate carrier mobility properties in nanowires experimentally. However, for accurate mobility in nanowires, the main difficulty originates from the ultra-small capacitance of one single nanowire, as well as serious parasitic effects within the transport channel. In other words, the intrinsic capacitance of one single nanowire is too difficult to be measured directly. Accordingly, channel that contains multiple nanowires is necessary. Then, how to fabricate multiple uniform nanowires and remove parasitic effects are challenging problems to be solved.

The basic objective of this work is to dig out the potential of Si-based nanowire MOSFETs and get further performance gain. To be particular, first of all, a special device design should be proposed to measure nanowire capacitance; then, one key problem we need to solve is to remove parasitic resistance and capacitance for intrinsic mobility measurements in nanowires; finally, based on the experimental data we have obtained, systematic investigations on mobility characteristics in nanowires will be performed, furthermore, strain effects on carrier mobility or device performance enhancements will be studied.

In this paper, on the basis of split C-V method together with double L_m method, experimental and theoretical investigations on carrier mobility characteristics in silicon nanowires are described systematically. It is found that the orientation of side surface plays the key role that determinates the mobility modulation in narrower nanowires, as well as the surface roughness. To be particular, [100]/(100) is the optimum channel direction for nanowires nMOSFETs while [110]/(110) is the optimum channel direction for nanowires pMOSFETs. In wide nanowires, electron mobility approaches to universal curve in [100]/(100) nanowires while hole mobility approaches to the

universal curve in [100]/(110) nanowires due to four identical surrounded surfaces with same orientations. For the same reason (side surface contribution), large mobility degradation is observed in narrower [110]/(100) nanowires nMOSFETs because the contribution from (110) side surface with low electron mobility will increase, whereas mobility enhancement is observed in narrower [110]/(110) nanowires nMOSFETs because the contribution from (100) side surface with high electron mobility will increase. As to [110]/(110) nanowires pMOSFETs, although larger contribution from (100) side surface with low hole mobility exist in narrower nanowires, surprisingly, high hole mobility still can be obtained in high N_{inv}, showing only a little degradation from wide nanowires. This is very impressive since the high N_{inv} region is very important for VLSI applications.

Furthermore, aiming at mobility enhancements, mobility modulations by uniaxial stress is studied in both nanowire nMOSFETs and nanowire pMOSFETs. In nanowire nMOSFETs, electron mobility enhancement is observed in (110) nanowires and [100]/(100) nanowires by longitude tensile stress. In nanowire pMOSFETs, hole mobility increases by [100] tensile stress while decreases by [110] tensile stress. Since (100) surface has much high sensitivity to [110]-directed stress, if [110] compressive stress is applied, it is believed that large mobility enhancement can be obtained in [110]/(110) nanowires due to the large contribution from (100) side surface.

The results obtained in this thesis give us basic and important information on carrier transport characteristics, shedding light on the structural optimization of silicon nanowire-based devices in future applications in “More Moore”

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Contents

Chapter1 Introduction

1.1 Background

As the size of very large scaling integration (VLSI) scales down into deep sub-micron regime, conventional device scaling concepts lose their effects and new physics turn to dominate device performance. Although we have achieved performance enhancement during the device scaling down, it is clear that there has a limit at the end of scaling and we can not diminish the device size forever. Accordingly, in ITRS [1], three different but related concepts are proposed: “More Moore”, “More than Moore”, and “Beyond CMOS”. Until now, we still have no concrete images that what will happened in “Beyond CMOS”, and we need to achieve further performance gain in Si-based devices before we enter into “Beyond CMOS” era in recent future. To suppress short channel effect (SCE), which is serious in traditional planar MOSFETs as scaling down, devices with multiple gates have been developed, such as MOSFETs with a double-gate (DG) structure [2]-[3], FinFETs with a DG or tri-gate (TG) structure [4]-[6], and nanowire FETs with a gate-all-around (GAA) structure [7]-[9].

“Nanowire” is a special one-dimension transport structure that owns two-dimensional quantum confinements and it plays an important role in “More Moore”. As a promising candidate for future VLSI technology, nanowire has attracted more and more attention in recent years. Carrier mobility is the underlying mechanism that determinates the device transport performance, such as the drive current and operation speed. Carrier mobility has been studied widely in planar bulk MOSFETs [10]-[11] and ultrathin-body (UTB) MOSFETs [12]-[14]. Recently, mobility behaviors in FinFETs with a TG structure have been studied experimentally, including strain effect [15]-[16]. For silicon nanowire MOSFETs, some theory work points out carrier mobility degradation is large [17], while one other simulation results show that mobility in cylindrical silicon nanowire will improve when the diameter is around 5nm [18] just like silicon UTB MOSFETs [19]. It has also been reported that ultra-high carrier mobility by phonon engineering can be achieved if we coat nanowire with diamond insulation layer instead of traditional SiO2 material [20]

To understand nanowires transport characteristics and figure out effective methods to get further performance enhancement, it is necessary to achieve experimental data of intrinsic mobility in nanowires. Although there are some experimental works on mobility in silicon nanowires [21]-[22], detailed analysis of nanowire width

dependence has not been reported. Aiming at accurate mobility in nanowires, one difficulty originates from the ultra-small capacitance between the gate and the channel of single nanowire; the other difficulty is the serious parasitic effect. In other words, the intrinsic capacitance of single nanowire is too difficult to be measured directly. Overestimation of parasitic resistance or capacitance results in large underestimation of carrier mobility. Accordingly, channel containing multiple nanowires is necessary. However, the structure of multiple nanowires introduces to another problem, that is, how to fabricate multiple uniform nanowires.

1.2 Objectives

The basic objective of this work is to dig out the potential of Si-based nanowire MOSFETs and get further performance enhancements in Si-based devices. To be in detail, first of all, aiming at intrinsic carrier mobility measurements in nanowires, we need to propose a special device design and measurement method; then, based on measured mobility characteristics in nanowires of various surface orientations and channel directions, nanowire structure optimization will be discussed; finally, uniaxial stress effects on mobility modulation will be studied.

1.3 Chapter Organizations

This paper is mainly organized into 6 chapters. In chapter 2, proposed structure design of nanowire MOSFETs is introduced and relative fabrication process is described. Then, the measurement method is introduced, using the advanced split C-V method together with double L_m method. In chapter 3, electron mobility in nanowires of [100]- and [110]-directions on both (100) and (110) SOI substrate are studied. For further information, low temperature measurements are also performed to understand the underlying physical mechanisms that dominate mobility behaviors in nanowires. Then, in chapter 4, hole mobility in nanowire pMOSFETs of various surface orientation and channel directions are described. Next, in chapter 5, mobility modulations in nanowires are investigated by applying mechanical uniaxial tensile strain. Finally, in chapter 6, our work is summarized and the future work is discussed.

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Chapter 2
Fabrication and Characterizations of Multiple Silicon Nanowire MOSFETs

2.1 Introduction

In recent decades, nanowire fabrication and characterization have attracted more and more attention. As to the fabrication, the widely used method in traditional CMOS process is called “top-down approach”, in which thermal oxidation, dry etching and wet etching are combined to form nanoscale nanowires. By thermal oxidation, long time oxidation is used to achieve ultra-narrow nanowires since stress induced by the thermal oxidation will stop the further oxidation in nanoscale structure [1-2]; by dry etching, it can transfer nanowire pattern to Si (or SOI, Si on Insulator) easily but the width of nanowires is relatively large and determined by EB resist or photo resist; as to the wet etching, including SC1 isotropic wet etching [3-4] and TMAH anisotropic etching [5-6], nanowire width can be controlled well. Therefore, in normal case, after transfer the nanowire pattern to Si layer, wet etching will be used to control the nanowire width, and then thermal oxidation is performed for gate insulation layer together with further reducing nanowire width, especially for nanowire of ultra-small diameter.

The operation of nanowire MOSFETs is similar to that of planar MOSFETs and ultra-thin-body (UTB) MOSFETs. However, due to its two-dimensional confinement structure, transport characteristics in nanowire MOSFETs are different from those in planar and UTB MOSFETs. In ultra-small nanowire, the shape of which is always cylindrical, surface orientation concept loses its meanings; while in wide and high rectangular nanowires, in which quantum confinement effects are ignorable, device transport characteristics have direct dependence on the surface orientation (top/bottom surface and side surfaces). Consequently, it is expected that some device characteristics, especially carrier mobility, will show width dependence.

In this chapter, aiming at carrier mobility measurements with high accuracy, device design and fabrication process of multiple silicon nanowire MOSFETs on SOI substrate are described in detail. Then, based on fabricated (100) n-type nanowire nMOSFETs, the mobility extraction method is introduced. It is observed that electron mobility in [100]-directed nanowire agrees with the universal curve of (100)-oriented planar nMOSFETs.

2.2 Design and Fabrication of Multiple Silicon Nanowire MOSFETs

2.2.1 Device Design

In this work, overlap structure is applied in this work and parasitic effects will be removed by comparing nanowires of different length, as shown in Figure 2.1. As declaimed in former parts, the main difficulty for mobility measurement in nanowire is that nanowire capacitance is too small to be measured. With a simple method, dividing oxidation insulator into ultra-small parts (T_{ox1}, T_{ox2}, …), taking each part acts as an parallel plate capacitor. The calculation results of nanowire capacitance of various shapes are illustrated in Figure 2.2, where the analytical data is given by equation $2*pi*\varepsilon_{ox}/\ln(R_2/R_1)$ for nanowires of cylindrical shape. Based on these results, it is found that at least 1000 NWs should be fabricated to make nanowire capacitance larger than 1 pF, supposing 5um length channel and T_{ox}=20 nm.

For optimized conditions of EB process, multiple nanowire structures with various pitch setting values are designed. The relationship between exposed nanowire width and designed nanowire width is illustrated in Figure 2.3. Type A: the pitch value is fixed to be 130 nm for NW width from 35nm ~ 70 nm while 150 nm for width from 75 nm~110 nm; Type B: the total width of pitch and NW equals 200 nm for NW width from 35nm~70nm while 250nm for width from 75nm to 110nm; Type C: pitch value is three times of NW width. Then, EB experiments of different drawing directions (parallel nanowires or vertical nanowires) were performed. Two points can be summarized: Firstly, the nanowires of different directions show almost same width after development and etching, Figure 2.4; Secondly, NWs widths only increase a little as changing EB dose from 630 $\mu C/cm^2$ to 780 $\mu C/cm^2$ for wide range of designed width.

However, due to so-called EB inter-proxy effect [7-8], on the one hand, nanowire width turns to be wider at the connect part between nanowire and mesa pattern, as shown in Figure 2.5; on the other hand, nanowire width depends on the nanowire length (longer→wider).

2.2.2 Fabrication Process

Figure 2.6 shows the fabrication process of silicon GAA multiple nanowire MOSFETs. The starting materials were (100) and (110) SOI wafers. The SOI layer was thinned down to the required thickness by repeated thermal oxidation and buffered HF (BHF) etching. Thermal oxidation was performed once again to form a SiO_2 mask, and then the mesa area (source/drain) was defined by laser exposure, followed by buffered HF (BHF) wet etching (Figure 2.6 (a)). EB lithography was performed to define multiple nanowires, and the pitch within parallel nanowires was 500 nm. To solve foresaid EB proximity problems, laser exposure and EB lithography are combined. First of all, thermal oxidation is done to form SiO_2 mask, followed by laser exposure and BHF wet etching. After the mesa fabrication, EB lithography is performed to draw narrow nanowires across the trench. With the protection of SiO_2 mask and EB resist, only the central part of developed nanowires is taken as the actual

transport channel after dry etching. So, EB proximity can be well removed, and the trench defines the nanowire channel length (Figure 2.6 (b)). In this work, nanowire pitch is 500nm, and the nanowire channel length was defined by the mesa trenches of 1~4 μm. After dry etching, with the protection of the SiO_2 mask and EB resist (HSQ), the source/drain and channels were fabricated simultaneously (Figure 2.6 (c)). Then, SC1 isotropic wet etching was performed to narrow nanowires until the required width was reached, and the GAA structure was achieved after BHF wet etching (Figure 2.6 (d)). Schematics of the top-view and three-dimensional structures are shown in Figs. 2(e) and 2(f), respectively. After removing the SiO_2 mask and EB resist by BHF wet etching, gate thermal oxidation and poly-silicon deposition were performed sequentially(Figure 2.6 (g)), and the following processes were similar to the normal CMOS process. A SEM image of multiple Si nanowires is shown in Figure 2.6 (h), where the inset shows an enlarged SEM image of one single nanowire.

2.3 Mobility Measurements in Multiple Silicon Nanowire MOSFETs

Figure 2.7(a) shows I_d-V_g characteristics of [100]/(100) nanowire MOSFETs with 1000 parallel nanowires (T_{soi}=22nm and L_g=3μm). I_d decreases as the nanowires turn to be narrower. Figure 2.7(b) shows C_{gc}-V_g characteristics of devices with L_g=3μm and 4μm, where W_{nw} is 7nm~48nm. Thanks to GAA structure and surface roughness control, sub-threshold properties show ideal performance in measured nanowire MOSFETs. Figure 2.8 shows I_d and C_{gc} of 48nm nanowires at V_g=3 V, changing the number of parallel nanowires and gate length (L_g=3μm, 4μm). Linear relationships along with nanowire number are observed clearly, which confirms that multiple nanowires work well.

Mobility measurements are usually performed by the widely used the split C-V method [9], measuring drain current and gate capacitance with respect to the gate voltage simultaneously. So, we can make it clear that how many carriers attributes to the current at a certain gate voltage and bias. The basic equation is expressed as

$$\mu = \frac{L_{eff}}{W_{eff} V_d} \cdot \frac{I_d(V_g)}{Q_i(V_g)} = \frac{L_{eff}^2}{V_d} \cdot \frac{I_d(V_g)}{\int_{-\infty}^{V_g} C_{gc}(V_g) dV_g} \tag{1}$$

where L_{eff}/W_{eff} is the effective channel length/width, V_d is the applied drain bias, and $I_d(V_g)$ and $C_{gc}(V_g)$ are the measured drain current and gate-channel capacitance at a certain gate voltage V_g, respectively.

To remove the effects of parasitic capacitance and resistance (R_p) in nanowire MOSFETs, mobility estimations are performed by the split C-V method together with the double L_{eff} method [9-11], that is, devices containing nanowires of different lengths are compared to remove parasitic effects. In our device structure (L_g>L_{nw}), three kinds of capacitance are included in the measured capacitance: constant parasitic capacitance C_{con} from the Al

pattern, parasitic MOSFET capacitance C_{MOS} from the overlap region between the gate and the source/drain, and intrinsic nanowire capacitance C_{nw}. Supposing identical parasitic capacitance (C_{con} +C_{MOS}) and resistance (R_p) in the two compared devices with different L_{nw} values, $V_d/I_{d,1(2)}=R_p+R_{nw}\times L_{nw,1(2)}$, $C_{gc,1(2)}=C_{nw}\times L_{nw,1(2)}+C_{MOS}+C_{con}$. Here, $L_{nw,\,1(2)}$, $I_{d,1(2)}$ and $C_{gc,1(2)}$ are the designed L_{nw}, I_d and C_{gc} in the two devices, respectively. The intrinsic characteristics of nanowires with L_{nw} can be derived. Parameters in eq. (1) can be replaced with the following definitions:

$$\begin{aligned} L_{eff} &= L_{nw,1} - L_{nw,2}\,, \\ I_d(V_g) &= (I_{d,1}^{-1} - I_{d,2}^{-1})^{-1}\,, \\ C_{gc}(V_g) &= C_{gc,1}(V_g) - C_{gc,2}(V_g)\,. \end{aligned} \tag{2}$$

The average surface carrier density is defined as

$$N_{inv} = \frac{\int_{-\infty}^{V_g}[C_{gc,1}(V_g) - C_{gc,2}(V_g)]dV_g}{2(L_{nw,1} - L_{nw,2})(W_{nw} + T_{SOI})} \tag{3}$$

where T_{soi} denotes the SOI thickness (nanowire height). In bulk MOSFETs, UTB MOSFETs, FinFETs with double gates, and even [100]/(100) nanowires with a rectangular cross section, N_{inv} in eq. (3) denotes the average carrier density of a certain orientation surface.

On the basis of eqs. (2) - (3), the mobilities in [100]/(100) 48 nm wide nanowire nMOSFET have been measured. Figure 2.9 shows the electron mobility in nanowire nMOSFET together with the (100) bulk universal curve [15]. With normal split C-V method, the gate capacitance C_{gc} is overestimated because of the parasitic C_{MOS} and the channel current is underestimated because of the parasitic resistance. By the double L_{eff} method, the estimated mobility is much improved and the intrinsic mobility in a nanowire is achieved. It is observed that the electron mobility in 48 nm wide [100]/(100) nanowires approaches the (100) bulk universal curve after correction.

2.4 Summary

Proposal and fabrication process of multiple gate-all-around nanowire MOSFETs have been described in this chapter. Aiming at accurate mobility measurement, double Lm method is introduced and combined with split C-V method, by comparing two identical nanowire MOSFETs of different nanowire length. Simultaneously, double exposure method with EB and laser lithography is introduced for uniform nanowires and reliable comparisons. Based on this device design and measurement method, electron mobility in [100]/(100) nanowire nMOSFETs is extracted and shows good agreement with bulk universal curve.

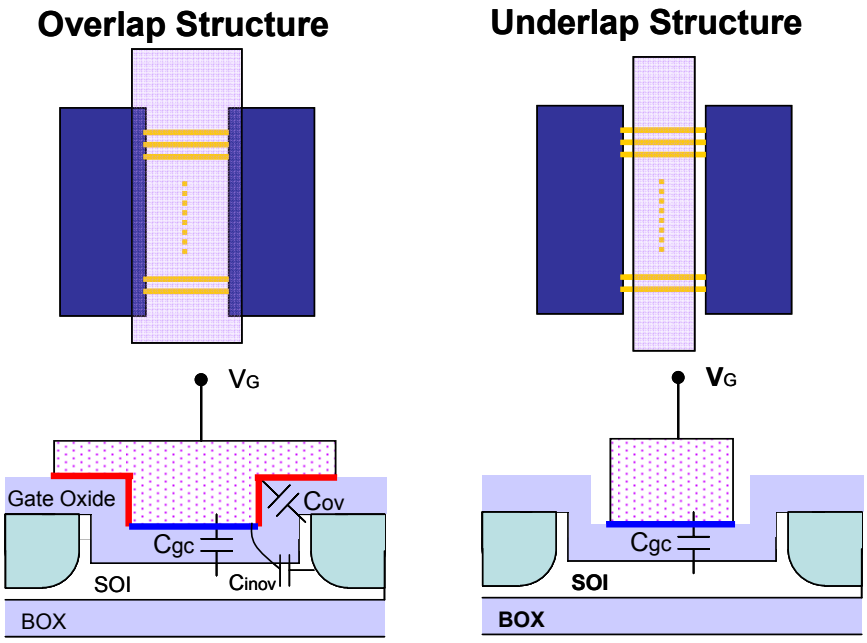


Figure 2.1 Schematics of overlap structure and under-lap structure in nanowire MOSFETs. Overlap structure concludes obvious parasitic capacitance while under-lap structure results in serious parasitic resistance.

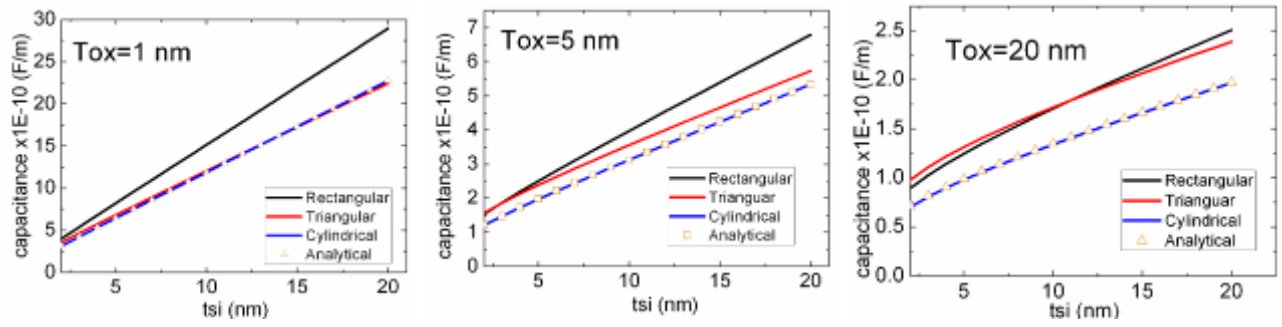


Figure 2.2 Calculated capacitance of SiO_2 coated single nanowire of various dimensions. Here, tsi changes from 1nm (left), 5nm (middle) to 20nm (right).

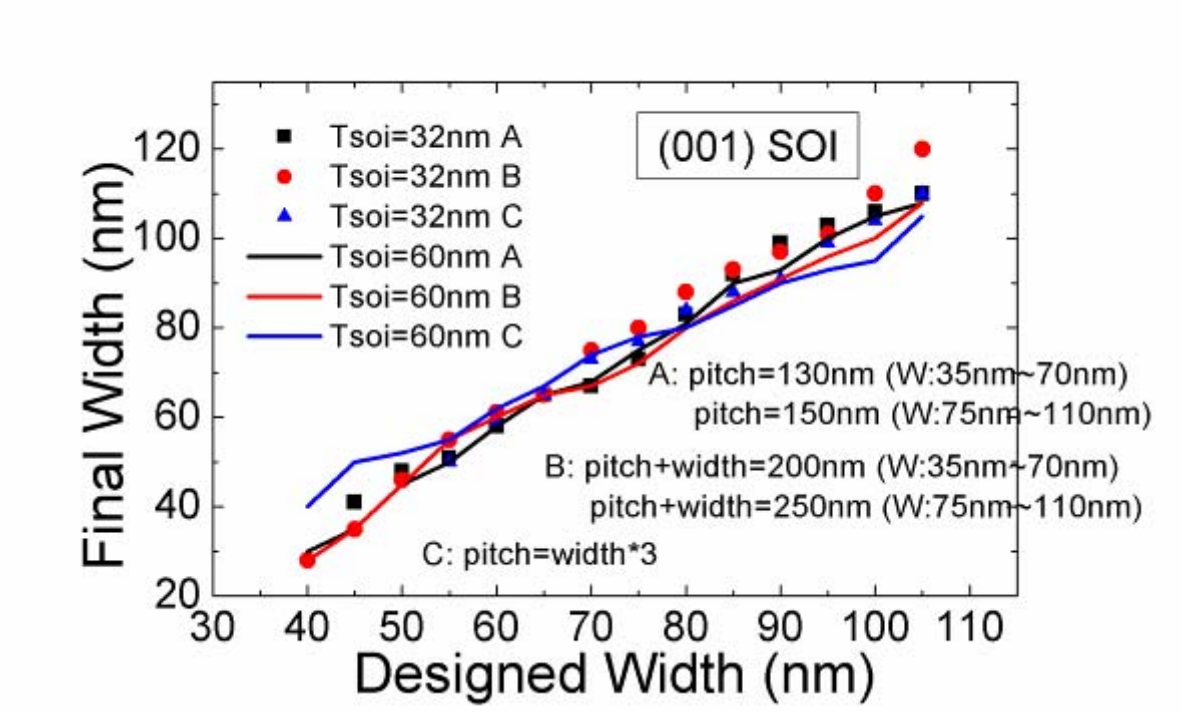
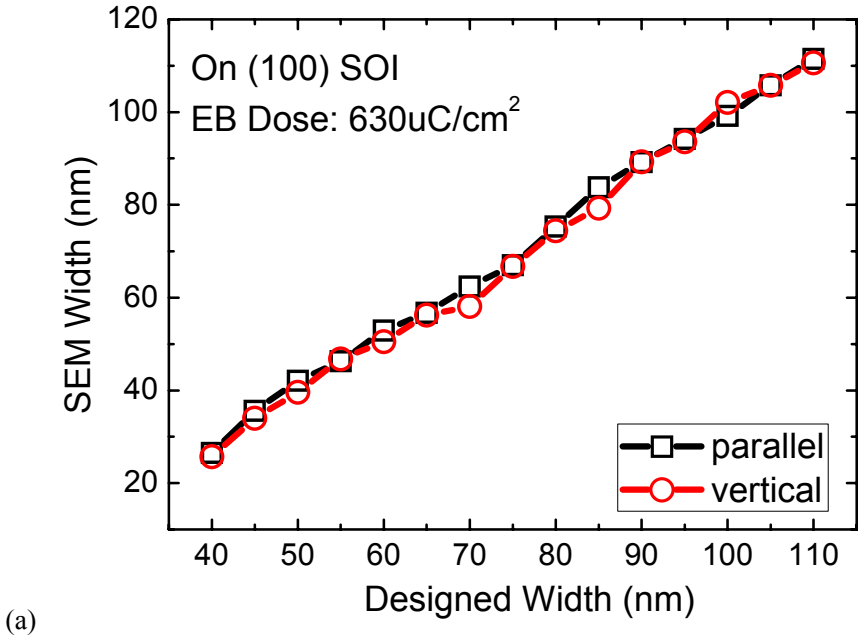
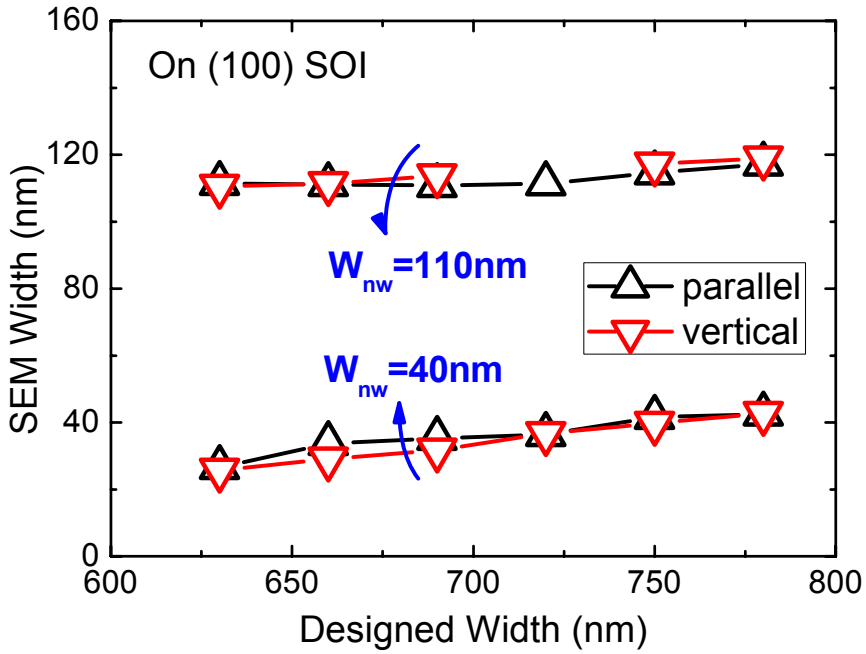


Figure 2.3 Comparisons between the designed nanowire width and nanowire width after development and dry etching. Here, different pitch designs are compared on SOI of various thicknesses.



(a)



(b)

Figure 2.4 Electron beam lithography (EBL) experiments (HSQ resist) on nanowire width. (a) Comparisons between designed width and width after EBL and dry etching, various nanowire widths of parallel/vertical directions are shown; (b) EB dose dependence of nanowire width of parallel/vertical directions.

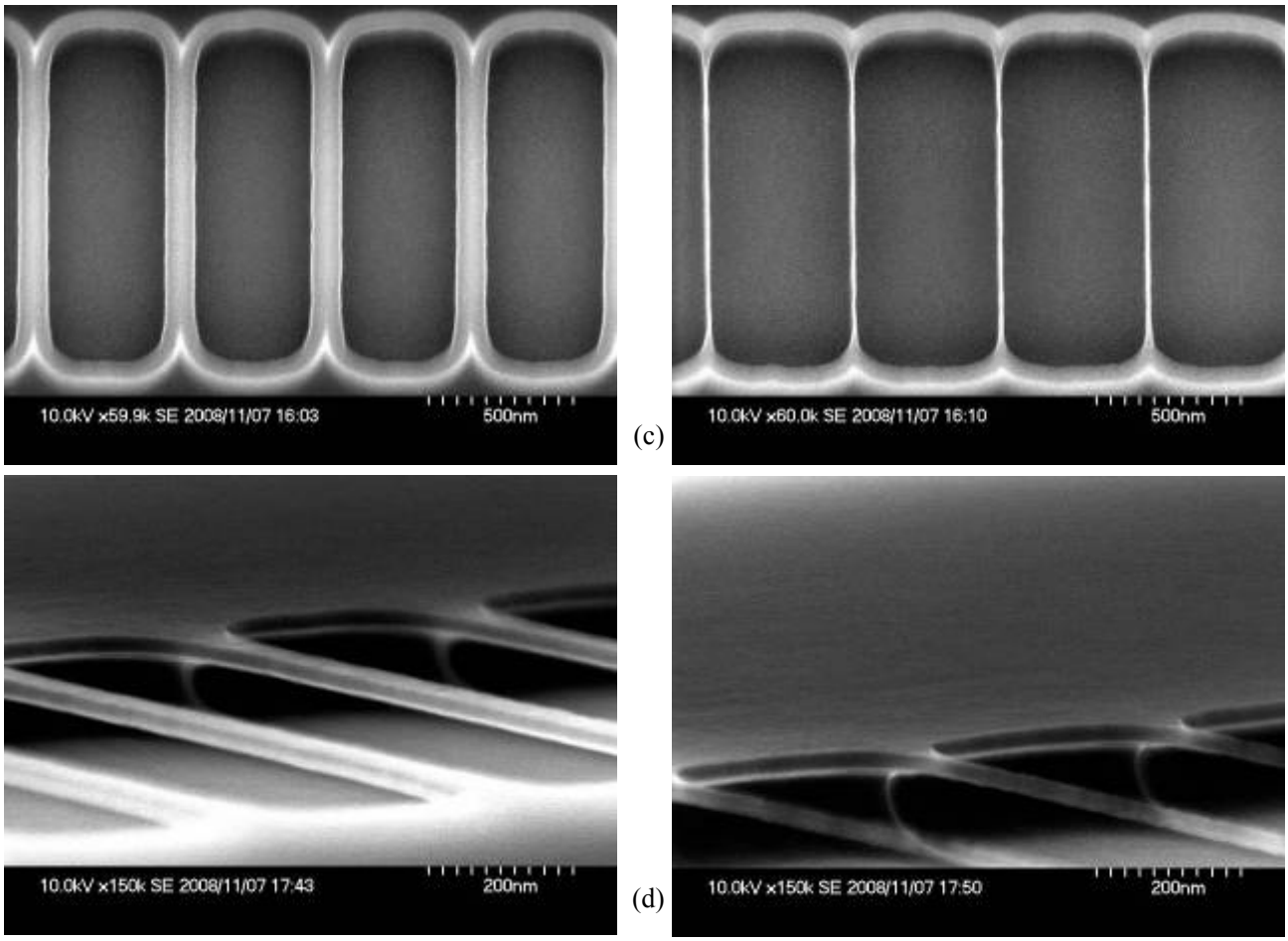


Figure 2.5 SEM observations of fabricated multiple nanowires. (a) and (c) are from top surface, while (b) and (d) shows 3-dimentional views from side surface. Here, nanowire width in (a)/(b) are ~ 100 nm wide, and nanowire width in (c)/(d) are ~ 14 nm wide.

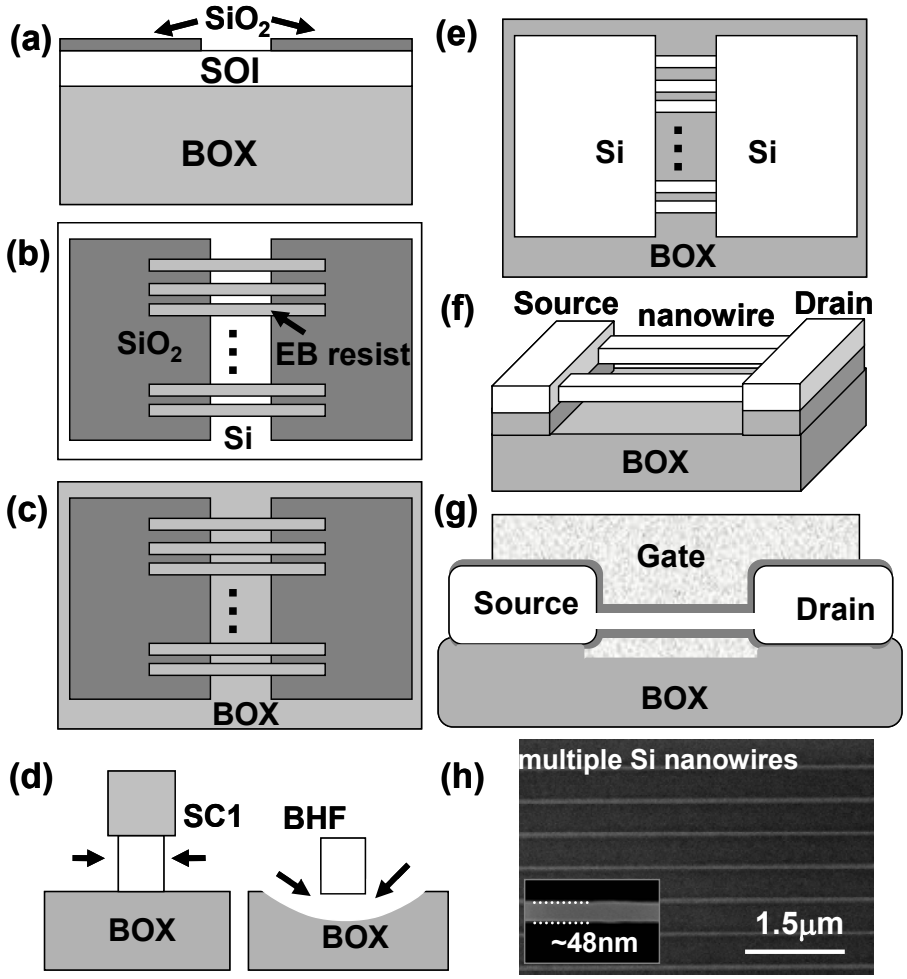


Figure 2.6 Main fabrication process flow of nanowire MOSFETs. (a) Formed mesa area after BHF wet etching; (b) nanowire pattern by EB lithography; (c) box layer is exposed after dry etching; (d) SC1 etching to reduce W_{nw} and BHF etching for GAA structure; (e) top view, and (f) and 3D structure after removing SiO_2 mask and EB resist; (h) cross section after gate poly-Si deposition; (g) SEM image of fabricated multiple Si nanowires, and the inset shows part of a single Si nanowire.

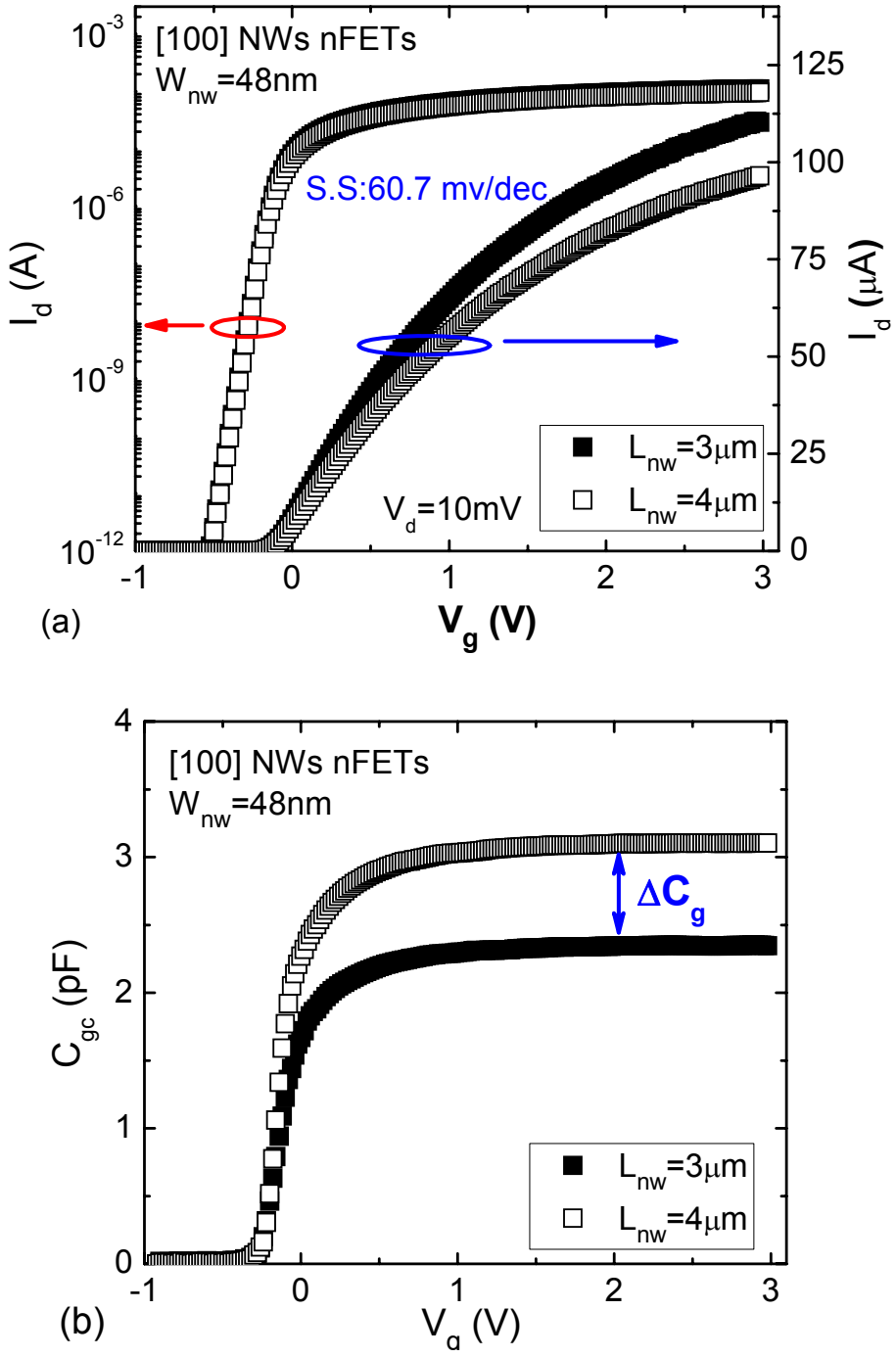


Figure 2.7 Measured characteristics in [100]/(100) nanowire nMOSFETs: (a) I_d-V_g at V_d=10mV; (b) C_{gc}-V_g. Here, L_{nw} values are 3 and 4 μm, and W_{nw} is 48 nm.

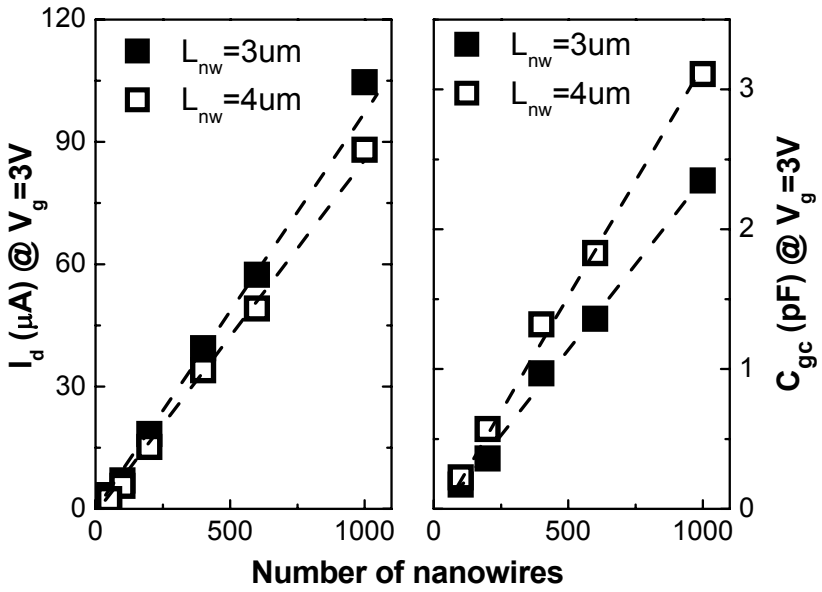


Figure 2.8 Linear relationship between the I_d / C_{gc} and nanowire number at V_g of 3 V.

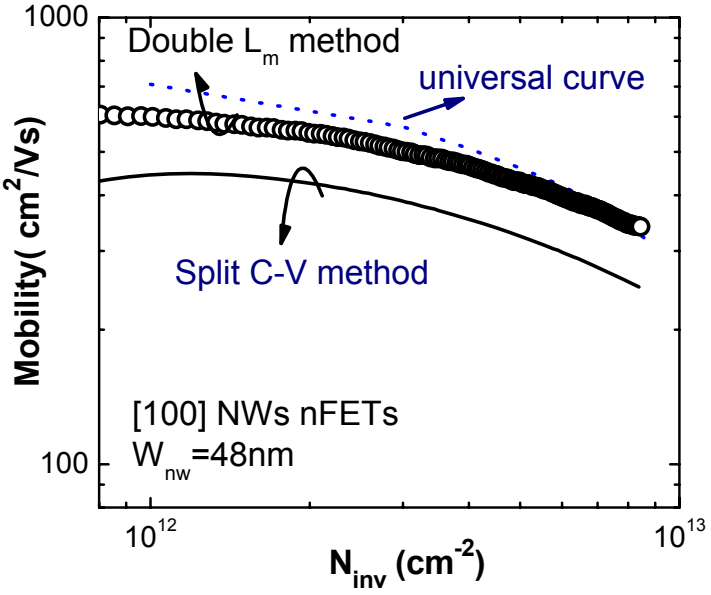


Figure 2.9 Measured electron mobilities in (a) [100]/(100) and (b) [110]/(100) nanowires by double L_{eff} method. The (100) bulk universal curve is used for reference.

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Chapter 3
Electron Mobility in Silicon Gate-all-around Nanowire nMOSFETs

3.1 Introduction

To suppress short channel effects (SCE) that are serious in traditional planar MOSFETs as scaling down, devices with multiple gates have been developed, such as MOSFETs with a double-gate (DG) structure [1]-[3], FinFETs with a DG or tri-gate (TG) structure [4]-[6], and nanowire FETs with a gate-all-around (GAA) structure [7]-[9]. However, there still exist a lot of things we don't understand on the transport characteristics, one of which is carrier mobility in nanowires. Just as we illuminated in last chapter, mobility directly affects the drive current and operation speed of devices. In planar MOSFETs, (100)-oriented surface owns the highest electron mobility, while (110)-oriented surface owns the highest hole mobility. Furthermore, higher electron mobility can be obtained in [100]-directed channel, while higher hole mobility can be obtained in [110]-directed channel [10]. Chanel orientation and direction dependence of planar MOSFETs and ultra-thin-body (UTB) MOSFETs have been studied widely [11]-[20]. However, due to limitations of fabrication and measurement technology, carrier mobility properties in nanowires have not been characterized well. Although there are some experimental works on mobility in nanowires [21]-[26], detailed analysis of nanowire width dependence down to sub-10nm wide nanowire MOSFETs is quite limited [26].

In this chapter, based on the advanced split CV method as we introduced in chapter 2, accurate measurements on electron mobility of [110]- and [100]-directed multiple NWs on both (100) and (110) SOI are carried out. Nanowire width dependence of electron mobility in <100>- and <110>-directed GAA nanowire nMOSFETs were compared and discussed. It is found that, in (100)-oriented nanowire nMOSFETs, although electron mobility degradations exist in narrower nanowires, electron mobility in nanowires of <110> direction approaches to that of <100> direction as the width is reduced to 7 nm wide. While in (110)-oriented nanowire nMOSFETs, [110]-directed mobility approaches to and is even higher than [100]-directed mobility. Furthermore, to understand physical mechanisms that dominate mobility properties in nanowires, low temperature measurements are performed and discussed.

3.2 Device Structure and Measurement Setup

The device structure is the same as described in chapter 2. Figure 3.1(a) shows a 3-dimentional schematic of fabricated multiple Si GAA nanowire nFETs. Gate oxidation is performed at 1000℃ for 10 minutes, which formed 13.6 nm SiO_2 on (100) planar surface and 21.6 nm SiO_2 on (110) planar surface. In our design, the overlap between gate and source/drain pads is 500 nm on each side and 40 nm undercut will be created under the source/drain pads. After gate oxidation, Tsoi on (100) is 22nm-30nm and Tsoi on (100) is 18 nm; the nanowire width W_{nw} is 7 nm-48 nm on (100) SOI and 24 nm-50 nm on (110) SOI. In this work, SiO_2 thickness (T_{ox}), SOI thickness (T_{soi}), or nanowire height, and W_{nw} were estimated by ellipsometry measurements and SEM observations. The cross section of 7 nm wide nanowires is further confirmed by TEM observation, as shown in Figure 3.1(b). Due to the retarded oxidation by accumulated stress [28]-[29], in 7 nm wide nanowire, gate oxide is only 4 nm on (100) surface and 13 nm on (110) surface. Ultra-thin-body (UTB) MOSFETs are also fabricated for reference.

3.3 Electron Mobility in Si Nanowires nMOSFETs at Room Temperature

3.3.1 (100)-oriented Si nanowire nMOSFETs

Figure 3.2 illustrates measured I_d-V_g characteristics of 7 nm wide nanowire nMOSFETs of both <100> and <110> directions at fixed drain voltage of 10 mV. The subthreshold slope (S.S.) is extracted to be ~62.0 mV/dec. In fact, S.S. values of all measured nanowire nMOSFETs shows almost no dependence on the nanowire width and the average value is 61.2 mV/dec. Ideal subthreshold characteristics originate from ideal surface interface and good gate-channel controllability from GAA nanowire structure. Figure 3.3 shows the measured C_{gc}-V_g characteristics of 7 nm wide nanowire nMOSFETs of different nanowire lengths (3 μm and 4 μm). By comparing these devices of different lengths, the intrinsic nanowire capacitances of 1 μm length are extracted in the same Figure. Simultaneously, 0.8~1.2 aF overlap capacitance for one 1μm nanowire can be estimated. This overlap capacitance belongs to the gated source/drain pads, including both gate overlap and undercut of the source/drain pads. In Figure 3.4, we summarized the extracted C_{gc} of 48 nm- 7 nm nanowire nMOSFETs at V_g of 3V. Furthermore, calculations on SiO_2 coated nanowire capacitance were performed for comparisons, using equations of $\mathbf{C_{gc} = 2\varepsilon_{ox} L_{nw} (W_{nw}/T_{ox(100)} + T_{soi}/T_{ox(110)})}$ and $\mathbf{C_{gc} = 2\varepsilon_{ox} L_{nw} (W_{nw} + T_{soi})/T_{ox(100)}}$ for <110>- and <100>-nanowires respectively. $T_{ox(100)}$ / $T_{ox(100)}$ indicate gate oxide thickness on (100) / (110) surfaces. In <100>-nanowire of 22 nm thick T_{soi}, calculation results (T_{ox}=6 nm, T_{soi}=22 nm) agree with the experimental data. While in <110>-nanowires of T_{soi}=18 nm, experimental data locates within the calculation result window of

different gate oxide conditions, $T_{ox(100)}/T_{ox(110)}$= 4 nm/13 nm and 13 nm/21 nm. To be particular, capacitance of 48 nm wide <110>-nanowire agrees with $T_{ox(100)}/T_{ox(110)}$= 13 nm /21 nm calculation results while that of 7 nm wide <110>-nanowire agrees with $T_{ox(100)}/T_{ox(110)}$= 4 nm/13 nm. This gives us evidence that the surrounded SiO_2 thickness in <110>- nanowires actually turns to be thinner in narrower nanowires.

Figures 3.5(a) and 3.5(b) show electron mobility in <100>-directed nanowire nMOSFETs with different T_{soi}. In wider nanowires of 48 nm W_{nw} on 22 nm T_{soi}, electron mobility converges to that in UTB nMOSFETs with T_{soi} of 30 nm, and mobility in nanowires of same width but on 30 nm thick SOI of is even higher than that of UTB nMOSFETs in high N_{inv} region. However, as W_{nw} is reduced from 48 nm to 7 nm, electron mobility degradation is clearly observed and the tendency is similar in nanowires of different SOI thickness. Figure 3.5 (c) illustrates the measured mobility in <110>-directed nanowires nMOSFETs on (100) SOI, where T_{soi} =18 nm. The mobility degradation with decreasing nanowire width is also observed. Figure 3.6 summarizes and compares measured electron mobility in (100) nanowires of <100>- and <110>-directions, as a function of nanowire width. Furthermore, it is found that electron mobility degradation in <110>-directed nanowire diminishes and turns to be comparable with <100>- directed nanowire in narrower nanowires. As shown in Figure 3.6, mobility in <110>-nanowire with 7 nm W_{nw} is close to that of <100>-directed nanowire. If we derive the mobility ratio of <110>- to <100>-directed nanowire, W_{nw} dependence of this ratio can be extracted in Figure 3.7. Interestingly, two different regions, Region A and B, can be distinguished. On the one hand, the mobility ratio of nanowires of two directions decreases as shrinking nanowire width from 48 nm to 21 nm, which is denoted as region A; while this ratio increases in narrower nanowires of 7 nm W_{nw}, as denoted as region B. This indicates that, in narrower nanowires, the predominance of <100>-directed nanowires in the viewpoint of high electron mobility shrinks; in other words, mobility degradation in <110>-directed nanowires of 7 nm W_{nw} is suppressed.

In this study, single GAA nanowire nMOSFET is treated as four separate planar nMOSFETs when the nanowire width is relatively large. As we know, in planar nMOSFETs, electron mobility is high in (100)-oriented surface no matter what the channel direction is, while it is ultra-low in (110)-oriented surface, especially in <110>-directed channel [10]. However, on the basis of Figures 3.6 and 3.7, it is found that obvious electron mobility degradation exists in narrower nanowires of both directions, though four surrounded surfaces of <100>-directed nanowire are of the same orientation and direction. Nevertheless, considering the side surface dependent concept in ref. [26]-[27], electron mobility in <110>-nanowires should be more degraded than in <100>-nanowires as shrinking nanowire width because of the increasing contribution from (110) side surfaces with low electron mobility. To make this problem clear, the relation between nanowire side surface contribution and electron mobility ratio of

<110>-directed nanowires to <100>-directed nanowires is extracted in Figure 3.8, where $T_{soi}/(T_{soi}+W_{nw})$ indicates the contribution from side surfaces. It is found that mobility ratio of two directions has a quasi-linear relationship with side surface contribution. That is, larger contribution from (110) surface with low electron mobility results in larger mobility degradation in <110>-directed nanowires. With this explanation, region A in Figure 3.7 also can be well understood.

As nanowire width is further shrunk to 7 nm, we can not treat single rectangular GAA nanowire MOSFETs as four separate planar MOSFETs anymore because of relative large quantum effect and gate-coupling from close side surfaces. But single ultra-narrower nanowire MOSFETs can be treated as two separate planar MOSFETs and one DG UTB MOSFET. So, we analyze electron mobility behaviors in region B by considering the subband structures in UTB MOSFETs with (100) and (110) surfaces, as illustrated in Figure 3.9.

In (100) UTB nMOSFET, the lowest 2-fold subband has a highest mobility, indicating that higher electron mobility for higher 2-fold subbands population while lower electron mobility for lower 2-fold subbands population. Compared with single-gate mode, surface potential confinement is reduced in DG, and the population of 4-fold subband increases [30]. Consequently, a (100) DG nMOSFET has smaller mobility than a (100) single-gate (SG) due to the subband modulations [30]-[32]. While in (110) UTB nMOSFET, lower confinement from DG mode increase the 2-fold subband population on the contrary, as a result, a (110) DG nMOSFET has larger mobility than (110) SG nMOSFET [33]. Please note, <110>-directed nanowire nMOSFET is in form of DG nMOSFET on (110) surface, and <100>-directed nanowire nMOSFET is in form of DG nMOSFET on (100) surface, as shown in Figure 3.9. Consequently, comparable mobility in <110> and <100> nanowire at region B can be understood considering the subband modulations from gate coupling between side surfaces. Besides, gate oxidation induced strain in narrower nanowires is also one possible reason that will cause electron mobility enhancement in <110>-nanowires, as reported in [26].

3.3.2 (110)-oriented Si nanowire nMOSFETs

For traditional CMOS, in view of high drive current, (100) is the best surface orientation for nMOSFETs while (110) is the best surface orientation for pMOSFETs [34]. However, in case of devices with short and narrow channel, it is found that the negative impart of (110)-oriented substrate on nMOSFETs is mitigated [34] [35]. In consideration of high hole mobility on (110)-oriented surface, studies of (110) nMOSFETs, including n-type FinFETs and nanowire nMOSFETs on (110) orientation surface, turn to be much more attractive.

Figure 3.10 illustrates the measured I_d-V_g characteristics in [100]-directed nanowire nMOSFETs that contain 1000 nanowires, where W_{nw} ranges from 24 nm to 50 nm and L_{nw} is 2 μm. In all measured devices, good

sub-threshold region were observed, where the subthreshold slope (S.S.) is around 61.5 mV/dec, which is quite close to the ideal 60 mV/dec. The inset in Figure 3.10 shows the measured drain current at V_g=3V, as a function of nanowires number, where the linear relationships are clearly observed. On the basis of advanced split C-V method, electron mobility in nanowires on (110)-oriented SOI is measured and shown in Figure 3.11. In [100]-directed nanowires, electron mobility in nanowires of 30 nm W_{nw} is lower than that in nanowires of 46 nm W_{nw} although the degradation is small; However, in [110]-directed nanowires, electron mobility in nanowire of 30 nm W_{nw} turns to be higher than that in nanowire of 46 nm W_{nw}.

For further investigations, in Figure 3.12, W_{nw} dependence of nanowire mobility and relative mobility ratio are illustrated. The mobility degradation in [100]-directed nanowire are observed as shrinking W_{nw}. However, in [110]-directed nanowires, surprisingly, narrower nanowire has higher mobility on the contrary and is even higher than universal mobility in [110]/(110) planar nMOSFETs in [10]. This is impressive since large electron mobility on (110) surface indicates higher drive current and faster operation speed in (110) CMOS circuit.

To understand the observed electron mobility behaviors, still, we treat single nanowire nMOSFET as four separate planar nMOSFETs. As we know, in planar MOSFETs, electron mobility in [110]/(110) nMOSFETs is higher than that in [100]/(110) nMOSFETs. Thus, the observed mobility enhancement in narrower [110]-directed nanowires, as shown in Figure 3.11(b), can be explained by considering larger contribution of (100) side surface with high electron mobility. However, this kind of mobility improvement can never be observed in [110]-directed nanowires on (100) surface because the (110) side surfaces have lower electron mobility than the (100) top/bottom surfaces, consequently, larger contribution of (110) side surfaces will result in lower mobility in narrower nanowires on the contrary. Therefore, electron mobility degradation in (110) nMOSFETs can be recovered to some extent by utilizing [110]-directed nanowire nMOSFETs.

3.4 Electron Mobility Characteristics at Low Temperatures

For better understandings on mechanisms that dominate the mobility degradation in narrower nanowires, low temperature measurements are performed from room temperature (RT) down to 40 K, on the basis of fabricated [100]-directed multiple Si nanowire nMOSFETs on (100) SOI. The results are illustrated in Figure 3.13, where the carrier inversion density (N_{inv}) dependence changes as lowering the temperature. Normally, carrier mobility behaviors are affected by three parts that dominated by different scattering mechanisms, that is, Coulomb scattering mobility (μ_c), phonon scattering mobility (μ_{ph}) and surface roughness scattering mobility (μ_r) [36]. Wherein, μ_c and μ_r dominate at low and high N_{inv}, respectively, and have no temperature dependence. However,

μ_{ph} has strong temperature dependence and dominate mobility behaviors at RT. As lowering the measurement temperature, μ_{ph} will be suppressed, as a result, electron mobility enhancement can be observed. Furthermore, slope values of μ_{eff} to N_{inv} are also estimated from measured μ_{eff}~N_{inv} characteristics, as denoted in the same Figure, showing increasing slope values from -0.22 to 0.44. This phenomenon is similar to the reported data in a bulk MOSFET [37].

Figure3.15 illustrates electron mobility in [100]-NWs at 40 K with T_{soi} of 30 nm. Electron mobility degradation with shrinking W_{nw} is observed at 40 K, and shows similar tendency to the electron mobility behaviors at RT. Furthermore, in Figure 3.16, W_{nw} dependence of mobility in nanowires of 30 nm T_{soi} is extracted at various temperatures, from RT to 40 K. It is found that electron mobility degradation slope with respect to W_{nw} increases as lowering the temperature.

For further understanding s on surface roughness scattering in nanowires, it is necessary to study the temperature dependence of electron mobility in nanowires by considering μ_{eff}~T^{α}, where the experimental α value is -1.75 for μ_{ph} [36]. Since the mobility determined by μ_r should have no dependence on the temperature as we explained in former section, as a result, α should approach to zero as lowering the temperature. Here, α is extracted by deriving $\Delta ln\mu_{eff}/\Delta lnT$ and its dependence on W_{nw} is shown in Figure 3.17. α value degradation slopes are almost same in all measured temperature stages. By using Matthinessen's rule of $\mu_{ph}^{-1}=\mu_{eff}(RT)^{-1}-\mu_r(40K)^{-1}$, μ_{ph} are extracted in the inset of Figure 3.17. Electron mobility measured at 40 K is considered as μ_r since μ_{ph} is enough weak and can be almost ignored at such low temperature. In this way, on the one hand, it is confirmed that μ_{ph} degradation is small in nanowires of beyond 20 nm W_{nw}; On the other hand, improvement of μ_{eff} in 15 nm nanowires is observed, which maybe result from the volume inversion effect due to formed GAA structure [30], though further experimental data is necessary to confirm it.

Then, N_{inv} dependence of α is extracted and shown in Figure 3.18. It is observed that α decreases and approaches to zero in narrower nanowires of 22 nm T_{soi} (Figure 3.18(a)) and thinner nanowires of 26 nm W_{nw} (Figure 3.18(b)). It is believed that much more serious surface roughness scattering together with Coulomb scattering exist in narrower and thinner nanowires. It should be noted here that an interesting thing can be observed here, that is, a peak exists in extracted α-N_{inv} characteristics, which is attributed to different scattering mechanisms domains. Particularly, α approaches to zero at low N_{inv} where the Coulomb scattering dominates and at high N_{inv} where the surface roughness scattering dominates.

3.5 Anomalous Mobility Behavior in Silicon Nanowire nMOSFETs

Figure 3.19 illustrates the W_{nw} dependence of mobility at 100K, which shows the "double peaks" behavior. The narrower NW has smaller "double-peak" spacing, which is observed only at middle N_{inv} region, where electron mobility is dominated by increased μ_{ph} as well as fixed μ_r and μ_c. Therefore, to understand this, it deserves to study the temperature dependence of μ_{ph} in detail. For phonon scattering, there are two important competition factors: phonon momentum ($p_{ph}=\hbar\omega/c\sim K_BT/c \propto T$) and Fermi momentum ($p_F=\hbar\pi^{0.5}N_{inv}^{0.5} \propto N_{inv}^{0.5}$) [37] [38]. In a simple word, at low temperatures, large angle scattering is restricted at middle-high N_{inv} region due to foresaid two competition factors. On the basis of Figure 3.20(a), we can explain it like this, on one hand, μ_{ph} behavior still follows conventional model and decreases along with respect to N_{inv} at low N_{inv} region; on the other hand, μ_{ph} increases with respect to N_{inv} at middle-high N_{inv} region, where the Fermi momentum is larger than the phonon momentum. Therefore, the N_{inv} value of the "transition point" within μ_{ph} turns to be lower as decreasing the temperature.

At the middle-low temperature of 100 K, the turning point of μ_{ph} locates within the lines of μ_c and μ_r, where μ_{ph} still affects the effective mobility in nanowires. Then, the observed anomalous "double-peak" mobility behavior in nanowires can be explained qualitatively by considering the degradation of μ_c and μ_r in narrower nanowires. Supposing the same μ_{ph} behaviors, lower μ_c and μ_r will cause narrower region that is affected by μ_{ph}, as a result, the spacing between double peaks decreases, as shown in Figure 3.20(b). W_{nw} dependence of "double-peak", from another point of view, proves the increasing surface roughness scattering and Coulomb scattering in narrower nanowires.

3.6 Summary

Electron mobility in [100]- and [110]-directed NWs on both (100)- and (110)-oriented SOI has been measured and discussed in this chapter. The main conclusion is that side surface orientation plays a key role in nanowire mobility if we consider the nanowire as a whole. It is found that, on (100) SOI, mobility of (100)-oriented nanowires decreases monotonically as narrowing nanowire width due to serious process-induced roughness in narrower nanowires. While on (110) SOI, electron mobility in [110]-directed nanowires approach to and is even higher than [100]-directed nanowires because of the increasing contribution from (100) side wall with high electron mobility. Also, measurements on [100]/(100) NWs at low temperatures were performed systematically. Anomalous 'double peak' is observed in NW mobility behavior at 100K and shows clear dependence on Wnw, which also originates from serious surface roughness scattering and coulomb scattering in narrower NWs.

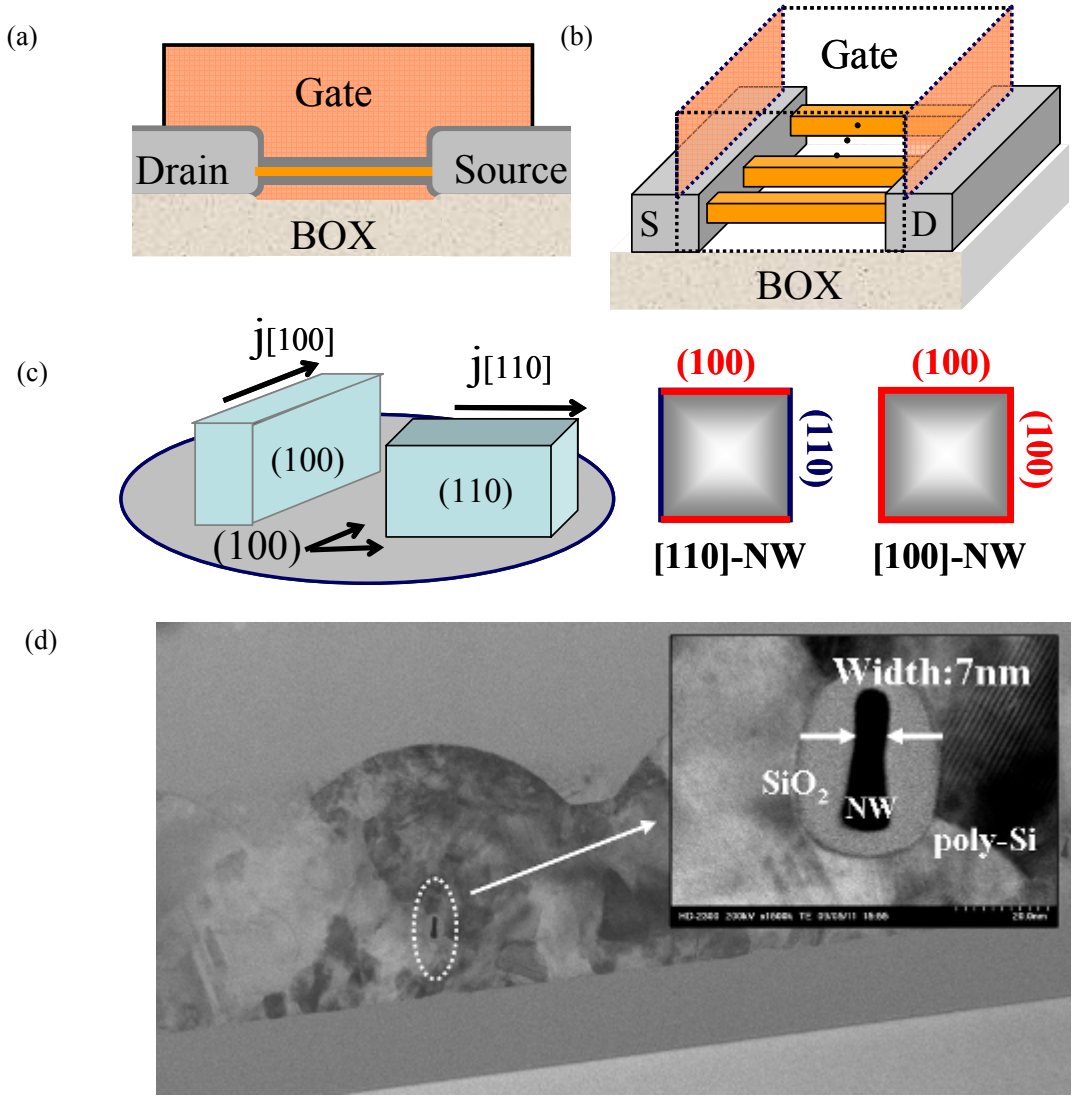


Figure 3.1 (a) A cross section view and (b) a three-dimensional schematic of the fabricated multiple nanowires GAA MOSFET; (c) Schematics of [100]- and [110]-directed nanowires and their relative side surface orientation; (d) shows a TEM photography of <110>-directed gate-all-around nanowire (W_{nw}=7 nm), surrounded by 4 nm/13 nm SiO_2 on top/side surface and poly-Si gate.

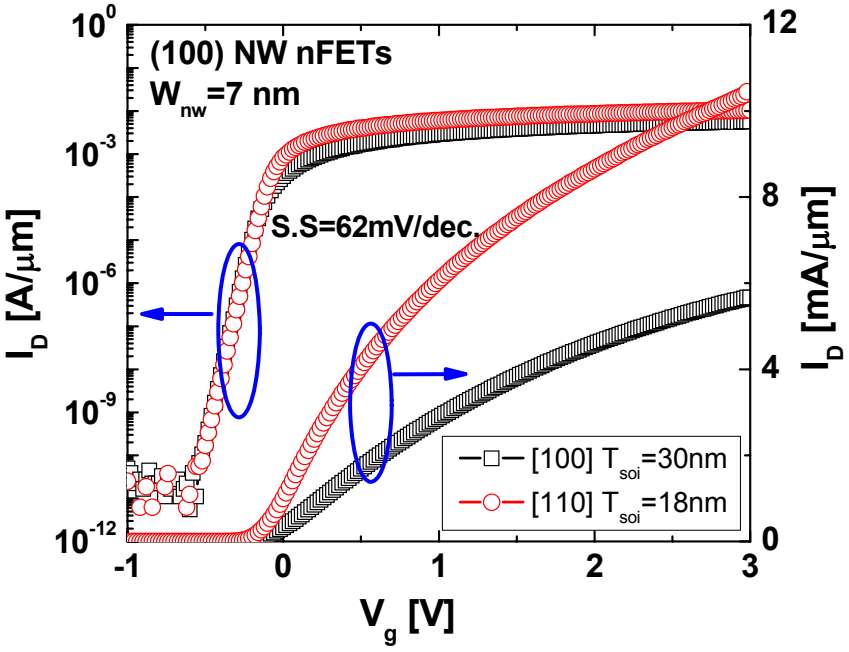


Figure 3.2 I_d-V_g characteristics of 7 nm wide nanowire nMOSFETs of <100> and <110> directions, normalized by nanowire numbers and lengths. S.S. factors of 62.0 mV/dec indicate good surface control and gate-channel controllability.

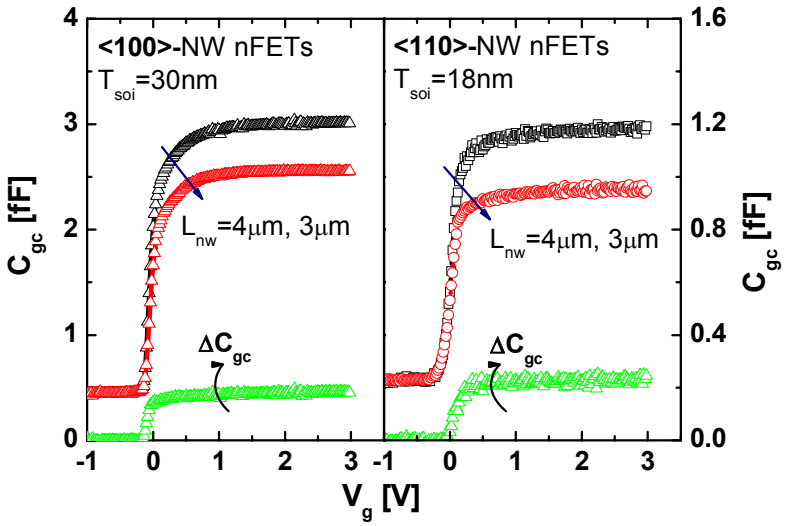


Figure 3.3 C_{gc}-V_g characteristics of 7 nm wide nanowire nMOSFETs of <100> and <110> directions, normalized by nanowire numbers. ΔC_{gc} is extracted by subtracting nanowire C_{gc} of L_{nw}=3 μm from L_{nw}=4 μm, indicating the intrinsic C_{gc} of one 1μm nanowire.

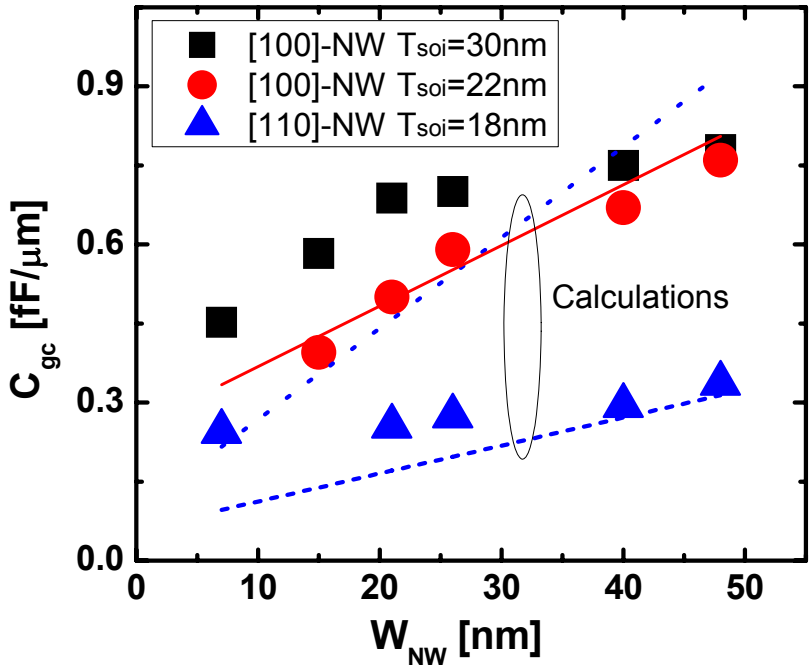
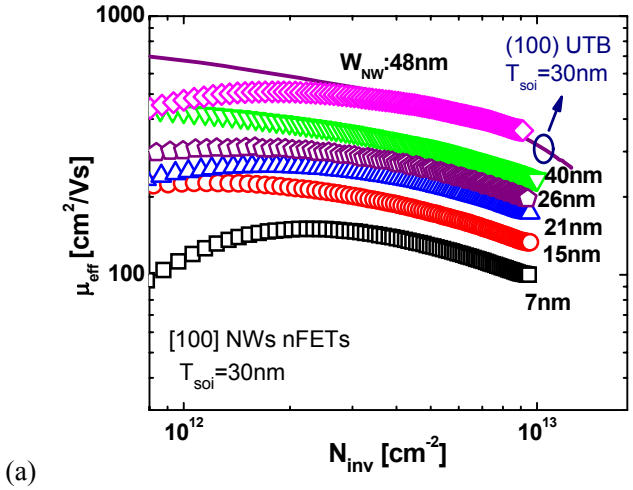
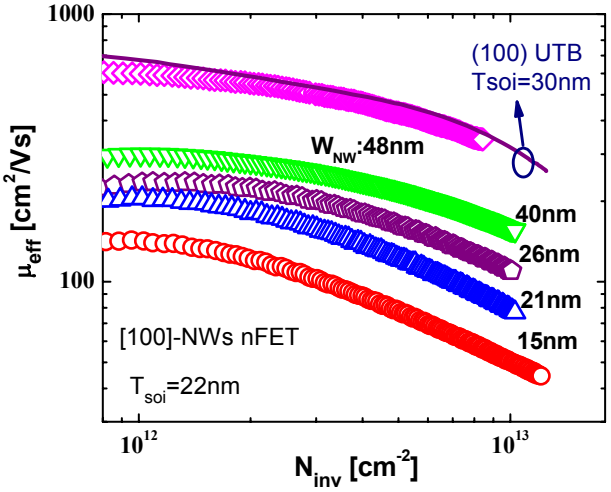


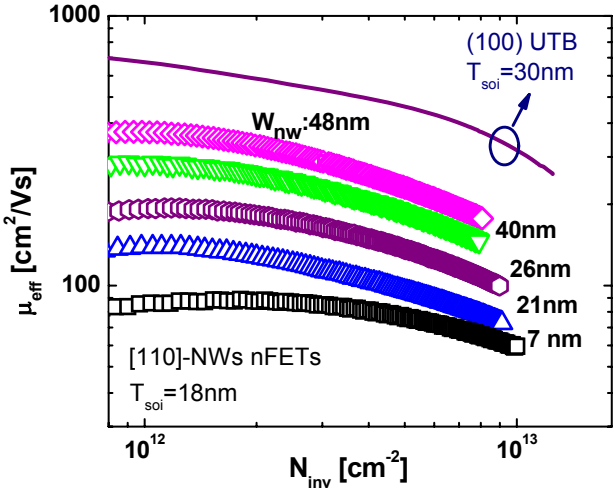
Figure 3.4 Extracted C_{gc} of one single nanowire of various W_{nw} (from 48 nm to 7 nm) and T_{soi} (18 nm, 22 nm and 30 nm). Here, C_{gc} is taken at V_g=3 V. Calculation results are also shown, using equations of $C_{gc} = 2\varepsilon_{ox} L_{nw} (W_{nw}/T_{ox(100)} + T_{soi}/T_{ox(110)})$ and $C_{gc} = 2\varepsilon_{ox} L_{nw} (W_{nw} + T_{soi})/T_{ox(100)}$ for <110>- and <100>-nanowires respectively. The solid line is calculation result on <100>-nanowire of T_{ox}=6 nm, T_{soi}=22 nm; while the dot (dash) lines are calculations on <110>-nanowires of T_{soi}=18nm, $T_{ox(100)}/T_{ox(110)}$= 4 nm/13 nm (the dot line)and 13 nm/21 nm (the dash line).



(a)



(b)



(c)

Figure 3.5 Measured electron mobility of (a) <100>-directed nanowires with T_{soi}=30 nm; (b) <100>-directed nanowires with T_{soi}=22 nm; (c) <110>-directed nanowires of T_{soi}=18 nm. Electron mobility degradation is observed in both <100>- and <110>-directed nanowires.

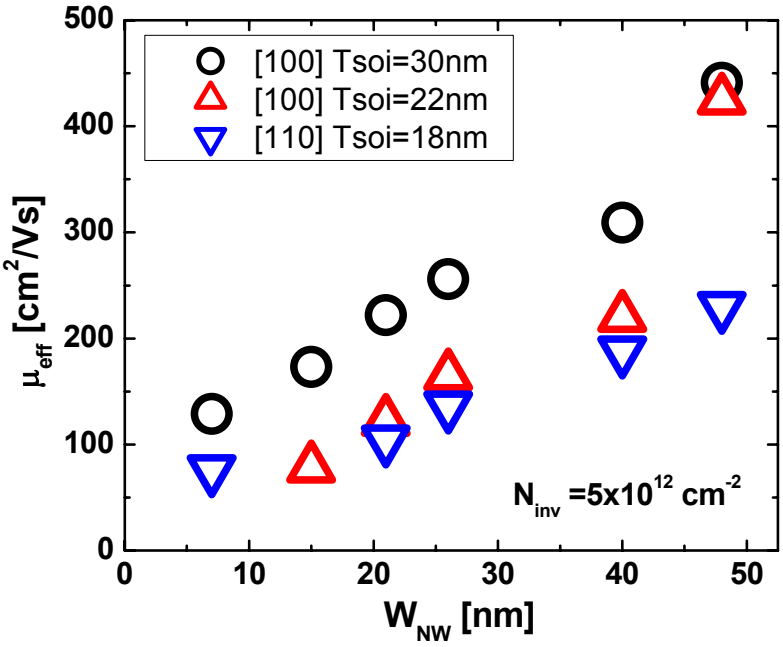


Figure 3.6 Electron mobility at N_{inv}=5x10^{12} cm^{-2} as a function of W_{NW}. W_{NW} estimations have 5nm error by SEM observations.

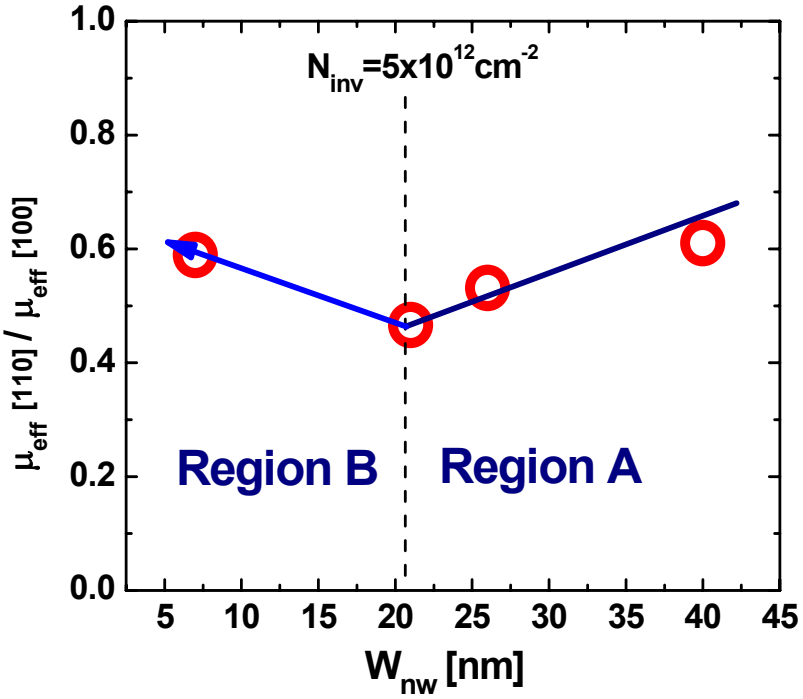


Figure 3.7 W_{nw} dependence of Mobility ratio of <110>- to <100>-directed nanowires. The mobility ratio decreases firstly and then increases as shrinking W_{nw} from 40 nm to 7 nm.

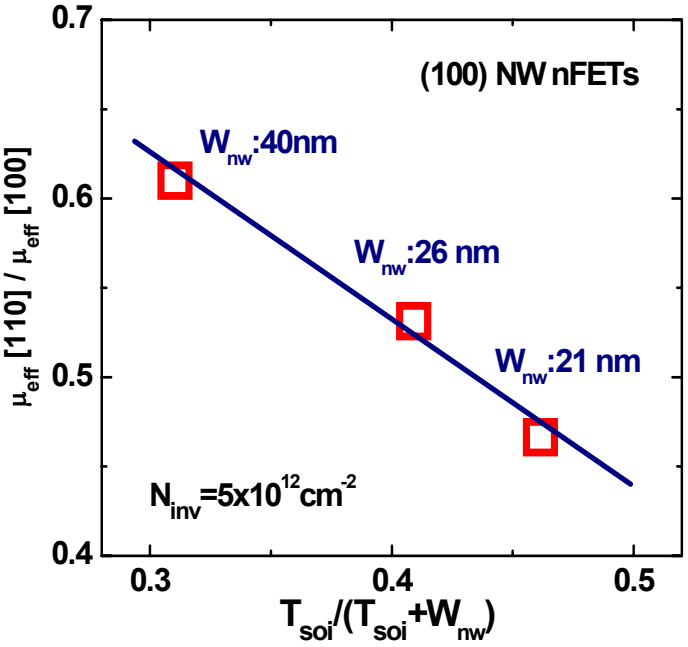


Figure 3.8 Relationship between mobility ratio of <100>- to <110>-directed nanowire with side surface contribution expressed by $T_{soi}/(T_{soi}*W_{nw})$.

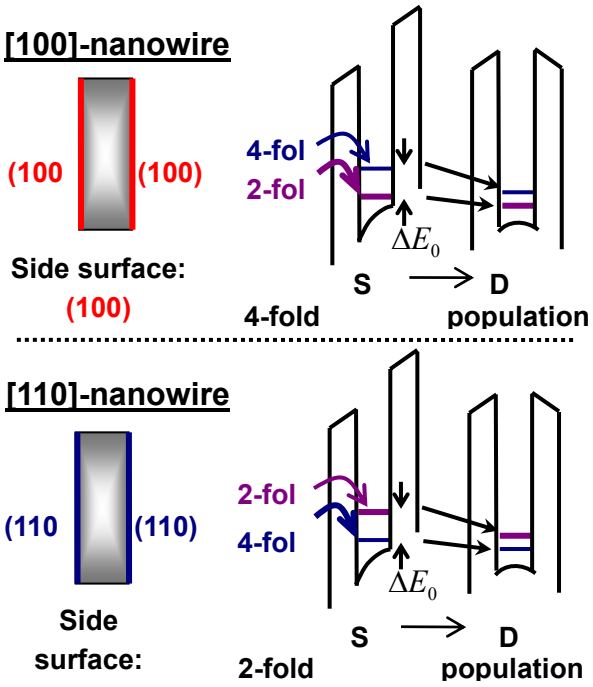


Figure 3.9 Schematic illustrations of subband modulations result from gate coupling effect when single-gate turns to be double-gate in narrower nanowire, with one-dimensional confinement on (100) surface and (110) surface, respectively.

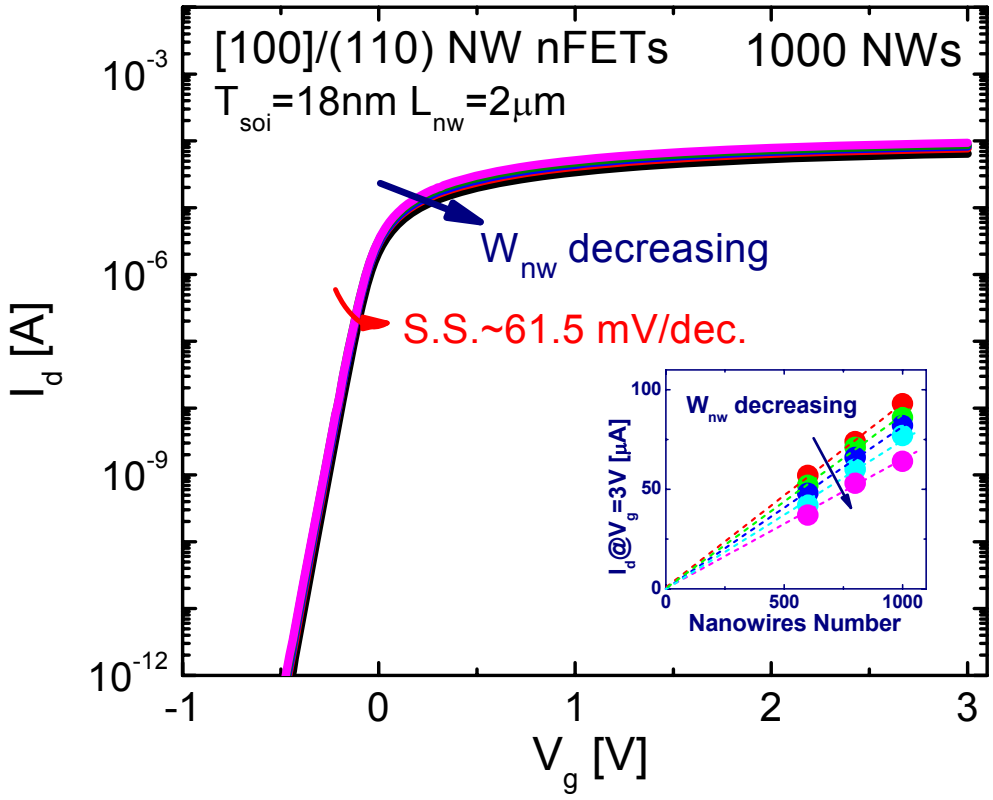
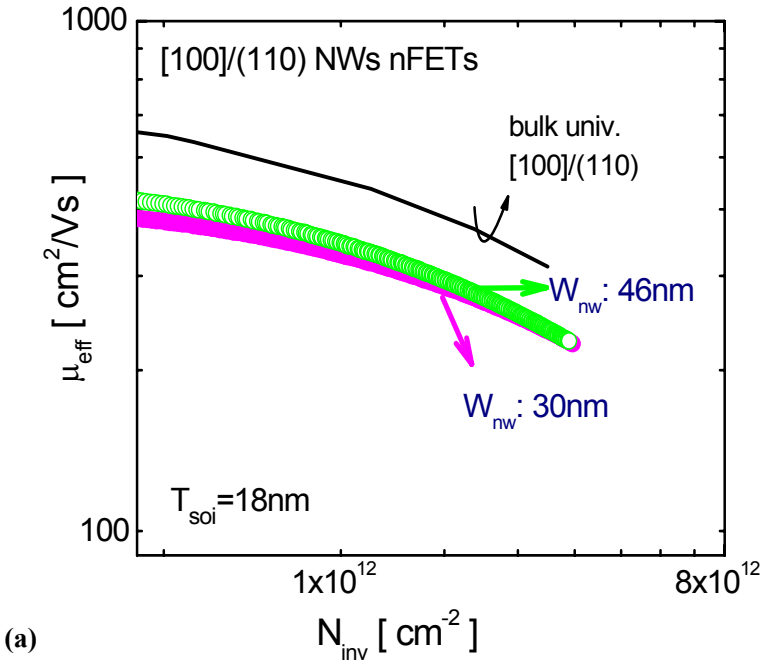
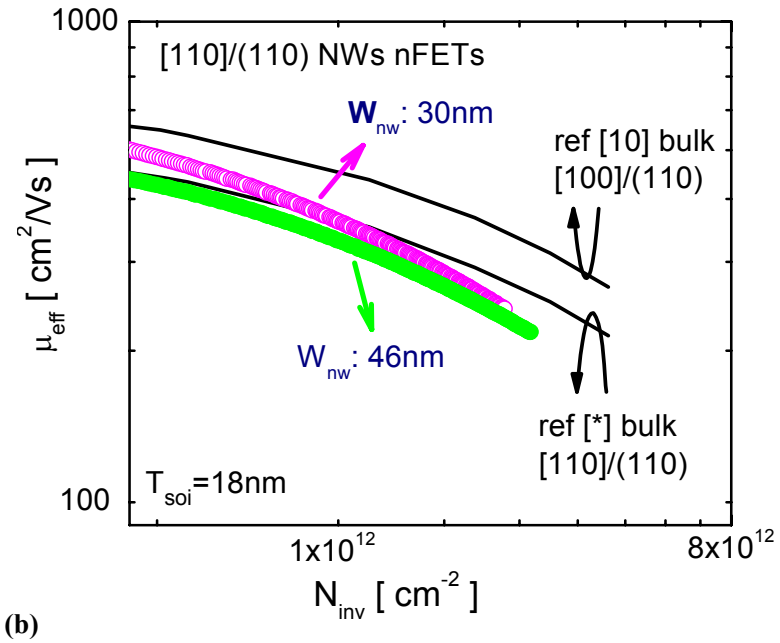


Figure 3.10 I_d-V_g characteristics in [100]-directed nanowires nFETs containing nanowires of various width W_{nw}, from 50 nm to 24 nm, T_{soi}=18 nm. Inset: I_d as a function of nanowires numbers at V_g=3 V.



(a)



(b)

Figure 3.11 Measured electron mobility in (a) [100]- and (b) [110]-NWs on (110) SOI. In [100]/(110) NWs, mobility degradation is observed while in narrower [110]-NWs, surprisingly, mobility improvement is obtained.

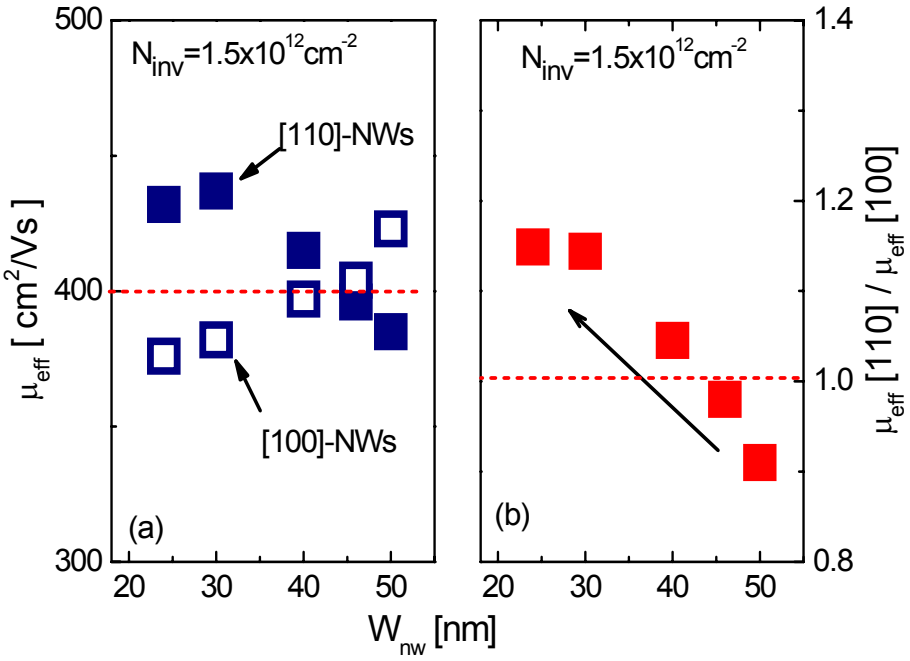


Figure 3.12 W_{nw} dependence of (a) electron mobility in [100]/(110) and [110]/(110) NWs and (b) relative mobility ratio at N_{inv}=1.5x10^{12}cm^{-2}. μ_{eff}[110] turns to be higher than μ_{eff}[110] in narrower NWs.

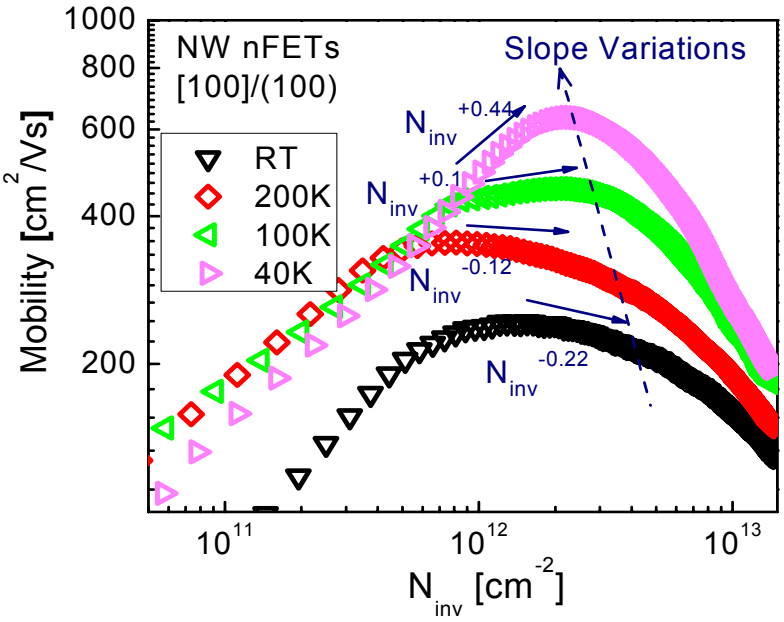


Figure 3.13 N_{inv} dependence on electron mobility at temperatures from 40K to RT. Estimated slope values turns from -0.22, -0.12, +0.1 to +0.44

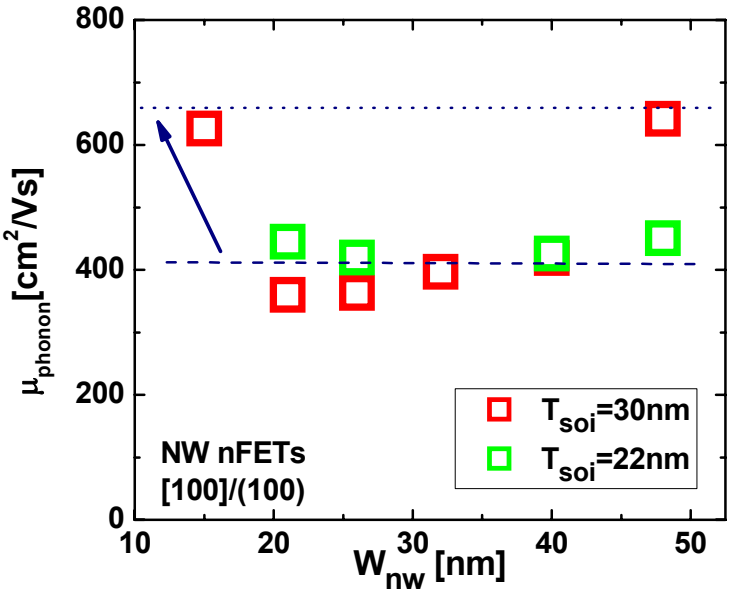


Figure 3.14 W_{nw} depdendence of μ_{phonon} values by the Matthinessen's rule of $\mu_{phonon}^{-1}=\mu_{eff}(RT)^{-1}-\mu_{rough}(40K)^{-1}$

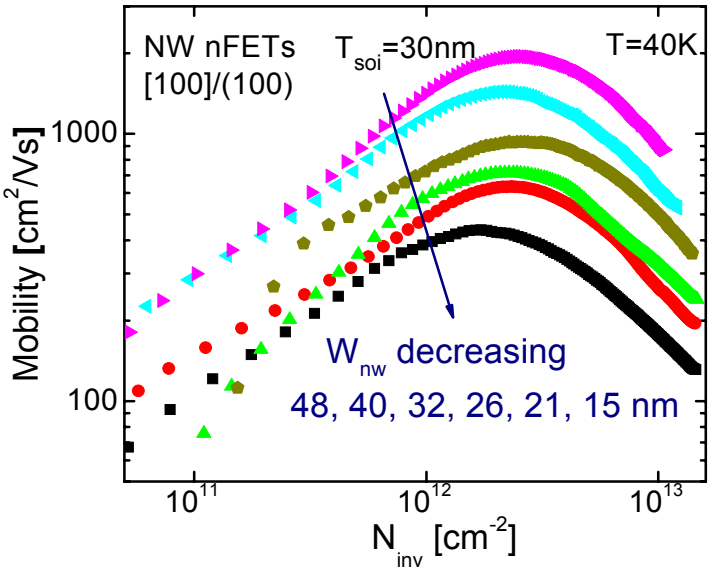


Figure 3.15 Electron Mobility in [100]-NWs at 40K, T_{soi}=30nm. Mobility degradation is clearly observed as shrinking W_{nw} from 48nm to 15nm.

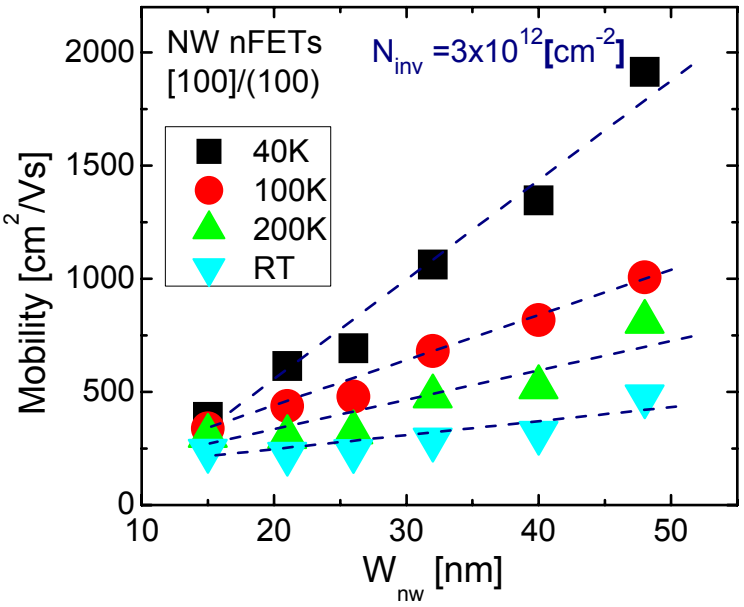


Figure 3.16 Electron mobility in [100]/(100) NWs of various width at N_{inv}=3x10^{12} cm^{-2}, T_{soi}=30nm. Measurement temperature ranges from RT to 40K.

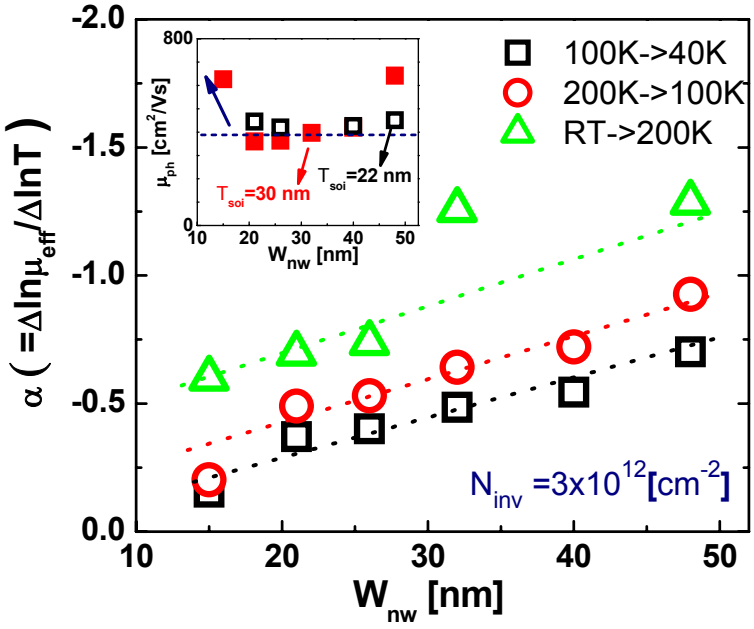


Figure 3.17 Relation between temperature dependence and nanowire width at N_{inv}=3x10^{12}cm^{-2}, from RT to 40K.

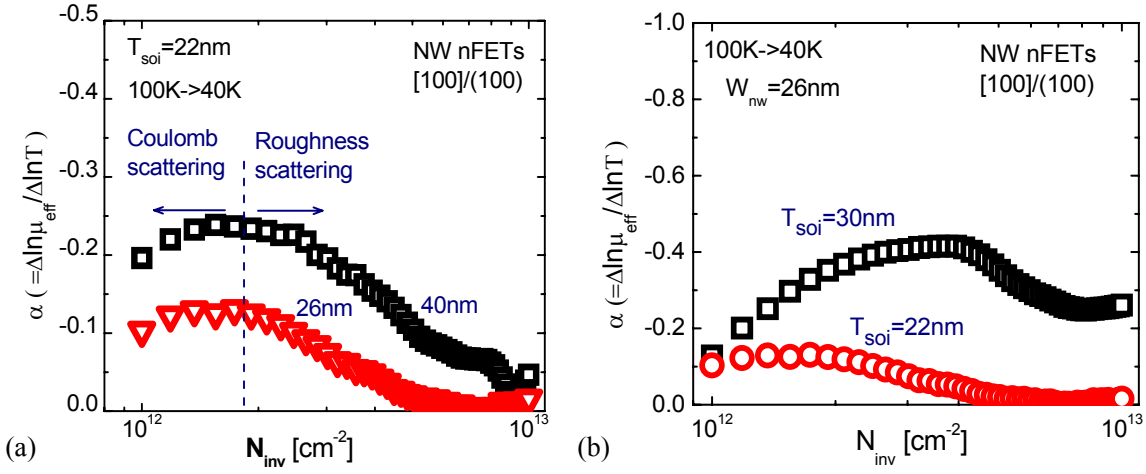


Figure 3.18 (a) N_{inv} dependence of α in NWs with W_{nw} of 26nm and 40nm, T_{soi}=22nm. (b) N_{inv} dependence of α in NWs with T_{soi} of 30nm and 22nm, W_{nw}=26nm.

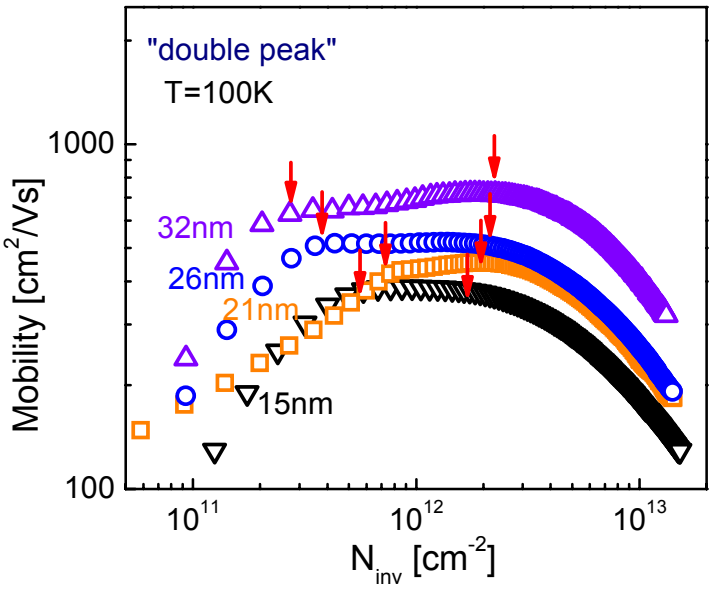


Figure 3.19 Observed "double peak" mobility at 100K in NWs of various widths. It is also observed that the spacing between double peaks decreases in narrower NWs.

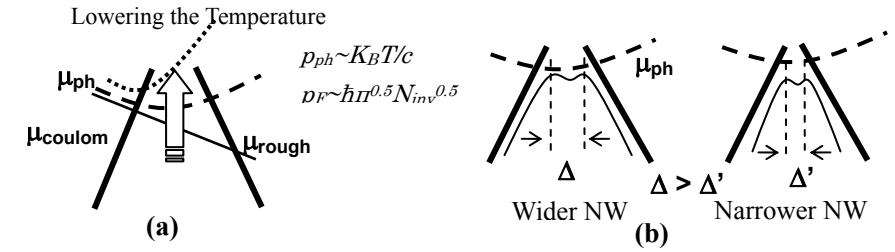


Figure 3.20 Schematic illustrations to explain possible mechanism that causes 'double peak' phenomenon as lowering the temperature. Observed W_{nw} dependence of spacing between double peaks originates from lower μ_{rough} and $\mu_{coulomb}$ in narrower NW.

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Chapter 4
Hole Mobility in Silicon Gate-all-around Nanowire pMOSFETs

4.1 Introduction

Electron mobility behaviors in Si nanowire nMOSFETs have been described in chapter 3, showing the important role of side surface orientation, which dominates the average mobility modulation as reducing the nanowire width. In this chapter, hole mobility in Si nanowire pMOSFETs will be investigated and discussed. On the contrary to electron mobility, in view of high hole mobility, (110) is the optimized surface orientation and [110] is the optimized channel direction [1-4]. Consequently, effects of side surface orientation with respect to nanowire width should be different for hole mobility in nanowires. Until now, there are quite limited works on hole mobility in nanowires. [5-9]

In this chapter, to elucidate hole transport characteristics in nanowires, experimental and theoretical investigations on the hole mobility in both (100) and (110) nanowire pMOSFETs are carried out from room temperature (RT) to the low temperature of 40K, utilizing the advanced split CV method introduced in chapter 2. In (110)-oriented nanowire pMOSFETs, at high N_{inv}, high hole mobility in narrow [110]-nanowire is achieved for the first time and, surprisingly, approaches to that in wide [110]-directed nanowires. The underlying physics are also discussed in this chapter.

4.2 Device Structure and Measurement Setup

The device structure and measurement setup studied in this chapter is the same as that in chapter 3, just the source/drain doping type is changed from n-type to p-type. Nanowire height is 12nm and 19nm on (100) surface, while 18nm on (110) surface. (100)-oriented nanowires pMOSFETs of [110] and [100] directions are fabricated on different SOI chips, while (110)-oriented nanowires pMOSFETs of two directions are fabricated on the same (110) SOI by rotating channel direction 90 degree. Nanowire widths (W_{nw}) after gate oxidation ranges from 15nm to 68 nm. Figure 4.1(b) shows the observed SEM image of suspended nanowires after removing the gate oxidation. Thick ultra-thin-body (UTB) pMOSFETs are also fabricated on the same chip for reference.

4.3 Hole Mobility in (100)-oriented Silicon nanowire pMOSFETs

Figure 4.1 (a) shows the measured I_d-V_g characteristics of measured [100]-directed nanowire pMOSFETs, where nanowire nMOSFETs characteristics are also shown for comparison. Figure 4.1(b) shows the calculated subband structure of electron and hole, by effective-mass method (EMA) for electron subbands [10] and six-band k.p. method for hole subbands [11-14]. Because of smaller effective mass that is perpendicular to (100) surface, V_{th} shift is large in nanowire pMOSFETs (heavy hole, m_h=0.29m_0) but small in nanowire nMOSFETs (m_e=0.918m_0). Furthermore, in Figure 4.2, detail calculations on subband structure of nanowire pMOSFETs are illustrated, indicating that small V_{th} shift can be obtained in (110)/[100] nanowire pMOSFETs due to four surrounded (110)-oriented surface with heavy effective mass (heavy hole, m_h=0.59m_0).

Figure 4.3 shows the extracted hole mobility in (100)-oriented nanowire pMOSFETs of both [100] and [110] directions, with W_{nw} ranging from 15nm to 40nm. Hole mobility decreases monotonically as decreasing W_{nw}, which is quite similar to (100)-oriented nanowire nMOSFETs that were described in chapter 3. In case of 40 nm wide [100]-nanowire pMOSFETs, hole mobility is quite close to 30nm thick UTB pMOSFETs. It is also found that, hole mobility in 21 nm wide [110]-directed nanowire (T_{soi}=12nm) is higher than in 15 nm wide [100]-directed nanowire (T_{soi}=19nm). Structures of two compared devices are shown in Figure 4.4. As we explained in chapter 3, larger hole mobility in [110]-directed nanowires originates from (110) side surfaces with high hole mobility.

4.4 High Hole Mobility in (110)-oriented Silicon Nanowire pMOSFETs

Similar to the analysis in nanowire nMOSFETs (chapter 2 and 3), hole mobility characteristics in planar pMOSFETs can be used to study the hole mobility behaviors in nanowire pMOSFETs. Figure 4.6(a) shows the TEM image of multiple nanowires array and Figure 4.6(b) shows the single [110]-directed nanowire cross section. Figure 4.6 (c) illustrations schematic of fabricated nanowires on (110) SOI wafer and relative nanowire cross sections of different directions. In [100]-directed nanowire, four surrounded surfaces are identically (110) surface, therefore, the hole mobility in [100]-directed nanowires should agree with [100]/(110) universal curve and hole mobility degradations should be observed in narrow nanowires. However, in [110]-directed nanowires, top/bottom surfaces are (110) orientation with the highest hole mobility while the side surfaces are (100) orientation with low hole mobility. It is difficult to anticipate if the hole mobility in [100]-directed nanowires is higher than that in [100]-directed nanowires, but obvious hole mobility degradation should be observed in narrow [110]-directed nanowires due to the larger contribution from (100) side surfaces with low hole mobility.

Figure 4.6 shows I_d-V_g and C_{gc}-V_g characteristics of [100]- nanowire pMOSFETs with 800 nanowires of W_{nw}=18nm, L_{nw}=1μm and 1.2μm. Thanks to the GAA structure, subthreshold characteristics illustrate ideal performance (Figure 4.7). The extracted S.S. values agree well with those in (100) nanowires pMOSFETs. As shown in Figure 4.8 (a), hole mobility in [100]- nanowires of 55nm W_{nw} is as high as that in UTB pMOSFETs and agrees well with bulk universal curve [1]. And, surprisingly, [100]-directed nanowires of W_{nw}=18nm also shows high mobility which approaches to the bulk universal curve at high N_{inv}. Figure 4.8 (b) shows measured hole mobility of [110]-directed nanowires, which is much higher than [100]-directed nanowires. At high inversion density N_{inv} =1x10^{13} cm^{-2}, hole mobility of [110]-directed nanowires (W_{nw}=25nm) is impressively 2.4 times higher than that of (100) planar universal value [1]. Summarizing these data in Figure 4.8, it is concluded that [110] is the optimum channel direction for (110) nanowire pMOSFETs.

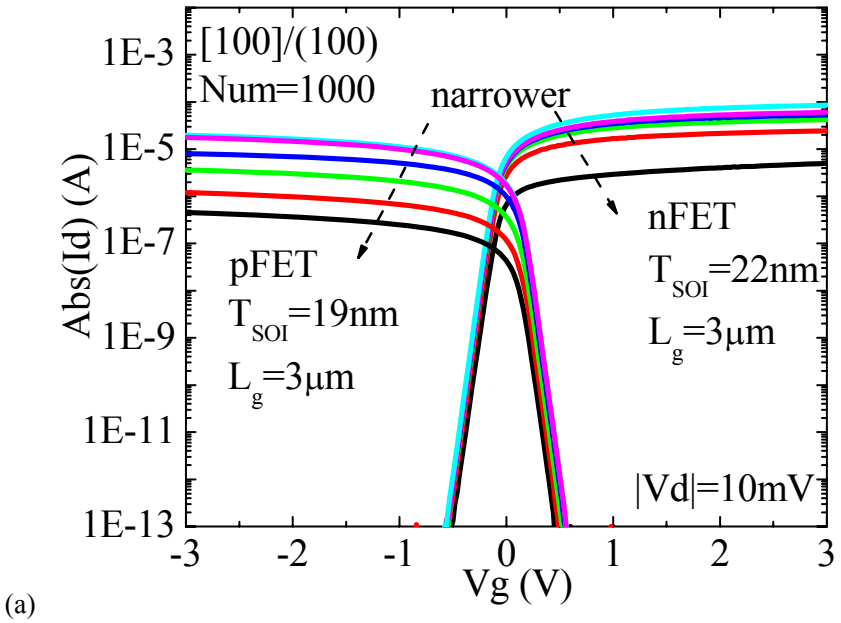
In [100]-directed nanowire, four surrounded surfaces are totally (110) surface (Figure 4.6(c)), that is why the hole mobility in [100]-directed nanowires agree well with [100]/(110) universal curve and shows low degradation even for 18nm-wide nanowires. However, in [110]-directed nanowires, observed hole mobility characteristics are out of the expectation. In general, larger contribution from side surfaces with low carrier mobility will decrease the average mobility in nanowires, which has been proved in [110]-directed nanowire nMOSFETs on (100) SOI. However, this degradation in [110]-directed nanowire pMOSFETs turns to be surprisingly ignorable at higher N_{inv}, as shown in Figure 4.10. It is very impressive to achieve high hole mobility in 25nm-wide [110]-directed nanowires at high N_{inv}, which region is very important for future VLSI applications. The underlying mechanism originates from the anisotropic heavy hole effective mass resulted carrier re-distribution and re-population [15]. At high surface potential Fs, hole distribution will be no longer in the center and be much closer to the corner, accordingly, surface area loses its meanings and hole population to each surface plays a quite important role in the measured hole mobility characteristics. From calculated hole subbands in relation to the Fs, it is found that the energy difference of the lowest hold subband to (100) and (110) will increase at higher Fs. This indicates that the hole population to (110) surface will increase and dominate the average hole mobility in nanowires. In other words, at high Fs, contribution from (100) surface with low hole mobility can be ignored. However, the reason why we can not observe same phenomena in nanowire nMOSFETs is not clear and further investigations are necessary.

To investigate the observed high hole mobility in [110]-directed nanowires at high N_{inv}, measurements at low temperatures are performed. Figure 4.12 illustrates the measured I_d-V_g and extracted G_m-V_g characteristics of [100]-nanowire pMOSFETs from 40K~200K. Temperature dependences on G_{m_max} are illustrated in Figure 4.13,

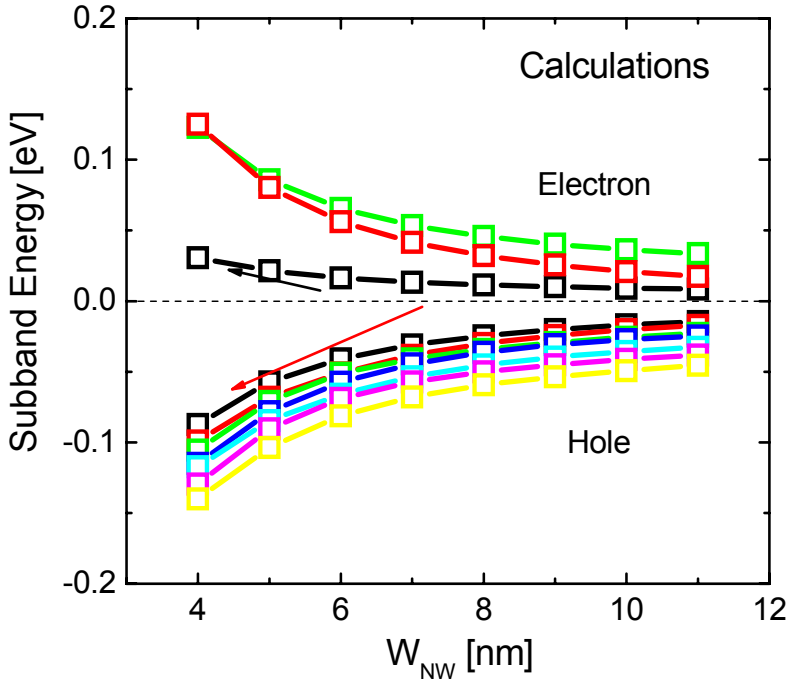
where 18nm wide [100]-directed nanowires and 25nm wide [110]-directed nanowires are compared. [110]-directed nanowires maintain the large G_{m_max} enhancement to [100]-nanowires from 200K to 40K. From the comparison of hole mobility between nanowires and UTB pMOSFETs at 40K (Figure 4.14), stronger roughness scattering in nanowires is confirmed [4]. Figure 4.15 shows the hole mobility ratio of [110]-directed nanowires to [100]-directed nanowires, where it is found that the mobility ratio is shifted to be lower from RT to 40K. This shift originates from the enhancement of phonon scattering mobility (μ_{ph}) at RT. Another important phenomenon should be noted here, that is, the mobility ratio increases with N_{inv} and the tendency has almost no temperature dependence. This can be explained by considering the m^*_{eff} modulation at high N_{inv}, which has been confirmed in (110) UTB pMOSFETs since m^*_{eff} in [110] direction will be much lighter than [100] direction as N_{inv} increases [16]. Based on six-band k.p. method [10], calculations on (110) surface hole subbands are performed (Figure 4.16). In addition to m^*_{eff} modulation at high N_{inv}, suppressed non-parabolicity in [110] direction at high N_{inv} will also result in the increasing mobility ratio. Considering the structure of nanowires on both (100) and (110) surfaces, as shown in Figure 4.17, hole mobility [110]-directed nanowires are much higher than that in [100]-directed nanowires; while considering the large side surface roughness, [110]/(110) is the best structure for nanowire pMOSFETs.

4.5 Summary

Systematic study of hole mobility in (100)- and (110)-oriented nanowire pMOSFETs has been described in this chapter. For (100)-oriented nanowire pMOSFETs, mobility degradation in narrower nanowires are observed, while [110]-directed nanowire pMOSFETs illustrates larger hole mobility than [100]-directed nanowire pMOSFETs in identical cross area. For (110)-oriented nanowire pMOSFETs, high hole mobility in [110]-directed nanowires is observed and shows ignorable mobility degradation from wide to narrow nanowires at high N_{inv}. Uniaxial tensile stress in nanowire pMOSFETs is also studied in this paper. It is concluded that [110] is the optimum channel direction for (110) nanowire pMOSFETs for high hole mobility.



(a)



(b)

Figure 4.1 (a) Measured I_d-V_g characteristics of nanowires of various widths, where the V_{th} shift in nanowire pMOSFETs is larger than V_{th} shift in nanowire nMOSFETs. (b) Calculations subband energy by using K.P method (hole subbands) and EMA method (electron subbands).

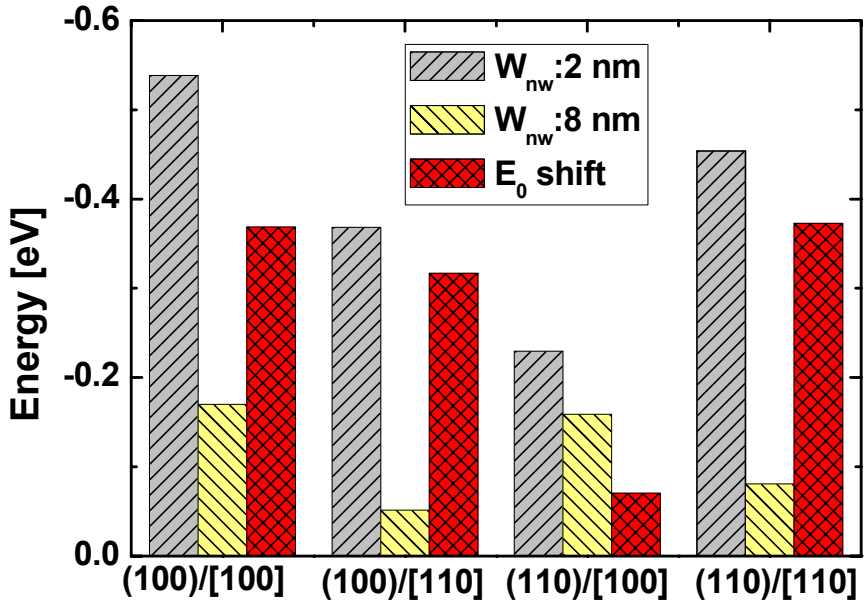


Figure 4.2 Calculated subband energy of the lowest subband and respective E_0 shift as nanowire width is reduced from 8nm to 2nm. Nanowires of both [100] and [110] directions, (100) and (110) orientations, are shown for comparison, where the smallest shift is observed in (110)/[100] nanowire.

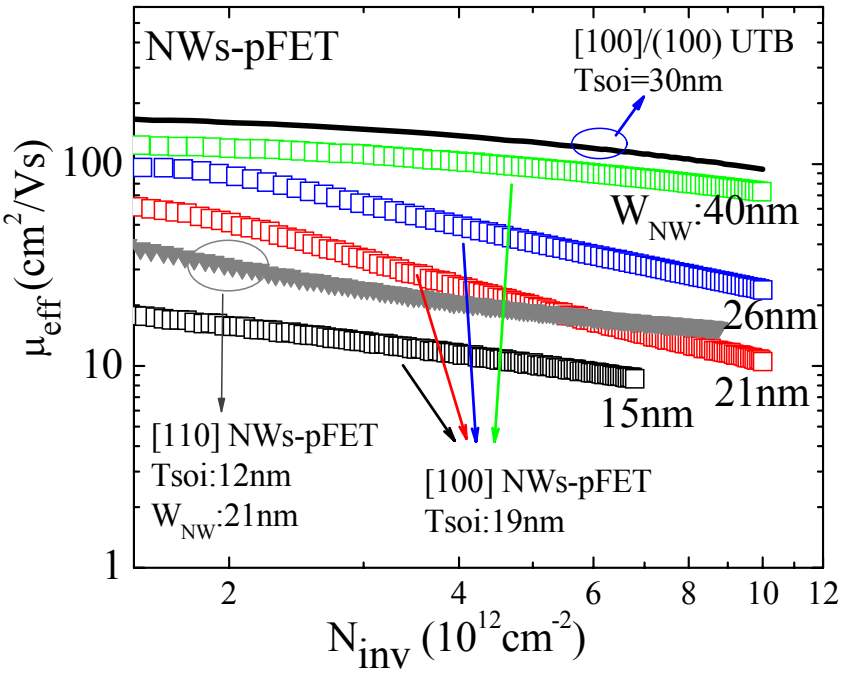


Figure 4.3 Hole mobility of [100] and [110]-directed nanowires. [110] is higher than [100] even in narrower nanowire with identical cross section area, where 15nm wide/ 19nm height [100]-nanowire and 21nm wide/ 12nm height [110]-nanowire are compared.

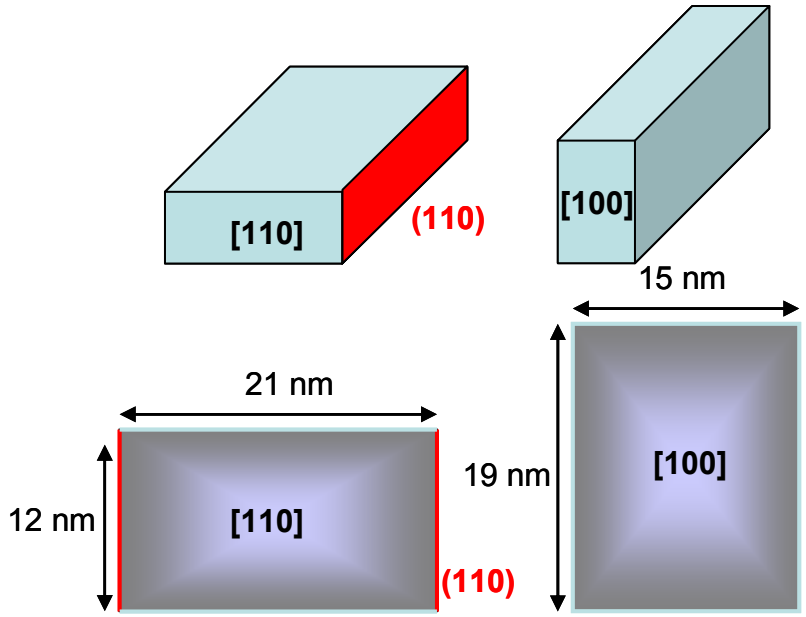


Figure 4.4 Quasi-identical cross section of [100]- and [110]-directed nanowires compared in Figure. 3. In [110]-directed nanowires, hole mobility is higher due to (110) side surface with high hole mobility.

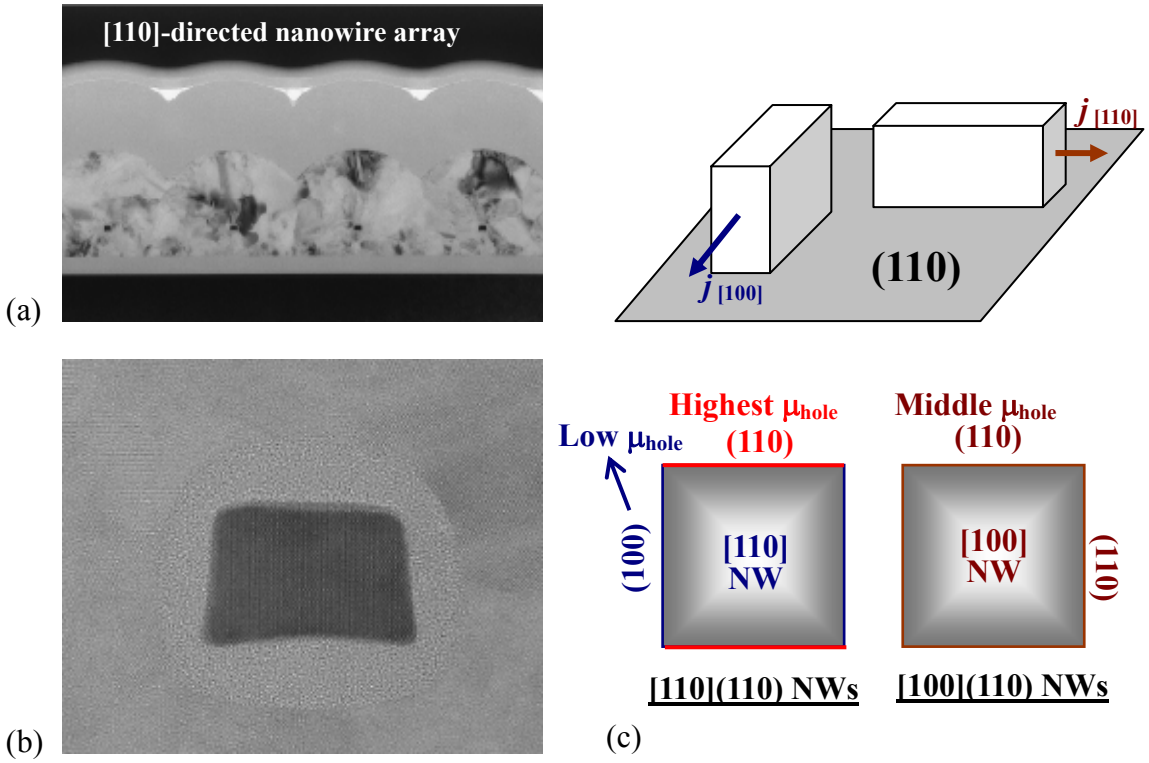


Figure 4.5 (a) TEM image of multiple [110]-directed nanowires array; (b) TEM image of one single [110]-directed nanowire of 18nm height and 25nm width; (c) Schematics of (100) nanowire pMOSFETs, showing that the orientation of side surfaces is different in [110]- and [100]- nanowires. In [110]-directed nanowires, (110) surface with highest hole mobility and (100) surface with low hole mobility are two competition factors; while in [100]-directed nanowires, four surrounded surface are totally (110) surface with middle hole mobility.

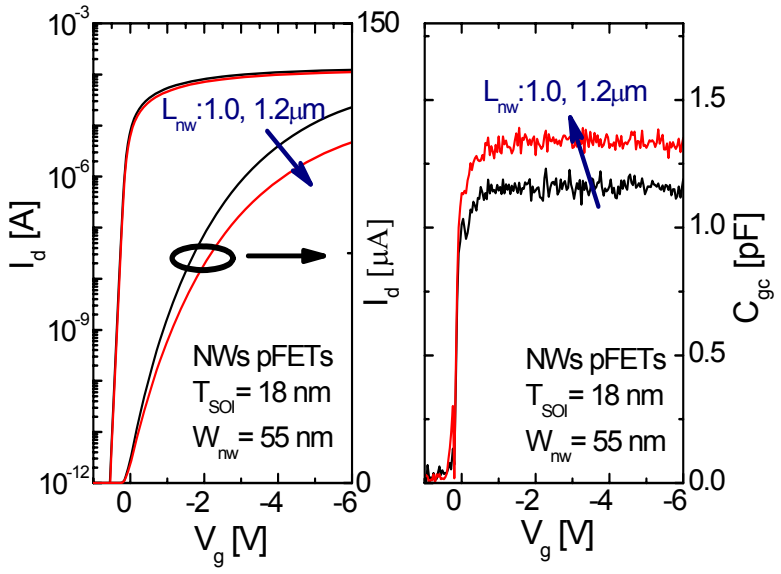


Figure 4.6 (a) I_d-V_g and (b) C_{gc}-V_g characteristics of [100]-directed nanowire pMOSFET on (110) SOI. Where, W_{nw}=55nm, L_{nw}=1/1.2um. SOI thickness is 18nm. Intrinsic nanowire capacitance can be obtained by comparing these two devices with different nanowire length but other identical structures.

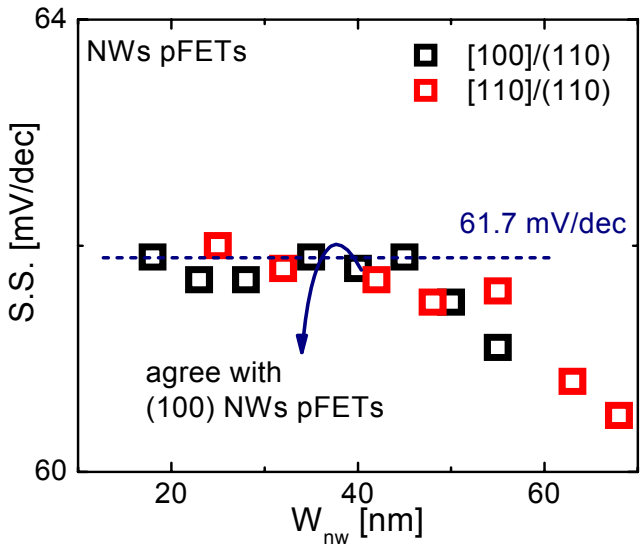
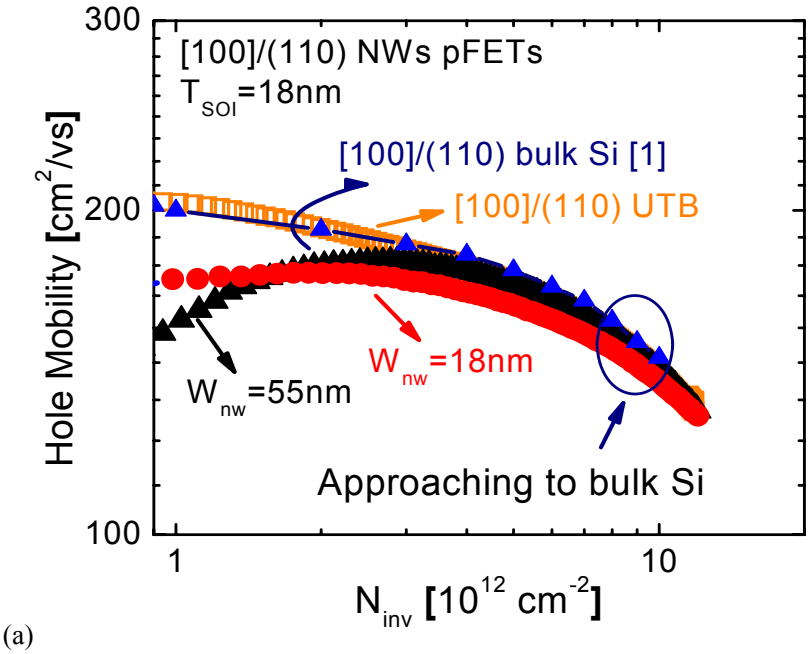
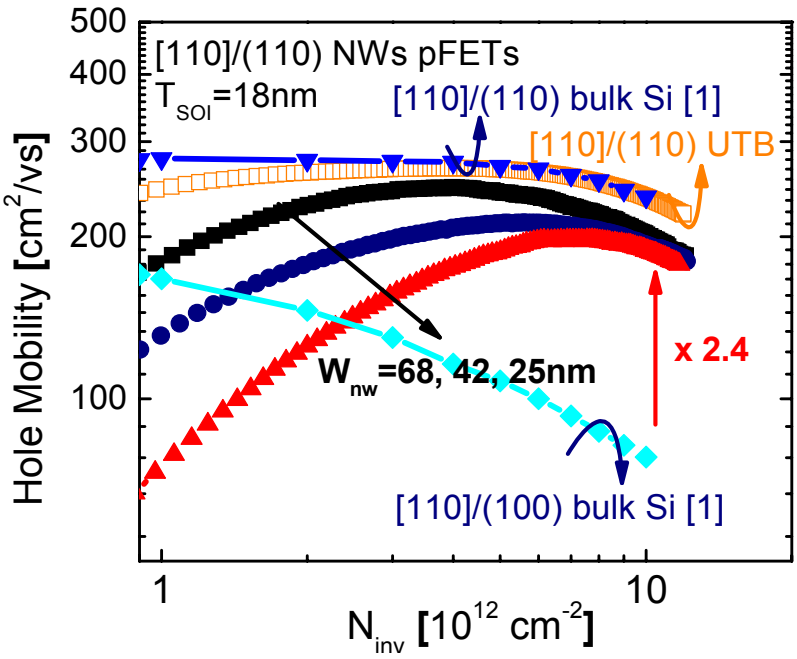


Figure 4.7 Extracted S.S. properties of both [110]- and [100]- directed nanowire pMOSFETs with W_{nw} ranging from 18nm to 68nm. The average value of 61.7 mV/dec agrees with that in (100)-oriented nanowire pMOSFETs.



(a)



(b)

Figure 4.8 Measured hole mobility in (a) [100]-directed nanowire pMOSFETs and (b) [110]-directed nanowires pMOSFETs. In [100]-directed nanowires, ignorable mobility degradation is confirmed from 55nm wide nanowire to 18nm wide nanowire, approaching to the bulk Si universal curve; while in [110]-directed nanowires, high hole mobility at high N_{inv} is obtained even in 25nm wide nanowire, indicating weak side surface contribution at high N_{inv}.

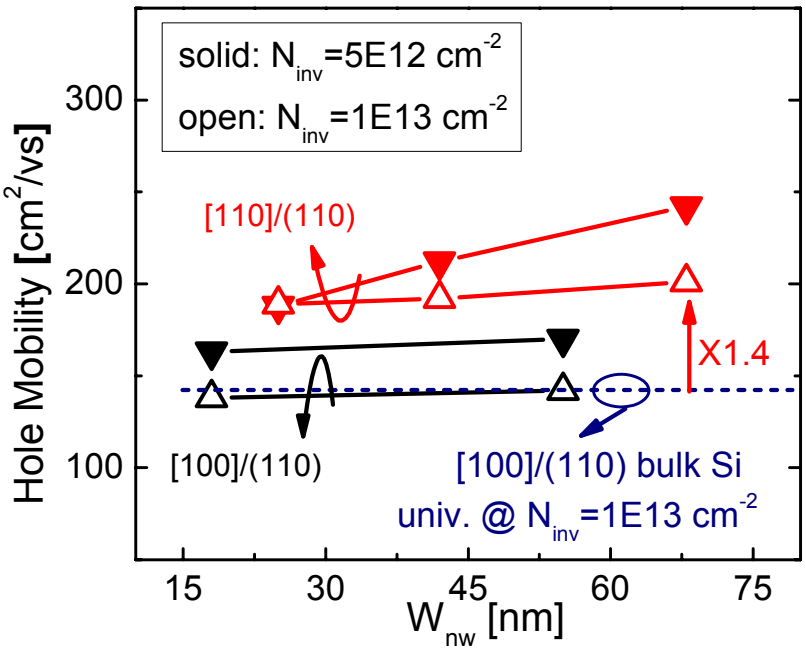


Figure 4.9 Comparisons between the hole mobility in nanowires of [100] and [110] directions. Even at high N_{inv} of 1E13 cm^{-2}, hole mobility in [110]-directed nanowire shows 1.4x enhancement from [100]/(110) universal data.

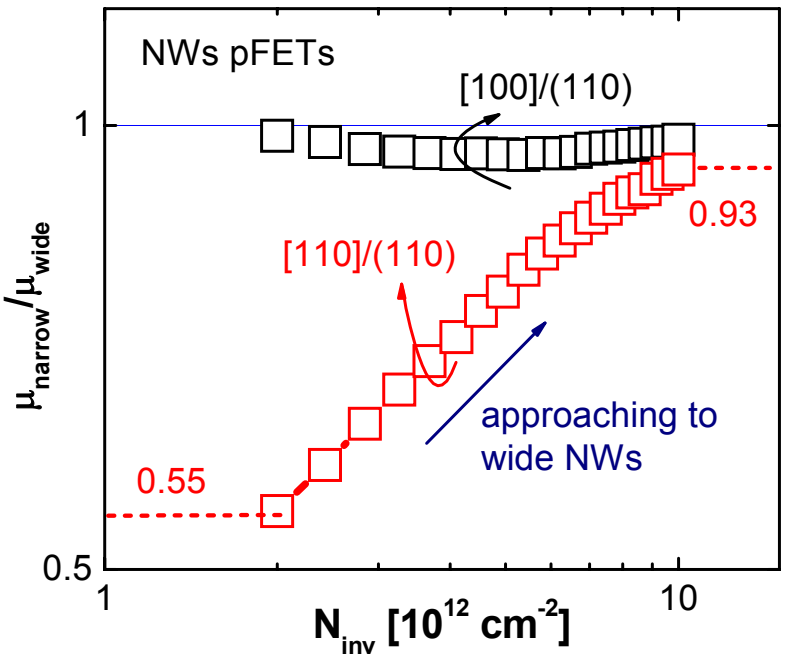
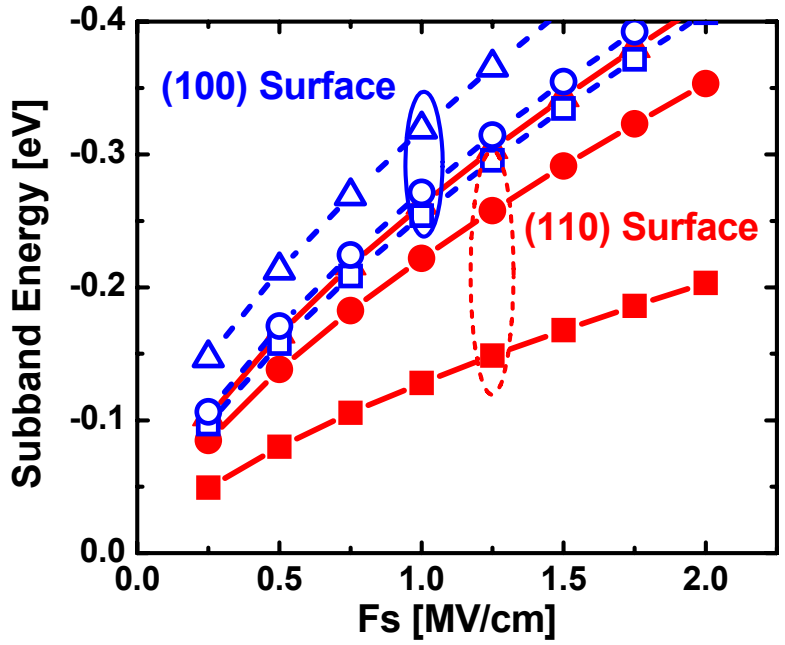
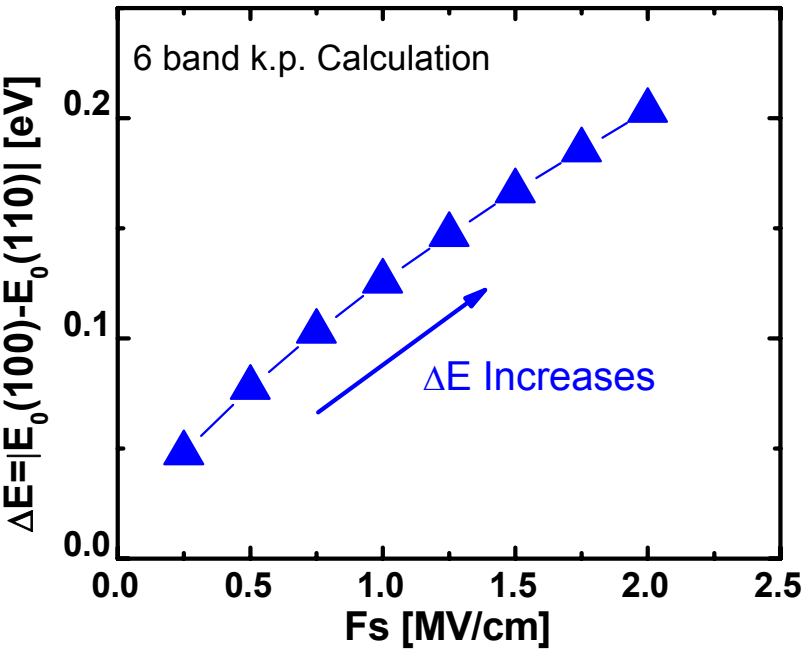


Figure 4.10 Hole mobility degradation from wide to narrow nanowires in (110) nanowire pMOSFETs. Obviously, ignorable mobility degradation in [100]-directed nanowires is confirmed. While large mobility degradation is observed in narrower [110]-directed nanowires, but this degradation is suppressed as increasing N_{inv}.



(a)



(b)

Figure 4.11 (a) Calculated lowest three hole subbands on (100) surface and (110) surface, respectively, in relation to the applied surface potential Fs; (b) Extracted energy difference ΔE between the lowest hole subband on (100) and (110) surface, indicating that ΔE will increase at higher Fs.

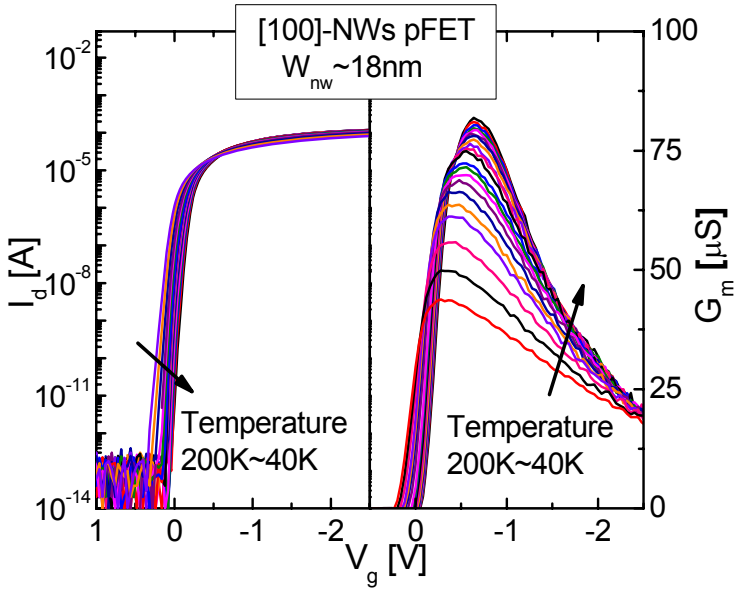


Figure 4.12 I_d-V_g and G_m-V_g characteristics of [100]-directed nanowire pMOSFETs of W_{nw}=18nm as lowering the temperature from 200K to 40K. Gm value increases as expected due to small parasitic resistance.

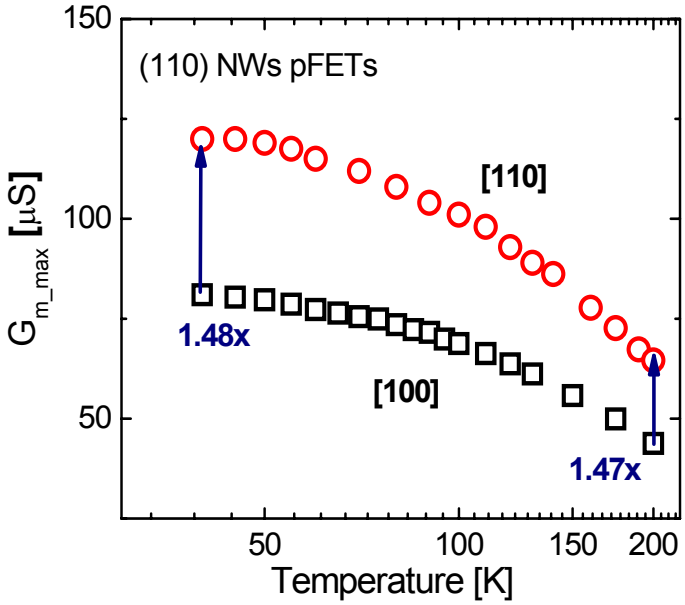


Figure 4.13 Extracted relationship between G_{m_max} and temperatures. Larger G_{m_max} in [110]- nanowire pMOSFET is observed in the whole measurement temperature range. This indicates that the observed mobility enhancement in [110]-directed nanowires over [100]-directed nanowires can not be explained by phonon scattering dominated mobility, but much more basic physical factor (effective mass).

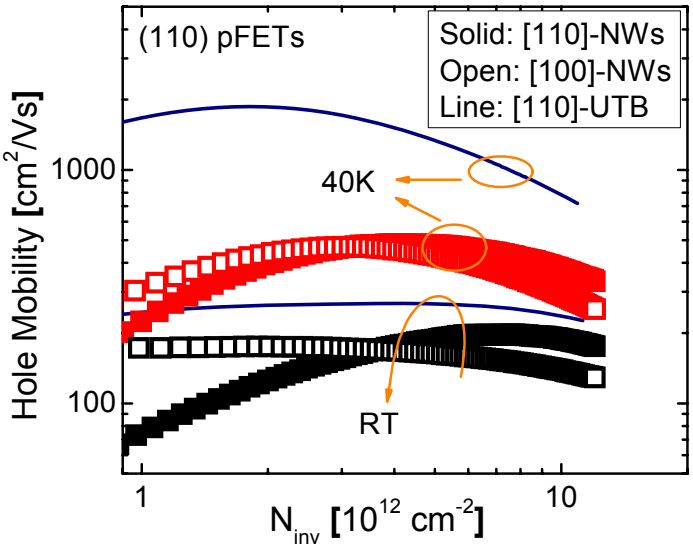


Figure 4.14 Hole mobility in (110) nanowire pMOSFETs at RT and 40K, as well as (110)/(110) UTB pMOSFET. From RT to 40K, hole mobility enhancement in UTB pMOSFET is much larger than nanowire pMOSFETs, which may originate from serious surface roughness in nanowire channels.

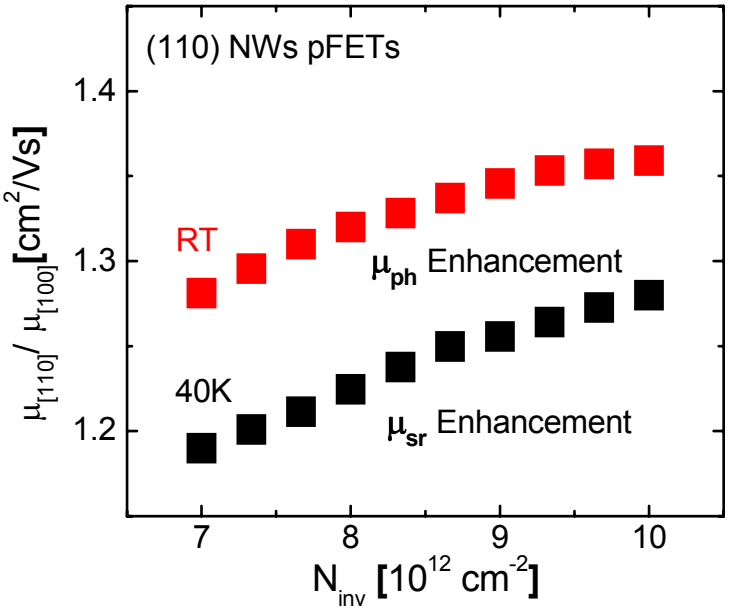


Figure 4.15 Hole mobility ratio of [110]- to [100]-directed nanowire pMOSFETs, and the ratio increases at higher $N_{inv.}$, no matter at RT or at 40K. Similar tendency indicates this mobility enhancement may be from conductive effective mass changing as a function of N_{inv}.

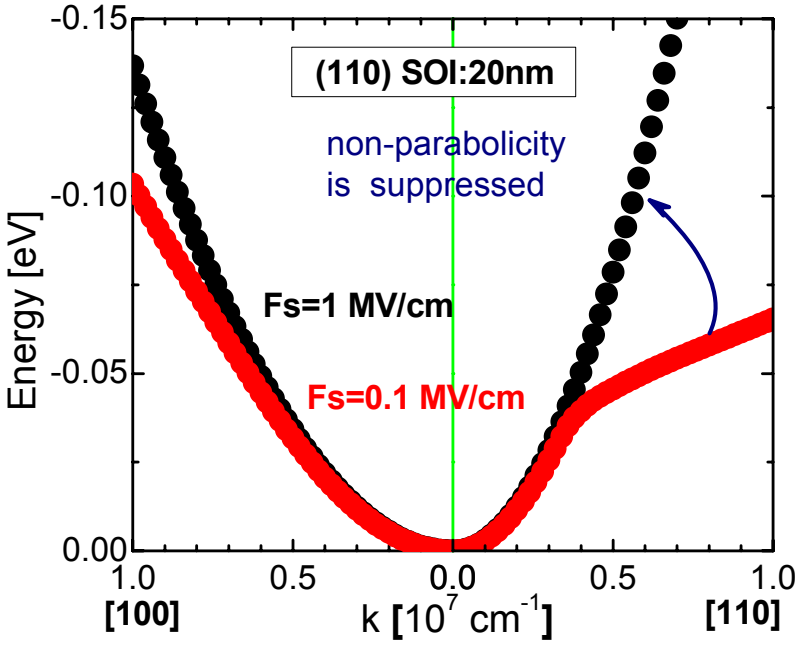


Figure 4.16 Calculated *E-K* relationship of the lowest hole subbands on (110) surface, the surface potentials (Fs) are set to be 0.1 MV/cm and 1 MV/cm. As increasing Fs from 0.1 to 1 MV/cm, non-parabolicity is obviously suppressed. As a result, mobility in [110]-directed nanowires at high Ninv can be recovered to some extend.

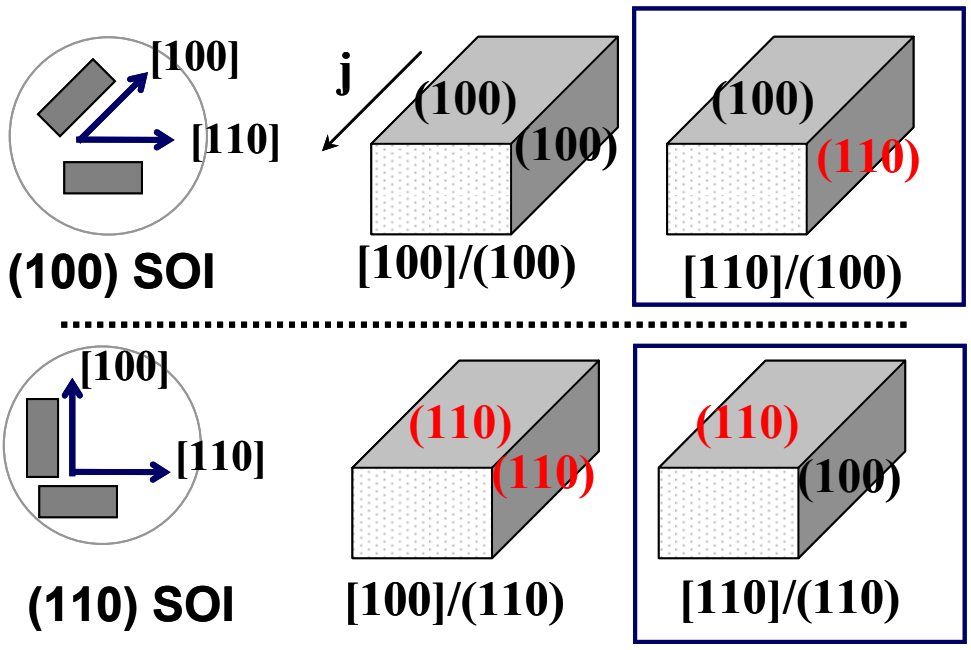


Figure 4.17 Device Structure of four type nanowire structures studied in this chapter. In a word, in narrower nanowires, [110]-directed nanowires is the optimum structure on both (110) and (100) surfaces.

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Chapter 5
Transport Performance Enhancement in Silicon Gate-All-Around Nanowire MOSFETs by Uniaxial Strain

5.1 Introduction

Nanowire-based FET is one important candidate in "More Moore" due to its high gate controllability and strong short channel effects (SCE) immunity. In chapter 3 and 4, we have described carrier mobility characteristics in Si nanowire MOSFETs. Now we have clear information on nanowire mobility characteristics, and it is time to consider how to modulate them and achieve mobility enhancements. Although there are calculation results that illustrate mobility enhancement in 5nm diameter nanowire [1], this kind of enhancement is still too small to get obvious performance enhancements. Also, one other theoretical work point out that replacing SiO_2 gate oxide with diamond insulator will obtain 2 times high mobility enhancement in 4 nm diameter Si nanowire [2]. Still, there is no experimental work on this. Actually, strain engineering method has been widely utilized in planar MOSFETs [3-7], UTB MOSFETs [8-12] and even FinFET MOSFETs [13-16]. In recent years, some important experimental works on strained nanowires have also been reported [17-19], indicating that strain engineering is still an effective method to achieve mobility enhancements in nanowire MOSFETs.

In this chapter, in order to elucidate strain effects on performance modulation in Si nanowire MOSFETs, uniaxial mechanical strain is applied to fabricated Si GAA nanowire MOSFETs on both (110) and (100) SOI wafer. Characteristics of strained nanowires are investigated and discussed, including the strain direction dependence, nanowire current direction dependence, and surface orientation dependence. These discussions are performed in both n-type and p-type nanowire MOSFETs. Relative calculations are also done for better understandings.

5.2 Device Structure and Measurement Setup

Figure 5.1(a) shows the 3-dimentional structure of fabricated GAA nanowire MOSFETs, where the schematic of applied strain are also shown for better understandings. Figure 5.1(b) illustrates the calculation method on applied mechanical stress value. Normally, there exist two methods to apply strain on devices, one is

process-induced strain, and the other one is mechanical stress by outside force, which is utilized in this work. By using different apparatus, we can apply tensile/compressive uniaxial strain on fabricated devices after they are polished to ~300um thickness. This method has been proved efficient in both UTB MOSFETs [8] and FinFETs [12], but seldom reported in nanowire MOSFETs [19].

5.3 Uniaxial Strain on Silicon nanowire nMOSFETs

Figure 5.2 shows the measured drain current modulation in (110)-oriented nanowire nMOSFETs by uniaxial tensile strain in both [110]- and [100]- directions. In Figure 5.2(b), the drain current enhancement and degradation in nanowire nMOSFETs of two directions are summarized. In [110]-directed nanowires, transverse strain effect is higher than longitude strain effect; while in [100]-directed nanowires, longitude strain effect is higher. In another word, strain effect by [100]-direction is larger than by [110]-direction. In pervious reported bulk nMOSFETs, it has already been confirmed that the effect of [100]-direction strain is larger than in [110]-direction strain, not only in [100]- but also in [110]-directed channels [9]. The underlying physical mechanism originates from the larger subband spacing modulation between 2-fold and 4-fold by [100]-directed strain than by [110]-directed strain. Furthermore, Id modulation in [110]-directed nanowires are higher than [100]-directed nanowires by uniaxial tensile strain at V_g = 3V. To explain this, mobility enhancement and degradation in [110]/[100] nanowires by longitude and transverse tensile strain is measured and shown in Figure 5.3. At low N_{inv}, mobility enhancement in [100]-directed nanowire is higher than in [110]-directed nanowire; while at high N_{inv}, mobility enhancement in [100]-directed nanowire turns to be lower than in [110]-directed nanowire. This is similar to the reported characteristics in FinFETs [13]. It is believed that the reduced conductivity mass *mc* of 2-fold valleys by [110] tensile strain contribute to this. Furthermore, because the occupancy of 2-fold valleys increases with N_{inv} due to band non-parabolicity [13], μ_{eff} and I_d enhancement in [110]-directed nanowires is maintained and even increases with N_{inv}. It is also found that the uniaxial strain is more efficient in narrower nanowires, as shown in Figure 5.2 (b), which is quite important for future VLSI design.

[100]-directed nanowires nMOSFETs on (100) SOI, as the optimum nanowire nMOSFETs structure, are also investigated. As shown in Figure 5.4, drain current increases by longitude tensile strain while decreases by transverse tensile strain, which is similar to the case of bulk nMOSFETs and originates from the mobility modulation at high inversion density.

5.4 Uniaxial Strain on Devices from Planar to Nanowire pMOSFETs

In this section, detail calculations on uniaxial strain effects from planar to nanowire pMOSFETs will be described. On the basis of spds* tight-binding (TB) method [20-21], the whole subband subband calculations can be done, as shown in Figure 5.5, where the subbands of heavy hole (HH), light hole (LH) and split-off hole (SH) are illustrated, respectively. However, TB method is quite complex and time-consuming. In the following work, calculations will be based on 6-band k.p. method [22-24].

Figure 5.6 shows calculation results in the bulk Si with/without applying uniaxial/biaxial strain. All results show that applying strain will enlarge the subband spacing, no matter biaxial strain or uniaxial strain. As to the effective mass m^*_{eff}, biaxial strain influence is small in both [110] and [001] directions; while uniaxial strain results in smaller m^*_{eff}, which means a lot for mobility enhancement. Furthermore, energy splitting between the lowest LH subband and HH subband (ΔE_0) are shown in Figure 5.6. From Figure 5.7(a), it is confirmed that, only >1Gpa strain is applied, ΔE_0 is larger than 60 meV (The intervalley scattering will be suppressed effectively is the energy spacing is higher than the optical energy value of 60 meV). While from Figure 5.7(b), it is found that, as increasing surface potential Fs, ΔE_0 increases by uniaxial strain but decrease by biaxial strain. To confirm the efficiency of [110]-directed uniaxial strain, whole band calculations are shown in Figure 5.8, comparing hole subbands structure w/o strain, with [110]-directed uniaxial compressive strain and with 1% biaxial tensile strain. These results show that uniaxial compressive strain results lighter effective mass along [110]-direction and higher carrier population along [-110]-direction, which will contribute to hole mobility enhancement in [110]-directed channel [25]. In Figure 5.9, when same tensile strain of various directions is applied on (100)- and (110)-oriented surface, it is found that (100) surface is much more sensitive to uniaxial strain. In summary, uniaxial strain is much better than biaxial strain in view of large mobility enhancements at low strain and high Fs, especially on (100)-oriented surface.

Above discussions can be used to explain experimental phenomenon in planar pMOSFETs, and also can be used to explain wide/high nanowires to some extend, as we discussed in chapter 3 and 4. But in narrower nanowires, or nanowire with small cross area, things will change due to strong quantum confinement. As shown in Figure 5.10, as the width/height of rectangular nanowire changing from 3nm to 2nm, strain effects are almost ignorable.

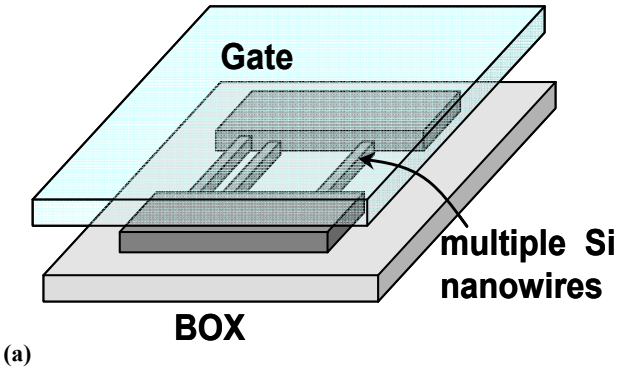
5.5 Uniaxial Strain on (110)-oriented Silicon nanowire pMOSFETs

Similar to nanowire nMOSFETs, strain effects on nanowire pMOSFETs are studied by applying 300MPa

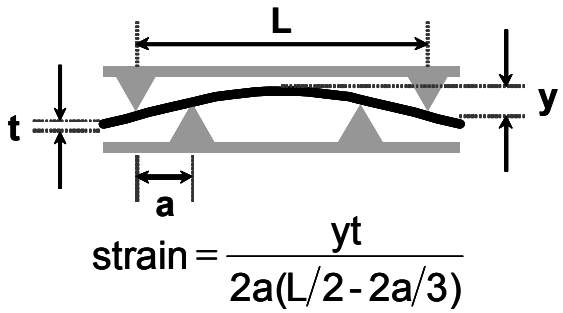
uniaxial tensile strain in both [110] and [100] directions. At high N_{inv}, (110) nanowire pMOSFETs of two directions show similar behaviors with UTB pMOSFETs, that is, [110]-strain is much more effective than [100]-strain [14]. To be particular, for [110]-directed uniaxial tensile strain, [110]-directed nanowires shows highest mobility modulation at high N_{inv}. As for [100]-directed uniaxial tensile strain, although the hole mobility enhancement in nanowires is observed at high Ninv, clear mobility degradations exist at low N_{inv}, indicating that nanowires have different piezoresistances properties from planar MOSFETs and FinFETs [3, 13-14]. Based on the calculated E-K diagram at high surface potential of 1MV/cm, as shown in Figure 5.9, (100) surface is more sensitive to the applied strain obviously, especially to [110]-strain [7]. In other words, large mobility modulation can be obtained in [110]-directed nanowire due to its (100) side surfaces. So, hole mobility enhancement is expected if [110] uniaxial compressive strain is applied to [110]-directed nanowires pMOSFETs.

5.6 Summary

In this chapter, systematic investigations on uniaxial strain effects on nanowire MOSFETs have been described, experimentally and theoretically. In nanowire nMOSFETs with uniaxial strain, observed mobility modulation and drive current modulation can be well explained by considering wide/high nanowires as separate planar MOSFETs. To be particular, in view of drive current enhancement in nanowire nMOSFETs, a) [110]-directed strain is much more efficient than [100]-directed strain; b) Uniaxial strain influence on [110]-directed nanowires is larger than on [100]-directed nanowires. As to the hole mobility, although mobility characteristics in strained nanowires are not agree with planar MOSFETs at low N_{inv}, it is still confirmed that a) [110]-directed uniaxial strain is effective than [100]-directed strain; b) [110]/(110) nanowires a little more sensitive to applied strain than [100]/(110) nanowires do due to (100)-oriented side surface with higher strain sensitivity.

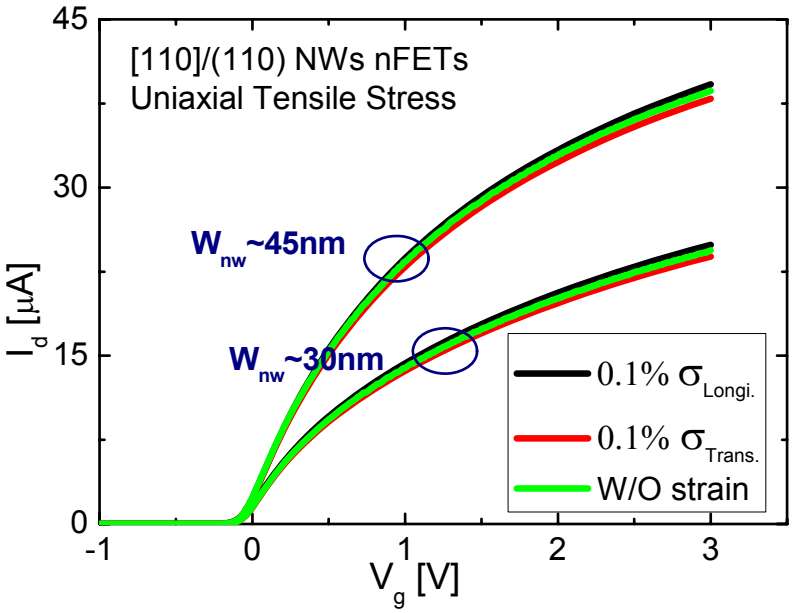


(a)

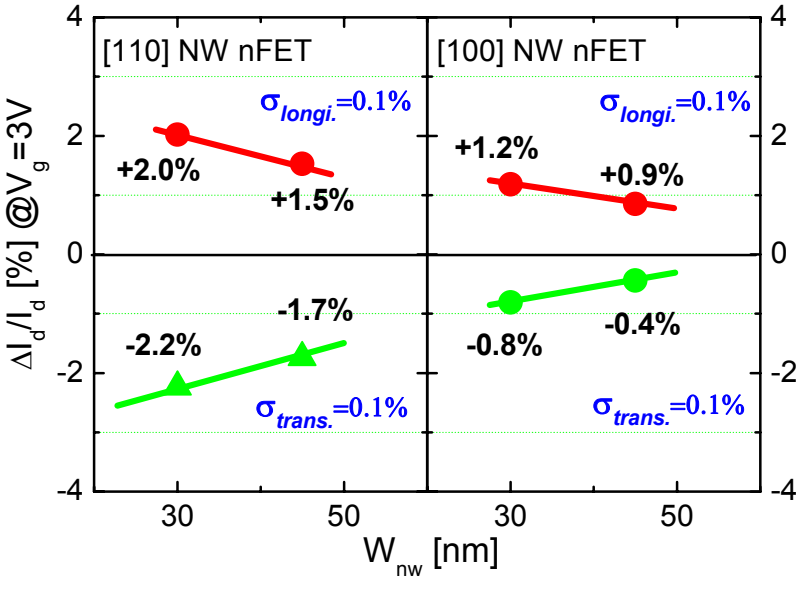


(b)

Figure 5.1 (a) Schematic of strained nanowires MOSFETs; (b) Strain apparatus utilized in this study. The equation shown here is used to calculated the strain value, "t" means the chip thickness. In this work, "t" are 250~300μm.



(a)



(b)

Figure 5.2 (a) Measured I_d-V_g characteristics of [110]/(110) nanowire nMOSFETs by longitude/transverse tensile stain; (b) Summarized I_d modulation with respect to I_d w/o strain in (100)-oriented nanowire nMOSFETs, at V_g=3V. Strain effects are much more obvious in [110]-directed nanowires.

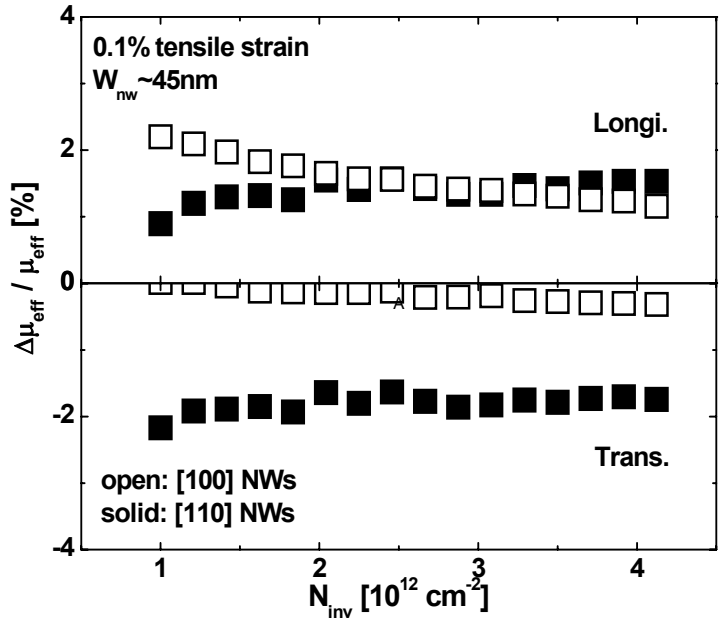


Figure 5.3 $\Delta\mu_{eff}/\mu_{eff}$ vs N_{inv} characteristics as longitudinal and transverse tensile strain is applied on (110)-oriented nanowire nMOSFETs, nanowire width W_{nw}= 45nm.

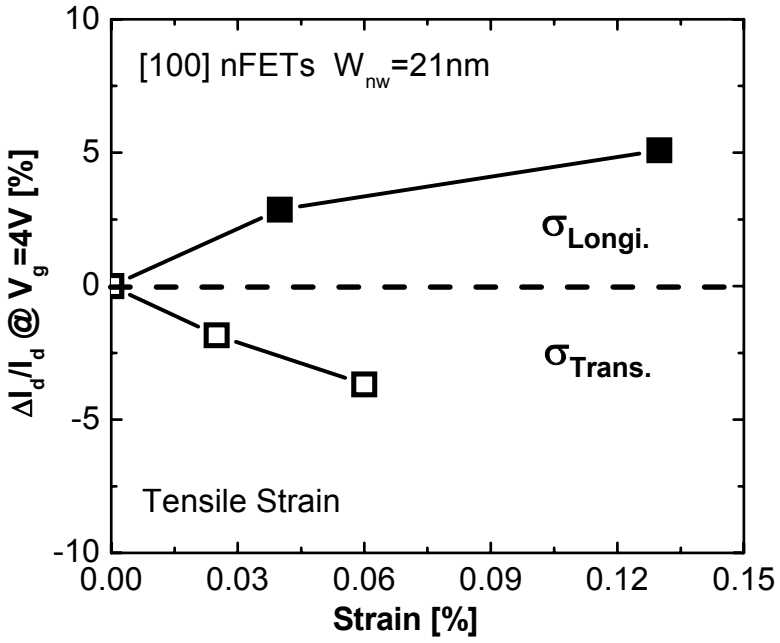
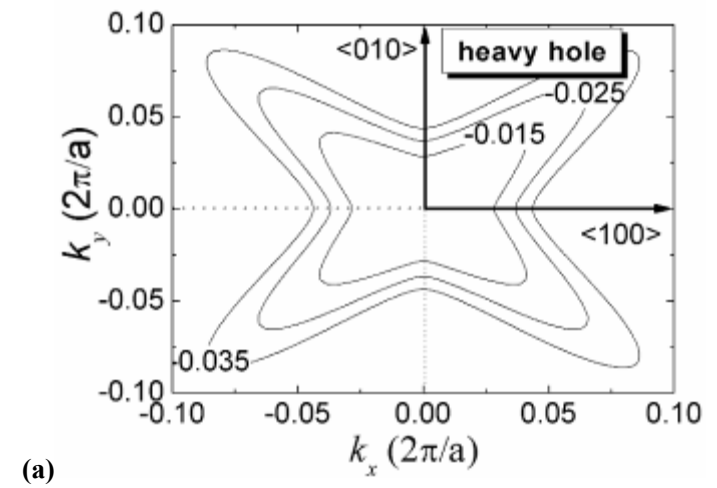
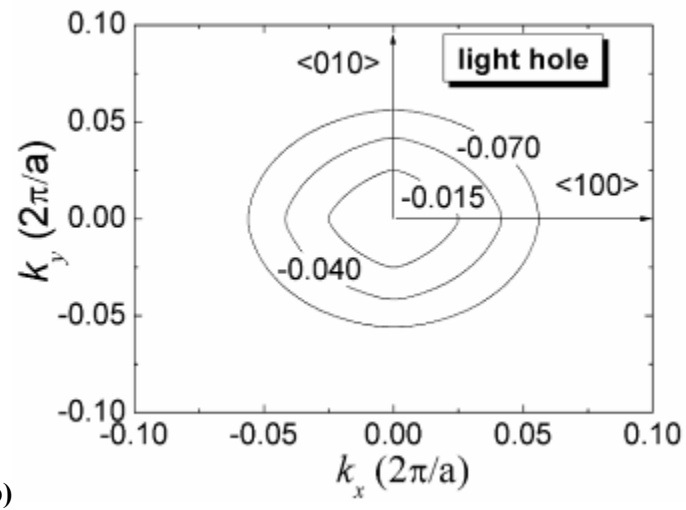


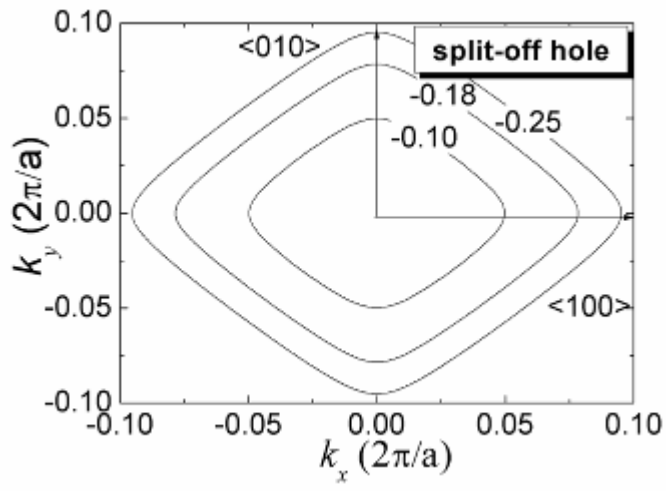
Figure 5.4 Drain current modulation $\Delta I_d/I_d$ as a function of applied uniaxial tensile strain in [100]/(100) nanowires nMOSFETs. Larger strain results in larger current modulation. Here, W_{nw}=21nm.



(a)



(b)



(c)

Figure 5.5 Calculated *E-K* diagram equivalent energy lines in bulk Si, for (a) heavy hole (HH); (b) light hole (LH); (c) split-off hole (SH). Here, the surface is (100)-oriented and kz=0.

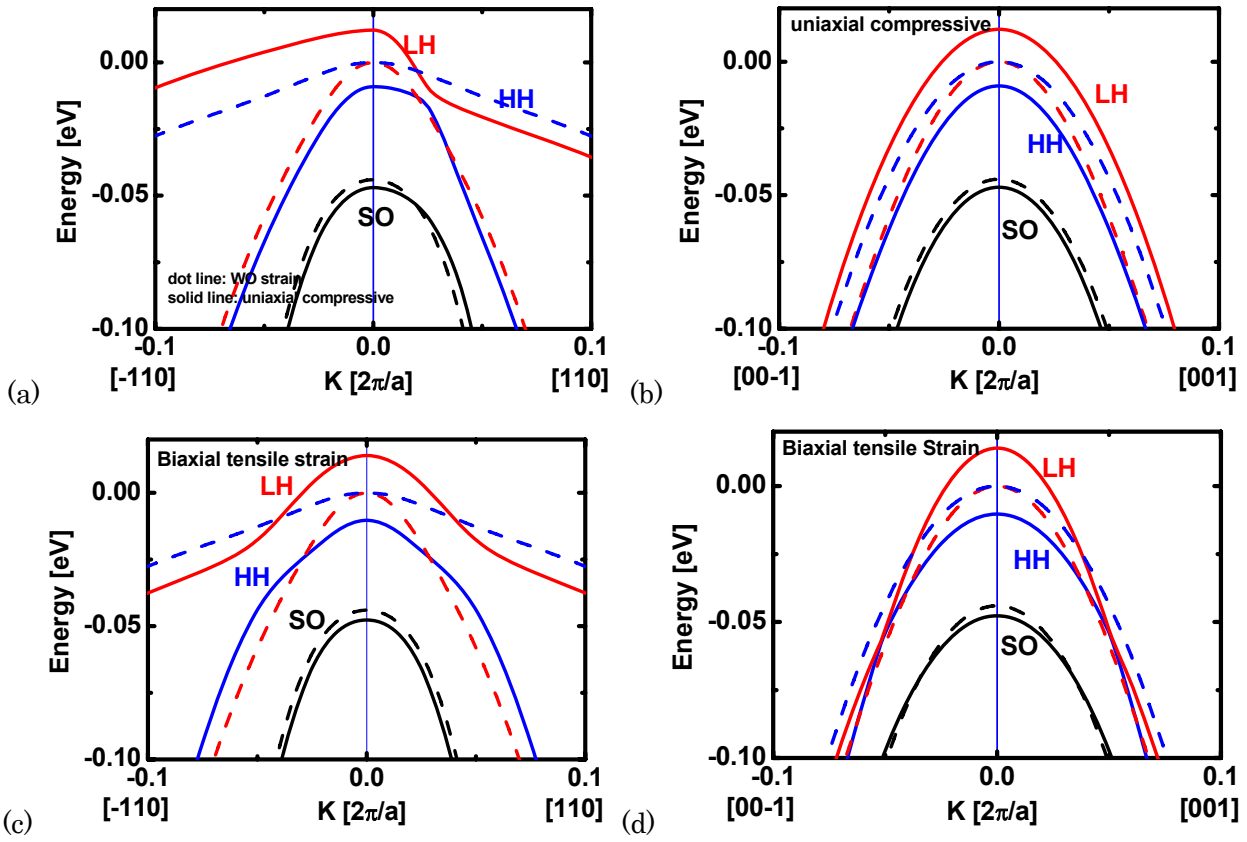
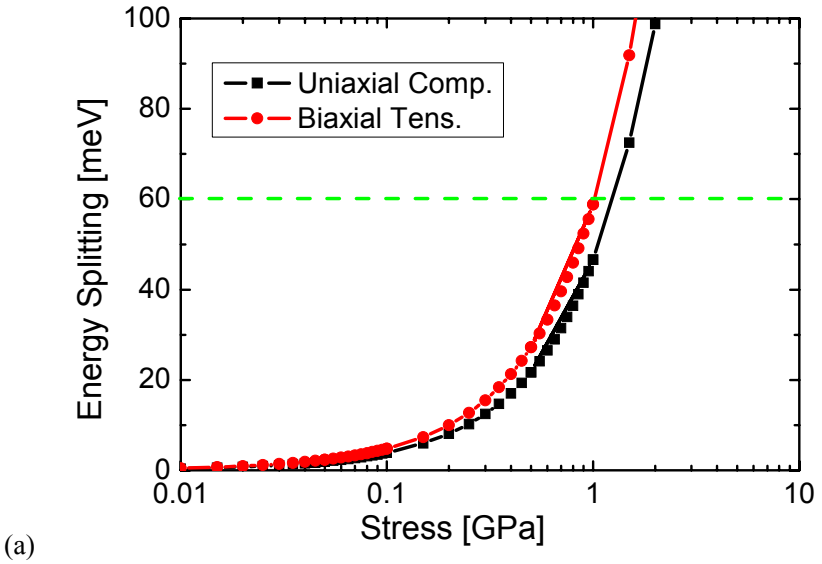
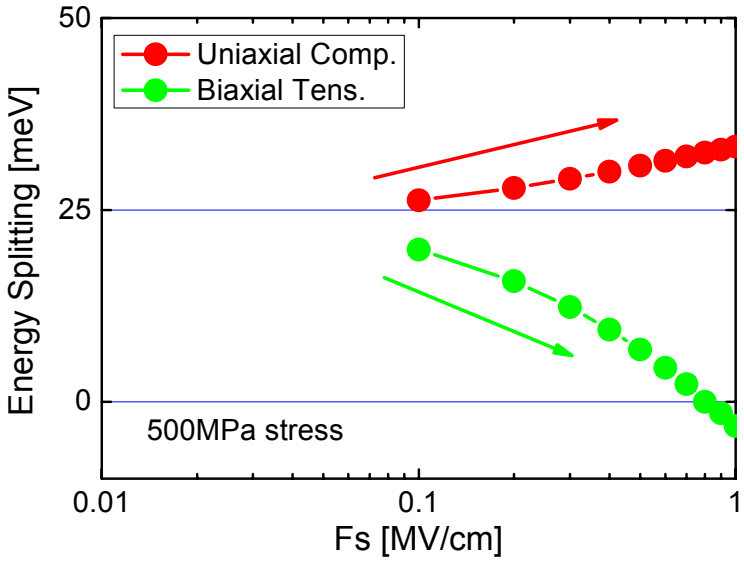


Figure 5.6 Calculated hole subband structures with (a)/(b) [110]-uniaxial compressive strain and (c)/(d) [110]-biaxial tensile strain. In the left Figures (a)/(c), vector k are along [110]-direction; while the right Figures (b)/(d), k are along with [001]-direction.



(a)



(b)

Figure 5.7 Energy splitting ΔE_0 between the lowest LH and HH subbands ($\Delta E_0 = E_0(LH) - E_0(HH)$) as uniaxial and biaxial strain are applied in bulk Si: (a) ΔE_0 as a function of applied strain value; (b) ΔE_0 as a function of applied vertical electric field.

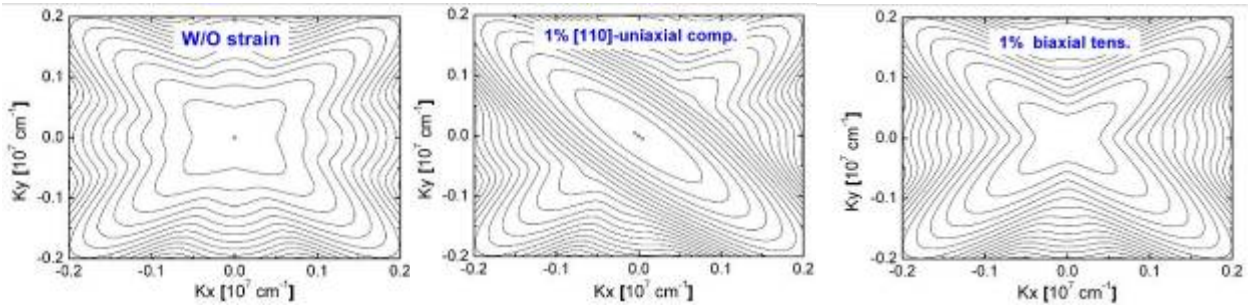


Figure 5.8 First hole subband energy contours (a) without strain; (b) with 1% [110]-directed uniaxial compressive strain; (c) 1% biaxial tensile strain, with an effective field of 1 MV/cm. These results show that uniaxial compressive strain results lighter effective mass along [110]-direction and higher carrier population along [-110]-direction, which will contribute to hole mobility enhancement in [110]-directed channel.

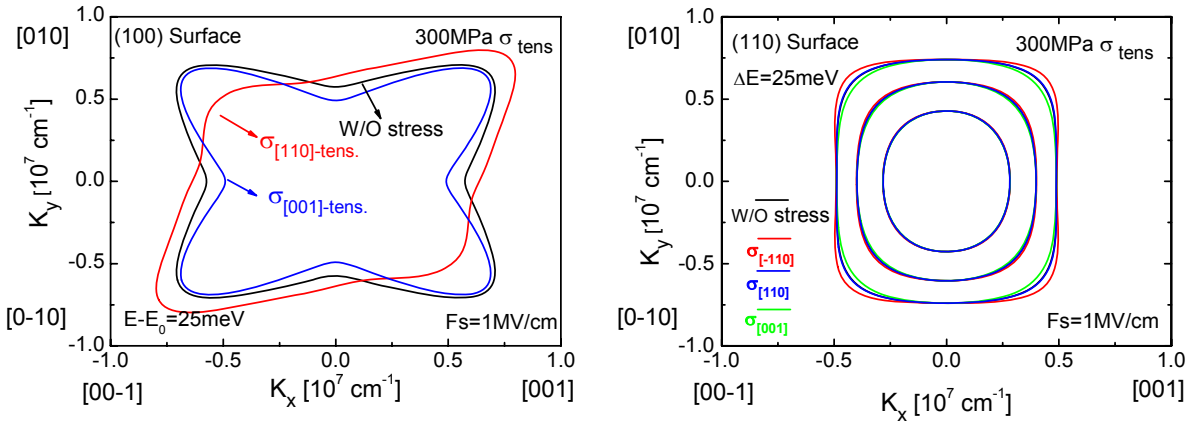


Figure 5.9 Calculated *E-K* diagram for the highest hole subband at Fs=1MV/cm, on both (a) (110) and (b) (100) surfaces, with and without uniaxial tensile strain. (100) surface is much more sensitive to the applied strain.

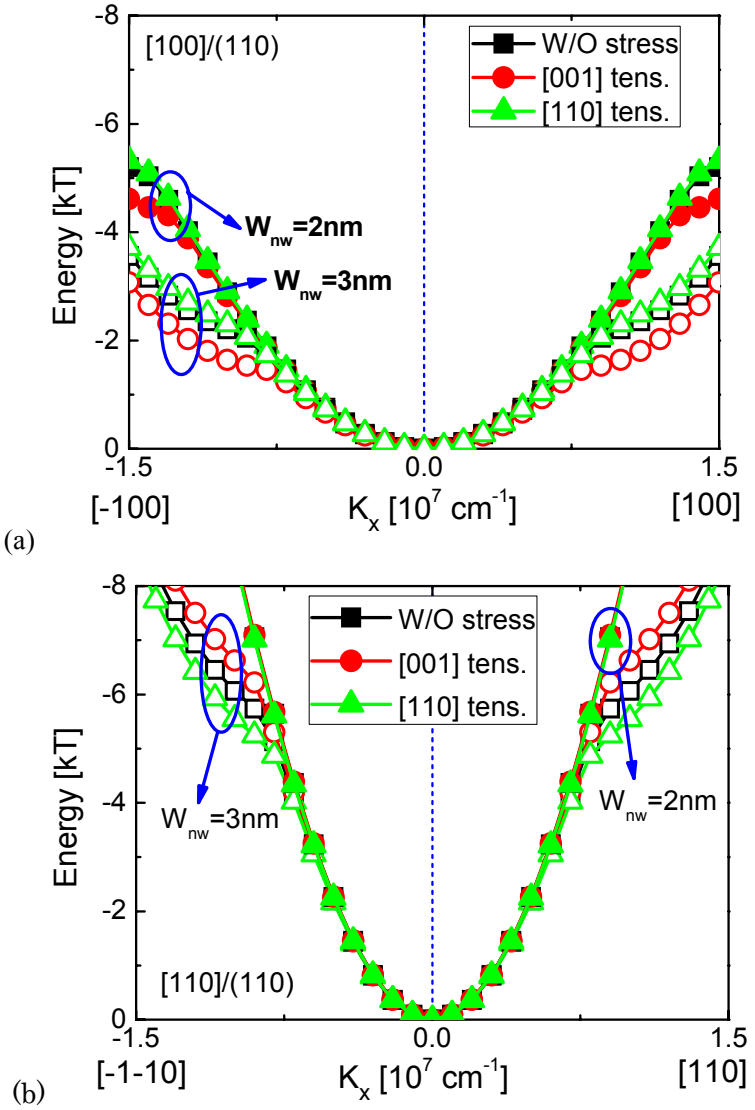


Figure 5.10 *E-K* relationships in (a) [100]- and (b) [110]-directed nanowires with square cross sections on (110) SOI, with and without uniaxial tensile strain. Uniaxial tensile strain effects are ignorable in these ultra-small nanowires.

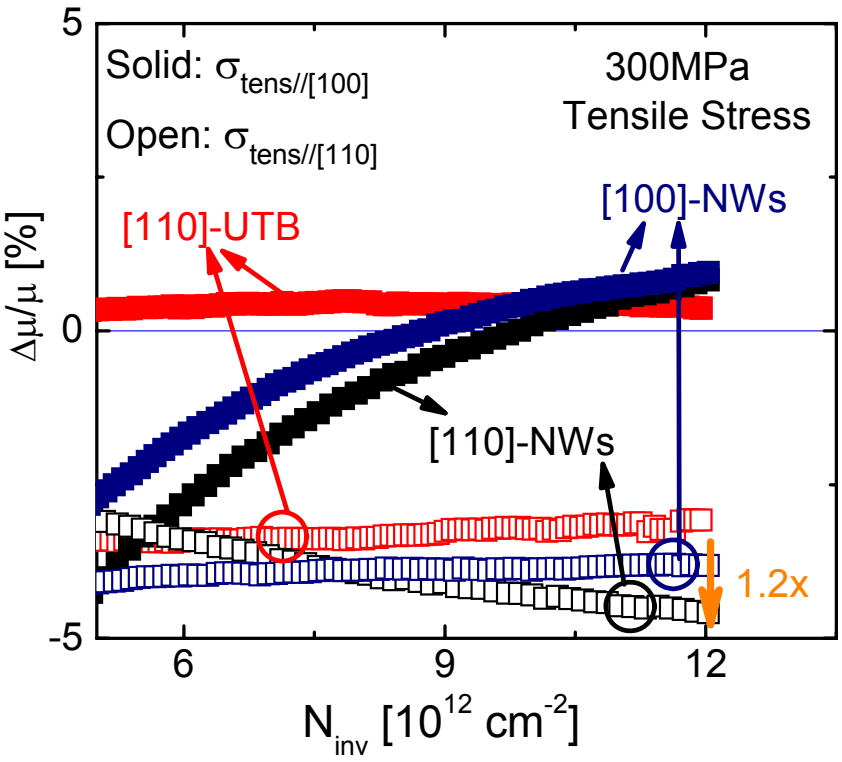


Figure 5.11 Hole mobility modulations when ~300MPa uniaxial tensile strain is applied in [110] and [100] directions. [110]-directed strain is much more effective than [100]-directed strain.

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Chapter 6
Conclusions

In this dissertation, carrier mobility properties of silicon multiple gate-all-around (GAA) nanowire MOSFETs are measured, characterized and discussed, aiming at further understanding and enhancing transport performance of nanowire-based devices. By changing the surface orientation and channel direction, structure optimization of nanowire MOSFETs is discussed and summarized, where the uniaxial strain effects are also included. The main results obtained in the dissertation are summarized as follows.

In Chapter 2, structure design and fabrication process of multiple GAA nanowire MOSFETs are described. Double L_m method is introduced and combined with split CV method for accurate mobility measurements, comparing two identical nanowire MOSFETs of different nanowire length. Simultaneously, double exposure method with EB and photo lithography is introduced for uniform nanowires and reliable comparisons. Based on this device design and measurement method, electron mobility in [100]/(100) nanowire nMOSFETs is extracted and shows good agreement with bulk universal curve.

In chapter 3, electron mobility in [100]- and [110]-directed NWs on both (100)- and (110)-oriented SOI are characterized and discussed. The main conclusion is that side surface orientation plays a key role in nanowire mobility. It is also found that, on (100) SOI, mobility of (100)-oriented nanowires decreases monotonically as narrowing nanowire width due to serious process-induced roughness in narrower nanowires; while on (110) SOI, electron mobility in [110]-directed nanowires approach to and is even higher than [100]-directed nanowires due to the increasing contribution from (100) side wall with high electron mobility. Furthermore, measurements on [100]/(100) NWs at low temperatures were performed. Anomalous “double peak” phenomenon is observed in nanowire mobility behaviors at 100K and shows clear dependence on W_{nw}, which can be explained by the serious surface roughness scattering and coulomb scattering in narrower nanowires.

In chapter 4, investigations of hole mobility in (100)- and (110)-oriented nanowire pMOSFETs has been described. For (100)-oriented nanowire pMOSFETs, mobility degradation in narrower nanowires are observed; while for (110)-oriented nanowire pMOSFETs, hole mobility in [100]-directed nanowires agrees well with universal curve in (110)/[100] planar pMOSFETs, and much higher hole mobility in [110]-directed nanowires is observed and shows ignorable mobility degradation from wide to narrow nanowires at high N_{inv}.

In chapter 5, investigations on uniaxial strain effects on nanowire MOSFETs are performed, experimentally and theoretically. In nanowire nMOSFETs with uniaxial strain, observed mobility modulation and drive current

modulation agree with those in planar MOSFETs and FinFETs. To be particular, for drive current enhancement, a) [110]-directed stress is much more efficient than [100]-directed stress; b) Uniaxial stress influence on [110]-directed nanowires is larger than on [100]-directed nanowires. As to the hole mobility, it is confirmed that a) [110]-directed uniaxial stress is effective than [100]-directed stress; b) [110]/(110) nanowires a little more sensitive to applied stress than [100]/(110) nanowires do due to (100)-oriented side surface with higher stress sensitivity.

In conclusion, the results obtained in this dissertation show important information on carrier mobility characteristics in Si nanowire MOSFETs, which are promising for investigations on mobility enhancement in Si nanowire based devices in future VLSI system.

Appendix
Fabrication Process Flow of Multiple Silicon Gate-All-Around Nanowire MOSFETs

Table 1. Flow and detailed conditions of the fabrication process of multiple Silicon gate-all-around nanowire MOSFETs. The thickness of SOI and other layers were determined by ellipsometry. Nanowire width and length were determined by SEM observations.

Step		Condition
Sample preparation	Dicing	6 or 8 inch UNIBOND SOI wafer (p-type, (100), (110)) → 2 cm × 1.5 cm
	Cleaning 1	Buffered HF (BHF) 15 sec SC1 $NH_4OH : H_2O_2 : H_2O = 1 : 1 : 6$, 75 ~ 85 degC, 10 min BHF 15 sec SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
	Cleaning 2	Numbering BHF 15 sec SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
SOI thinning	Cleaning	$HF : H_2O = 1 : 100$, 90 sec SPM H2O2 : H2SO4 = 1 : 3, 110 ~ 130 degC, 10 min HF : H2O = 1 : 100, 90 sec
	SOI thinning	Dry oxidation 1000/900 degC, 10 ~ 25 min
	Oxide removal	BHF 2 min
Mask oxidation	Cleaning	$HF : H_2O = 1 : 100$, 90 sec SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min $HF : H_2O = 1 : 100$, 90 sec
	Mask oxidation	Dry oxidation 900 degC, 20 min
Area lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec
	Pre-baking	100 degC, 10 min
	Exposure	DWL 200
	Development	NMD-3 (TMAH 2.38 %) 60 sec
	Post-baking	100 degC, 15 min
Area etching	Oxide removal	BHF 25~35 sec
	Helicon RIE	Step 2 : 5 sec, Step 3 : 20 ~ 35 sec, Step 4 : 0 sec
	BOX removal	BHF 2 min-4min30sec
	Resist removal	Acetone SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
Mark lithography	Spin coating	Az 1500 (38cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec

	Pre-baking	100 degC, 10 min
	Exposure	DWL 200
	Development	NMD-3 (TMAH 2.38 %) 60 sec
	Post-baking	100 degC, 15 min
Mark etching	Helicon RIE	Step 2 : 10 sec, Step 3 : 405 sec, Step 4 : 0 sec
	Resist removal	Acetone SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
Mesa lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec
	Pre-baking	100 degC, 10 min
	Exposure	DWL 200
	Development	NMD-3 (TMAH 2.38 %) 60 sec
	Post-baking	100 degC, 15 min
Mesa etching	Mesa Mask	BHF 25 sec
	Resist removal	Acetone SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
EB lithography	Spin coating	HSQ (FOx-12) 4000 rpm, 40 sec
	Pre-baking	120 degC, 2 min
	Exposure	Beam current 120 pA, Acceleration voltage 50 keV Area dose 690 ~ 750 mC/cm^2 (for wire channel) Area dose 330 mC/cm^2 (for wire bar)
	Development	NMD-3 (TMAH 2.38 %) 60 sec
Channel and mesa RIE	Helicon RIE	Step 2 (mask oxide ething) : 5 sec, Step 3 (anisotropic silicon etching) : 20 ~ 35 sec, Step 4 (isotropic silicon etching) : 0 sec
Channel Narrowing	Isotropic SC1 etching	SC1 $NH_4OH : H_2O_2 : H_2O = 1 : 1 : 6$, 75 ~ 85 degC, 10 ~ 60 min
	HSQ (BOX) removal	BHF 20 sec SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
Gate oxidation	Cleaning	HF : H_2O = 1 : 100, 90 sec SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min HF : H_2O = 1 : 100, 90 sec SC1 $NH_4OH : H_2O_2 : H_2O = 0.25 : 1 : 5$, 75 ~ 85 degC, 10 min HF : H_2O = 1 : 100, 60 sec
	Gate oxidation	Dry oxidation 900 degC, 10 ~ 20 min
Gate deposition	Poly-Si deposition	CVD 580 degC, SiH_4 250 sccm, 33 Pa, 45 min
Gate lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec
	Pre-baking	100 degC, 10 min
	Exposure	DWL 200
	Development	NMD-3 (TMAH 2.38 %) 60 sec
	Post-baking	100 degC, 15 min
Gate etching	Helicon RIE	Step 2 : 5 sec, Step 3 : 100 ~ 105 sec, Step 4 : 30 sec
	Resist removal	Acetone

		SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
Ion implantation		P^+ 35 keV, 3×10^{15} cm^{-2} (for n-type) BF^{2+} 35 keV, 3×10^{15} cm^{-2} (for p-type)
Passivation deposition	Cleaning	SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
	Oxide deposition	CVD 400 degC, SiH_4 15 sccm, O_2 60 sccm, 33 Pa, 140 min
Annealing	Cleaning	SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
	N_2 Annealing	950 degC, N_2 1.0 l/min, 20 min
	H_2 Annealing	430 degC, N_2 6.5 l/min, H_2 100 sccm, 25 ~ 45 min
Contact hole lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec
	Pre-baking	100 degC, 10 min
	Exposure	Karl Suss aligner 10 sec
	Development	NMD-3 (TMAH 2.38 %) 90 sec
	Post-baking	110 degC, 15 min
Contact hole etching	Contact hole etching	BHF 3 ~ 5 min
	Resist removal	Acetone SPM $H_2O_2 : H_2SO_4 = 1 : 3$, 110 ~ 130 degC, 10 min
Al evaporation	Cleaning	$HF : H_2O = 1 : 100$, 90 sec
	Al evaporation	
Al electrode lithography	Spin coating	Az 1500 (20cp) 500 rpm, 5 sec, → 6000 rpm, 60 sec
	Pre-baking	100 degC, 10 min
	Exposure	DWL 200
	Development	NMD-3 (TMAH 2.38 %) 60 sec
	Post-baking	110 degC, 15 min
Al etching	Al etching	Al etchant 45 ~ 55 degC, 1 min
	Resist removal	Acetone

List of Publications and Presentations

Journals

[1] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, T. Hiramoto, "Electron Mobility in Silicon Gate-All-Around [100]- and [110]-Directed Nanowire Metal-Oxide-Semi conductor Field-Effect Transistor on (100)-Oriented Silicon-on-Insulator Substrate Extracted by Improved Split Capacitance-Voltage Method," Japanese Journal of Applied Physics, Vol.48, No.1, p.011205, January, 2009.

[2] T. Hiramoto, J. Chen, Y.J. Jeong, and T. Saraya, "Transport in Silicon Nanowire Transistors", ECS Transactions, Vol. 18, No. 1, p.55, March, 2009.

[3] J. Chen, T. Saraya, and T. Hiramoto, "Experimental Investigations of Electron Mobility in Silicon Nanowire nMOSETs on (110) Silicon-On-Insulator," to be published in *IEEE Electron Device Letter.*

[4] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, T. Hiramoto, "Experimental Study on Electron Mobility Behaviors in Silicon Gate-All-Around Nanowire nMOSFETs on (100) Silicon-On-Insulator," submitted to *Trans. on Electron Devices.*

Presentations (International)

[1] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, T. Hiramoto, "Experimental Study of Mobility in [110]- and [100]-Directed Multiple Silicon Nanowire GAA MOSFETs on (100) SOI," in *Symposium on VLSI Technology*, Hawaii, USA, p.93, 2008.

[2] J. Chen, T. Saraya, T. Hiramoto, "Electron Mobility in Multiple Silicon Nanowires GAA nMOSFETs on (110) and (100) SOI at Room and Low Temperature," in *IEDM Tech. Dig.*, San Francisco, CA, USA, p.757, 2008.

[3] J. Chen, T. Saraya, T. Hiramoto, "High Hole Mobility in Multiple Silicon Nanowire Gate-All-Around pMOSFETs on (110) SOI," in *Symposium on VLSI Technology*, Kyoto, Japan, p.90, 2009.

[4] Y. Jeong, J. Chen, T. Saraya, T. Hiramoto. "Uniaxial Strain Effects on Silicon Nanowire pMOSFET and Single-Hole Transistor at Room Temperature," in *IEDM Tech. Dig.*, San Francisco, CA, p.761, 2008.

[5] T. Hiramoto, J. Chen, Y. Jeong, and T. Saraya (Invited), "Silicon Nanowire FETs and Single-Electron/Hole Transistors under Uniaxial Strain at Room Temperature", *International Symposium on Nanoscale Transport and Technology (NTT2009)*, NTT Atsugi R&C Center, Kanagawa, p.99, January 22, 2009.

[6] T. Hiramoto, M. Kobayashi, and J. Chen (Invited), " Mobility and Variability in Silicon Nanowire MOSFETs", *14th International Symposium on the Physics of Semiconductors and Applications (ISPSA-2008)*, Korea, Ramada Plaza Jeju Hotel, Jeju, p.192, August, 2008.

Presentations (Domestic)

[1] 陳杰智, 清水健, 筒井元, 平本俊郎. "(100)面 UTB MOSFET における音響フォノン散乱移動度の劣化機構の考察," 平成 19 年秋季第 68 回応用物理学会学術講演会, 7p-ZL-9,北海道, 2007 年 9 月.

[2] 陳杰智, 更屋拓哉, 宮地幸祐, 清水健, 平本俊郎. "(100) SOI基板上に作製した[110]および[100]方向マルチシリコンナノワイヤGAA MOSFETの移動度評価," 応用物理学会シリコンテクノロジー分科会, 東京, 2008年7月.

[3] 陳杰智, 更屋拓哉, 宮地幸祐, 清水健, 平本俊郎. "[110]および[100]方向マルチシリコンナノワイヤ GAA MOS トランジスタにおける移動度評価," 平成 20 年秋季第 69 回応用物理学会学術講演会, 4p-E-14, 名古屋, 2008 年 9 月.

[4] 陳杰智, 更屋拓哉, 平本俊郎. "[110]および[100]方向(110)シリコンナノワイヤ GAA MOS トランジスタにおける電子移動度評価," 平成 21 年春季第 56 回応用物理学関係連合講演会, 筑波大学, 1a-V-10, 2009 年 4 月.

[5] 陳杰智, 更屋拓哉, 平本俊郎. "シリコンナノワイヤGAA MOSトランジスタにおける電子移動度の温度依存性評価," 平成 21 年春季第 56 回応用物理学関係連合講演会. 筑波大学, 1a-V-11, 2009 年 4 月.

[6] 陳杰智, 更屋拓哉, 平本俊郎. "(110)SOI 基板上に作製したシリコンナノワイヤ pMOSFETs の移動度," SDM 研究会, 東京, 2009 年 7 月.

[7] 陳杰智, 更屋拓哉, 平本俊郎. "(110)シリコンナノワイヤ GAA MOS トランジスタにおける正孔移動度に関する研究," 平成 21 年秋季第 70 回応用物理学会学術講演会. 東京, 11a-TH-11, 2009 年 9 月.

[8] 平本俊郎, 陳杰智, 鄭然周, 更屋拓哉, "シリコンナノワイヤトランジス タにおける移動度とひずみ効果", 2009 年春季第 56 回応用物理学関係連合講演会, 筑波大学, 1p-X-5, 2009 年 4 月.

[9] 鄭然周, 陳杰智, 更屋拓哉, 平本俊郎. "シリコンナノワイヤ pMOSFET 及び室温動作単正孔トランジスタにおける一軸歪みの効果," SDM 研究会, 北海道, 2009 年 2 月.

Award

[1] IEEE EDS Japan Chapter Student Award, January, 19, 2009, Tokyo.