Mobility in SOI MOSFETs under Strain and Quantum Confinement

SOI MOSFET の移動度に歪みと量子効果が与える影響

by

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Abstract

For nearly forty years, Si-based LSI systems have made a tremendous advance in performance by miniaturizing the metal-oxide-semiconductor field-effect-transistor (FET) size, following the "scaling rule." However, as the size of FETs shrinks, one big, physically inevitable problem becomes prominent than ever: threshold voltage (V_{th}) variability. As one LSI consists of a few billions of FETs, V_{th} variability results in severe yield degradation. To continue enhancing LSI performance for another decade, V_{th} variability problem must be dealt and solved.

To overcome V_{th} variability problem, the channel dopant concentration should be decreased. However, a reduction in dopant concentration means a weak immunity to the short channel effect, which is known as another big problem. Thus, the increase or decrease in dopant concentration, which has been a key in LSI scaling for many years, cannot solve problems in state-of-the-art FETs.

For further scaling, a silicon-on-insulator (SOI) technology is thought to be one of the most promising FET structures in near future. SOI-based strictures, including partially-depleted, fully-depleted, double-gate, Fin-type FET, and gate-all-around structure, enables us to obtain the lower doping concentration because of their structural confinement to the channel. However, to suppress the short channel effectively with non-doped SOI-based structures, the SOI thickness should be one quarter of the gate length in SOI FETs, and a half of it in double-gate FETs or FinFETs, which means the SOI thickness is less than 10 nm in near future. In such a thin SOI, the quantum confinement effect significantly affects the carrier conduction, which is not fully taken into consideration in the design of FETs.

The purpose of this dissertation is to address the possibility of (110)-oriented CMOS FETs, based on the experimental investigation on the effects of both the quantum confinement and the strain on carrier transport in SOI FETs. The results obtained in this dissertation are summarized as follows.

Hole mobility in (110) surface benefits from the quantum confinement effects. Stronger quantum

confinement, such as higher surface electric field or thinner SOI thickness, reduces the conduction effective mass especially in <110> direction. Therefore, the advantage of hole mobility in (110) FETs over that in (100) FETs is prominent especially under strong quantum confinement.

The sensitivity of hole motility to the strain is smaller in (110) surface than that in (100) surface in both bulk and ultrathin body FETs. The benefits from the strain and the quantum confinement seem to saturate if they are larger than a certain amount. Despite the smaller sensitivity to the strain, (110)-oriented ultrathin body pFETs is expected to have higher performance than (100)-oriented ultrathin body pFETs thanks to originally high hole mobility.

The non-parabolicity in <110> direction leads to the invalidity of the effective mass approximation, and it is more prominent in ultrathin body FETs. <110>-directed electron mobility is always lower than <100>-directed electron mobility in bulk nFETs, however, the electron mobility in <110> direction is higher than that in <100> direction in an ultimately thin SOI. Considering that the hole mobility in <110> direction is higher than that in <100> direction, higher CMOS circuit performance can be obtained with both p- and nFETs in <110> direction in ultimately thin SOI CMOS circuits.

The sensitivity of electron mobility to the strain is comparable to bulk FETs if the SOI is thick enough, though the sensitivity reduces as SOI thins. This is because the subband energy shift, which is thought to be the main mobility modulation mechanism, won't affect the electron mobility in ultrathin body FETs. However, the strain is still effective to enhance electron mobility in ultrathin body FETs.

The CMOS performance of (110) ultrathin body FETs is higher if the strain is low enough. As the strain increases, the performance of (100) CMOS increases, though the (110) CMOS doesn't increase much. Therefore, it is concluded that the CMOS FETs utilizing (110)-oriented ultrathin body FETs is one of the performance boosting technologies for the low-cost devices instead of high performance devices with high amount of strain.

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Chapter 1

Introduction

1.1 What Limits the CMOS Scaling?

For nearly forty years, Si-based LSI systems have made a tremendous advance in performance by shrinking the metal-oxide-semiconductor (MOS) field-effect-transistor (FET) size, following the "scaling rule." This simple rule has given us a guideline how to obtain smaller die size, lower power consumption, and higher operation speed [1]. Even though there have been many hard problems to solve from the fabrication point of view, breakthrough technologies have always been invented to every tiny problem. For instance; the shallow trench isolation technique was invented, instead of the local oxidation of silicon (LOCOS) process to obtain dense pattern. The ion-implantation process was adopted instead of the vapor phase diffusion process to make steep dopant profile. By these efforts, the size of MOSFETs has been successfully shrunk and now the gate length reaches around 40 nm even in the mass production [2–5].

However, as the size of FETs shrinks, one big, physically-inevitable problem severely degrades the performance of LSI: threshold voltage V_{th} variability (V_{th} variability) [6–9]. As one LSI consists of millions of FETs, V_{th} variability results in yield degradation. To continue enhancing LSI performance for another decade, V_{th} variability problem must be dealt and solved.

V_{th} variability originates from the dopant number fluctuation under the gate. The dopant distribution is known as a statistical phenomena, following a normal distribution [8]. Thus, its impact on V_{th} is exaggerated as the FET size is smaller and the dopant number under the gate is larger.

A reduction in dopant number under the gate can be one of the key techniques to overcome V_{th} variability. However, a reduction in dopant concentration means a weak immunity to the short channel effect, which is known as another performance and yield degradation problem [10]. Thus,

V_{th} variability and short channel effect are two competing problems in terms of dopant number, which makes it difficult to continue scaling by utilizing bulk FET technology.

1.2 Silicon-on-Insulator Technology and its Potential Problem

To overcome V_{th} variability and short channel effect problems, a silicon-on-insulator (SOI) technology is thought to be one of the most promising FET's structures in near future [11]. SOI-based structures, including partially-depleted (PD), fully-depleted (FD), double-gate, Fin-type FET (FinFET), and gate-all-around structure, enables us to obtain the lower doping concentration at the same short channel effect because of their structural confinement to the channel. The channel of these FETs is surrounded by the gate oxide and/or the buried oxide (BOX), thus the short channel effect is effectively suppressed. By utilizing a SOI structure, lower dopant concentration, or potentially, non-doped channel can be achieved.

In terms of the short channel effect, the SOI thickness (t_{SOI}) should be one quarter of the gate length in FD SOI FETs, and a half of it in double-gate FETs with non-doped channel [12, 13]. This means t_{SOI} must be less than 10 nm in near future. In such a thin SOI, another physics-based problem emerges: quantum confinement effect. Carriers in the channel is confined by ultimately thin SOI, which makes the behavior of carriers completely different from that in bulk FETs [14–19].

Thus, the quantum confinement effects, such as the threshold voltage increase [14], mobility modulation [15,16] and finite inversion layer thickness [20], should be taken into consideration in advanced SOI-based FETs.

1.3 High mobility materials

On the other hand, as the shrinkage of FETs size becomes more difficult, another method to improve the LSI performance has been sought: high hole mobility materials. Mobility is one of the important parameters which determine the LSI performance. Higher mobility means higher drive current, and hence, higher performance. By replacing Si (100)-surface with high mobility material, high performance can be obtained without shrinkage.

There are many high mobility candidates: III-V or II-VI compound materials for nFETs, and germanium or Si (110)-surface for pFETs. Even though many studies have been done on high

mobility materials [21–25] , all of them except Si (110) suffers from engineering problems, such as poor quality of films and difficulty in making short channel FETs. This is partly because few engineering experience has been had on compound materials or germanium, while many experiences have on silicon. Cost is another issue. Almost all the equipments can be utilized for Si (110), while another equipment is necessary for compound materials or germanium. Since the manufacturability and integrity is of great importance for LSI, Si (110)-surface is one of the most promising materials.

1.4 Near future LSI and objectives of this work

Considering the state-of-the-art research and development situation, Si-based LSI will be utilized at least for another decade. Performance boosting technologies, which are 100% compatible with Si LSI will be introduced in mass production.

In that sense, Si (110) is one of the most promising options. Both high compatibility with Si-based LSI technology and higher hole mobility than Si (100) are maintained. It should be noted that Si (110) surface could be utilized in FinFETs, in which the Fin direction is <110>-direction on Si (100) surface. In this case, the main current paths are side surfaces of FinFETs and their orientation is Si (110).

In spite of its importance, the physics behind Si (110) surface is not fully understood yet. To design the future nano-scale FETs, they must be clarified.

In this dissertation, the former part focuses on the physics on carrier transport behind ultra-thin body SOI FETs on Si (110) surface; After the brief summary of general descriptions on carrier mobility (chapter 2), the direction dependence of hole mobility (chapter 3) and hole mobility enhancement by strain (chapter 4) will be shown. Then, the direction dependence of electron mobility (chapter 5) is discussed, followed by electron mobility enhancement by strain (chapter 6). The final aim of this dissertation, whether Si (110) could defeat the Si (100) surface in terms of a CMOS operation, is discussed in chapter 7.

Chapter 2

Physics on Carrier Mobility

2.1 Drive Current and Low-Field Mobility

The drive current I_D in a FET is described as follows.

$$\frac{I_D}{W} = qN_{inv}v_d \tag{2.1}$$

where W, q, N_{inv}, and v_d are the gate width, the unit charge, the surface inversion charge density and the carrier velocity, respectively. This simple equation means that the current is the multiplication of the " number of carriers" by "velocity of carriers." This equation is always true.

In a long channel FET, v_d is proportion to the multiplication of the low-field mobility μ by the lateral electric field E and it approaches to the saturation velocity (v_{sat}) as E increases.

$$v_d = \mu E < v_{sat} \tag{2.2}$$

Here, v_{sat} is defined by state scattering between the lattice and the carriers at the the thermal equilibrium, which is a constant value in each material. Once the velocity saturation occurs, the mobility no longer affects the drive current. However, the higher mobility leads to higher velocity at a certain electric field, which means it takes less time to charge the capacitance of the next nodes in a CMOS circuit. Thus, the mobility is a direct indicator of a CMOS performance.

In a short channel FET, carriers are less scattered and can acquire larger energy than the thermal equilibrium state, especially near the drain edge. Velocity of these carriers can easily exceeds the saturation velocity (velocity overshoot). Since v_d is larger than v_{sat}, the drive current is mainly determined by the velocity which is thermally injected to the channel at the source edge (thermal injection velocity v_{inj}) (Fig. 2.1). I_D is described by the thermal injection velocity as [26]

$$I_{Dsat} = WC_{ox}v_{inj}\frac{1-r_c}{1+r_c}\big(V_{GS} - V_{th}\big) \tag{2.3}$$

where C_{ox} is the gate capacitance, V_{GS} is the gate voltage, and V_{th} is the threshold voltage. Here, r_c is the back-scattering coefficient, indicating the fraction of carriers which are back-scattered in the channel region. r_c can be estimated from the mean-free-path near the thermal equilibrium. More explicitly, Eq. (2.3) can be re-written as [27]

$$\frac{\Delta I_{Dsat}}{I_{Dsat}} = \frac{\Delta\mu}{\mu}(1 - B_{sat}) \tag{2.4}$$

where ΔI_{Dsat} and $\Delta\mu$ represent the change in I_{Dsat} and μ, respectively. B_{sat} is the change in ratio of actual current to its ballistic limit.

In the ballistic limit, where no carriers are scattered in the channel region, B_{sat} is equal to unity. Thus, $\Delta I_{Dsat}/I_{Dsat}$ is equal to zero, meaning that the drive current is no longer affected by the mobility. However, a FET at room temperature may not reach its ballistic limit: it has experimentally reported that B_{sat} of a FET with its gate length of 10 nm is 0.43 [28] and that B_{sat} with gate length of 40 nm is 0.5 [27], both of which are far from the ballistic transport. Though the low-field mobility will less affect the drive current at shorter channel length, the mobility will still be a good indicator of performance of a FET.

2.2 Scattering Mechanisms and Their Impacts on Mobility

It is well known carriers in the inversion layer of bulk FETs are mainly scattered by three factors [29]:

coulomb scattering
: substrate impurities, interface state densities, charges trapped in gate oxide

phonon scattering
: lattice vibrations by finite temperature

surface roughness scattering
: spatial nanoscale heterogeneity of Si/SiO_2 interface

Each scattering mechanism from the top is dominant at the low-, middle-, and high- surface electric field. The total mobility curve is schematically shown in Fig. 2.2. Empirically, total mobility is evaluated by the Matthiessen's rule as [29]

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{coulomb}} + \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{sr}} \tag{2.5}$$

where $\mu_{coulomb}$ is the coulomb scattering-limited mobility, μ_{phonon} is the phonon scattering-limited mobility, and μ_{sr} is the surface roughness scattering-limited mobility.

Though there are other scattering mechanisms in inversion layer carriers, such as the remote coulomb scattering [30], the remote phonon scattering [31], or the δt_{SOI} scattering mechanism [32,33]. Here, only an ultimately thin SOI-related scattering mechanism, the δt_{SOI} scattering mechanism, will be mentioned here.

A special scattering mechanism which only occurs in a SOI FET is the δt_{SOI} scattering. As t_{SOI} becomes around less than 3 nm, mobility is dominated by t_{SOI} fluctuation-induced scattering. t_{SOI} fluctuation locally induces large potential barriers, which scatter the inversion layer carriers as shown in Fig. 2.3. It is experimentally confirmed that mobility limited by local t_{SOI} fluctuation is proportional to t_{SOI}^6 in both (100) ultrathin body (UTB) FETs [17] and (110) UTB FETs [34].

2.3 Quantum Confinement Effects on Carrier Mobility

Even in the bulk FETs, inversion carriers are confined in a triangular-shaped well, which is formed by the gate dielectric barrier and the conduction band. Therefore, carriers are not induced from the bottom of the well, but located in discretized subbands [10] as shown in Fig. 2.4 (a). The quantum confinement effects on inversion carriers cause [10]:

(1) higher threshold voltage at higher surface electric field

(2) finite inversion layer thickness

These effects are well-known, and especially the finite inversion layer thickness is a severe problem in the equivalent oxide thickness (EOT) scaling.

In UTB FETs, an additional confinement by the SOI layer exists. The carriers in SOI FETs are much influenced by the quantum confinements effects (Fig. 2.4 (b)). Typically, a FET with SOI thickness below 20 nm suffers from the quantum confinement effects, such as threshold voltage increase (Fig. 2.5) or the mobility modulation (Fig. 2.6). Though a mobility enhancement mechanism has been reported in (100)-oriented UTB nFETs [17] and (110)-oriented UTB pFETs [34] at a certain SOI thickness, the mobility itself is comparable or less than that in bulk FETs.

Even though an UTB FET is one of the most promising device structure in near future, the mobility enhancement techniques are mandatory to compensate the mobility degradation by the quantum confinements effects.

2.4 Mobility Enhancement Technique

So far, the importance of the low-field mobility is confirmed. Even though the mobility has a less influence on the drive current at shorter gate length, it is directly related to the drive current. The mobility will remain one of the most important parameters in a FET. By improving the low-field mobility, the higher drive current can be obtained. In a UTB FET, which is one of the best candidates in near future FET structure, the mobility enhancement technique is a mandatory technology in performance enhancement to compensate the degraded mobility.

In the relaxation time approximation, the mobility can be described as

$$\mu = \frac{q}{m^*} < \tau > \tag{2.6}$$

where m^* is the effective mass, and the $<\tau>$ is the relaxation time. $<\tau>$ is different in each scattering mechanism, representing the physics behind. Following Eq. (2.6),

(1) lighter m^*

(2) larger $<\tau>$

are preferable to obtain higher mobility. This is a basic concept to enhance the mobility.

A key technique to improve the mobility is the strain engineering. The strain alters the lattice constant of Si, and hence, the subband structures. Proper strain enlarges the subband energy difference (less inter-subband scattering) and/or makes the effective mass smaller.

For qualitative understandings, the piezoresistive coefficients in bulk silicon (Table 2.1) is often referred [35, 36]. Since the piezoresistive coefficients are measured in bulk silicon, the quantitative discrepancy between bulk and FETs has been observed and reported [37]. However, at least the proper strain direction to enhance the mobility is well-described by them.

Physically, the strain mainly alters the effective mass, the density-of-states (DOS), and the subband energy difference. The latter two are related to the relaxation time. It has been reported that strain mainly affects the subband energy difference in nFETs, and the effective mass in pFETs [38, 39].

In the state-of-the-art mass production, the tensile- or compressive- etch stop layer (tESL and cESL, respectively) have been widely used to introduce the strain into the channel. Recently, the embedded silicon-germanium (SiGe) is epitaxially grown in source and drain region so that the larger stress (∼1.5 GPa) can be introduced to the channel [4, 40], which is also in mass-production.

2.5 Summary

The physics behind the low-field mobility has been overviewed. Even in a state-of-the-art short channel FETs, the mobility is still one of the key parameters to evaluate a performance of a FET. Thus, strain technology to enhance the mobility will be of great importance in the mass production.

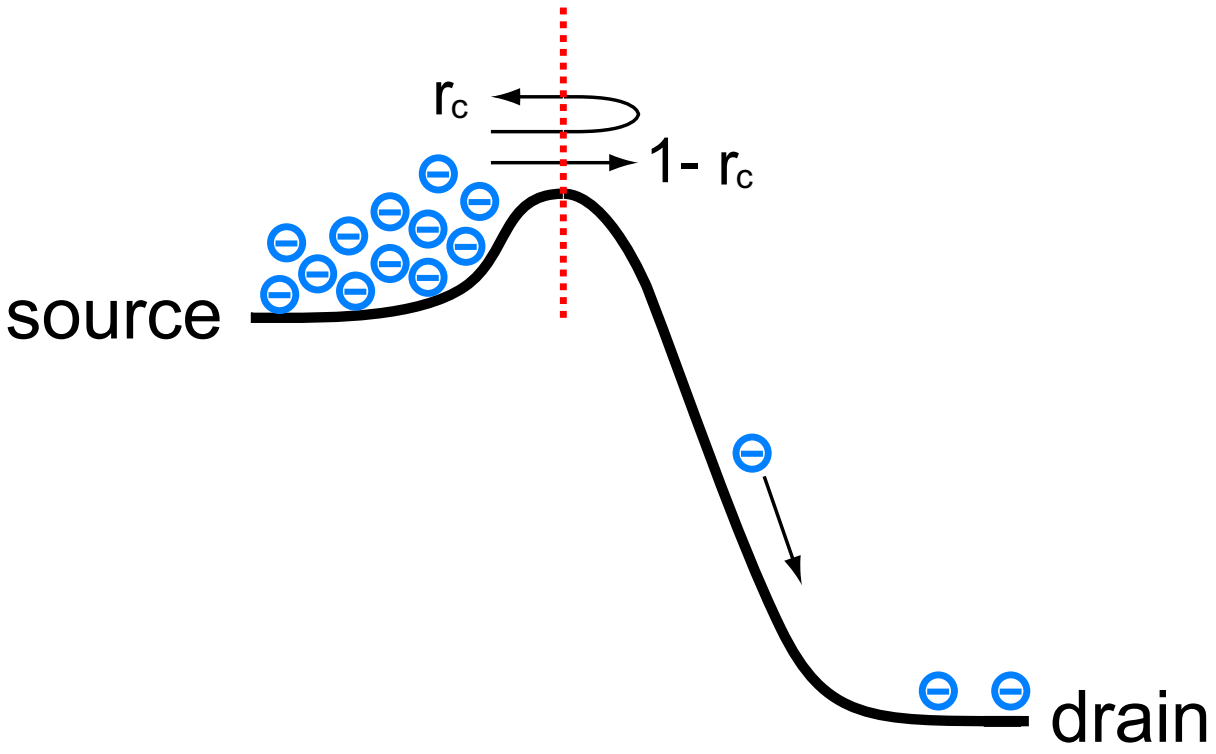


Fig.2.1 A schematic of energy band diagram. The potential barrier is the highest near source edge. Once the carrier gets across the potential barrier, it won't scattered back to source.

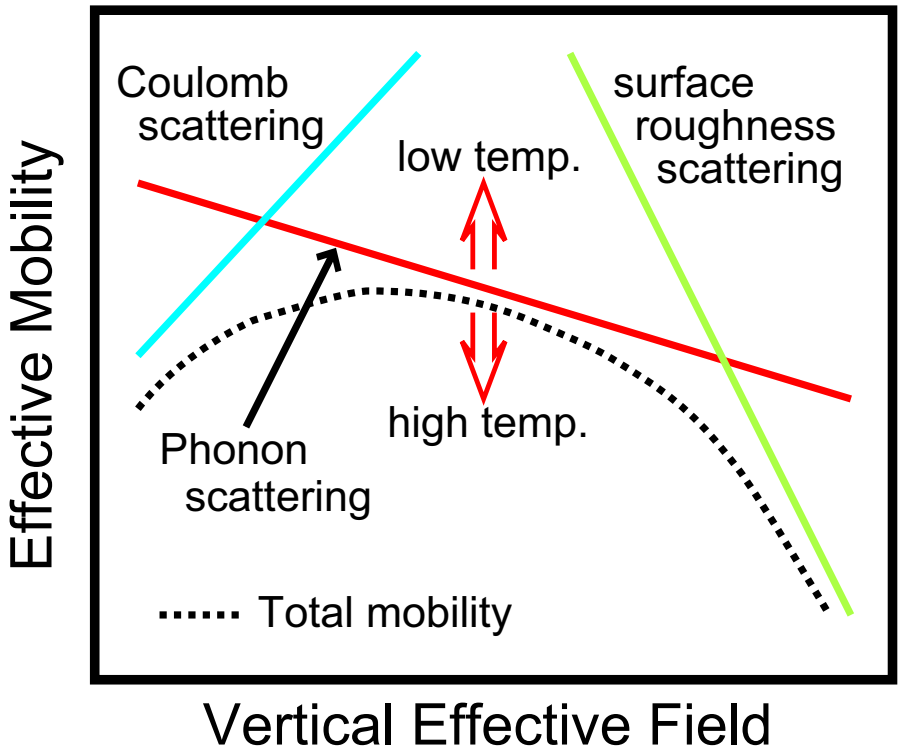


Fig.2.2 A schematic diagram of mobility determining factors. Each scattering mechanism is combined by the Matthiessens' Rule. Note that only phonon scattering is temperature dependent.

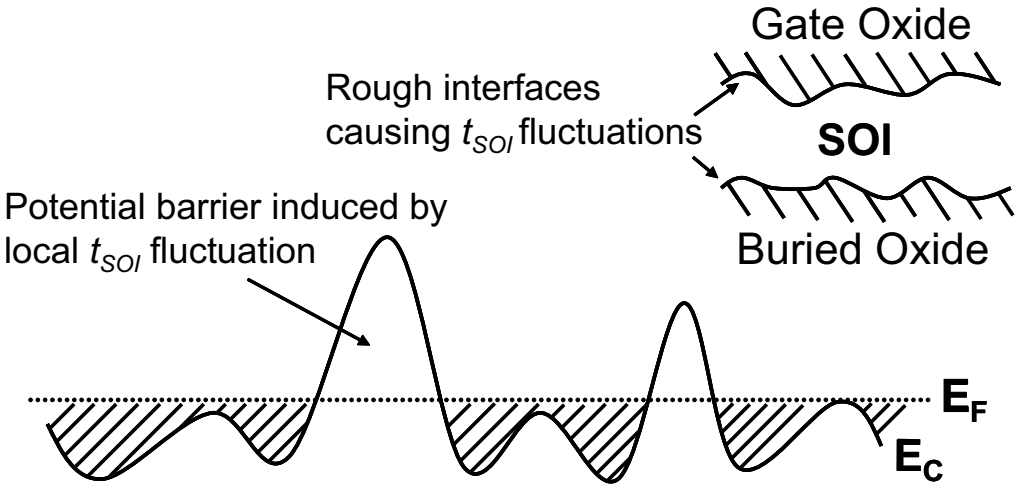


Fig.2.3 Schematic diagrams showing Si/SiO_2 interface fluctuation. Large barriers are locally induced by t_{SOI} fluctuation in an atomic level, which scatters the conducting carriers.

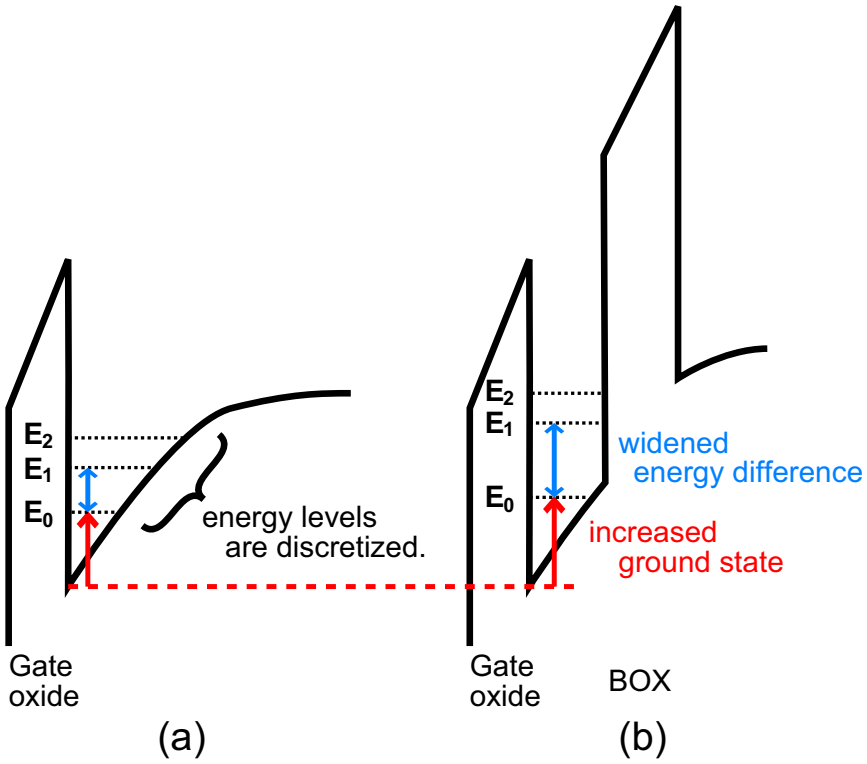


Fig.2.4 Subband structures of (a) bulk FETs and (b) SOI FETs. In both cases, subbands are formed because of the well between the gate dielectric and conduction band. In addition to a potential well, a SOI layer confinement exists in SOI FETs.

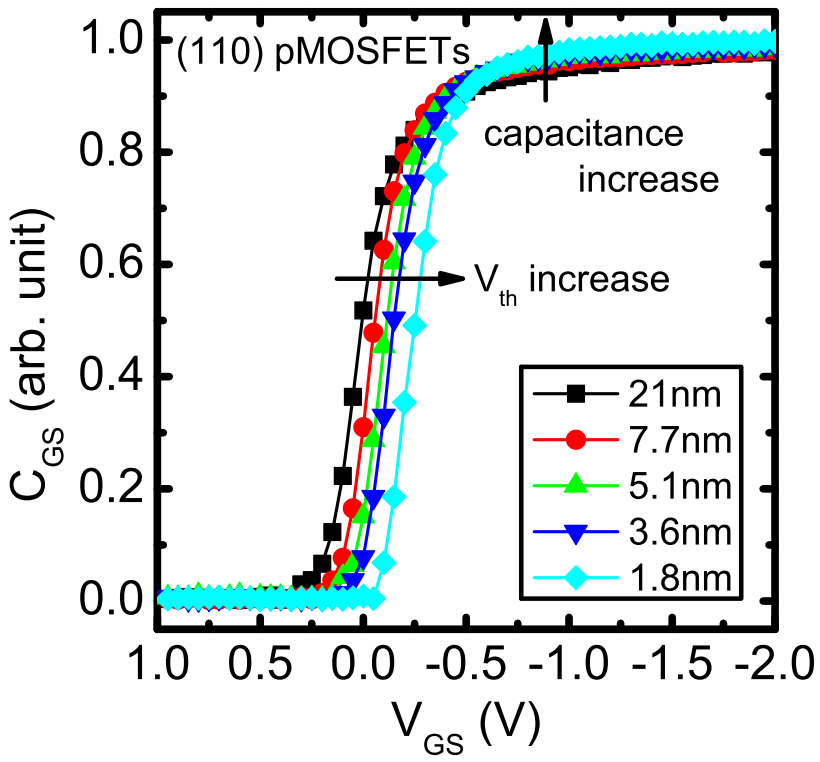


Fig.2.5 Experimental dependence of threshold voltage on SOI thickness in (110) pFETs fabricated in this dissertation. Monotonic threshold voltage increase is observed as previously reported [34].

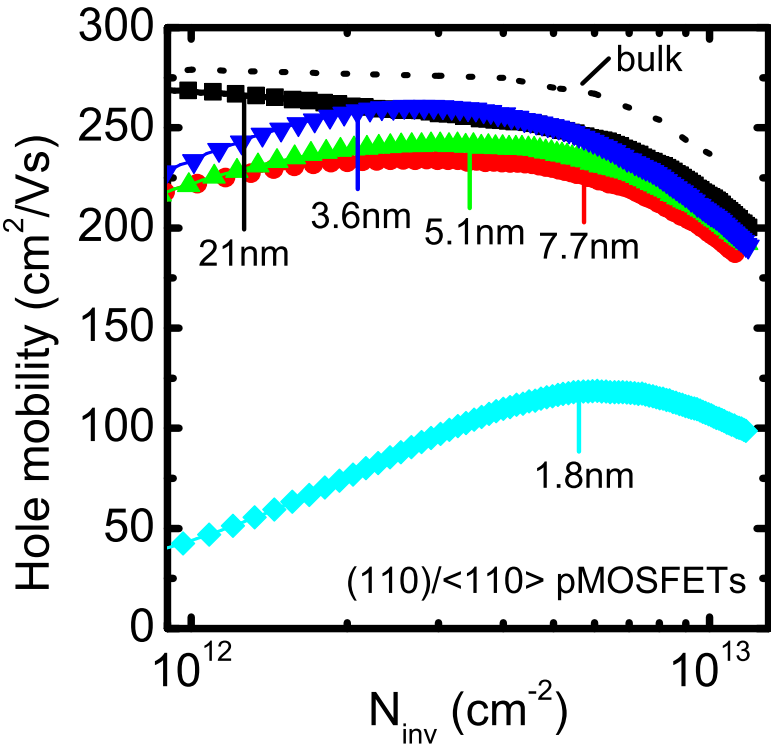


Fig.2.6 Experimental hole mobility behavior as a function of inversion layer charge density for various SOI thickness in (110) SOI pFETs fabricated in this dissertation. Mobility modulation by SOI thickness can be confirmed.

Table2.1 Piezoresistance coefficients of bulk silicon [35,36]. Unit: 10^{-12} Pa^{-1}.

direction	strain parallel to the channel	strain perpendicular to the channel
n-<110>	-31.2	53.4
n-<100>	-102.2	53.4
p-<110>	71.8	-1.1
p-<100>	-1.1	6.6

Chapter 3

Direction Dependence of Hole Mobility in Si (110) pMOSFETs

3.1 Introduction

Si (110) surface is very attractive because of its high hole mobility (μ_h) [34, 37, 40–43]. Especially in an ultimately scaled device structure, such as a FinFET or an ultra-thin body (UTB) FET, this superiority becomes more prominent since μ_h in Si (110) is less degraded by thinning SOI thickness (t_{SOI}) than μ_h in Si (100) [34, 44]. Even in a bulk FET, μ_h in Si(110) has advantages over μ_h in Si (100) not only because μ_h is higher, but also because μ_h keeps high even at a high inversion layer density (N_{inv}) region. In other words, the superiority of μ_h in Si (110) becomes greater as N_{inv} becomes higher. This μ_h difference has been explained by the inter-subband scattering suppression due to large subband energy difference at the strong quantum confinement experimentally [44] and theoretically [45], originating from the heavy (110) effective mass normal to Si/SiO_2 surface (m_z).

However, μ_h in Si (110) has the direction dependence and μ_h in (110)/<100> shows stronger N_{inv} dependence than μ_h in (110)/<110> (Fig. 3.1). Since the subband energy structure of both <110> and <100> directions is the same, this peculiar direction dependence cannot be understood only by the suppression of the inter-subband scattering.

Another whispering experimental result on the peculiarity of μ_h in (110) is the direction dependent mobility universality [37, 46, 47]. While the hole mobility universality in (100) surface holds in different substrate impurities or under different substrate bias, it doesn't hold in (110) surface. Note the application of the substrate bias effectively means the increased or decreased substrate impurities, since the back bias strengthens or weakens the surface electric field. Figure 3.2 shows

experimentally obtained the substrate dependence of μ_h at N_{inv} of $3x10^{12}cm^{-2}$ for various t_{SOI}. As has reported in bulk pFETs [37, 46], slightly increased μ_h is observed in <110> direction by increasing the substrate bias, while slightly decreased μ_h is observed in <100> direction. In most cases, μ_h becomes smaller as substrate bias increases, since higher surface electric field, or the larger quantum confinement effect, makes μ_h smaller. Though this behavior is peculiar to (110) surface, the direction dependence of μ_h on the substrate bias cannot be understood only by the subband energy structure.

In both cases, the peculiarity of μ_h in (110) is prominent at higher stronger quantum confinement. Therefore, in order to clarify the mechanism of superior μ_h in (110)/<110>, the direction dependence of μ_h in (110) under different confinement effects should be investigated.

In this study, we focused on UTB pFETs because of their strong quantum confinement effect. μ_h in <110>- and <100>-directed Si (110) UTB pFETs was experimentally compared by utilizing a new device structure, which shares the same channel in both directions. It is newly found that the carrier re-population and average conductivity effective mass (m_c) change play a key role in the difference between μ_h in <110> direction and μ_h in <100> direction. In addition to the suppression of the inter-subband scattering, (110)/<110> pFETs enjoys high hole mobility even at high N_{inv} since average m_c becomes lighter as the confinement increases.

3.2 Device Structure of Common Channel FETs (CC FETs)

In UTB FETs (t_{SOI} smaller than ~5 nm), the mobility is very sensitive to t_{SOI}, which means the difficulty of making a fair comparison between different devices even if designed t_{SOI} is the same. To study the direction dependence of the mobility in UTB FETs, a special treatment is mandatory.

In (110) surface, both <110> and <100> directions are orthogonal. Therefore, to make the fair comparison between <110>- and <100>-directed UTB pFETs with an extremely thin SOI, a new device structure was utilized (Fig. 3.3). The new FET structure (common channel; CC) shares completely the same channel in both directions. The current direction can be controlled by the side gate (SG) voltage; by controlling the voltage of SG parallel to the current so that the channel under the SG is depleted, it behaves as a normal FET. Note that without a SG voltage control, the current flows through lower resistance regions (i.e. source and drain), as shown in Fig. 3.4 (a), resulting in

current overestimation (Fig. 3.4 (b)).

The fabrication process of CC FETs is quite similar to that of UTB FETs [17,34]. Four processes are added to the conventional fabrication process of UTB FETs. A detailed process flow is shown in Appendix A.2. Both gate length and width are 200 μm , and gate oxide thickness is 20 nm so that μ_h can be extracted precisely by using the split capacitance-voltage (C-V) method.

Figure 3.5 shows μ_h comparison between a CC FET (t_{SOI} =31 nm) and a normal SOI FET (t_{SOI} =31 nm). CC FETs show almost the same μ_h as μ_h of normal FETs, confirming the effectiveness of CC FETs. Though some μ_h degradation in both directions can be seen, this might be attributed to the series resistance under the side gate or the overlap capacitance between the main gate and the side gate.

3.3 Direction Dependence of (110) Hole Mobility

Figure 3.6 shows N_{inv} dependence of μ_h for various t_{SOI} by utilizing CC FETs. The N_{inv} dependence of μ_h in <110> direction is totally different from that in <100> direction. In particular, μ_h in <110> direction has weak N_{inv} dependence and keeps a high value even in a high N_{inv} region when t_{SOI} =31 nm. Another difference between two directions is the μ_h enhancement behavior when t_{SOI} is extremely small. It is well known that μ_h enhancement occurs when t_{SOI} is around 3-4 nm [34]. However, large μ_h enhancement in extremely thin SOI is observed only in <110> direction as clearly shown in Fig. 3.7. The μ_h enhancement mechanisms in thin SOI have been thought to be the suppression of the inter-subband scattering [34], which does not explain the direction dependence. Therefore, the behavior observed in Fig. 3.7 cannot be understood in terms of only the subband energy structure.

Figure 3.8 shows the ratio of μ_h in <110> direction to μ_h in <100> direction. Utilized devices are the same as those in Fig. 3.6. It is interesting to point out that the μ_h ratio increases in following two cases:

(1) higher N_{inv}

(2) thinner SOI

Both of above conditions mean the stronger quantum confinement effects. It should also be noted

that as SOI becomes thinner, the dependence of the ratio of μ_h on N_{inv} becomes weaker.

3.4 The Ratio of Hole Mobility under Different Temperature

To investigate the direction dependence in more detail, μ_h degradation ratio of 400K to 300K is derived. Under the relaxation time approximation, μ_h can be roughly expressed as

$$\mu_h = \frac{q}{m_c} < \tau >$$

where q is the Coulomb constant and $<\tau>$ is the relaxation time. Therefore, provided only the lowest subband is occupied, the component of m_c can be eliminated in the ratio of μ_h under different temperature. Note this assumption is theoretically valid in a high N_{inv} region even at the room temperature [45].

Figure 3.9 shows μ_h at 400 K. As the inter-subband phonon scattering increases, μ_h is degraded compared to that at 300 K. Figure 3.10 shows the μ_h ratio in the same direction. Negligible difference between <110> and <100> directions can be seen, indicating the direction dependence originates from m_c, rather than $<\tau>$. Figure 3.11 shows the ratio of μ_h in <110> direction to μ_h in <100> direction at 400 K. As expected, almost the same tendency as that at 300 K is confirmed.

3.5 Physical Understandings of Direction Dependence of Hole Mobility

3.5.1 Quantum confinement dependence of conduction effective mass

To understand m_c behavior under different quantum confinement effect, subband structures (subband diagram and population) were calculated by diagonalizing the 6-band k·p Hamiltonian [45, 48]. In this study, quantum confinement effects by

(1) the surface electric field (via triangular well approximation)

(2) the SOI thickness (via infinite potential at the Si/SiO_2 interface)

were taken into calculation. The detailed procedure of the numerical calculation are described in Appendix B. Figure 3.12 (a)-(d) shows the E-k diagram under the surface electric field F_s of 0.1 MV/cm (corresponding to weak inversion) for various t_{SOI}, and Fig. 3.12 (e)-(h) under F_s of 1 MV/cm (corresponding to strong inversion). Figure 3.13 shows the population of each subband (only the lowest two subbands are shown). The key to understand the

m_c in <110> direction

As shown in Fig. 3.12 (a), the energy dispersion of the second lowest subband in <110> direction is relatively large with t_{SOI} of 20 nm under low F_s, while it is much smaller as t_{SOI} decreases (Fig. 3.12 (b)-(d)). On the contrary, energy dispersion is almost the same under high F_s (Fig. 3.12 (e)-(h)). This means that the m_c of the second lowest subband in <110> direction decreases as the quantum confinement effects increases.

m_c in <100> direction

As shown in Fig. 3.12, the energy dispersion of the two lowest subbands in <100> direction is less dependent on t_{SOI} and F_s than that in <110> direction. This means that $m_c$in <100> direction is not so much dependent on t_{SOI} and F_s.

population in each subband

As shown in Fig. 3.13, the population of the lowest subband with t_{SOI} of 20 nm decreases with increasing F_s, while that with t_{SOI} of 3 nm keeps the same regardless of F_s.

These theoretical understandings of m_c and population can be summarized as follows. In <110> direction, the average m_c decreases as quantum confinement effects (i.e. thinner t_{SOI} or higher F_s) due to the carrier re-population to the lowest subband, which has smaller m_c. However, in <100> direction, the lowest and the second lowest subband have almost the same m_c. Therefore, the carrier re-population has almost no impacts on the average m_c, regardless of the quantum confinement effects.

This is the reason why the mobility universality doesn't hold in (110)/<110> pFETs, while it holds in (110)/<100> pFETs [37, 46, 47]. Since possible physics behind the mobility universality is based on the constant m_c [29], conditions precedent on the mobility universality doesn't satisfied in (110) pFETs.

3.5.2 Physical explanation of direction dependence

The experimental results and theoretical explanations are summarized in Fig. 3.14. As quantum confinement becomes larger (i.e. thin SOI or high F_s), two mechanisms play important roles:

(A) average m_c in <110> direction becomes lighter while that in <100> direction doesn't change

much.

(B) inter-subband scattering is suppressed due to larger subband energy difference.

The behavior of the μ_h ratio (Fig. 3.8) of <110> direction to <100> direction for various t_{SOI}

can be understood by (A). When SOI is thick, average m_c in <110> direction becomes lighter with increasing N_{inv}, while average m_c in <100> direction keeps almost constant, resulting in the larger ratio in a larger N_{inv} region. When SOI is thin, average m_c of both directions keeps constant, resulting in almost the same ratio regardless of N_{inv}.

The direction dependence of μ_h in thick SOI (Fig. 3.1) (and bulk FET)

is also understood by (A) in addition to (B) (Fig. 3.15). Average m_c becomes lighter as N_{inv} increases in <110> direction, leading to less dependence on N_{inv} than μ_h in <100> direction.

The direction dependence of μ_h enhancement in thin SOI (Fig. 3.7)

can be also explained by (A), in addition to (B). Though μ_h enhancement itself is explained by (B), average m_c of thin SOI is lighter than that of thick SOI only in <110> direction. As a result, μ_h enhancement is more prominent in <110> direction as schematically shown in Fig. 3.16.

3.6 Summary

The direction dependence of hole mobility behavior in (110) UTB pFETs has been investigated experimentally and theoretically utilizing a new device structure. The direction dependent behavior of Si (110) hole mobility can be understood in terms of average conductivity mass change by the quantum confinement, which is more prominent in <110> direction. Therefore, Si (110)/<110> hole mobility keeps higher mobility than (110)/<100> even in a high surface electric field region.

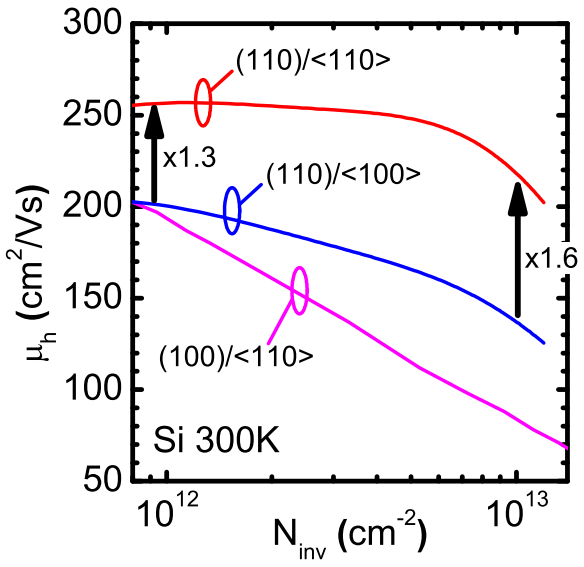
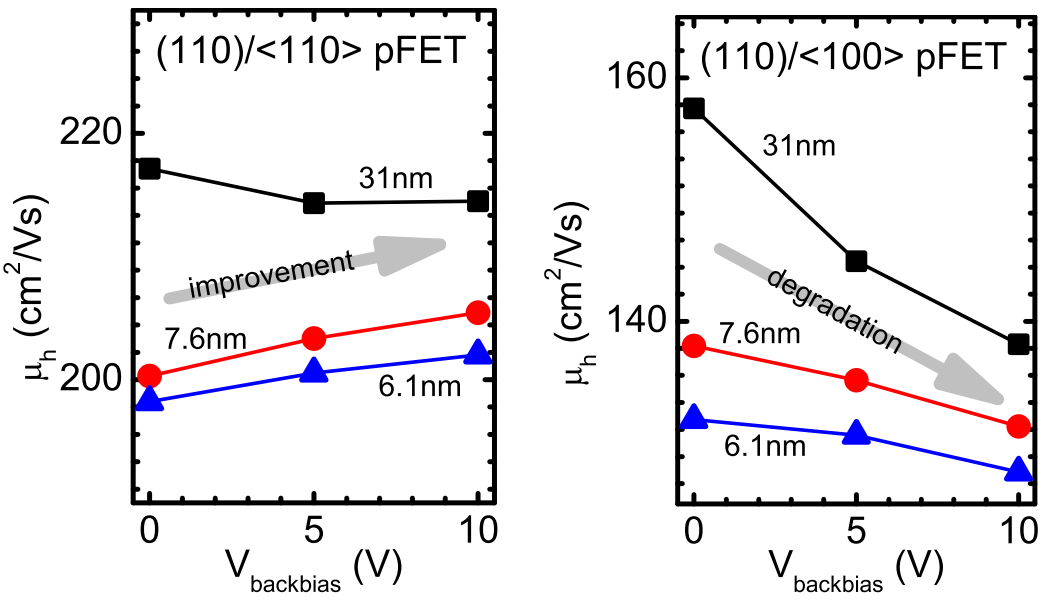


Fig.3.1 The N_{inv} dependence of μ_h in (110)/<110>, (110)/<100> and (100)/<110> pFETs. Superior μ_h in (110)/<110> to μ_h in (100)/<110> is confirmed. This superiority has been explained by the large subband energy difference [37], however, the N_{inv} dependence of μ_h in (110) surface is also dependent on directions. Since both (110)/<100> and (100)/<110> have the same subbands, the subband energy difference cannot explain this peculiar dependence.



(a) (b)

Fig.3.2 The dependence of μ_h on substrate bias for various t_{SOI}. In <110> direction, μ_h slightly increases as substrate bias increases as previously reported [37, 46]. On the contrary, μ_h monotonically decreases in <100> direction. Again, these results cannot be explained only by the suppression of inter-subband scattering.

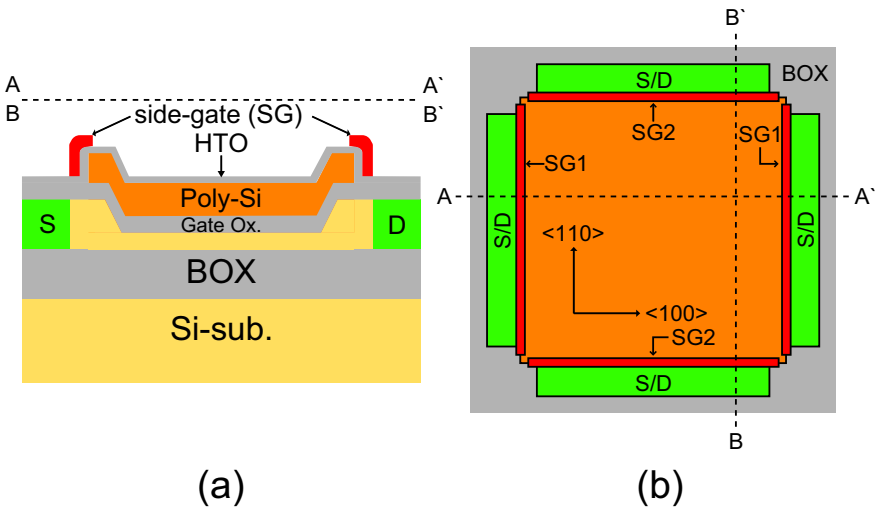


Fig.3.3 Schematics of (a) cross-section and (b) top view of a fabricated device structure (a common channel FET). The key of this structure is that both <110> and <100> directions share completely the same channel. The difference is only the current direction. This structure enables one to compare mobility of UTB FETs in two directions with exactly identical thickness in an atomistic order. By controlling the side gate voltage, current flows like a normal FET (see also Fig. 3.4).

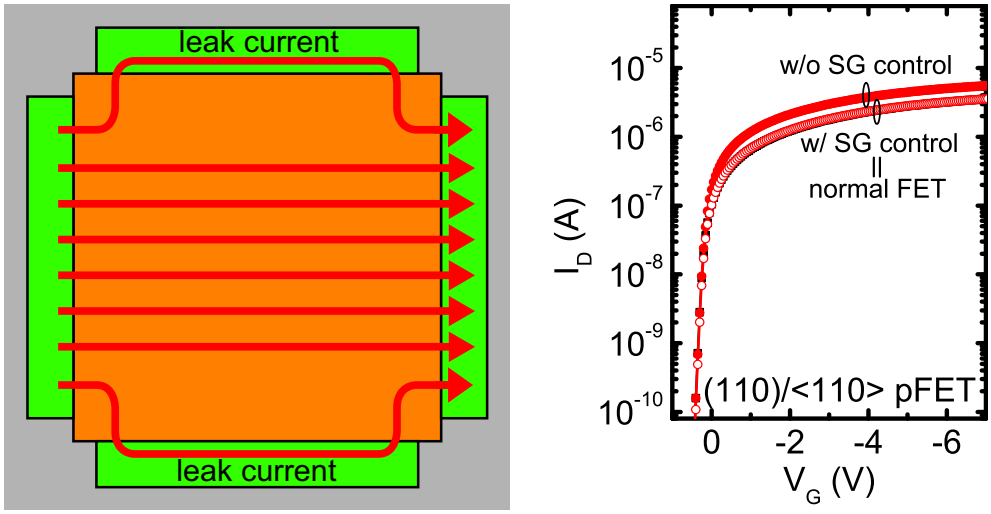
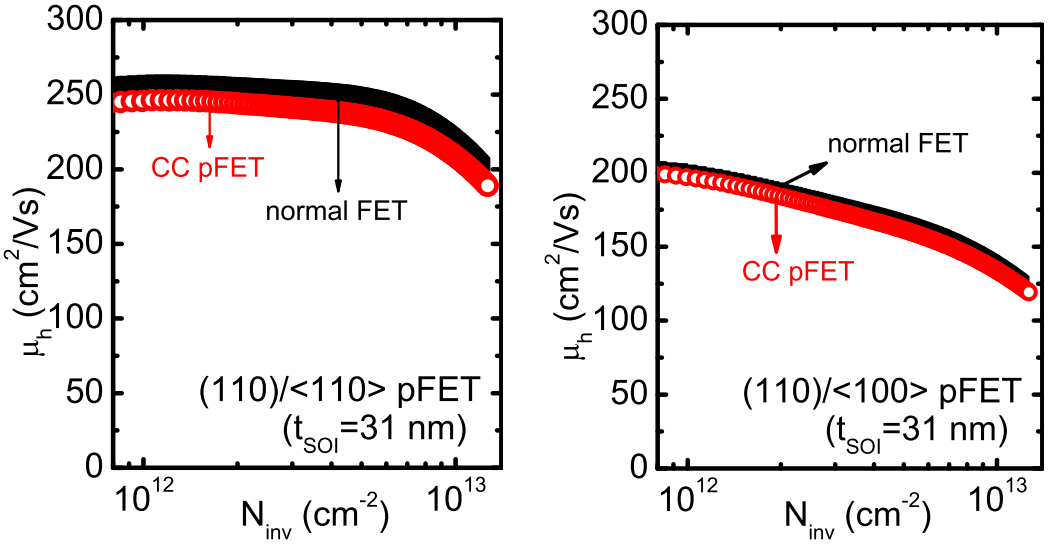
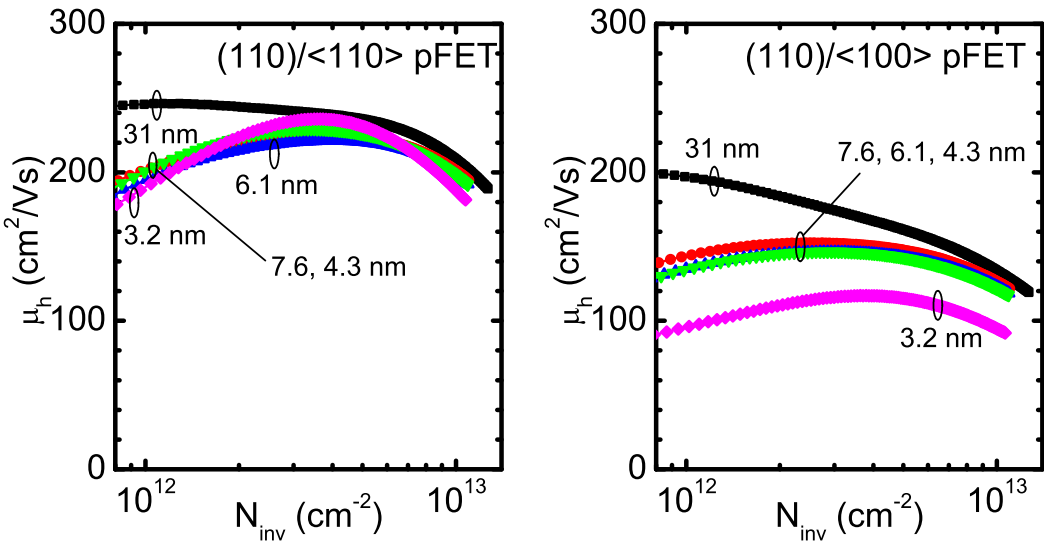


Fig.3.4 (a) A schematic of leakage current flow. Since the resistance of source and drain region is smaller than that of channel under the gate, current flows are no longer limited under the gate without side gate control. As a result, current (and mobility) is overestimated. (b) I_D-V_G characteristics of a common channel FET with and without side gate voltage control, and of a normal FET. Without side gate voltage control, current is overestimated.



(a) (b)

Fig.3.5 A comparison of extracted μ_h between normal FETs and common channel FETs with thick t_{SOI} of 31 nm in (a) <110> direction (b) <100> direction. In both directions, almost the same μ_h is obtained, strongly indicating the effectiveness of a common channel structure. Though some μ_h degradation is observed, this degradation might be attributed to the series resistance under the side gate or the overlap capacitance between main gate and side gate.



(a) (b)

Fig.3.6 The N_{inv} dependence of μ_h for various t_{SOI} in (a) <110> direction (b) <100> direction. As has already reported in a previous work [34], clear μ_h enhancement with t_{SOI} of 3.2 nm is observed in <110> direction. On the contrary, μ_h enhancement is relatively small in <100> direction (see also Fig. 3.7). Though physical mechanism of μ_h enhancement in Si (110) UTB FETs has been thought to be the suppression of the inter-subband scattering because of its large subband energy difference [37], this direction dependence cannot be understood only by that, strongly indicating the existence of another physical mechanism.

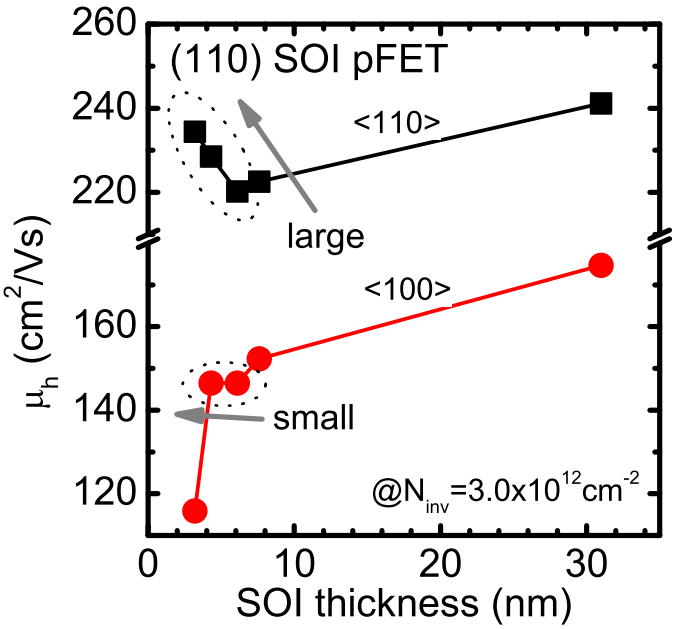


Fig.3.7 The t_{SOI} dependence of μ_h at N_{inv} of $3.0x10^{12}cm^{-2}$. Clear μ_h enhancement is observed in <110> direction, while negligible μ_h enhancement in <100> direction. This result implies μ_h enhancement mechanism in thin SOI isn't explained only by the suppression of the inter-subband scattering.

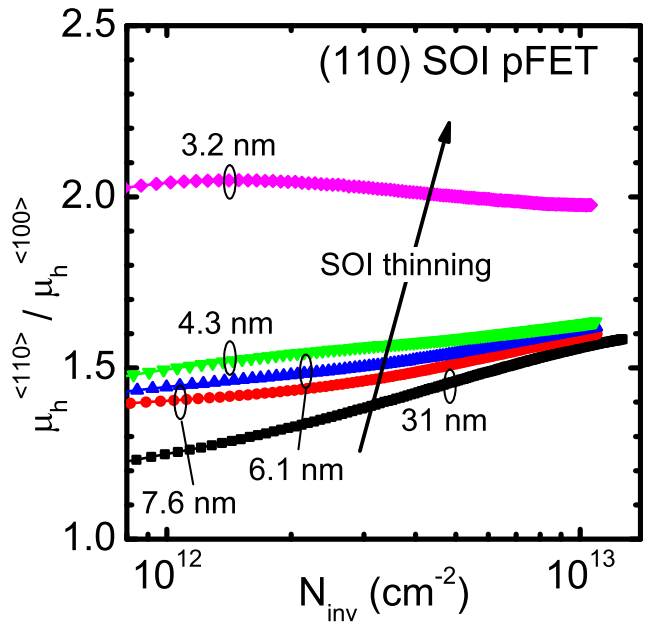


Fig.3.8 The μ_h ratio of <110> direction to <100> direction as a function of N_{inv}. As N_{inv} enlarges, the ratio also increases. Moreover, the ratio becomes larger as t_{SOI} becomes smaller. These results mean that the superiority of <110> direction over <100> direction becomes greater as the quantum confinement effect becomes more prominent.

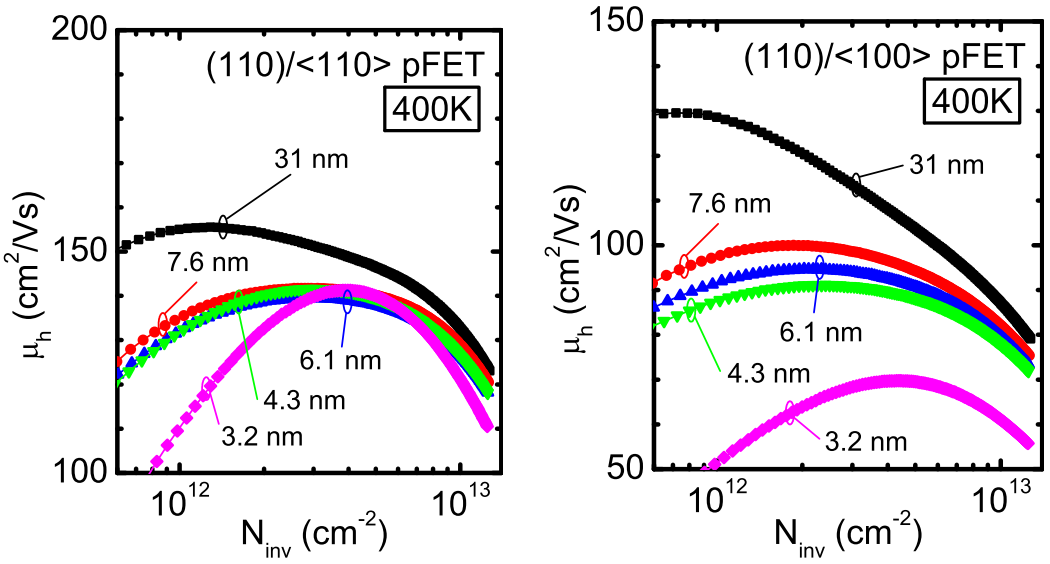


Fig.3.9 The N_{inv} dependence of μ_h for various t_{SOI} at 400 K. As temperature increases, the phonon scattering increases. As a result, degraded μ_h is observed. Especially μ_h with t_{SOI} of 3.2 nm pFET is severely degraded, because it benefits from the suppression of the inter-subband scattering at 300 K [34].

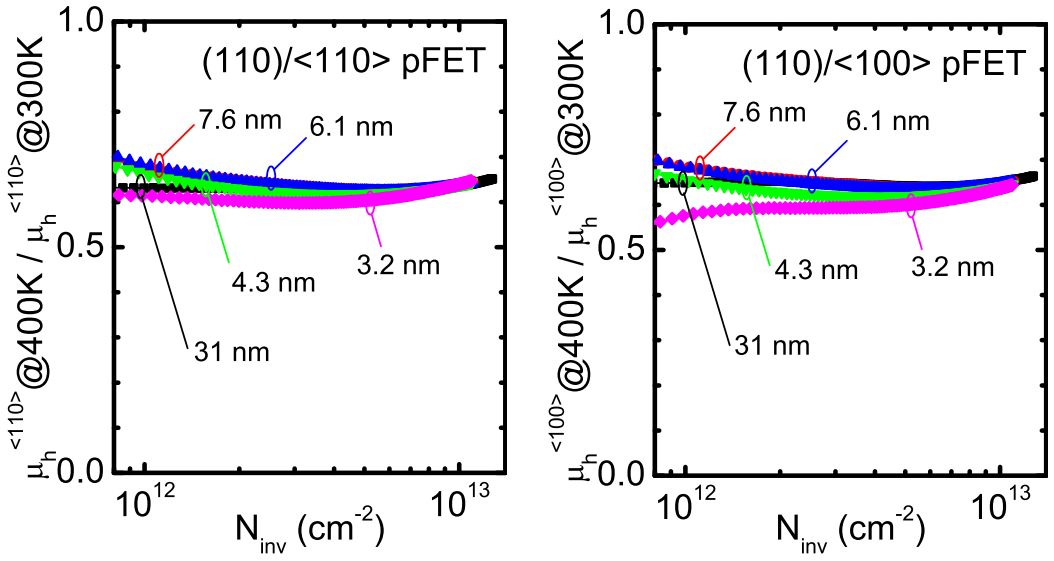


Fig.3.10 The ratio of μ_h at 300 K to μ_h at 400 K in the same direction. As μ_h can be described as $q<\tau>/m_c$, the ratio between different temperature eliminates m_c term in μ_h. Negligible difference between the ratio in <110> direction and the ratio in <100> direction can be seen, strongly suggesting that direction dependent behavior of μ_h is attributable to m_c, rather than $<\tau>$.

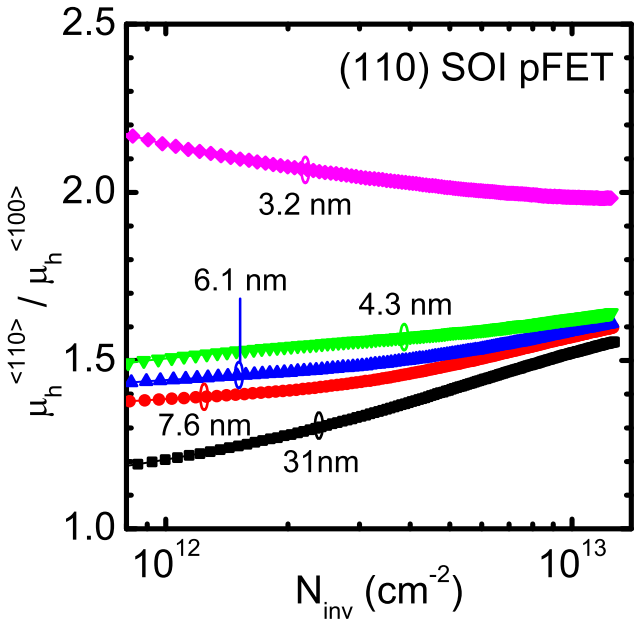


Fig.3.11 The μ_h ratio of <110> direction to <100> direction as a function of N_{inv} at 400 K. Comparing to the ratio at 300 K (Fig. 3.8), almost the same tendencies are found, indicating that the dependence of μ_h on N_{inv} and t_{SOI} is independent on temperature.

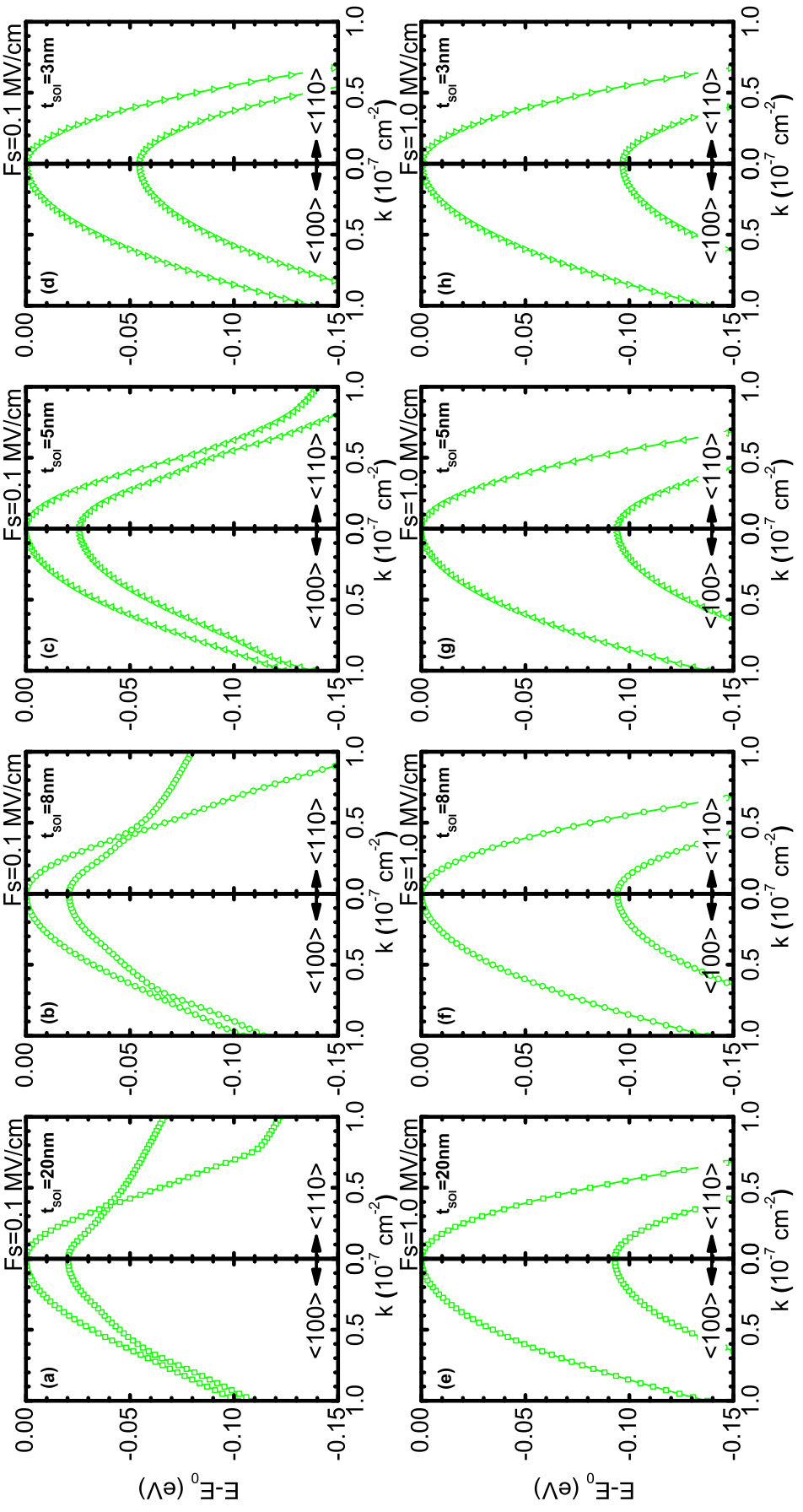


Fig.3.12 The E-k diagram under a triangular-well approximation for various t_{SOI} and F_s in (110) UTB pFETs: (a) t_{SOI}=20 nm, F_s=0.1 MV/cm (b) t_{SOI}=8 nm, F_s=0.1 MV/cm (c) t_{SOI}=5 nm, F_s=0.1 MV/cm (d) t_{SOI}=3 nm, F_s=0.1 MV/cm (e) t_{SOI}=20 nm, F_s=1.0 MV/cm (f) t_{SOI}=8 nm, F_s=1.0 MV/cm (g) t_{SOI}=5 nm, F_s=1.0 MV/cm (h) t_{SOI}=3 nm, F_s=1.0 MV/cm. Note that only the lowest two subbands are plotted to simplify the figures. It is interesting to point out that m_c of the second lowest subband becomes lighter by strengthening the quantum confinement effects. Therefore, the average m_c also decreases in thinner t_{SOI} or higher F_s especially in <110> direction, while smaller m_c change is observed in <100> direction (see also Fig. 3.13).

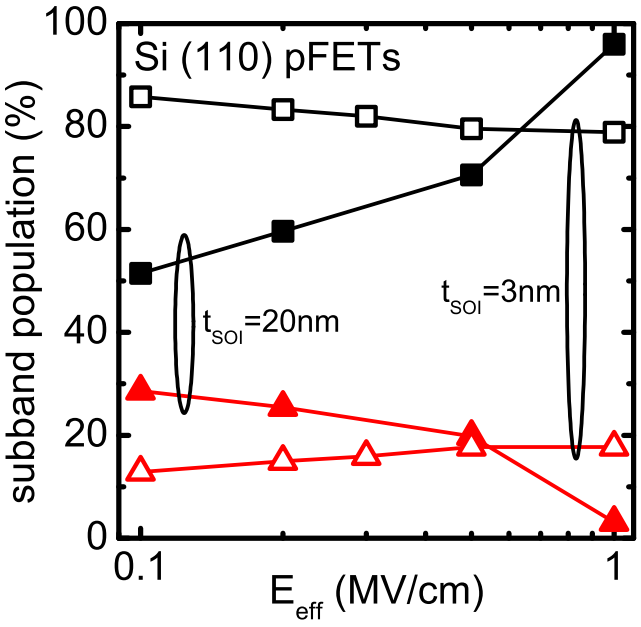


Fig.3.13 Calculated population of each subband with t_{SOI} of 20 nm and 3 nm for various F_s. While the population in the lowest subband increases as F_s increases in 20-nm case, it keeps almost constant in 3-nm case.

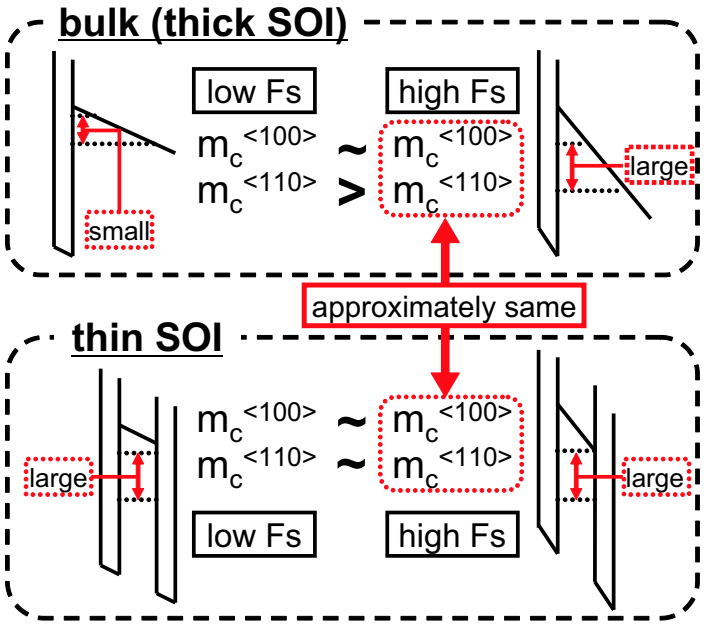


Fig.3.14 A schematic of dependence of m_c on F_s and t_{SOI}. Though average m_c in <100> direction is almost the same for all four conditions, average m_c in <110> direction is dependent on the strength of quantum confinement. i.e., average m_c in <110> direction becomes lighter as quantum confinement increases. The inter-subband scattering is also suppressed due to larger subband energy difference at high F_s and thin SOI.

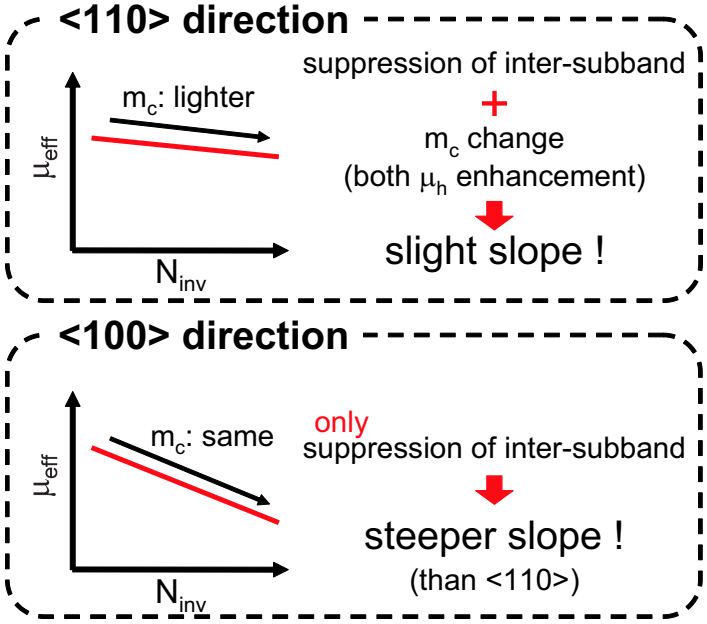


Fig.3.15 A schematic showing direction dependence of μ_h in thick SOI (or bulk). Average m_c in <110> direction decreases as N_{inv} becomes higher, while average m_c in <100> direction is almost independent of N_{inv}. Thus, μ_h in <110> direction keeps a high value even in a high N_{inv} region. Note that suppression of inter-subband occurs in both directions, resulting in less dependence of μ_h on N_{inv} than μ_h in Si (100).

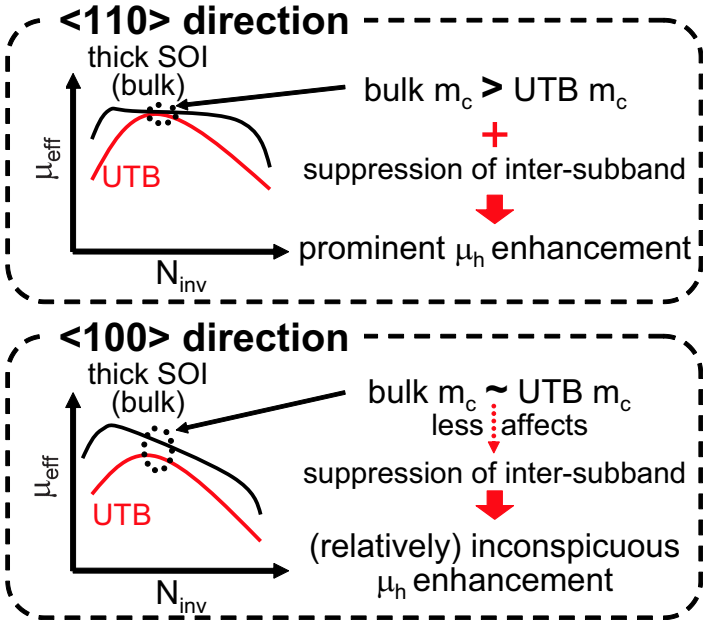


Fig.3.16 A schematic showing direction dependence of μ_h enhancement in (110) UTB pFETs. Both suppression of inter-subband and average m_c reduction contribute higher μ_h in <110> direction, while mainly the former mechanism does in <100> direction. As a result, μ_h enhancement in <110> direction is more prominent than μ_h in <100> direction (Figs. 3.6, 3.7).

Chapter 4

Hole Mobility Enhancement by Uniaxial Strain

4.1 Introduction

In chapter 3, the superiority of Si (110) pFETs has been confirmed. This superiority originates from the average m_c reduction by the quantum confinement effects caused by the surface electric field (F_s) and SOI thickness (t_{SOI}). Hole mobility (μ_h) in (110)/<110> is four times as high as that in (100)-oriented pFETs [37]. Even more, it is comparable to or higher than Ge μ_h in UTB structure [34].

However, the strain technology to boost up the mobility is widely utilized in state-of-the-art mass production, and a recent study shows hole mobility enhancement ($\Delta\mu/\mu$) in (110) pFETs is smaller than that in (100) pFETs [37–39, 48]. Therefore, the superiority of (110) pFETs is expected to be diminish with the strain technology. One paper experimentally shows that μ_h in (110) pFETs is comparable to that in (100) pFETs under a large amount of strain [49].

On the other hand, it is still unclear whether μ_h in (110) ultrathin body (UTB) pFETs with strain is higher than that in (100) UTB pFETs with strain or not. The strain effects on UTB pFETs which have strong quantum confinement effect are practically very important. So far, no experimental results on strained (110) UTB pFETs have been published, and the physical origin of the strain effects and the optimum strain direction are still unclear.

In this chapter, the effect of <110>- and <111>-directed uniaxial compressive strain ($\sigma_{<110>}$ and $\sigma_{<111>}$, respectively) on (110) UTB pFETs has been investigated. The origins of mobility enhancement by strain and its decrease in <110>-directed UTB pFETs are clarified. Moreover,

it is newly found that $\sigma_{<111>}$ shows larger mobility enhancement than $\sigma_{<110>}$ because of smaller density-of-state (DOS) change and larger conduction effective mass (m_c) change even in UTB pFETs with t_{SOI} of as thin as 3 nm, indicating that uniaxially strained <111>-directed UTB pFETs are promising device structures.

4.2 Experiments

The measured devices are (110)-oriented UTB pFETs with recessed channel. Both gate length and width are 200 μm , and the source and drain region were kept thick to minimize the parasitic resistance. A schematic of a fabricated UTB FET and its process flow can be found in Appendix A.1. Figure 4.1 shows measured inversion layer density (N_{inv}) dependence of μ_h for various t_{SOI} .

The uniaxial compressive strain was applied mechanically by a 4-point bending apparatus (Fig. 4.2). The strength of the strain is estimated as follows;

$$\sigma = \frac{ty}{2a(L/2 - 2a/3)}$$

where t, y, a, and L are the thickness of the wafer, the displacement, the distance between inner ridges, and the distance between outer ridges, respectively. Figure 4.2 schematically illustrates each parameter.

Considered are uniaxial strain configurations which enhance μ_h on (110) surface. $\sigma_{<110>}$ is applied to <110>- and <100>-directed pFETs, and $\sigma_{<111>}$ is applied to <111>-directed devices as schematically shown in Fig. 4.3.

The observed $\Delta\mu/\mu$ is as small as a few %, which calls for careful measurement. To perform an accurate measurement, the full Kelvin proves were equipped to measure $\Delta\mu/\mu$. The full Kelvin proves allow one to evaluate the electrical characteristics without the contact resistance variation between a prove and a pad.

Applied strain is at least one-decade smaller compared to the state-of-the-art strain degree in mass production. However, investigating the $\Delta\mu/\mu$ behavior at lower strain possibly gives us information on

- insights on physics behind carrier transport
- upper limit of $\Delta\mu/\mu$ under large amount of strain

It should be noted here that $\Delta\mu/\mu$ under large amount strain saturates. Therefore, by linear-extrapolating $\Delta\mu/\mu$ under small amount of strain, one obtains the upper limit of $\Delta\mu/\mu$.

4.3 <110> Uniaxial Compressive Strain Effects on (110) pFETs

4.3.1 <110> uniaxial compressive strain effects

It has been reported that $\sigma_{<110>}$ enhances μ_h in both <110>- and <100>-directed bulk pFETs [37, 41]. However, one remaining problem in strained (110) bulk pFETs is that $\Delta\mu/\mu$ by strain is highly dependent on N_{inv}, which is not observed in strained (100) bulk pFETs [37]. It has been reported that $\Delta\mu/\mu$ in <110> direction becomes smaller at larger N_{inv}, while $\Delta\mu/\mu$ in <100> direction is almost independent of N_{inv}.

Figure 4.4 shows $\Delta\mu/\mu$ at low N_{inv} of 1x10^{12} cm^{-2} and high N_{inv} of 1x10^{13} cm^{-2} as a function of $\sigma_{<110>}$. In <110> direction, $\sigma_{<110>}$ at low N_{inv} is larger than that at high N_{inv}, while $\Delta\mu/\mu$ is almost independent of N_{inv} in <100> direction. Figure 4.5 shows $\Delta\mu/\mu$ as a function of N_{inv} under 0.05 % $\sigma_{<110>}$. $\Delta\mu/\mu$ in <110> direction becomes smaller as N_{inv} becomes larger (i.e. stronger quantum confinement). Thus, it is speculated that the quantum confinement effect plays a significant role in $\Delta\mu/\mu$ by strain.

4.3.2 Quantum confinement effects on <110> strain

To study the quantum confinement effects on $\Delta\mu/\mu$ in detail, the dependence of $\Delta\mu/\mu$ by strain on substrate bias (V_{bs}) with t_{SOI} of 24 nm is shown in Fig. 4.6. Note that reverse V_{bs} strengthens F_s (and hence the quantum confinement) even at the same N_{inv}. It is interesting to point out here that V_{bs} dependence is different between <110>- and <100>-directed pFETs. $\Delta\mu/\mu$ slightly decreases in <110> direction (Fig. 4.6 (a)), while $\Delta\mu/\mu$ increases in <100> direction (Fig. 4.6 (b)).

Another method to strengthen quantum confinement effect is utilizing an UTB structure. The same trend can be seen in $\Delta\mu/\mu$ with t_{SOI} of 7.1 nm (Fig. 4.7 (a)). However, under much stronger confinement (t_{SOI} of 4.5 nm), $\Delta\mu/\mu$ is independent of a device direction and the dependence of N_{inv} is smaller (Fig. 7(b)). Under weak quantum confinement, $\Delta\mu/\mu$ in <110> direction is significantly different from that in <100> direction, while negligible $\Delta\mu/\mu$ difference is observed under strong quantum confinement.

4.3.3 Subband structure under <110> compressive strain

Physically, the following three parameters are modulated by strain:

(1) m_c

(2) subband energy difference (ΔE)

(3) carrier population in each subband

These are important parameters that determine mobility. Considering that ΔE and the carrier population are common in both directions, above experimental results strongly suggest the discrepancy in $\Delta\mu/\mu$ by $\sigma_{<110>}$ between <110> and <100> direction originates from the difference in m_c change (Δm_c).

To investigate physics behind the effect of strain on (110) pFETs in detail, subband structures were calculated by the six-band k·p framework with a triangular well approximation [45, 48]. The detailed calculation procedures can be found in Appendix B. Figure 4.9 shows equienergy lines with and without $\sigma_{<110>}$ under low F_s of 0.1 MV/cm and high F_s of 1.0 MV/cm. Under low F_s, m_c in <110> direction is modulated by such a small $\sigma_{<110>}$, while m_c in $\sigma_{<110>}$ direction at high F_s and m_c in <100> direction are not much modulated. These results are well-consistent with experimental results, in which higher $\Delta\mu/\mu$ in <110> direction at low F_s and smaller $\Delta\mu/\mu$ in other conditions are observed. Therefore, $\Delta\mu/\mu$ by $\sigma_{<110>}$ is thought to be direction-dependent.

Figure 4.10 shows the population of the lowest two subbands and Fig. 4.11 shows the ΔE between the lowest two subbands with and without 100 MPa $\sigma_{<110>}$. Slight difference in carrier population and increase in ΔE between the third lowest subband and the lowest subband can be seen. Note that the changes in the population and ΔE are common in both <110> and <100> directions and these changes enhance μ_h in both directions. On the other hand, the difference in $\Delta\mu/\mu$ between <110> and <100> directions is attributable to the difference in Δm_c, instead of population and ΔE.

Even though $\Delta\mu/\mu$ by $\sigma_{<110>}$ in <110> direction is high under weak quantum confinement, it is expected to be smaller as device size shrinks (i.e. higher F_s or thinner SOI, which leads to stronger quantum confinement). Therefore, it is strongly required to investigate the higher $\Delta\mu/\mu$ in (110)

pFETs.

4.4 <111> Uniaxial Compressive Strain Effects on (110) pFETs

4.4.1 <111> uniaxial compressive strain effects

It has been reported that in bulk pFETs, $\Delta\mu/\mu$ by $\sigma_{<111>}$ in <111> direction is larger than $\Delta\mu/\mu$ by $\sigma_{<110>}$ in <110> direction [37]. A recent theoretical study pointed out μ_h in <111> direction is comparable to μ_h in <110> direction under as large strain as 2 GPa in (110)-oriented bulk pFETs [48]. Thus, there is a possibility that in UTB structures, μ_h in <111> direction can surpass μ_h in <110> direction under large strain, even though μ_h in <111> direction without strain is inferior to μ_h in <110> direction.

Figure 4.12 shows $\Delta\mu/\mu$ in <111>-directed pFET with t_{SOI} of 24 nm as a function of $\sigma_{<111>}$. Clearly, $\Delta\mu/\mu$ by $\sigma_{<111>}$ is larger than $\Delta\mu/\mu$ by $\sigma_{<110>}$, as previously reported in bulk pFETs [37]. Figure 4.13 shows $\Delta\mu/\mu$ with t_{SOI} of 4.5 nm. It is experimentally confirmed that $\Delta\mu/\mu$ in <111> direction is still larger than $\Delta\mu/\mu$ in <110> direction. It is interesting to point out here that $\Delta\mu/\mu$ in <111> direction becomes smaller at higher N_{inv} or thinner SOI. This tendency of $\Delta\mu/\mu$ by strain is similar to $\Delta\mu/\mu$ in <110> direction, suggesting that Δm_c is also the key in mobility enhancement by $\sigma_{<111>}$.

4.4.2 Subband structure under <111> compressive strain

To investigate $\sigma_{<111>}$ effects, subband structures were calculated by the six-band k·p framework under a triangular well approximation. Figure 4.14 shows equienergy lines with and without 100 MPa $\sigma_{<111>}$ under low F_s of 0.1 MV/cm and high F_s of 1.0 MV/cm. Similar to equienergy lines with 100 MPa $\sigma_{<110>}$ (Fig. 4.9), Δm_c is larger at lower F_s. This behavior is quite consistent with the experimental results, and therefore, larger $\Delta\mu/\mu$ by $\sigma_{<111>}$ at lower F_s is also attributable to Δm_c.

4.5 Physical Understandings of Uniaxial Compressive Strain

Above experimental results can be summarized as shown in Fig. 4.15. In <110>- and <111>-directed bulk pFETs, Δm_c plays a role in $\Delta\mu/\mu$. The degree of Δm_c by strain depends on the

present amount of the quantum confinement, since the quantum confinement by F_s also contributes to Δm_c in (110) pFETs. Δm_c by strain under weak quantum confinement (low F_s) is larger than Δm_c under strong quantum confinement (high F_s). Thus, $\Delta\mu/\mu$ of <110>- and <111>-directed bulk pFETs decreases as the quantum confinement effects increase (higher N_{inv}).

In <100>-directed bulk pFETs, on the other hand, Δm_c is small and almost independent of the quantum confinement. Therefore, $\Delta\mu/\mu$ keeps constant regardless of N_{inv} . Similarly, the quantum confinement by the extremely thin SOI limits the Δm_c in UTB pFETs. As a result, $\Delta\mu/\mu$ in UTB pFETs is less dependent on N_{inv} than $\Delta\mu/\mu$ in bulk pFETs even in <110> or <111> directions.

4.6 Performance Estimation in UTB pFETs by Uniaxial Strain

So far, the strain effects under weak strain are discussed by measurements and calculations. In this section, to estimate $\Delta\mu/\mu$ under the state-of-the-art strain technology, subband structures (ΔE, population in each subband and Δm_c) under a high amount of strain have also been calculated by six-band k·p framework. Assumed are SOI thickness of as thin as 3 nm under 1 GPa $\sigma_{<110>}$ and $\sigma_{<111>}$. Note that t_{SOI} of as thin as 3 nm corresponds to the physical gate length of 12 nm, which is scheduled for the high performance logic transistor in 2017 [50]. F_s effect is also taken into calculation with a triangular well approximation.

4.6.1 <110> compressive strain effects on <110> UTB pFETs

reduction, which is a key in large $\Delta\mu/\mu$, is relatively small under $\sigma_{<110>}$ (Fig. 4.16 (a), (b)). Even though ΔE becomes large by strain (Fig. 4.17 (a)), it is very close to the optical phonon energy at room temperature and is expected to exhibit negligible difference with and without strain in terms of the suppression of inter-subband phonon scattering. The population modulation is negligibly small (Fig. 4.18 (a)). All of them leads to smaller $\Delta\mu/\mu$ in UTB pFETs than that in bulk pFETs. Thus, it is expected that strain will have a limited contribution to mobility enhancement in <110>-directed UTB pFETs.

4.6.2 <111> compressive strain effects on <111> UTB pFETs

In contrast to $\sigma_{<110>}$, $\Delta\mu/\mu$ is expected to be larger in $\sigma_{<111>}$. Relatively large Δm_c (Fig. 4.16 (c), (d)) is observed, though the ΔE (Fig. 4.17 (b)) and population (Fig. 4.18 (b)) are almost the same as those in $\sigma_{<110>}$. Thus, strained <111>-directed UTB pFETs have an advantage over strained <110>-directed UTB pFETs, and will obtain larger $\Delta\mu/\mu$ by strain.

4.7 Summary

<110> and <111> uniaxial compressive strain effects on (110) ultrathin body pFETs have been systematically investigated. It is clarified by measurements and calculations that the strain effect in <111>-directed ultra-thin body pFETs is larger than <110>-directed ultra-thin body pFETs due to larger conduction effective mass change.

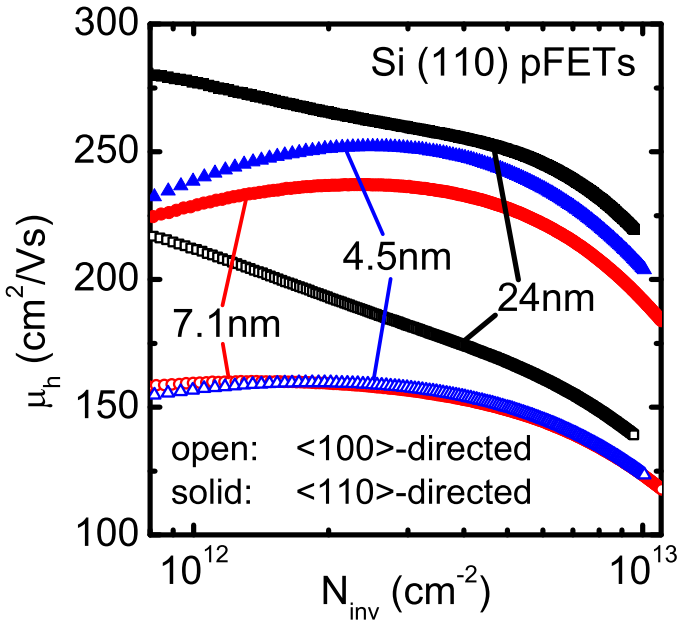


Fig.4.1 The N_{inv} dependence of μ_h for various t_{SOI}. μ_h enhancement with t_{SOI} of 4.5 nm is observed, as previously reported [34].

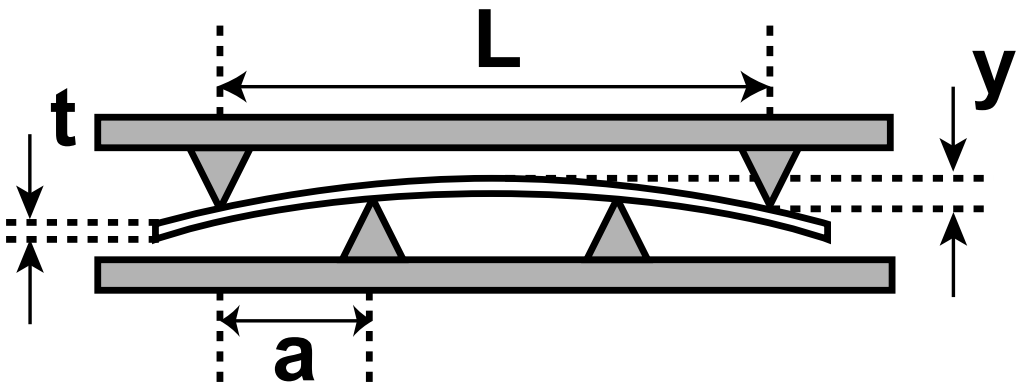


Fig.4.2 A schematics of a four-points mechanical bending apparatus utilized in this work. The amount of applied strain is estimated theoretically [51].

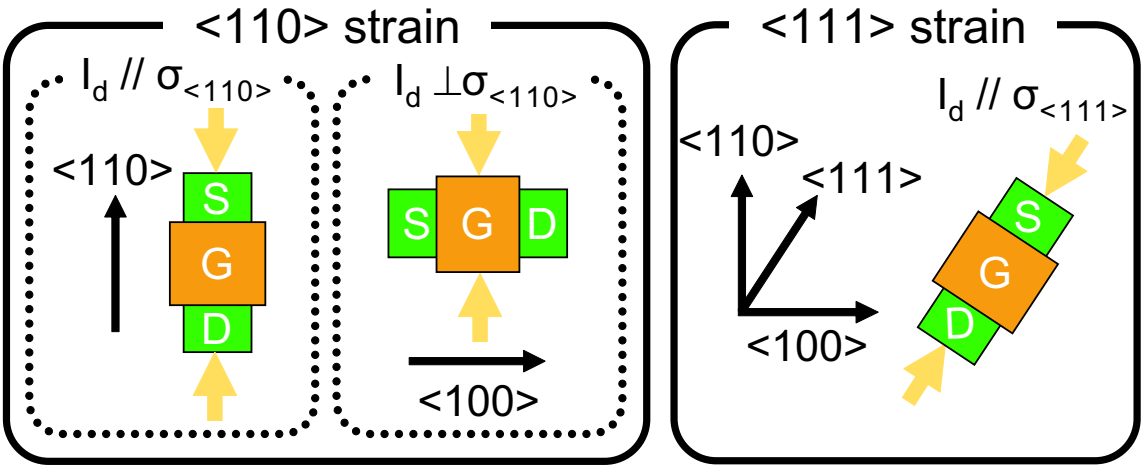
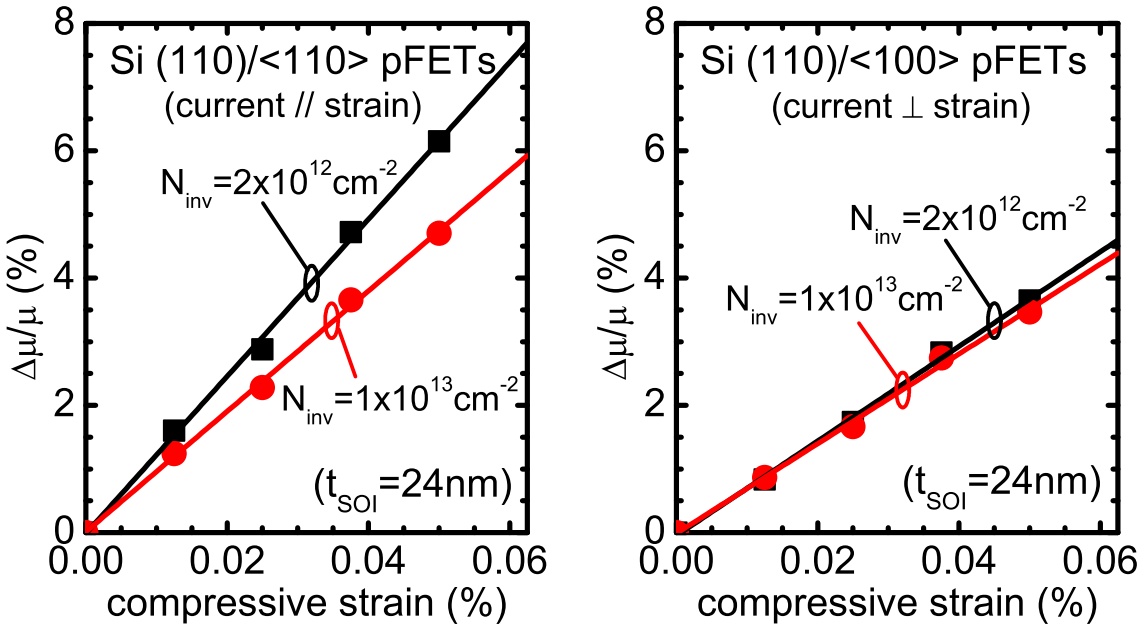


Fig.4.3 Schematics of considered strain configuration. Yellow arrows indicate the applied strain. Note that μ_h in both <110> and <100> directions is enhanced by <110>-directed uniaxial compressive strain.



(a) (b)

Fig.4.4 $\Delta\mu/\mu$ of (a) <110>-directed pFETs and (b) <100>-directed pFETs as a function of $\sigma_{<110>}$. $\Delta\mu/\mu$ becomes small at N_{inv} of 1x10^{13} cm^{-2} in <110> direction, while it is almost the same in <100> direction, as previously reported [37]. These results strongly suggest that quantum confinement is a key in $\Delta\mu/\mu$ by strain.

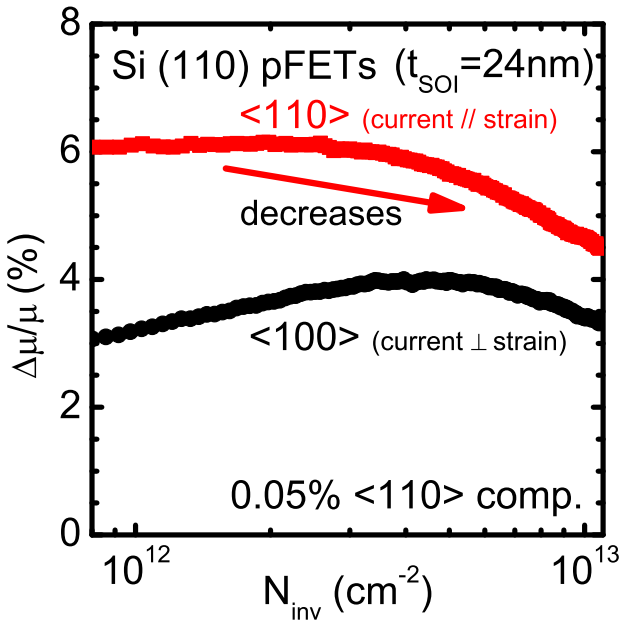
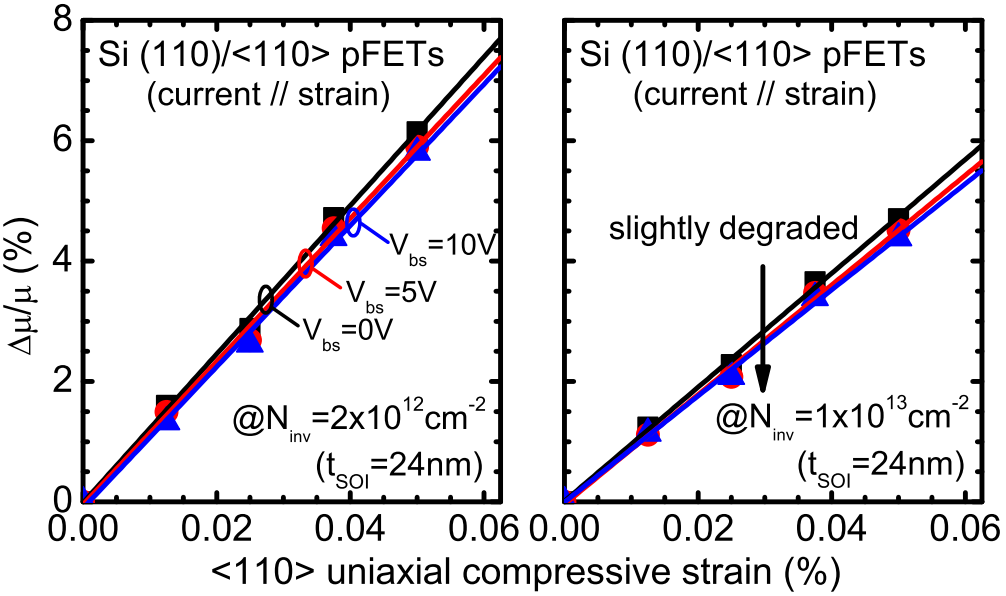
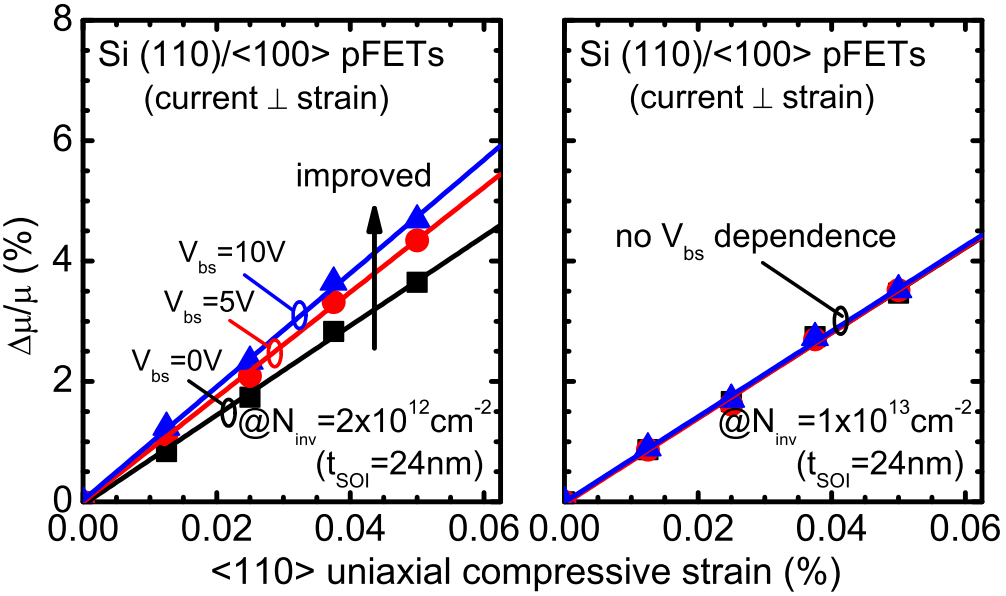


Fig.4.5 $\Delta\mu/\mu$ by $\sigma_{<110>}$ as a function of N_{inv}. In <110> direction, $\Delta\mu/\mu$ becomes smaller as N_{inv} becomes larger, while $\Delta\mu/\mu$ is almost independent of N_{inv} in <100> direction.

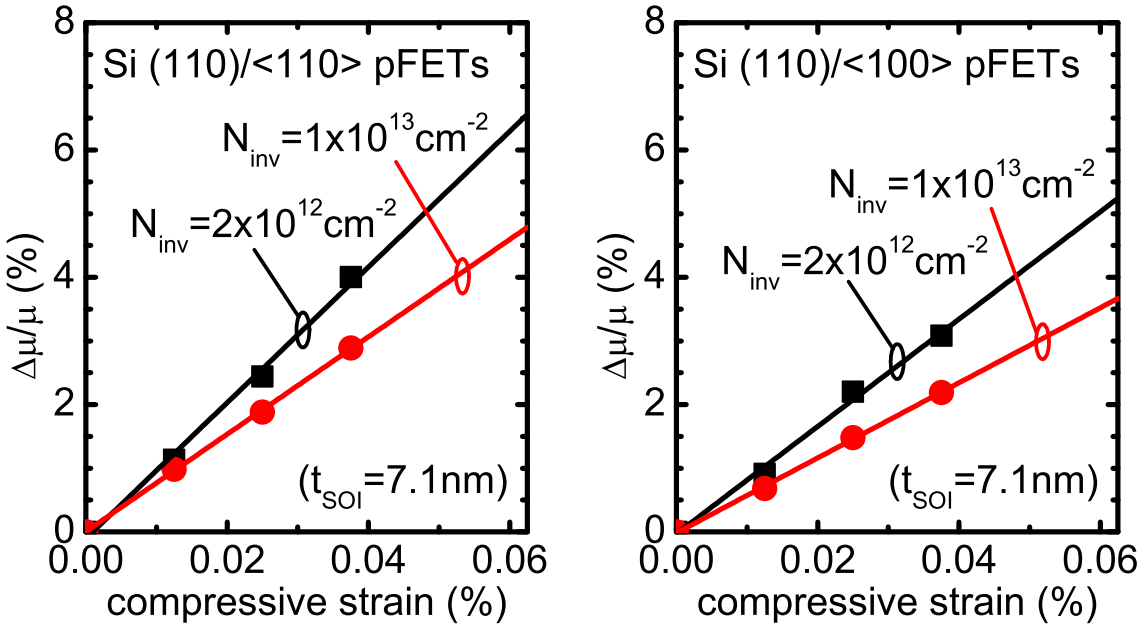


(a)



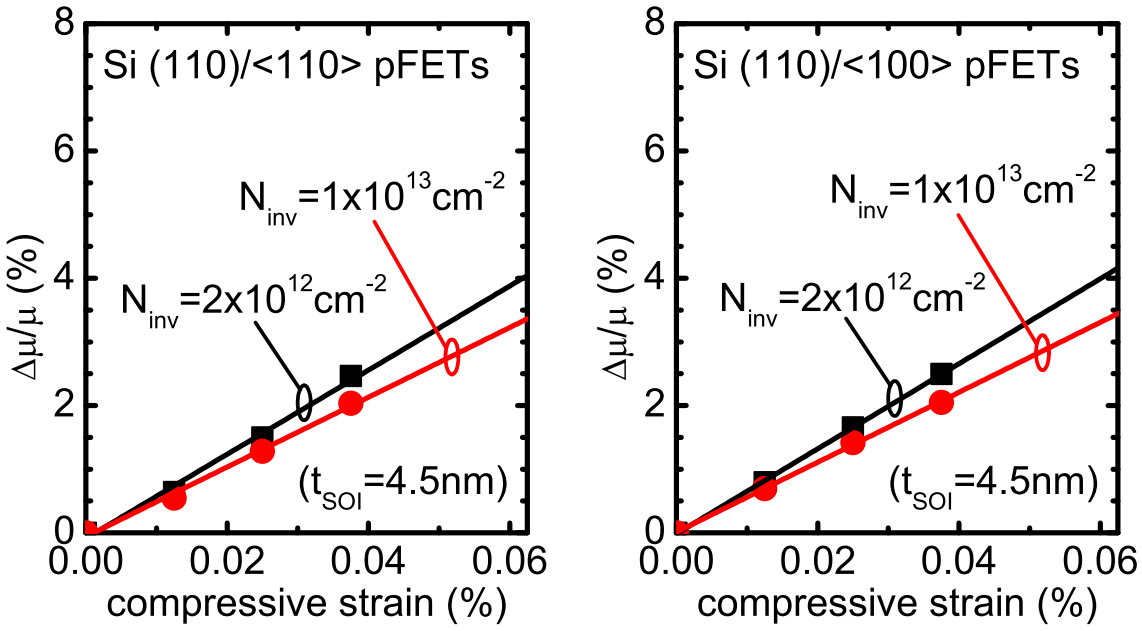
(b)

Fig.4.6 $\Delta\mu/\mu$ by $\sigma_{<110>}$ of (a) <110>-directed pFETs and (b) <100>-directed pFETs under reverse substrate bias as a function of $\sigma_{<110>}$. In <110>-directed pFETs, $\Delta\mu/\mu$ decreases as reverse substrate bias increases, while $\Delta\mu/\mu$ enlarges at N_{inv} of $2x10^{12}$ cm^{-2} in <100> direction. Considering that larger reverse substrate bias corresponds to higher surface electric field (or higher N_{inv}), these results are well-consistent with Fig. 4.5.



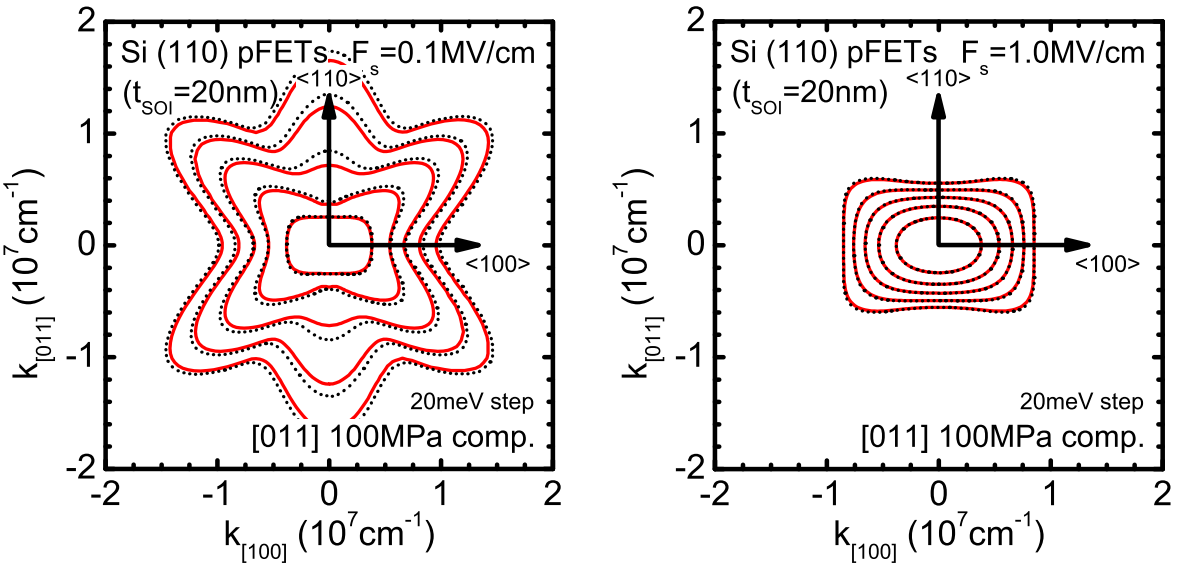
(a) (b)

Fig.4.7 $\Delta\mu/\mu$ of pFETs with t_{SOI} of 7.1 nm in (a) <110> direction and (b) <100> direction as a function of $\sigma_{<110>}$. In (b), $\Delta\mu/\mu$ is larger than $\Delta\mu/\mu$ with t_{SOI} of 24 nm (Fig. 4.4 (b)) in <100> direction at N_{inv} of $2x10^{12}$ cm^{-2}, while $\Delta\mu/\mu$ is smaller in (a) than $\Delta\mu/\mu$ with t_{SOI} of 24 nm in Fig. 4.4 (a).



(a) (b)

Fig.4.8 $\Delta\mu/\mu$ of pFETs with t_{SOI} of 4.5 nm in (a) <110> direction and (b) <100> direction as a function of $\sigma_{<110>}$. $\Delta\mu/\mu$ is smaller than 7.1 nm or 24 nm (Fig. 4.4) cases, as well as direction differences are small. This tendency is well consistent with experimental results in Fig. 4.5, namely the "moderate" quantum confinement enhances $\Delta\mu/\mu$ in <100>-directed pFETs.



(a) (b)

Fig.4.9 Equienergy lines of the lowest subbands with (red line) and without (dotted black line) 100 MPa uniaxial [011] stress under a triangular well of (a) F_s=0.1 MV/cm and (b) F_s=1.0 MV/cm. Δm_c can be seen in <110> direction at low F_s, while Δm_c is small at high F_s in both <110> direction and in <100> direction. Thus, larger $\Delta\mu/\mu$ in <110> pFETs at low N_{inv} (or low F_s) is attributable to larger Δm_c.

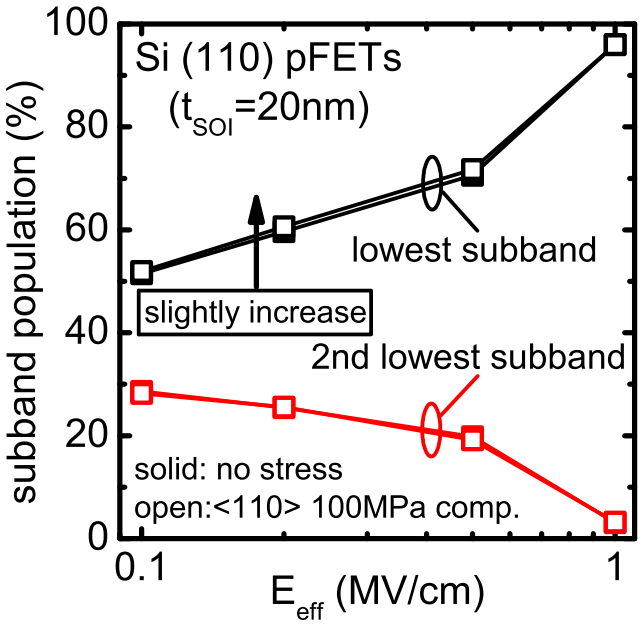


Fig.4.10 Subband population of the lowest and second lowest subband. Slightly increased population in the lowest subbands is also the origin of μ_h enhancement. Note that this mechanism is common in both <110> and <100> directions.

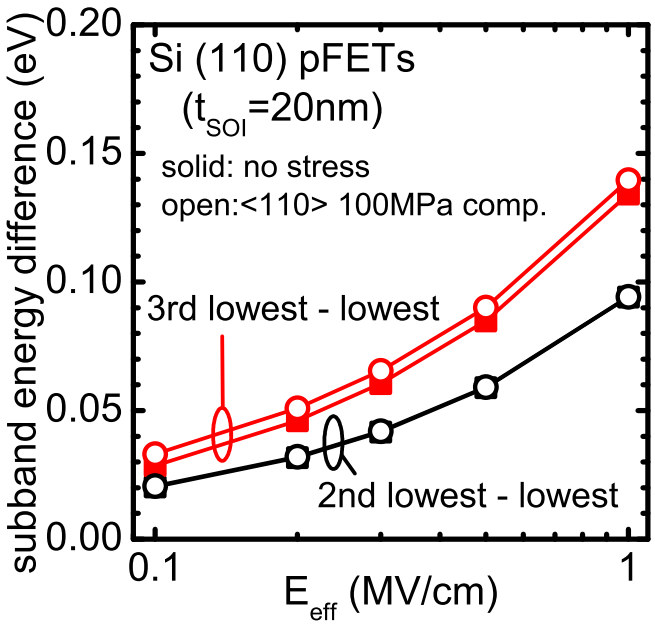


Fig.4.11 Subband energy splitting with (open) and without (solid) 100 MPa $\sigma_{<110>}$. Small difference between lowest and 2nd lowest subband can be seen, suggesting less effect of ΔE on $\Delta\mu/\mu$.

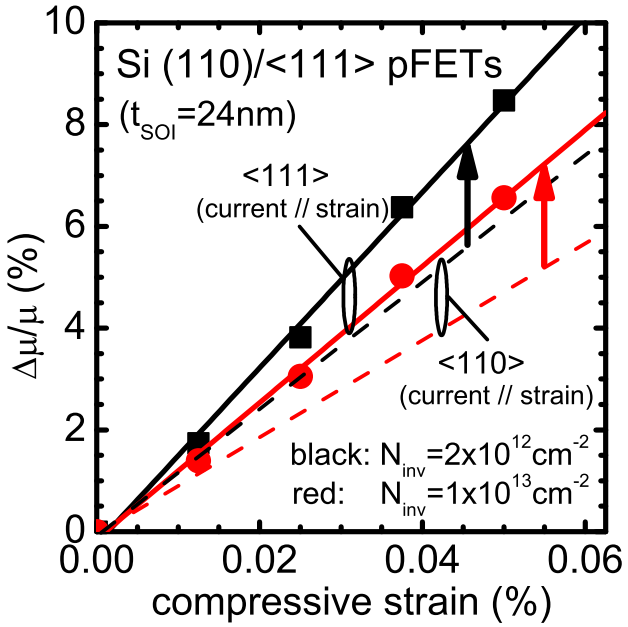


Fig.4.12 $\Delta\mu/\mu$ of <111>-directed pFETs with t_{SOI} of 24 nm. Similar to $\sigma_{<110>}$, higher N_{inv} results in smaller $\Delta\mu/\mu$ (Fig. 4.4). As previously reported [37, 41], $\Delta\mu/\mu$ of <111>-directed pFETs is larger than $\Delta\mu/\mu$ of <110>-directed pFETs.

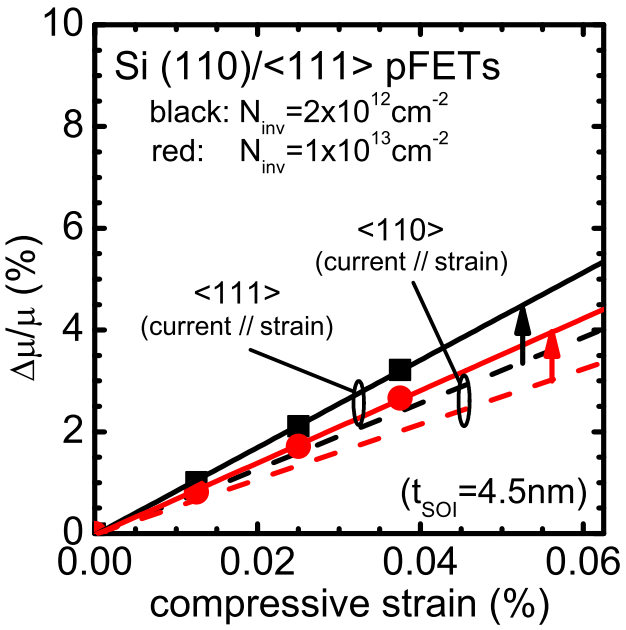
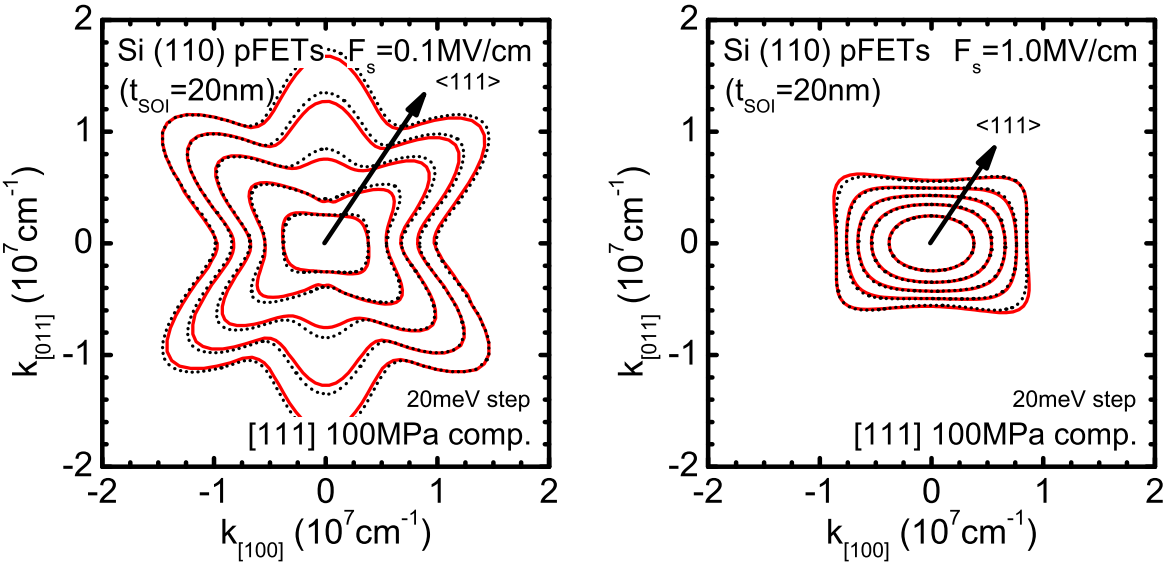


Fig.4.13 $\Delta\mu/\mu$ of <111>-directed pFETs with t_{SOI} of 4.5 nm. Similar to $\sigma_{<110>}$, thinner t_{SOI} results in smaller $\Delta\mu/\mu$. It is interesting to point out here that $\Delta\mu/\mu$ of <111>-directed pFETs is larger than $\Delta\mu/\mu$ of <110>-directed pFETs even in thin SOI case.



(a) (b)

Fig.4.14 Equienergy surface of the lowest subbands with (red line) and without (dotted black line) 100 MPa uniaxial [111] stress under a triangular well of (a) F_s=0.1 MV/cm and (b) F_s=1.0 MV/cm. Large Δm_c at low F_s can be seen, while $\Delta m_c$is small at high F_s. This difference is the origin of larger $\Delta\mu/\mu$ at low F_s than $\Delta\mu/\mu$ at high F_s.

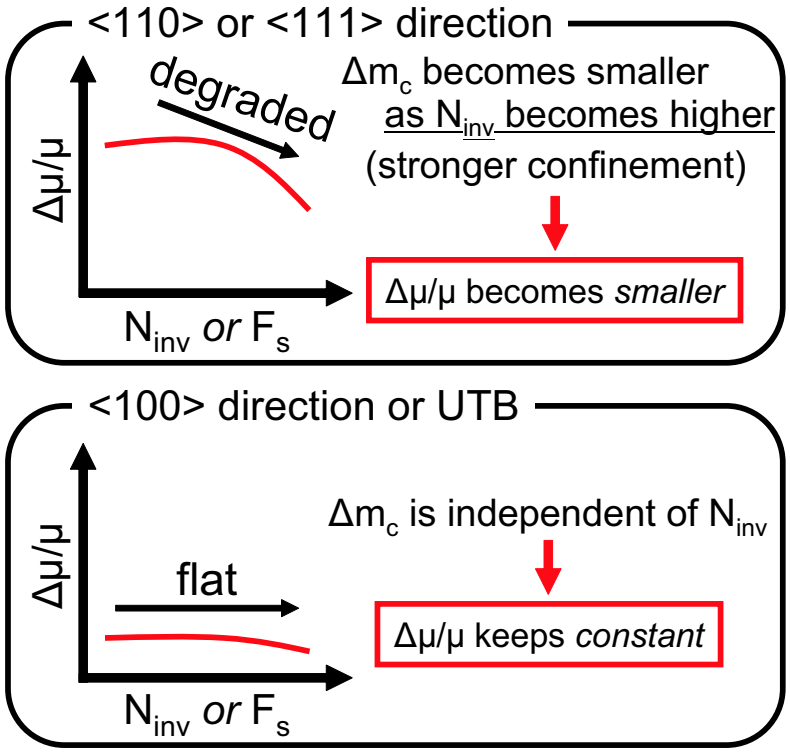


Fig.4.15 Schematics of different $\Delta\mu/\mu$ behavior by strain. In <110> or <111> directions, Δm_c decreases as N_{inv} increases while Δm_c is almost the same in <100> direction and in UTB pFETs. The difference in Δm_c results in different N_{inv} dependence.

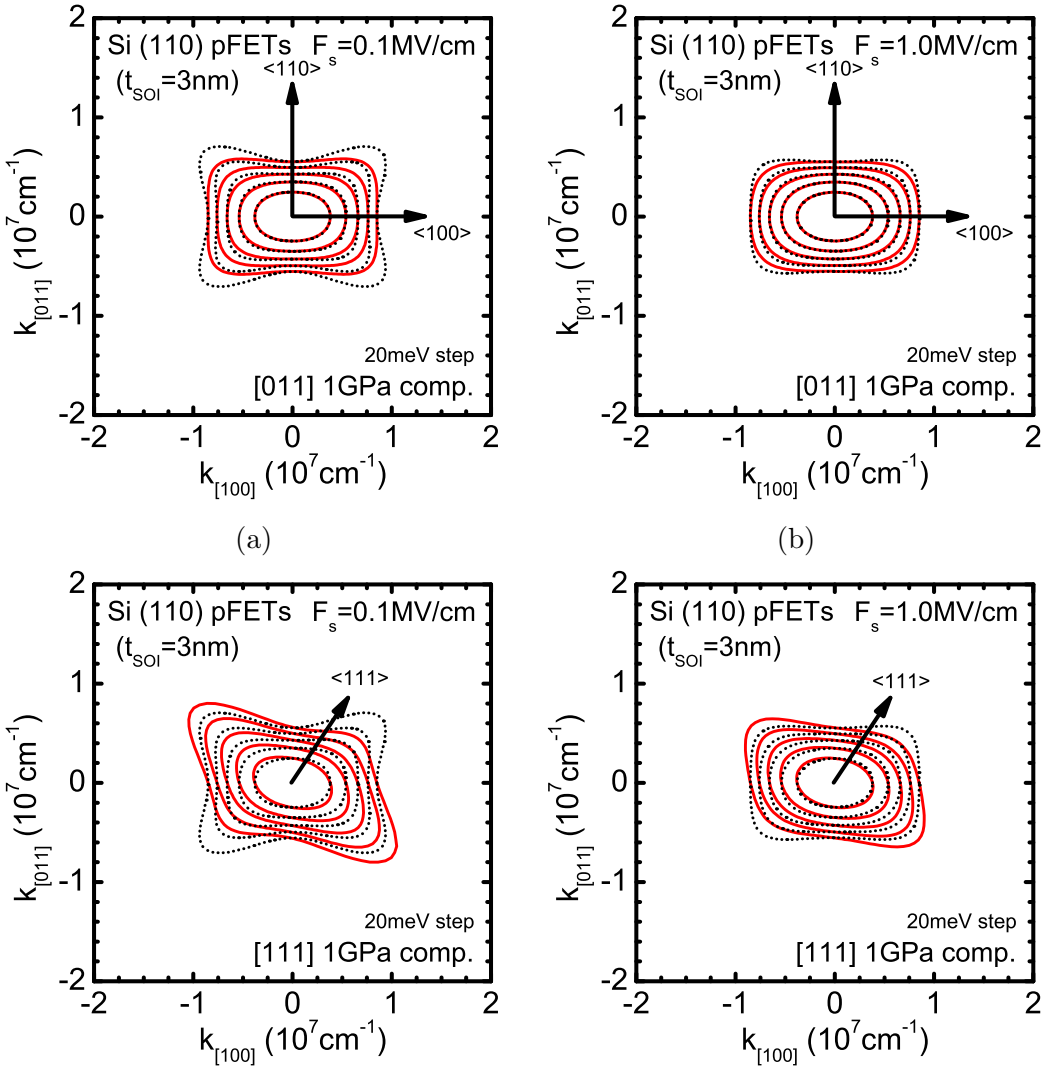
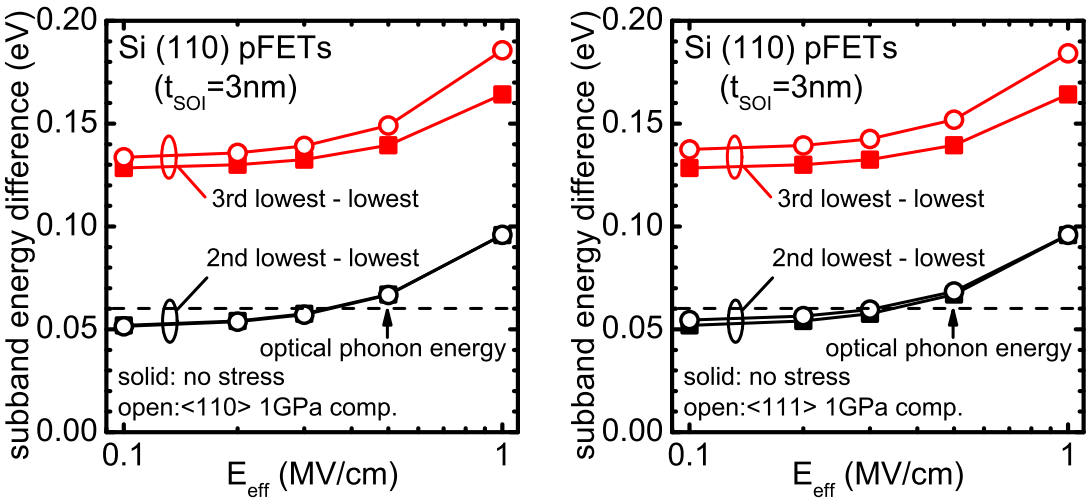
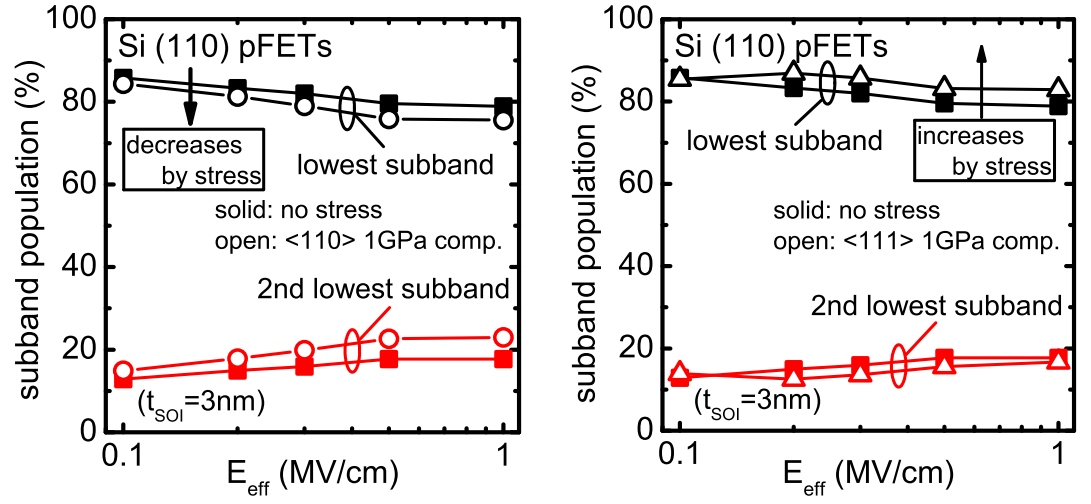


Fig.4.16 Equienergy surface of the lowest subbands with (red line) and without (dotted black line) 1 GPa uniaxial stress with t_{SOI} of 3 nm under a triangular well (a) F_s=0.1 MV/cm, [011] stress (b) F_s=1.0 MV/cm, [011] stress (c) F_s=0.1 MV/cm, [111] stress (d) F_s=1.0 MV/cm, [111] stress . In (a) and (b), Δm_c in both <110> and <100> directions is relatively small because of strong confinement by thin SOI. In contrast, larger Δm_c can be observed in <111> direction, which is an advantage of $\sigma_{<111>}$ over $\sigma_{<110>}$.



(a) (b)

Fig.4.17 Calculated subband energy splitting (a) under 1 GPa $\sigma_{<110>}$ and (b) under 1 GPa $\sigma_{<111>}$. ΔE becomes larger by stress, but it is close to or larger than optical phonon energy, indicating less effect of ΔE on $\Delta\mu/\mu$ regardless of stress.



(a) (b)

Fig.4.18 Calculated each subband population (a) under 1 GPa $\sigma_{<110>}$ and (b) under 1 GPa $\sigma_{<111>}$. Slightly decreased population at the lowest subband is observed in <110> direction, while increased population in <111> direction. These differences are caused by the ΔE and DOS modulation.

Chapter 5

Direction Dependence of Electron Mobility in (110) nMOSFETs

5.1 Introduction

In chapters 3 and 4, the superiority of (110) ultrathin body (UTB) pFETs has been confirmed. Even though the mobility enhancement by strain is smaller than those in (100) UTB pFETs, higher unstrained hole mobility (μ_{h}) can compensates that.

In terms of a CMOS integration, electron mobility (μ_{e}) in (110)-oriented UTB nFETs should be clarified. However, the physics behind (110) μ_{e} in UTB nFETs is not fully understood. One such problem is the direction dependence of μ_{e} in (110) surface. Even in bulk nFETs, it has been reported that the quantum confinement effect by the surface electric field ($\mathrm{F_s}$) changes the effective mass perpendicular to $\mathrm{Si/SiO_2}$ surface ($\mathrm{m_z}$) [52]. The mobility anisotropy, which means μ_{e} is different from one direction to another direction, is suppressed in a high inversion charge density ($\mathrm{N_{inv}}$) region, while the anisotropy is significant in a low $\mathrm{N_{inv}}$ region.

Therefore, it is speculated that an ultimately thin SOI must affect μ_{e} in UTB nFETs. However, no paper has focused on the direction dependence of μ_{e} in (110) surface. In this chapter, μ_{e} anisotropy in (110) UTB nFETs will be demonstrated. It is experimentally observed that μ_{e} in <110> direction is higher than μ_{e} in <100> direction in an ultimately thin SOI nFETs, though μ_{e} in <110> direction is smaller than μ_{e} in <100> direction in bulk or relatively thick SOI. The physical origin can be attributed to the non-parabolicity of the 2-fold valleys in <110> direction.

5.2 Device Structure and Experiments

To investigate μ_e anisotropy in (110) nFETs, a common channel structure was utilized. This structure shares completely the same channel in both <110> and <100> directions, which allows one to evaluate direction dependence of μ_e. The detailed process flow can be found in Appendix A.2, and the operation procedure can be found in chapter 3.

Figure 5.1 shows the comparison between μ_e by utilizing a normal FET structure and that by utilizing the common channel structure with relatively thick SOI. Almost identical μ_e in both directions means the validity of a common channel structure.

5.3 Direction Dependence of Electron Mobility

Figure 5.2 shows N_{inv} dependence of μ_e for various SOI thickness (t_{SOI}). As t_{SOI} becomes thinner, monotonic μ_e degradation is observed as previously reported [19,53]. In (110) bulk nFETs, it is well known that μ_e in <100> direction is higher than μ_e in <110> direction. This tendency is applicable when t_{SOI} is larger than 4.3 nm. However, when t_{SOI} is 3.2 nm, μ_e in <100> direction is smaller than μ_e in <110> direction.

To investigate in more detail, the ratio of μ_e in <100> direction to μ_e in <110> is derived and shown in Fig. 5.3. Though the ratio becomes larger as t_{SOI} decreases with t_{SOI} of larger than 4.3 nm, it sharply becomes smaller than unity with t_{SOI} of 3.2 nm. Obviously, the transport mechanism changes with t_{SOI} of 3.2 nm.

Figure 5.3 shows the μ_e ratio at N_{inv} of $8x10^{12}$ cm^{-2}, confirming that the μ_e ratio drops at t_{SOI} of 3.2 nm. Note that several data points can be seen at the same t_{SOI} because several devices were measured and plotted.

5.4 Physical Understandings of Direction Dependence of Electron Mobility

5.4.1 Effective mass approximation and its limitation in (110) nMOSFETs

Basic carrier transport can be understood by the effective mass theory. There are two types of energy ellipsoids; the 2-fold valley and the 4-fold valley. These two valleys have the opposite

characteristics (Fig. 5.5): In terms of m_z, the 2-fold valley has a lighter m_z than the 4-fold valley. In terms of in-plane effective mass (m_c), the 2-fold valley has a lighter m_c in the <110> direction than the 4-fold valley, while the 4-fold valley has a lighter m_c in the <100> direction. In terms of the density-of-states mass, the 2-fold valley has a larger value than the 4-fold valley. The heavier m_z of the 4-fold valley leads to higher carrier population in the 4-fold valley. m_c of the 4-fold valley in <100> direction is lighter than that in <110> direction, leading to higher μ_e in <100> direction [52].

However, the effective mass approximation is not valid in a high N_{inv} region (and hence, higher surface electric field, F_s) even in bulk nFETs [52]. The effective mass approximation is based on the assumption that the band structure is parabolic near the band minima. In (110) surface, the conduction band structure in the <110> direction is not parabolic, especially with the energy larger than 0.1 eV above the conduction band minima [52, 54, 55]. It has been reported that a subband with such a energy is occupied with N_{inv} of larger than $2x10^{12}$ cm^{-2}. Therefore, in a higher N_{inv} region, m_z of the 2-fold valley becomes heavier because of the "non-parabolicity", which means the invalidity of the effective mass approximation. As a result, the subband energy difference between the 4-fold valley and the 2-fold valley becomes closer, resulting in weaker μ_e anisotropy [52].

5.4.2 Physical origin of higher electron mobility in <110> direction in UTB nMOSFETs

The keys to understand experimental results are the non-parabolicity in the 2-fold valley and the modulation of m_z of the 2-fold valley by quantum confinement effect.

SOI thickness dependence of electron mobility ratio

At thick SOI case (t_{SOI} = 31 nm) or thin SOI case (t_{SOI} > 4.3 nm), μ_e behavior is close to bulk nFETs results. Superior μ_e in <100> direction to μ_e in <110> direction originates from the lighter m_c in <100> direction of the 4-fold valley. Subband energy increase by SOI layer confinement results in larger μ_e ratio, since the population in the 4-fold valley becomes larger as SOI becomes thinner.

At ultimately thin SOI case (t_{SOI} = 3.2 nm), non-parabolicity dominates μ_e. Because of the heavier m_z of the 2-fold valley, the subband energy difference between the 2-fold valley the 4-fold valley becomes very close. A larger occupation in the 2-fold valley is expected to be observed because of both heavier m_z and the larger density-of-states mass of the 2-fold valley.

Above explanation is summarized in Fig. 5.6. A recent theoretical calculation result shows that the effective mass approximation is invalid with t_{SOI} of less than 4 nm [56], supporting the physical explanation above.

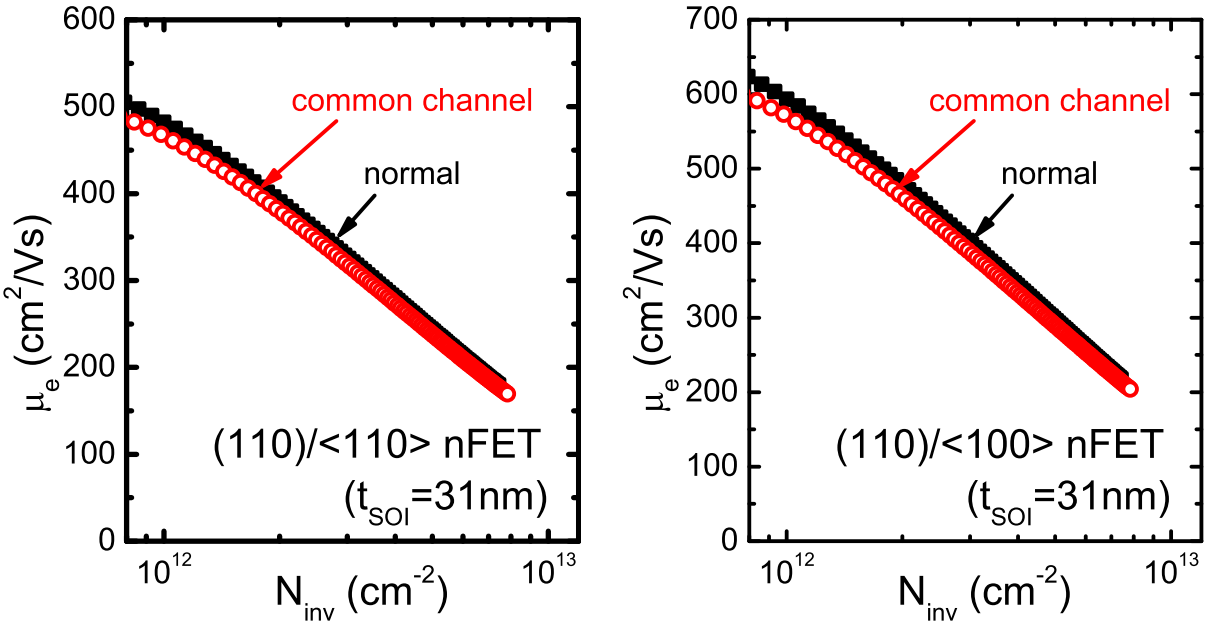
Inversion layer density dependence of electron mobility ratio

At thick SOI case (t_{SOI} = 31 nm) or thin SOI case (t_{SOI} > 4.3 nm), the behavior of μ_e ratio can be understood by the same framework as bulk nFETs. Gradually reduced μ_e ratio as increasing N_{inv} in Fig. 5.3 is attributable to increased carrier population in the 2-fold valley, originating from the non-parabolicity in the 2-fold valley.

At ultimately thin SOI case (t_{SOI} = 3.2 nm), subband energy is rarely affected by surface electric field because of strong structural confinement by SOI layer. On the other hand, higher N_{inv} means more carriers in the channel. Hence, not only the ground state (2-fold valley), but also the excited state (4-fold valley) is occupied by increasing N_{inv}. This leads to weaker anisotropy of μ_e or μ_e ratio closer to unity as increasing N_{inv} (Fig. 5.3).

5.5 Summary

It is experimentally demonstrated that electron mobility in <110> direction is higher than that in <100> direction in an ultimately thin SOI nFETs. Therefore, without any performance degradation, a CMOS operation is realized by utilizing both <110>-directed ultrathin body n- and pFETs.



(a) (b)

Fig.5.1 A comparison of extracted μ_e between normal FETs and common channel FETs with thick t_{SOI} (=31 nm). In both directions, almost the same μ_e is obtained, strongly indicating the validity of a common channel structure. Though some μ_e degradation is observed, this degradation might be attributed to the series resistance under the side-gate.

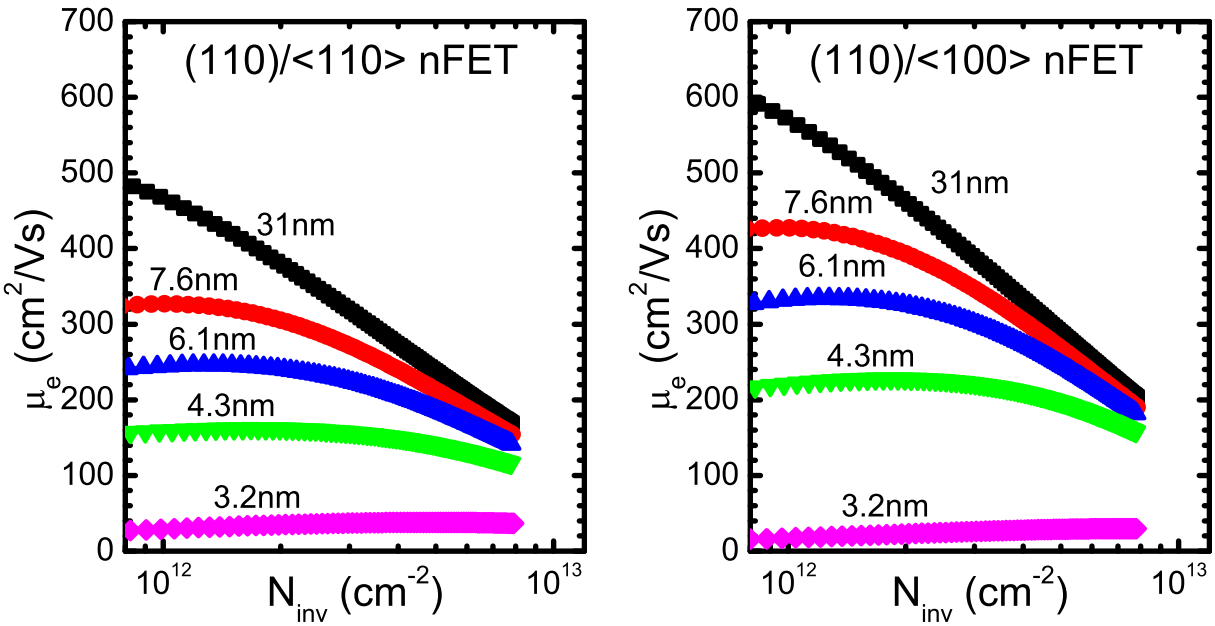


Fig.5.2 The N_{inv} dependence of μ_e for various t_{SOI}. As has already reported in previous works [19, 53], monotonic μ_e degradation is observed as t_{SOI} becomes thinner. It is well known that μ_e in <100> direction is higher than μ_e in <110> direction in (110) bulk nFETs. However, μ_e in <110> direction is larger than μ_e in <100> with t_{SOI} of 3.2 nm.

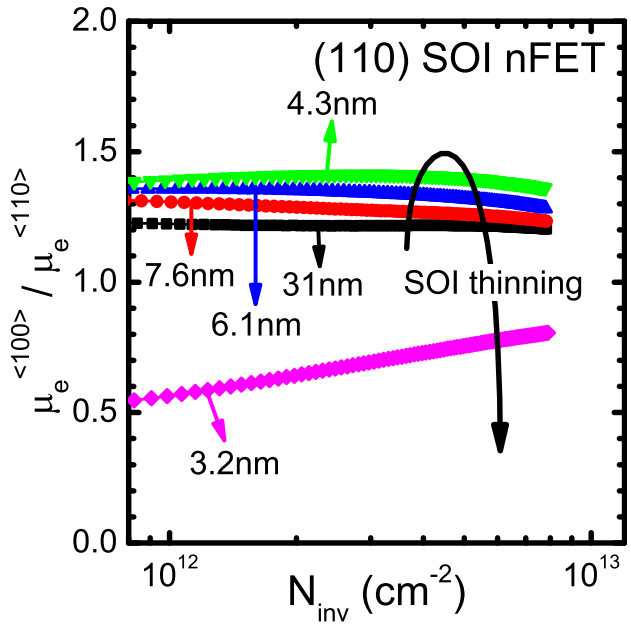


Fig.5.3 μ_e ratio of <100> direction to <110> as a function of N_{inv}. As t_{SOI} becomes thinner, the ratio becomes larger. However, the ratio sharply becomes smaller with t_{SOI} of 3.2 nm. It is interesting to point out here that μ_e in <100> direction is smaller than μ_e in <110> direction with t_{SOI} of 3.2 nm, though μ_e in <100> direction is larger than μ_e in <110> direction in other conditions.

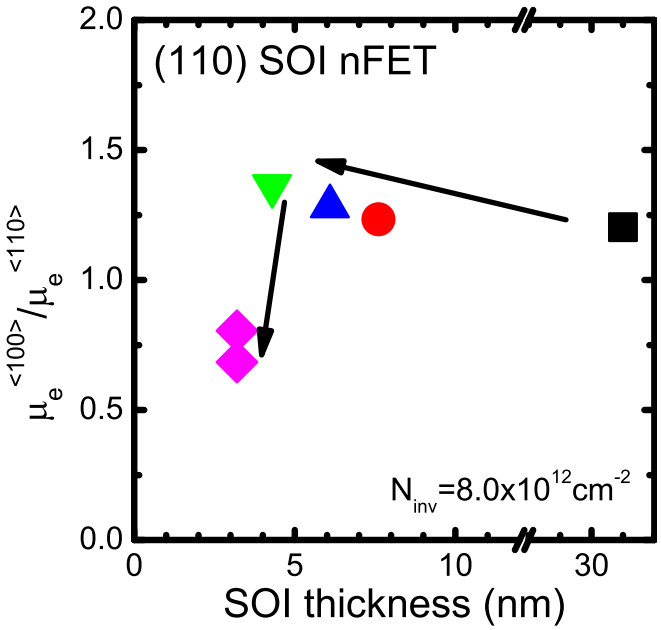


Fig.5.4 The t_{SOI} dependence of μ_e at N_{inv} of $8x10^{12}$ cm^{-2}. Clear μ_e ratio degradation is confirmed. Note that several devices were measured and corresponding data points are plotted.

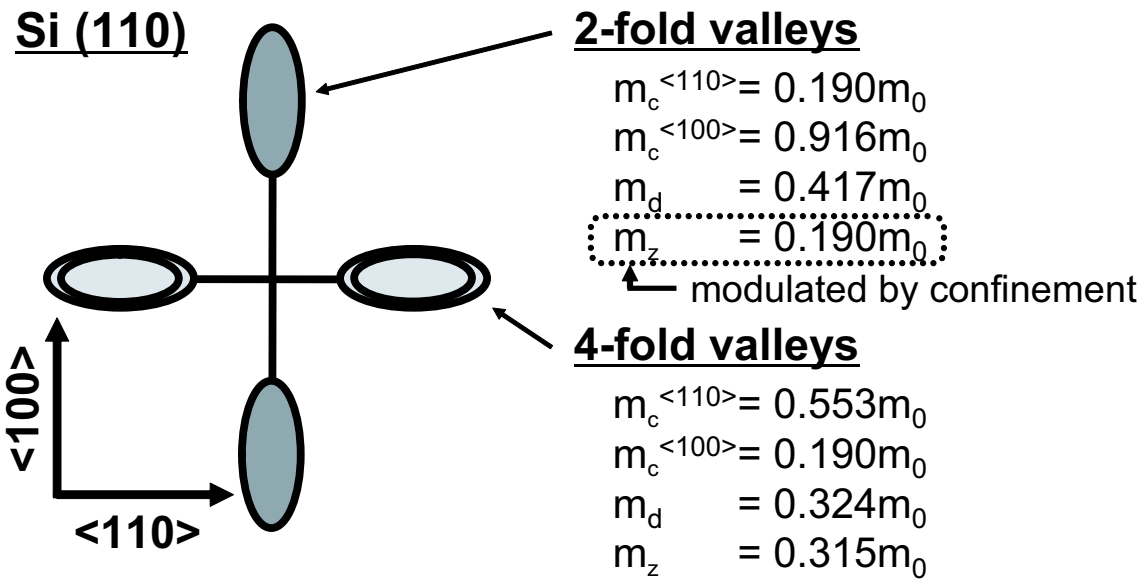


Fig.5.5 A schematic of energy valleys in Si (110). Basically, 4-fold valleys have larger m_z (and occupation) than 2-fold valleys. Thus, μ_e in <100> direction is higher than μ_e in <110> direction, reflecting the anisotropy of m_c. m_0 denotes the free electron mass.

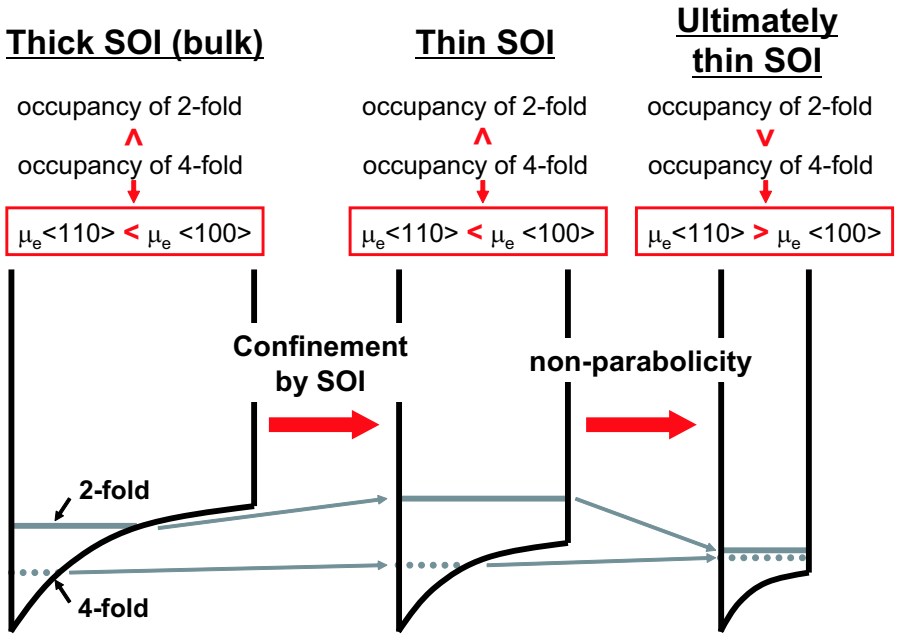


Fig.5.6 Schematic diagrams of subband energy modulation as a function of t_{SOI}. At relatively weak confinement region (thick SOI and thin SOI case), non-parabolicity is not prominent; Subband energy difference between the 4-fold and the 2-fold valley becomes larger, resulting in larger ratio of μ_e in <100> direction to μ_e in <110> direction. However, at strong confinement region (ultimately thin SOI), m_z of the 2-fold valley becomes heavier, resulting in larger occupation in the 2-fold valley, and hence, smaller ratio of μ_e in <100> direction to μ_e in <110> direction than unity.

Chapter 6

Electron Mobility Enhancement by Strain

6.1 Introduction

In chapter 5, it has shown that the electron mobility (μ_e) in <110> direction surpass μ_e in <100> direction in ultlathin body (UTB) nFETs, suggesting the possibility of a high performance CMOS operation with both n- and pFETs in the same direction (<110> direction) on (110) surface.

On the other hand, μ_e in (110) is well known to have lower mobility than μ_e in (100), which would limit the CMOS performance in Si (110) surface. However, it has been reported that the strained μ_e in (110) nFETs can surpass universal mobility, namely μ_e in (100) nFETs [52]. In addition, δt_{SOI} scattering degrades μ_e in UTB nFETs. Therefore, the strain technology in (110) UTB nFETs is a key, which has been discussed only by theory so far [57].

In this chapter, mobility enhancement ($\Delta\mu/\mu$) in (110)-oriented UTB nFETs under uniaxial stress has been experimentally investigated. It is newly found that stress engineering is still effective in UTB nFETs even if SOI thickness (t_{SOI}) is less than 4 nm.

6.2 Device Fabrication and Experimental Setup

The devices were fabricated on a (110) oriented SOI wafer. Selective SOI thinning was performed followed by a conventional SOI mesa process. Both gate length and width are 200 μm. The detailed process flow can be found in Appendix A.1. Figure 6.1 shows unstrained μ_e as a function of the inversion layer density (N_{inv}) in UTB nFETs. Monotonic μ_e degradation with decreasing t_{SOI} in both <110> and <100> directions was observed. These results are consistent with previous reports [19, 53].

μ_e in both <110> and <100> directions was extracted using the split capacitance-voltage (C-V)

measurement. Uniaxial tensile strain was applied mechanically using a 4-point bending apparatus as shown in Fig. 4.2 (chapter 4). Considered are the tensile strain of longitudinal to and transverse to the channel as shown in Fig. 6.2. The detailed strain application procedure can be found in chapter 4.2. The strength of the strain was carefully measured and calibrated by referring to a previous report on $\Delta\mu/\mu$ in (110) bulk nFETs [37].

Although the corresponding strain is relatively small, experimental $\Delta\mu/\mu$ gives the information on physics behind strain, and allows us the rough estimation of mobility under large amount of strain.

6.3 Longitudinal Uniaxial Tensile Strain on (110) nFETs

It has been reported that the longitudinal uniaxial tensile strain enhances μ_e in (110) surface in both <110> and <100> directions [37]. Figure 6.3 shows $\Delta\mu/\mu$ as a function of applied uniaxial tensile strain in UTB nFETs with thick t_{SOI} of 21 nm. Here, $\sigma_\perp$ and $\sigma_{//}$ denote the strain perpendicular to the channel direction, and strain parallel to the channel direction, respectively. For both directions, $\sigma_{//}$ enhances mobility while $\sigma_\perp$ degrades. These tendencies are consistent with the bulk piezo-resistance coefficients [36] and those in bulk nFETs [52].

Figure 6.4 shows $\Delta\mu/\mu$ as a function of applied uniaxial tensile strain in UTB nFETs with t_{SOI} of 7.1 nm. The tendencies of $\Delta\mu/\mu$ are the same as thick devices in Fig. 6.3; the longitudinal strain enhances μ_e, while the transverse strain degrades μ_e in both directions. Compared to $\Delta\mu/\mu$ in bulk-like nFETs, $\Delta\mu/\mu$ is slightly smaller.

It should be noted here that the absolute value of $\Delta\mu/\mu$ by the uniaxial tensile strain in <110> direction is smaller than that by the uniaxial tensile strain in <100> direction. This is because the subband energy difference between the 2-fold and the 4-fold valleys is enlarged by the <100> strain, while it is reduced by the <110> strain, as previously discussed in bulk nFETs [52].

Figure 6.5 shows $\Delta\mu/\mu$ as a function of applied uniaxial tensile strain in UTB nFETs with as thin t_{SOI} as 3.6 nm. Even in such a thin SOI, μ_e enhancement by uniaxial tensile strain is confirmed; the longitudinal uniaxial tensile strain enhances μ_e in (110)-oriented UTB nFETs. $\Delta\mu/\mu$ by uniaxial tensile strain is almost the same as that in UTB nFETs with t_{SOI} of 7.1 nm.

The noteworthy difference between 7.1 nm nFETs and 3.6 nm nFETs are the direction dependence of $\Delta\mu/\mu$ by strain. In 7.1 nm nFETs, $\Delta\mu/\mu$ by the <100>-directed uniaxial tensile strain is larger

than that by the <110>-directed uniaxial tensile strain, while $\Delta\mu/\mu$ by the <100>-directed strain and that by the <110>-directed strain are almost the same in 3.6 nm nFETs.

6.4 Physical Understandings of Uniaxial Tensile Strain

The above experimental results can be summarized as follows;

(1) $\Delta\mu/\mu$ by strain slightly decreases as t_{SOI} decreases.

(2) direction dependence of $\Delta\mu/\mu$ by strain weakens as t_{SOI} decreases.

The keys to understand physics behind above results are:

(1) enlargement of subband energy difference (ΔE) by the SOI layer.

(2) opposite trend of the strain-induced ΔE (<100>-directed tensile strain enlarges ΔE, while <110>-directed tensile strain reduces ΔE.)

Figure 6.6 shows the schematic of ΔE by strain in bulk FETs and UTB FETs. In UTB FETs, an extremely thin SOI enlarges ΔE, meaning less inter-subband scattering. Even if ΔE by strain is supposed to be the same in bulk and UTB FETs, ΔE by strain will less contribute to the suppression of inter-subband scattering in UTB FETs. As a result, $\Delta\mu/\mu$ by strain in UTB nFETs is slightly degraded as t_{SOI} decreases.

The weaker direction dependent $\Delta\mu/\mu$ by strain can also be understood by above theory. Direction dependent $\Delta\mu/\mu$ by strain has been explained by the sign of ΔE [52]; tensile strain in <100> direction enlarges ΔE while that in <110> direction reduces. However, as t_{SOI} decreases, ΔE by strain is thought to lose its impact on suppression of the inter-subband scattering. Therefore, the weaker direction dependence of $\Delta\mu/\mu$ is observed.

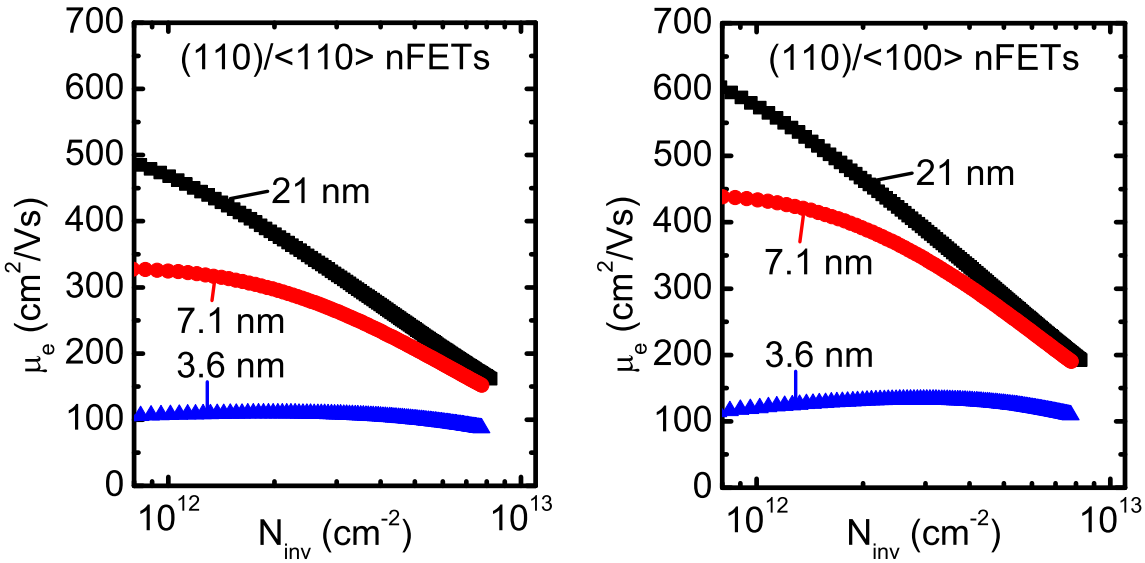
Both of above experimental results imply that the m_c change contributes more to μ_e enhancement, rather than the enlargement of ΔE, since ΔE by strain is thought to have less effects on mobility enhancement/degradation in nFETs with thin t_{SOI}.

A recent theoretical study based on the subband structure analysis by empirical pseudo potential method shows that the mobility enhancement by strain in (110)-oriented UTB nFETs is understood by ΔE only, and therefore, it is smaller than that in bulk nFETs [57]. However, these experimental

results clearly shows the important role of m_c in $\Delta\mu/\mu$ by strain, strongly suggesting that the m_c change by strain should be taken into consideration to model μ_e in (110)-oriented UTB nFETs.

6.5 Summary

Mobility enhancement in (110)-oriented ultrathin body nFETs was experimentally demonstrated. It is found that stress engineering is still effective in such thin UTB nFETs and that the mobility enhancement not only by the enlargement of subband energy difference, but also by the effective mass change, should be considered for accurate electron mobility modeling in (110)-oriented UTB nFETs.



(a) (b)

Fig.6.1 The N_{inv} dependence of μ_e (a) in <110> direction and (b) in <100> direction for various t_{SOI}. Monotonic mobility degradation as decreasing t_{SOI} is observed. This result is consistent with previous reports [19, 53], indicating the successful device fabrication.

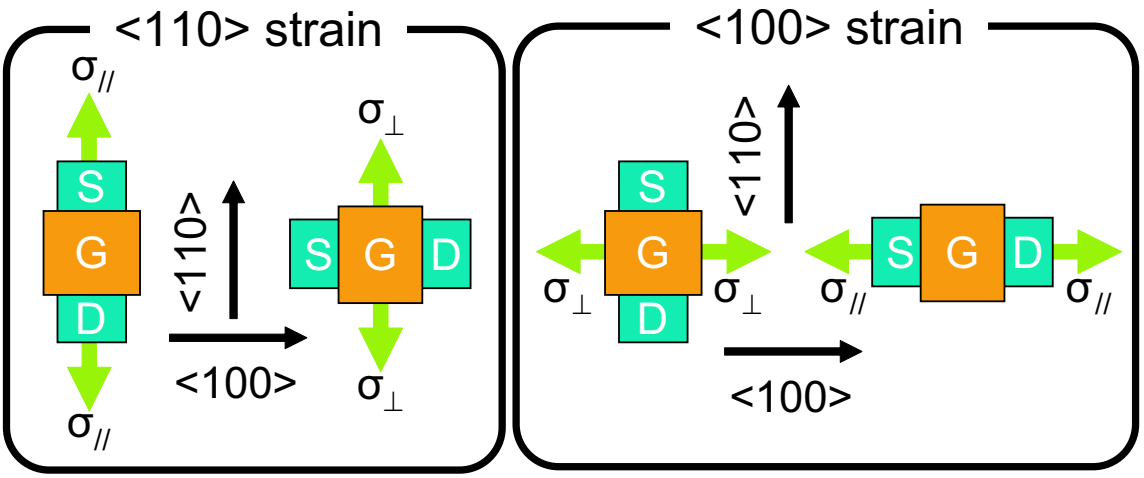
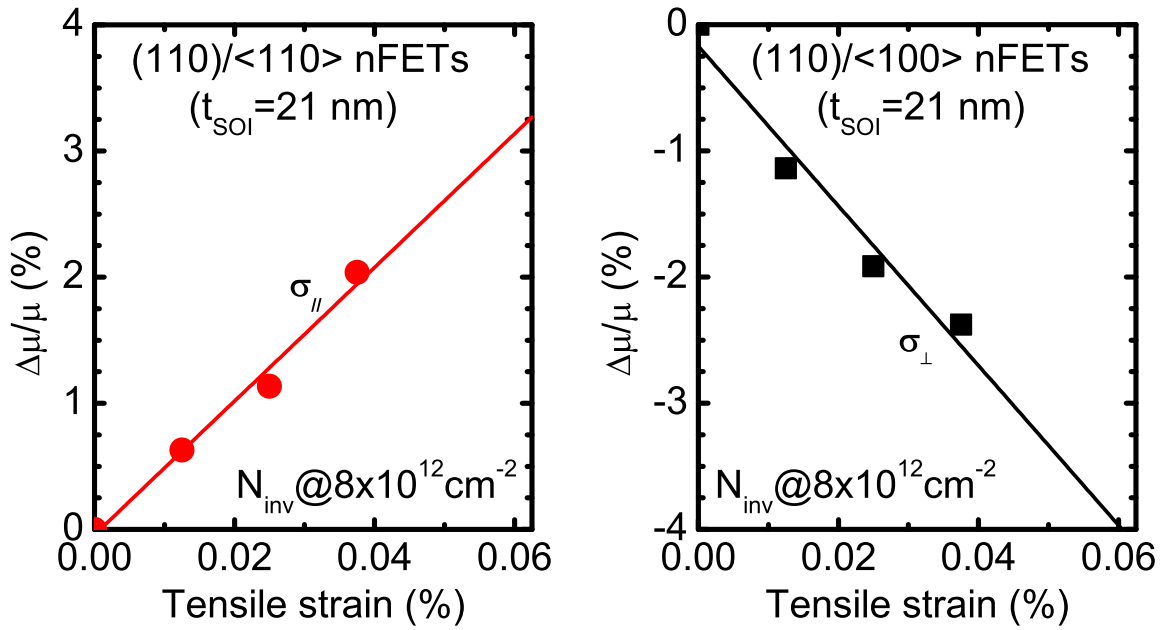
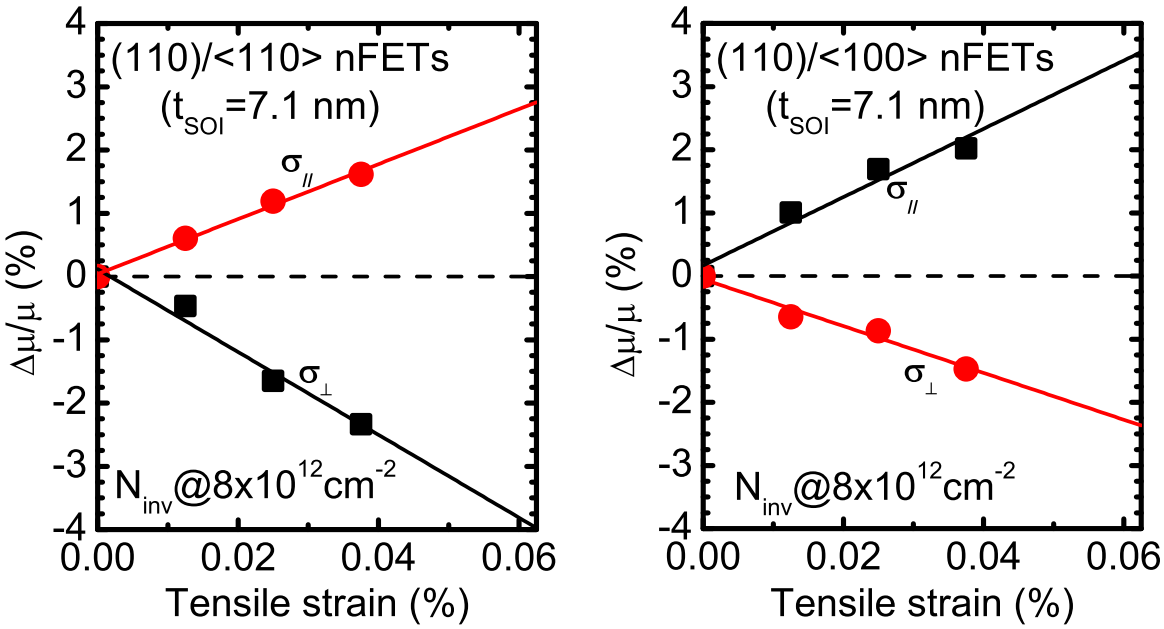


Fig.6.2 Schematics of considered strain configuration. Arrows indicate the applied strain. In both <110>- and <100>-directed bulk nFETs, μ_e is enhanced by the longitudinal tensile strain, while it is degraded by transverse tensile strain.



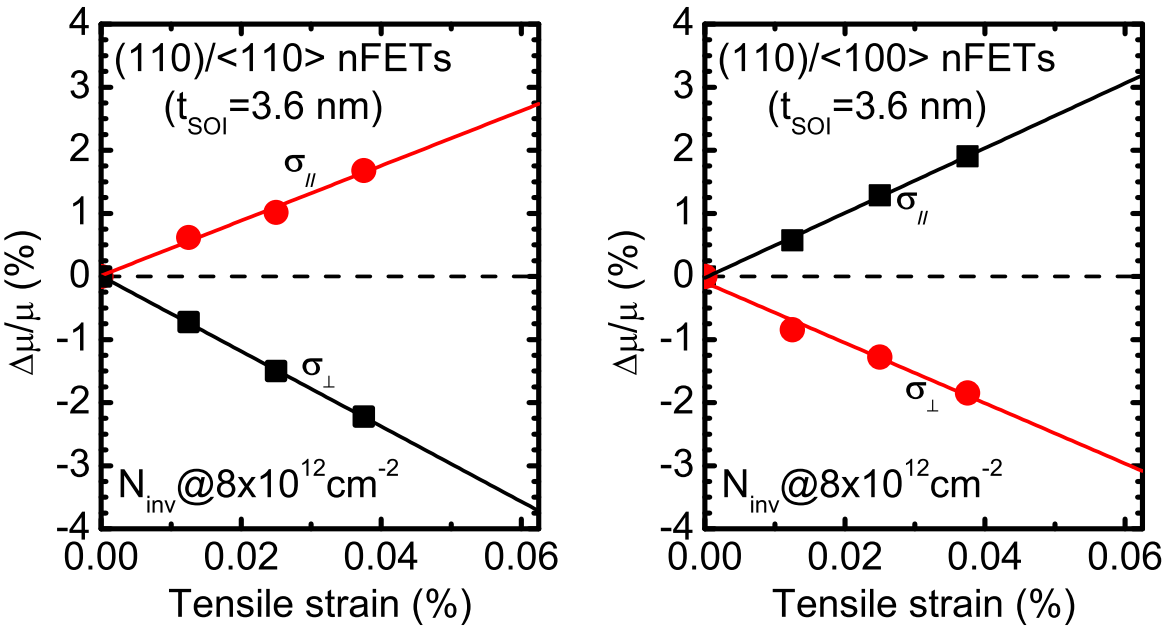
(a) (b)

Fig.6.3 $\Delta\mu/\mu$ of (a) <110>-directed nFETs and (b) <100>-directed nFETs with thick SOI (t_{SOI} of 21 nm) as a function of applied uniaxial tensile strain. Here, $\sigma_{\perp}$ and $\sigma_{//}$ denote the strain perpendicular to and parallel to the channel, respectively. These results are consistent with a previous report on bulk nFETs [37].



(a) (b)

Fig.6.4 $\Delta\mu/\mu$ of (a) <110>-directed nFETs and (b) <100>-directed nFETs with t_{SOI} of 7.1 nm as a function of applied uniaxial tensile strain. Smaller $\Delta\mu/\mu$ than that with t_{SOI} of 21 nm is observed. It is interesting to point out that absolute value of $\Delta\mu/\mu$ is larger under <100>-directed strain.



(a) (b)

Fig.6.5 $\Delta\mu/\mu$ of (a) <110>-directed nFETs and (b) <100>-directed nFETs with t_{SOI} of 3.6 nm as a function of applied uniaxial tensile strain. Smaller $\Delta\mu/\mu$ than bulk-like FETs is observed, though it is very close to $\Delta\mu/\mu$ with t_{SOI} of 7.1 nm pFETs.

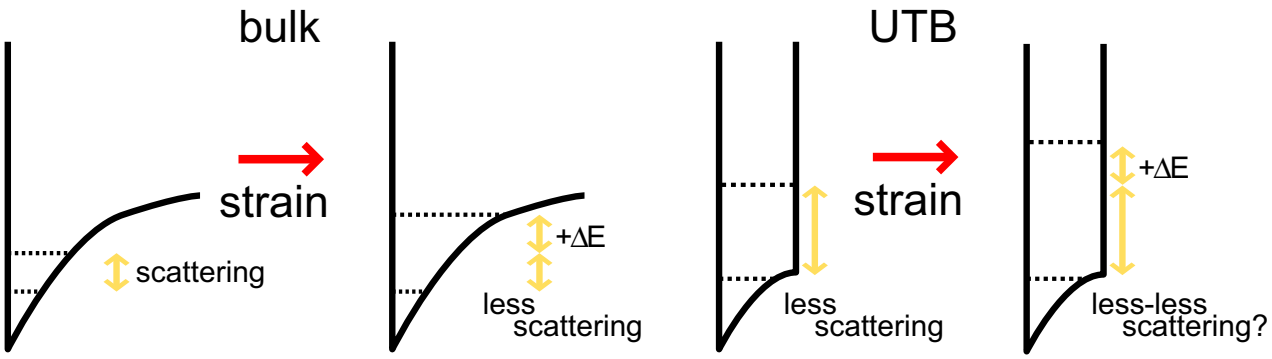


Fig.6.6 Schematics describing the subband energy enlargement effects on mobility. Even if the enlargement of the subband energy differences is the same, the practical effects are dependent on the unstrained subband energy difference. Therefore, the tensile strain is thought to have less contributions to $\Delta\mu/\mu$ in UTB nFETs.

Chapter 7

Performance Estimation of Si (110) Ultrathin Body CMOS FETs

7.1 Introduction

The physics behind mobility behavior in ultrathin body (UTB) pFETs (in chapters 3 and 4) and UTB nFETs (in chapters 5 and 6) under stain has been investigated and discussed in this dissertation. Even though the mobility behavior and its enhancement technique are understood, there is still one remaining and crucial problem; "which surface orientation has a higher performance in a CMOS operation, (100) or (110)? "

Obvious drawbacks of Si (110)-oriented CMOS technology are;

(1) smaller electron mobility

(2) smaller sensitivity to the strain

Recently, many papers focus on the CMOS performance in (110) bulk FETs [42, 44, 49, 58, 59]. All of those papers concluded that the performance of Si (110) CMOS is comparable or higher even in advanced technology nodes, regardless of some drawbacks.

In this chapter, the CMOS performance comparison between (100)- and (110)-oriented UTB FETs is made. Utilizing the experimental results, the mobility under large amount of strain is estimated. The propagation gate delay is also estimated based on the extracted mobility.

7.2 Performance Estimation Method and Assumptions

7.2.1 Gate propagation delay

The state-of-the-art CMOS performance is estimated with the sum of the gate propagation delay as

$$\tau = \sum \frac{CV}{I} = \frac{CV}{I_n} + \frac{CV}{I_p}$$

where C, V, I, I_n and I_p represents the gate capacitance, the source voltage, the drive current, the drive current of nFETs, and the drive current of pFETs, respectively. In this study, all the parameter except I_n and I_p are assumed to be the same, and I is assumed to be proportional to the square root of mobility μ ($\sqrt{\mu}$) [60, 61].

7.2.2 Applied strain and mobility enhancement

The appropriate uniaxial strain is assumed to be applied to each FETs; <110>-directed uniaxial compressive strain to (110) pFETs and (100) pFETs, the longitudinal uniaxial tensile strain to nFETs. Considered amount of strain is up to 1%. Compared to the state-of-the-art bulk CMOS technology, they are small. However, it has been reported that the introduction of strain to the UTB FETs are difficult because of their ultimately thin SOI, and the total amount of applied strain has been reported as large as 500 MPa (around 0.3-0.4%) [62].

The mobility enhancement is estimated by the linear-extraporation of experimental results. This approximation is too optimistic, as it is also well known experimental and theoretically that the mobility enhancement by strain is saturated under a high amount of strain [39]. Therefore, the results shown in this study gives an upper limit of the CMOS performance.

7.2.3 Other miscellaneous assumptions

For higher performance in (110) surface, <110>-directed pFETs and <100>-directed nFETs should be utilized (Fig. 7.1 (c)). Practically, this configuration is not realistic especially for digital circuit designers. In terms of the circuit design, both nFETs and pFETs should be directed to the same direction. Therefore, <110>-directed (110)-oriented CMOS FETs, <100>-directed (110)-oriented CMOS FETs, and <110>-directed (100)-oriented CMOS FETs (as a reference) are mainly

investigated as shown in Fig. 7.1 (a) and (b).

Assumed SOI thickness (t_{SOI}) is 4 nm, which corresponds to the gate length of 15 nm. A gate length of 15 nm is scheduled to be in mass production in around 2015 [50].

7.3 Estimated Performance of (110) Ultrathin Body CMOS FETs

7.3.1 Estimated mobility

Figure 7.2 shows the electron mobility (μ_e) at inversion layer density (N_{inv}) of 8x10^{12} cm^{-2} as a function of applied strain. μ_e of (100) UTB nFETs and its enhancement by strain are cited from previous papers [33, 63]. Clearly, μ_e difference between (100) nFETs and (110) nFETs enlarges.

In constrast to μ_e, hole mobility (μ_h) shows the opposite results. Figure 7.3 shows μ_h at N_{inv} of 8x10^{12} cm^{-2} as a function of applied strain. μ_h of (100) UTB pFETs and its enhancement by strain are cited from previous papers [17, 64]. Even though the strain sensitivity is lower in (110) UTB pFETs, high μ_h at unstrained condition can compensate it.

7.3.2 Estimated gate propagation delay

Next, the gate propagation delay is estimated based on the assumptions described in the previous chapter. Figure 7.4 shows the propagation delay (τ_{pd}) as a function of applied strain. τ_{pd} is normalized so that the τ_{pd} in (100) CMOS UTB FETs without strain equals to unity.

As has already pointed out in the previous literature [53], (110)-oriented CMOS UTB FETs show higher performance than (100)-oriented CMOS UTB FETs. However, as the applied strain increases, the performance advantage of (110)-oriented CMOS UTB FETs reduces not only in (110)/<100>, but also in (110)/<110> CMOS UTB FETs. τ_{pd} of the optimised (110)-oriented CMOS UTB FETs (the combination of <110>-directed pFETs and <100>-directed nFETs) is also calculated as a reference, but even τ_{pd} of the optimised (110) CMOS UTB FETs shows lower performance under strain larger than 0.5%.

Above discussion is based on the same gate width of nFETs and pFETs. However, wider gate is utilized for pFETs in a CMOS circuit. Therefore, it's possible that τ_{pd} is over- or under-estimated in above results. To solve this problem, the optimised gate width is also calculated by keeping the total gate width constant, and τ_{pd} is re-calculated. By changing the ratio of nFETs and pFETs, the

minimum τ_{pd} is evaluated. Explicitly, τ_{pd} is defined by the minimum value of the following equation:

$$\tau = \sum \frac{CV}{I} = \frac{CV}{I_n} + \frac{CV}{I_p} = \frac{CV}{x\sqrt{\mu_n}} + \frac{CV}{(1-x)\sqrt{\mu_p}}$$

where μ_n, μ_p, and x are the electron mobility, the hole mobility, and the ratio of nFETs to the total gate width ($0<x<1$). Figure 7.5 shows optimised τ_{pd} in each structure. The tendency is quite similar to that in Fig. 7.4, meaning that the performance of (110)-oriented CMOS UTB FETs is higher under small amount of strain.

Therefore, (110)-oriented CMOS UTB FETs won't or shouldn't be utilized under highly strained CMOS UTB FETs, such as high-performance devices. Considering that the introduction of high amount of strain is a challenging problem due to the extremely thin SOI, (110) CMOS UTB FETs will be one of the most promising device structure in near future.

7.4 Summary

The gate propagation delay is estimated based on the experimental results and some simple assumptions. As a first-order estimation result, the performance advantage of (110) ultrathin body CMOS FETs over (100) ultrathin body CMOS FETs reduces as applied strain enhances. Thus, CMOS FETs based on (110) ultrathin body FETs could be one of the performance booster technology for low-cost LSIs in which high-cost strain technology cannot be utilized.

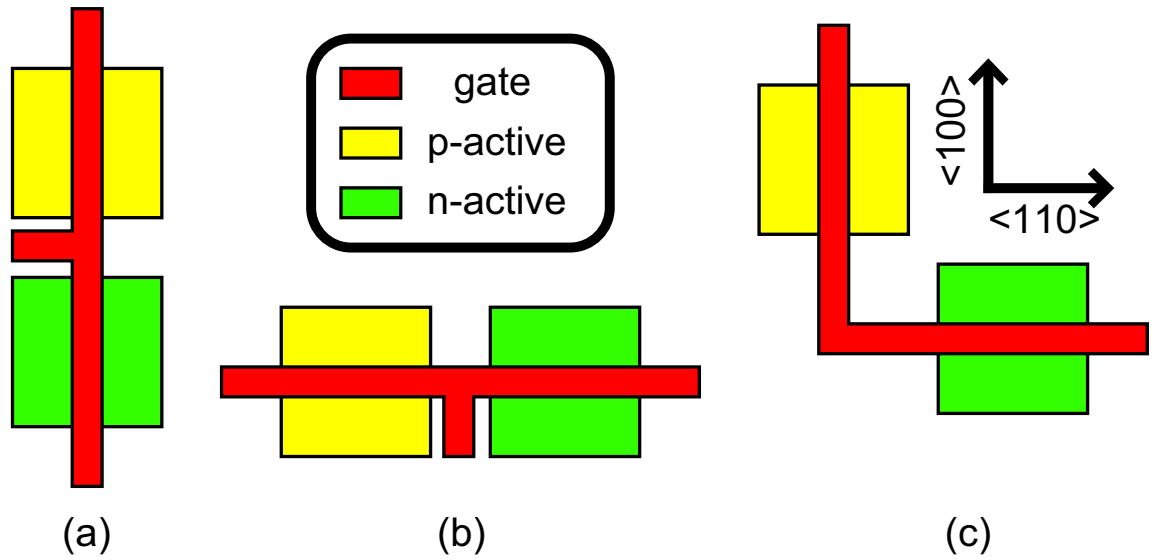


Fig.7.1 Schematics of the inverter layout in (110) surface. As hole mobility is higher in <110> direction and electron mobility is higher in <100> direction, the highest performance is expected in (c). However, it is not realistic in terms of circuit design. Therefore, only (a) and (b) is investigated.

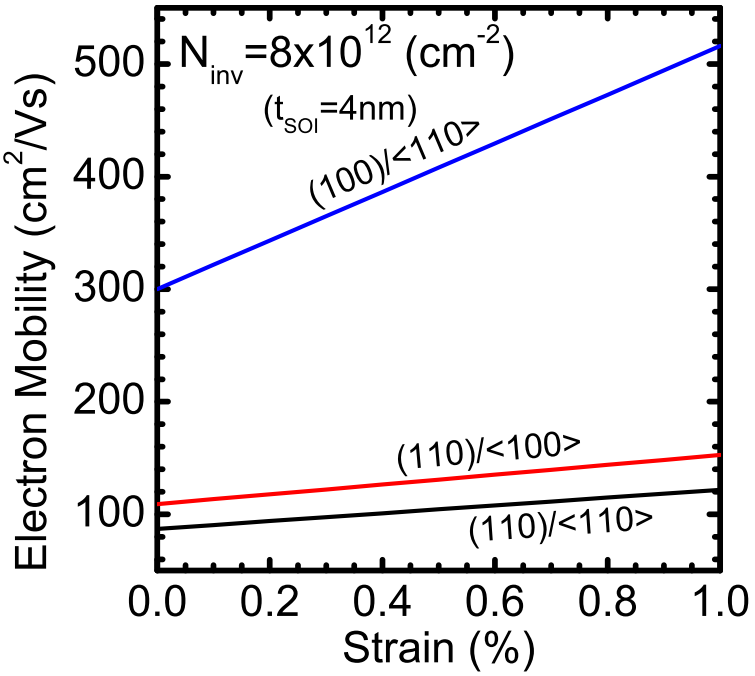


Fig.7.2 Calculated electron mobility as a function of applied strain at N_{inv} of $8x10^{12}$ cm^{-2}. Thanks to both initially high electron mobility and high sensitivity to strain, (100) nFETs shows the highest electron mobility.

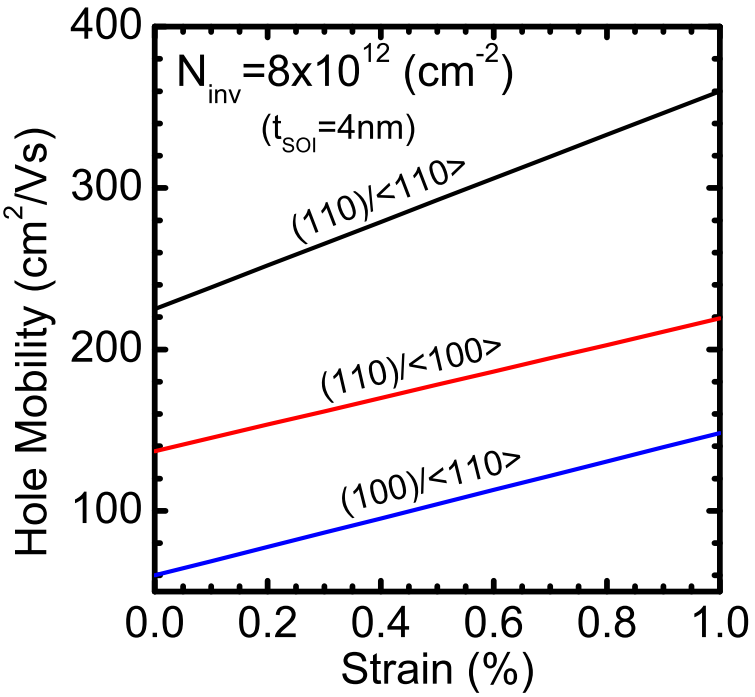


Fig.7.3 Calculated hole mobility as a function of applied strain at N_{inv} of $8x10^{12}$ cm^{-2}. Even though the sensitivity to strain is smaller in (110) pFETs, (110)/<110> pFETs shows the highest performance thanks to initially high hole mobility.

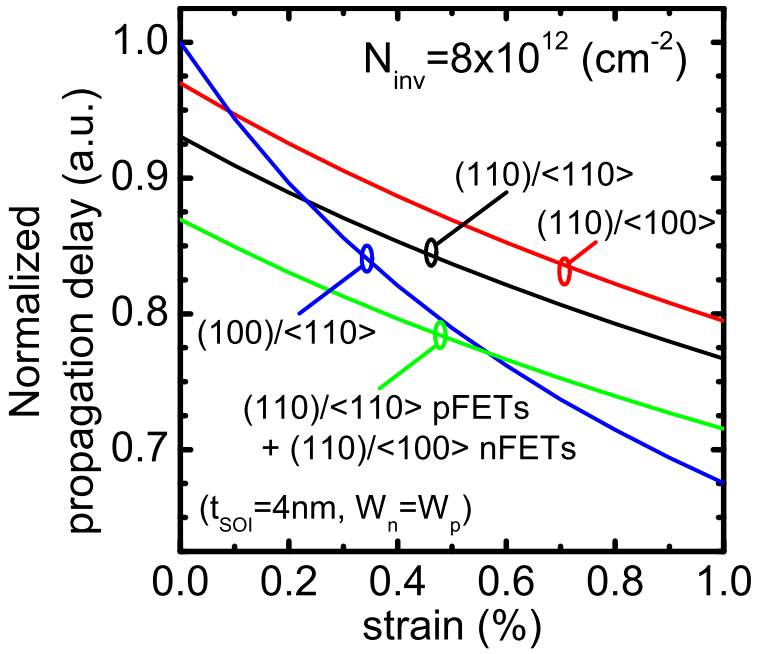


Fig.7.4 Calculated gate propagation delay as a function of applied strain. τ_{pd} is normalized by τ_{pd} of the (100)-oriented CMOS FETs without strain. Under no strain, (110) CMOS FETs show higher performance than (100), however, (110) CMOS FETs show lower performance at the strain as small as 0.2%.

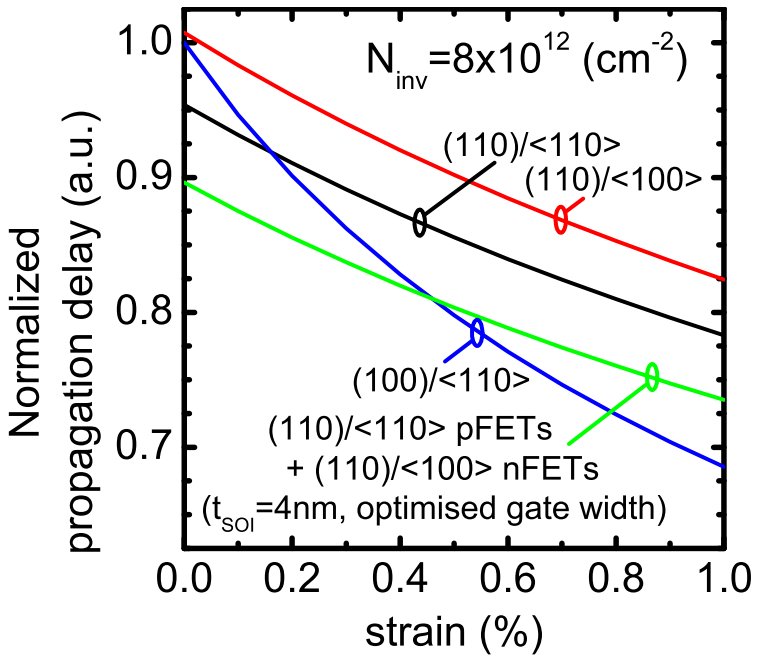


Fig.7.5 Calculated gate propagation delay as a function of applied strain. τ_{pd} is normalized by τ_{pd} of the (100)-oriented CMOS FETs without strain. Note that the gate width ratio is optimised to achieve minimum τ_{pd} in each CMOS FETs. The performance tendency is almost the same as that in Fig. 7.4 regardless of gate width ratio. Under no strain, (110) CMOS FETs show higher performance than (100), however, (110) CMOS FETs show lower performance at the strain as small as 0.2%.

Chapter 8

Conclusions

In this dissertation, the mobility in (110)-oriented ultrathin body pFETs and nFETs has been investigated experimentally and theoretically. The ultrathin body FETs show high-level of immunity not only to the short channel effect but also to the threshold voltage variability, and hence, is thought to be one practical option for near-future device structure. It is revealed that in (110)-oriented ultrathin body FETs, the quantum confinement effects play more significant role in carrier transport than in (100) FETs. The results obtained in this dissertation are summarized as follows;

Hole mobility in (110) surface benefits from the quantum confinement effects. Stronger quantum confinement, such as higher surface electric field or thinner SOI thickness, reduces the conduction effective mass especially in <110> direction. Therefore, the advantage of hole mobility in (110) bulk FETs over that in (100) bulk FETs, where no such effective mass reduction occurs, is prominent especially under strong quantum confinement. The same phenomenon happens in ultrathin body FETs. The thinner the SOI thickness is, the lighter the conduction effective mass is, which doesn't occur in (100) ultrathin body FETs.

The sensitivity of hole motility to the strain is smaller in (110) surface than that in (100) surface. This is because both the strain and the quantum confinement have the same effect on hole mobility, such as reduction in conduction effective mass and the enlargement of subband energy difference. The benefits from the strain and the quantum confinement seem to saturate if they are larger than a certain amount.

Despite the smaller sensitivity to the strain, (110)-oriented ultrathin body pFETs is expected to have higher performance than (100)-oriented ultrathin body pFETs, based on the experimental results. Therefore, (110) pFETs is one of the best performance boosting technologies in near future.

In electron mobility in (110) surface, the quantum confinement affects the direction dependence of electron mobility in ultrathin body nFETs. The non-parabolicity in <110> direction leads to the invalidity of the effective mass approximation. Though this phenomenon occurs in both bulk FETs and ultrathin body FETs, it is more prominent in ultrathin body FETs. <110>-directed electron mobility is always lower than <100>-directed electron mobility in bulk nFETs, however, the electron mobility in <110> direction is higher than that in <100> direction in an ultimately thin SOI. Considering that the hole mobility in <110> direction is higher than that in <100> direction, higher CMOS circuit performance can be obtained with both p- and nFETs in <110> direction in ultimately thin SOI CMOS circuits.

The sensitivity of electron mobility to the strain is comparable to bulk FETs if the SOI is thick enough, though the sensitivity reduces as SOI thins. This is because the subband energy shift, which is thought to be the main mobility modulation mechanism, won't affect the electron mobility in ultrathin body FETs. However, the strain is still effective to enhance electron mobility in ultrathin body FETs. The sensitivity of (110)-oriented ultrathin body FETs to the strain is comparable to (100)-oriented ultrathin body FETs, therefore, the difference of electron mobility enlarges as strain increases.

The CMOS performance of (110) ultrathin body FETs is higher if the strain is low enough. As the strain increases, the performance of (100) CMOS increases, though the (110) CMOS doesn't increase much. Therefore, it is concluded that the CMOS FETs utilizing (110)-oriented ultrathin body FETs is one of the performance boosting technologies for the low-cost devices, in which high amount of strain isn't applied to the channel.

Appendix A

Fabrication Process

A.1 Device Fabrication of Ultrathin Body SOI MOSFETs

The devices used in this study were fabricated on an UNIBOND SOI wafer through the conventional SOI mesa process. A briefly summarized mesa process is as follows;

(1) active areas are patterned (Fig. A.1 (a)).

(2) the gate oxidation and the poly-silicon deposition are performed sequentially (Fig. A.1 (b)).

(3) the gate pattern is formed (Fig. A.1 (c)).

(4) the self-aligned ion implantation is performed (Fig. A.1 (d)).

After the formation of FETs, the back-end process to make metal contacts (such as the passivation, contact patterning, metal wiring) is performed. Note that the FETs are isolated each other without the local oxidation of silicon (LOCOS) or the shallow trench isolation (STI) process.

A problem to investigate an ultlathin body SOI FET is the parasitic resistance of source and drain region. A thin SOI layer cannot be fully doped by the ion implantation process, resulting in severely large resistance. To avoid this problem, the LOCOS process was utilized to recess the channel region [17, 34, 65]. Key processes in the recess are as follows;

(1) A silicon nitride film was deposited and patterned. (Fig. A.2 (a))

(2) An SOI film was locally oxidized. (Fig. A.2 (b))

(3) A recessed structure was formed, followed by the removal of the silicon nitride and silicon-dioxide. (Fig. A.2 (c))

(4) An SOI MOSFET with a recessed channel was formed after the conventional MOSFET

process. (Fig. A.2 (d))

The recess process is performed before the active area formation (Fig. A.1), or between the active area formation (Fig. A.1 (a)) and the gate oxidation (Fig. A.1 (b)) The detailed procedure can be found in Table A.1.

The size of each device is large enough to exclude parasitic components (such as the overlap capacitance, and the difference between patterned size and fabricated one), which affect the accuracy of the measurement. The typical gate length and width in this study are both 200 μm, and the gate oxide thickness is around 20 nm.

A.2 Device Fabrication of Common Channel MOSFETs

The fabrication process of common channel FETs, which shares completely the same channel in both <110> and <100> directions in (110) orientation, needs additional processes to the SOI mesa process as previously described in section A.1.

Additional processes are illustrated in Fig. A.3. In Fig. A.3, the first poly-silicon is colored as orange, and the second poly-silicon is colored as red. The procedure is summarized as follows;

(1) After the gate oxidation and the poly-silicon deposition, the ion implantation is performed. Note the source and the drain region is not doped at this time (Fig. A.3 (a)).

(2) the gate is patterned and formed (Fig. A.3 (b)).

(3) the high-temperature oxide (HTO) and the second poly-silicon are deposited sequentially to form the side gate (Fig. A.3 (c)).

(4) the side gate is formed, followed by the self-aligned ion implantation (Fig. A.3 (d)).

The side gate formation process is right after the gate oxidation and the poly-silicon deposition in the SOI mesa process. The detailed procedure can be found in Table A.2.

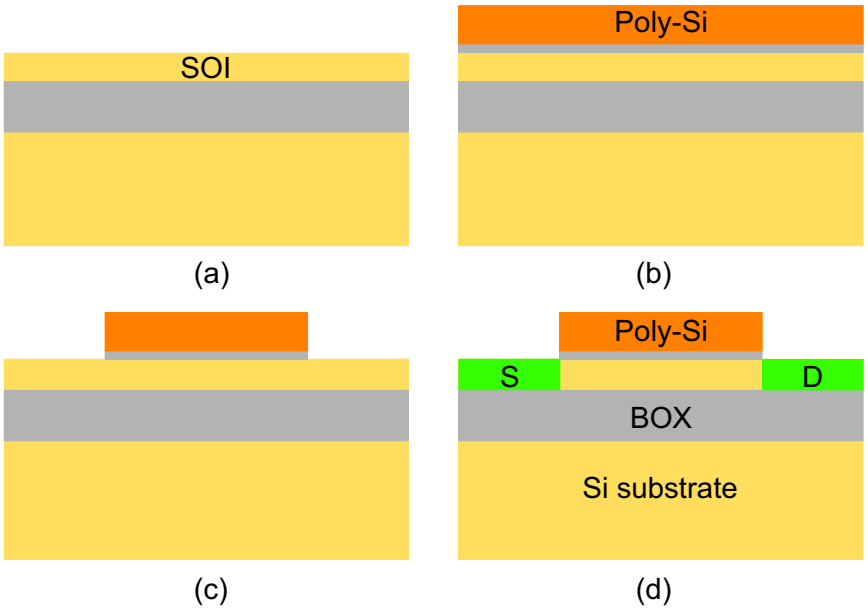


Fig.A.1 Schematics of key processes in the SOI mesa process. (a) initial SOI wafer (b) gate oxidation and poly-silicon deposition (c) gate patterning (d) self-aligned ion implantation.

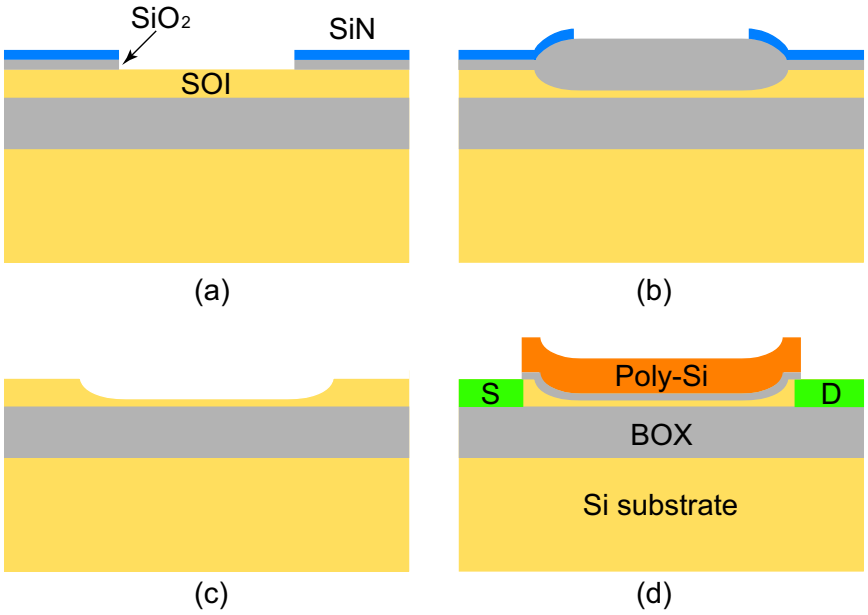


Fig.A.2 Schematics of a recess process to keep the source and drain region thick. (a) silicon-nitride deposition and patterning (b) local oxidation of silicon (LOCOS) (c) silicon-nitride and silicon-dioxide removal (d) final device structure.

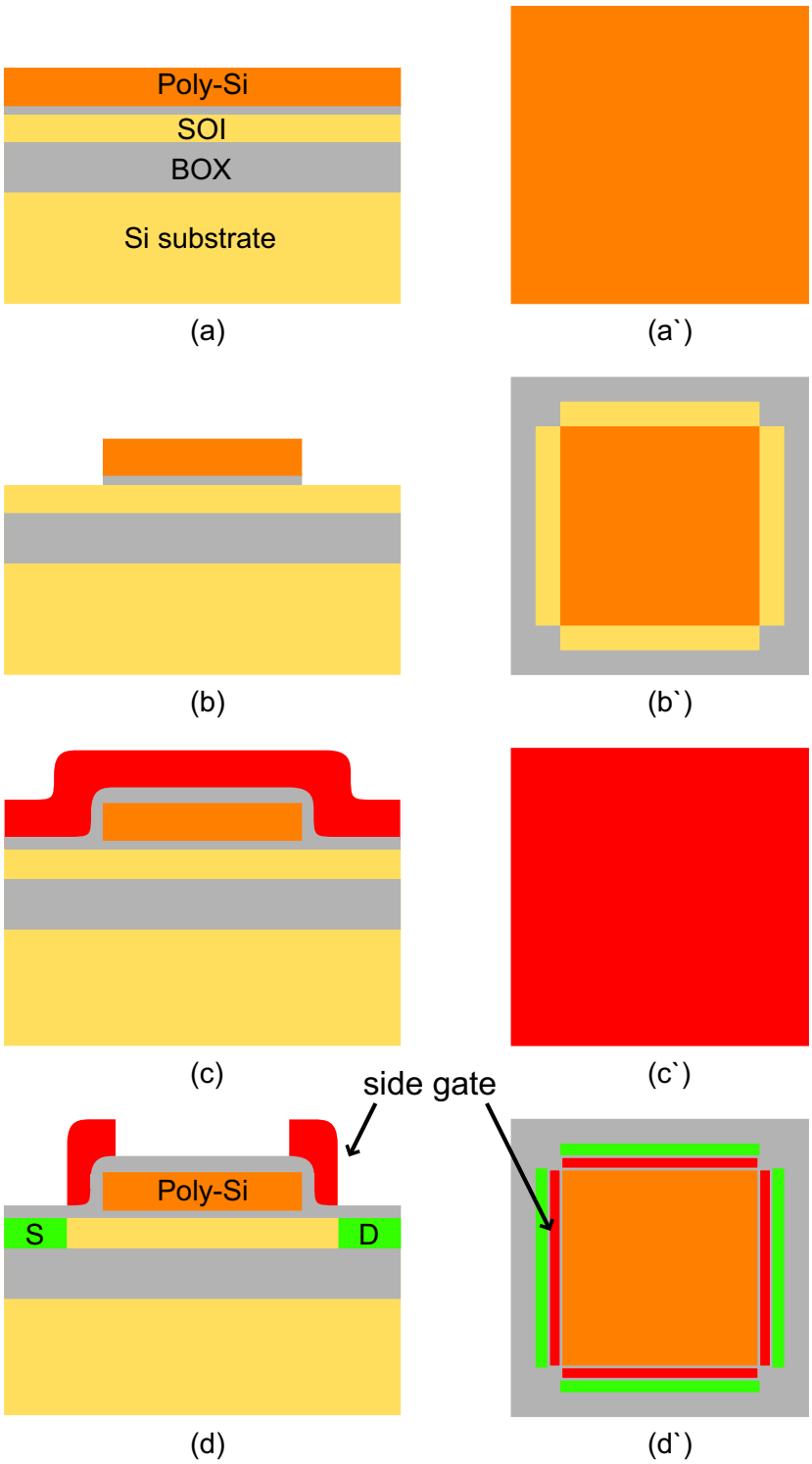


Fig.A.3 Schematics of a common channel MOSFETs fabrication. The left hand side figures show the top view, and the right hand side figures show the cross section view. (a)/(a‘) the first ion implantation (b)/(b’) the gate patterning (c)(c‘) the high temperature oxide and the second poly-silicon deposition for the side gate (d)/(d‘) the side gate formation and the second ion implantation.

TableA.1 A process flow of (100)/(110) oriented UTB FD SOI FETs. The oxidation temperature is usually lower in (110) surface because of the higher oxidation rates of Si (110) surface than those of Si (100) surface. The inequality sign represents the laser drawing process.

#	Process	Conditions
1	Dicing	chip size 20 mm x 15 mm or 22 mm x 20 mm
2	Cleaning1	SPM: H_2SO_4+H_2O_2=3:1, 120-130 deg., 10 min. BHF: 1min. SC1: H_2O_2:NH_4OH:H_2O=1:0.25:5, 80-85 deg., 10 min.
3	Cleaning2	numbering SC1: H_2O_2:NH_4OH:H_2O=1:0.25:5, 75-80 deg., 10 min.
4	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min. HF: 1%, 1 min.
5	SOI thinning	Samco #4, (100): Dry oxidation O_2 1.0 l/min., 1100 deg., 150 min. Samco #4, (110): No thinning
6	Oxide removal	BHF: 5 min.
7	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125deg., 10min. HF: 1%, 1 min.
8	Pad oxidation	Samco #4, (100): Dry Oxidation O_2=1.0 l/min., 1000deg., 9min. Samco #4, (110): Dry Oxidation O_2=1.0 l/min., 900deg., 5.5min.
9	elllipsometry	Measure SOI thickness
10	<Markarea>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec. prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. Postbake 120 deg., 10 min.
11	SOI etching	Helicon Ethcher (step2: 80 sec., step3: 20 sec., step4: 0 sec., Recipe: Poly-Gate)
12	BOX removal	BHF: 4 min.
13	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125deg., 10min.
14	<Mark>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser Exposure. NMD-3 1 min. Postbake 110 deg., 10 min.
15	Mark Etching	Helicon Etcher (step2: 0 sec., step3: 405 sec., step4: 0 sec., Recipe: MarkHarata)
16	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
17	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1 120-125 deg., 10 min.
18	Nitride deposition	Vertical CVD #1 (SiH_2Cl_2 20 sccm, NH_3 80sccm, 33 Pa, 780deg., 25 min.)
19	<Recess>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500rpm 5sec., 6000rpm 60sec., pre bake 100deg., 10min. Laser Exposure NMD-3 1 min. Postbake 120 deg., 10 min.
20	SiN-Etching	DFR etcher (step2: 30 sec.)
21	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
22	elllipsometry	Measure SOI thickness (target: aimed SOI thickness + 6 nm)
23	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min. HF: 1%, 4 min.
24	LOCOS	Samco #5, (100): Dry oxidation O_2=1.0 l/min., 1100 deg. Samco #5, (110): Dry oxidation O_2=1.0 l/min., 1000 deg.

25	SiN removal	H_3PO_4: 180 deg., 7 min.
26	elllipsometry	Measure SOI thickness.
27	<Mesa>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser Exposure NMD-3 1 min. Postbake 120 deg., 10 min.
28	Mesa etching	Helicon etcher (step2: 40 sec., step3: 25 sec., step4: 0 sec., Recipe: Poly-Gate)
29	Resist removal	Acetone: 10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
30	RCA cleaning	HF: 1%, 7min. SPM: H_2SO_4+H_2O_2=3:1, 125-130 deg., 10 min. HF: 1%, 1.5 min. SC1: H_2O_2:NH_4OH:H_2O=1:0.25:5 75-77 deg., 10 min. HF: 1%, 1 min. SC2: HCl:H_2O_2:H_2O=1:1:6, 75-77 deg., 10 min. HF: 1%, 1.5 min.
31	Gate oxidation	Pyro furnace, (100): Dry oxidation O_2=1.0 l/min., 1000 deg., 7 min. Pyro furnace, (110): Dry oxidation O_2=1.0 l/min., 950 deg., 9 min.
32	Poly-Si deposition	Vertical CVD #1 (SiH_4 250 sccm, 33 Pa, 580 deg., 45 min.)
33	<Gate>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
34	Gate etching	Helicon etcher (step2: 15 sec., step3: 70 sec., step4: 10 sec., Recipe: Poly-gate)
35	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
36	ellipsometry	Measure SOI thickness
37	<N>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
38	Ion implantation	P^+ 35 keV, 3.0x10^{15} cm^{-2}
39	Resist removal	Acetone: 60 min. SPM: H_2SO_4+H_2O_2=3:1, 150-160 deg., 10 min. (three times)
40	O_3 ashing	Ozone asher: O_2=0.5 l/min., 300 deg., 30 min.
41	<P>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
42	Ion implantation	BF^{2+} 35 keV, 3.0x10^{15} cm^{-2}
43	Resist removal	Acetone: 60 min. SPM: H_2SO_4+H_2O_2=3:1, 150-160 deg., 10 min. (three times)
44	O_3 ashing	Ozone asher: O_2=0.5 l/min., 300 deg., 30 min.
45	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
46	Ion activation	Samco #5: N_2=0.5 l/min., 950 deg., 5 min.
47	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
48	SiO_2 Passivation	Vertical CVD #2 (SiH_4 15 sccm, O_2 60 sccm, 33 Pa, 400 deg., 150 min.)
49	H_2 anneal	Samco #2: H_2 100 sccm, 400 deg., 120 min.
50	<Contact>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min.

		AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
51	Contact etching	BHF: 4 min.
52	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1 120-125 deg., 10 min.
53	Native oxide removal	HF: 1%, 2 min.
54	Al evaporation	
55	<Al>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
56	Al-Etch	Al etchant: 45 deg., 45 sec.
57	Resist removal	Acetone: 5-10 min.

TableA.2 A process flow of a common channel FET, which shares completely the same SOI between (110)/<110> and (110)/<100> pFETs. Several processes were added to the process of UTB FD SOI FETs to form the side gate.

#	Process	Conditions
1	Dicing	chip size 22 mm x 20 mm
2	Cleaning1	SPM: H_2SO_4+H_2O_2=3:1, 120-130 deg., 10 min. BHF: 1 min. SC1: H_2O_2:NH_4OH:H_2O=1:0.25:5, 80-85 deg., 10 min.
3	Cleaning2	numbering SC1: H_2O_2:NH_4OH:H_2O=1:0.25:5, 75-80 deg., 10 min.
4	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min. HF: 1%, 1 min.
5	SOI thinning	Samco #4: Dry oxidation O_2=1.0 l/min., 1000 deg., 20 min.
6	Oxide removal	BHF: 5 min.
7	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125deg., 10min. HF: 1%, 1 min.
8	Pad oxidation	Samco #4: Dry oxidation O_2=1.0 l/min., 900deg., 5 min.
9	elllipsometry	Measure SOI thickness
10	<Markarea>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec. prebake 100 deg., 10min. Laser Exposure NMD-3 1 min. Postbake 120 deg., 10 min.
11	SOI etching	Helicon Ethcher (step2: 80 sec., step3: 20 sec., step4: 0 sec., Recipe: Gate-Poly)
12	BOX removal	BHF: 4 min.
13	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125deg., 10min.
14	<Mark>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser Exposure. NMD-3 1 min. Postbake 110 deg., 10 min.
15	Mark Etching	Helicon Etcher (step2: 0 sec., step3: 405 sec., step4: 0 sec., Recipe: MarkHarata)
16	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
17	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1 120-125 deg., 10 min.
18	Nitride deposition	Vertical CVD #1 (SiH_2Cl_2 20 sccm, NH_3 80sccm, 33 Pa, 780deg., 25 min.)
19	<Recess>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500rpm 5sec., 6000rpm 60sec., pre bake 100deg., 10min. Laser Exposure NMD-3 1 min. Postbake 120 deg., 10 min.
20	SiN-Etching	DFR etcher (step2: 30 sec.)
21	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
22	elllipsometry	Measure SOI thickness (target: aimed SOI thickness + 6 nm)
23	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min. HF: 1% 4 min.
24	LOCOS	Samco #5: Dry oxidation O_2=1.0 l/min., 1000 deg.
25	SiN removal	H_3PO_4: 180 deg., 7 min.
26	elllipsometry	Measure SOI thickness.
27	<Mesa>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min.

		AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser Exposure NMD-3 1 min. Postbake 120 deg., 10 min.
28	Mesa etching	Helicon etcher (step2: 40 sec., step3: 25 sec., step4: 0 sec., Recipe: Poly-Gate)
29	Resist removal	Acetone: 10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
30	RCA cleaning	HF: 1%, 7min. SPM: H_2SO_4+H_2O_2=3:1, 125-130 deg., 10 min. HF: 1%, 1.5 min. SC1: H_2O_2:NH_4OH:H_2O=1:0.25:5 75-77 deg., 10 min. HF: 1%, 1 min. SC2: HCl:H_2O_2:H_2O=1:1:6, 75-77 deg., 10 min. HF: 1%, 1.5 min.
31	Gate oxidation	Pyro furnace: Dry oxidation O_2=1.0 l/min., 950 deg., 9 min.
32	Poly-Si deposition (main-gate)	Vertical CVD #1 (SiH_4 250 sccm, 33 Pa, 580 deg., 45 min.)
33	<Pre-N>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
34	Ion implantation	P^+ 35 keV, 3.0x10^{15} cm^{-2}
35	Resist removal	Acetone: 60 min. SPM: H_2SO_4+H_2O_2=3:1, 150-160 deg., 10 min. (three times)
36	O_3 ashing	Ozone asher: O_2=0.5 l/min., 300 deg., 30 min.
37	<Pre-P>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
38	Ion implantation	BF^{2+} 35 keV, 3.0x10^{15} cm^{-2}
39	Resist removal	Acetone: 60 min. SPM: H_2SO_4+H_2O_2=3:1, 150-160 deg., 10 min. (three times)
40	O_3 ashing	Ozone asher: O_2=0.5 l/min., 300 deg., 30 min.
41	<Gate>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
42	Gate etching	Helicon etcher (step2: 15 sec., step3: 70 sec., step4: 10 sec., Recipe: Poly-gate)
43	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
44	ellipsometry	Measure SOI thickness
45	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
46	SiO_2 deposition	Vertical CVD #2 (SiH_2Cl_2 20 sccm, N_2O 50 sccm, 80 Pa, 840 deg., 45 min.)
47	poly-Si deposition (side-gate)	Vertical CVD #1 (SiH_4 250 sccm, 33 Pa, 580 deg., 45 min.)
48	<SideGate>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.

49	Side-gate etching	Helicon etcher (step2: 15 sec., step3: 70 sec., step4: 10 sec., Recipe: Poly-gate)
50	Resist removal	Acetone 5-10 min. SPM: H_2SO_4+H_2O_2=3:1, 125-130 deg., 10 min.
51	<N>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
52	Ion implantation	P^+ 35 keV, 3.0x10^{15} cm^{-2}
53	Resist removal	Acetone: 60 min. SPM: H_2SO_4+H_2O_2=3:1, 150-160 deg., 10 min. (three times)
54	O_3 ashing	Ozone asher: O_2=0.5 l/min, 300 deg., 30 min.
55	<P>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
56	Ion implantation	BF^{2+} 35 keV, 3.0x10^{15} cm^{-2}
57	Resist removal	Acetone: 60 min. SPM: H_2SO_4+H_2O_2=3:1, 150-160 deg., 10 min. (three times)
58	O_3 ashing	Ozone asher: O_2=0.5 l/min, 300 deg., 30 min.
59	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
60	Ion activation	Samco #5: N_2=1.0 l/min., 950 deg., 5 min.
61	Pre-cleaning	SPM: H_2SO_4+H_2O_2=3:1, 120-125 deg., 10 min.
62	SiO_2 Passivation	Vertical CVD #2 (SiH_4 15 sccm, O_2 60 sccm, 33 Pa, 400 deg., 150 min.)
63	H_2 anneal	Samco #2: H_2 100 sccm, 400 deg., 120 min.
64	<Contact>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
65	Contact etching	BHF: 4 min.
66	Resist removal	Acetone: 5-10 min. SPM: H_2SO_4+H_2O_2=3:1 120-125 deg., 10 min.
67	Native oxide removal	HF: 1%, 2 min.
68	Al evaporation	
69	<Al>	HMDS 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. AZ1500 20CP 500 rpm 5 sec., 6000 rpm 60 sec., prebake 100 deg., 10 min. Laser exposure NMD-3 1 min. Postbake 120 deg., 10 min.
70	Al-Etch	Al etchant: 45 deg., 45 sec.
71	Resist removal	Acetone: 5-10 min.

Appendix B

Six-Band k·p Hamiltonian and Its Application to MOS Structure

It is well-known that the valence band structures of silicon can be extracted via the k·p perturbation method, and the most famous implementation is the six-band k·p Hamiltonian [45].

$$\mathbf{H} = \begin{bmatrix} \mathbf{H_{kp}} + \mathbf{H_{strain}} & \mathbf{0} \\ \mathbf{0} & \mathbf{H_{kp}} + \mathbf{H_{strain}} \end{bmatrix} + \mathbf{H_{so}} \tag{B.1}$$

where

$$\mathbf{H_{kp}} = \begin{bmatrix} Lk_1^2 + M(k_2^2 + k_3^2) & Nk_1k_2 & Nk_1k_3 \\ Nk_1k_2 & Lk_2^2 + M(k_1^2 + k_3^2) & Nk_2k_3 \\ Nk_1k_3 & Nk_2k_3 & Lk_3^2 + M(k_1^2 + k_2^2) \end{bmatrix} \tag{B.2}$$

,

$$\mathbf{H_{kp}} = \begin{bmatrix} le_{xx} + m(e_{yy} + e_{zz}) & ne_{xy} & ne_{xz} \\ ne_{xy} & le_{yy} + m(e_{xx} + e_{zz}) & ne_{yz} \\ ne_{xz} & n_{yz} & le_{zz} + m(e_{xx} + e_{yy}) \end{bmatrix} \tag{B.3}$$

and

$$\mathbf{H_{so}} = \frac{\Delta_{so}}{3} \begin{bmatrix} 0 & -i & 0 & 0 & 0 & 1 \\ i & 0 & 0 & 0 & 0 & -i \\ 0 & 0 & 0 & -1 & i & 0 \\ 0 & 0 & -1 & 0 & i & 0 \\ 0 & 0 & -i & -i & 0 & 0 \\ 1 & i & 0 & 0 & 0 & 0 \end{bmatrix} \tag{B.4}$$

Δ_{so} is the spin-orbit coupling, L, M, N are related to the Luttinger parameters, and l, m, n are related to the deformation potential. The parameters utilized in this study are described in Table. B.1. k_1, k_2, and k_3 are the coordinate system in k-space. e_{xx}, e_{yy}, e_{zz}, e_{xy}, e_{yz}, and e_{xz} are the strain tensors. Each subband energy at the point of $\mathbf{k}$ can be extracted by diagonalizing Eq. (B.1). It should be noted here that the $\mathbf{H_{strain}}$ is associated with strain in (100) surface, which requires the tensor rotation to deal with strain in (110) surface.

In this method, two-dimensionally confined subband structure can also extracted by discretizing in confinement direction, or, by replacing k_z with $-id/dz$ [45]. Numerically, Eq. (B.1) can be solved

on a z-mesh of N_z points in the SOI thickness interval with a variation method. It looks like

$$\begin{bmatrix} \ddots & \ddots & \ddots & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{D_-} & \mathbf{D_{l-1}} & \mathbf{D_+} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{D_-} & \mathbf{D_l} & \mathbf{D_+} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{D_-} & \mathbf{D_{l+1}} & \mathbf{D_+} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \ddots & \ddots & \ddots \end{bmatrix} \begin{bmatrix} \vdots \\ \Psi_{l-1} \\ \Psi_l \\ \Psi_{l+1} \\ \vdots \end{bmatrix} = E(\mathbf{k}) \begin{bmatrix} \vdots \\ \Psi_{l-1} \\ \Psi_l \\ \Psi_{l+1} \\ \vdots \end{bmatrix} \tag{B.5}$$

where each Ψ is a vector with six components, and $\mathbf{D_l}$, $\mathbf{D_-}$, and $\mathbf{D_+}$ are matrices with six by six components. The diagonal element, $\mathbf{D_l}$, contains $\mathbf{H_{so}}$, $\mathbf{H_{strain}}$, and $V(z)\mathbf{I}$, where $V(z)$ is the electrostatic potential and $\mathbf{I}$ is the unit matrix. $\mathbf{D_-}$ and $\mathbf{D_+}$ come from the finite difference terms, i.e., $df(z)/dz \rightarrow (f(l+1) - f(l-1))/2\Delta z$.

Therefore, the subband structure calculation is based on the diagonalization of a matrix with $6N_z \times 6N_z$ components. The diagonalization of such a huge size matrix is known as a time-consuming computational problem. In this dissertation, the following two libraries are utilized.

BLAS/LAPACK

The BLAS/LAPACK is one famous library which allows one easy to program, but to obtain almost the highest performance in famous numerical problems.

Parallelazation

Parallelization is another powerful tool to solve the numerically hard problem in a symmetric multiple processor (SMP) or multiple processor (MP) systems. OpenMP or MPI are famous and convinient middlewares.

It is noted that the conduction band structures of silicon cannot be analyzed, because the six-band k·p Hamiltonian is based on the perturbation around Γ point. Another method, such as the empirical pseudo potential method must be utilized.

TableB.1 Parameters utilized in the subband structure calculation by the six-band k·p Hamiltonian. All the parameters are cited from Ref. [66].

parameter	value	unit
L	-5.53	a.u.
M	-3.64	a.u.
N	-8.32	a.u.
Δ_{so}	0.044	eV
l	-1.74	eV
m	4.56	eV
n	-8.31	eV

Appendix C

List of Publications and Presentations

Journal Articles

(1) K. Shimizu, G. Tsutsui and T. Hiramoto, "Experimental study on mobility universality in (100) ultra thin body nMOSFET with SOI thickness of 5nm," *Japanese Journal of Applied Physics*, Vol. 46, No.20, pp. L480–L482, 2007.

(2) K. Shimizu, G. Tsutsui, D. Januar, T. Saraya and T. Hiramoto, "Experimental study on breakdown of mobility universality in <100>-directed (110)-oriented pMOSFETs," *IEEE Transaction on Nanotechnology*, Vol. 6, Issue 3, pp. 358–361, May, 2007.

(3) K. Shimizu, T. Saraya and T. Hiramoto, "Mobility degradation in (110)-oriented ultrathin body double-gate p-type metal-oxide-semiconductor field-effect-transistors with silicon-on-insulator thickness of less than 5 nm," *Japanese Journal of Applied Physics*, *accepted for publication.*

(4) K. Shimizu, T. Saraya and T. Hiramoto, "Suppression of electron mobility degradation in (100)-oriented double-gate ultra-thin body nMOSFETs," *IEEE Electron Device Letters*, *accepted for publication.*

(5) K. Shimizu, T. Saraya and T. Hiramoto, "Superior <110>-Directed Electron Mobility to <100>-Directed Electron Mobility in Ultrathin Body (110) n-Type Metal-Oxide-Semiconductor Field-Effect-Transistors," *Japanese Journal of Applied Physics*, *submitted.*

Presentations at International Conferences

(1) K. Shimizu and T. Hiramoto, "Mobility Degradation in (110)-Oriented Ultra-thin Body Double-Gate pMOSFETs with SOI Thickness of less than 5nm," *International Conference on Solid State*

Device & Materials (SSDM), pp.732–733, Tsukuba, Ibaraki, Sep. 2007.

(2) K. Shimizu and T. Hiramoto, "Suppression of Electron Mobility Degradation in (100)-Oriented Double Gate Ultra-Thin Body nMOSFETs with SOI Thickness of Less Than 2 nm," *IEEE International SOI Conference*, pp.145–146, Palm Springs, CA, USA, Oct. 2007.

(3) K. Shimizu and T. Hiramoto, "Mobility Enhancement in Uniaxially Strained (110) Oriented Ultra-Thin Body Single- and Double-Gate MOSFETs with SOI Thickness of less than 4 nm," *IEEE International Electron Device Meeting (IEDM)*, pp.715-718, Washington D.C., USA, Dec. 2007.

(4) K. Shimizu and T. Hiramoto, "Hole Mobility Enhancement by [110] Uniaxial Compressive Strain in (110) Oriented Ultra-Thin Body pMOSFETs with SOI Thickness of Less Than 4 nm," *2008 IEEE Silicon Nanoelectronics Workshop*, Honolulu, HI, USA, Jun. 2008.

(5) K. Shimizu, T. Saraya and T. Hiramoto, "Experimental Investigation on the Origin of Direction Dependence of Si (110) Hole Mobility Utilizing Ultra-Thin Body pMOSFETs," *IEEE International Electron Device Meeting (IEDM)*, pp. 67–70, SanFrancisco, CA, USA, Dec. 2008.

(6) K. Shimizu, T. Saraya and T. Hiramoto, "Superior <110>-Directed Mobility to <100>-Directed Mobility in Ultrathin Body (110) nMOSFETs," *IEEE International SOI conference*, Session 11–4, Foster City, CA, USA, Oct. 2009.

(7) K. Shimizu, T. Saraya and T. Hiramoto, "Physical Understandings of Si (110) Hole Mobility in Ultra-Thin Body pFETs by <110> and <111> Uniaxial Compressive Strain," *IEEE International Electron Device Meeting (IEDM)*, Session 19–6, Baltimore, MD, USA, Dec. 2009.

Presentations at Domestic Conferences

(1) 清水 健, 平本 俊郎, "SOI 膜厚 5nm 以下における (110) 面ダブルゲート UTB pMOSFET の移動度劣化," 第 68 回応用物理学会学術講演会, 7p–ZL–10, 北海道, 2007 年 9 月.

(2) 清水 健, 平本 俊郎, "膜厚 4nm 以下の (110) 面極薄 SOI シングルゲート/ダブルゲート n/pMOSFET における一軸引っ張り歪みによる移動度向上," 応用物理学会シリコンテクノロジー研究会, pp. 6–9, 東京, 2008 年 1 月.(招待講演)

(3) 清水 健, 平本 俊郎, "膜厚 4nm 以下の (110) 面極薄 SOI シングルゲート/ダブルゲート n/pMOSFET における一軸引っ張り歪みによる移動度向上," 第 55 回応用物理学関連講演会, 29a–P11–20, 東京,

2008 年 3 月.

(4) 清水 健, 平本 俊郎, “膜厚 2nm 以下の (100) 面極薄 SOI ダブルゲート MOSFET における移動度劣化の抑制,” 第 55 回応用物理学関連講演会, 29a–P11–21, 東京, 2008 年 3 月.

(5) 清水 健, 更屋 拓哉, 平本 俊郎, “Si(110) 面正孔移動度における方向依存性の起源–極薄 SOI を用いた実験的考察–,” 応用物理学会シリコンテクノロジー研究会, pp. 12–15, 東京, 2009 年 1 月.(招待講演)

(6) 清水 健, 平本 俊郎, “一軸性圧縮応力による (110) 面極薄 SOI pMOSFET の移動度向上,” 第 56 回応用物理学関連講演会, 1p–V–1, 東京, 2009 年 3 月.

(7) 清水 健, 更屋 拓哉, 平本 俊郎, “Si(110) 面正孔移動度における方向依存性の起源–極薄 SOI を用いた実験的考察–,” 第 56 回応用物理学関連講演会, 1p–V–2, 東京, 2009 年 3 月.

(8) 清水 健, 更屋 拓哉, 平本 俊郎, “(110) 面薄膜 SOI nMOSFET における電子移動度の方向依存性,” 第 70 回応用物理学会学術講演会, 9a–TA–2, 富山, 2009 年 9 月.

(9) 清水 健, 更屋 拓哉, 平本 俊郎, “歪みによる (110) 面極薄 SOI MOSFET 正孔移動度向上の物理的起源,” 第 57 回応用物理学関連講演会, 神奈川, 2010 年 3 月, 発表予定

Other Journal Articles

(1) J. Chen, T. Saraya, K. Miyaji, K. Shimizu and T. Hiramoto, “Electron mobility in silicon gate-all-around [100]- and [110]-directed nanowire metal-oxide-semiconductor field-effect-transistor on (100)-oriented silicon-on-insulator substrate extracted by improved split capacitance-voltage method,” *Japanese Journal of Applied Physics*, Vol. 48, No. 1, p.011205, Jan. 2009.

(2) C. Lee, A. T. Putra, K. Shimizu and T. Hiramoto, “Threshold voltage dependence of threshold voltage variability in intrinsic channel silicon-on-insulator metal-oxide-semiconductor field-effect transistors with ultrathin buried oxide,” *JJAP Special Issue, 2010, accepted for publication.*

Other Presentations at International Conferences

(1) K. Takahashi, T. Ohtou, A. T. Putra, K. Shimizu, and T. Hiramoto, “Body factor and leakage current reduction in bulk FinFETs,” *2007 IEEE Silicon Nanoelectronics Workshop*, Kyoto, Japan, Jun. 2007.

(2) J. S. Park, T. Saraya, K. Miyaji, K. Shimizu, A. Higo, K. Takahashi, Y. H. Yi, H. Toshiyoshi, and

T. Hiramoto, "Characteristic Modulation of Silicon MOSFETs and Single Electron Transistors with a Movable Gate Electrode," *2008 IEEE Silicon Nanoelectronics Workshop*, Honolulu, HI, USA, Jun. 2008.

(3) J. Chen, T. Saraya, K. Miyaji, K. Shimizu and T. Hiramoto, "Experimental study of mobility in [110]- and [100]-directed multiple silicon nanowire GAA MOSFETs on (100) SOI," *2008 VLSI symposium Technology*, pp. 32–33, Honolulu, HI, USA, Jun. 2008.

(4) S. W. Bedell, N. Daval, K. Fogel, K. Shimizu, J. Ott, J. Newbury, and D. K. Sadana, "Opportunities and challenges for germanium and silicon- germanium channel p-FETs (invited)," *215th ECS spring meeting*, San Francisco, CA, USA, May 2009.

(5) M. Suzuki, T. Saraya, K. Shimizu, T. Sakurai and T. Hiramoto, "Post-fabrication self-convergence scheme for suppressing variability in SRAM cells and logic transistors," *2009 VLSI symposium on Technology*, pp. 148–149, Kyoto, Japan, Jun. 2009.

(6) C. Lee, A. T. Putra, K. Shimizu and T. Hiramoto, "V_{th} Dependence of V_{th} Variability in Intrinsic Channel SOI MOSFETs with Ultra-Thin BOX," *International Conference on Solid State Devices & Materials (SSDM)*, pp. 10–11, Sendai, Oct. 2009.

(7) M. Suzuki, T. Saraya, K. Shimizu, T. Sakurai and T. Hiramoto, "Improvement of Static Noise Margin in SRAM by Post-Fabrication Self-Convergence Technique," *International Semiconductor Device Research Symposium (ISDRS)*, TP7–03, University College, MD, USA, Dec. 2009.

Other Presentations at Domestic Conferences

(1) 陳 杰智, 清水 健, 筒井 元, 平本 俊郎, "(100) 面 UTB MOSFET における音響フォノン散乱移動度の劣化機構の考察," 第 68 回応用物理学会学術講演会, 7p–ZL–9, 北海道, 2007 年 8 月.

(2) 陳 杰智, 更屋 拓哉, 宮地幸祐, 清水 健, 平本 俊郎, "(100) SOI 基板上に作製した [110] 及び [100] 方向マルチシリコンナノワイヤ GAA MOSFET の移動度評価," 応用物理学会シリコンテクノロジー分科会, 東京, 2008 年 7 月.

(3) 陳 杰智, 更屋 拓哉, 宮地幸祐, 清水 健, 平本 俊郎, "[110] 及び [100] 方向マルチシリコンナノワイヤ GAA MOS トランジスタにおける電子移動度評価," 第 69 回応用物理学会学術講演会, 4p–E–14, 名古屋, 2008 年 9 月.

(4) 鈴木 誠, 更屋 拓哉, 清水 健, 桜井貴康, 平本 俊郎, "SRAM およびロジックトランジスタにおける特

性ばらつき一括自己修復手法," 応用物理学会シリコンテクノロジー研究会, pp. 32–35, 東京, 2009 年 7 月.

(5) イ チホ, アリフィンタムシルプトラ, 清水 健, 平本 俊郎, "極薄 BOX を有する SOI MOSFET におけるしきい値電圧ばらつきのしきい値電圧依存性," 第 70 回応用物理学会学術講演会, 8a–TE–6, 富山, 2009 年 9 月.

(6) 鈴木 誠, 更屋 拓哉, 清水 健, 平本 俊郎, "ロジックトランジスタにおける特性ばらつき一括自己修復手法," 第 70 回応用物理学会学術講演会, 8a–TE–7, 富山, 2009 年 9 月.

(7) 鈴木 誠, 更屋 拓哉, 清水 健, 平本 俊郎, "SRAM における特性ばらつき一括自己修復手法," 第 70 回応用物理学会学術講演会, 8a–TE–8, 富山, 2009 年 9 月.

Awards

(1) 第 6 回 IEEE EDS Japan Chapter Student Award, 2008 年 1 月.

(2) 第 7 回 IEEE EDS Japan Chapter Student Award, 2009 年 1 月.

(3) 第 8 回 IEEE EDS Japan Chapter Student Award, 2010 年 1 月.

(4) 第 26 回（2009 年春期）応用物理学会講演奨励賞.

Reference

[1] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 256–268, 1974.

[2] C. H. Diaz, K. Goto, H. Huang, Y. Yasuda, C. Tsao, T. Chu, W. Lu, V. Chang, Y. Hou, Y. Chao, P. Hsu, C. Chen, K. Lin, J. Ng, W. Yang, C. Chen, Y. Peng, C. C. (Ryan), C. Chen, M. Yu, L. Yeh, K. You, K. Chen, K. Thei, C. Lee, S. Yang, J. Cheng, K. Huang, J. Liaw, Y. Ku, S. Jang, H. Chuang, and M. Liang, "32nm gate-first high-k/metal-gate technology for high performance low power applications," in *IEDM Tech. Dig.*, Dec 2008, pp. 629–632.

[3] F. Arnaud, J. Liu, Y. Lee, K. Lim, S. Kohler, J. Chen, B. Moon, C. Lai, M. Lipinski, L. Sang, F. Guarin, C. Hobbs, P. Ferreira, K. Ohuchi, J. Li, H. Zhuang, P. Mora, Q. Zhang, D. Nair, D. Lee, K. Chan, S. Satadru, S. Yang, J. Koshy, W. Hayter, M. Zaleski, D. Coolbaugh, H. Kim, Y. Ee, J. Sudijono, A. Thean, M. Sherony, S. Samavedam, M. Khare, C. Goldberg, and A. Steegen, "32nm general purpose bulk CMOS technology for high performance applications at low voltage," in *IEDM Tech. Dig.*, Dec 2008, pp. 633–636.

[4] S. Natarajan, M. Armstrong, M. Bost, R. Brain, M. Brazier, C.-H. Chang, V. Chikarmane, M. Childs, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, I. Jin, C. Kenyon, S. Klopcic, S.-H. Lee, M. Liu, S. Lodha, B. McFadden, A. Murthy, L. Neiberg, J. Neirynck, P. Packan, S. Pae, C. Parker, C. Pelto, L. Pipes, J. Sebastian, J. Seiple, B. Sell, S. Sivakumar, B. Song, K. Tone, T. Troeger, C. Weber, M. Yang, A. Yeoh, and K. Zhang, "A 32nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and $0.171\mu m^2$ SRAM cell size in a 291Mb array," in *IEDM Tech. Dig.*, Dec 2008, pp. 941–943.

[5] S.-Y. Wu, J. Liaw, C. Lin, M. Chiang, C. Yang, J. Cheng, M. Tsai, M. Liu, P. Wu, C. Chang, L. Hu, C. Lin, H. Chen, S. Chang, S. Wang, P. Tong, Y. Hsieh, K. Pan, C. Hsieh, C. Chen, C. Yao, C. Chen, T. Lee, C. Chang, H. Lin, S. Chen, J. Shieh, M. Tsai, S. Jang, K. Chen, Y. Ku, Y. See, and W. Lo, "A highly manufacturable 28nm CMOS low power platform technology with fully functional 64Mb SRAM using dual/tripe gate oxide process," in *VLSI Symp. Tech. Dig.*, Jun 2009, pp. 210–211.

[6] R. Keyes, "Effects of randomness in the distribution of impurity ions on FET thresholds in integrated electronics," *IEEE Journal of Solid-State Circuits*, vol. 10, pp. 245–247, 1975.

[7] B. Hoeneisen and C. A. Mead, "Fundamental limitations in microelectronics-I. MOS technology," *Solid State Electronics*, vol. 15, pp. 819–829, 1972.

[8] T. Mizuno, J. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopand number in MOSFET's," *IEEE Transaction on Electron Devices*, vol. 41, pp. 2216–2221, 1994.

[9] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-$0.1\mu m$ MOSFET's: A 3-D "atomistic" simulation study," *IEEE Transaction on Electron Devices*, vol. 45, pp. 2505–2513, 1998.

[10] Y.Taur and T.H.Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University press, 1998.

[11] J. P. Colinge, *Silicon-on-insulator Technology: Materials to VLSI*. Kluwer Academic Publishers, 1991.

[12] L. Su, J. Jacobs, J. Chung, and D. Antoniadis, "Deep-submicrometer channel design in silicon-on-insulator (SOI) MOSFET's," *IEEE Electron Device Letters*, vol. 15, pp. 183–185, 1993.

[13] V. Trivedi and J. Fossum, "Scaling fully depleted SOI CMOS," *IEEE Transaction on Electron Devices*, vol. 50, pp. 2095–2103, 2003.

[14] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFET's," *IEEE Electron Device Letters*, vol. 14, pp. 569–571, 1993.

[15] S.Takagi, J.Koga, and A.Toriumi, "Subband structure engineering for performance enhancement of Si MOSFETs," in *IEDM Tech. Dig.*, Dec 1997, pp. 219–222.

[16] M.Shoji, Y.Omura, and M.Tomizawa, "Physical basis and limitation of universal mobility behavior in fully depleted silicon-on-insulator Si inversion layers," *J. Applied Physics*, vol. 81, no. 2, pp. 786–794, Jan 1997.

[17] K.Uchida, H.Watanabe, A.Kinoshita, J.Koga, T.Numata, and S.Takagi, "Experimental study on carrier transport machanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5nm," in *IEDM Tech. Dig.*, Dec 2002, pp. 47–50.

[18] D. Esseni, M. Mastrapasqua, G. Celler, F. Baumann, C. Fiegna, L. Selmi, and E. Sangiorgi, "Low field mobility of ultra-thin SOI n- and p-MOSFETs: Measurements and implications on the performance of ultra-short MOSFETs," in *IEDM Tech. Dig.*, Dec 2000, pp. 671–674.

[19] G. Tsutsui, M. Saitoh, and T. Hiramoto, "Mobility enhancement due to volume inversion in (110)-oriented ultra-thin body double-gate nMOSFETs with body thickness less than 5nm," in *IEDM Tech. Dig.*, Dec 2005, pp. 747–750.

[20] F.Stern and W.E.Haward, "Properties of semiconductor surface inversion layers in the electric quantum limit," *Physical Review*, vol. 163, no. 3, pp. 816–835, Nov 1967.

[21] S. W. Bedell, A. Majumdar, J. Ott, J. Arnold, K. Fogel, S. Koester, and D. Sadana, "Mobility scaling in short-channel length strained Ge-on-insulator p-MOSFETs," *IEEE Electron Device Letters*, vol. 29, pp. 811–813, 2008.

[22] G. Nicholas, B. D. Jaeger, D. Brunco, P. Zimmerman, G. Eneman, K. Martens, M. Meuris, and M. Heyns, "High-performance deep submicron Ge pMOSFETs with halo implants," *IEEE Transaction on Electron Devices*, vol. 54, pp. 2503–2511, 2007.

[23] M. Kobayashi, T. Irisawa, B. Kope, Y. Sun, K. Saraswat, H.-S. Wong, P. Pianetta, and Y. Nishi, "High quality geo_2/ge interface formed by SPA radical oxidation and uniaxial stress engineering for high performance Ge nMOSFETs," in *VLSI symp. Tech. Dig.*, Jun 2009, pp. 76–77.

[24] M. Yokoyama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "High mobility metal S/D III-V-on-insulator MOSFETs on a Si substrate using direct wafer bonding," in *VLSI symp. Tech. Dig.*, Jun 2009, pp. 242–243.

[25] H.-C. Chin, X. Gong, X. Liu, Z. Lin, and Y.-C. Yeo, "Strained $In_{0.53}Ga_{0.47}As$ n-MOSFETs: Performance boost with in-situ doped lattice-mismatched source/drain stressors and interface engineering," in *VLSI symp. Tech. Dig.*, Jun 2009, pp. 244–245.

[26] M.Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul 1997.

[27] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 133–141, Feb 2002.

[28] V. Barral, T. Poiroux, F. Rochette, M. Vinet, S. Barraud, O. Faynot, L. Tosti, F. Andrieu, M. Casse, B. Previtali, R. Ritzenthaler, P. Grosgeorges, E. Bernard, G. LeCarval, D. Munteanu, J. Autran, and S. Deleonibus, "Will strain be useful for 10nm quasi-ballistic FDSOI devices? an experimental study," in *VLSI Symp. Tech. Dig.*, Jun 2007, pp. 128–129.

[29] S.Takagi, A.Toriumi, M.Iwase, and H.Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I - effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec 1994.

[30] S.Takagi and M.Takayanagi, "Experimental evidence of inversion-layer mobility lowering in ultrathin gate oxide metal-oxide-semiconductor field-effect-transistors with direct tunneling current," *Jpn. J. Applied Physics*, vol. 41, no. 1, pp. 2348–2352, Jan 2002.

[31] M.V.Fischetti, D.A.Neumayer, and E.A.Cartier, "Effective electron mobility in Si inversion layers in

metal-oxide-semiconductor systems with a high-κ insulator: The role of remote phonon scattering," *J. Applied Physics*, vol. 90, no. 9, pp. 4587–4608, Nov 2001.

[32] A. Gold, "Electronics transport properties of a two-dimensional electron gas in a silicon quantum-well structure at low temperature," *Physical Review B*, vol. 35, no. 2, pp. 723–733, Jan 1987.

[33] K. Uchida, J. Koga, and S. Takagi, "Experimental study on carrier transport mehcanisms in double- and single-gate ultrahin-body MOSFETs - coulomb scattering, volume inversion, and δ t_{SOI}-induced scattering-," in *IEDM Tech. Dig.*, Dec 2003, pp. 805–808.

[34] G. Tsutsui, M.Saitoh, and T.Hiramoto, "Experimental study on superior mobility in (110)-oriented UTB SOI pMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 836–838, Nov 2005.

[35] C. S. Smith, "Piezoresistance effects in germanium and silicon," *Physical Review*, vol. 94, pp. 42–49, 1954.

[36] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Trans. Electron Devices*, vol. 29, pp. 64–70, 1982.

[37] M. Saitoh, S. Kobayashi, and K. Uchida, "Physical understandings of fundamental properties of Si (110) pMOSFETs -inversion-layer capacitance, mobility universality, and uniaxial stress effects-," in *IEDM Tech. Dig.*, Dec 2007, pp. 711–714.

[38] S. E. Thompson, G. Sun, K. Wu, J. Kim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *IEDM Tech. Dig.*, Dec 2004, pp. 221–224.

[39] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-Si: Extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, pp. 1010–1020, 2006.

[40] B. Yang, A. Waite, H. Yin, J. Yu, L. Black, D. Shidambarrao, A. Domenicucci, X. Wang, S. H. Ku, Y. Wang, H. V. Meer, B. Kim, H. Nayfeh, S. D. Kim, K. Tabakman, R. Pal, K. Nummy, B. Greene, P. Fisher, J. Liu, Q. Liang, J. Holt, S. Narasimha, Z. Luo, H. Utomo, X. Chen, D. Park, C. Y. Sung, R. Wachnik, G. Freeman, D. Schepis, E. Maciejewski, M. Khare, E. Leobandung, S. Luning, and P. Agnello, "(110) channel, SiON gate-dielectric pMOS with record high I_{on} = 1mA/μm through channel stress and source drain external resistance enginnering," in *IEDM Tech. Dig.*, Dec 2007, pp. 1032–1034.

[41] H. C.-H. Wang, S.-H. Huang, C.-W. Tsai, H.-H. Lin, T.-L. Lee, S.-C. Chen, C. H. Diaz, M.-S. Liang, and J. Y.-C. Sun, "High-performance pmos devices on (110)/<111'> substrate/channel with multiple stressors," in *IEDM Tech. Dig.*, Dec 2006, pp. 67–70.

[42] P. Packan, S. Cea, H. Deshpande, T. Ghani, M. Giles, O. Golonzka, M. Hattendorf, R. Kotlyar, K. Kuhn, A. Murthy, P. Ranade, L. Shifren, C. Weber, and K. Zawadzki, "High performance hi-k + metal gate strain enhanced transistors on (110) silicon," in *IEDM Tech. Dig.*, Dec 2008, pp. 63–67.

[43] M. Yang, V. W. C. Chan, K. K. Chan, L. Shi, D. M. Fried, J. H. Stathis, A. I. Chou, E. Gusev, J. A. Ott, L. E. Burns, M. V. Fischetti, and M. Ieong, "Hybrid-orientation technology (HOT): opportunities and challenges," *Trans. Electron Devices*, vol. 53, no. 2, pp. 965–978, Feb 2006.

[44] M. Saitoh, N. Yasutake, Y. Nakabayashi, T. Numata, and K. Uchida, "Comprehensive performance assessment of scaled (110) CMOSFETs based on understandings of STI stress effects and velocity saturation," in *IEDM Tech. Dig.*, Dec 2008, pp. 573–576.

[45] M.V.Fischetti, Z.Ren, P.M.Solomon, M.Yang, and K.Rim, "Six-band k 鐔 p calculation of the hole mobility in silicon inversion layers: dependence on surface orientation, strain, and silicon thickness," *J. Applied Physics*, vol. 94, no. 2, pp. 1079–1095, Jul 2003.

[46] H.Irie, K.Kita, K.Kyuno, and A.Toriumi, "In-plane mobility anisotropy and universality under uni-axial strains in n- and p-MOS inversion layers on (100), (110), and (111) Si," in *IEDM Tech. Dig.*, Dec 2004, pp. 225–228.

[47] K. Shimizu, G. Tsutsui, D. Januar, T. Saraya, and T. Hiramoto, "Experimental study on break-down of mobility universality in <100>-directed (110)-oriented pMOSFETs," *IEEE Transaction on Nanotechnology*, vol. 6, pp. 358–361, May 2007.

[48] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-

semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 101, no. 104503, pp. 1–22, Jan 2007.

[49] S. Mayuzumi, S. Yamakawa, D. Kosemura, M. Takei, K. Nagata, H. Akamatsu, K. Aamari, Y. Tateshita, H. Wakabayashi, M. Tsukamoto, T. Ohno, M. Saitoh, A. Ogura, and N. Nagashima, "Comparative study between Si (110) and (100) substrates on mobility and velocity enhancements for short-channel highly-strained pfets," in *VLSI symp. on Technology Tech. Dig.*, Jun 2009, pp. 14–15.

[50] "International technology roadmap for semiconductors, 2008 update," 2008, available online, http://www.itrs.net.

[51] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (-1.5 GPa) channel stress," *IEEE Electron Device Lett.*, vol. 28, pp. 58–61, 2005.

[52] K. Uchida, A. Kinoshita, and M. Saitoh, "Carrier transport in (110) nMOSFETs: Subband structures , non-parabolicity, mobility characteristics, and uniaxial stress enginnering," in *IEDM Tech. Dig.*, Dec 2006, pp. 1019–1021.

[53] G. Tsutsui and T. Hiramoto, "Mobility and threshold-voltage comparison between (110)- and (100)-oriented ultrathin-body silicon MOSFETs," *IEEE Transaction Electron Devices*, vol. 50, pp. 2582–2588, Oct 2006.

[54] H. Takeda, N. Morii, and C. Hamaguchi, "Self-consistent calculations of two-dimensional electronic states in SOI-MOSFETs using full-band modeling," *Physica B*, vol. 314, pp. 377–380, 2002.

[55] D. Esseni and P. Palestri, "Linear combination of bulk bands method for investigating the low-dimensional electron gas in nanostructured devices," *Physical Review B*, vol. 72, p. 165342, 2005.

[56] J. Yamauchi, "Electronic transport properties of thin, channel regions from SOI through GOI: A first principle study," *Thin Solid Films*, vol. 508, pp. 342–345, 2006.

[57] E. Ungersboeck, V. Sverdlov, H. Kosina, and S. Selberherr, "Low-field electron mobility in stressed UTB SOI MOSFETs for differnt substrate orientations," *ECS Trans.*, vol. 3, pp. 45–54, 2006.

[58] H. Fukutome, K. Okabe, K. Okubo, H. Minakata, Y. Morisaki, K. Ikeda, T. Yamamoto, K. Hosaka, Y. Momiyama, M. Kase, and S. Satoh, "(110) nMOSFETs competitive to (001) nMOSFETs: Si migration to create (331) facet and ultra-shallow Al implantation after NiSi formation," in *IEDM Tech. Dig.*, Dec 2008, pp. 59–62.

[59] M. Saitoh, N. Yasutake, Y. Nakabayashi, K. Uchida, and T. Numata, "Understanding of strain effects on high-field carrier velocity in (100) and (110) CMOSFETs under quasi-ballistic transport," in *IEDM Tech. Dig.*, Dec 2009, pp. 469–472.

[60] M. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Letters*, vol. 22, pp. 591–593, 2001.

[61] A. Lochtefeld and D. A. Antoniadis, "Investigating the relationship between electron mobility and velocity in deeply scaled nMOS via mechanical stress," *IEEE Electron Device Letters*, vol. 22, pp. 293–295, 2001.

[62] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, and B. Doris, "Extremely thin SOI (ETSOI) CMOS with record low variability low power system-on-chip applications," in *IEDM Tech. Dig.*, Dec 2009, pp. 49–52.

[63] K.Uchida, R.Zednik, C.H.Lu, H.Jagannathan, J.McVittie, P.C.McIntyre, and Y.Nishi, "Experimental study of biaxial and uniaxial strain effects on carrier mobility in bulk and ultrathin-body SOI MOSFETs," in *IEDM Tech. Dig.*, Dec 2004, pp. 229–232.

[64] M. Fischetti and S. Laux, "More-than-universal mobility in double-gate SOI p-FETs with sub–10-nm body thickness –role of light-hole band and compatibility with uniaxial stress engineering–," in *IEDM Tech. Dig.*, Dec 2007, pp. 707–710.

[65] M.Chan, F.Assaderaghi, S.A.Parke, C.Hu, and P.K.Ko, "Recessed-channel structure for fabricating ultrathin soi mosfet with low series resistance," *IEEE Electron Device Lett.*, vol. 15, no. 1, pp. 22–24,

Jan 1994.

[66] M. Fischetti and S. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *Journal of Applied Physics*, vol. 80, pp. 2234–2252, 1996.