Abstract

For nearly forty years, Si-based LSI systems have made a tremendous advance in performance by miniaturizing the metal-oxide-semiconductor field-effect-transistor (FET) size, following the "scaling rule." However, as the size of FETs shrinks, one big, physically inevitable problem becomes prominent than ever: threshold voltage (V_{th}) variability. As one LSI consists of a few billions of FETs, V_{th} variability results in severe yield degradation. To continue enhancing LSI performance for another decade, V_{th} variability problem must be dealt and solved.

To overcome V_{th} variability problem, the channel dopant concentration should be decreased. However, a reduction in dopant concentration means a weak immunity to the short channel effect, which is known as another big problem. Thus, the increase or decrease in dopant concentration, which has been a key in LSI scaling for many years, cannot solve problems in state-of-the-art FETs.

For further scaling, a silicon-on-insulator (SOI) technology is thought to be one of the most promising FET structures in near future. SOI-based strictures, including partially-depleted, fully-depleted, double-gate, Fin-type FET, and gate-all-around structure, enables us to obtain the lower doping concentration because of their structural confinement to the channel. However, to suppress the short channel effectively with non-doped SOI-based structures, the SOI thickness should be one quarter of the gate length in SOI FETs, and a half of it in double-gate FETs or FinFETs, which means the SOI thickness is less than 10 nm in near future. In such a thin SOI, the quantum confinement effect significantly affects the carrier conduction, which is not fully taken into consideration in the design of FETs.

The purpose of this dissertation is to address the possibility of (110)-oriented CMOS FETs, based on the experimental investigation on the effects of both the quantum confinement and the strain on carrier transport in SOI FETs. The results obtained in this dissertation are summarized as follows.

Hole mobility in (110) surface benefits from the quantum confinement effects. Stronger quantum

confinement, such as higher surface electric field or thinner SOI thickness, reduces the conduction effective mass especially in <110> direction. Therefore, the advantage of hole mobility in (110) FETs over that in (100) FETs is prominent especially under strong quantum confinement.

The sensitivity of hole motility to the strain is smaller in (110) surface than that in (100) surface in both bulk and ultrathin body FETs. The benefits from the strain and the quantum confinement seem to saturate if they are larger than a certain amount. Despite the smaller sensitivity to the strain, (110)-oriented ultrathin body pFETs is expected to have higher performance than (100)-oriented ultrathin body pFETs thanks to originally high hole mobility.

The non-parabolicity in <110> direction leads to the invalidity of the effective mass approximation, and it is more prominent in ultrathin body FETs. <110>-directed electron mobility is always lower than <100>-directed electron mobility in bulk nFETs, however, the electron mobility in <110> direction is higher than that in <100> direction in an ultimately thin SOI. Considering that the hole mobility in <110> direction is higher than that in <100> direction, higher CMOS circuit performance can be obtained with both p- and nFETs in <110> direction in ultimately thin SOI CMOS circuits.

The sensitivity of electron mobility to the strain is comparable to bulk FETs if the SOI is thick enough, though the sensitivity reduces as SOI thins. This is because the subband energy shift, which is thought to be the main mobility modulation mechanism, won't affect the electron mobility in ultrathin body FETs. However, the strain is still effective to enhance electron mobility in ultrathin body FETs.

The CMOS performance of (110) ultrathin body FETs is higher if the strain is low enough. As the strain increases, the performance of (100) CMOS increases, though the (110) CMOS doesn't increase much. Therefore, it is concluded that the CMOS FETs utilizing (110)-oriented ultrathin body FETs is one of the performance boosting technologies for the low-cost devices instead of high performance devices with high amount of strain.