CHAPTER 5

LOW NOISE TECHNOLOGY

Acceleration by reducing program cycles, Npulse

5.1 Introduction

The most important design problem in the 3V multi-level cell and the low-voltage multi-level cell is that the simultaneously written states, Nstate is three times larger than that of the single-level cell. This problem is solved by introducing the multipage cell technology as discussed in Chapter 3. Then, to increase the program throughput further, the major problem is the circuit noise. As described in Chapter 2, in the case of the multi-level cell, the program speed drastically degrades if the circuit noise becomes large. To control the cell Vth precisely, the program step voltage, ⊿Vpgm should be small, which increases the number of pulses, Npulse.

In this chapter, the effect circuit on the performance is analyzed. Next, two circuit technologies are presented to eliminate the circuit noise. First, a double-level Vth select gate array architecture [1], [2] is proposed for the 3V multi-level cell. This novel architecture is ideal in that it not only eliminates the circuit noise but also minimize the die size and the production costs. However, this new array cannot be used for the low-voltage multi-level cell because the low load capacitance technology described in Chapter 4 cannot be used in this new array. Instead, a Vcc bit-line shield sensing scheme [3], [4] is proposed for the low voltage multi-level cell, which also eliminates the circuit noise and improve the program speed.

In Section 5.2 it is explained that array noise during a bit-by-bit program verify operation in NAND Flash Memories, causes a threshold voltage fluctuation which leads to the program speed degradation. This threshold voltage fluctuation can not be eliminated by the bit-by-bit program verify technique. The fluctuation is composed of a threshold voltage shift in both positive and negative direction, as shown in Fig.5.1. The array noise is mainly dominated by 1) the inter bit-line capacitive coupling noise and 2) the source-line noise caused by the high resistance of the diffused source-line. In Section 5.2, the inter bit-line capacitive coupling noise is described. Next, it will be explained that even though inter bit-line capacitive coupling noise is eliminated by using a shielded bit-line sensing method, source-line noise definitely worsens the threshold voltage control. In Section 5.3, a new

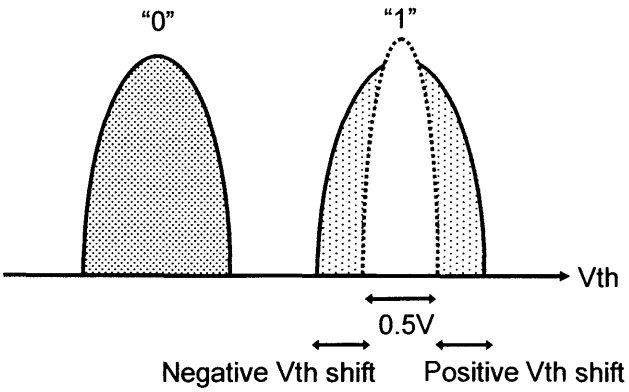


Fig.5.1 Schematic threshold voltage distribution. The threshold voltage distribution without array noise can be narrowed to 0.5V if the program voltage increment is 0.5V. Due to array noise, threshold voltages of memory cells shift in both positive and negative directions.

array architecture, a double-Level Vth select gate array architecture, is introduced to eliminate both the source-line noise and the inter bit-line capacitive coupling noise for the 3V multi-level cell. This architecture enables a very accurate threshold voltage control without cell area overhead and a fast programming. In Section 5.4, the Vcc bit-line shield sensing method is introduced as a solution for the low voltage multi-level cell. Finally, the conclusion will be given in Section 5.5.

5.2 Circuit noise issues deteriorating Vth control

Fig.5.2 shows a memory block in a conventional NAND-type memory cell array [5-7]. The memory block is composed of a number of NAND cell units, for example 4k units which share 16 control gates (CG1～CG16), two select gates (SG1,SG2) and a common diffused source-line. Each unit is connected to a bit-line control circuit via a bit-line (BL0～BL2). All memory cells, which share the same control gates are simultaneously read and programmed by using the bit-line control circuits.

The threshold voltages of the memory cells are determined in the following manner [8], [9]. After the bit-lines are precharged to a high level, for example 3/5Vcc, a reference voltage Vvrfy is applied to the selected control gate, while the select gates are raised to Vcc and the un-selected control gates are raised to a read voltage, Vread. These voltages are kept constant during a predetermined period, for example 4μs. After that, in case a bit-line voltage decreases below a low level, for example 1/2Vcc, the threshold voltage of the

corresponding memory cell is determined to be lower than the reference voltage, Vvrfy. On the other hand, if the bit-line voltage stays above 1/2Vcc, the threshold voltage of the memory cell is determined to be higher than the reference voltage, Vvrfy.

In a bit-by-bit program operation [10], [11], program verify, which monitors the threshold voltage of the memory cells is carried out after each programming pulse. If the threshold voltage reaches the desired level, additional programming of the corresponding memory cells is inhibited. Programming and program verify are repeated until all selected memory cells are sufficiently programmed. Therefore, by using this program scheme, in principle, the threshold voltage of the memory cells can be controlled precisely.

However, if the cell read current or bit-line voltage fluctuates due to array noise during program verify, the threshold voltage will also vary. The fluctuation of the threshold voltage results in a widened programmed threshold voltage distribution.

5.2.1 Inter bit-line capacitive coupling noise

As the bit-line pitch is narrowed, the coupling noise from adjacent bit-lines becomes more significant. In a NAND Flash Memory, a 16-bit NAND-type cell array has only 1/32 contact hole per memory cell. Thus, the capacitance ratio of the bit-line-bit-line capacitance and the total bit-line capacitance is large in comparison with a NOR-type flash memory [12-16]. This large capacitive coupling ratio causes a large inter bit-line capacitive coupling noise [17].

In this section, the threshold voltage fluctuation is discussed, focusing on the fluctuation

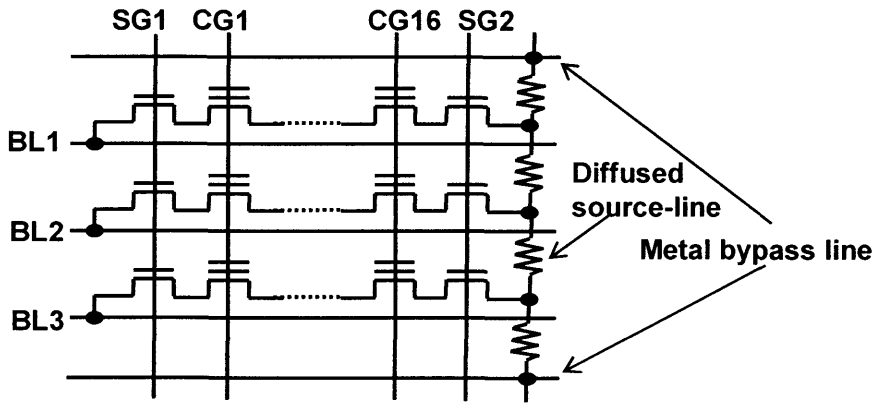


Fig.5.2 A NAND-type cell array. Each NAND cell unit shares sixteen control gates, two select gates, and a diffused source-line which is shunted with metal bypass lines. As the number of metal bypass lines increases, the source-line resistance decreases with a drawback of a cell area overhead.

caused by the inter bit-line capacitive coupling noise. For simplicity, a 2-level memory cell, which can have two programmed states "0" or "1" (Fig.5.1), is considered. The "0"-state is equal to the erased state which has a negative threshold voltage. A "1"-state memory cell has a threshold voltage higher than 0.5V. In order to verify the "1"-state, the selected control gate is raised to 0.5V during a program verify operation.

Fig.5.3 shows the worst condition during a program verify operation. In this figure, "Cell A" is connected to bit-line BL1. In Fig.5.3 (a), "Cell A" is programmed. The neighboring memory cells are still in the erased state and therefore the voltages of the bit-lines BL0 and BL2 decrease to 0V. Under this condition, the BL1 voltage can be significantly reduced, because in addition to the cell read current through "Cell A", the capacitive coupling with the adjacent bit-lines BL0 and BL2 lower the voltage of BL1, as shown in Fig.5.3(a). After that, if the neighboring cells are programmed (Fig.5.3(b)), no cell read current flows through the neighboring cells and there is no inter bit-line capacitive coupling noise, as shown in Fig.5.3(b). Therefore, the voltage of BL1 does not decrease and as a result, the sensed threshold voltage of "Cell A" is higher than that in case of Fig.5.3(a).

The SPICE simulated results of the threshold voltage shift in the positive direction Δ Vth(POS) as a function of the bit-line coupling ratio *Rcp* is shown in Fig.5.4. *Rcp* is defined as $Rcp=2\times CBL\text{-}BL/Ctotal$, where *CBL-BL* is the coupling capacitance to the adjacent bit-line, and *Ctotal* is the bit-line capacitance. Due to the inter bit-line capacitive coupling noise, the threshold voltage distribution is widened in the positive direction by ΔVth(POS), as shown in Fig.5.1.

In order to suppress the inter bit-line capacitive coupling noise, a shielded bit-line sensing method has been proposed [17]. Fig.4.11 illustrates the shielded bit-line architecture. The bit-lines are alternately selected and un-selected bit-lines are grounded. For example, in case BL1A is selected during a program verify operation, the selected bit-line BL1A and the dummy bit-line BL1B are pre-charged, while neighboring bit-lines BL0A, BL0B, BL2A and BL2B are grounded. However, even if inter bit-line capacitive coupling noise is eliminated, source-line noise, another array noise causes a widening of the program threshold voltage distribution.

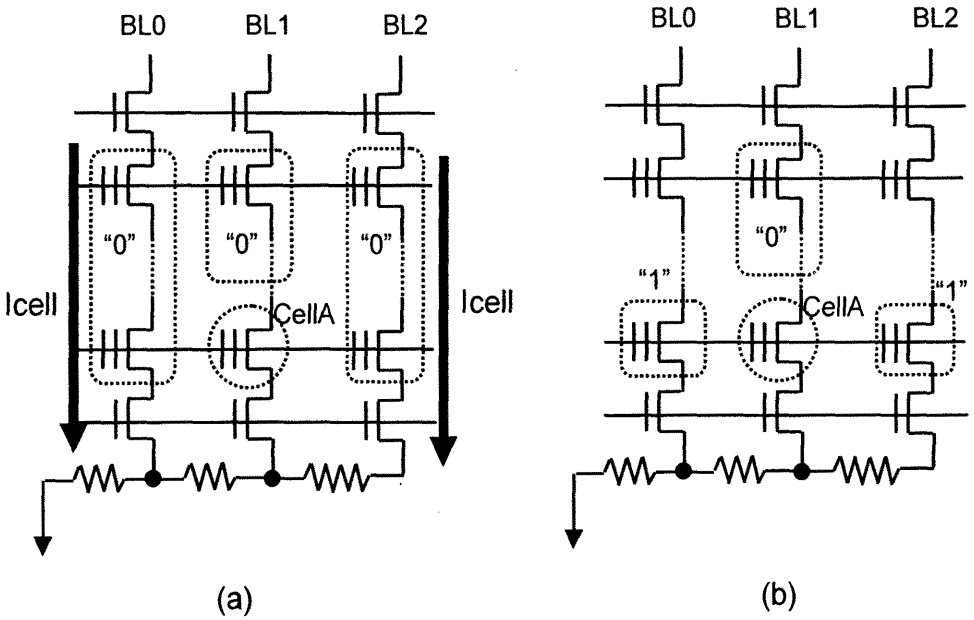


Fig.5.3 A model for the threshold voltage shift due to inter bit-line capacitive coupling noise.

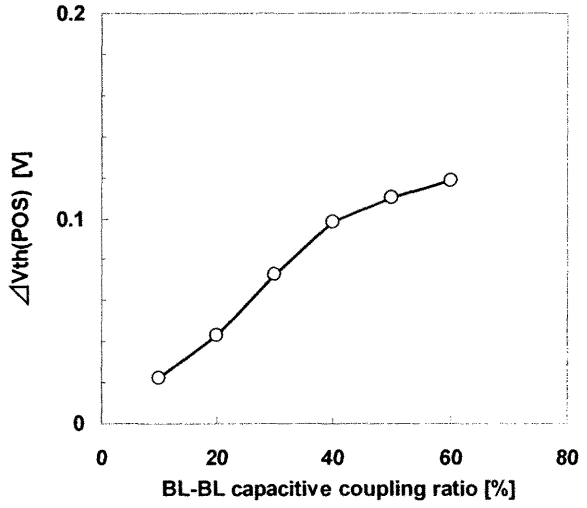


Fig.5.4 Calculated threshold voltage shift in the positive direction due to inter bit-line capacitive coupling noise.

5.2.2 Source-line noise

In a conventional NAND-type cell array, each NAND cell unit shares a common n^+ diffused source-line which is shunted with metal bypass lines parallel to the metal bit-lines, as shown in Fig.5.2 [5], [18]. The resistance of the diffused source-line becomes higher as the metal bypass line pitch increases, and causes source-line noise during a bit-by-bit program verify operation. In this section, it is explained how the source-line noise adversely affects the threshold voltage control, and causes both negative and positive threshold voltage shifts.

A. Threshold voltage shift in the negative direction due to source-line noise

A simplified model of the noise is shown in Fig.5.5. In this model, a shielded bit-line sensing method is used. Therefore, half of the memory cells sharing the same control gates are programmed and verified simultaneously. In the case that half of the memory cells, except "Cell B", stay in the erased state after the first program pulse, a large current I flows through the erased cells during the first program verify (Fig.5.5(a)). As a result, the n^+ diffused source-line bounces up to $\Delta VSL = I \times R$. The source voltage of "Cell B" is even higher than ⊿VSL, due to the resistance of the series connected memory cells. In this case, the cell read current through "Cell B" is reduced and "Cell B" is read out to be successfully programmed. However, after that, if the other memory cells that share the same control gates with "Cell B" are also programmed (Fig.5.5(b)), the ground bounce of the source-line is reduced. In that case, a larger cell read current flows through "Cell B" than in the case of the first program verify operation (Fig.5.5(a)). In this worst case, the threshold voltage of "Cell B" is ⊿Vth(NEG) below the reference voltage, Vvrfy, as shown in Fig.5.1.

The calculated threshold voltage shift in the negative direction, ⊿Vth(NEG), is shown in Fig.5.6. As the metal bypass line pitch decreases, source-line bounce is reduced and ⊿Vth(NEG) decreases, however the cell area overhead increases.

B. Threshold voltage shift in the positive direction due to source-line noise

Fig.5.7 illustrates the mechanism, of the threshold voltage shift in the positive direction. The program cycle starts from the source-line side cell and ends at the bit-line side cell to prevent interference between selected and un-selected cells. Therefore, in the case that "Cell C" is programmed, the series connected cells, except "Cell C", are still in the erased state (Fig.5.7(a)) and the series resistance is low. After programming "Cell C", and after the series connected cells are also programmed (Fig.5.7(b)), the series resistance of the NAND cell unit is higher. Therefore, the cell read current through "Cell C" is reduced compared with the case of Fig.5.7(a). In this worst case, the threshold voltage of "Cell C" is

⊿Vth(POS) higher than is expected without noise. Fig.5.8 shows the calculated threshold voltage shift in the positive direction, ⊿Vth(POS). ⊿Vth(POS) is also enhanced as the source-line bounce is increased.

C. Program speed degradation

Fig.5.9 shows the total circuit noise. In this calculation, the inter bit-line capacitive coupling noise is assumed to be eliminated by adopting a shielded-bit-line sensing scheme, as discussed above. As the metal bypass line pitch increases, the threshold voltage distribution of each level, ⊿Vth, is increased. Without the circuit noise, the program voltage increment, ⊿Vpgm is assumed 0.35V [19], [20]. Actually, since the circuit noise is 0.27V with 5% cell area overhead, ⊿Vpgm should be decreased to 0.08V. Consequently, the number of program pulses as well as the programming time increases by 338%, which is unacceptable too long.

Source-line noise is a dynamic noise, when dynamic differential sensing is used during program verify. Therefore, if the access time is increased, the threshold voltage shift can be reduced. On the other hand, in the case of the current sensing method [21], the source-line noise is continuous and causes a large threshold voltage shift, irrespective of the access time.

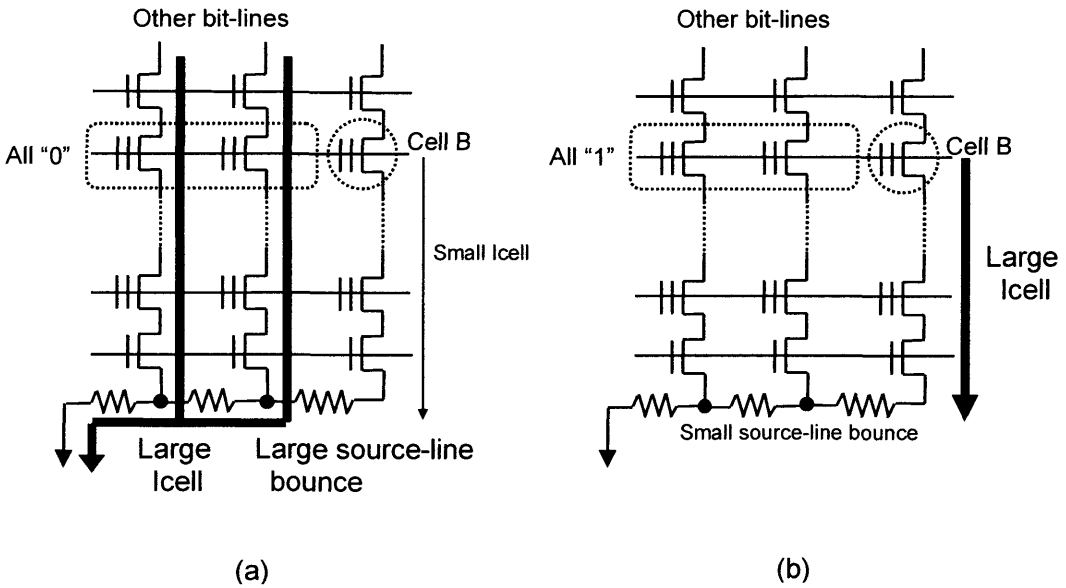


Fig.5.5 A model for the threshold voltage shift in the positive direction due to the source-line noise.

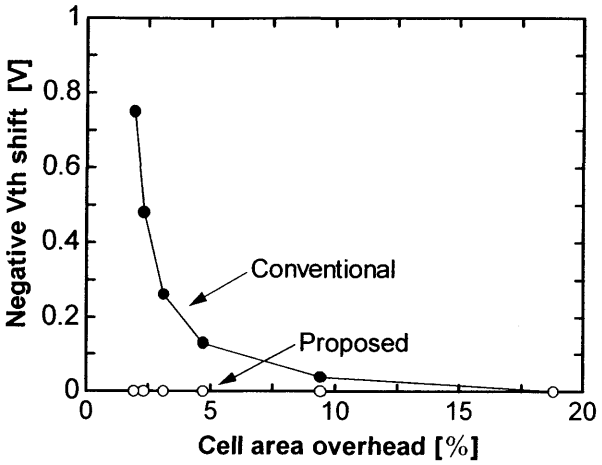


Fig.5.6 Calculated threshold voltage shift in the negative direction due to the source-line noise.

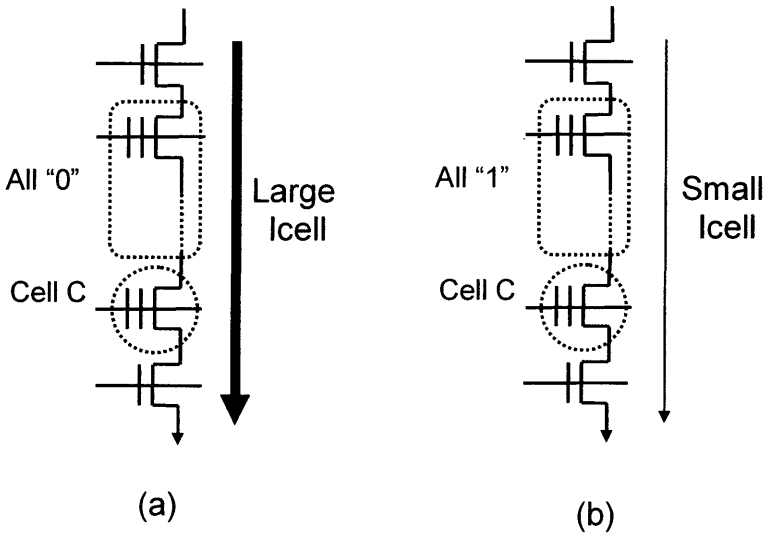


Fig.5.7 A model for the threshold voltage shift in the positive direction due to the source-line noise.

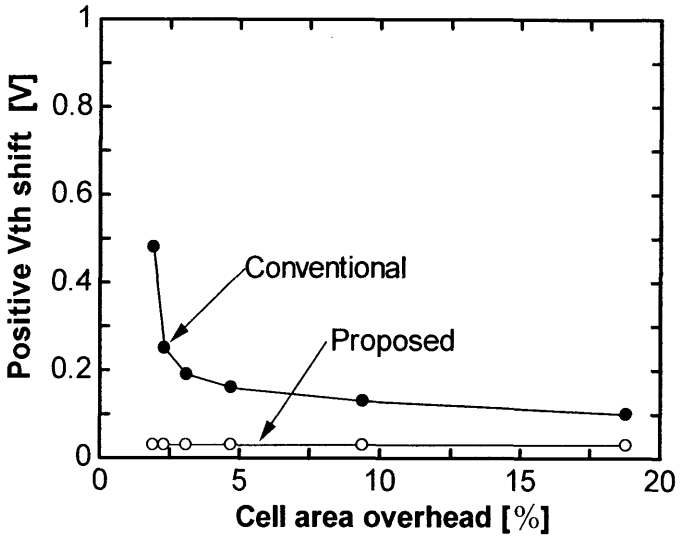


Fig.5.8 Calculated threshold voltage shift in the positive direction due to the source-line noise.

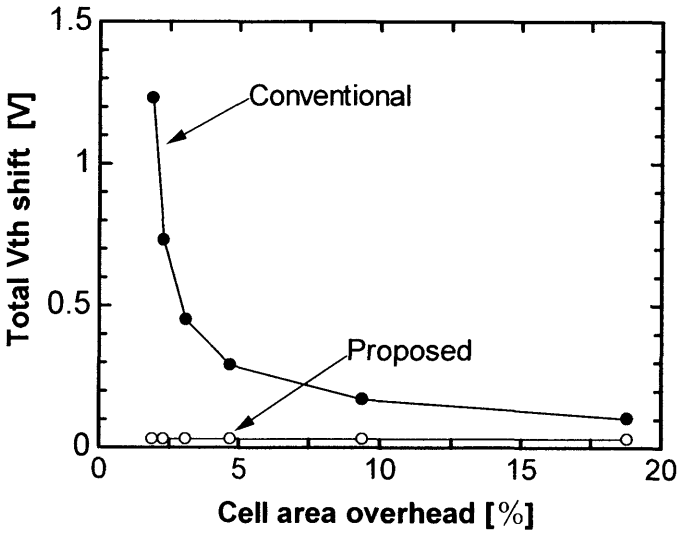


Fig.5.9 Calculated total threshold voltage shift due to the source-line noise.

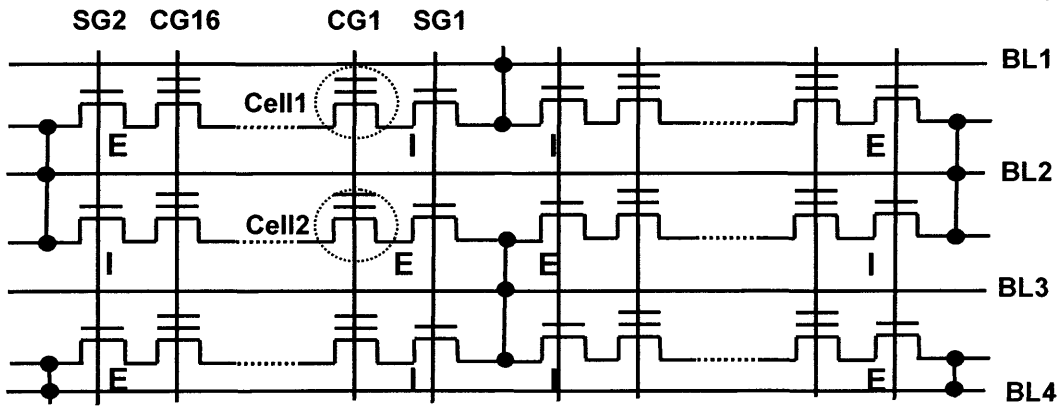
5.3 Double-level Vth select gate array architecture

A Double-Level-Vth Select Gate Array Architecture [1], [2] is illustrated in Fig.5.10. Each NAND cell unit is composed of an E-type (Vth=2.0V) select gate, an I-type (Vth=0.5V) select gate and 16 memory cells. I-type and E-type select gates are fabricated by respectively masked and un-masked channel implantations. The metal-lines are used both as bit-lines and source-lines. For example, in case BL1 acts as a bit-line, the neighboring BL2 acts as a source-line. In this structure, the high resistance diffused source-line is removed. Consequently, the source-line noise is eliminated. Compared with a conventional array, the cell area is reduced, because neither additional select transistors nor source-line-shunts are needed. The bit-line-contact pitch is relaxed, which increases the process margin when the isolation width between memory cells is reduced with trench isolation [22-25].

5.3.1 Circuit implementations

A. Read Operation

The operating conditions are summarized in Table 5.1. In the case that "Cell 1" is selected (Fig.5.11(a)) during read, the select gate line SG1 is raised to 1.5V, to turn on the I-type select gates, while the E-type select gates are tuned-off. The select gate line SG2 is



E-type select gate : Vth = 2V

I-type select gate : Vth = 0.5V

Fig.5.10 A double-level-Vth select gate array architecture. Each NAND cell unit is composed of an E-type select gate (Vth=2.0V), an I-type select gate (Vth=0.5V) and 16 memory cells.

connected to Vcc (3V), so that the E-type select gates are biased to the "ON"-states. Therefore, a cell read current may flow through unit 1, according to the stored data in "Cell 1". On the other hand, unit 2 is un-selected because the E-type select gates are turned-off. The selected bit-line BL1 is connected to a sense amplifier, while the un-selected bit-line BL2 is grounded. In this operation, BL2 acts as a low resistance source-line, forming a shield, between the selected BL1 and BL3. As a result, both source-line noise and inter bit-line capacitive coupling noise are eliminated. Due to the excellent noise immunity, a fast and stable read operation can be achieved.

On the other hand, if "Cell 2" in unit 2 is selected, the select gate lines SG1 and SG2 are respectively raised to 3V and 1.5V.

Therefore, a cell read current may flow from the precharged BL2 through unit 2 to the grounded BL3. In this case, unit 1 is un-selected, because the E-type select gate of unit 1 is turned-off.

B. Program Operation

Fig.5.11(b) explains the program operation. In Fig.5.11(b), "Cell 1" is selected. The selected control gate CG1 is raised to about 18V, and the un-selected control gates CG2~CG16 are connected to 10V. 1.5V is applied to both SG1 and SG2, in order to turn on the I-type select gates of both unit 1 and unit 2 and turn off the E-type select gates of both unit 1 and unit 2. The program data for the selected unit 1 is applied via the selected bit-line BL1. If the program data is "1","2" or "3", BL1 is grounded. In this condition, electrons are injected from the grounded channel into the floating gate by the FN-tunneling mechanism. On the other hand, in case of "0"-programming, BL1 is connected to 3V. The channel voltage during "0"-programming is raised to about 8V by the capacitive coupling with the control gates [20] and electron injection is inhibited. The un-selected bit-line BL2 is also connected to Vcc to prevent the un-selected "Cell 2" from "1","2" or "3"-programming.

	BL1	BL2	CG1	CG2-16	SG1	SG2	Pwell
Program cell1	Vcc/0V	Vcc	18V	10V	1.5V	1.5V	0V
Program cell2	Vcc	Vcc/0V	18V	10V	1.5V	1.5V	0V
Read cell1	1.3V	0V	Vsense	Vread (4.5V)	1.5V	Vread (4.5V)	0V
Read cell2	0V	1.3V	Vsense	Vread (4.5V)	Vread (4.5V)	1.5V	0V
Verify cell1	1.3V	0V	0.5V	Vread (4.5V)	1.5V	Vread (4.5V)	0V
Verify cell2	0V	1.3V	0.5V	Vread (4.5V)	Vread (4.5V)	1.5V	0V
Erase	Open	Open	0V	0V	20V	20V	20V

Table 5.1 Operation conditions

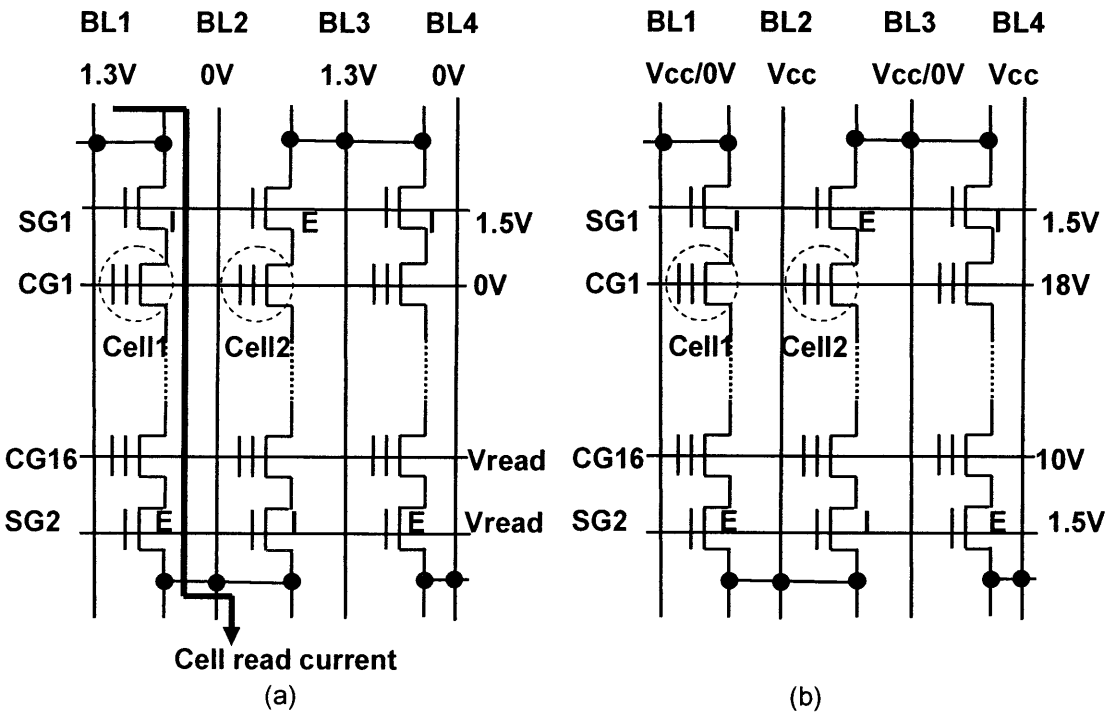


Fig.5.11 Operation principles.

(a) Read.

(b) Program.

5.3.2 Experimental results

The characteristics of the proposed cell array are summarized in Table 5.2. The cell read current paths of each NAND cell unit, from a bit-line via a selected cell to a grounded bit-line, are completely independent. Thus, the cell read current is not affected by the cell read current that flows through neighboring cells. The threshold voltage shift in the negative direction, ⊿Vth(NEG), is eliminated, independent of the value of the bit-line resistance. The threshold voltage shift in the positive direction, ⊿Vth(POS), is significantly reduced, because the source-line bounce is removed. Due to the high noise immunity, a precise threshold voltage control can be achieved, as shown in Table 5.2. The threshold voltage fluctuation which is the sum of the threshold voltage shift in the negative and positive direction is decreased from 0.27V (conventional array) to 0.03V. The program voltage increment can be increased from 0.35V (conventional array) to 0.62V. As a result, the program speed of the proposed scheme improves by 77% compared with the conventional scheme. In addition, in the proposed array, the metal bypass lines are eliminated and consequently the cell area decreases by 5%.

The effect of the array noise on the threshold voltage control was measured using a test device with 0.7um double-metal CMOS technologies. In the experiment, programming is performed by using staircase programming pulses [19], [20]. After each programming pulse, a program verify operation is carried out. In the measurement, the value for ⊿Vpgm is 0.5V and the pulse width Tpulse is 20μs. The program characteristics of the most easy-to-program memory cell and the most difficult-to-program one are shown in Fig.15 in [2]. The threshold voltage change, dVth/dt, during programming is completely constant with a value of dVpgm/dt (0.5V/20μs). Therefore, if array noise does not worsen the threshold voltage control, the threshold voltage distribution would be narrowed to ⊿Vpgm (0.5V). Fig.16 in [2] shows the measured threshold voltage distribution of a 4-level NAND-type cell, where all memory cells are "1","2" or "3"-programmed. Without verify, the threshold voltage distribution of the programmed cells in the test device is around 2.5V. The threshold voltage distribution of the conventional array increases to 0.7V because of the circuit noise. In contrast, in the proposed array, the threshold voltage distribution is narrowed to almost 0.5V.

	Total Vth shift due to the circuit noise	⊿Vpgm	Program speed	Cell area overhead
Conventional	**0.27V**	**0.35V**	-	-
Proposed	**0.03V**	**0.62V**	**77% faster**	**5% smaller**

Table 5.2 Comparison of the proposed double-level Vth select gate array and the conventional array.

5.4 Vcc bit-line shield sensing scheme

In the case of the low-voltage multi-level cell, the double-level select gate architecture described in Section 5.3 cannot be used because in the new cell array, the source-line is eliminated and therefore the low load capacitance technologies shown in Chapter 4 cannot be used. To reduce the circuit noise of the low-voltage multi-level cell, a Vcc bit-line shield sensing scheme is proposed.

Fig.5.12 compares the proposed sensing scheme with the conventional one. In the proposed scheme, the source-line is biased to Vcc and the bit-line is charged from Vss through the memory cell. As shown in Fig.5.12(a), in the conventional scheme, if the source-line bounces, the source of the cell transistor bounces and as a result, the cell read current decreases. On the other hand, in the proposed scheme shown in Fig.5.12(b), even if the source-line drops because of the source-line resistance, the drain of the cell transistor drops and therefore the cell read current does not change. By using this novel sensing scheme, the source-line noise is eliminated.

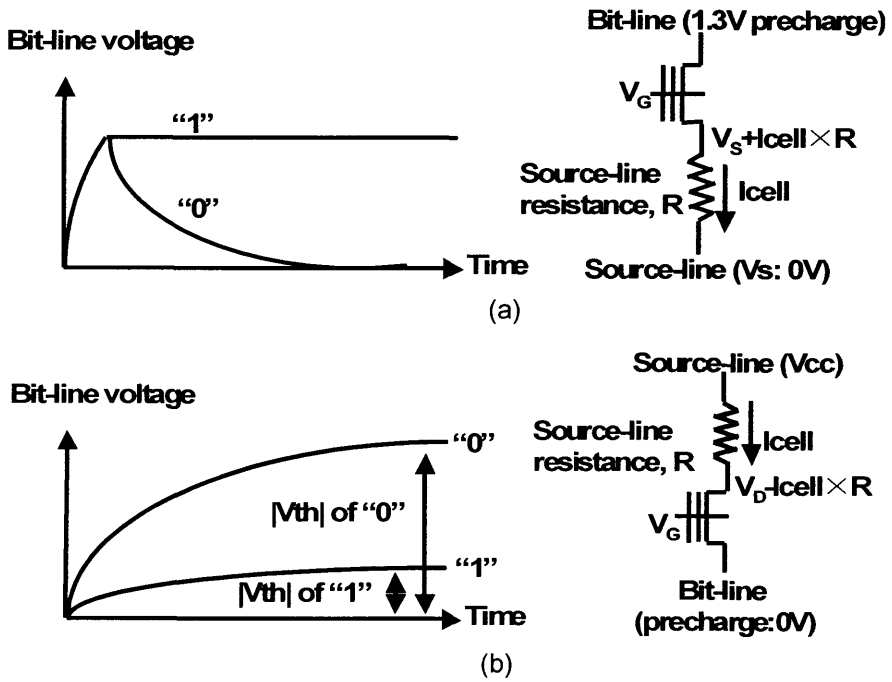


Fig.5.12 Comparison of the conventional (a) and the proposed (b) sensing methods.

5.4.1 Circuit implementation

The simplified circuit schematic diagram of the proposed page buffer is shown in Fig.5.13. The key components of the page buffer are a PMOS sense transistor and a latch circuit that temporarily stores the data to be read out from or programmed into a memory cell. Two bit-lines share one page buffer and are alternately selected during read and program operations. Bias conditions for read, program and erase operations are shown in Table 5.3.

A. Read operation

In a conventional read operation, after the selected bit-line is precharged to Vcc, a cell

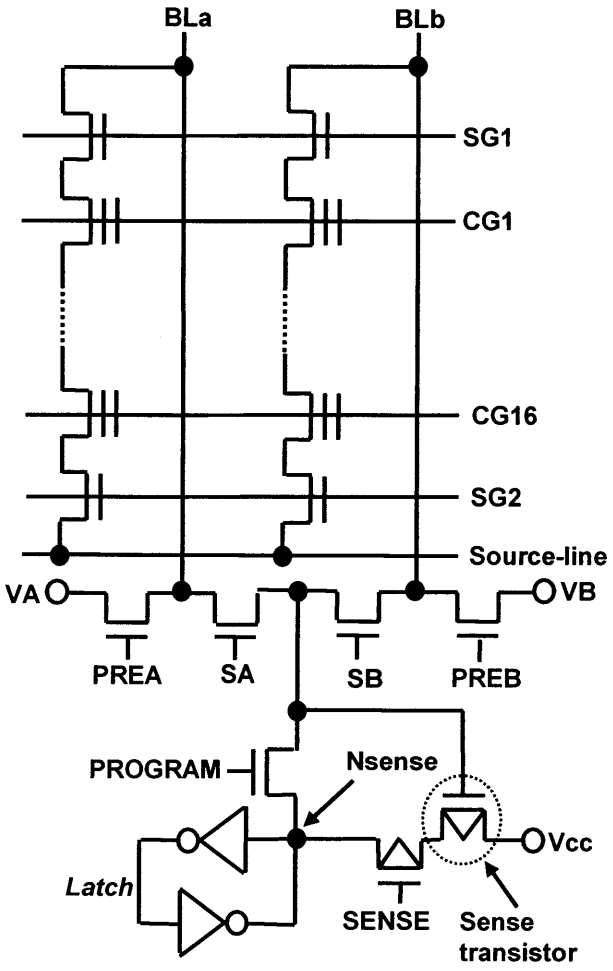


Fig.5.13 A simplified schematic diagram of the proposed PMOS drive page buffer.

read current flows from the bit-line to the grounded source-line. Conversely, in the proposed scheme, a source-line bias method is used. The timing chart for the proposed read operation is shown in Fig.5.14(a). After the selected bit-line, BLa is precharged to 0V, the source-line is applied to Vcc. The selected word-line, CG1 is 0V and the unselected word-lines, CG2...16 are 2V. In this bias condition, the cell read current flows from the source-line to the bit-line. As a result, the bit-line voltage becomes the absolute value of Vth. In case of "0"-read, the bit-line becomes a high-level and that of "1"-bit-line is a low-level. In this way, the data stored in a memory cell is successfully read out to the bit-line. After the sense node, Nsense in Fig.5.13 is reset to 0V, the SENSE signal is activated and the bit-line voltage is sensed by the PMOS sense transistor.

As discussed in Section 5.2, to eliminate the inter bit-line capacitive coupling noise, a shielded bit-line sensing method has been proposed [17], where neighboring bit-lines are alternately selected, and unselected bit-lines are kept grounded. However, if used together with the source-line bias method, the cell current continuously flows throughout the read operation from the source-line (Vcc) to the unselected bit-lines (0V). As the number of unselected bit-lines is 4000, the total current increase is as much as 100mA.

To overcome this problem, a Vcc-bit-line shield sensing method is developed, where unselected bit-lines are connected to Vcc during a read operation. In this case, after the unselected bit-lines are charged to Vcc, no current flows through the unselected bit-lines. Moreover, Vcc-biased unselected bit-lines form a shield between the neighboring selected bit-lines. Therefore, both the inter-bit-line capacitive coupling noise and a large current consumption can be successfully eliminated. In this research, the read access time is assumed to be the same as that of the conventional cell.

B. Program operation

	BLa	*BLb*	*CG1*	*CG2..16*	*SG1*	*SG2*	*Source-line*	*P-well*
Read	0V-precharge	Vcc	0	2	4.5	4.5	Vcc	0
Program	Vcc/0	Vcc	18	10	Vcc	0	Vcc	0
Program verify read	0V-precharge	Vcc	0.3	2	4.5	4.5	Vcc	0
Erase	open	open	0	0	21	21	open	21
Erase verify read	0V-precharge	Vcc	0	0	4.5	4.5	Vcc	0

Table 5.3 Operation conditions

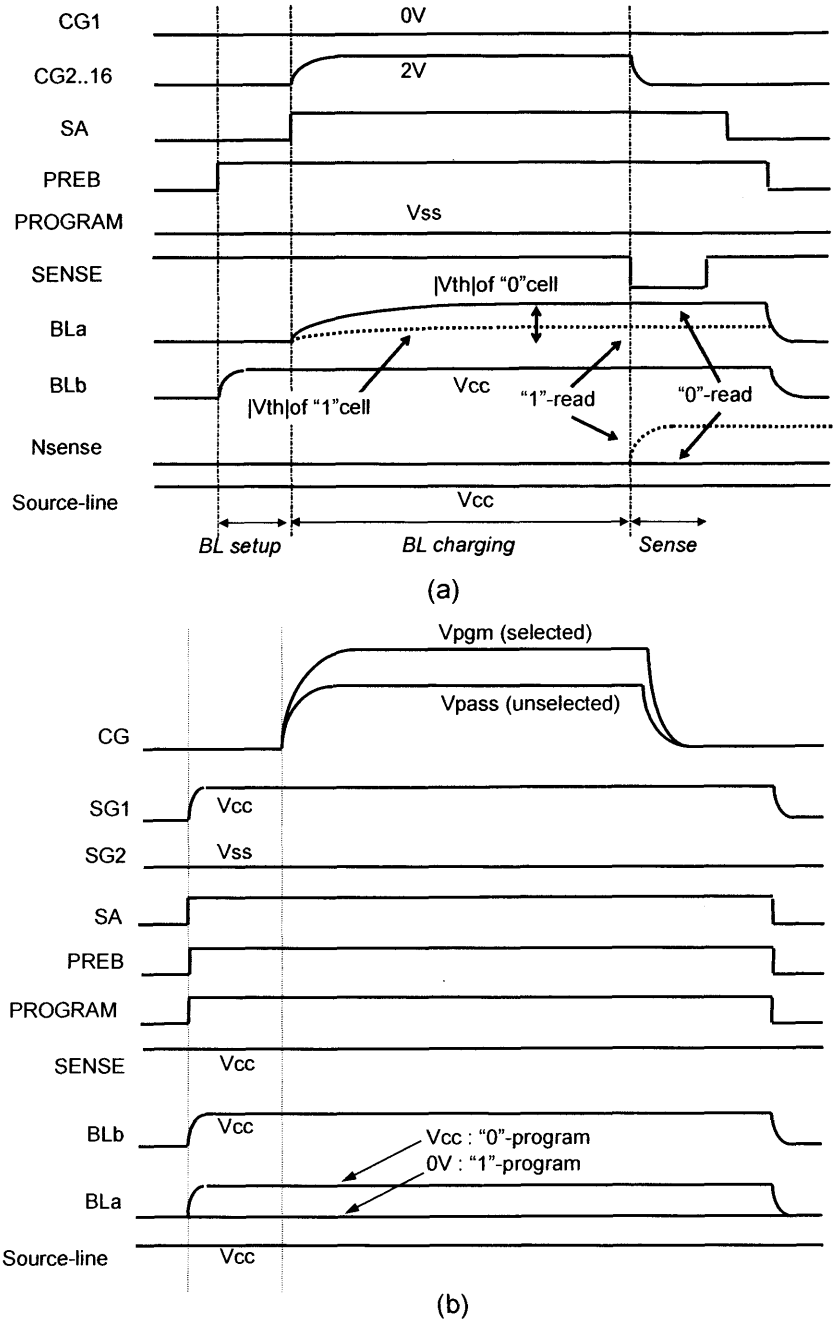


Fig.5.14 Signal timing diagram. (a) Read operation. (b) Program operation.

By using the new page buffer, a bit-by-bit program verify successfully operates and a narrow Vth distribution is realized. The program data is latched in the page buffer. Fig.5.15 shows the program data stored at the latch node, Nsense in Fig.5.13. Fig.5.14(b) shows the timing diagram of the proposed program operation. During a programming, the bit-line voltage is changed according to the program data by activating the PROGRAM

signal in Fig.5.13. As a result, the "0"-program bit-line is grounded and the program inhibit bit-line is biased to Vcc. In the case in which the program data is "0", electrons inject from the channel to the floating gate and the Vth increases. If the program data is "1", the select gate transistor connected to SG1 is turned off because SG1 is set to Vcc. As a result, the whole channel of the selected memory cell is coupled to word-line signals, and the memory cell remains in the erased state [20]. The program time is the same as that of the conventional cell because the voltage difference between the programmed Vth and the thermal equilibrium Vth in the proposed cell is the same as the conventional one.

The program verify read operation is the same as the read operation except that selected CG1 is 0.3V and the reset of Nsense is not performed. The re-program data is modified, such that the programming is executed only on memory cells that have not been successfully programmed as shown in Fig.5.15.

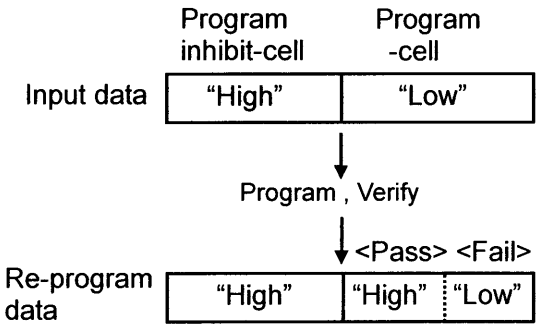


Fig.5.15 Program and re-program data stored at the page buffer node, Nsense during a programming and a program verify read.

5.4.2 Experimental results

The simplified models of the noise in the proposed scheme are shown in Fig.5.16. Fig.5.16(a) describes the first program verify read of the proposed cell. At the first program verify read operation, Cell B is successfully programmed. The other memory cells are still in erased state and a large cell read current flows through the other memory cells just like in Fig.5.16(a). As a result, the source-line drops from Vcc due to the source-line resistance. The last verify read operation is shown in Fig.5.16(b). At the last program verify read operation, the other memory cells are also successfully programmed. In this case, the source-line drop is smaller than that of the first verify read. In this way, the source-line drop changes as the neighboring cells are programmed. However, even if the source-line drops, what is decreased is the gate-drain voltage, Vgd of the memory cell, not the gate-source voltage, Vgs. Therefore, the cell read current does not change throughout the verify read operation.

The proposed sensing method is verified with a 0.25um 256Mbit NAND flash memory. The microphotograph of the chip is shown in Fig.5.17. The experimental data are shown in Fig.5.18. In the proposed scheme, the cell read current does not change with the source-line noise, whereas in the conventional scheme the cell read current drastically changes because of the source-line noise.

The characteristics of the proposed cell array are summarized in Table 5.4. The threshold voltage shift in the negative direction, ΔVth(NEG), is eliminated because the source-line drop does not affect the cell read current. The threshold voltage shift in the positive direction, ΔVth(POS), is significantly reduced. The threshold voltage fluctuation which is the sum of the threshold voltage shift in the negative and positive direction is decreased from 0.3V (conventional array) to 0.1V. The program voltage increment can be increased from 0.35V (conventional array) to 0.55V. Therefore, the program speed of the proposed scheme improves by 57% compared with the conventional scheme.

5.4.3 Erase verify operation

The proposed scheme is used in the erase verify operation following the erase operation in 0.25um 256Mbit [8], 0.16um 1Gbit [26], 0.13um 2Gbit [27], 90nm 4Gbit [28] and 70nm 8Gbit [29] products.

In the erase verify operation, a negative Vth should be read out. One possible solution is a negative voltage bias to the control gate. But this method is not preferred from the viewpoint of manufacturing costs. In a conventional NAND flash memory, NMOS connecting to the control gate is fabricated directly on the p-substrate as shown in Fig.5.19. If the negative voltage bias method is used, the NMOS must be fabricated on a double-well structure shown in Fig.5.19 and this increases the manufacturing costs. Therefore, a new

sensing method is required.

On the other hand, in the proposed sensing method, the negative Vth can be read out without negative world line bias. Consequently, a low process cost and a small circuit area are realized.

The erase and the erase verify operations are performed in the following ways. The erase operation is performed in a NAND-block unit. All memory cells that are connected in series or share the same control gates are selected at once. Therefore, 16k memory cells are erased simultaneously. The selected control gates are set to 0V and an erase voltage about 21V is applied to the P-well of the cell array. As a result, electrons are ejected from the floating gate to the channel and the Vth decreases. After the erase operation, the erase verify read operation is performed. Sixteen series connected memory cells are verified at the same time. The erase verify read operation is the same as the read operation except that all control gates from CG1 to CG16 are grounded. Only when all sixteen memory cells connected in series are successfully erased, the bit-line becomes a high level. Otherwise, the bit-line becomes a low level. The erase and the erase verify read operations are repeated until all selected memory cells are successfully erased.

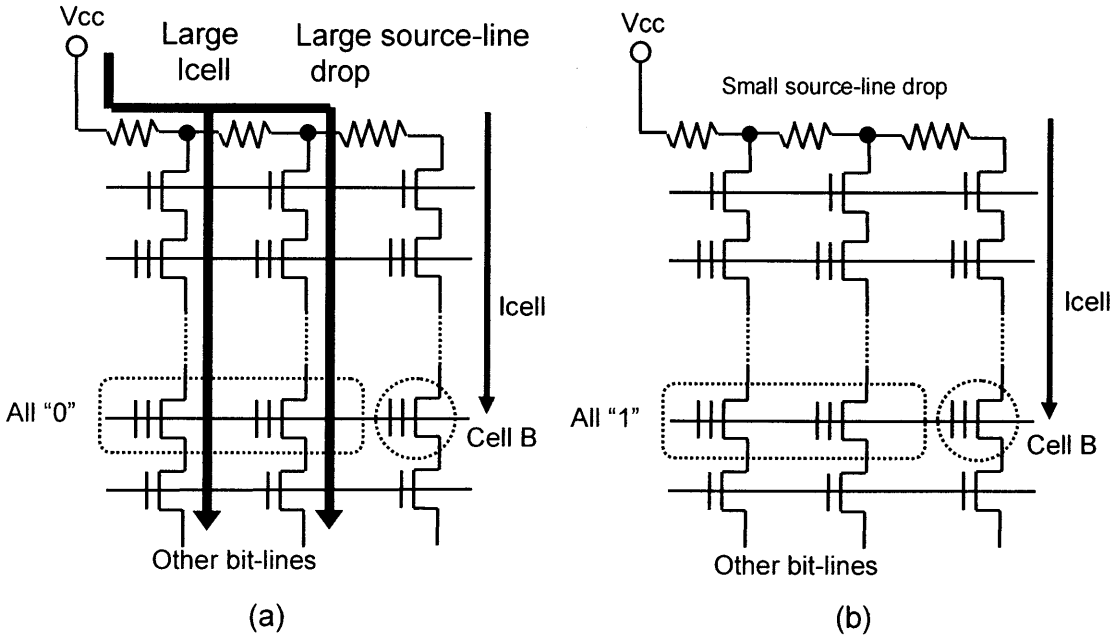


Fig.5.16 A model for the negative threshold voltage shift of the proposed cell due to source-line noise.

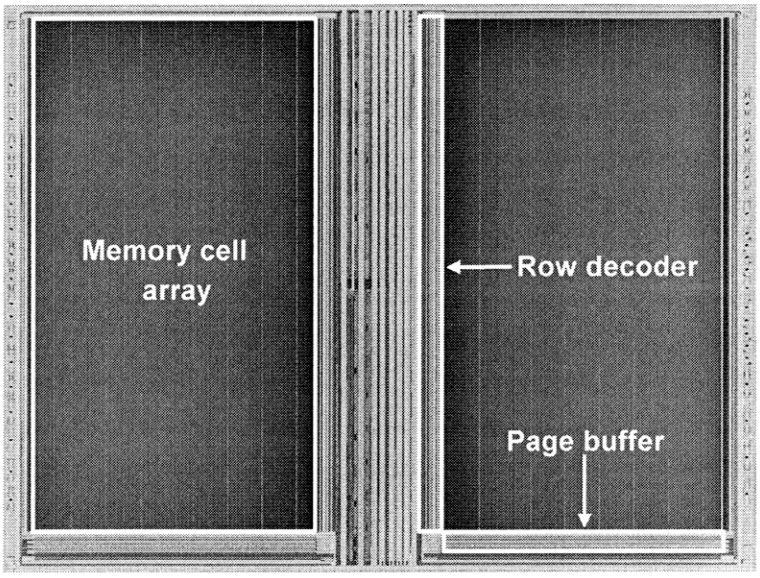


Fig.5.17 A micrograph of the proposed 256Mbit NAND flash memory chip.

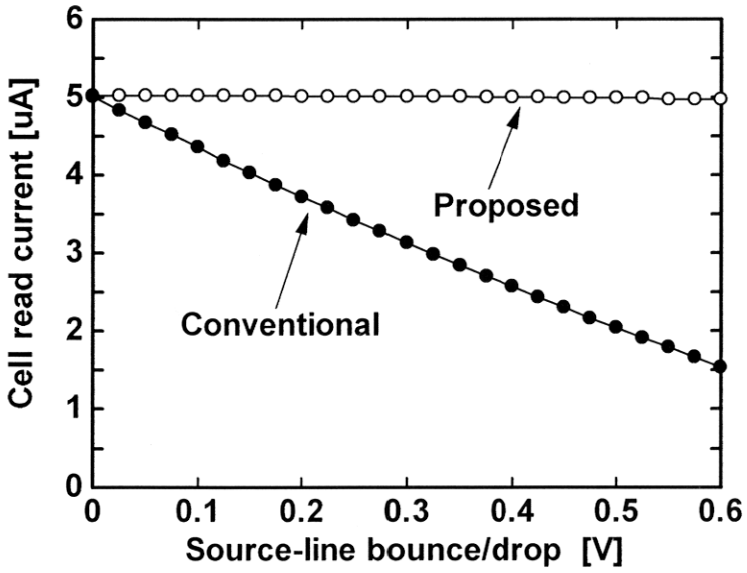


Fig.5.18 Measured cell read current change due to the source-line drop in the proposed cell and the source-line bounce in the conventional cell.

	Total Vth shift due to the circuit noise	⊿Vpgm	Program speed
Conventional	**0.3V**	**0.35V**	-
Proposed	**0.1V**	**0.55V**	**57% faster**

Table 5.4 Comparison of the proposed Vcc bit-line shield sensing scheme and the conventional array.

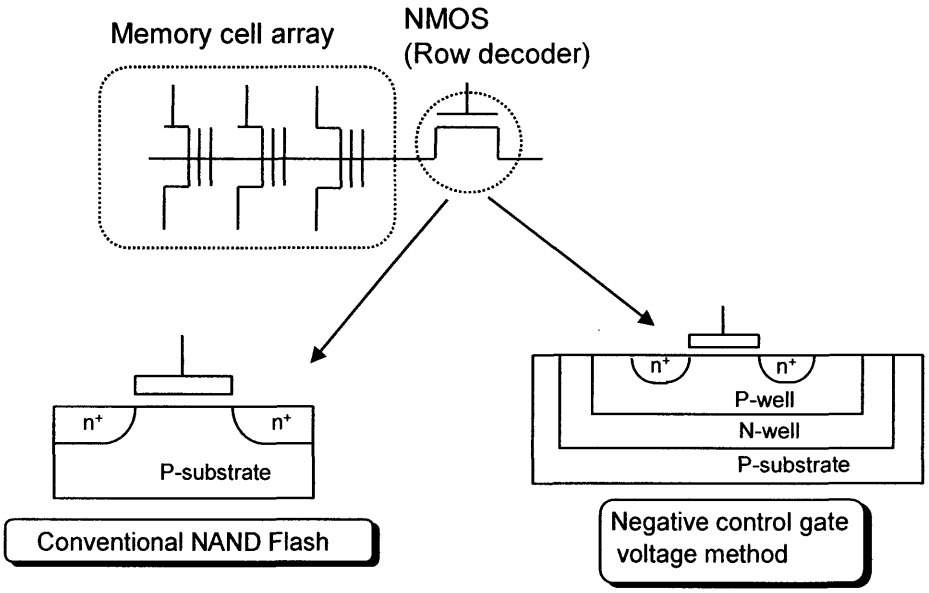


Fig.5.19 Structure of a peripheral NMOS transistor in a conventional NAND flash memory and that with a negative control gate voltage method.

5.5 Summary

The effect of the array noise such as an inter bit-line capacitive coupling noise and the source-line noise on the performance are analyzed. Moreover, two low noise technologies are proposed. First, a double-level Vth select gate array architecture is proposed for the 3V multi-level cell. The circuit noise is eliminated and as a result, the program speed is improved by 77% with this new architecture. This architecture also minimizes the chip area and therefore is best suitable for the 3V multi-level cell. The proposed cell array is verified with 0.7um NAND flash memory. Second, the Vcc bit-line shield sensing method is proposed for the low-voltage multi-level cell. Again, the circuit noise is suppressed and the program speed is improved by 57%. The new sensing method is verified with 0.25um 256Mbit NAND flash memory [8]. This technology is used in the erase verify operation in 0.25um 256Mbit [8], 0.16um 1Gbit [26], 0.13um 2Gbit [27], 90nm 4Gbit [28] and 70nm 8Gbit [29] products.

Fig.5.20 shows the program speed trend of the low-voltage multi-level cell. The program speed is 60-70% improved. Because of the low noise technology, fast programming 10MB/sec 3V multi-level cell or 5MB/sec low-voltage multi-level cell can be realized and therefore the speed target of the 3V multi-level cell and the low voltage multi-level cell described in Chapter 1 are fulfilled.

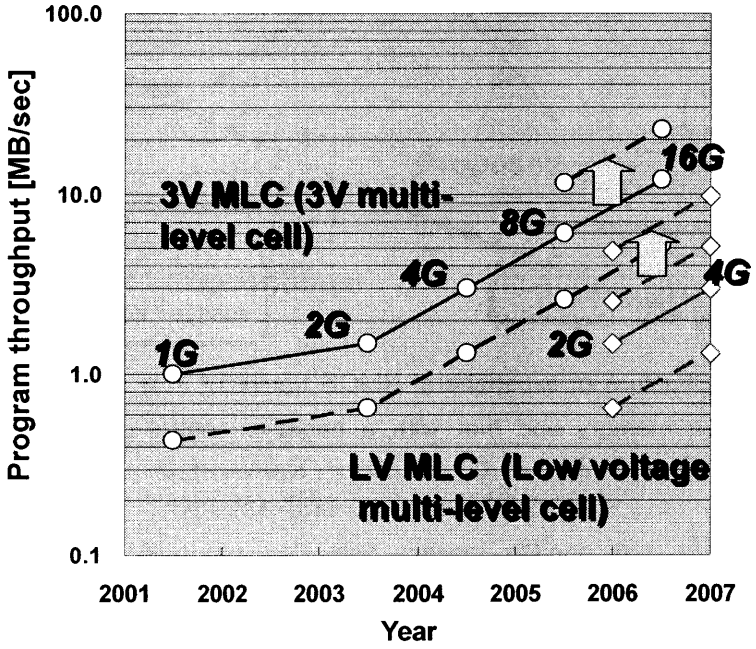


Fig.5.20 Program speed improvement with the low noise technology
(Circle : 3V MLC, Lozenge : LV MLC)

References

[1] K.Takeuchi, T.Tanaka and H.Nakamura, "A double-level-Vth select gate array architecture for multi-level NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1995, pp.69-70.

[2] K.Takeuchi, T.Tanaka and H.Nakamura, "A double-level-Vth select gate array architecture for multi-level NAND flash memories", *IEEE Journal of Solid-State Circuits*, vol.31, no.4, April 1996, pp.602-609.

[3] K. Takeuchi, S. Satoh, T. Tanaka, K. Imamiya, and K. Sakui, " A negative Vth cell architecture for highly scalable, excellently noise immune and highly reliable NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1998, pp.234-235.

[4] K. Takeuchi, S. Satoh, T. Tanaka, K. Imamiya, and K. Sakui, " A negative Vth cell architecture for highly scalable, excellently noise immune and highly reliable NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.34, no.5, May 1999, pp.675-684.

[5] F. Masuoka, M. Momodomi, Y. Iwata and R. Shirota, "New ultra high density EPROM and flash EEPROM with NAND structured cell," in *IEDM Tech. Dig.,* 1987, pp.552-555.

[6] K. Imamiya, Y. Iwata, Y. Sugiura, H. Nakamura, H. Oodaira, M. Momodomi, Y. Ito, T. Watanabe, H. Araki, K. Narita, K. Masuda and J. Miyamoto, "A 35 ns-cycle-time 3.3 V-only 32 Mb NAND flash EEPROM", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.32-33.

[7] Kang-Deog Suh, Byung-Hoon Suh, Young-Ho Um, Jin-Ki Kim, Young-Joon Choi, Yong-Nam Koh, Sung-Soo Lee, Suk-Chon Kwon, Byung-Soon Choi, Jin-Sun Yum, Jung-Hyuk Choi, Jang-Rae Kim and Hyung-Kyu Lim, "A 3.3 V 32 Mb NAND flash memory with incremental step pulse programming scheme", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.128-129.

[8] Tae-Sung Jung, Young-Joon Choi, Kang-Deog Suh, Byung-Hoon Suh, Jin-Ki Kim, Young-Ho Lim, Yong-Nam Koh, Jong-Wook Park, Ki-Jong Lee, Jung-Hoon Park, Kee-Tae Park, Jang-Rae Kim, Jeong-Hyong Lee and Hyung-Kyu Lim, "A 3.3 V 128 Mb multi-level NAND flash memory for mass storage application", in *ISSCC Digest of Technical Papers*, Feb., 1996, pp.32-33.

[9] J.K. Kim, K. Sakui, S.S. Lee, J. Itoh, S.C. Kwon, K. Kanazawa, J.J. Lee, H. Nakamura, K.Y. Kim, T. Himeno, J.R. Kim, K. Kanda, T.S. Jung, Y. Oshima, K.D. Suh, K. Hashimoto, S.T. Ahn, and J. Miyamoto, "A 120 mm^2 64 Mb NAND flash memory achieving 180 ns/byte effective program speed," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1996, pp.168-169.

[10] T.Tanaka, M.Momodomi, Y.Iwata, Y.Tanaka, H.Oodaira, Y.Itoh, R.Shirota, K.Ohuchi and F.Masuoka, "A 4-Mbit NAND-EEPROM with Tight Programmed Vt Distribution," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1990, pp.105-106.

[11] T.Tanaka, Y.Tanaka, H.Nakamura, H.Oodaira, S.Aritome, R.Shirota and F.Masuoka, "A

quick intelligent program Architecture for 3V-only NAND-EEPROMs," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1992, pp.20-21.

[12] T. Takeshima, H. Sugawara, H. Takada, Y. Hisamune, K. Kanamori, T. Okazawa, T. Murotani and I. Sasaki, "A 3.3 V single-power-supply 64 Mb flash memory with dynamic bit-line latch (DBL) programming scheme", in *ISSCC Digest of Technical Papers*, Feb., 1994, pp.148-149.

[13] M. Ohkawa, H.; Sugawara, N. Sudo, M. Tsukiji, K. Nakagawa, M. Kawata, K. Oyama, T. Takeshima and S. Ohya, "A 98 mm^2 3.3 V 64 Mb flash memory with FN-NOR type 4-level cell", in *ISSCC Digest of Technical Papers*, Feb., 1996, pp.376-379.

[14] A. Baker, R. Alexis, S. Bell, V. Dalvi, R. Durante, E. Baer, M. Fandrich, O. Jungroth, J. Kreifels, M. Landgraf, K. Lee, H. Pon, M. Rashid, R. Rozman, J. Tsang, K. Underwood, C. Yarlagadda, "A 3.3 V 16 Mb flash memory with advanced write automation", in *ISSCC Digest of Technical Papers*, Feb., 1994, pp.146-147.

[15] T. Jinbo, H. Nakata, K. Hashimoto, T. Watanabe, K. Ninomiya, T. Urai, M. Koike, T. Sato, N. Kodama, K. Oyamaand T. Okazawa, "A 5 V-only 16 Mb flash memory with sector-erase mode", in *ISSCC Digest of Technical Papers*, Feb., 1992, pp.154-155.

[16] K. Seki, H. Kume, Y. Ohji, T. Tanaka, T. Adachi, M. Ushiyama, K. Shimohigashi, T. Wada, K. Komori, T. Nishimoto, K. Izawa, T. Hagiwara, Y. Kubota, K. Shohji, N. Miyamoto, S. Saeki and N. Ogawa, "An 80 ns 1 Mb flash memory with on-chip erase/erase-verify controller", in *ISSCC Digest of Technical Papers*, Feb., 1990, pp.60-61.

[17] T.Tanaka, Y.Tanaka, H.Nakamura, K.Sakui, H.Oodaira, R.Shirota K.Ohuchi F.Masuoka and H.Hara, "A Quick Intelligent Programming Architecture and a Shielded Bit-line Sensing Method for 3V-only NAND Flash Memory," *IEEE J.Solid-State Circuits*, vol.29, November 1994, pp.1366-1373.

[18] R. Kirisawa, S. Aritome, R. Nakayama, T. Endoh, R. Shirota and F. Masuoka, "A NAND structured cell with a new programming technology for highly reliable 5 V-only flash EEPROM," in *Symp. VLSI Technology Dig. Tech. Papers*, June 1990, pp.129-130.

[19] G.J.Hemink, T.Tanaka, T.Endoh, S.Aritome and R.Shirota, "Fast and Accurate Programming Method for Multi-level NAND Flash EEPROMs," *Symp. VLSI Technology Dig. Tech. Papers*, June 1995, pp.129-130.

[20] K. D. Suh, B. H. Suh, Y. H. Lim, J. K. Kim, Y. J. Choi, Y. N. Koh, S. S. Lee, S. C. Kwon, B. S. Choi, J. S. Yum, J. H. Choi, J. R. Kim, and H. K. Lim, "A 3.3V 32Mb NAND flash memory with incremental step pulse programming scheme," in *ISSCC Digest of Technical Papers*, Feb. 1995, pp.128-129.

[21] A.Baker, R.Alexis, S.Bell, V.Dalvi, R.Durante, E.Baer, M.Fandrich, O.Jungroth, J.Kreifels, M.Landgraf, K.Lee, H.Pon, M.Rashid, R.Rozman, J.Tsang, K.Underwood, C.Yarlagadda, "A 3.3V 16Mb Flash Memory with Advanced Write Automation", *ISSCC Dig. of Tech. Papers*, February 1994, pp.146-147.

[22] S.Aritome, S.Satoh, T.Maruyama, H.Watanabe, S.Shuto, G.J.Hemink, R.Shirota, S.Watanabe and F.Masuoka, "A 0.67μm2 Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) for 3V-only 256Mbit NAND EEPROMs," *IEDM Tech. Dig.*, December 1994, pp.61-64.

[23] S. Satoh, T. Nakamura, K. Shimizu, K. Takeuchi, H. Iizuka, S. Aritome, and R. Shirota, "A novel gate-offset NAND cell (GOC-NAND) technology suitable for high-density and low-voltage-operation flash memories", in *IEDM Tech. Dig.*, 1999, pp.271-274.

[24] D.S. Byeon, S.S.Lee, Y.H.Lim, J.S.Park, W.K.Han, P.S.Kwak, D.H.Kim, D.H.Chae, S.H.Moon, S.J.Lee, H.C.Cho, J.W.Lee, M.S.Kim, J.S.Yang, Y.W.Park, D.W.Bae, J.D.Choi, S.H.Hur and K.D.Suh, "An 8Gb multi-level NAND flash memory with 63nm STI CMOS process technology", in *ISSCC Digest of Technical Papers*, 2005, pp.46-47.

[25] T.Hara, K.Fukuda, K.Kanazawa, N.Shibata, K.Hosono, H.Maejima, M.Nakagawa, T.Abe, M.Kojima, M.Fujiu, Y.Takeuchi, K.Amemiya, M.Morooka, T.Kamai, H.Nasu, K.Kawano, C.M.Wang, K.Sakurai, N.Tokiwa, H.Waki, T.Maruyama, S.Yoshikawa, M.Higashitani, T.D.Pham and T.Watanabe, "A 146mm^2 8Gb NAND flash memory with 70nm COMS technology", in *ISSCC Digest of Technical Papers*, 2005, pp.44-45.

[26] S.Aritome, "Advanced flash memory technology and trends for file storage application", in *IEDM Tech. Dig.*, 2000, pp.763-766.

[27] H.Nakamura, K.Imamiya, T.Himeno, T.Yamamura, T.Ikehashi, K.Takeuchi, K.Kanda, K.Hosono, T.Futatsuyama, K.Kawai, R.Shirota, N.Arai, Fumitaka Arai, K.Hatakeyama, H.Hazama, Masanobu Saito, H.Meguro, K.Conley, K. Quader and J.Chen, "A 125mm^2 1Gb NAND Flash Memory with 10MB/s Program Throughput," *ISSCC Digest of Technical Papers*, 2002, pp.106-107.

[28] K. Kobayashi, "Toshiba's NAND flash strategy", in *CEATEC 2004 Dig. Tech. Papers*, Oct. 2004.

[29] T.Hara, K.Fukuda, K.Kanazawa, N.Shibata, K.Hosono, H.Maejima, M.Nakagawa, T.Abe, M.Kojima, M.Fujiu, Y.Takeuchi, K.Amemiya, M.Morooka, T.Kamai, H.Nasu, K.Kawano, C.M.Wang, K.Sakurai, N.Tokiwa, H.Waki, T.Maruyama, S.Yoshikawa, M.Higashitani, T.D.Pham and T.Watanabe, "A 146mm^2 8Gb NAND flash memory with 70nm COMS technology", in *ISSCC Digest of Technical Papers*, 2005, pp.44-45.

CHAPTER 6
PARALLEL WRITE TECHNOLOGY
Acceleration by increasing the page size

6.1 Introduction

To increase the program throughput of the 3V single-level cell, the most effective method is to increase the page size, i.e., the number of memory cells programmed simultaneously [1-4]. Yet, in a conventional NAND flash memory, one page buffer storing the program data is needed to program one memory cell. If the page size is doubled to increase the program speed, the number of page buffers is also doubled [5], [6]. However, this increases the chip size by 10%.

To overcome this problem, a new architecture, "a dual-page programming scheme" [5], [6], is introduced. In this scheme, two memory cells are programmed at the same time using only one page buffer. As a result, the page size is doubled without increasing the number of page buffers and a very fast program operation can be realized. This unique operation is made possible by using a bit-line as a dynamic latch to temporarily store the program data. When a program pulse is applied to one memory cell, the memory cell is disconnected from the page buffer and its programming data is stored on the dynamic latch of the bit-line. Meanwhile, the other memory cell is verified using the page buffer. In this way, two memory cells are programmed at the same time. Due to this technology, the programming is accelerated by 73% in a 1-Gbit generation and 62% in a 4-Gbit generation. 18.2-Mbyte/sec 1-Gbit or 30.7-Mbyte/sec 4-Gbit NAND flash memory can be realized with this new architecture.

In Section 6.2, the concept of the dual page programming scheme is described. Also, the reason why the bit-line can be used as a dynamic latch during a programming is explained. Next, in Section 6.3, the new NAND flash protocol using the proposed scheme is presented. Circuit implementations to realize the proposed program operation are shown in Section 6.4. In Section 6.5, the experimental results regarding the performance of the proposed scheme are presented. Circuit considerations such as the charge leakage issue, the noise issue and the power consumption are discussed in Section 6.6. The summary is given in Section 6.7.

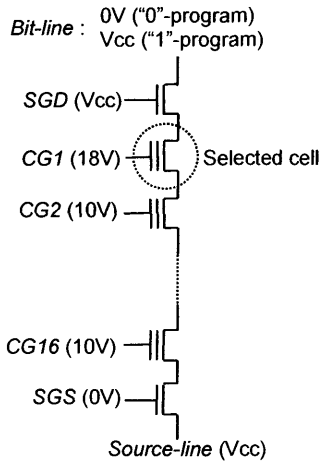


Fig. 6.1 Program operation of a NAND-type cell

6.2 Dual page programming scheme

A. Concept

In this section, the concept of the new programming scheme is introduced. Fig.6.1 shows a program operation of a NAND flash memory. During a programming, the selected control gate is Vpgm, for example 18V. The unselected control gates are Vpass that is about 10V. In the case of the "0"-program, the selected bit-line is set to 0V and the channel of the selected memory cell is grounded. As a result, electrons are injected from the channel to the floating gate [7-9]. On the other hand, the program inhibit bit-line is applied to Vcc [10]. Vcc is typically 3.3V in a NAND flash system. In this case, the select gate transistor connected to the bit-line is turned off, because the select gate, SGD is biased to Vcc. As a result, the whole channel of the program inhibit memory cells is raised by the capacitive coupling with control gates. The electron injection is prohibited and the unselected memory cells remain in the erased state.

In a conventional scheme, one page buffer is needed to program one memory cell. If the page buffers are doubled to increase the program speed, the chip area increases by 10%. On the contrary, in the proposed scheme, two memory cells, CellA and CellB in Fig.6.2, are programmed at the same time using only one page buffer. Therefore, twice as many memory cells are programmed simultaneously. Off course, the program data of CellA are different from those of CellB. However, there is only one page buffer. Thus, the most important issue is whether the two bit of program data can be stored in a chip with one page buffer.

Fig.6.3 explains how the two bits of data are stored. The left hand Fig.6.3 shows a program algorithm. At first, the program data are input to the device. Then, a program pulse and a verify read are repeated until all memory cells are programmed. In the conventional scheme, the program data are stored in a page buffer throughout these operations. On the other hand, in the proposed scheme, the two bit program data are stored both in a page buffer and in a bit-line. That is, a bit-line is used as a dynamic latch storing the program data. Using a bit-line as a dynamic latch has already been proposed [11]. However, in the reference [11], the page buffer stores the program data during both the programming and the verify read. Moreover, the same number of page buffers as the page size are required.

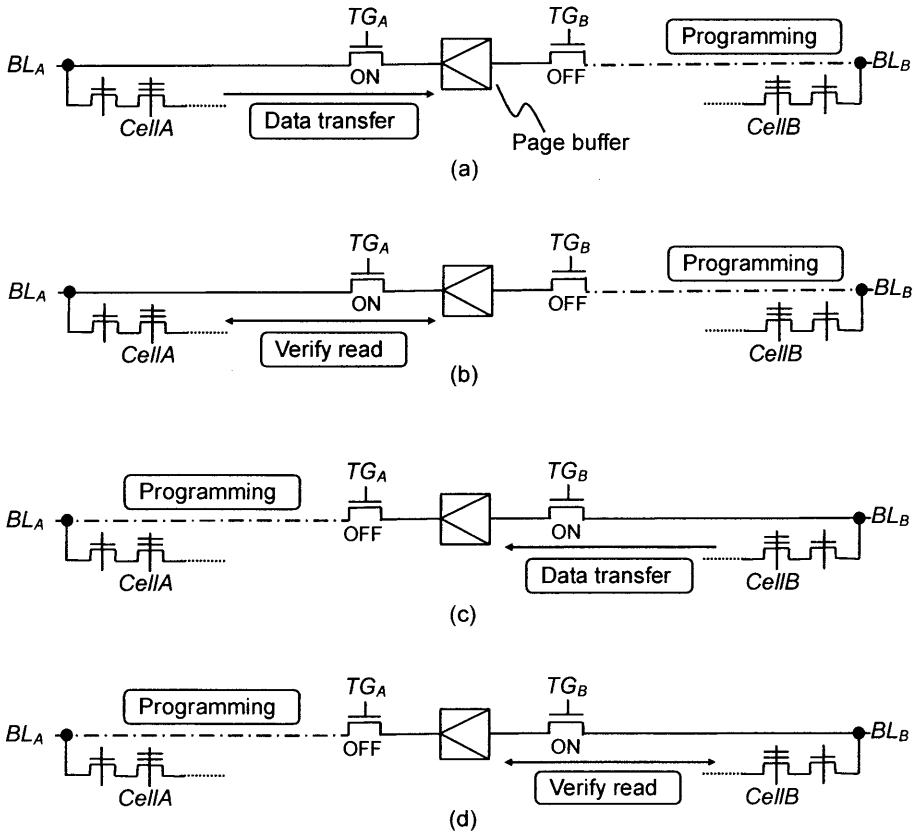


Fig. 6.2 Key operations of the proposed scheme.

(a) Program data of CellA are transferred from BLA to the page buffer. A program pulse is applied to CellB.

(b) CellA is verified using a page buffer. A program pulse is applied to CellB.

(c) Program data of CellB are transferred from BLB to the page buffer. A program pulse is applied to CellA.

(d) CellB is verified using a page buffer. A program pulse is applied to CellA.

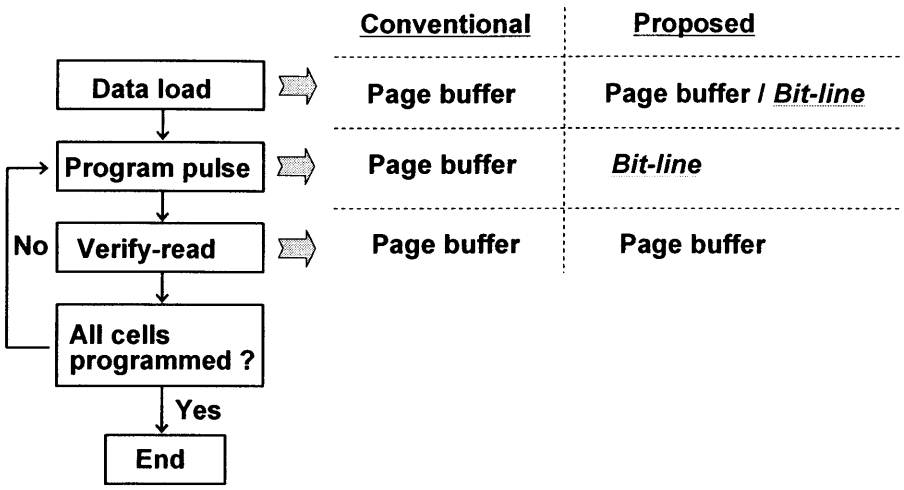


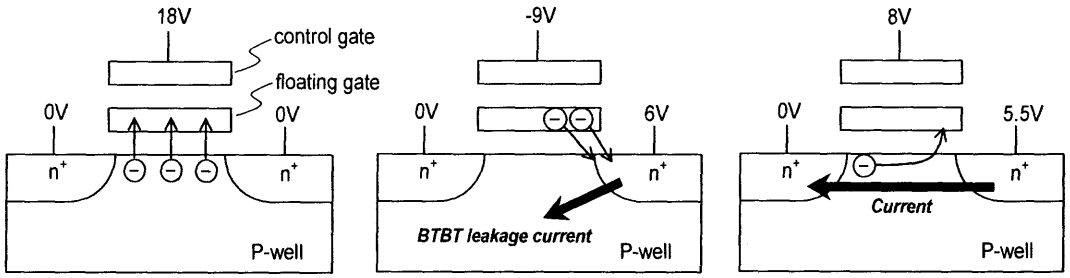
Fig. 6.3 Circuits storing the program data. In the conventional scheme, a page buffer stores the program data throughout the program operation. In the proposed scheme, a bit-line is used as a dynamic latch storing the program data.

As shown in Fig.6.3, during the data loading, one of the two bit data is stored in a page buffer and the other is stored on a bit-line. When a program pulse is applied, the program data are stored on a bit-line. However, in the case of the verify read, one page buffer is needed to verify one memory cell. Yet, there is only one page buffer.

The key operation to solve this problem is that one memory cell is verified at the different timing from the other memory cell. That is, one memory cell is verified when the other memory cell is programmed. In Fig.6.2(a) and (b), the program pulse is applied to CellB. BLB is disconnected from the page buffer and is in the floating state. The program data of CellB are stored on BLB. The page buffer is connected to BLA and is used to verify CellA. First, the program data of CellA stored on BLA are transferred to the page buffer by sensing the bit-line voltage, as shown in Fig.6.2(a). Then, the verify read of CellA is performed, as shown in Fig.6.2(b). On the other hand, when CellA is programmed, BLA is disconnected from the page buffer and the program data of CellA are stored on BLA, as shown in Fig.6.2(c) and (d). BLB is connected to the page buffer. As shown in Fig.6.2(c), the program data of CellB stored on BLB are transferred to the page buffer by sensing the bit-line voltage. Then, CellB is verified, as shown in Fig.6.2(d). In this way, if CellA is verified at a different timing from that of CellB, these two memory cells can be programmed simultaneously with only one page buffer. Actually, one memory cell can be verified when the program pulse is applied to the other memory cell.

B. Why bit-line can be used as a dynamic latch

Here, it is explained why the bit-line can be floating during the programming. There are three reasons. First, the charge of the floating bit-line is not discharged to the source-line, because the select transistor connected to the source-line, SGS, is turned off. Second, the channel FN-tunneling program shown in Fig.6.4 (a) is free from the band-to-band tunneling (*BTBT*) leakage [12-15]. Third, the current from the channel to the floating gate is a few pico-amperes and very small. This means the voltage change of the floating bit-line is less than 0.1mV and negligibly small. In contrast with that, in the case of the drain-edge FN tunneling programming [11, 16-22], the BTBT leakage shown in Fig.6.4(b) occurs and the charge stored on the floating bit-line can be discharged. Also, in the case of the hot-electron injection [23-35] programming shown in Fig.6.4(c), the programming current is large and the proposed architecture cannot be used.



(a) (b) (c)

Fig. 6.4 (a) Channel FN-tunneling programming. The programming current is a few pico-amperes and is very small [12-15].
(b) Drain-edge FN tunneling programming [11,16-22]. The band-to-band tunneling (BTBT) leakage occurs.
(c) Hot-electron injection programming [23-35]. Large current flows through the channel.

6.3 New NAND flash protocol

The diagram of the proposed 1-Gbit NAND flash memory is shown in Fig.6.5. There are a total of eight banks and the page size of each bank is 4-kbit. Bank1,2,3,4^{U} compose the upper bank and the lower bank consists of Bank1,2,3,4_{L}. The page buffers are shared by the upper and the lower banks. Therefore, there is a total of 16k page buffers in a chip. 32k memory cells of Page1,2,3,4^{U} and Page1,2,3,4_{L} are programmed simultaneously.

A new access protocol for the proposed architecture is shown in Fig.6.6. At the beginning of the program operation, the device receives the DATA INPUT command. Then, the address and the 16-kbit program data of Page1,2,3,4^{U} are serially loaded to the page buffers, as shown in Fig.6.7(a). Next, the BIT-LINE DATA LOAD command is issued. The Ready/Busy (R/B) signal becomes low and the device goes into the 'Busy' state. The upper bank program data stored in the page buffers are transferred to the bit-lines of the upper bank, as shown in Fig.6.7 (b). During the following data load of the lower bank, the program data of the upper bank are stored on the floating bit-lines. When the data transfer from the page buffers to the bit-lines is completed, the R/B signal becomes high and the device returns to the 'Ready' state. Then, the DATA INPUT command is issued again. The address and the program data of Page1, 2, 3, 4_{L} are loaded to the page buffers. Finally, when the WRITE command is input, the device carries out the program operation.

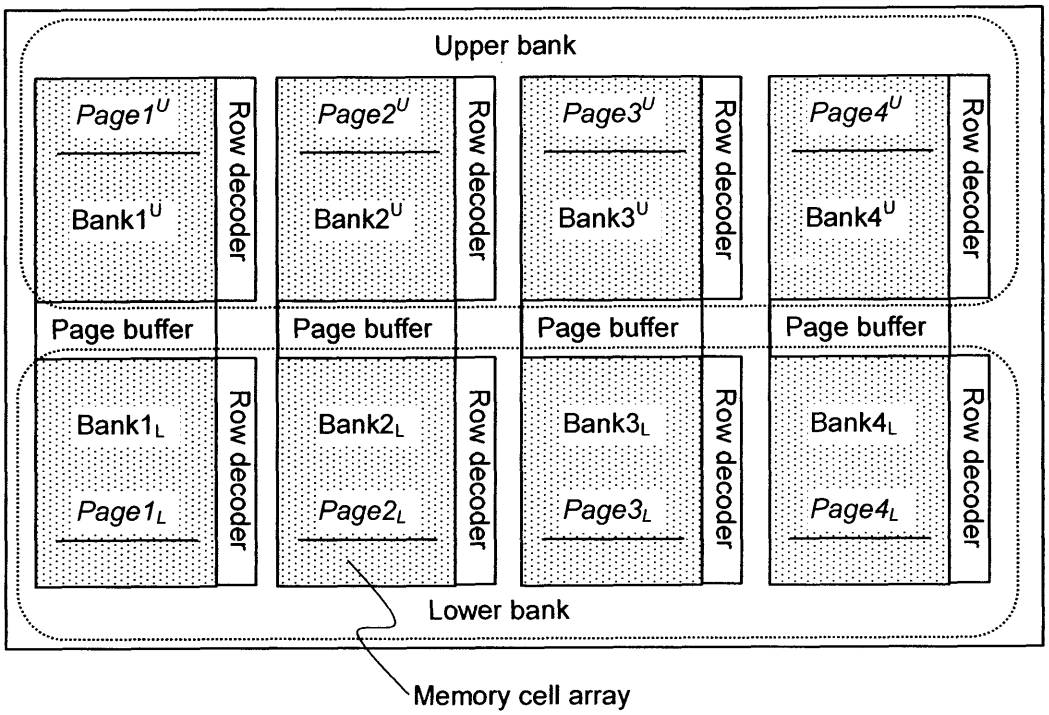


Fig. 6.5 A diagram of the proposed 1-Gbit NAND flash memory. Bank1,2,3,4^{U} compose the upper bank and the lower bank consists of Bank1,2,3,4$_{L}$. The page size of each bank is 4-kbit. The maximum page size is 32-kbit.

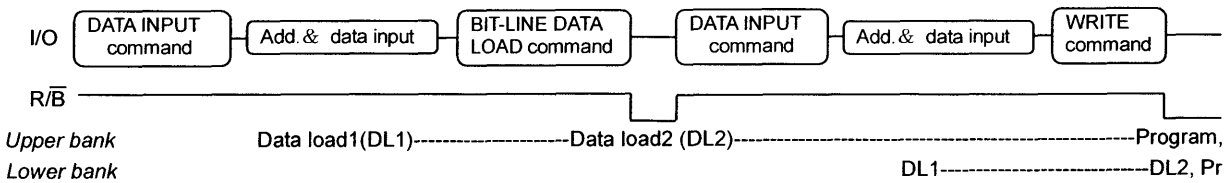


Fig. 6.6 Proposed NAND flash protocol.

Data load1: data load from the flash controller to the page buffer.

Data load2: data transfer from the page buffer to the bit-line.

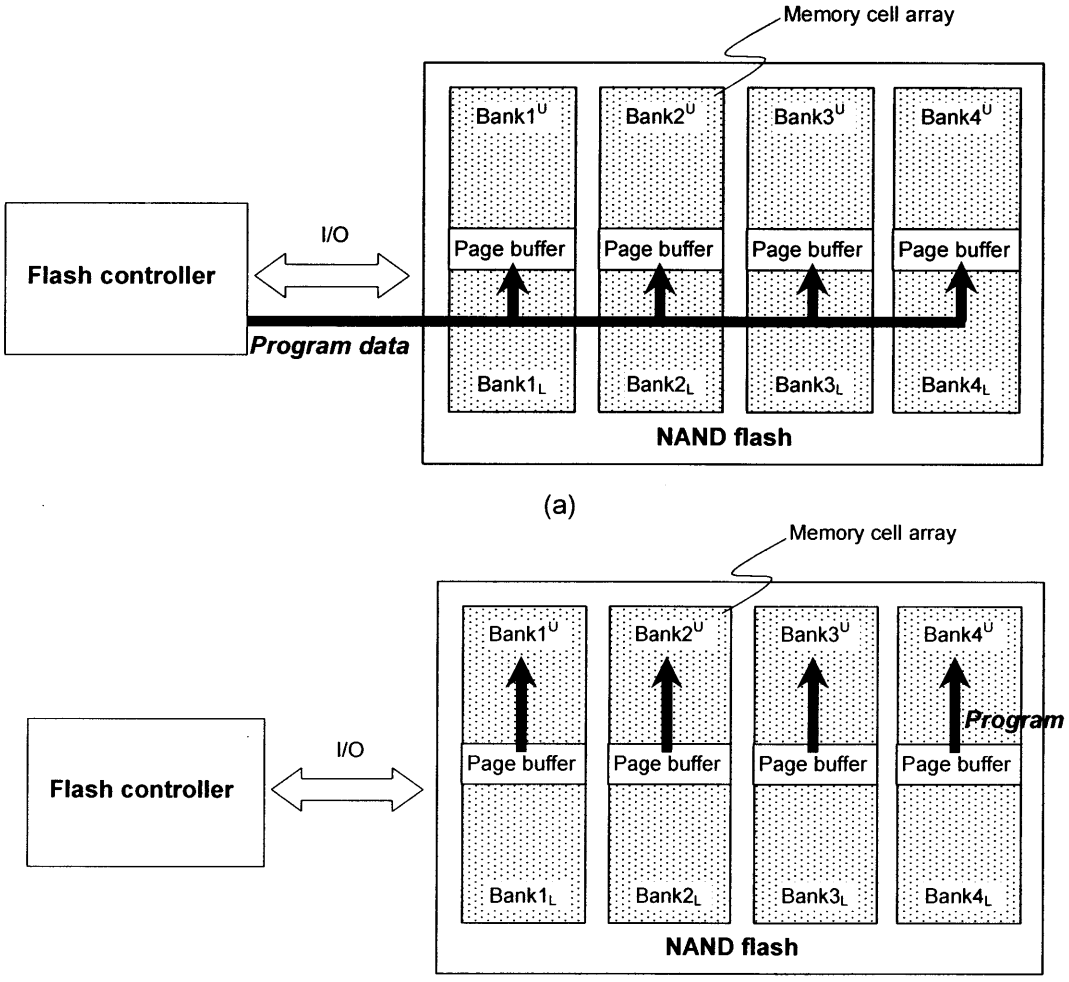


Fig. 6.7

(a) Data load from the flash controller to the page buffer (Data Load1).

(b) Data transfer from the page buffer to the bit-line (Data Load2).

6.4 Circuit implementations

In this section, circuit techniques to realize the proposed program operation are described. The simplified circuit diagram of the page buffer is shown in Fig.6.8. The program data or the data read out from a memory cell are temporarily stored in the page buffer. In order to suppress the inter bit-line capacitive coupling noise, a shielded bit-line method is used [36]. Neighboring two bit-lines share a page buffer and are alternately selected during a program and a read operations. In Fig.6.8, CellA and CellB are selected. Unselected BLC and BLD are biased to Vcc or Vss via VSC and VSD. The unselected bit-lines form a shield

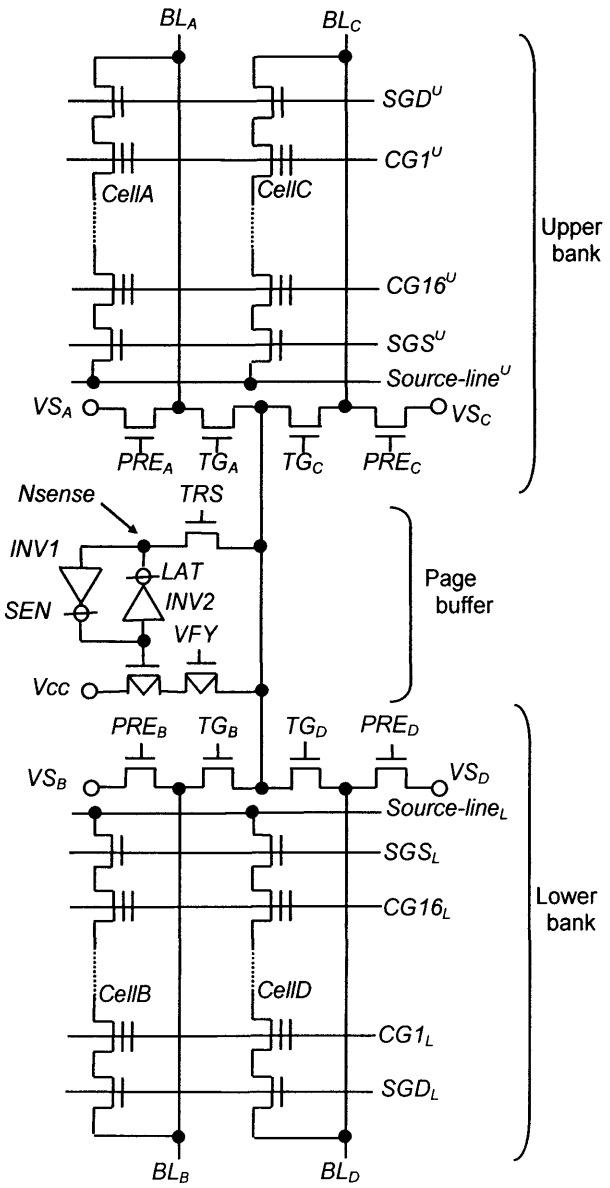


Fig. 6.8 Simplified schematic diagram of a proposed page buffer.

between the selected bit-lines. As a result, the inter bit-line capacitive coupling noise to the selected bit-lines, BLA and BLB, which act as a dynamic latch, is eliminated.

The proposed program operation is shown in Fig.6.9. The signal timing diagrams of the program pulse, the data transfer, the verify read are shown in Fig.6.10(a), (b) and (c), respectively. At the beginning of the program, the program data of the upper bank are input to the page buffer. In the case of the "0"-program, the node, Nsense in Fig.6.8, is 0V. Nsense of the "1"-program is Vcc. Then, both the TRS-signal and the TGA-signal are activated and the program data are transferred to BLA (step1). After that, TGA is turned off. During the following data load of the lower bank, the program data of CellA are stored on the floating BLA. Next, the program data of the lower bank are loaded to the page buffer.

In step2, the device receives the WRITE command. Then, a program pulse is applied to CellA. In the lower bank, TGB is turned on and the program data are transferred to BLB. In step3, the program pulse is applied to CellB. The timing diagram of programming CellB is shown in Fig.6.10(a). In the case of the "0"-programming, Nsense is Vss and BLB is biased to 0V. As a result, electrons are injected form the grounded channel to the floating gate. If the program data are "1", Nsense is Vcc. As a result, BLB is applied to Vcc and the electron injection into CellB is prohibited.

Next, we proceed to the verify read of CellA. First, TGB is turned off and TGA is turned on. In step4, the program data on BLA are transferred to the page buffer. The timing diagram of the data transfer is shown in Fig.6.10(b). The clocked inverters, INV1, 2 are deactivated at Tdt1. At Tdt2, the TRS-signal is activated and the bit-line voltage is transferred to the sense node. The voltage of Nsense is sensed with the clocked inverter, INV1 at Tdt3. The program data of CellA are latched at Tdt4.

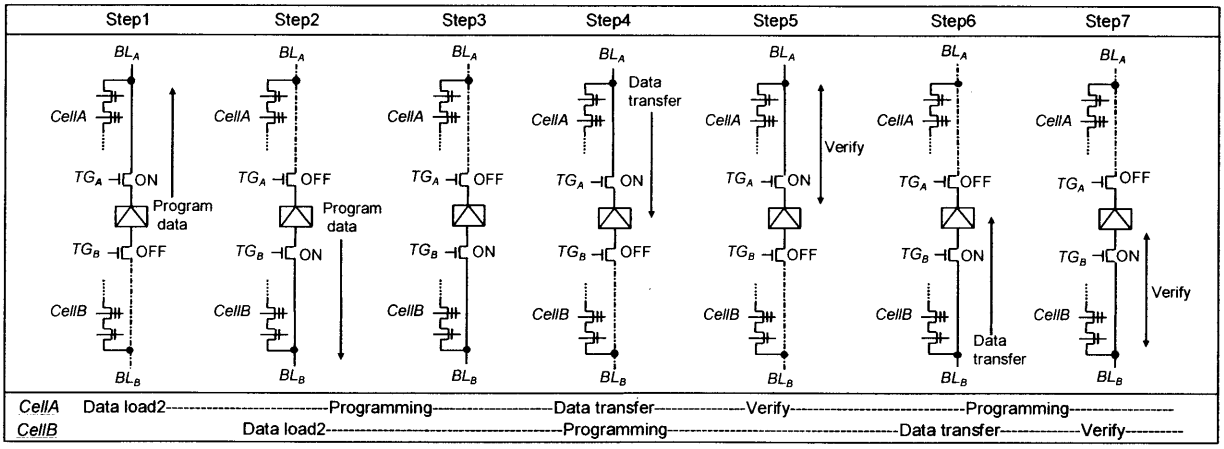


Fig. 6.9 Proposed program operation.

Then the verify read of CellA is performed in step5. The timing diagram of the verify read is shown in Fig.6.10(c). First, BLA is pre-charged to 1.2V at Tv1. The word-lines are activated at Tv2. The bit-line is kept or discharged according to the memory cell data. At Tv3, the VFY-signal is activated. As a result, the bit-line of the "1"-program is charged to Vcc. In the case of the "0"-program, the bit-line is kept at the predetermined voltage. At Tv4, the bit-line voltage is transferred to the sense node, Nsense. By activating the SEN-signal, the voltage of BLA is sensed at Tv5. As a result, the reprogram data in the page buffer are modified such that the programming is executed only on memory cells that have not been successfully programmed [37]. At Tv6, the LAT-signal is activated and the reprogram data are transferred to BLA. After that, the reprogram of CellA is performed.

During the reprogramming of CellA, CellB is verified. TGA is turned off and then TGB is turned on. At first, the program data of CellB are transferred to the page buffer in step6.

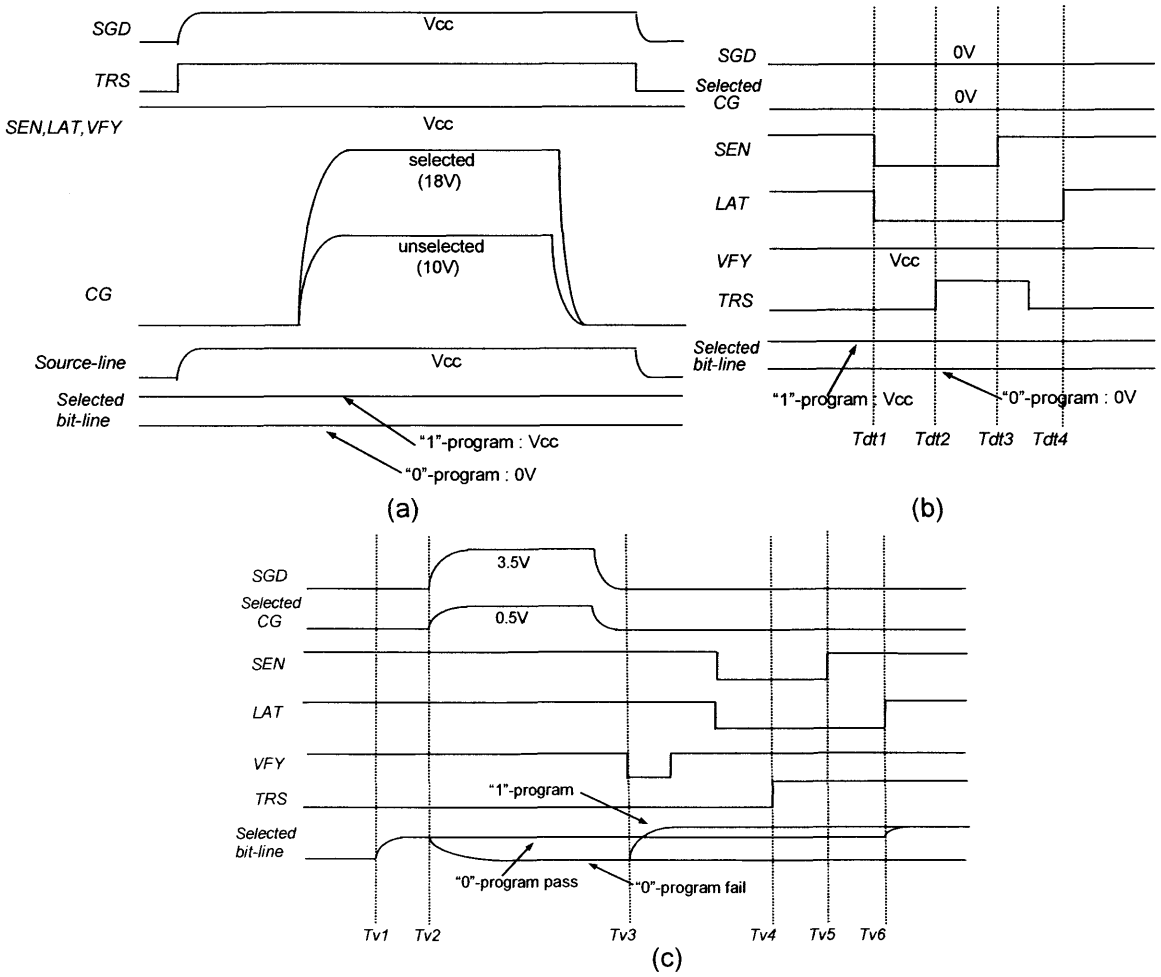


Fig. 6.10 Signal timing diagram. (a) Program pulse. (b) Data transfer from the bit-line to the page buffer. (c) Verify read operation.

Then the verify read of CellB is executed in step7. The verify read and the reprogram are repeated until all memory cells are successfully programmed.

6.5 Experimental results

Fig.6.11 depicts the conventional and the proposed program operations. In this Figure, the number of program and verify read cycles is assumed to be four. In the proposed

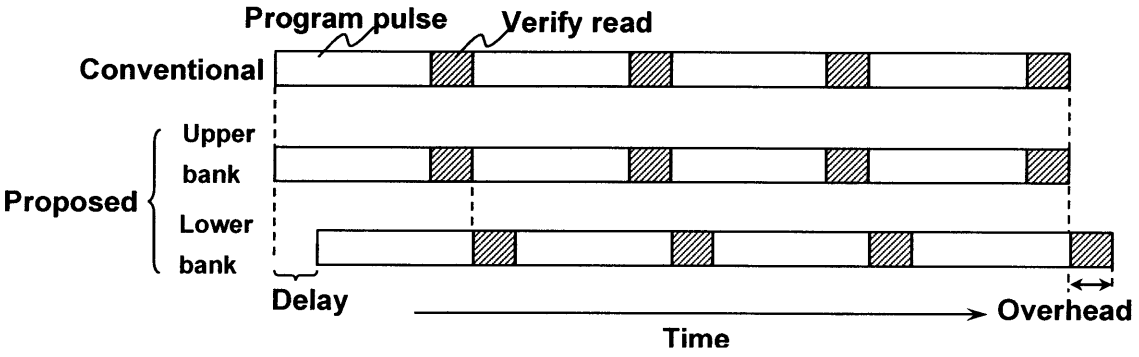


Fig. 6.11 Comparison of the conventional and the proposed program operations. The number of program and verify read cycles is assumed to be four.

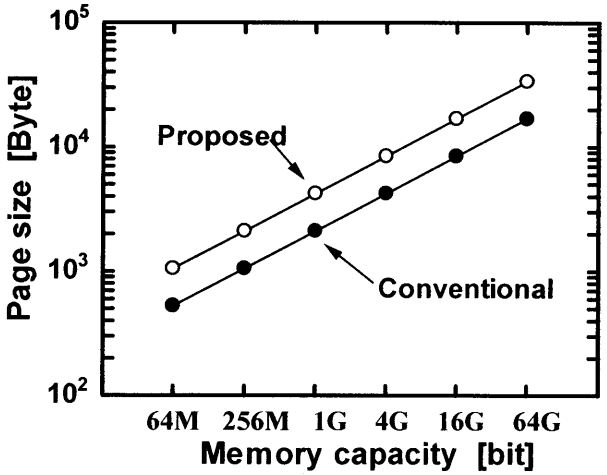


Fig. 6.12 Page size trend. The chip size of the proposed scheme is assumed to be the same as that of the conventional scheme.

scheme, the programming, the data transfer and the verify read are repeated without interruption. Two factors causes to prolong the programming time of the proposed scheme. The first one is the data transfer. Each program cycle of the proposed scheme is composed of the program pulse, the data transfer and the verify read, whereas the conventional one consists of the program pulse and the verify read. Therefore, the data transfer is an overhead.

The second one is that the program cycle of the lower bank is delayed, compared with that of the upper bank, as shown in Fig.6.11. For example, although the verify read of CellA is performed in step5 of Fig.6.9, that of CellB is executed in step7. In total, these overheads increase the program time by 5%.

Fig.6.12 shows the page size trend. It is assumed that the number of page buffers

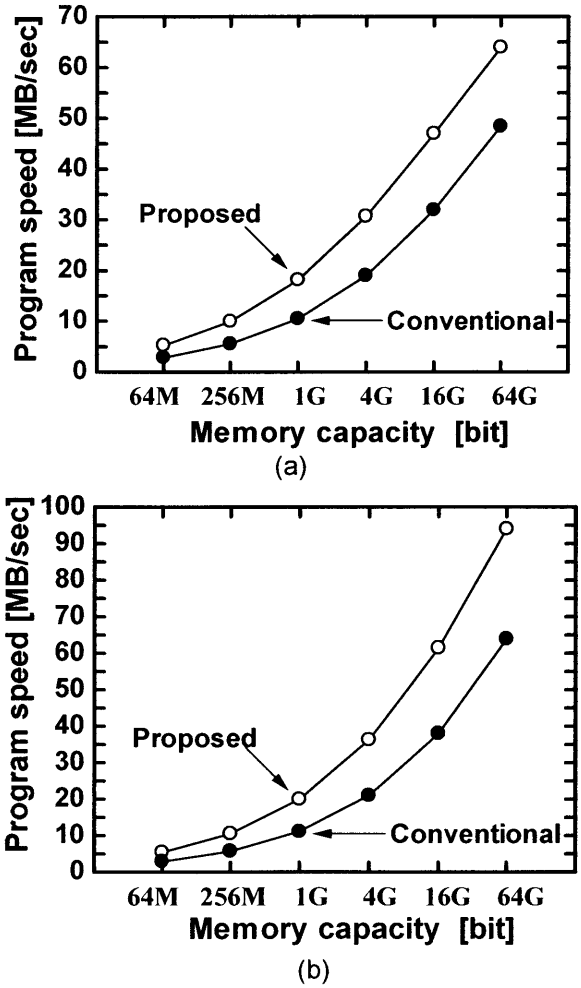


Fig. 6.13 Program throughput. The data input rate is assumed to be (a) 100 Mbyte/sec and (b) 200 Mbyte/sec.

doubles as the memory capacity quadruples to keep the circuit area of the page buffers less than 10% of the chip size. The page size of the proposed scheme is twice that of the conventional one. Fig.6.13(a) shows the program throughput. The data input rate is assumed to be 100-Mbyte/sec. With this new architecture, the program speed increases by 73% in a 1-Gbit generation and 62% in a 4-Gbit generation, because twice as many memory cells are programmed simultaneously. 18.2-Mbyte/sec 1-Gbit or 30.7-Mbyte/sec 4-Gbit NAND flash memory can be realized with this new architecture. Although the page size is doubled, the program speed is not doubled due to the overheads described above and the prolonged data load. As the page size increases, the data loading becomes longer and degrades the program speed. If the data input is accelerated by increasing the bus frequency or the data bus width, the program speed is improved. Actually, in the case that the data input rate is 200 Mbyte/sec, the program throughput can be increased to 20.0 Mbyte/sec or 36.3 Mbyte/sec in a 1-Gbit or 4-Gbit generation, respectively.

6.6 Design considerations

In this section, some noise problems of the proposed architecture are discussed. When operating a bit-line as a dynamic latch, there are two major concerns. The first one is a charge leakage from a floating bit-line. The second one is a capacitive coupling noise to a bit-line. In addition, power consumption is discussed.

6.6.1 Charge leakage issue

During the programming, the select transistor eliminates the charge leakage of a bit-line, as discussed in Section 6.2. In this section, I will discuss the charge leakage more in detail. In the selected NAND string, the select transistor connected to the source-line is turned off. In the unselected NAND strings, the select transistors connected to the bit-line are turned off. To suppress the voltage change of a floating bit-line during the read to be much less than 0.01V [1, 36], the charge leakage of each select transistor is designed to be less than 5pA. Therefore, although as many as one thousand select transistors are connected to a bit-line, the drop of the "1"-program bit-line is suppressed to be less than 0.01V.

6.6.2 Capacitive coupling noise

The capacitive coupling noise does not cause a serious problem. First, the inter bit-line capacitive coupling noise to the selected bit-line, is eliminated by adopting the shielded bit-line method, as described in Section 6.4.

The second source of the capacitive coupling noise is the control gates shown in Fig.6.14.

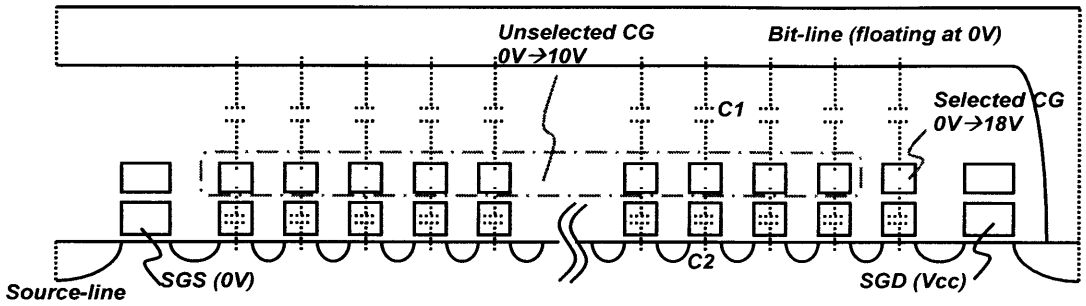


Fig. 6.14 Capacitive coupling noise between control gates and a bit-line. During the "0"-program, the bit-line is kept floating at 0V.

In the case of the "0"-program, both the bit-line and the channel of memory cells are biased to 0V and then kept floating. When the control gates are raised to Vpgm or Vpass, the channel and the bit-line are raised due to the capacitance, C1 and C2 in Fig.6.14. In a NAND flash memory, one bit-line is connected to one thousand NAND strings, as mentioned above. Among them, only one NAND string operates at a time and its capacitive coupling to a bit-line is very small. Actually, when the control gates are raised to Vpgm or Vpass during the programming, the bounce of a floating bit-line is less than 0.01V. Therefore, the use of a bit-line as a dynamic latch does not cause any problem.

6.6.3 Power consumption

In the proposed scheme, while the page size is doubled, the power consumption is almost the same as the conventional architecture. In the proposed scheme, the capacitance of the bit-line is half because the bit-line length is half. Therefore, although the number of bit-lines is doubled, the total bit-line capacitance in a chip is the same as the conventional architecture. Thus, the power consumption is the same as the conventional architecture.

6.7 Summary

A new programming scheme, a dual page programming scheme, is proposed which drastically increases the program throughput without circuit area overhead. By using a bit-line as a dynamic latch, the page size can be doubled without increasing the page buffers. The charge leakage from and the capacitive coupling noise to the dynamic latch is negligibly small. Although the page size is doubled, the total bit-line capacitance is the same as the conventional architecture and thus the power consumption is the same as the conventional architecture. The programming is accelerated by 73% in a 1-Gbit generation

and 62% in a 4-Gbit generation. 18.2-Mbyte/sec 1-Gbit or 30.7-Mbyte/sec 4-Gbit NAND flash memory can be realized with this new scheme. The program speed trend of 3V single-level cell is shown in Fig.6.15. By using this new architecture, an extremely high-speed 30MB/sec single-level NAND flash memory can be realized and the speed target of the 3V multi-level cell described in Chapter 1 is fulfilled. The operation is verified with Spice simulation. This architecture is a promising candidate for the prospective high-speed multi-Gb-scale NAND flash memories.

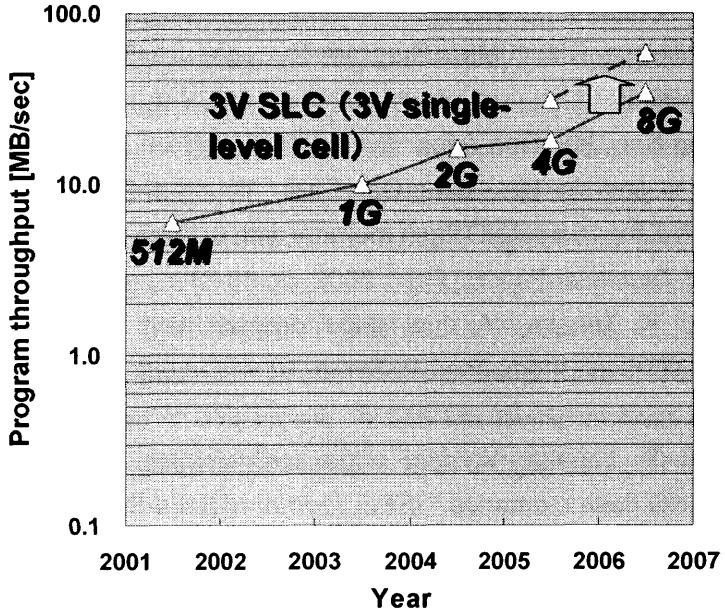


Fig.6.15 Program speed improvement with the parallel write technology

References

[1] K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, K. Takeuchi, T. Ikehashi, K. Kanda, K. Hosono, R. Shirota, S. Aritome, K. Shimizu, K. Hatakeyama and K. Sakui " A 130mm^2 256Mb NAND Flash with Shallow Trench Isolation Technology," *ISSCC Digest of Technical Papers*, 1999, pp.112-113.

[2] K. Kobayashi, "Toshiba's NAND flash strategy", in *CEATEC 2004 Dig. Tech. Papers*, Oct. 2004.

[3] H.Nakamura, K.Imamiya, T.Himeno, T.Yamamura, T.Ikehashi, K.Takeuchi, K.Kanda, K.Hosono, T.Futatsuyama, K.Kawai, R.Shirota, N.Arai, Fumitaka Arai, K.Hatakeyama, H.Hazama, Masanobu Saito, H.Meguro, K.Conley, K. Quader and J.Chen, "A 125mm^2 1Gb NAND Flash Memory with 10MB/s Program Throughput," *ISSCC Digest of Technical Papers*, 2002, pp.106-107.

[4] June Lee, Heung-Soo Im, Dae-Seok Byeon, Kyeong-Han Lee, Dong-Hyuk Chae, Kyong-Hwa Lee, Young-Ho Lim, Jung-Dal Choi, Young-Il Seo, Jong-Sik Lee, and Kang-Deog Suh, "A 1.8V 1Gb NAND flash memory with 0.12um STI process technology", in *ISSCC Digest of Technical Papers*, Feb., 2002, pp.80-81.

[5] K. Takeuchi and T. Tanaka, "A dual page programming scheme for high-speed multi-Gb-scale NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 2000, pp.156-157.

[6] K. Takeuchi and T. Tanaka, "A dual page programming scheme for high-speed multi-Gb-scale NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.36 no.5, May 2001, pp.744-751.

[7] F. Masuoka, M. Momodomi, Y. Iwata and R. Shirota, "New ultra high density EPROM and flash EEPROM with NAND structured cell," in *IEDM Tech. Dig.,* 1987, pp.552-555.

[8] K. Imamiya, Y. Iwata, Y. Sugiura, H. Nakamura, H. Oodaira, M. Momodomi, Y. Ito, T. Watanabe, H. Araki, K. Narita, K. Masuda and J. Miyamoto, "A 35 ns-cycle-time 3.3 V-only 32 Mb NAND flash EEPROM", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.32-33.

[9] T.Tanaka, M.Momodomi, Y.Iwata, Y.Tanaka, H.Oodaira, Y.Itoh, R.Shirota, K.Ohuchi and F.Masuoka,"A 4-Mbit NAND-EEPROM with Tight Programmed Vt Distribution," *Symp. VLSI Circuits Dig. Tech. Papers*, June 1990, pp.105-106.

[10] K. D. Suh, B. H. Suh, Y. H. Lim, J. K. Kim, Y. J. Choi, Y. N. Koh, S. S. Lee, S. C. Kwon, B. S. Choi, J. S. Yum, J. H. Choi, J. R. Kim, and H. K. Lim, "A 3.3V 32Mb NAND flash memory with incremental step pulse programming scheme," in *ISSCC Digest of Technical Papers*, Feb. 1995, pp.128-129.

[11] T. Takeshima, H. Sugawara, H. Takada, Y. Hisamune, K. Kanamori, T. Okazawa, T. Murotani and I. Sasaki, "A 3.3V single-power-supply 64Mb flash memory with dynamic bit-line latch (DBL) programming scheme," in *ISSCC Digest of Technical Papers*, Feb.,

1994, pp.148-149.

[12] S. Aritome, R. Shirota, R. Kirisawa, T. Endoh, R. Nakayama, K. Sakui, and F. Masuoka, "A reliable bi-polarity write/erase technology in flash EEPROMs", in *IEDM Tech. Dig.,* 1990, pp.111-114.

[13] S. Satoh, T. Nakamura, K. Shimizu, K. Takeuchi, H. Iizuka, S. Aritome, and R. Shirota, "A novel gate-offset NAND cell (GOC-NAND) technology suitable for high-density and low-voltage-operation flash memories", in *IEDM Tech. Dig.,* 1999, pp.271-274.

[14] A. Goda, W. Moriyama, H. Hazama, H. Iizuka, K. Shimizu, S. Aritome, and R. Shirota, "A novel surface-oxidized barrier-SiN cell technology to improve endurance," in *IEDM Tech. Dig.,* 2000, pp.771-774.

[15] R. Kirisawa, S. Aritome, R. Nakayama, T. Endoh, R. Shirota and F. Masuoka, "A NAND structured cell with a new programming technology for highly reliable 5 V-only flash EEPROM," in *Symp. VLSI Technology Dig. Tech. Papers*, June 1990, pp.129-130.

[16] A. Nozoe, T. Yamazaki, H. Sato, H. Kotani, S. Kubono, K.; Manita, T. Tanaka, T. Kawahara, M. Kato, K. Kimura, H. Kume, R. Hori, T. Nishimoto, S. Shukuri, A. Ohba, Y. Kouro, O. Sakamoto, A. Fukumoto and M. Nakajima, "A 3.3 V high-density AND flash memory with 1 ms/512B erase and program time", in *ISSCC Digest of Technical Papers*, 1995, pp.126-127.

[17] A. Nozoe, H. Kotani, T. Tsujikawa, K. Yoshida, K. Furusawa, M. Kato, T. Nishimoto, H. Kume, H. Kurata, N. Miyamoio, S. Kubono, I. Kanamitsu, K. Koda, T. Nakayama, Y. Kouro, A. Hosogane, N. Ajika, and K. Kobayashi, "A 256 Mb multilevel flash memory with 2 MB/s program rate for mass storage applications", in *ISSCC Digest of Technical Papers*, Feb., 1999, pp.110-111.

[18] T. Ishii, K. Oshima, H. Sato, S. Noda, J. Kishimoto, H. Kotani, A. Nozoe, K. Furusawa, T. Yoshitake, M. Kato, M. Takaheshi, A. Sato, S. Kubano, K. Manita, K. Koda, T. Nakayama and A. Hosogane, "A 126.6 mm^2 AND-type 512 Mb flash memory with 1.8 V power supply", in *ISSCC Digest of Technical Papers*, Feb., 2001, pp.30-31.

[19] H. Miwa, T. Tanaka, K.; Oshima, Y. Nakamura, T. Ishii, A. Ohba, Y. Kouro, T. Furukawa, Y. Ikeda, O. Tsuchiya, R. Hori and K. Miyazawa, "A 140 mm^2 64 Mb AND flash memory with a 0.4um technology", in *ISSCC Digest of Technical Papers*, Feb., 1996, pp.34-35.

[20] S. Kobayashi, M. Mihara, Y. Miyawaki, M. Ishii, T. Futatsuya, A. Hosogane, A. Ohba, Y. Terada, N. Ajika, Y. Kunori, K. Yuzuriha, M. Hatanaka, H. Miyoshi, T. Yoshihara, Y. Uji, A. Matsuo, Y. Taniguchi and Y. Kiguchi, "A 3.3 V-only 16 Mb DINOR flash memory", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.122-123.

[21] M. Mihara, Y. Miyawaki, O. Ishizaki, T. Hayasaka, K. Kobayashi, T. Omae, H. Kimura, S. Shimizu, H. Makimoto, Y. Kawajiri, M. Wada, H. Sonoyama and J. Etoh, "A 29 mm^2 1.8V-only 16Mb DINOR Flash Memory with Gate-Protected Poly-Diode (GPPD) Charge Pump," in *ISSCC Digest of Technical Papers*, Feb., 1999, pp.114-116.

[22] M. Ohkawa, H.; Sugawara, N. Sudo, M. Tsukiji, K. Nakagawa, M. Kawata, K. Oyama, T. Takeshima and S. Ohya, "A 98 mm^2 3.3 V 64 Mb flash memory with FN-NOR type 4-level cell",

in *ISSCC Digest of Technical Papers*, Feb., 1996, pp.376-379.

[23] A. Baker, R. Alexis, S. Bell, V. Dalvi, R. Durante, E. Baer, M. Fandrich, O. Jungroth, J. Kreifels, M. Landgraf, K. Lee, H. Pon, M. Rashid, R. Rozman, J. Tsang, K. Underwood, C. Yarlagadda, "A 3.3 V 16 Mb flash memory with advanced write automation", in *ISSCC Digest of Technical Papers*, Feb., 1994, pp.146-147.

[24] T. Jinbo, H. Nakata, K. Hashimoto, T. Watanabe, K. Ninomiya, T. Urai, M. Koike, T. Sato, N. Kodama, K. Oyamaand T. Okazawa, "A 5 V-only 16 Mb flash memory with sector-erase mode", in *ISSCC Digest of Technical Papers*, Feb., 1992, pp.154-155.

[25] K. Seki, H. Kume, Y. Ohji, T. Tanaka, T. Adachi, M. Ushiyama, K. Shimohigashi, T. Wada, K. Komori, T. Nishimoto, K. Izawa, T. Hagiwara, Y. Kubota, K. Shohji, N. Miyamoto, S. Saeki and N. Ogawa, "An 80 ns 1 Mb flash memory with on-chip erase/erase-verify controller", in *ISSCC Digest of Technical Papers*, Feb., 1990, pp.60-61.

[26] D. Mills, M. Bauer, A. Bashir, R. Fackenthal, K. Frary, T. Gullard, C. Haid, J. Javanifard, P. Kwong, D. Leak, S. Pudar, M. Rashid, R. Rozman, S. Sambandan, S.; Sweha and J. Tsang, "A 3.3V 50MHz synchronous 16Mb flash memory", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.120-121.

[27] M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, M. Ishac, J. Javanifard, M. Landgraf, D. Leak, K. Loe, D. Mills, P. Ruby, R. Rozman, S. Sweha, S. Talreja and K. Wojciechowski, "A multilevel-cell 32 Mb flash memory", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.132-133.

[28] S. Atsumi, A. Umezawa, M. Kuriyama, N. Banba, N. Ohtsuka, N. Tomita, Y. Iyama, T. Miyaba, R. Sudoh, E. Kamiya, M. Tanimoto, Y. Hiura, Y. Araki, E. Sakagami, N. Arai, S. Mori, "A 3.3 V-only 16 Mb flash memory with row-decoding scheme", in *ISSCC Digest of Technical Papers*, Feb., 1996, pp.42-43.

[29] G. Campardo, R. Micheloni, S. Commodaro, E. Yero, M. Zammabio, S. Mognoni, A. Sacco, M. Picca, A. Manstleita, M. Scotti, I. Motta, C. Golla, A. Pierin, A. Ohba, T. Fulatsuya, R.; Makabe, S. Kawai, Y. Kai, S. Shimizu, T. Ohnakado, I. Sugihara, R. Bez, A. Grossi, A. Modelli, P. Khouri, and G. Torelli, "A 40 mm^2 3 V 50 MHz 64 Mb 4-level cell NOR-type flash memory", in *ISSCC Digest of Technical Papers*, Feb., 2000, pp.274-275.

[30] S. Atsumi, A. Umezawa, T. Tanzawa, T. Taura, H.; Shiga, Y. Takano, T. Miyaba, M. Matsui, H. Watanabe, K. Isobe, S. Kitamura, S. Yamada, M. Saito, S. Mori, and T. Watanabe, "A channel-erasing 1.8 V-only 32 Mb NOR flash EEPROM with a bit-line direct-sensing scheme", in *ISSCC Digest of Technical Papers*, Feb., 2000, pp.276-277.

[31] B. Pathak, A. Cabrera, G. Christensen, A. Darwish, M. Goldman, R. Haque, J. Jorgensen, R. Kajley, T. Ly, F. Marvin, S. Monasa, Q. Nguyen, D. Pierce, A. Sendrowski, I. Sharif, H. Shimoyoshi, A. Smidt, R. Sundaram, M. Taub, W. Tran, R. Trivedi, P. Walimbe and E. Yu, "A 1.8 V 64 Mb 100 MHz flexible read while write flash memory", in *ISSCC Digest of Technical Papers*, Feb., 2001, pp.32-33.

[32] T.Tanzawa, A. Umezawa, T. Taura, H. Shiga, T. Hara, Y. Takano, T. Miyaba, N. Tokiwa,

K. Watanabe, H. Watanabe, K. Masuda, K. Naruke, H. Kato, S. Atsumi, "A 44 mm^2 4-bank 8-word page read 64 Mb flash memory with flexible block redundancy and fast accurate word-line voltage controller", in *ISSCC Digest of Technical Papers*, Feb., 2002, pp.102-103.

[33] H. Stiegler, B. Ashmore, R. Bussey, M. Gill, S. Lin, M. McConnell, D. McElroy, J. Schreck, P. Shah, P. Truong, A.L. Esquivel, J. Paterson and B. Riemenschneider, "A 4Mb 5V-only flash EEPROM with sector erase", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1990, pp.103-104.

[34] S.C. Tsao, J.E. Frayer, C.S. Pang, Y. Ma, K. Kwon Y. Choi, D. Kim, J. Kim, and J. Park, "A 5V-only 16M flash memory using a contactless array of source-side injection cells", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1995, pp.77-78.

[35] J. C. Chen, T. H. Kuo, L. E. Cleveland, C. K. Chung, N. Leong, Y. K. Kim, T. Akaogi and Y. Kasa, "A 2.7V only 8Mbx16 NOR Flash Memory", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1996, pp.172-173.

[36] T. Tanaka, Y. Tanaka, H. Nakamura, K. Sakui, H. Oodaira, R. Shirota, K. Ohuchi, F. Masuoka, and H. Hara, "A quick intelligent programming architecture and a shielded bit-line sensing method for 3V-only NAND flash memory," *IEEE J. Solid-State Circuits*, vol.29, November 1994, pp.1366-1373.

[37] T. Tanaka, Y. Tanaka, H. Nakamura, H. Oodaira, S. Aritome, R. Shirota, and F. Masuoka, "A quick intelligent program architecture for 3V-only NAND-EEPROMs," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1992, pp.20-21.

CHAPTER 7
DISCUSSION AND CONCLUSION

7.1 Discussion on future program speed trend

This section describes the future program speed trend for the 3V multi-level cell, the low-voltage multi-level cell and the 3V single-level, that is, how the program speed will improve by utilizing the proposed technologies discussed in Chapter 3, 4, 5 and 6.

A. 3V multi-level cell

Fig.7.1(a) describes the future program speed trend of the 3V multi-level cell. First, the multi-page cell technology [1], [2] described in Chapter 3 made it possible to improve the program speed by 130% and realized the 1MB/sec 3V multi-level cell. By using this technology, the world first 3V multi-level NAND flash memory with 0.16um CMOS double metal technologies was commercialized in 2001 [3]. All 3V multi-level cell products such as 0.16um 1Gbit [3], 0.13um 2Gbit [4], 90nm 4Gbit [5], [6] and 70nm 8Gbit [7] products adopt this multipage cell technology.

Next, in the near future, the program speed of the 3V multi-level cell will be improved by using the low noise technology [8], [9] described in Chapter 5. By adopting a new array architecture, a double-level Vth select-gate array architecture, both a source-line noise as well as the inter bit-line capacitive coupling noise are eliminated. As a result, the program speed will improve by 77% and a very fast 10MB/sec 3V multi-level cell products will be realized with this new architecture as shown in Fig.7.1(a), fulfilling the speed target of the 3V multi-level cell.

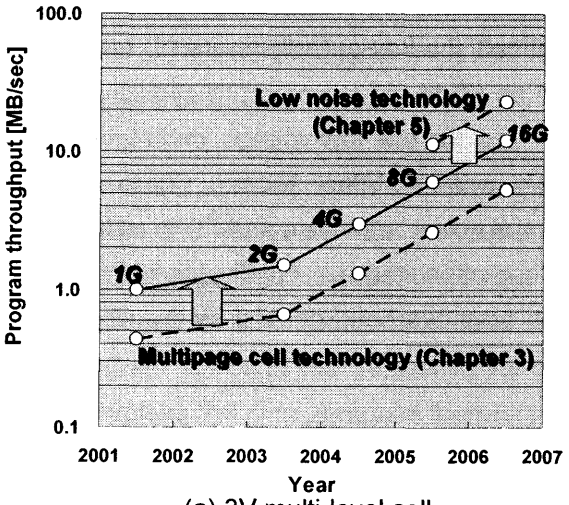
B. Low-voltage multi-level cell

Fig.7.1(b) describes the program speed trend of the low-voltage multi-level cell. Like the 3V multi-level cell, the multipage cell technology described in Chapter 3 is essential to realize the low-voltage multi-level cell. In addition, the low load capacitance technology [10], [11] is necessary to actualize the low-voltage multi-level cell products. By means of the low load capacitance technology shown in Chapter 4, the program speed is improved by

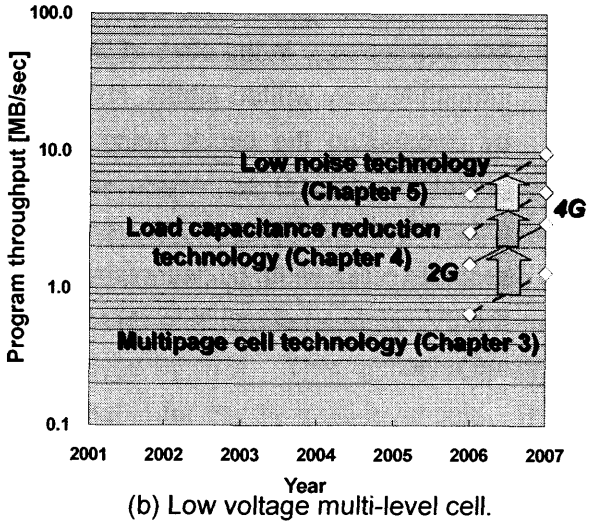
70%. Moreover, a small energy dissipation and a low cost are achieved at the same time. Finally, the low noise technology shown in Chapter 5 will be adopted to further accelerate the performance of the low voltage multi-level cell. By adopting a new sensing scheme, Vcc bit-line sensing scheme [12], [13], the program speed will improve by 57% and a fast programming 5MB/sec low voltage multi-level cell will be realized, achieving the speed target of the low voltage multi-level cell.

C. 3V single-level cell

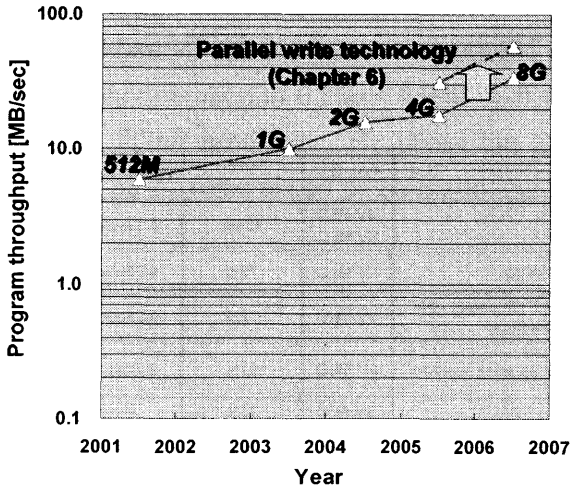
A dual page programming scheme [14], [15] described in Chapter 6 will be implemented in the 3V single-level cell. A very high program throughput will be realized without circuit area overhead. By using this new architecture, an extremely high-speed 30MB/sec single-level NAND flash memory can be realized, fulfilling the speed target of the 3V multi-level cell.



(a) 3V multi-level cell.



(b) Low voltage multi-level cell.



(c) 3V single-level cell.

Fig.7.1 Future program speed trend.

7.2 Conclusion

Circuit design techniques of the NAND flash memory for the high-speed programming have been discussed. The programming mechanism are analyzed and moreover based on the analysis novel circuit techniques are proposed to realize a high-speed programming NAND flash memories.

In this chapter, the achievements of this research are summarized. Table 7.1 summarizes the figure of merits of the new circuits described in each chapter. The followings are investigated in this research.

1) Basic principles of the program operation are developed. Furthermore, an analytical framework of the program throughput is proposed. The program speed is expressed as a function of key parameters, such as the simultaneously written states, the program pulse width, the verify read time, the circuit noise and the page size. By using the framework, the problems, the guidelines and the solutions for the high-speed design are developed. In the case of 3V multi-level cell, the key guidelines are (1) to reduce simultaneously written states, Nstate as well as (2) to reduce program cycles, Npulse by decreasing the circuit noise, ΔVnoise. As for the low-voltage multi-level cell, guidelines are (1) to reduce simultaneously written states, Nstate, (2) to reduce program cycles, Npulse by decreasing the circuit noise, ΔVnoise and (3) to reduce the program pulse width by decreasing the core load capacitance. Finally, the guideline of the 3V single-level cell is to (1) to reduce the area overhead caused by the page size increase.

2) To improve the performance of the 3V multi-level cell as well as the low voltage multi-level cell, a multi-page cell technology is proposed. This technology allows for both the precise control of the threshold voltage of a memory cell and fast programming without area penalty. The program speed of the 3V and low voltage multi-level cell is

Chapter	Methodology		Category	Speed improvement	Verification method	Commercial products
3	Multipage cell technology		3V MLC LV MLC	130%	0.16um product	All MLC products with 0.16um 0.13um, 90nm and 70nm.
4	Load capacitance reduction technology		LV MLC	70%	0.25um product	0.25um products
5	Low noise technology	Double-level Vth select gate array architecture	3V MLC	77%	0.25um product	-
		Vcc bit-line sensing scheme	LV MLC	57%	0.7um test chip	All SLC&MLC products with 0.25um, 0.16um, 0.13um, 90nm and 70nm.
6	Parallel write technology		3V SLC	73%	simulation	-

Table 7.1 Figure of merits of the proposed circuits.

accelerated by 130%. A fast programming of more than 1MB/sec multi-level cell is realized with 0.16um CMOS double metal technology. Due to this novel technology, the program speed of the multi-level cell becomes higher than 1MB/sec and consequently enabled us to commercialize first multi-level 1Gbit products. The multipage cell technology is used in all multi-level cell NAND flash memory products such as 0.16um 1Gbit, 0.13um 2Gbit, 90nm 4Gbit and 70nm 8Gbit products. In addition to the program speed improvement, the random read access time becomes half because only one or two cycles are required during the read. Moreover, a higher reliability with four orders of magnitudes less error rate is secure with this new architecture.

3) A low load capacitance technology is proposed for the low voltage multi-level cell. The proposed architecture shows excellent program disturb characteristics irrespective of the supply voltage. The program speed of the low-voltage multi-level cell is improved by 70%. In addition, small energy dissipation and low cost are achieved at the same time. The proposed scheme is verified with commercial 0.25um 256Mbit NAND flash memory [16].

4) The effect of the array noise such as an inter bit-line capacitive coupling noise and the source-line noise on the performance are analyzed. Moreover, two low noise technologies are proposed. First, a double-level Vth select gate array architecture is proposed for the 3V multi-level cell. The circuit noise is eliminated and as a result, the program speed of the 3V multi-level cell is improved by 77%. This architecture also minimizes the chip area and therefore is best suitable for the 3V multi-level cell. The proposed cell array is verified with 0.7um NAND flash memory. Second, the Vcc bit-line shield sensing method is proposed for the low-voltage multi-level cell. Again, the circuit noise is suppressed and the program speed is improved by 57%. The new sensing method is verified with 0.25um 256Mbit NAND flash memory. This technology is used in the erase verify operation in 0.25um 256Mbit, 0.16um 1Gbit, 0.13um 2Gbit, 90nm 4Gbit and 70nm 8Gbit products. By using the low noise technology, fast programming 10MB/sec 3V multi-level cell or 5MB/sec low-voltage multi-level cell can be realized.

Market	Product	Performance improvement	Program speed	Chapter	Circuit technologies
Mass market	3V MLC	307%	10MB/s	3	Multipage cell technology
				5	Low noise technology
Mobile market	LV MLC	514%	5MB/s	3	Multipage cell technology
				4	Low load capacitance technology
				5	Low noise technology
High-end market	3V SLC	73%	30MB/s	6	Parallel write technology

Table 7.2 Summary of the research

5) A new programming scheme, a dual page programming scheme, is proposed for the 3V single-level cell. The new scheme drastically increases the program throughput without circuit area overhead. By using a bit-line as a dynamic latch, the page size can be doubled without increasing the page buffers. The charge leakage from and the capacitive coupling noise to the dynamic latch is negligibly small. By using this new architecture, an extremely high-speed 30MB/sec single-level NAND flash memory can be realized.

6) Finally, the future program speed trend for the 3V multi-level cell, the low-voltage multi-level cell and the 3V single-level are presented. By utilizing the circuit techniques mentioned above, the 10MB/sec 3V multi-level cell, the 5MB/sec low voltage multi-level cell and the 30MB/sec 3V single-level cell will be realized in the near future.

Table 7.2 summarizes the result of this research. The program speed of the 3V multi-level cell, low voltage multi-level cell and 3V single-level cell are all fulfilled with this research. The program speed of the 3V multi-level cell has been improved by 307%. As a result, the world's first 1MB/sec was realized and the world's first multi-level NAND flash memory was commercialized in 2001. Moreover, 10MB/sec 3V multi-level cell is realized, which makes it possible to store HDTV movies or to store a music or movie data as fast as FTTH. The programming of the low voltage multi-level cell has been accelerated by 514% and 5MB/sec low voltage multi-level cell has been realized, which enables us to take or download DVD movies with mobile phones. Finally, as for the 3V single-level cell, the program speed is improved by 73%. A very fast programming higher than 30MB/sec will

be realized, which makes it possible for digital still cameras to continuously take very high-resolved pictures with more than 10M pixels.

7.3 Perspective

This section describes prospective technologies which have not been studied in this research and instead should be studied in the future to further increase the program speed. Table 7.2 summarizes the prospective technologies.

A. 3V multi-level cell

1) To further increase the memory capacity, multi-level cell technologies with more than 2bit/cell will be developed in the future. In case of more than 2bit/cell, reducing simultaneously written states, Nstate is the most effective way to accelerate the program speed. Therefore, it is recommended to develop a multipage cell technology for more than 2bit/cell to increase the program speed as well as increase the capacity.
2) Decreasing the program pulse width, Tpulse is effective to decrease the programming time. One way to decrease the program pulse is to decrease the word-line ramp up time by introducing hierarchical row decoder. By making half the word-line length, the

Product	Market	High speed circuit techniques	Methodology
3V MLC	Mass market	Reduce simultaneously written states, Nstate	Multipage cell technology for more than 2bit/cell MLC
		Decrease program pulse width, Tpulse	Hierarchical row decoder w.o. area penalty
		Decrease verify read time, Tvfy	Low bit-line swing sensing [17-20]
			Hierarchical row decoder w.o. area penalty
		Increase Vth distribution width, ⊿Vth, which makes worse the cell reliability	More efficient ECC [21], [22]
		Increase page size	Parallel write technology
			Power reduction of core circuits
LV MLC	Mobile market	Decrease program pulse width, Tpulse	Hierarchical row decoder w.o. area penalty
			Efficient charge pump circuit [23-25]
		Decrease verify read time, Tvfy	Low bit-line swing sensing [17-20]
			Hierarchical row decoder w.o. area penalty
		Increase Vth distribution width, ⊿Vth, which makes worse the cell reliability	More efficient ECC [21], [22]
		Increase page size	Parallel write technology
			Power reduction of core circuits
3V SLC	High-end market	Decrease program pulse width, Tpulse	Hierarchical row decoder w.o. area penalty
		Decrease verify read time, Tvfy	Low bit-line swing sensing [17-20]
			Hierarchical row decoder w.o. area penalty
		Increase page size	Power reduction of core circuits
		Accelerate data loading	Pipelining of data loading and programming [4], [26]
			High speed interface

Table 7.2 Prospective high-speed circuit techniques beyond this research.

ramp up time of the word-line can be one quarter. Just increasing the number of row decoders drastically increases the chip size. Consequently, new hierarchical row decoder architecture is required.

3) Decreasing the verify read time, Tvfy can also effectively reduce the programming time. New low bit-line swing sensing which accelerates the bit-line discharge through the memory cell or new hierarchical row decoder which decreases the bit-line ramp up time is required.
4) If we can improve the cell reliability by implementing a more efficient ECC, we can increase the Vth distribution width, ⊿Vth, which makes worse the cell reliability. As a result, ⊿Vpgm can be increased, which decreases the number of program pulses, Npulse.
5) The program performance of the multi-level cell can be further improved by introducing the page size with the parallel write technology described in Chapter 6. If the page size increases the power consumption in the page buffer drastically increases. Therefore, a low power technique of the core circuit is required.

B. Low voltage multi-level cell

In addition to the items described in the 3V multi-level cell, a higher efficient charge pump circuit is very effective in decreasing the programming time because at low Vcc, the ramp up time of the charge pump increases the programming time.

C. 3V multi-level cell

In addition to introducing a hierarchical row decoder, decreasing the bit-line swing during the sensing discussed above, reducing the power consumption of the core circuits, accelerating the data loading is required. This is because as the page size increases, the data loading occupies more time during the total programming time. To accelerate the data loading, pipelining of data loading and programming or a high speed interface are recommended.

Finally, Table 7.3 summarizes the capacity trend of various mobile mass storage devices [27]. In case of the NAND flash memory, in the year of 2010, 64Gbit NAND flash memory will be realized with 30nm lithography technologies. By using SiP (System in package) technologies, eight NAND flash chip will be stacked in one package. With SiP technology, in 2010, 64GByte NAND flash memory can be realized, which will be comparable with mobile 1inch HDD in terms of the capacity. Other nonvolatile semiconductor memories such as MRAM, FeRAM and PRAM cannot compete with the NAND flash memory in the file memory market because as shown in Table 7.3 the capacity of other semiconductor

memories is one-tenth of the NAND flash memories. These semiconductor memories have a merit of fast random access. Therefore, they will be used as RAM and will replace DRAM. As for the optical disk, although it has an advantage of a higher capacity over the NAND flash memory, it has many disadvantages such as large size, large power consumption and therefore will not be used in mobile equipments. In summary, in the year 2010, the most promising storage devices are the NAND flash memory and HDD. As mentioned above, since the capacity of the NAND flash memory become comparable with HDD, the NAND flash memory will be used in more mobile electronic devices because NAND flash memory has many advantages such as small size, thin thickness, low power consumption, low supply voltage operation and high reliability compared with HDD. Therefore, research on the program speed improvement of the NAND flash memory will become much more important.

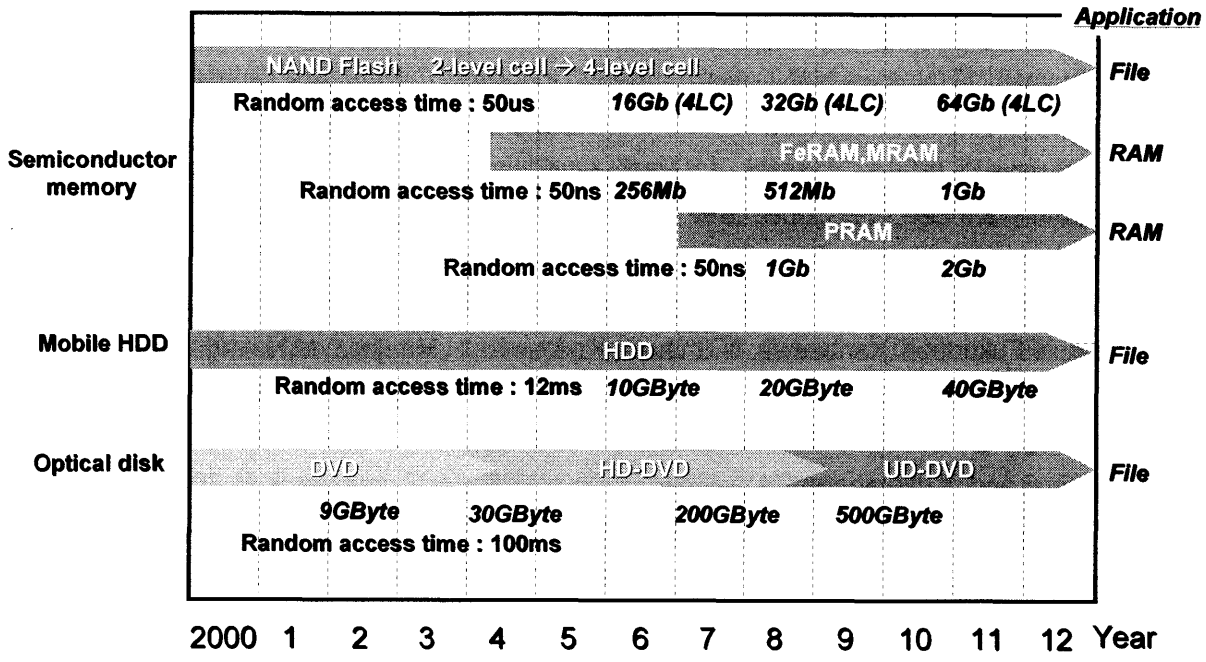


Table 7.3 Future capacity trend of mobile mass storage devices [27].

References

[1] K.Takeuchi, T.Tanaka and T.Tazawa, "A multi-page cell architecture for high-speed programming multi-level NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1997, pp.67-68.

[2] K.Takeuchi, T.Tanaka and T.Tazawa, "A multipage cell architecture for high-speed programming multi-level NAND flash memories", *IEEE Journal of Solid-State Circuits*, vol.33, no.8, August 1998, pp.1228-1238.

[3] S.Aritome, "Advanced flash memory technology and trends for file storage application", in *IEEE Tech. Dig. IEDM 2000*, pp.763-766.

[4] H.Nakamura, K.Imamiya, T.Himeno, T.Yamamura, T.Ikehashi, K.Takeuchi, K.Kanda, K.Hosono, T.Futatsuyama, K.Kawai, R.Shirota, N.Arai, Fumitaka Arai, K.Hatakeyama, H.Hazama, Masanobu Saito, H.Meguro, K.Conley, K. Quader and J.Chen, "A 125mm^2 1Gb NAND Flash Memory with 10MB/s Program Throughput," *ISSCC Digest of Technical Papers*, 2002, pp.106-107.

[5] K. Kobayashi, "Toshiba's NAND flash strategy", in *CEATEC 2004 Dig. Tech. Papers*, Oct. 2004.

[6] D.S. Byeon, S.S.Lee, Y.H.Lim, J.S.Park, W.K.Han, P.S.Kwak, D.H.Kim, D.H.Chae, S.H.Moon, S.J.Lee, H.C.Cho, J.W.Lee, M.S.Kim, J.S.Yang, Y.W.Park, D.W.Bae, J.D.Choi, S.H.Hur and K.D.Suh, "An 8Gb multi-level NAND flash memory with 63nm STI CMOS process technology", in *ISSCC Digest of Technical Papers*, 2005, pp.46-47.

[7] T.Hara, K.Fukuda, K.Kanazawa, N.Shibata, K.Hosono, H.Maejima, M.Nakagawa, T.Abe, M.Kojima, M.Fujiu, Y.Takeuchi, K.Amemiya, M.Morooka, T.Kamai, H.Nasu, K.Kawano, C.M.Wang, K.Sakurai, N.Tokiwa, H.Waki, T.Maruyama, S.Yoshikawa, M.Higashitani, T.D.Pham and T.Watanabe, "A 146mm^2 8Gb NAND flash memory with 70nm COMS technology", in *ISSCC Digest of Technical Papers*, 2005, pp.44-45.

[8] K.Takeuchi, T.Tanaka and H.Nakamura, "A double-level-Vth select gate array architecture for multi-level NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1995, pp.69-70.

[9] K.Takeuchi, T.Tanaka and H.Nakamura, "A double-level-Vth select gate array architecture for multi-level NAND flash memories", *IEEE Journal of Solid-State Circuits*, vol.31, no.4, April 1996, pp.602-609.

[10] K. Takeuchi, S. Satoh, K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, T. Ikehashi, K. Kanda, K. Hosono and K. Sakui, "A source-line programming scheme for low voltage operation NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1999, pp.37-38.

[11] K. Takeuchi, S. Satoh, K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, T. Ikehashi, K. Kanda, K. Hosono and K. Sakui, "A source-line programming scheme for low voltage operation NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.35 no.5, May

2000, pp.672-681.

[12] K. Takeuchi, S. Satoh, T. Tanaka, K. Imamiya, and K. Sakui, " A negative Vth cell architecture for highly scalable, excellently noise immune and highly reliable NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1998, pp.234-235.

[13] K. Takeuchi, S. Satoh, T. Tanaka, K. Imamiya, and K. Sakui, " A negative Vth cell architecture for highly scalable, excellently noise immune and highly reliable NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.34, no.5, May 1999, pp.675-684.

[14] K. Takeuchi and T. Tanaka, "A dual page programming scheme for high-speed multi-Gb-scale NAND flash memories," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 2000, pp.156-157.

[15] K. Takeuchi and T. Tanaka, "A dual page programming scheme for high-speed multi-Gb-scale NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.36 no.5, May 2001, pp.744-751.

[16] K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, K. Takeuchi, T. Ikehashi, K. Kanda, K. Hosono, R. Shirota, S. Aritome, K. Shimizu, K. Hatakeyama and K. Sakui " A 130mm^2 256Mb NAND Flash with Shallow Trench Isolation Technology", *ISSCC Digest of Technical Papers*, pp.112-113, 1999.

[17] Tae-Sung Jung, Do-Chan Choi, Sung-Hee Cho, Myong-Jae Kim, Seung-Keun Lee, Byung-Soon Choi, Jin-Sun Yum, San-Hong Kim, Dong-Gi Lee, Jong-Chang Son, Myung-Sik Yong, Heung-Kwun Oh, Sung-Bu Jun, Woung-Moo Lee, Ejaz Haq, Kang-Deog Suh, Syed Ali and Hyung-Kyu Lim, "A 3.3 V 16 Mb nonvolatile virtual DRAM using a NAND flash memory technology", in *ISSCC Digest of Technical Papers*, Feb., 1997, pp.398-399.

[18] M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, M. Ishac, J. Javanifard, M. Landgraf, D. Leak, K. Loe, D. Mills, P. Ruby, R. Rozman, S. Sweha, S. Talreja and K. Wojciechowski, "A multilevel-cell 32 Mb flash memory", in *ISSCC Digest of Technical Papers*, Feb., 1995, pp.132-133.

[19] S. Atsumi, A. Umezawa, T. Tanzawa, T. Taura, H.; Shiga, Y. Takano, T. Miyaba, M. Matsui, H. Watanabe, K. Isobe, S. Kitamura, S. Yamada, M. Saito, S. Mori, and T. Watanabe, "A channel-erasing 1.8 V-only 32 Mb NOR flash EEPROM with a bit-line direct-sensing scheme", in *ISSCC Digest of Technical Papers*, Feb., 2000, pp.276-277.

[20] D. Montanari, J. Van Houdt, G. Groeseneken and E. Maes, "Novel level-identifying circuit for flash multi-level memories", in *ISSCC Digest of Technical Papers*, Feb., 1997, pp.184-187.

[21] T. Tanzawa, T. Tanaka and K. Takeuchi, "A compact on-chip ECC for low cost flash memories", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1996, pp.74-75.

[22] T. Tanzawa, T. Tanaka, K. Takeuchi, R. Shirota, S. Aritome, H. Watanabe, G. Hemink, K. Shimizu, S. Sato, Y. Takeuchi and K. Ohuchi, "A compact on-chip ECC for low cost flash memories", *IEEE Journal of Solid-State Circuits*, vol.32 no.5, 1997, pp.662-669.

[23] T. Tanzawa and T. Tanaka, "A stable programming pulse generator for high-speed programming single power supply voltage flash memories", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1995, pp.73-74.

[24] Ki-Hwan Choi, Jong-Min Park, Jin-Ki Kim, Tae-Sung Jung and Kang-Deog Suh , "Floating-well Charge Pump Circuits For Sub-2.0V Single Power Supply Flash Memories", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1997, pp.61-62.

[25] T. Tanazwa, Y. Tanaka, T. Tanaka, H. Nakamura, H. Oodaira, K. Sakui, M. Momodomi, S. Shiratake, H. Nakano, Y. Oowaki, S. Watanabe, K. Ohuchi and F. Masuoka, "A Quick Boosting Charge Pump Circuit for High Density and Low Voltage Flash Memories", in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1997, pp.65-66.

[26] Taehee Cho, Young-Taek Lee, Euncheol Kim, Jinwook Lee, Sunmi Choi, Seungjae Lee, Dong-Hwan Kim, Wook-Kee Han, Young-Ho Lim, Jae-Duk Lee, Jung-Dal Choi, and Kang-Deog Suh, "A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution", in *ISSCC Digest of Technical Papers*, 2001, pp.28-29.

[27] K. Kobayashi, "Storage Media in 2010", in *Nikkei Electronics Technology Summit Dig. Tech. Papaers*, September 2005.

List of research achievement

Full papers (自著論文)

1) K.Takeuchi, T.Tanaka and T.Tazawa, "A multipage cell architecture for high-speed programming multi-level NAND flash memories", *IEEE Journal of Solid-State Circuits*, vol.33, no.8, August 1998, pp.1228-1238. (Chapter 2, 3, 7)
2) K. Takeuchi, S. Satoh, K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, T. Ikehashi, K. Kanda, K. Hosono and K. Sakui, "A source-line programming scheme for low voltage operation NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.35 no.5, May 2000, pp.672-681. (Chapter 2, 4, 7)
3) K.Takeuchi, T.Tanaka and H.Nakamura, "A double-level-Vth select gate array architecture for multi-level NAND flash memories", *IEEE Journal of Solid-State Circuits*, vol.31, no.4, April 1996, pp.602-609. (Chapter 2, 5, 7)
4) K. Takeuchi, S. Satoh, T. Tanaka, K. Imamiya, and K. Sakui, " A negative Vth cell architecture for highly scalable, excellently noise immune and highly reliable NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.34, no.5, May 1999, pp.675-684. (Chapter 2, 5, 7)
5) K. Takeuchi and T. Tanaka, "A dual page programming scheme for high-speed multi-Gb-scale NAND flash memories," *IEEE Journal of Solid-State Circuits*, vol.36 no.5, May 2001, pp.744-751. (Chapter 2, 7)

International conference presentation (国際学会口頭発表)

1) K.Takeuchi, T.Tanaka, and H.Nakamura, "a double-level-Vth select gate array architecture for multilevel NAND flash memories," *Symp. on VLSI Circuits*, 1995, pp. 69-70.
2) K.Takeuchi, T.Tanaka, and T.Tanzawa, "a multipage cell architecture for high-speed programming multilevel NAND flash memories," *Symp. on VLSI Circuits*, 1997, pp. 67-68.
3) K.Takeuchi, T.Tanaka, and T.Tanzawa, "a multipage cell architecture for high-speed

programming multilevel NAND flash memories," *International Workshop on Advanced LSI's*, 1997, pp. 105-110.

4) K.Takeuchi, S.Satoh, T.Tanaka, K.Imamiya, and K.Sakui, "a negative Vth cell architecture for highly scalable, excellently noise-immune, and highly reliable NAND flash memories," *Symp. on VLSI Circuits*, 1998, pp. 234-235.
5) K.Takeuchi, S.Satoh, K.Imamiya, and K.Sakui, "a source-line programming scheme for low voltage operation NAND flash memories," *Symp. on VLSI Circuits*, 1999, pp. 37-38.
6) K.Takeuchi and T.Tanaka, "a dual page programming scheme for high-speed multi-giga-bit-scale NAND flash memories," *Symp. on VLSI Circuits*, 2000, pp.156-157.
7) H.Nakamura, K.Imamiya, T.Himeno, T.Yamamura, T.Ikehashi, K.Takeuchi, K.Kanda, K.Hosono, T.Futatsuyama, K.Kawai, R.Shirota, N.Arai, F.Arai, K.Hatakeyama, H.Hazama, M.Saito, H.Meguro, K.Conley, K.Quader and J.Chen, "a 125mm^2 1Gb NAND flash memory with 10MB/s program throughput," *International Solid-State Circuits Conference (ISSCC)*, 2002, pp.106-107.

Other papers (共著論文)

1) Toru Tanzawa, Tomoharu Tanaka, Ken Takeuchi, Riichiro Shirota, Seeichi Aritome, Hiroshi Watanabe, Gertjan Hemink, Kazuhiro Shimizu, Shinji Sato, Yuji Takeuchi, and Kazunori Ohuchi, "A Compact On-Chip ECC for Low Cost Flash Memories," *Symp. on VLSI Circuits*, 1996, pp. 59-60.
2) Tomoharu Tanaka, Toru Tanzawa, and Ken Takeuchi, "A 3.4-Mbyte/sec Programming 3-Level NAND Flash Memory Saving 40% Die Size per Bit," *Symp. on VLSI Circuits*, 1997, pp. 65-66.
3) Toru Tanzawa, Tomoharu Tanaka, Ken Takeuchi, and Hiroshi Nakamura, "Circuit Technology for a Single-1.8V Flash Memory," *Symp. on VLSI Circuits*, 1997, pp. 63-64.
4) Shinji Satoh, Hiroyuki Hagiwara, Toru Tanzawa, Ken Takeuchi, and Riichiro Shirota, "A Novel Isolation-Scaling Technology for NAND EEPROMs with the Minimized Program Disturbance," *International Electron Devices Meeting (IEDM)*, 1997, pp. 291-294.
5) Toru Tanzawa, Tomoharu Tanaka, Ken Takeuchi, Riichiro Shirota, Seeichi Aritome, Hiroshi Watanabe, Gertjan Hemink, Kazuhiro Shimizu, Shinji Sato, Yuji Takeuchi, and Kazunori Ohuchi, "A Compact On-Chip ECC for Low Cost Flash Memories," *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, 1997, pp. 662-669.
6) Kenichi Imamiya, Yoshihisa Sugiura, Hiroshi Nakamura, Toshihiko Himeno, Ken Takeuchi, Tamio Ikehashi, Kazushige Kanda, Koji Hosono, Riichiro Shirota, Seiichi Aritome, Kazuhiro Shimizu, Kazuo Hatakeyama, and Koji Sakui, "A 130-mm^2, 256-Mbit NAND Flash with Shallow Trench Isolation Technology," *IEEE J. of Solid-State Circuits*,

vol. 34, no. 11, 1999, pp. 1536-1542.

7) Kenichi Imamiya, Yoshihisa Sugiura, Hiroshi Nakamura, Toshihiko Himeno, Ken Takeuchi, Tamio Ikehashi, Kazushige Kanda, Koji Hosono, Riichiro Shirota, Seiichi Aritome, Kazuhiro Shimizu, Kazuo Hatakeyama, and Koji Sakui, "A 130-mm^2, 256-Mbit NAND Flash with Shallow Trench Isolation Technology," *International Solid-State Circuits Conference (ISSCC)*, 1999, pp. 112-113.
8) Shinji Satoh, Takuya Nakamura, Kazuhiro Shimizu, Ken Takeuchi, Hiroshi Iizuka, Seiichi Aritome, and Riichiro Shirota, "A Novel Gate-Offset NAND Cell (GOC-NAND) Technology Suitable for High-Density and Low-Voltage-Operation Flash Memories," *International Electron Devices Meeting (IEDM)*, 1999, pp. 271-274.
9) Kenichi Imamiya, Hiroshi Nakamura, Toshihiko Himeno, Toshio Yamamura, Tamio Ikehashi, Ken Takeuchi, Kazushige Kanda, Koji Hosono, Takuya Futatsuyama, Koichi Kawai, Riichiro Shirota, Norihisa Arai, Fumitaka Arai, Kazuo Hatakeyama, Hiroaki Hazama, Masanobu Saito, Hisataka Meguro, Kevin Conley, Khandker Quader and Jian J. Chen, "A 125-mm^2 1-Gb NAND Flash Memory with 10MByte/sec Program Speed," *IEEE J. of Solid-State Circuits*, vol. 37, no. 11, 2002, pp. 1493-1501.
10) Ken Takeuchi, "Future Semiconductor Technologies shown in the 1999 Symposium on VLSI Circuits", *Nikkei Microdevices*, June 1999.
11) Ken Takeuchi, "Future Semiconductor Technologies shown in the 2000 Symposium on VLSI Circuits", *Nikkei Microdevices*, June 2000

United States patents (米国登録特許)

1) Ken Takeuchi, Koji Sakui, Tomoharu Tanaka, and Seiichi Aritome, "Nonvolatile semiconductor memory device," U.S.P. 5,680,347, October 21, 1997.
2) Seiichi Aritome, Tomoharu Tanaka, and Ken Takeuchi, "Nonvolatile semiconductor memory device," U.S.P. 5,698,879, December 16, 1997.
3) Toru Tanzawa, Tomoharu Tanaka, and Ken Takeuchi, "Semiconductor memory device and high-voltage switching circuit," U.S.P. 5,708,606, January 13, 1998.
4) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device," U.S.P. 5,781,478, July 14, 1998.
5) Toru Tanzawa, Tomoharu Tanaka, and Ken Takeuchi, "Semiconductor memory device and high-voltage switching circuit," U.S.P. 5,828,621, October 27, 1998.
6) Ken Takeuchi and Tomoharu Tanaka, "Memory system," U.S.P. 5,844,841, December 1, 1998.
7) Toru Tanzawa, Tomoharu Tanaka, and Ken Takeuchi, "Nonvolatile semiconductor memory with temperature compensation for read/verify referencing scheme," U.S.P.

5,864,504, January 26, 1999.

8) Ken Takeuchi and Tomoharu Tanaka, "Semiconductor device and memory system," U.S.P. 5,903,495, May 11, 1999.
9) Toru Tanzawa, Ken Takeuchi, and Tomoharu Tanaka, "Semiconductor memory," U.S.P. 5,905,691, May 18, 1999.
10) Toru Tanzawa, Tomoharu Tanaka, and Ken Takeuchi, "Semiconductor memory device and high-voltage switching circuit," U.S.P. 5,909,398, June 1, 1999.
11) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device," U.S.P. 5,920,507, July 6, 1999.
12) Ken Takeuchi, Koji Sakui, Tomoharu Tanaka, and Seiichi Aritome, "Nonvolatile semiconductor memory device," U.S.P. 5,940,321, August 17, 1999.
13) Tomoharu Tanaka, Kazunori Ohuchi, Toru Tanzawa, and Ken Takeuchi, "Nonvolatile semiconductor memory device," U.S.P. 5,969,985, October 19, 1999.
14) Ken Takeuchi and Tomoharu Tanaka, "Semiconductor memory device having variable number of selected cell pages and subcell arrays," U.S.P. 5,986,933, November 16, 1999.
15) Ken Takeuchi, Tomoharu Tanaka, and Hiroshi Nakamura, "Nonvolatile semiconductor memory device using a bit line potential raised by use of a coupling capacitor between bit lines," U.S.P. 6,005,802, December 21, 1999.
16) Tomoharu Tanaka and Ken Takeuchi, "Multi-level memory for verifying programming results," U.S.P. 6,028,792, February 22, 2000.
17) Tomoharu Tanaka, Kazunori Ohuchi, Toru Tanzawa, and Ken Takeuchi, "Nonvolatile semiconductor memory device," U.S.P. 6,044,013, March 28, 2000.
18) Ken Takeuchi and Tomoharu Tanaka, "Semiconductor device and memory system," U.S.P. 6,046,935, April 4, 2000.
19) Ken Takeuchi, Koji Sakui, Tomoharu Tanaka, and Seiichi Aritome, "Nonvolatile semiconductor memory device," U.S.P. 6,046,940, April 4, 2000.
20) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device having a data circuit for erasing and writing operations," U.S.P. 6,055,188, April 25, 2000.
21) Ken Takeuchi and Tomoharu Tanaka, "Memory system," U.S.P. 6,064,591, May16, 2000.
22) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory," U.S.P. 6,069,823, May 30, 2000.
23) Tomoharu Tanaka, Hiroshi Nakamura, Ken Takeuchi, Riichiro Shirota, Fumitaka Arai, Susumu Fujimura, "Nonvolatile semiconductor memory device with soft-programming to adjust erased state of memory cells," U.S.P. 6,134,140, Oct 17, 2000.
24) Ken Takeuchi, "Nonvolatile semiconductor memory device capable of preventing data from being written in error," U.S.P. 6,134,157, Oct 17, 2000.

25) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device," U.S.P. 6,147,911, Nov 14, 2000.
26) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device," U.S.P. 6,154,391, November 28, 2000.
27) Tomoharu Tanaka, Hiroshi Nakamura, Ken Takeuchi, Riichiro Shirota, Fumitaka Arai, Susumu Fujimura, "Nonvolatile semiconductor memory device with soft-programming to adjust erased state of memory cells," U.S.P. 6,208,560, Mar 27, 2001.
28) Hiroshi Nakamura, Ken Takeuchi, Hideko Oodaira, Kenichi Imamiya, Kazuhito Narita, Kazuhiro Shimizu and Seiichi Aritome, "Semiconductor memory device capable of realizing a chip with high operation reliability and high yield," U.S.P. 6,240,012, May 29, 2001.
29) Koji Hosono, Hiroshi Nakamura, Tamio Ikehashi, Kazushige Kanda, Ken Takeuchi, Kenichi Imamiya, "Booster circuit having booster cell sections connected in parallel, voltage generating circuit and semiconductor memory which use such booster circuit," U.S.P. 6,278,639, August 21, 2001.
30) Tomoharu Tanaka, Kazunori Ohuchi, Toru Tanzawa, and Ken Takeuchi, "Nonvolatile semiconductor memory device," U.S.P. 6,282,117, August 28, 2001.
31) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device," U.S.P. 6,301,153, Oct 9, 2001.
32) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory device," U.S.P. 6,307,785, Oct 23, 2001.
33) Tamio Ikehashi, Yoshihisa Sugiura, Kenichi Imamiya, Ken Takeuchi and Yoshihisa Iwata, "Semiconductor integrated circuit having active mode and standby mode converters," U.S.P. 6,351,179, Feb 26, 2002.
34) Hiroshi Watanabe, Hiroshi Nakamura, Kazuhiro Shimizu, Seiichi Aritome, Toshitake Yaegashi, Yuji Takeuchi, Kenichi Imamiya, Ken Takeuchi and Hideko Oodaira, "Nonvolatile semiconductor memory," U.S.P. 6,353,242, Mar 5, 2002.
35) Tomoharu Tanaka, Kazunori Ohuchi, Toru Tanzawa, and Ken Takeuchi, "Nonvolatile semiconductor memory device," U.S.P. 6,363,010, Mar 26, 2002.
36) Ken Takeuchi, Tomoharu Tanaka and Noboru Shibata, "Nonvolatile semiconductor memory having plural data storage portions for a bit line connected to memory cells," U.S.P. 6,374,746, April 16, 2002.
37) Koji Hosono, Yasuo Itoh and Ken Takeuchi, "Internal voltage generating circuit capable of generating variable multi-level voltages," U.S.P. 6,404,274, June 11, 2002.
38) Hiroshi Nakamura, Ken Takeuchi, Hideko Oodaira, Kenichi Imamiya, Kazuhiro Narita, Kazuhiro Shimizu and Seiichi Aritome, "Semiconductor memory device capable of realizing a chip with high operation reliability and high yield," U.S.P. 6,424,588, July 23, 2002.
39) Tomoharu Tanaka, Hiroshi Nakamura, Ken Takeuchi, Riichiro Shirota, Fumitaka Arai,

and Susumu Fujimura, "Nonvolatile semiconductor memory device," U.S.P. 6,434,055, August 13, 2002.

40) Ken Takeuchi and Tomoharu Tanaka, "Voltage generator for compensating for temperature dependency of memory cell current", U.S.P. 6,452,437, September 17, 2002.

41) Kazushige Kanda, Tamio Ikehashi, Ken Takeuchi and Kenichi Imamiya, "Semiconductor integrated circuit", U.S.P. 6,469,573, October 22, 2002.

42) Koji Hosono, Tamio Ikehashi, Tomoharu Tanaka, Kenichi Imamiya, Hiroshi Nakamura and Ken Takeuchi , "Fail number detecting circuit of flash memory", U.S.P. 6,507,518, January 14, 2003.

43) Hiroshi Watanabe, Hiroshi Nakamura, Kazuhiro Shimizu, Seiichi Aritome, Toshitake Yaegashi, Yuji Takeuchi, Kenichi Imamiya, Ken Takeuchi and Hideko Oodaira, "Nonvolatile semiconductor memory", U.S.P. 6,512,253, January 28, 2003.

44) Tomoharu Tanaka, Kazuhiro Ohuchi, Toru Tanzawa and Ken Takeuchi, "Nonvolatile semiconductor memory device", U.S.P. 6,545,909, April 8, 2003.

45) Tomoharu Tanaka, Hiroshi Nakamura, Ken Takeuchi, Riichiro Shirota, Fumitaka Arai and Susumu Fujimura, "Nonvolatile semiconductor memory device", U.S.P. 6,549,464, April 15, 2003.

46) Tamio Ikehashi, Yoshihisa Sugiura, Kenichi Imamiya, Ken Takeuchi and Yoshihisa Sugiura, "Semiconductor integrated circuit with a down converter for generating an internal voltage" U.S.P. 6,590,444, July 08, 2003.

47) Hiroshi Nakamura, Ken Takeuchi, Hideko Oodaira, Kenichi Imamiya, Kazuhito Narita, Kazuhiro Shimizu and Seiichi Aritome, "Semiconductor memory device capable of realizing a chip with high operation reliability and high yield", U.S.P. 6,611,447, August 26, 2003.

48) Tamio Ikehashi, Ken Takeuchi and Toshihiko Himeno, "Semiconductor memory device with test mode", U.S.P. 6,643,180, November 4, 2003.

49) Ken Takeuchi, Tamio Ikehashi and Toshihiko Himeno, "Non-volatile semiconductor memory", U.S.P. 6,646,930, November 11, 2003.

50) Koji Hosono, Tamio Ikehashi, Tomoharu Tanaka, Kenichi Imamiya, Hiroshi Nakamura and Ken Takeuchi, "Fail number detecting circuit of flash memory", U.S.P. 6,657,896, December 2, 2003.

51) Ken Takeuchi and Tomoharu Tanaka, "Multi-level non-volatile semiconductor memory device with verify voltages having a smart temperature coefficient", U.S.P. 6,667,904, December 23, 2003.

52) Kazushige Kanda, Tamio Ikehashi, Ken Takeuchi and Kenichi Imamiya, "Semiconductor integrated circuit", U.S.P. 6,674,318, January 6, 2004.

53) Hiroshi Nakamura, Kenichi Imamiya and Ken Takeuchi, "Semiconductor memory device having a plurality of chips and capability of outputting a busy signal", U.S.P.

6,680,858, January 20, 2004.

54) Tomoharu Tanaka, Hiroshi Nakamura, Ken Takeuchi, Riichiro Shirota, Fumitaka Arai and Susumu Fujimura, "Nonvolatile semiconductor memory", U.S.P. 6,798,698, September 28, 2004.

55) Tamio Ikehashi, Yoshihisa Sugiura, Kenichi Imamiya, Ken Takeuchi and Yoshihisa Iwata, "Semiconductor integrated circuit", U.S.P. 6,801,060, October 5, 2004.

56) Tamio Ikehashi, Ken Takeuchi and Toshihiko Himeno, "Semiconductor memory device with test mode", U.S.P. 6,819,596, November 16, 2004.

57) Hiroshi Nakamura, Ken Takeuchi, Hideko Oodaira, Kenichi Imamiya, Kazuhito Narita, Kazuhiro Shimizu and Seiichi Aritome, "Semiconductor memory device capable of realizing a chip with high operation reliability and high yield", U.S.P. 6,836,444, December 28, 2004.

58) Koji Hosono, Tamio Ikehashi, Tomoharu Tanaka, Kenichi Imamiya, Hiroshi Nakamura and Ken Takeuchi, "Fail number detecting circuit of flash memory", U.S.P. 6,859,401, February 22, 2005.

59) Koji Hosono, Hiroshi Nakamura, Ken Takeuchi and Kenichi Imamiya, "Non-volatile semiconductor memory", U.S.P. 6,937,510, August 30, 2005.

60) Tomoharu Tanaka, Hiroshi Nakamura, Ken Takeuchi, Riichiro Shirota, Fumitaka Arai and Susumu Fujimura, "Non-volatile semiconductor memory", U.S.P. 6,940,752, September 6, 2005.

Japan patents (日本登録特許)

1) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory", J.P. 3,172,086, March 23, 2001.

2) Tomoharu Tanaka, Toru Tanzawa and Ken Takeuchi, "Semiconductor memory", J.P. 3,176,011, April 6, 2001.

3) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory", J.P. 3, 200,006, June 15, 2001.

4) Ken Takeuchi and Tomoharu Tanaka, "Memory system", J.P. 3, 200,012, June 15, 2001.

5) Ken Takeuchi and Tomoharu Tanaka, "Semiconductor memory and memory system", J.P. 3,210,259, July 13, 2001.

6) Seiichi Aritome, Tomoharu Tanaka and Ken Takeuchi, "Nonvolatile semiconductor memory", J.P. 3, 238,576, October 5, 2001.

7) Toru Tanzawa, Tomoharu Tanaka and Ken Takeuchi, "Semiconductor memory", J.P. 3,294,153, April 5, 2002.

8) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory", J.P. 3, 400,214, February 21, 2003.
9) Tomoharu Tanaka and Ken Takeuchi, "Multi-level memory", J.P. 3,409,986, March 20, 2003.
10) Ken Takeuchi, Tomoharu Tanaka, and Hiroshi Nakamura, "Nonvolatile semiconductor memory", J.P. 3, 425,340, May 2, 2003.
11) Ken Takeuchi, Tomoharu Tanaka, Seiichi Aritome, and Koji Sakui, "Nonvolatile semiconductor memory", J.P. 3, 532,659, March 12, 2004.
12) Tomoharu Tanaka, Toru Tanzawa, and Ken Takeuchi, "Nonvolatile semiconductor memory", J.P. 3,563,702, June 11, 2005.
13) Ken Takeuchi and Tomoharu Tanaka, "Semiconductor memory", J.P. 3,576,763, July 16, 2004.
14) Ken Takeuchi, Koji Sakui and Kazunori Ohuchi, "Semiconductor memory", J.P. 3,581,170, July 30, 2004.
15) Ken Takeuchi and Tomoharu Tanaka, "Semiconductor memory", J.P. 3,590,270, August 27, 2004.
16) Ken Takeuchi and Tomoharu Tanaka, "Nonvolatile semiconductor memory", J.P. 3,592,887, September 3, 2004.
17) Ken Takeuchi and Koji Hosono, "Nonvolatile semiconductor memory", J.P. 3,595,691, September 10, 2004.
18) Tamio Ikehashi, Kazushige Kanda, Yoshihisa Iwata, Hiroshi Nakamura, Ken Takeuchi, and Koji Hosono, "Nonvolatile semiconductor memory", J.P. 3,595,691, September 24, 2004.
19) Ken Takeuchi, "Nonvolatile semiconductor memory", J.P. 3,615,041, November 12, 2004.
20) Ken Takeuchi, Yuji Takeuchi, and Kenichi Imamiya, "Nonvolatile semiconductor memory", J.P. 3,615,046, November 12, 2004
21) Ken Takeuchi and Tamio Ikehashi, "Nonvolatile semiconductor memory", J.P. 3,624,098, December 3, 2004.
22) Hiroshi Nakamura, Koji Hosono, Kazushige Kanda, and Ken Takeuchi, "Semiconductor memory", J.P. 3,624,100, December 3, 2004.
23) Ken Takeuchi, Hiroshi Nakamura, and Tomoharu Tanaka, "Semiconductor memory", J.P. 3,637,211, January 14, 2005.
24) Toru Tanzawa, Ken Takeuchi, and Tomoharu Tanaka, "Nonvolatile semiconductor memory", J.P. 3,648,304, February 18, 2005.