Study on Noise Immunity of Low-Power Static CMOS Digital Design

（低電力スタティック CMOS デジタル設計における
ノイズ耐性に関する研究）

A Dissertation
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Summary

In the past, noise was not such a big issue in digital integrated circuits. However, the continuous progress in semiconductor technology put the noise issue among the major concerns of digital CMOS IC designers. This study concerns with the noise immunity of static CMOS low power digital design by investigating the noise immunity of the current low power static CMOS design schemes and presenting a fast and accurate methodology to evaluate the noise sensitivity of the different nodes in a design during the design phase. In addition, for the modeling/characterization of noise in digital circuits, techniques to measure the non-periodic noise and sensing the peak minimum/maximum fluctuation on-chip have been presented. The study is presented in five chapters in addition to conclusion.

The first chapter includes a background about the power consumption and noise issues in current and future VLSI/ULSI digital design. It also includes the objectives of the study and thesis organization.

In chapter two, we present the effect of noise on the performance of a selected group of low power as well as traditional digital design techniques. First, we present a model for the different noise sources in the digital circuits. Then we applied the model to a selected group of low power and traditional designs as testing circuits. The noise immunity of the tested schemes has been reported in terms of logic error and delay error. At the end of the chapter, we present a methodology for leakage power saving and at the same time it has high noise immunity. One of the ways to increase the noise immunity of a digital circuit is to give special strengthen considerations to the soft (weak) parts (nodes) against

noise. Since it is time consuming to analyze the noise-sensitivity of different nodes in a big design using transistor level simulators, an analytical (fast and accurate) method is required.

In chapter three, we present a methodology to evaluate the noise-induced logic error probability in a given CMOS digital design in terms of supply voltage, threshold voltage, noise level and circuit configuration. At first, we modeled the noise immunity of the different logic gates in terms logic error probability including the effect of supply and threshold voltage, which is called electrical masking. Then, time masking has been modeled to include the variation of the spurious pulse width and generation time in the overall logic error probability. Moreover, the logic masking effect has been also considered. The electrical, timing and logic masking have been combined to form the overall logic error probability model. The model has been used to evaluate the logic error probability caused by the noise at the different nodes in digital circuit examples. The model results have been compared with results obtained from HSPICE simulation. The results reveal that the model fit with the expected simulation results achieving speedup factor of more than 1000 over HSPICE. Moreover, the calculation time of the methodology is linearly proportional with the number of gates in a design, and hence, the method is suitable for investigating the noise immunity of the big circuits. The model can be used to identify the weak parts against the noise in a given design during the design phase and hence it helps the designer in giving specific design considerations to strengthen the weak nodes. The methodology is based on hypothetical noise distribution. So that, for more accurate results, a real noise distribution should be provided.

In chapter four we, at first, present an overview on the previous works regarding the on-chip noise measurement. To avoid the problems attached with the previous designs, an on-chip noise detector has been designed and fabricated using 0.18μm technology. The detector has the capability to detect the single-event or

the non-periodic signals within a measurement time window. It is equipped with a programmable voltage divider to be able to detect high-swing signals having maximum theoretical frequency of 5GHz. The bandwidth of the output signal can be controlled by the user to fit the monitoring tools capability off-chip and to avoid the effects of the on-chip parasitic elements, therefore conventional equipments can be used to measure the signal off-chip. Moreover, the detector is synthesizable and the designer can flexibly adjust its main parameters. A test chip is fabricated and tested successfully. The detector's design has been modified to increase the sampling rate. Upon the simulation results, the modified version is capable to measure signals of frequency (theoretically) up to 10GHz.

Chapter five includes the description of a CPU-interfaced system to monitor the minimum/maximum fluctuation in both V_{DD} and ground in a design. In addition to the magnitude information, the system has the ability to report the timing and spatial information of the spurious pulse. The system is designed using Rohm 0.18μm technology. The fluctuation is detected by comparing the voltage of node-under-test with a reference voltage supplied form off-chip, and the fluctuation information is send off-chip in digital format. The detector is simple, therefore, it can be replicated within a design to detect the fluctuations on VDD/Ground net at different spots and hence, safe operation can be guaranteed. The detector is interfaced by a CPU; therefore it is suitable for future VLSI/ULSI circuits.

Finally, we conclude the study in chapter six.

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Chapter 1

Introduction

1.1 Background

Integration density and performance of integrated circuits have gone through an astounding revolution in the last couple of decades. In 1960s, Gordon Moore predicated that the number of transistors that can be integrated on a single die would grow exponentially with time. This prediction, later called Moore's law, has proven to be amazingly visionary. Its validity is best illustrated with the aid of figure 1.1 [1], which plots the transistor count per chip as a function of time. As it can be observed that integration complexity doubles approximately every one to two years. As a result, the number of transistors in a MPU chip has increased by more than a hundred thousands times since 1970. The continuous progress in semiconductor technology has enabled scaling down the transistor and interconnects' sizes and pitches, which effectively increase the integration density. As it expected by the International Technology Roadmap for Semiconductor (ITRS) [2], the transistor channel length will continue scale down to 25 nano-meters and below as it is shown by figure 1.2. Thanks to technology scaling, it has enabled increasing the speed of digital system considerably. As a result to technology scaling, the speed of digital systems is also increasing almost exponentially as it will be shown the next section. The CMOS digital circuits had been known as low-power high-noise immunity circuits. However, it is not the case in the era of deep submicron (nano-scale) technology. In the following subsection, the consequences of technology scaling on power consumption and noise immunity of VLSI are explained.

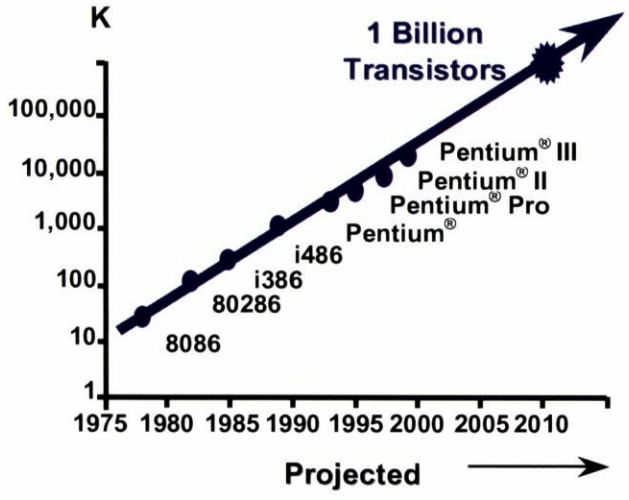

Figure 1.1 CPU transistor count trend [1].

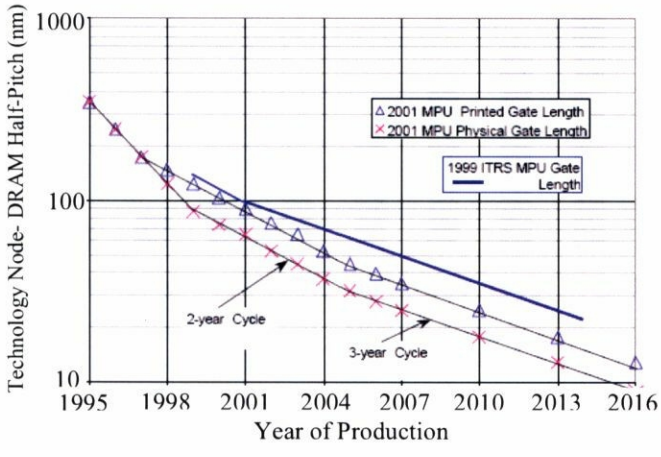

Figure 1.2 Future trend of gate length [2].

1.2 Power and Reliability Issues in Future LSI Design

The continuous increase in integration density of VLSI circuits and the demand of higher circuit speed resulted in higher power consumption in ICs. Before 1990's, power dissipation in LSI systems had less concern than after that.

The main emphasis was on performance and miniaturization. The battery-powered applications, such as pocket computers, portable communication devices, pacemakers, hearing aids and wrist watches, drove low-power electronics, wherein, the battery life, in such applications, is very important for convenient usage of them. And currently, the exploding market of portable electronic appliances, (for instance, the plot in figure 1.3 shows the evolution of the world-wide market for mobile phones [3]) power consumption has become one of the most important factors in the continued development of microelectronic technology. The reasons for that can be explained as follows:

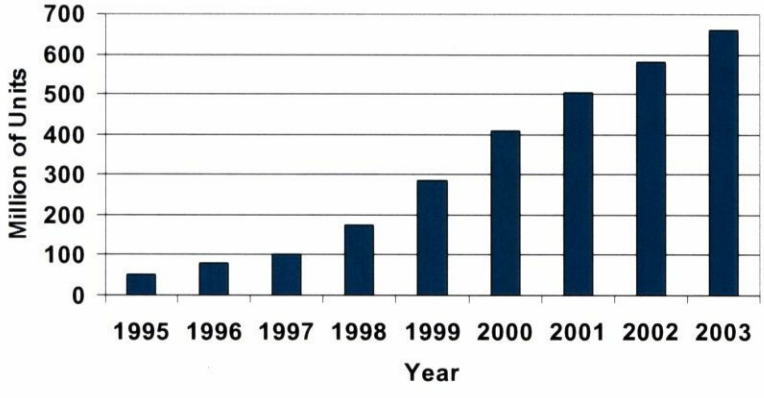

Figure 1.3 Global market for cellular phones [3].

First: There is a continuous demand for improving the circuit performance and integrating more functions into a chip, therefore, the feature size has to continue shrink. In consequence, the magnitude of power per unit area is increasing. Although the feature size miniaturization is accompanied with scaling down the supply voltage -to keep the device reliability- the power dissipation consumption does not come down. Moreover, the current drown from the power

unit is rapidly increasing. Figure 1.4 shows the trend of current and power dissipation in CPUs [2]. It is clear that some MPUs consume power higher than 100W. i.e. more than light bulb, and it continues increase as indicated by figure 1.4. High power consumption in ICs has many consequences on its performance and applications. From the technical point of view, the consumed electrical power is transformed into thermal power. As a result, the chip temperature increases, which may be tends to electro-migration problem or degrade the reliability of MOS gate oxide in addition to causing instable system operation. Economically, to sink the generated heat, an expensive packing material is needed to help the heat sinking process, which means higher packing cost and finally increase the total product cost. Moreover, using cooling fan is impractical in some cases, such as speech applications, that is, it adds acoustic noise to the system.

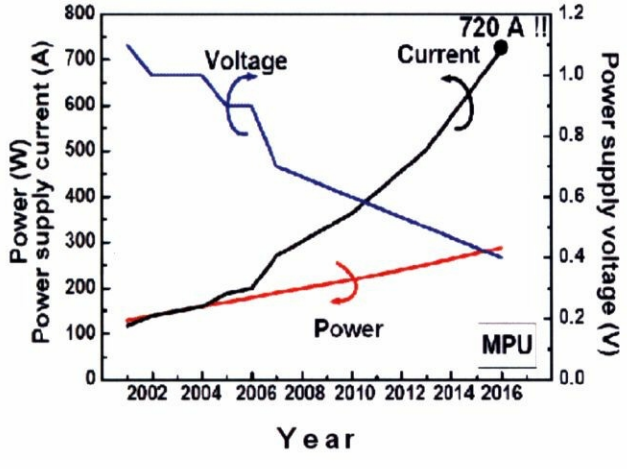

Figure 1.4 CPU power supply voltage and current trend [2].

Second: Hand-held (battery-powered) devices of the past were characterized by low-computational requirements. However, the current and future portable application, in particular, laptops, cell phones and games devices, require higher

power consumption for the impeded high computation capabilities. People are expecting to have access to some computing power, information resources and communication abilities when they are in travel as they do when they are at their desks [4].

Third: As energy costs rise, designing for low power will save, to some extent, the global need for energy sources.

For all the above reasons, decreasing the power consumption in LSI systems has been being one of the major concerns of VLSI designers. Hence, design for low power has been studied extensively in the past two decades [4-7]. In the next chapter, more focus on the different low power design techniques is given.

In fact, power consumption in LSI circuit is not the only concern for the designers in the current and future design. The continuous progress and scaling of semiconductor technology as well as the demand for higher speed systems has brought the noise immunity issue among the major concerns of VLSI designers. The speed of VLSI system is increasing, for instance, figure 1.5 shows how the clock frequency of MPU is increasing almost twenty times every decade [8].

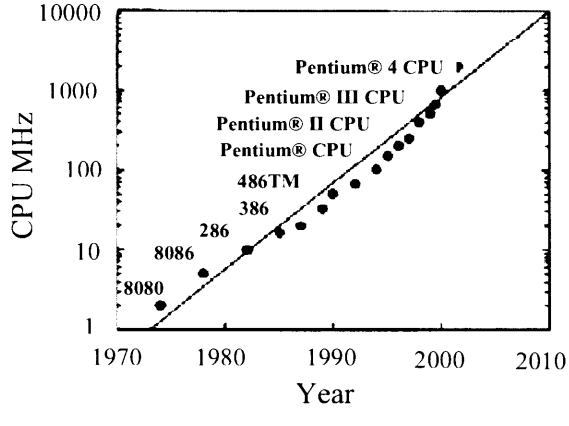

Figure 1.5 CPU speed (MHz) trend [8].

At the same time, the continuous scaling of MOS feature size entails scaling of the supply voltage, mainly for two reasons; the first is to be suitable for such short channel transistor, otherwise, the high electric field could destroy the MOS and hence a vital reliability problem would happen, the second is to decrease the power consumption. An hence, the threshold voltage has to also be scaled down to keep the circuit speed. In consequence, the noise margin of digital circuit is considerably decreased. Furthermore, in the scaled technology, interconnects have become more condensed and closer. The previously isolated neighbored lines are no longer isolated. The coupling capacitance and inductance between the closely routed and stacked lines are increasing with the technology progress. As a result, when a signal on a line changes high to low or (low to high) a glitch(s) on the neighbor(s) is (are) generated due to the coupling effect. The glitch might propagate to the register element at the primary output causing functional problem. The higher integration density, lower supply and threshold voltages and using a higher frequency and steeper clock signal have made the digital circuits more susceptible to noise where it was not before [9-12]. The instantaneous large current variation due to large number of simultaneously switching circuits has added un-ignorable fluctuation to both supply and ground nets in addition to decreasing the effective supply value feeding the circuit [13]. The closely routed signal line has increased their coupling capacitance and hence the crosstalk effect should be carefully considered. The power supply/ground fluctuations and inductive/capacitive crosstalk in addition to the external noise sources including and electromagnetic interference and noise induced by alpha particle, can cause sever problems to the system performance and/or reliability. These problems can be ranged from decreasing the system throughput [14-19] to causing glitches on wires, which can result in function failure. The noise effects on the performance and reliability of IC have been, mainly, studied individually and most of them concentrate on the delay error caused by specific noise source. The works, which focus on the noise induced logic error, mainly consider the soft-error as a noise

source [20-23]. The deleterious effects of noise in digital circuit make it imperative to consider the noise immunity as a first class design constraint. Despite the extensive researches on individual noise sources, a few researches have been tried to develop a technique for combined noise sources. That is, the different noise sources tend to aggravate one another's effects [23].

From the above discussion, it is clear that the current LSI designer should consider both the low power consumption and high reliability simultaneously for better system usability and performance.

1.3 Objectives and Thesis Organization

The discussion presented in the above two sections indicates the importance of taking the power-consumption and noise-immunity as two important design constraints into account during the design phase of VLSI circuits. At first glance, it seems that there is a contradiction between designing for low power and high noise immunity. Furthermore, the effects of different kinds of noise sources on the performance of static CMOS low power digital design schemes were not studied completely so far. So that the study has been run to achieve the following objectives:

The first objective of this research is to investigate the effect of noise on performance of the most famous low power digital design schemes in terms of logic error and delay error, and hence, for the designer, who has multiple choices of low-power design schemes, the best technique from the noise immunity point of view is presented. The comparison is done based on transistor level simulation.

The second objective is to present a fast and accurate methodology to evaluate the noise-immunity of a CMOS digital system taking into account the important factors, which determine the system's power consumption. The methodology should have the ability to identify the noise-sensitive nodes in a

given design and hence the designer would give special considerations for these nodes during the design phase.

The third objective of the study is to present a technique to measure the noise in a design, which will help in characterizing the reliability and performance of the fabricated systems, at the same time, the results can be used as a feedback for enhancing the design of the subsequent systems.

The thesis is organized as follows:

Chapter 2 starts by a revision for the different static CMOS low-power design schemes. The schemes have been classified into three main categories. Then, the noise sources in digital design have been summarized. A model representing the different noise sources has been presented. The model has been applied to a group of testing circuits, which are designed using four different low-power design methodologies in addition to the conventional design techniques, to investigate the relative noise-immunity of each technique. The comparison has been done in terms of logic and delay error as will as the power consumption by each technique.

In chapter 3, a calculation methodology to evaluate the noise-immunity of a given system is presented. Based on the noise model presented in chapter two, the logic error probability, due to different noise sources in a static CMOS digital system has been calculated. The accuracy of the methodology has been tested by comparing its results with those obtained form HSPICE.

Chapter 4 includes the description of an on-chip non-periodic high-swing noise (signal) detector. The chapter includes detector details, simulation and measurement results.

In chapter 5, an on-chip minimum/maximum fluctuation detector has been presented. The block diagram, theory of operation and simulation results discussed. The, the study is concluded in chapter 6.

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