Chapter 2

Noise Immunity Investigation of Low Power Schemes

2.1 Introduction

In the past, noise was not such a big issue in digital integrated circuits. However, the continuous progress in semiconductor technology put the noise issue among the major concerns of digital CMOS IC designers. With the modern technology trend, the complexity of integrated circuits is approaching one billion transistors as described by ITRS [1]. Recently, interconnects have a smaller width/depth aspect ratio and are more condensed resulting in increases in their resistance, parasitic capacitance and inductance [2]. Moreover, the transistor size is scaled down to 65nm and below, which entails decreasing the supply voltage for the sake of device reliability. In consequence, the device threshold voltage is also scaled down in order to not lose circuit performance. One more feature of the modern digital CMOS IC is that the clock frequency has become higher and steeper, which means that the rate of current change (di/dt) due to the switching process has also become higher. The high di/dt has increased the effect of parasitic inductance of the bonding wire and internal power/ground net, which added an effective noise source to the digital circuits. Furthermore, parametric variations due to technology, temperature variation as well as electromagnetic interference could be a serious noise source for future digital design.

For all these reasons, the modern digital circuits became more sensitive to noise and the signal integrity became a crucial problem in modern CMOS digital integrated circuits design.

On the other hand, power consumption is also an important metric in modern digital CMOS circuits. The rapidly increasing use of battery powered equipment, the desire to decrease the heat generated inside the die for the sake of interconnects' reliability and better circuit performance, as well as for lower cost packaging and cooling systems, are the driving forces behind the invention of many low power CMOS design schemes [3-4].

At first glance, it seems that there is a contradiction between designing for low power and high noise immunity. Furthermore, the effects of different kinds of noise sources on the performance of static CMOS low power digital design schemes were not studied completely so far. So that, in this chapter, the effects of noise on performance of the most famous low power digital design schemes in terms of logic error and delay error have been investigated. In addition to identifying the robust low power design scheme, the results clearly demonstrate that the low power design could also have high noise immunity compared with traditional design.

2.2 Overview on Low Power Design Methodologies

The low power electronics was driven by the battery-powered applications such as pocket calculator, hearing aids, implantable pacemakers, portable military equipments used by the individual soldier and, most importantly, wrist watches. In such applications it is important to prolong the battery life as much as possible. Currently, with the growing trends toward portable computing and wireless communications, power dissipation has become one of the most critical factors for the development of microelectronic technology and hence many schemes have been presented to minimize the power consumption in LSI digital design. Before

giving details about the schemes used for evaluation, it is worth to summarize the sources of power consumption in digital integrated circuits.

2.2.1 Sources of Power Dissipation in Digital Circuits

In CMOS digital circuits, power dissipation consists of dynamic and static components. Taking the inverter gate as a representative for the static CMOS logic gates, the elements of power consumption are indicated in figure 2.1 and the total power consumption can be given by equation 2.1 [4].

$$P_{total} = \alpha_t C_L V V_{DD} f_{clk} + I_{sc} V_{DD} + I_{Leakage} V_{DD} \qquad (2.1)$$

The first component represent the switching component of power consumption where C_L is the loading capacitance, f_{clk} is the clock frequency and α_t is the probability that a power consuming transition occurs (the activity factor). In most cases the voltage swing voltage V is the same as the supply voltage V_{DD}. The second term is due to the direct path short circuit current I_{sc}, which flows when both NMOS and PMOS transistors are simultaneously turned on. The conducting current passes directly form supply voltage to ground. It should be noted that I_{sc} represents the average value of the short circuit current, which passes only during a short time of switching process. So in other researches it may be expressed as $\alpha_t I_{sc}$. The first and second components are the elements of dynamic power consumption. Finally, the last power dissipation component is due to the leakage current which composed of many sub-components as shown in figure 2.1-b. The leakage current components can be described as follows [6]. PN reverse bias junction leakage is due to the minority carrier drift near the edge of the depletion region and the electron-hole pair generation in the depletion region. It is very small and can be ignored. However, when the electric field across a reverse-biased p-n junction approaches 10^6V/cm, significant current flow can occur due to band-to-band tunneling. The sub-threshold leakage is the weak inversion current

between source and drain of MOS transistor when the gate voltage is less than the threshold voltage. It increases exponentially with the reduction of the threshold voltage, making it critical for low voltage low power CMOS circuit design. The short channel effect, such as V_{th} roll-off and drain-induced-barrier lowering, make the sub-threshold leakage even worse. Gate induced drain leakage occurs at negative V_G and high V_D. It is due to the high electric field under the gate and drain overlap region, which results in the band-to-band tunneling. Punch-through occurs when the drain voltage is high and the drain and source depletion regions approach each other. In the punch-through condition, the gate totally loses the control of the channel current and the sub-threshold slope starts to degrade. Gate Oxide Tunneling, which is due to the high electric field in the gate oxide. Gate oxide tunneling current became important especially for sub 100nm technology when the oxide thickness is less than 2nm.

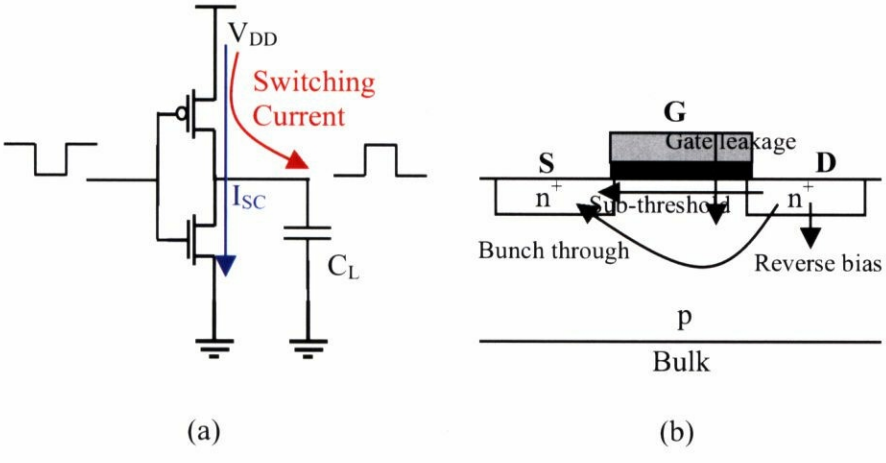


Figure 2.1 Components of power consumption in static CMOS logic gate
(a) Dynamic power components (b) Static power components.

The power consumption equation indicates that the switching power is approximately proportional to the square of supply voltage and both short circuit

and static power is proportional to V_{DD}. This implies that the supply voltage the most effective parameter in the power consumed in an integrated circuit. Since dynamic power is proportional to the square value of the supply voltage (V_{DD}) and static power also has positive dependence on V_{DD}, lowering the supply voltage is the most effective way to reduce the power consumption. With the scaling of supply voltage, transistor threshold voltage V_{th} is also scaled in order to satisfy the performance requirements. Unfortunately, such scaling leads to an increase in leakage current, which becomes an important concern in low-voltage high-performance circuit designs. The circuit topology plays an important rule as well. That is, the number of fan out identifies the value of load capacitance C_L. Also using chain or tree connection affect the number of spurious transitions consequently the switching power will be affected. In the following subsection, the different methodologies used for power saving are summarized.

2.2.2 Supply Voltage Based Schemes

Since dynamic power is approximately proportional to the square of supply voltage and static power is proportional to V_{DD}, reducing supply voltage is obviously the most effective way to reduce the power consumption. Furthermore, the electric field can be reduced and the high field effects can be suppressed, which is beneficial for device reliability. Supply voltage reduction is simple and direct task but it has detrimental effects on the performance of the circuit. That is the propagation delay (t_{pd}) is related to V_{th} and supply voltage V_{DD} by equation 2.2 [7]. Where k is the proportionality factor. On the other hand, digital circuits are characterized by the variety of delay paths, which means that there are some paths whose propagation delay are longer than some others. Exploiting this feature enables using the idea of feeding digital circuits with more than one supply voltage value.

$$t_{pd} = \frac{kQ}{I} = \frac{kC_L V_{DD}}{(V_{DD} - V_{th})^{1.3}} \tag{2.2}$$

In supply voltage based schemes, two (or more) supply voltages are used. The highest supply voltage is assigned to the gates, which are in the longest path (critical path(s)) and the lower ones are assigned to the shorter delay paths. In this way, portion of the power consumed in the circuit is saved by decreasing the supply voltage of some gates, which are in the non-critical path(s). At the same time, the circuit performance is preserved through feeding the critical path gates with the suitable supply value. Figure 2.2 demonstrates the general idea of supply-voltage based low power design schemes.

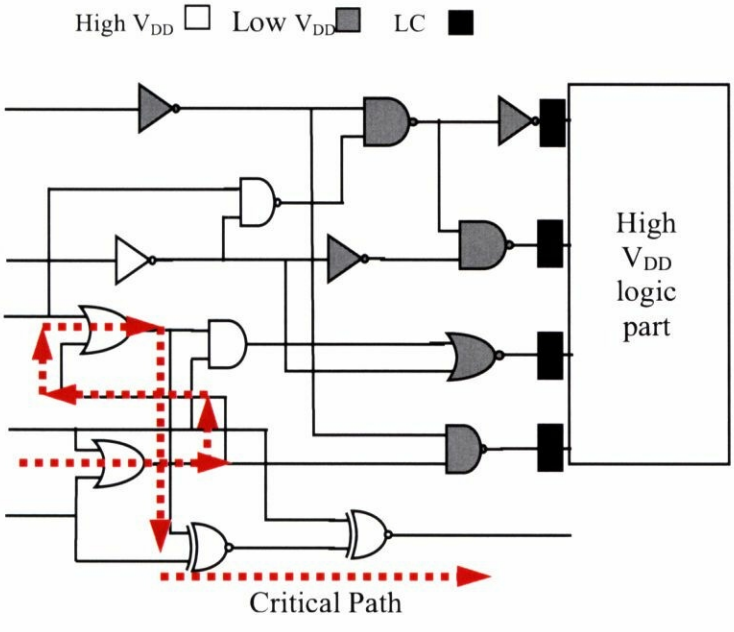


Figure 2.2 Demonstration of using multiple supply voltage.

The problem in these schemes is the need to insert a voltage level converter (LC) in front of high voltage cluster if it is preceded by low voltage cluster.

Otherwise, a leakage circuit current will path through the high voltage cluster. An example of the voltage level converter is shown in figure 2.3.

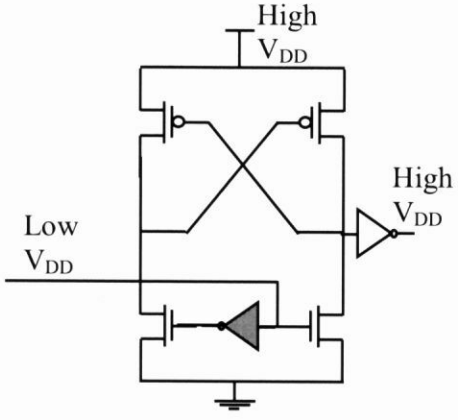


Figure 2.3 Example of voltage level converter.

Based on supply voltage reduction, many schemes had been presented to save the power consumption in digital circuits. Usami et al in [8, 9] had presented the dual supply voltage scheme. Later in [10], the same author et al had presented a methodology for a gate-level power minimization by feeding not only the gates but also the flip flops off the critical path by low supply voltage. Enhanced algorithms for selecting the high and low supply voltage gates have been presented by Chen et al in [11]. The voltage level converter adds an overhead power and area to the design. Different configurations for the level converters had been studied in [12] and a trial for converter-free multiple voltage low power technique had been presented in [13]. Instead of using only two values of supply voltage, Kuroda et al had presented a scheme for supplying the system with a supply voltage according its operating frequency. The scheme had been called variable supply voltage [14]. In [15], Kawaguchi et al have presented a controller for realizing supply voltage-hopping scheme, in which the supply voltage of a

processor is changed dynamically according the work load by a hardware-software cooperative mechanism.

2.2.3 Threshold Voltage Based Schemes

The scaling down of MOS transistor feature sizes entails scaling down the supply voltage to keep the device reliability. At the same time reducing the threshold is mandatory to keep the circuit performance. By reducing V_{DD}, the switching power is reduced quadratically, on the other side, because of V_{th} decreases, the sub-threshold leakage current increases exponentially and hence the leakage power dramatically increase to the extent that it dominates the consumed power. As it is stated above, digital circuits are featured by variety of delay paths. Using two kinds of MOS transistor with two different threshold voltages enables saving some of the leakage power. The circuit is divided into critical and non-critical paths either up on transistor level [16] or gate level [17]. Low V_{th} transistors are assigned to critical paths and high V_{th} are assigned to non-critical paths. In this way, low leakage is achieved through non-critical paths and high performance is also achieved through critical path. In contrast with the dual supply voltage schemes, voltage level converter is not needed and hence no area or power overhead is added. Figure 2.4 illustrates the idea of dual-V_{th} scheme. Another scheme based on varying the threshold voltage is known as variable threshold CMOS scheme (VTCMOS) is presented in [18][19]. In this scheme, the threshold voltage of NMOS and PMOS is controlled by using back bias effect upon the workload. In case of high workload (high frequency) the control circuit decreases the threshold voltage by increasing the body bias of the PMOS and decreasing the body bias of the NMOS. In this way the leakage current can be substantially controlled in the different operation regions. In VTCMOS scheme, triple well technology is essential to guarantee the isolation of transistors bodies. Figure 2.5 shows the basic idea of VTCMOS. The issue in this scheme is the identification of low and high threshold voltage gates/transistor. Many algorithms have been

presented to deal with this issue [16-21]. A different methodology to dynamically control the threshold voltage according to the workload through the software is presented in [22]. The threshold voltage is altered dynamically to suit the operating state of the circuit. These schemes effectively reduce the leakage at the standby mode.

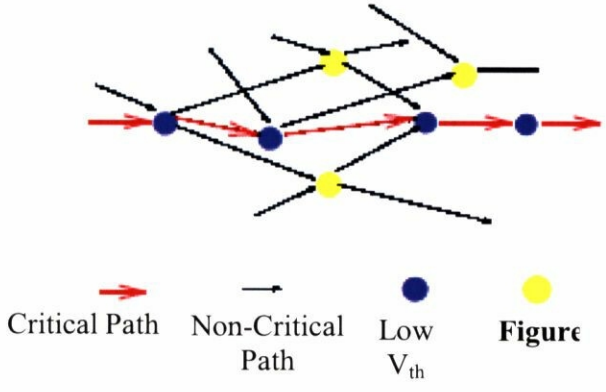


Figure 2.4 Illustration of the dual-threshold voltage scheme.

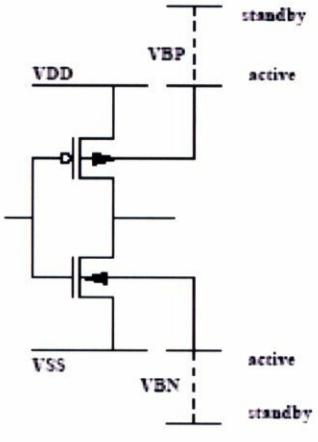


Figure 2.5 Schematic diagram of VTCMOS.

For ultra-low voltage (0.6 V and below) VLSI circuits, [23] presents a technique called (DTCMOS). In this technique, the threshold voltage of the MOS

device is a function of its gate voltage, i.e., as the driving voltage increases the threshold voltage (V_{th}) drops resulting in a much higher current drive than standard MOSFET for low-power supply voltages. On the other hand, V_{th} is high at Vgs = 0, therefore the leakage current is low. Figure 2.6 shows an illustrative schematic diagram of the technique.

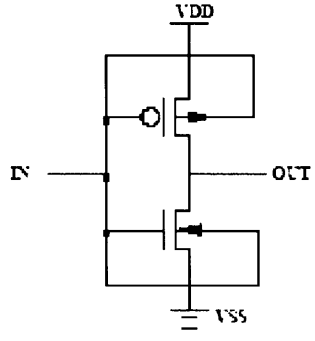


Figure 2.6 Schematic diagrams of DTMOS.

2.2.4 Gating-Transistor Based Schemes

In deep submicron regime, the leakage power is comparable with the dynamic power and in many applications; circuits spend most of their time in an idle state where no task is being performed. During these "sleep" times, it is very wasteful to have large sub-threshold leakage currents. Static power dissipation can be reduced in the sleep mode by using high V_{th} transistors with very low leakage currents to gate the power supply lines for the entire module. Since the circuits utilized two different threshold voltage transistors, the technique is referred to as multiple threshold voltage technique, (MTCMOS) [24]. Figure 2.7 demonstrate the idea of MTCMOS. The technique had been started by using two gating transistor as shown in figure 2.7-a, however, one transistor (NMOS or PMOS) is enough as shown in figure 2.7-b and c. In case of using NMOS sleep transistor (figure 2.7-c), SL signal is set high during the active mode, therefore, the low V_{th}

circuit is connected to V_{DD} and GND and hence high performance can be achieved. In idle mode, the sleep signal SL goes low and the gating transistor become off. Because of high threshold gating MOS, the leakage current is dramatically reduced. And hence the leakage power is reduced. The scheme is successful in leakage current reduction during standby mode. However, it is not suitable in a circuit where data retention is required during standby mode. Moreover, because off high threshold gating transistor, the circuit performance is drastically degraded when the supply voltage is smaller than 1V. The difficulty of the scheme is to find a suitable size for the sleep transistor. The recent work is to find suitable size of sleep transistor [25].

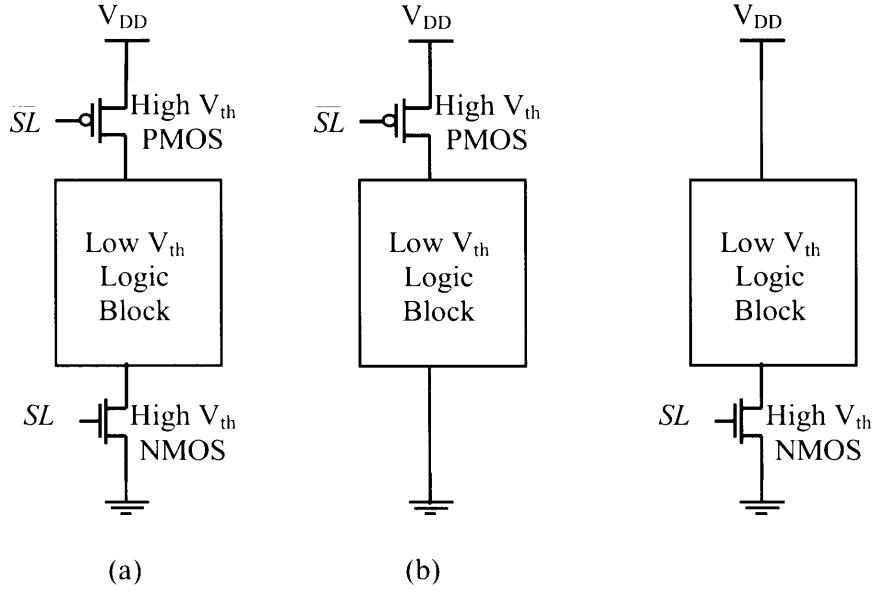


Figure 2.7 Configurations of MTCMOS technique.

To break through the barrier of 1V supply voltage for logic circuits, super cut off scheme (SCCMOS) has been proposed by [26]. The configuration is similar to figure 2.7-b and c, but instead of using high threshold voltage gating transistor, low threshold voltage ones are used. PMOS transistor, which has low V_{th}, is

inserted in series to the logic circuits consisting of low-V_{th} MOSFETs. The low threshold voltage assures high-speed operation of the logic circuits. Instead of PMOS, NMOS can be inserted between the circuit and the ground line. During active mode, the gate voltage of PMOS/NMOS is connected to ground/V_{DD} to turn it on. When the logic circuits enter the stand-by mode, the gate of PMOS/NMOS is overdriven to V_{DD}+0.4 /V_{SS}-0.4 to completely cut off the leakage current. The disadvantage of this scheme is the high voltage stress across the gate oxide of the gating transistor, which may degrade the reliability of the gate oxide especially in the sub 100nm technology. This problem has been solved in an upgraded version of the scheme called zigzag super cut off scheme (ZSCCMOS) [27].

2.3 Low Power Schemes for Evaluation

Form the above discussion; the minimization of the power consumption in digital systems has been tackled through many ways. Most of these ways are within one or more of the following methodologies:

(i) Decrease the supply voltage when possible.

(ii) Increase the threshold voltage when possible.

(iii) Disconnect the power supply when the circuit is in sleep mode.

There are some other ways used for low power digital design such as using multiple channel lengths and oxide thicknesses. However, in this work, we consider only three different schemes. Each utilizes one of the three mentioned approaches. The first scheme is based one supply voltage, namely, dual supply voltage scheme. In this scheme, two supply voltage values are used. The higher is assigned to the gates in critical path(s) in order to keep the circuit performance, while the lower supply voltage is assigned to some of the other gates according to slack time. To avoid the creation of leakage current paths, the higher V_{DD} cluster should be placed in front of the lower V_{DD} cluster; otherwise a voltage level converter should be used to adapt the output of the low V_{DD} gate to the input of the

high V_{DD} gate. In this work, the technique will be referred to as DSVCMOS (Dual Supply Voltage CMOS scheme). The testing circuits of this technique have been design by using the methodology described in [11] where the level converters are inserted if needed.

The second scheme is based on threshold voltage variation, namely, Dual threshold voltage CMOS scheme. In this scheme, two threshold voltage values are used. The higher is assigned to the gates outside critical path. Therefore, the leakage power in these gates is reduced. While to maintain the circuit performance, a lower threshold voltage is assigned to gates in the critical path. The scheme will be referred to as (DVTCMOS). In this work, the testing circuits of this technique have been design according to the methodology described in [16].

The third technique is based on gating transistor, namely, multiple threshold voltage CMOS. The multiple threshold voltage CMOS (MTCMOS) circuit was proposed by inserting high V_{th} transistor(s), which is sometimes called sleep transistor, in series to a low threshold voltage circuit. In this work, the size of the sleep transistor is chosen such that the effective supply voltage is decreased by less than 5%.

2.4 Noise Sources

The main reason of all kinds of noise sources in the modern digital circuits is the existence of parasitic elements which are increasing with the scaling of LSI technology. An example of the existence of parasitic elements in digital circuit is shown in figure 2.8 [28-29]. In the following subsection, we, briefly, explore the different noise sources in digital circuits.

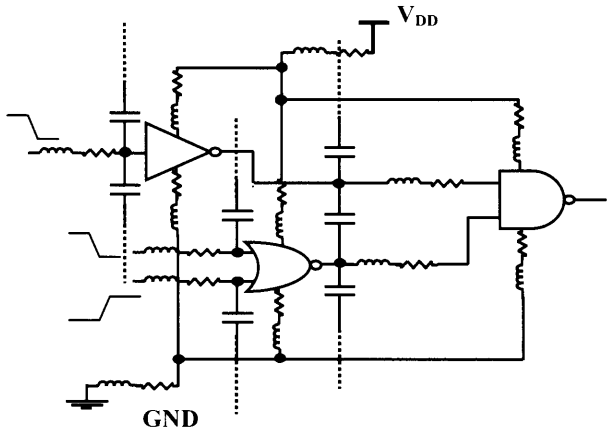


Figure 2.8 Schematic diagram of a digital circuit with parasitic elements.

2.4.1 Power Supply and Ground Bounce Noise

Power supply and ground bounce noise includes IR drop and Ldi/dt noise. Traditionally, IR drop occurs mostly on chip and di/dt was considered only in the package. However, as the technology of VLSI is developed toward nano technology with faster switching speed and higher density, the inductive component of the off-chip wires and on-chip interconnects cannot be ignored. di/dt noise is caused by the sudden change in the current of power/ground net due to the switching processes. The value of di/dt is increasing with technology development. That is, the number of simultaneously switching gates is increasing due to the higher integration. Furthermore, the effect of both IR drop and Ldi/dt has become higher because of the scaling of the supply voltage. The deleterious effect of the supply/ground noise can be ranged from deterioration of the circuit speed due to decreasing the effective value of the supply voltage to the generation of false pulses, which may tend to function failure [30-33].

2.4.2 Crosstalk Noise

Crosstalk is induced due to capacitive and/or inductive coupling between two, (or more), adjacent wires when their parasitic cross-coupling capacitance and/or inductance are large enough to influence the electrical characteristics of each other. Whenever a transition takes place in a wire, a noise pulse is produced through this coupling in another wire(s). It has been shown that crosstalk between interconnects can significantly affect the performance of the design. [34-35]. The major effects of crosstalk are delays, which change signal propagation time and thus can cause setup or hold time failures, and glitches, which can cause voltage spikes on wires resulting in false logic behavior. Although there are some efforts to avoid the crosstalk during the design phase, it is difficult to be totally eliminated [36]. To mathematically model the crosstalk signal is a tough task. That is, in a real circuit, a given signal line may be coupled with several thousands signal lines [35].

2.4.3 Other Noise and Pseudo Noise Sources

The other noise sources are due to electromagnetic interference with the adjacent IC on the same board as well as the signal reflection due to impedance mismatching. There is some other pseudo noise because of the parametric variation during the fabrication phase, the temperature variation during circuit operation in addition to the unreliable extraction of the parasitic elements during the design phase. These pseudo noise sources can be treated statistically because it is too complicated to determine in the design phase.

2.5 Noise Modeling

To accurately study the noise effect on the performance of a design, the noise model should include all kinds of noise sources discussed so far. In this work, the noise has been

modeled as a random voltage source to combine all the possible noise sources. The random voltage source is inserted in the testing circuit where it is appropriate. For example, given a digital circuit similar to that is shown in figure 2.8, the parasitic elements are exchanged with voltage sources having random distribution as shown in figure 2.9.

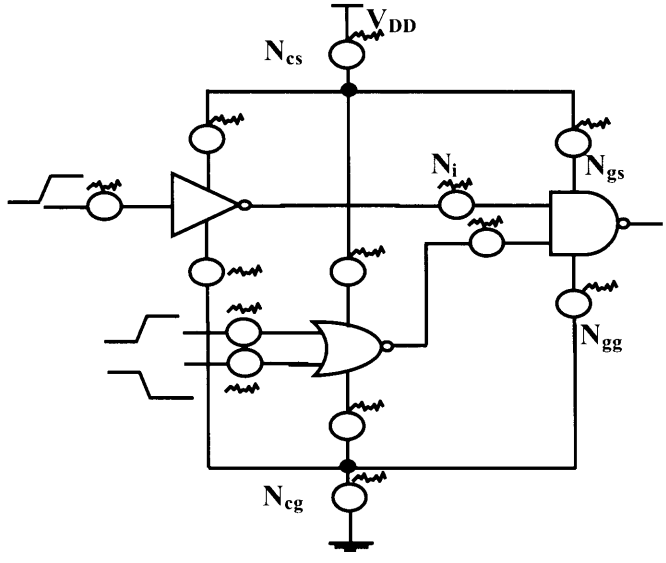


Figure 2.9 Schematic diagram of digital circuit with noise sources.

The noise sources in adjacent gates are strongly correlated; especially the power supply/ground noise. So that, in our model, there are common noise sources in power line (N_{cs}) and in ground line (N_{gs}) in order to express the correlated noise. The other noise sources in power/ground net (N_{gs}, N_{gg}) are to represent the uncorrelated noise sources mentioned in subsection 2.4.1 in addition to the local noise in each gate. In other words, the total power supply and ground noise can be expressed by (Ncs + Ngs) and (Ncg + Ngg) respectively. The noise on interconnects, in our model, is represented by two components. The first is the crosstalk noise, which is represented by the noise source (Ni). The second

component is the noise propagated from the power/ground lines of preceding stage(s), which is (Ncs + Ngs), or (Ncg + Ngg). It is obvious that the model expresses all noise sources existing in the digital circuits. The noise sources are assumed to have Gaussian distribution. The variances of the noise sources can be controlled during the evaluation. In this way, we can measure the noise immunity of different circuit techniques at specific noise levels.

2.6 Evaluation Framework

The study in this chapter is based on transistor-level simulation. Given a digital design, the noise sources are inserted according to the model described in the pervious section. The the circuit is simulated (by using HSPICE) many times under different noise levels staring from level zero (clean signals and power/ground nets). The HSPICE analog outputs are then converted into ones/zeros using C++ code. After that, the results at different noise levels are compared with results at zero noise to evaluate the error. Since that the noise sources are assumed to be random noise source, the simulation has been repeated many times and averaged to obtain reliable results. The results are examined for two kinds of errors, which are logic error rate and delay error. The logic error rate is defined as the ratio of number of output error pulses to the number of input pulses, while the delay error is defined as the ratio of delay-increase (due to noise) to the delay without noise.

2.7 Simulation Results

In order to compare the noise immunity of the mentioned low power techniques, three circuits have been designed and simulated assuming 0.18μm technology. The circuits are:

(i) 4-bit ripple carry adder (ckt1).

(ii) 4x4 carry-save multiplier (ckt2).

(iii) Random logic circuit taken from [9] (ckt3).

PathMill, from Synopsys, has been used during the design phase of the low power circuits to make the necessary timing analysis. For the sake of reliability comparison between the low power and the traditional design, the testing circuits have also been designed using the ordinary techniques. The ordinary techniques are (Low V_{th}) at which, all the gates have low threshold voltage and (High V_{th}) at which all the gates are high threshold voltage. So, we have five different techniques for each of the three testing circuits. All but high-V_{th} have the same critical path maximum speed.

Comparing the reliability of each technique is done by answering the following question; which low power technique is the robust one with regard to the noise and how is it compared with the traditional techniques? The answer of this question can be given by answering the following two sub-questions.

1- Which technique will work correctly (with no logic error) under a higher noise level?

2- Which technique has the lowest delay error due to the effect of a given noise level?

2.7.1 Power Consumption Comparison

Despite that the main objective of the work is to investigate the noise immunity of low-power static CMOS design schemes, it is worth to compare the power consumption of each technique of the testing circuits. The digital circuits may work in two modes, which are active mode and sleep mode. In active mode, a sequence of input vectors are supplied to the testing circuits and the sleep transistor is set on in the circuits implemented by MTCMOS technique. In sleep

mode, the primary inputs of the testing circuits are connected to ground and the sleep transistor is set off. Although the input vector in the second case might not be the optimum vector to save the leakage power in the sleep mode, it has been applied to all circuits for fair comparison. The noise sources are disabled. The testing circuits are simulated and the power consumption are calculated and normalized to that of the conventional technique (Low V_{th}) in the two different modes. The results are shown in table 1.

Normalized power consumption of		Low V_{th}	MTCMOS	DVSCMOS	DVTCMOS
Active mode	ckt1	1	~1	0.787	~1
	ckt2	1	~1	0.843	~1
	ckt3	1	~1	0.832	~1
Sleep mode	ckt1	1	7.57E-4	~1	0.595
	ckt2	1	3.29E-4	~1	0.558
	ckt3	1	1.03E-3	~1	0.702

Table 2.1 Comparison between the power consumption of the testing circuits.

2.7.2 Logic Error Rate

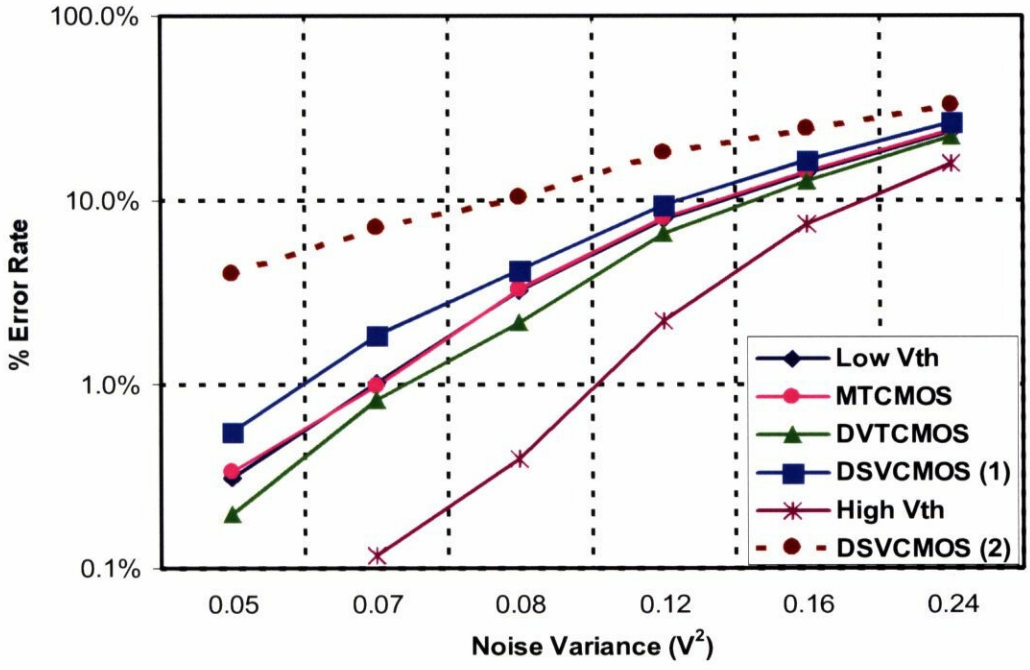
To evaluate the logic error rate, Gaussian noise sources have been inserted in the testing circuits according to figure 2.9. The noise is defined as piecewise linear (PWL) signal and the interval is chosen to be 70 pico-second, which is slightly larger than the inverter delay of this technology (0.18μm). That is, the effective noise bandwidth is limited by the inverter delay. Then, the circuits have been simulated at discrete noise levels by using HSPICE. To get an accurate logic error result, the analysis has been done fifteen times. The results of HSPICE have been

analyzed to evaluate the average logic error rate. The logic error rate of each technique is plotted against the noise level. The results are shown in figure 2.10. In case of DSVCMOS, the simulation has been done twice; first, when the RMS of the noise sources have the same values in all gates at each simulation point, the result in this case is referred to as DSVCMOS(2), second, the RMS of power supply noise sources are adjusted according to V_{DD} utilized by the gate assuming that there are two separate power supply nets, one is for high V_{DD} and the other is for the low V_{DD}, the results in the second case is referred to as DSVCMOS (1). In all curves of figure 2.10, but DSVCMOS(1), the RMS of V_{DD}, GND and input noise sources have been assigned similar values in all gates at each simulation point due to the lack of information about the relationship between the RMS of the different noise sources. In case of DSVCMOS(1), the RMS of low V_{DD} noise source is equal to that of high V_{DD} multiplied by the ratio of low V_{DD} to high V_{DD} [32]. Although it is difficult to exactly determine the minimum noise level at which the logic error starts to occur in each design technique, it is possible to find out which technique is the robust one by extrapolating the curves toward the horizontal axis. Doing this, we can say that the error will more likely happen at first in the DSVCMOS technique followed by Low V_{th} and the MTCMOS with approximately the same degree, then in DVTCMOS and finally in the high V_{th} technique. Excluding the high-V_{th} technique from the results, it has longer critical delay. We can conclude the following two points.

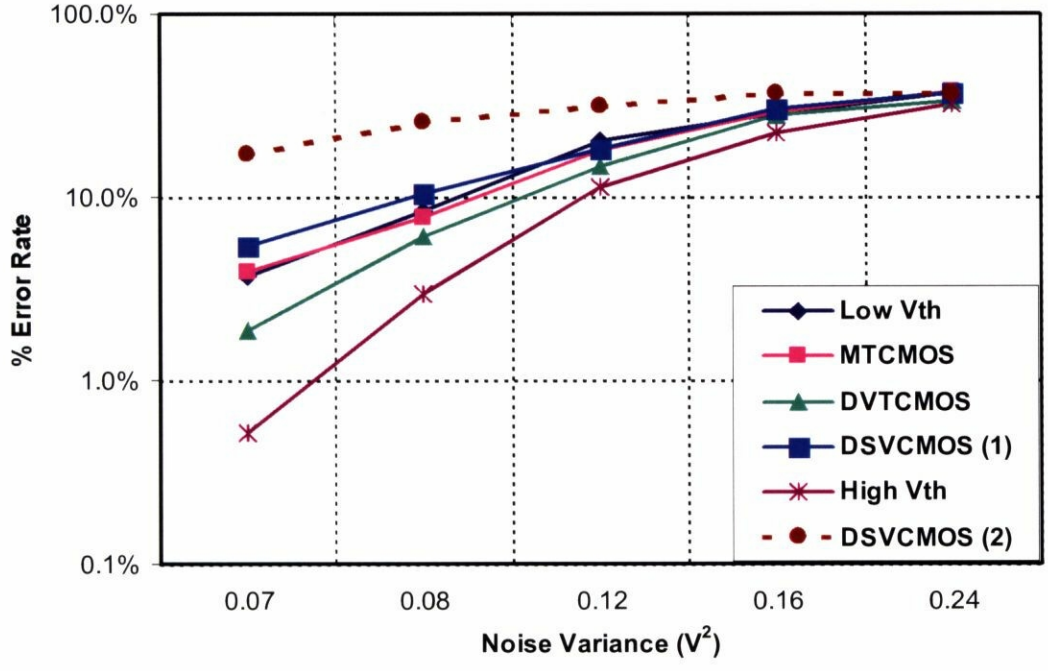
1- The DVTCMOS is the robust low power technique among the investigated techniques.

2- The DVTCMOS is better than the traditional low V_{th} not only in power consumption but also in logic error rate.

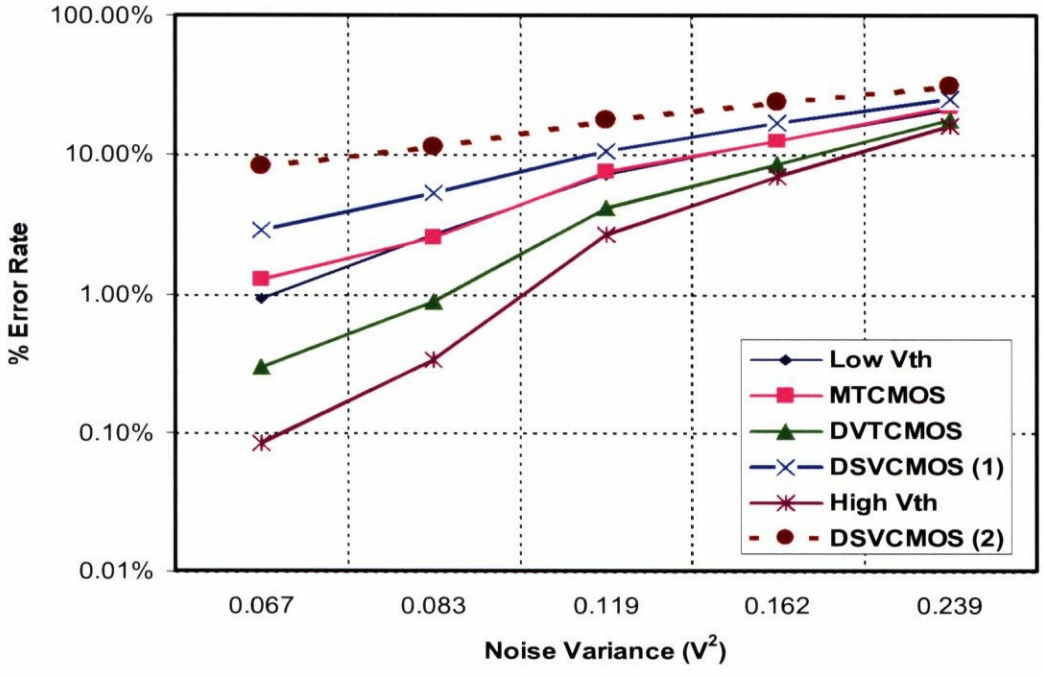
This is the answer of the first sub-question.


100.0%
10.0%
1.0%
0.1%
% Error Rate
0.05
0.07
0.08
0.12
0.16
0.24
Noise Variance (V²)
Low Vth
MTCMOS
DVTCMOS
DSVCMOS (1)
High Vth
DSVCMOS (2)

(a)


100.0%
10.0%
1.0%
0.1%
% Error Rate
0.07
0.08
0.12
0.16
0.24
Noise Variance (V²)
Low Vth
MTCMOS
DVTCMOS
DSVCMOS (1)
High Vth
DSVCMOS (2)

(b)

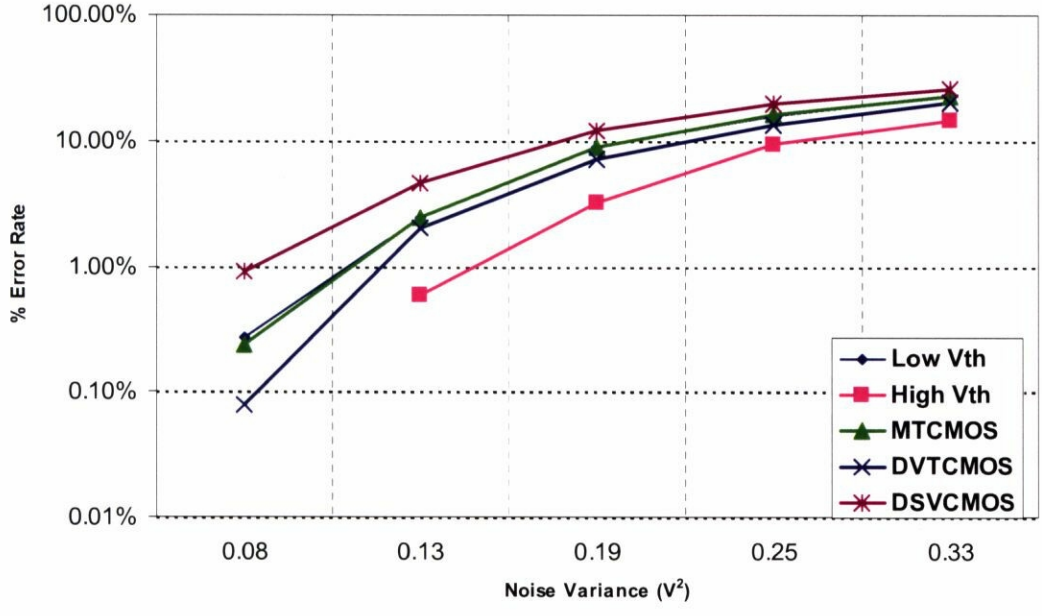


(c)

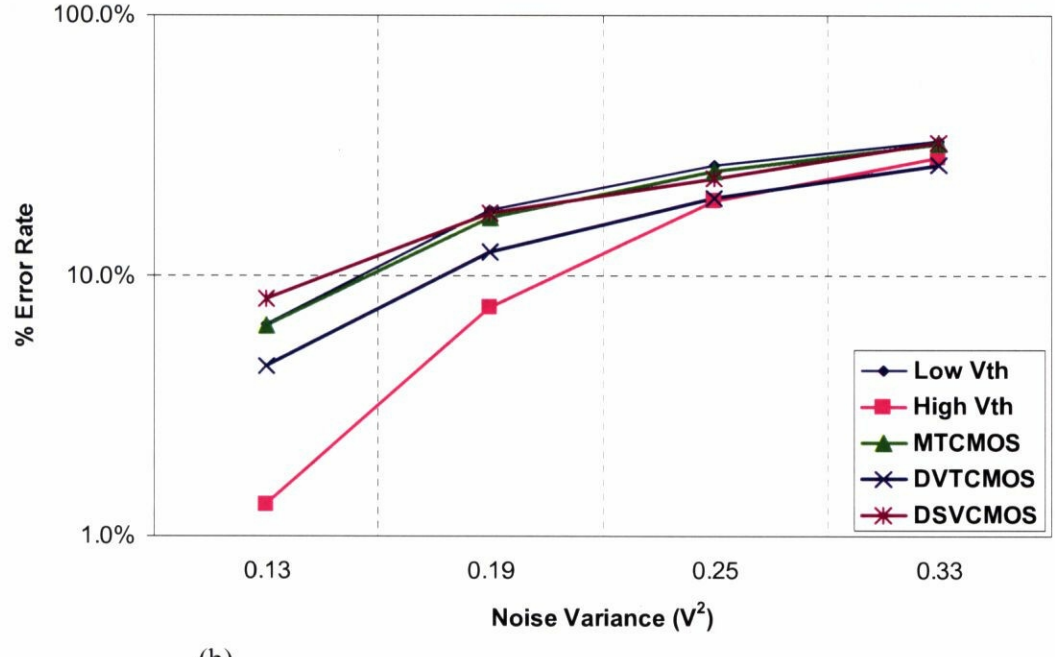
Figure 2.10 Logic error rate in the testing circuits at different noise values (a) ckt1. (b) ckt2. (c) ckt3. HV_{DD}=1.8V, LV_{DD}=1.2V, LV_{th}=0.15V and HV_{th}=0.4V. The RMS of V_{DD}, GND and input noise sources have been assigned similar values in all gates at each simulation point. In case of DSVCMOS(1), the RMS of low V_{DD} noise source is equal to that of high V_{DD} multiplied by the ratio of low V_{DD} to high V_{DD}.

The comparison has been done at different noise conditions to test the relative noise immunity of the different low-power design schemes. Figure 2.11 shows the comparison results at the existence of power/ground noise only (interconnects noise sources are set to zero), while figure 2.12 shows the

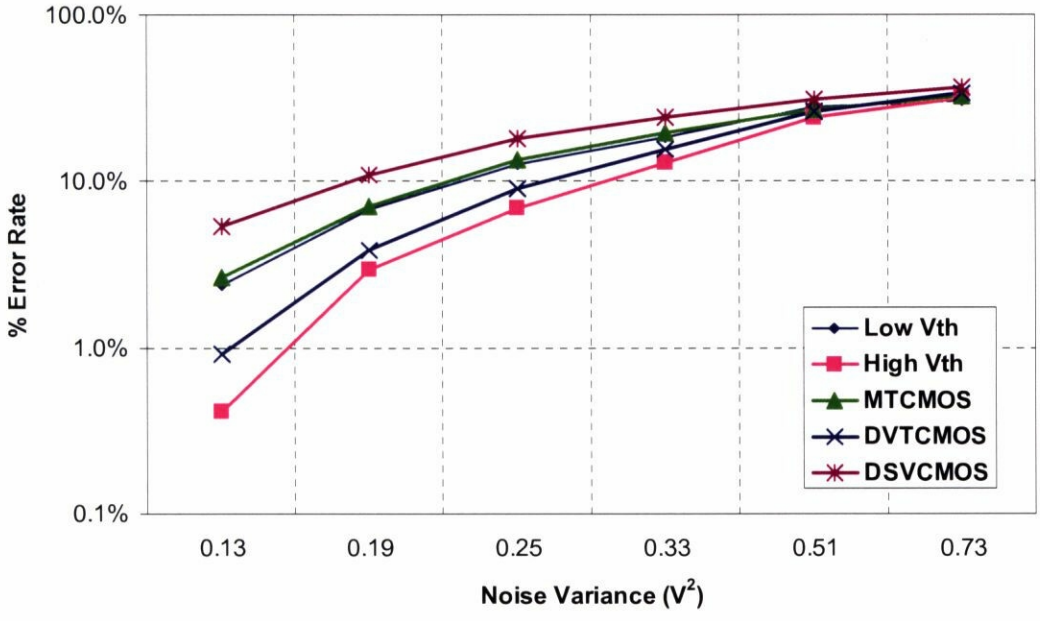
comparison at the existence of interconnect noise sources only (the supply and ground noise sources are set to zero).



(a)



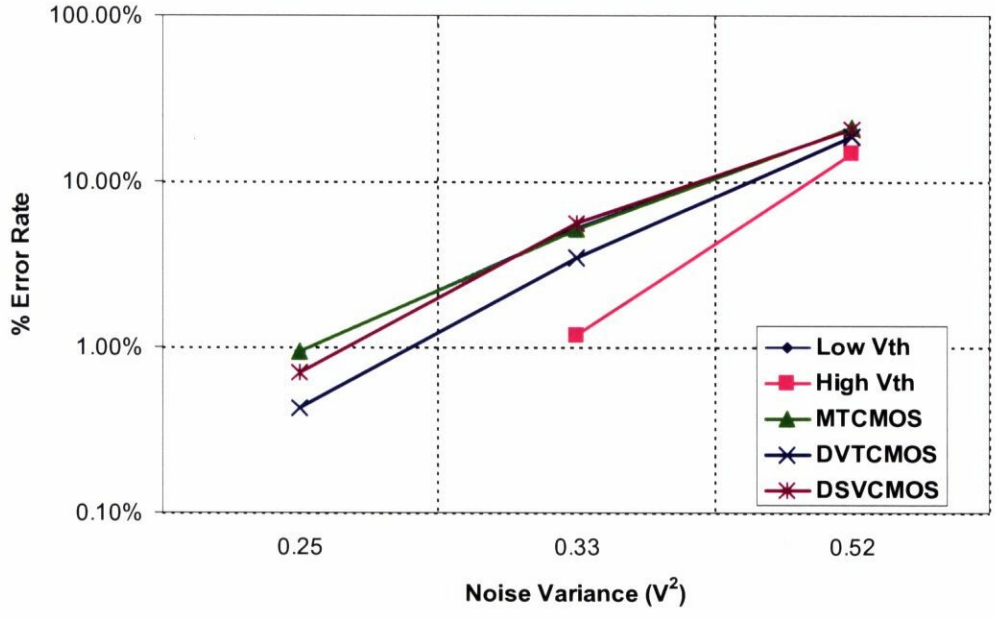
(b)



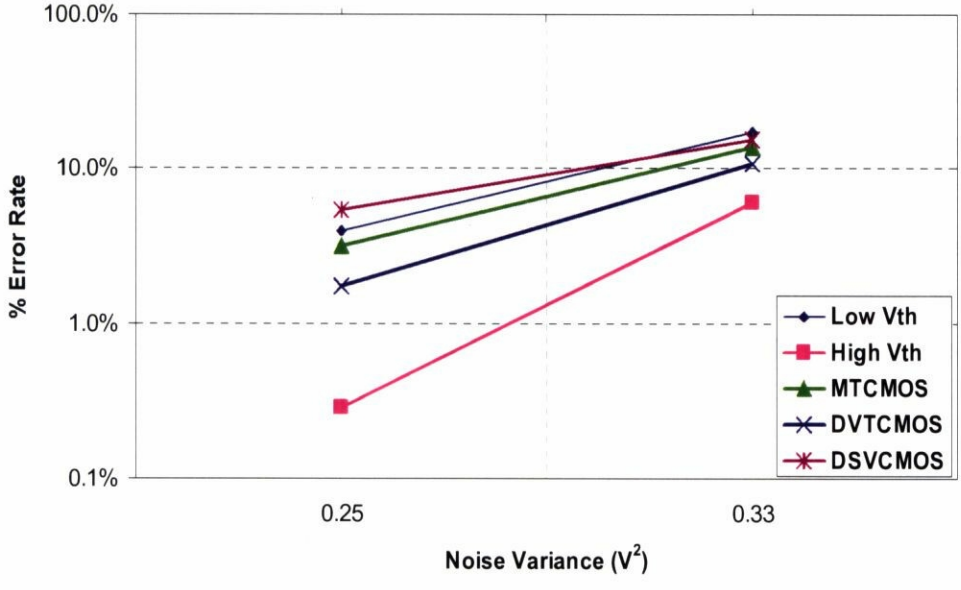
(c)

Figure 2.11 Logic error rate in the testing circuits at different power supply noise values (a) ckt1. (b) ckt2. (c) ckt3. HV_{DD}=1.8V, LV_{DD}=1.2V, LV_{th}=0.15V and HV_{th}=0.4V. The RMS of V_{DD}, and GND noise sources have been assigned similar values in all gates at each simulation point. In case of DSVCMOS, the RMS of low V_{DD} noise source is equal to that of high V_{DD} multiplied by the ratio of low V_{DD} to high V_{DD}. The noise on interconnects are set to zero.

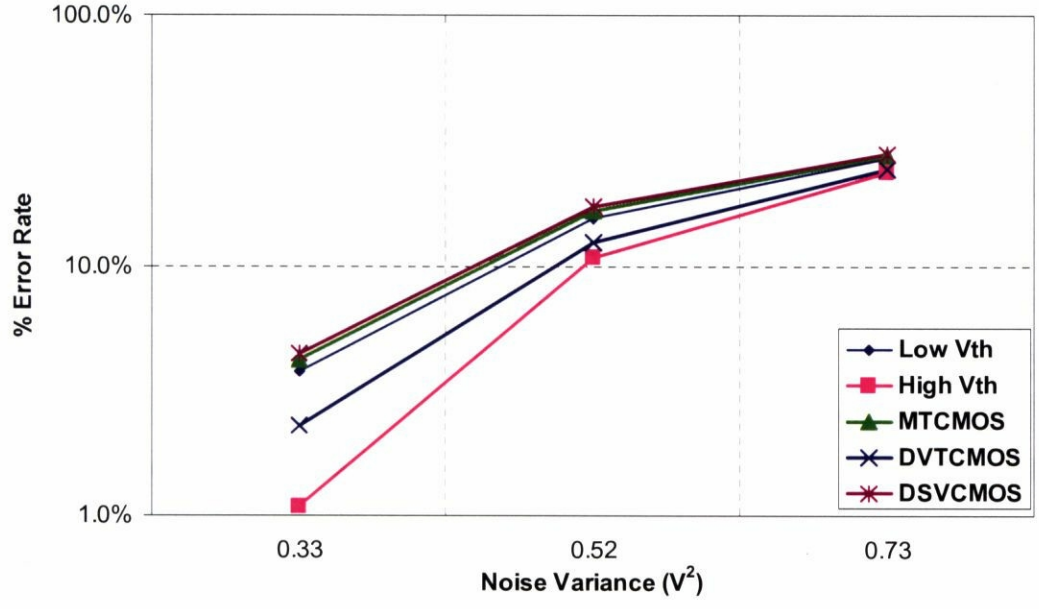
Note that the RMS of low V_{DD} noise source is equal to that of high V_{DD} multiplied by the ratio of low V_{DD} to high V_{DD}. Figures 2.11 and 2.12 reveal the same information given by figure 2.10, which ensures the rigidity of the obtained results.


100.00%
10.00%
1.00%
0.10%
% Error Rate
0.25
0.33
0.52
Noise Variance (V²)
Low Vth
High Vth
MTCMOS
DVTCMOS
DSVCMOS

(a)


100.0%
10.0%
1.0%
0.1%
% Error Rate
0.25
0.33
Noise Variance (V²)
Low Vth
High Vth
MTCMOS
DVTCMOS
DSVCMOS

(b)



(c)

Figure 2.12 Logic error rate in the testing circuits at different noise values on the interconnects (a) ckt1. (b) ckt2. (c) ckt3. HV_{DD}=1.8V, LV_{DD}=1.2V, LV_{th}=0.15V and HV_{th}=0.4V. The RMS of V_{DD}, and GND noise sources have been set to zero, and those of noise source on interconnect have been assigned similar values in all gates at each simulation point.

It is worth to note that it is very difficult in practice to measure a very low logic error rate even by simulation. For example, to produce a 10^{-20} error rate in a 100MHz clock system, we need to run for 10^{12} second (around 4000 years), so that we accelerate the error rate by increasing the noise level. The validation of

extrapolation process is confirmed by the calculations results as it will be explained in the next chapter.

2.7.3 Delay Error

The second category of error, which is caused by noise, is the delay error. To study the noise effect on the delay of the different paths in a low power design, the different paths in the design are first categorized. In ordinary digital design, there are many paths with different propagation delays. One (or more) out of them is (are) critical. After converting the ordinary design into a low power one, many paths have a delay equal or at least very near to that of critical path especially if the concepts of potential slack [37] is used. In our testing circuits, we may find three path categories; these paths have similar delay in absence of the noise. The path categories are:

1. The original critical path, at which all gates are fed at high supply voltage and have low threshold voltage. This path exists in all testing circuits. It will be referred to as low V_{th}- high V_{dd} (HVDD-LVt) path.

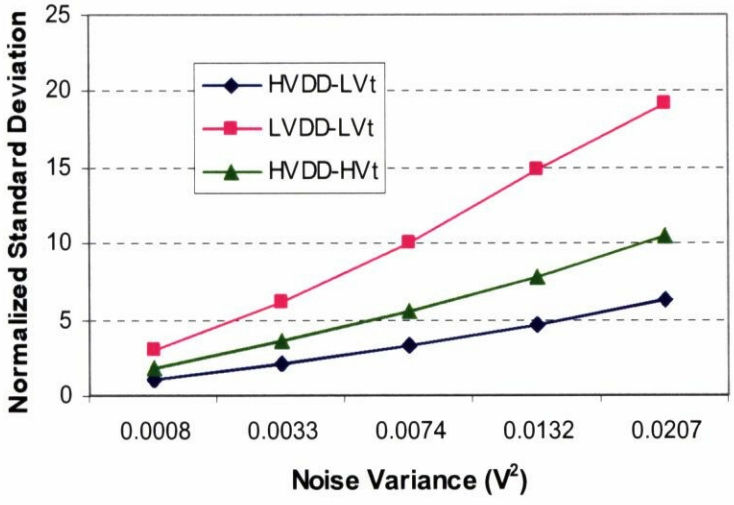
2. A path has lower number of gates than the path of the first category; the gates on this path are supplied by the same supply voltage value as path of the first category but the threshold voltage is higher. This category exists in the DVTCMOS technique. It will be referred to as high-V_{th} high-V_{dd} (HVDD-HVt).

3. A path has lower number of gates than the path of the first category with the same threshold voltage and powered at lower supply voltage. This path exists in the DSVCMOS circuits and it will be referred to as low-V_{th} low-V_{dd} (LVDD-LVt).

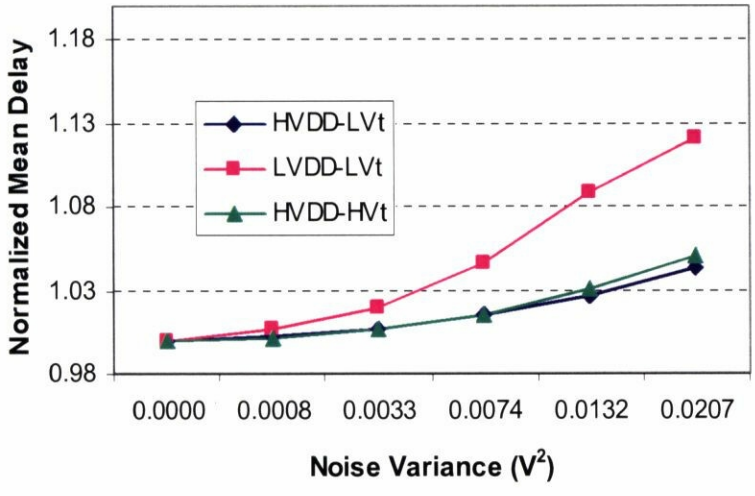
The other paths have lower propagation delay than the delay of the critical path(s), which means that in presence of noise, their propagation delay would still almost lower than that of critical path and hence they show no delay penalty. Therefore, they are less important than the above-mentioned paths because they will not determine the circuit speed in presence of noise.

To compare the delay error due to noise in the mentioned paths, a statistical timing analysis to the propagation delay in these paths is done in presence of noise at different levels. Each path is consisted of inverter chain with unity fan out. The number of inverters is chosen such that the delays of all paths are identical at noise-free condition. The RMS of V_{DD}, GND and input noise sources have been assigned similar values in all gates at each simulation point. It is assumed that the sleep transistor used in MTCMOS is large enough such that the difference between the performance of MTCMOS and that of LV_t- HV_{DD} is not substantial. So that MTCMOS is not included in this comparison. The mean and standard deviation values of the propagation delay of each path category is calculated and the results are as shown in figure 2.13. The results imply that (LV_{DD}-LV_t) path is more susceptible to the noise than (HV_{DD}-HV_t) and (HV_{DD}-LV_t). Therefore, in presence of the noise, the performance of the DSVCMOS circuits would be determined by the low voltage paths and would be determined by the high threshold voltage paths in case of DVTCMOS circuits. However, in terms of delay error, the DVTCMOS technique is better than DSVCMOS. This is the answer of the second sub-question.

The results also imply that the effect of noise should be carefully taken into account when designing low power circuits by (i) accurate estimation of the noise level during the design phase, (ii) leaving an enough time slack room according to the noise level in the high threshold voltage paths in case of DVTCMOS circuits and in the Low supply voltage paths in case of DSVCMOS.



(a)



(b)

Figure 2.13 Effect of noise on propagation delay of different path categories in Low power techniques (a) Normalized standard deviation. (b) Normalized mean. HV_{DD}=1.8V, LV_{DD}=1.2V, LV_{th}=0.15V and HV_{th}=0.4V. The RMS of V_{DD}, GND and input noise sources have been assigned similar values in all gates at each simulation point.

2.8 DVTMTCMOS: a High Noise Immunity Design Scheme with Low Leakage Power Consumption

The scheme is simply a combination from dual V_{th} (DVT) and multiple V_{th} (MT) techniques. For a given circuit, at first it is designed as a dual V_{th} circuit using any of the above mentioned methodologies. Low V_{th} would be assigned to the gates of critical paths and hence these gates only should be connected to sleep transistor to control the leakage current during standby mode. That is other gates have high V_{th} and hence it is originally low leakage. In some cases, the threshold voltage of the high V_{th} gates is the same as that of sleep transistor, which simplifies the implementation process. Furthermore, in most circuits, the number of high V_{th} gates may reach 70-90% of the total number of gates [16], which imply that the size of the required sleep transistor would be small. The important thing to notice is that most of the low V_{th} gates are in critical paths, which make it easy to classify these gates into groups to use the phenomenon of mutual exclusive discharging in designing smaller size sleep Tr. A block representation for the scheme is shown in figure 2.14.

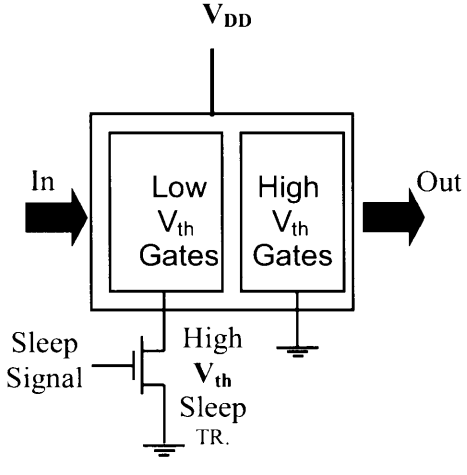


Figure 2.14 Block Diagram of DVTMTCMOS.

2.8.1 Leakage Power and Area Overhead Comparison

To investigate the power consumption reliability of the technique compared with above-mentioned techniques, the testing circuits stated above are also designed using DVTMTCMOS. The testing circuits have been simulated at noise-free conditions and the power consumption is calculated. Table 2.2 shows the results. The power consumed by the different testing circuits at different schemes normalized to the leakage power of low V_{th} circuits in active and sleep mode. The results say that the scheme has the virtue of DVTCMOS in the active mode and the virtue of MTCMOS in sleep mode. Moreover, the sleep transistor area is also saved. Since that, in case of DVTMTCMOS, the sleep transistor is used to control a fewer number of transistor than in case of MTCMOS. Table 2.3 shows the size of sleep Tr. used in DVTMTCMOS compared to that used in MTCMOS and the speed degradation of both MTCMOS and DVTMTCMOS with respect to DVTCMOS technique.

		Low V_{th}	MT	DVT	(This work) DVTMT
Active mode	ckt1	1	~1	0.702	0.702
	ckt2	1	~1	0.558	0.558
	ckt3	1	~1	0.595	0.595
Sleep mode	ckt1	1	7.57E-04	0.702	6.88E-04
	ckt2	1	3.29E-04	0.558	3.28E-04
	ckt3	1	1.03E-03	0.595	3.84E-04

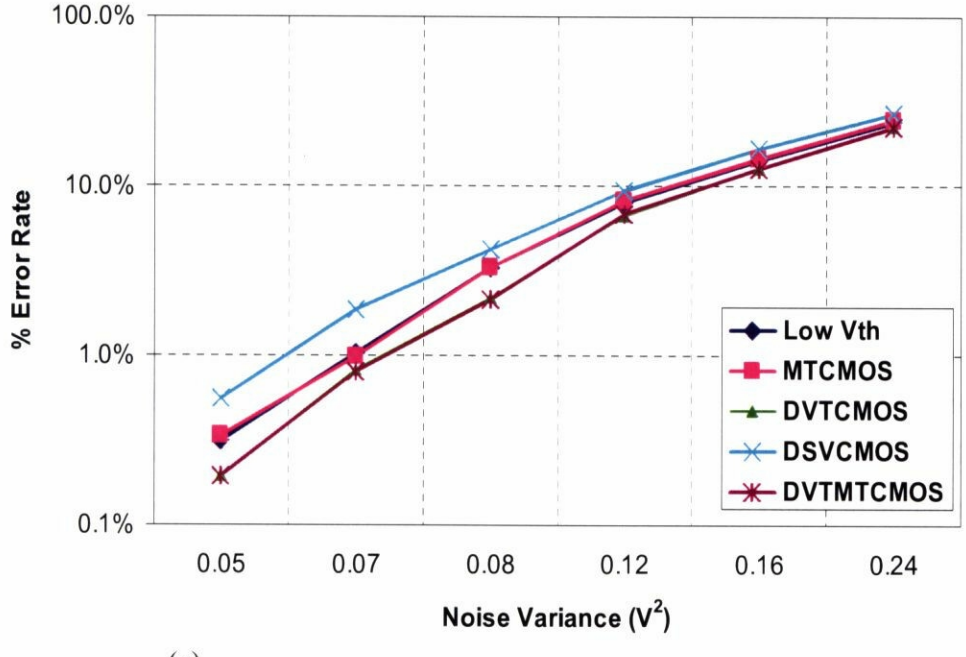
Table 2.2 Power consumption comparison.

	MT	DVTMT	Speed degradation
ckt1	1	0.4	1.40%
ckt2	1	0.625	1.30%
ckt3	1	0.4	3.40%

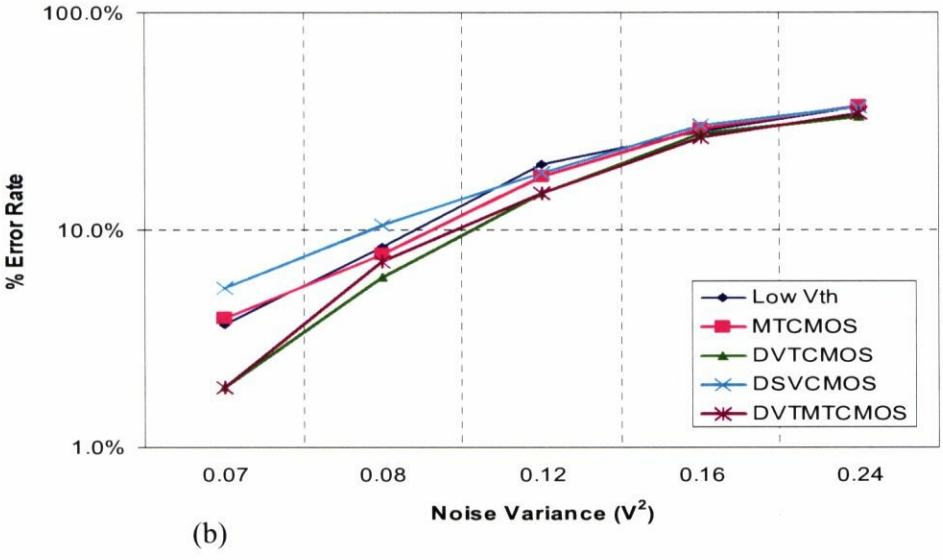
Table 2.3 Area overhead and speed comparison.

2.8.2 Logic Error Rate Comparison

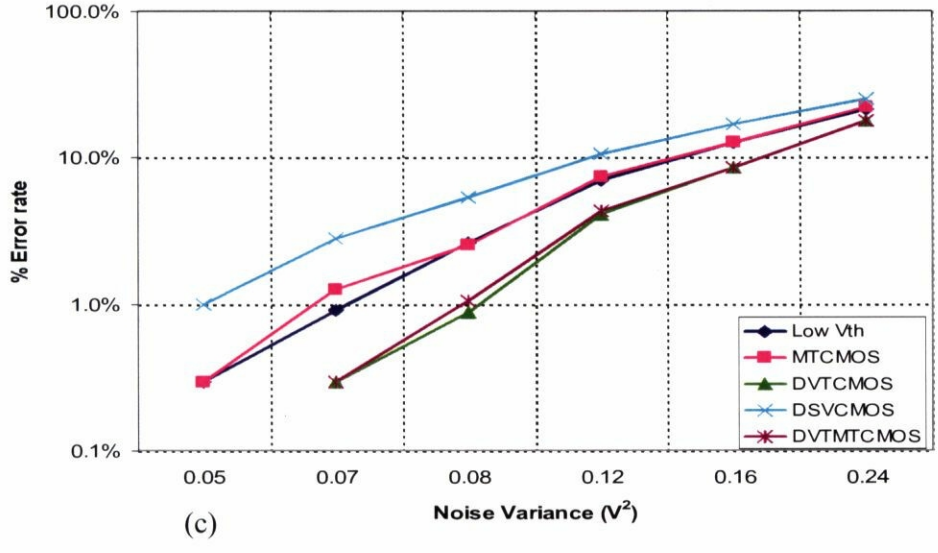
The testing circuits have been simulated at discrete noise levels by using HSPICE. The simulation has been done fifteen times and the results have been analyzed to evaluate the average logic error. The logic error rate of the testing techniques at different noise levels is shown in figure 2.15. The results imply that threshold voltage plays an outstanding rule in the noise immunity of digital circuits. Although it is quite difficult to exactly determine the minimum noise level at which logic error starts to occur at each design technique, it is possible to find out which technique is the robust one by just extrapolating the curves toward the horizontal axis points. Doing that, we can say that the error will more likely happen at first in DSVCMOS technique followed by Low V_{th} and MTCMOS with approximately the same degree, then DVTCMOS and DVTMTCMOS with approximately the same level.



(a)



(b)



(c)

Figure 2.15 Logic error rate of DVTMTCMOS compared with other schemes different noise values (a) ckt.1 (b) ckt.2 (c) ckt3. HV_{DD}=1.8V, LV_{DD}=1.2V, LV_{th}=0.15V and HV_{th}=0.4V. The RMS of V_{DD}, GND and input noise sources have been assigned similar values in all gates at each simulation point. In case of DSVCMOS the RMS of low V_{DD} noise source is equal to that of high V_{DD} multiplied by the ratio of low V_{DD} to high V_{DD}.

From the results we can conclude the following point. DVTCMOS and DVTMTCMOS are the robust low power techniques among the investigated techniques.

2.9 Discussion and Technology Dependence

From the above results, one can notice that (LVDD-LVth) path or cell has the worst immunity form delay or logic error point of view. The logic error is, in some how, function of the gate noise margin. The noise margin is better in case of HVth than in case of LVth. This may explain why (HVDD-HVth) is better than (LVDD-LVth) in figure 2.10-2.12. On the other hand, in case of delay error as shown in figure 2.13, the delay of the gate (path), which has HV_{th}, is more sensitive to the decrease in V_{DD} (caused by the noise) than the delay of the gate (path), which has LV_{th} if the gates have the same supply voltage. However, in case of DSVCMOS and DVTCMOS, the scenario is governed by the ratio of V_{th}/V_{DD}, which are used in the non-critical paths. Looking to equation 2.2 and the design ratios given the literature, it is found that, in presence of noise, (LVDD-LVth) will show more delay than (HVDD-HVth).

The assumed technology during simulation or calculation is 0.18μm technology. The ratio between HV_{DD} and LV_{DD} is calculated by using the formula reported in the papers concerning the dual supply voltage technique [3] keeping the constraints of critical path and minimum power consumption. The same thing has been done in choosing the high and low V_{th} for DVTCMOS/DVTMTCMOS. For other technologies (larger/smaller), the ratios of LV_{DD}/HV_{DD} and HV_{th}/LV_{th} will not dramatically differ from those of 0.18μm technology. Although the logic error rate that may occur in other technologies may not be the same as measured (calculated) in case of 0.18μm technology, we believe that the results will have the same trend and hence our conclusion, regarding the robustness of DVTCMOS/DVTMTCMOS over the other low power design schemes, is valid for

any other technology. In a particular design, the average values and standard deviation of the noise sources could be derived using circuit simulator.

2.10 Chapter Conclusion

This chapter presents the effect of noise on the performance of a selected group of low power as well as traditional digital design techniques. First, we present a model for the different noise sources in the digital circuits. Then we applied the model to a group of low power and traditional design testing circuits. The results clearly demonstrate that, from the noise immunity point of view, the dual threshold voltage technique is the best among the tested LP schemes having the same performance. In addition, in presence of strong noise, the low V_{dd} paths determine the speed of the dual supply circuits and the high V_{th} paths determine the speed of the dual V_{th} circuits, however the performance of the high V_{th} (dual V_{th} circuits) is better. The chapter also includes a proposed methodology for leakage power saving and at the same time it has the same reliability of DVTCMOS, which is DVTMTCMOS. Since the simulation time is prohibitively long for bigger circuits than the tested circuits, in the next chapter, we will present a methodology to calculate the logic error rate of the big digital circuit and hence we will be able to calculate the logic error rate of a given digital system at different biasing, threshold voltage and noise levels. Therefore we can anticipate the logic error rate of a given digital system during the design phase.

2.11 References

[1] http://public.itrs.net/

[2] J. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, Prentice Hall Electronics and VLSI Series, Pearson Education Inc., New Jersey, 2003.

[3] K. Roy and Sharat C. Prasad, Low-Power CMOS VLSI Circuit Design, John Wiley & Sons Inc., Canada, 2000.

[4] A. Chandrakasan, S. Sheng and R. W. Brodersen, "Low–power CMOS digital design", IEEE Journal of Solid State Circuits, Vol. 27, No. 4, April 1992, pp. 473 - 484.

[5] M. Pedram, "Power minimization in IC design: Principles and applications", ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 1, January 1996, pp. 3 - 56.

[6] L. Wei, K. Roy and Vivek K. De, "Low voltage low power CMOS design techniques for deep submicron ICs" 13th International Conference on VLSI Design, January, 2000, India, pp. 24 - 29.

[7] T. Sakurai, "Reducing power consumption of CMOS VLSI's through VDD and VTH control," Proceedings of IEEE International Symposium on Quality Electronic Design, Mar. 2000, pp.417 - 423.

[8] K. Usami and M. Horowitz, "Clustered voltage scaling technique for low-power design," Proceeding of 1995 Int. Symposium on Low Power Design (ISLPD'95), pp. 3 - 8.

[9] K. Usami, M. Igarashi, F. Minami, T. Ishikawa, M. Kanzawa, M. Ichida, and K. Nagami, "Automated low-power technique exploiting multiple supply voltages applied to a media processor", IEEE Journal of Solid State Circuits, Vol. 33. No.3 March 1998, pp. 462 - 472.

[10] K. Usami and M. Igarashi, "Low-power design methodology and applications utilizing dual supply voltages", Proceedings of the ASP-DAC 2000, pp.123 - 128.

[11] C. Chen, A. Srivastava and M. Sarrafzadeh, " On gate level power optimization using dual-supply voltages", IEEE Transactions on VLSI Systems, Vol. 9, No. 5 October 2001, pp. 616 - 629.

[12] F. Ishihara, F. Sheikh and B. Nikolic, " Level conversion for dual-supply systems", IEEE Transaction on VLSI systems, Vol. 12 No. 2, February 2004, pp. 185 - 195.

[13] Y. Yeh, S. Kuo and J. Jou, "Converter-free multiple-voltage scaling technique for low power CMOS digital design", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Vol. 20, No. 1 January 2001, pp. 172 - 176.

[14] T. Kuroda, K. Suzuki, S. mita, T. Fujita, F. Yamane, F. Sano, A. Chiba, Y. Watanabe, K. Matsuda, T. maeda, T. Sakurai and T. Furuyama, "Variable supply-voltage scheme for low-power high-speed CMOS digital design", IEEE Journal of Solid State Circuits, Vol 33, No. 3. March 1998, pp. 454 - 462.

[15] H. Kawaguch, G. Zang, S. Lee, Y. Shin and T. Sakurai, " A controller LSI for realizing V_{DD}-hopping scheme with off-the-shelf processors and its application to MPEG4 system", IEICE Transactions on Electronics, Vol. Ess-C, No. 2 February 2002, pp. 263 - 271.

[16] L. Wei, Z. Chen, K. Roy, M. Johnson, Y. Ye and V. De "Design and optimization of dual-threshold circuits for low-voltage low-power applications" IEEE Transactions on VLSI , Vol. 7, No. 1, March 1999, pp. 16 - 24.

[17] P. Pant, R. Roy, and A. Chatterjee "Dual-threshold voltage assignment with transistor sizing for low power CMOS circuits" IEEE Transactions on VLSI, Vol. 9, No. 2, April 2001, pp. 390 - 394.

[18] Chris H. Kim and K. Roy "Dynamic V_{TH} scaling scheme for active leakage power reduction" Proceedings of Design Automation and Test Conference at Europe (DATE) March, 2002, pp. 163 - 167.

[19] T. Sakurai, H. Kawaguchi and T. Kuroda, "Low-power CMOS design through V_{th} control and low-swing circuits", ACM 1997, pp. 1 - 6.

[20] N. Tripathi, A. Bhosle, D. Samanta and A. Pal, "Optimal assignment of high threshold voltage for synthesizing dual threshold CMOS circuits", Proceedings of the 14th international Conference on VLSI design 2001, pp. 227 - 232.

[21] Y. Ho and T. Hwang, "Low power design using dual threshold voltage", Proceedings of ASPDAC 2004, pp. 205 - 208.

[22] K. Nose, M. Hirabayashi, H. Kawaguchi , S. Lee and T. Sakurai, "V_{th}-hopping scheme to reduce subthreshold leakage for low-power processors", IEEE Journal of Solid-State Circuits, Vol. 37, No. 3, March 2002, pp. 413 - 419.

[23] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko and Hu Chenming, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI" IEEE Transaction on Electron Devices, Vol. 44, No. 3, March 1997, pp. 414 - 422.

[24] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, J. Yamada, "1-V power supply high-speed digital circuit technology with multi-threshold-voltage CMOS," IEEE Journal of Solid State circuits, Vol. 30, No. 8, August 1995, pp. 847 - 854.

[25] M. Anis, S. Areibi, and M.Elmasry "Design and optimization of multi-threshold CMOS (MTCMOS) circuits" IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Vol. 22 issue 10, Oct. 2003, pp. 1324 - 1342.

[26] H. Kawaguchi, K. Nose, and T. Sakurai, "A super cut-off CMOS (SCCMOS) scheme for 0.5-V supply voltage with pico ampere stand-by current," IEEE Journal of Solid-State Circuits, Vol.35, No.10, Oct. 2000, pp.1498 - 1501.

[27] K. Min and T. Sakurai "Zigzag super cut-off CMOS (ZSCCMOS) scheme with self saturated virtual power line for sub-threshold leakage suppressed sub-1V V_{DD} LSI's" ESSCIRC 2002, pp. 679 - 882.

[28] K. L. Shepard and V. Narayanan, "Conquering noise in deep-submicron digital ICs", IEEE Design and Test of Computers, Jan.-March 1998, pp. 51 - 62.

[29] X. Aragon, J. Gonzalez, F. Moll and A. Rubio, "Noise generation and coupling mechanisms in deep-submicron ICs", IEEE Design and Test of Computers, Sept.-Oct. 2002, pp. 27 - 35.

[30] H. Chen and D. Ling, "Power supply noise analysis methodology for deep-submicron VLSI chip design", Proceeding of Design Automation Conference 1997, pp. 638 - 641.

[31] H. Bakoglu, "Circuits, Interconnections and Packaging for VLSI", Addison-Wesley, 1990.

[32] P. Heydari and M. Pedram, "Ground bounce in digital VLSI circuits", IEEE Transaction on VLSI Systems, VOL. 11, NO. 2, April 2003, pp. 180 - 193.

[33] Y. Jiang and K. Cheng, "Analysis of performance impact caused by power supply noise in deep submiron devices", IEEE Design Automation Conf. Proceeding, 21-25 June 1999, pp. 760 - 765.

[34] C. Tsai and M. Marek-Sadowska, "Modeling Crosstalk Induced Delay", Proceedings of IEEE ISQED, March 2003, pp. 189-194.

[35] P. B. Sabet and F. Ilponse, ``A Model for Crosstalk Noise Evaluation in Deep Submicron Process", Proceedings of IEEE ISQED March 2001, pp. 139 - 144.

[36] Lou and W. Chen, ``Crosstalk-aware placement", IEEE Design & Test of Computers, Jan.- Feb. 2004, pp. 24 - 32.

[37] C. Chen, X. Yangand and M. Sarrafzadeh, "Potential slack: an effective metric of combinational circuit performance", Proceeding of ICCAD, Nov. 2000, pp. 198 - 201.