Chapter 4

On-chip Noise Measurement

4.1 Introduction

The continuous progress and scaling of semiconductor technology has given the ability to speed-up and increase the integration density of integrated circuits. On the other hand, the signal integrity of digital and mixed signal circuits became an issue. The power supply is being scaled down, in consequence, the power supply/ground fluctuations due to Ldi/dt and IR droop may cause a sever problem to the system performance and/or reliability. Moreover, the inductive/capacitive coupling represents an obstacle in front of increasing the operating frequency [1]. During the design phase, the information provided to the designer about these phenomena, is limited and might be inaccurate due to the lack of information about packing, full-application processing and process variation effects, and hence, the design margin has to be large to avoid the noise effects. As a result, the design cost is increased while the performance limits are still precisely undefined. No doubt that familiarity with the nature of on-chip power supply/ground, crosstalk and substrate noise will be helpful to the VLSI designer in taking these phenomena into account during the design phase of the subsequent system generation and/or precisely predicting the performance of the off-the-shelf product. There are extensive CAD works regarding the modeling/analysis of power supply/ground bounce [2-13], coupling effect [14-19] and their effects on system performance. These are to give the chip-designers the ability to find the potential problems during simulation. However, the increasing complexity and the accompanied physical phenomena in VLSI design are not completely included in

the CAD tools. Therefore, noise measurement is inevitable for accurate estimation of system performance and reliability. Since that noise signal is an analog signal, the traditional digital test methodologies [for example, automatic test pattern generation (ATPG) and built-in self test (BIST)] can not address the analog issues of high-speed design such as crosstalk noise and complex non-monotonic waveforms resulting from the inductive response of high-speed interconnect. E-beam probing is an alternative commonly available for measuring analog waveforms; however, this technique is expensive and difficult due to the need to have top-level metal available for probing, and frequently invasive due to introducing additional capacitive coupling. Moreover, the advent of systems-on-a-chip design is driving the need for testing analog blocks embedded within largely digital integrated circuits. In the next section, an over view of the previous works regarding the on-chip noise measure are presented followed by our methodology.

4.2 Overview on Previous Works

Noise on chip can be described as a wide band signal. So that it is difficult to drive this signal off chip directly and measure by using high frequency sampling oscilloscope. The parasitic elements caused by on-chip wires filter out the high frequency component of the signal. Assuming specific properties, several techniques to measure or characterize the noise signal had been presented. Most of these techniques are summarized below.

4.2.1 On-chip Sampler

The idea behind the sampling technique is to exploit the high bandwidth of MOS transmission gates by using one to sample the analog voltage on a capacitor. This voltage is then converted to a current and driven off-chip. By making the internal waveform repetitive and then sampling only once per period (or more), the bandwidth of the output signal can be allowed to be significantly lower than that

of the internal one being measured [20]. An example of a sampling circuit is shown in figure 4.1 [21]. M1-M5 make up the voltage sampler and voltage-to-current converter. A periodic signal of period T is sampled by M1-2 using an externally generated clock, which runs at a slightly different period T+Δt. M1 and M2 form a master/slave sample-and-hold circuit. A sequence of samples of the signal waveform at intervals of Δt is taken over a period of T/Δt cycles. Thus the sampler output is a time-expanded version of the signal waveform whose frequency is the beat frequency of the signal and sampling clock frequencies. PMOS M4 converts the sampled voltage into a current, which is then mirrored twice and driven off-chip. The transconductance of each sampler is calibrated by sampling an externally supplied DC voltage through M3. The on-chip sampler is an attractive idea so that it has been used, but in different ways, in many of the succeeded works [22][23]. Based on on-chip sampler idea, many circuits have been developed to measure the power supply noise signal. In [23], for example, Takamiya et al had proposed an on-chip 100GHz-sampling 8-channel sampling oscilloscope with embedded sampling clock generator.

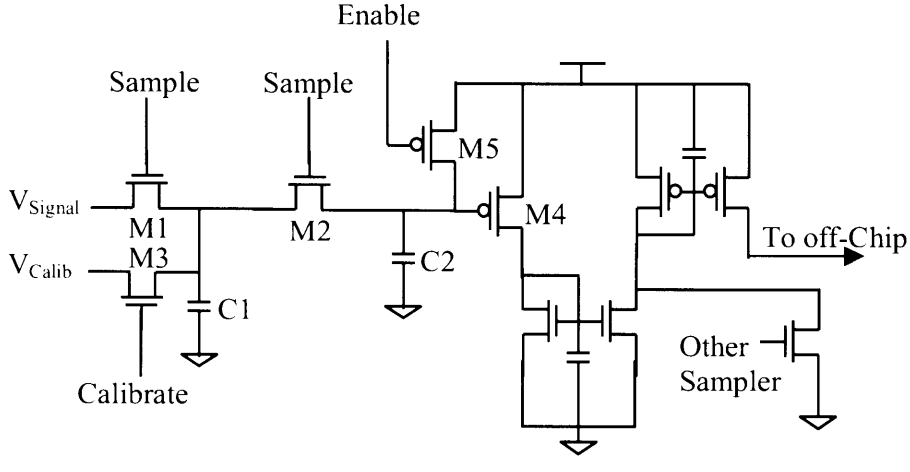


Figure 4.1 Schematic Diagram of an on-chip sampler circuit [21].

4.2.2 Analog Detection of PS/GND Noise

A different methodology to detect the power supply and ground noise in analog fashion has been proposed by Nagata et al in [24]. As shown in figure 4.2, the noise detector circuit is consisting mainly of n-channel (M1, M2) MOSFET source follower for probing power-supply wirings, and a single MOSFET common-source amplifier (g_m) M3. In addition, switch MOSFETs for shuttering by signal SHU, M4, and for selective activation by signal SEL, M5, M6 and M7 are provided. The source follower senses voltage fluctuation on the nearest digital power-supply DVDD wirings and the g_m continuously translates it to a current-mode noise signal that is transmitted on a shared current bus IBUS and then read out through a current mirror by an external oscilloscope with a termination resistor. One of the detectors sharing IBUS can be activated at a time while all the others are cut off. By changing the NMOS source follower to PMOS one, the circuit can be used to detect the ground noise.

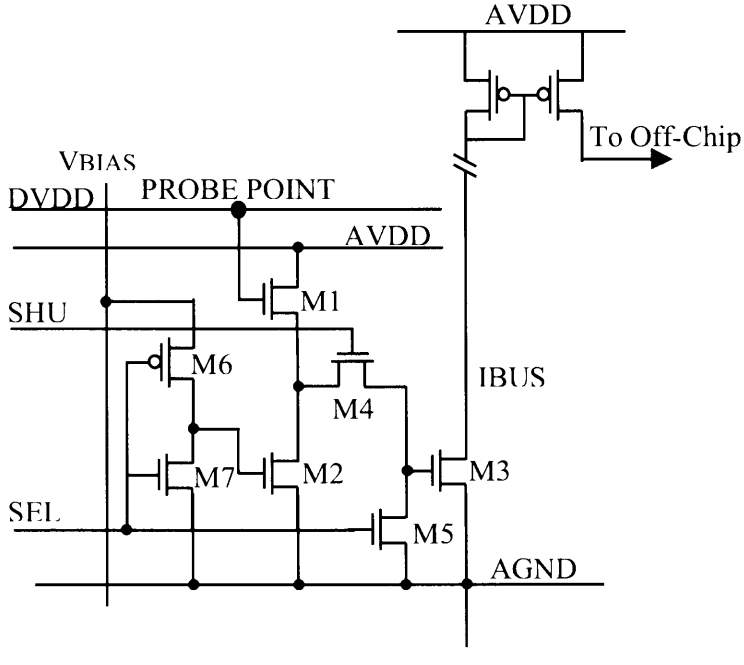


Figure 4.2 Schematic diagram of power supply noise sensing head [24].

All of the built-in noise detectors other than the digital parts were covered by deep n-type wells and isolated from a p-type substrate and supplied through AVDD/AGND wirings connected to dedicated bonding pads or sufficiently on-chip decoupled branches from common DVDD/DGND pads. An on-chip bias voltage generator is used to provide VBIAS. Only the detection head should be replicated to observe another location within the chip. The signal derived off-chip is a high frequency signal and hence a high frequency oscilloscope and special precautions should be used to avoid filtering the high frequency content of the signal.

4.2.3 Digital Detection of PS/GND Noise.

In this section, some of noise detectors based on digital fashion are explained. The merit of noise digital detection is that the detected signal can be derived off-chip without worrying about the possibility of coupling with noise. The methodologies presented here also utilize the idea of sampling oscilloscope which means that they also assume the signal is periodic. Ali et al have presented an on-die droop detector for analog sensing of power supply noise in [25]. Aoki et al in [26] had presented an On-chip voltage noise monitor for measuring voltage bounce in power supply lines using a digital tester. The block diagram of the basic idea is shown in figure 4.3. This circuit samples power supply line voltage (Vmeas) and reference voltage (Vref) and compare them. Its output (Vout) becomes high if Vmeas > Vref and low is Vmeas < Vref. The reference voltage (Vref) is supplied from off the chip.

To measure the voltage bounce waveform, Vmeas is repeatedly measured at the same timing with changing the reference voltage. Thus Vmeas is estimated form Vref when the output Vout get reversed. By changing the sampling time of Vmeas it is possible to measure the noise waveform. Takamiya et al have proposed another sampling oscilloscope macro in [27]. The macro has been

optimized to measure an overshooting /undershooting waveform caused by the on-chip inductive effect. In addition, it can be applied to detect another high-speed waveform such as the power supply noise and the substrate noise. To measure the overshooting/undershooting, a voltage-range converter has been used to reduces the measured signal's amplitude to fit within the comparator input range. A comparator compares the output of the converter and a reference voltage. In this macro, they could sample the measured signal with a cycle time of T using a sampling clock with a cycle time of T+ΔT, where the minimum ΔT is 5 ps. The sampling clock is generated on-chip by the VCO in the macro. Also, neither the reference voltage nor the control voltage for the VCO needs to be supplied from an off-chip voltage source because both are generated by D/A converters in the macro. Therefore, all the inputs and the outputs for the macro are digital signals and analog I/O is not needed. Moreover, to suppress the power supply noise from the surrounding digital LSI to the macro, an on-chip power supply noise filter is embedded in the macro; this eliminates the need for a dedicated power supply for the macro.

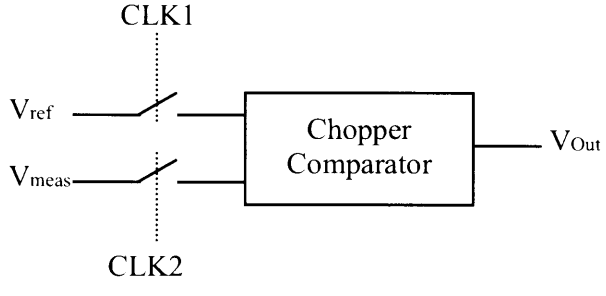


Figure 4.3 Illustrative diagram of noise digital detector.

4.3 On-Die Non-Periodic/Single-Event High Swing Noise Detector

From the pervious section, it can be noticed that the previous works are either assuming specific signal properties such as periodicity or directly probing the signal using expensive, and sophisticated monitoring tools and precaution off-chip, though, it is difficult to avoid the parasitic filtering effects. Consequently, it is difficult to apply any of the above works as a single-event high-frequency signal detector.

In this work we developed an on-chip noise sensing circuit, which is unique having the following features:

1. It does not assume specific signal properties such as periodicity.
2. It can capture a (noise) signal continuously over a specific time window with a resolution of 50 Pico-Sec.
3. By using our detector, no need to use sophisticated monitoring or expensive tools off-chip.
4. Signals having wide dynamic and frequency ranges could be detected (up to 4V in 0.18μm and band width up to 10GHz).
5. Our detector is synthesizable and the designer can flexibly adjust its main parameters.

Despite that the detector is used to measure the power supply noise of an LSI, it can be used as an interface for general on-chip high-frequency high-swing signal monitoring using conventional off-chip monitoring tools, which gives the detector another bonus as an on-chip signal monitoring circuits.

In the first trail, we have designed and tested the detector to measure a signal having frequency up to 4GHz. A modification has been done such that the detector is able to measure signals having frequencies up to 8GHz. The modified version will be discussed in the next section.

Previously in chapter three we have presented a methodology to evaluate the performance of the different CMOS low-power design schemes in presence of noise. The noise has been assumed to have a non-periodic random distribution. To complete the model, we need a circuit, which is suitable to measure either the supply voltage/ground fluctuation or cross-talk noise regardless the signal periodicity. In addition to the above-mentioned features of the proposed circuit, it is also suitable for this purpose.

4.3.1 Detector Architecture and Operation

The proposed detector has been designed to measure the noise waveforms in an LSI design. Figure 4.4 shows the block diagram of the detector. The detector is equipped with a programmable capacitive voltage divider having three tabs in order to be able to measure large and small signal fluctuations accurately. Each tab consists of two capacitors and a selection switch. The desired tab is connected to the input buffer by closing the corresponding switch and opening the others. The dividing ratios of the tabs are 6/7, 2/5 and 1/7 respectively. The measured signal is coupled to the sampling node by capacitor and leveled by the input buffer. The first trail of the detector is designed such that it samples the input signal over around 10 ns time window with a resolution of 100 ps. The capturing time window can be narrowed/widened by decreasing/increasing the number of samplers as it is explained later. The signal is sampled during the capturing time window and stored by sample and hold array. The stored signals are then multiplexed to produce the output signal. The multiplexing rate can be controlled by choosing the clock frequency such that the bandwidth of output signal fits within the frequency band of the monitoring tools off-chip and also to make it less than the cut off frequency of parasitic low pass filter, which is resulted from the capacitive and inductive response of on-chip interconnects and bonding wires.

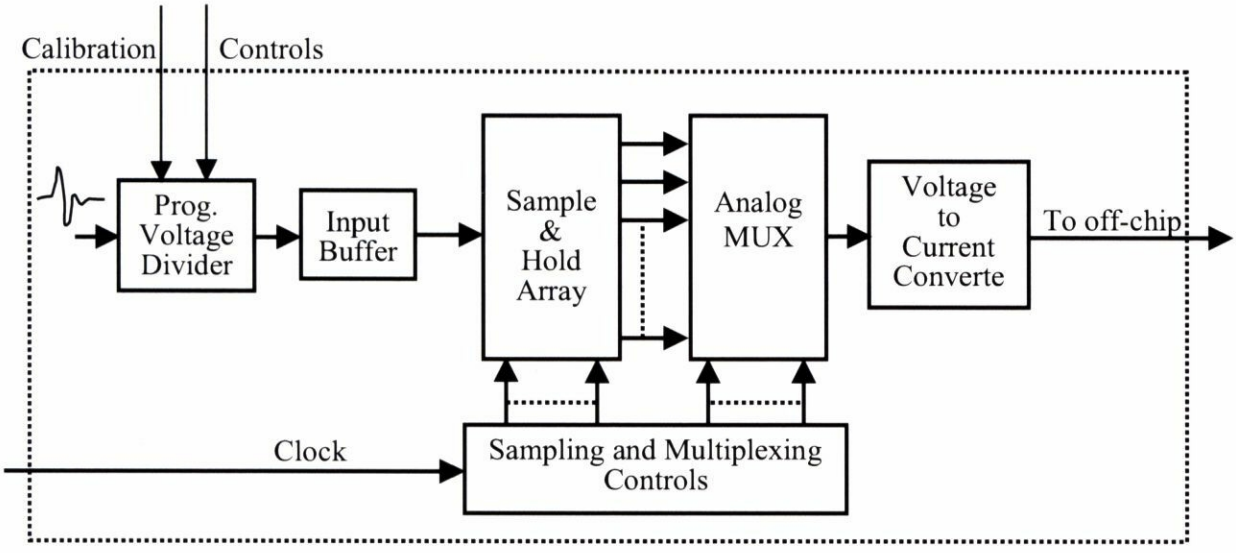


Figure 4.4 Block diagram of the detector.

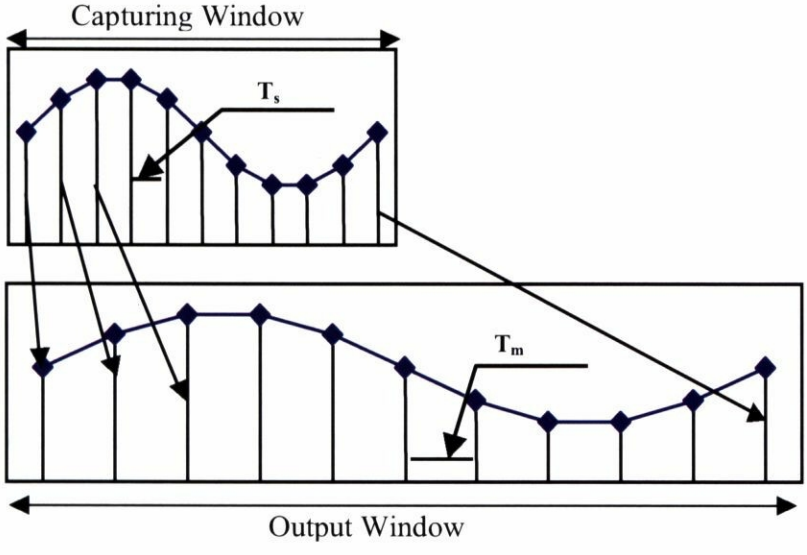


Figure 4.5 Example of the input and output signals.

The sampling and multiplexing processes can significantly lower the bandwidth of the measured signal by the ratio T_m/T_s. Where T_s is the sampling interval and T_m is the multiplexing time interval. Figure 4.5 explains the theory of

operation of the detector. It is clear that the output signal is a time-expanded version of the measured signal. For better immunity, the signal produced by the analog MUX is fed to a voltage to current converter and then driven off chip. For convenient control of the output channel bandwidth, the clock is fed from off-chip. The ratio T_m/T_s can be adjusted freely as long as it the multiplexing time is less than the retention time of the holding capacitor. The retention time consideration is discussed later in this chapter.

4.3.2 Input Buffer

The role of the input buffer can be summarized in three points. First, it isolates DC voltage of the probed node from the sample and hold (S&H) array, so that the sampling pulses do not disturb the probed node. Second, it supplies an adequate current to charge the holding capacitor within the sampling time. Third, it helps adjusting the signal being sampled to a suitable range such that it can be sampled by S&H circuit. Figure 4.6 shows the schematic diagram of the input buffer. The transistor M1 is biased by applying a short pulse (biasing pulse) on the gate of M3 before starting the sampling process. Therefore the voltage of N1 is charged to V_{DD}-V_{th3} where V_{th3} is the threshold voltage of M3. M4 is added to prevent N1 from clamping to V_{DD} by the effect of leakage current through M3. To ensure the quiescent voltage of N1, M4 is turned on (by applying a discharging pulse to its gate) for a short time before applying the biasing pulse. The timing of biasing and discharging pulses is also shown in figure 4.6. The bias level of the divider output (N1) is V_{DD}-V_{th3}. Then, the threshold voltage of M1 lowers the bias level further so that simple S&H circuit can capture the signal. This configuration is referred to as detector I. M3 and M4 can be replaced by R1 and R2 respectively as shown by dotted lines in figure 4.6. This guarantees fixed biasing voltage at N1. However, it costs area overhead, increases power consumption and raises the minimum frequency that can be sensed by the circuit. The configuration in this

case will be referred to as detector II. Both cases are investigated in this work. The buffer is designed such that the bandwidth is larger than 10GHz. The frequency response of the buffer is shown in figure 4.7.

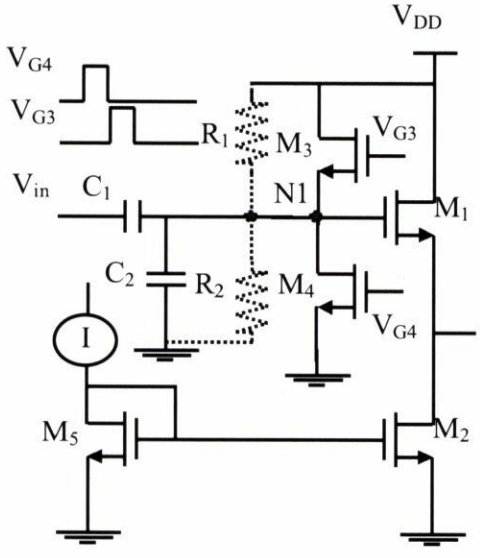


Figure 4.6 Schematic diagram of the input buffer.

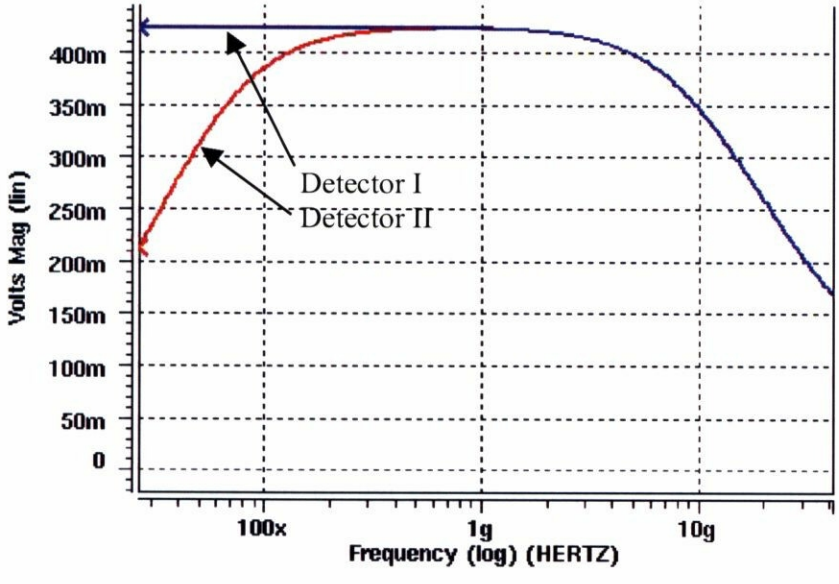


Figure 4.7 Frequency response of the input buffer (simulation).

4.3.3 Sample and Hold Array

The sample and hold circuit is built by using NMOS sampling switch and capacitor as shown in figure 4.8. The sampling speed and accuracy are important parameters in this circuit. To maximize the sampling speed, first; the swing of input signal is made low such that the driving voltage (V_G-V_A) of the switch M_S is high enough to ensure low r_{SD}. Second; the NMOS width and the holding capacitor size are optimized to minimize the circuit time constant and clock feed through. The input range to the sampler is set to (0.1 ~ 0.8 V) by the divider and the input buffer. The feed through is checked by simulation and it is found that the feed through is ranged from 23mV to 25mV over the mentioned input range. Since the clock feed through is almost constant over the S&H array, it can be processed as a DC offset voltage and taken into account during calibration. Therefore, it is not a vital problem in this design. Each S&H cell is followed by PMOS buffer, shown in figure 4.8, to isolate the corresponding sample from the multiplexing capacitor to ensure that the multiplexed samples are independent of each other. The buffer also raises the sample to a level suitable to drive the input stage of the voltage to current converter. The PMOS buffer consists of two PMOS transistors. One is a driver and is connected to the holding capacitor and the other serves as active load with current mirror.

4.3.4 Analog Multiplexer

The role of analog MUX is to construct the low bandwidth signal from the buffered samples. It consists of an array of switches. Each switch in the array is an NMOS transistor and is connected to the buffered outputs of S&H array as shown in figure 4.8. The switches are turned on sequentially at a given frequency to compose a signal that has lower bandwidth than that of the measured signal. For better immunity, the output voltage is then converted to current and driven off-chip. The voltage to current converter circuit is similar to that used in [21]. The

feed through due to the multiplexing process has been studied by simulation. The results have shown that the feed through difference between the lowest and highest values of the input range is 15mV, which is considered within the accuracy of the detector.

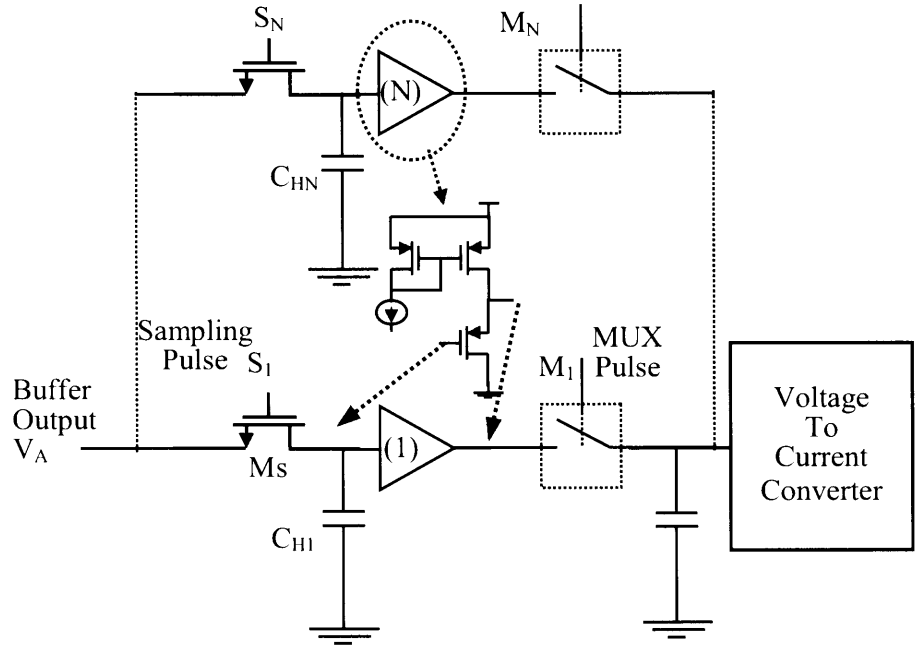


Figure 4.8 Schematic diagram of sample and hold and multiplexing cells. The buffer is PMOS buffer.

4.3.5 Sampling and Multiplexing Controls

The sampling and multiplexing control block comprises digital logic to generate the sampling and multiplexing pulses. As shown in figure 4.9, the block starts with pulse generator. The pulse generator is a digital logic consisting of frequency divider and AND gates to generate one pulse every cycle time. The pulse is fed to a delay line to generate the sampling pulses. To increase the sampling pulse width without decreasing the sampling frequency, we designed the sampling pulses generator such that three sampling pulses are overlapped. In this way, we realized enough sampling time more than the time-constant of the

sampler in order to avoid the hysteresis effect of the sampler. The sampling pulse generator has been built as shown in figure 4.10.

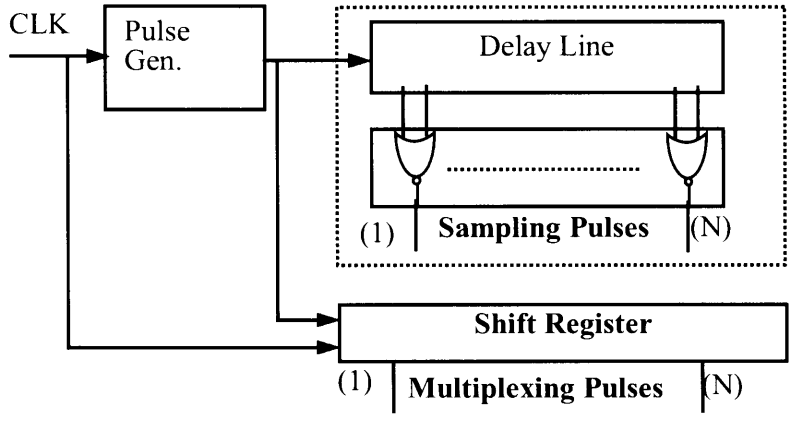


Figure 4.9 Block diagram of the sampling and multiplexing pulses generator.

The generated pulses are positive going pulses, which are suitable to control a simple S&H circuits. However the sampling interval is limited to the delay of two successive inverters, which is 100 Pico-seconds in this case. Note that the sampling pulse width is independent of the clock frequency. The generated pulse and the clock are fed to a shift register to generate the multiplexing (MUX) pulses. The MUX pulse width is equal to the clock period, which means that the multiplexing time is controlled by the clock frequency and hence the user can flexibly adjust the bandwidth of the output channel. It is important to note that the MUX time is limited by the retention time of the holding capacitor. The timing diagram of sampling and multiplexing pulses are shown in figure 4.11-a, b respectively.

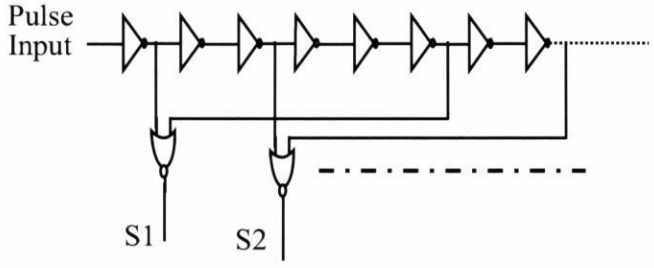


Figure 4.10 Logic diagram of the sampling pulses generator.

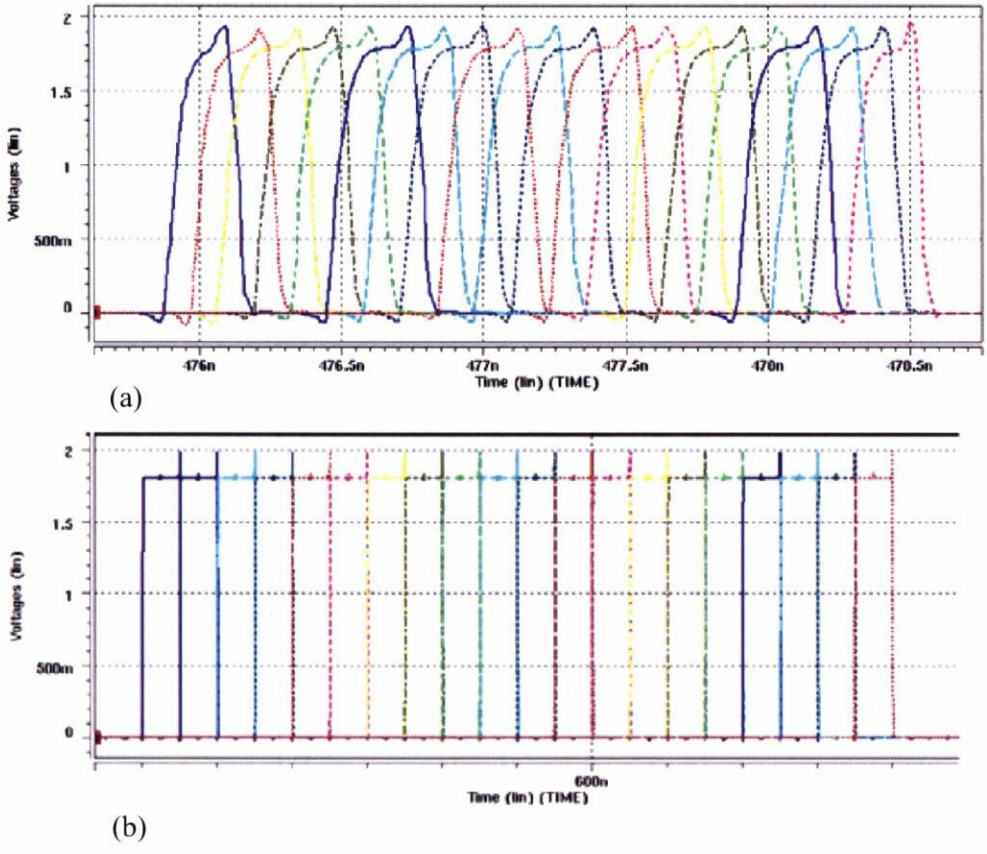


Figure 4.11 The timing diagram of (a) sampling pulses (b) Multiplexing pulses.

4.4 Test Chip Configuration

To examine the noise detector, a test chip has been designed using Hitachi 0.18μm technology. The detector is used to measure the power supply noise of a

noise generation circuit. The noise generation circuit comprises 5K gates CMOS inverter. It consists of four blocks as shown in figure 4.12. To obtain various noise levels, the activation of any of the four blocks is controlled from off-chip. The power supply voltages are supplied separately to the detector circuit and noise generation circuit. The detector circuit is also isolated from the noise generation circuit by using a guard ring. The detector has been replicated to check the effect of using biasing resistance instead of biasing transistor with and without the voltage divider. An on-chip decoupling capacitor (150 pf) is used to guarantee the integrity of the detector supply voltage line.

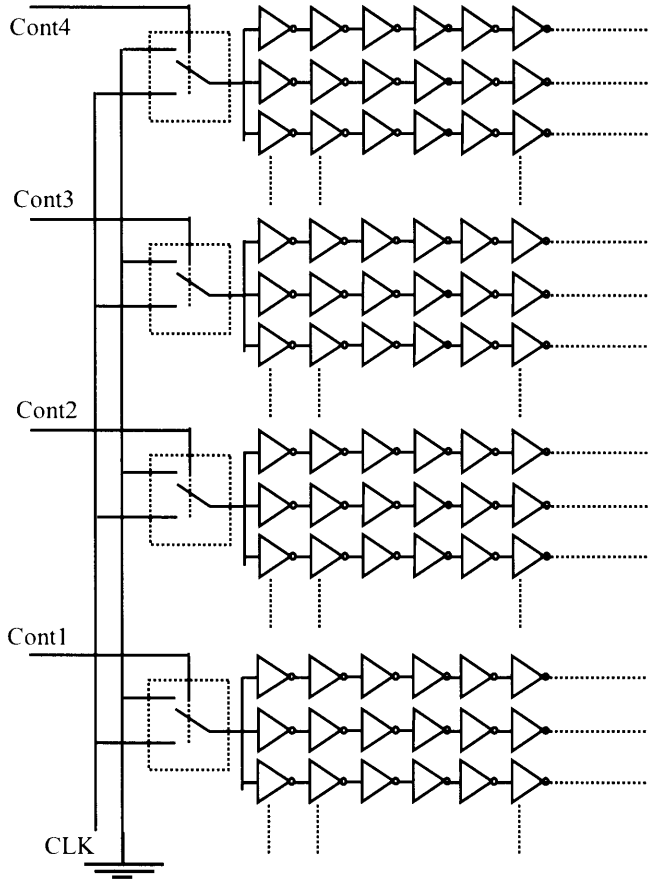


Figure 4.12 Schematic diagram of the noise generation circuit.

The layout of the test chip is shown in figure 4.13.

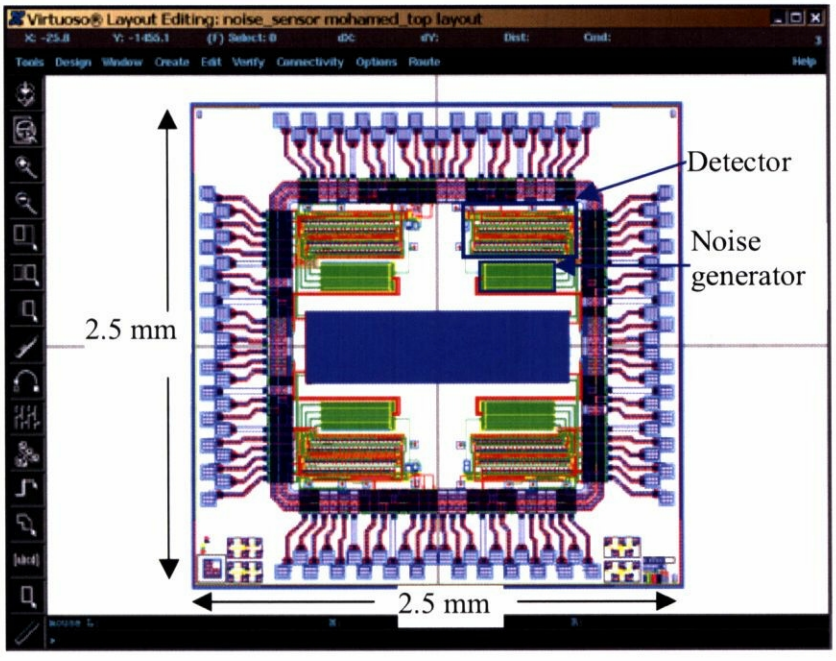


Figure 4.13 Test chip layout.

4.4.1 Simulation Results

Each detector in the layout is extracted individually as well as the whole design. The extracted netlists have been simulated using HSPICE. First, both detectors are fed by a synthetic noise signal. As it was mentioned earlier, the detector is designed such that the capturing time window is 10nSec and Tab 2 of the capacitor voltage divider is chosen. The output of voltage to current converter is terminated by a resistor of 100Ω shunted with a 10pf capacitor. The signals at the probing point (tstin), divider output (in1), buffer output (out1) and the detector output (out) of detector I are shown in figure 4-14-a, b, c and d respectively. Those of detector II are shown in figure 4-15-a, b and c respectively. Figures 4.16 and 4.17 show the simulation results of detector I and II respectively at tab3. The figures show that the detector is capable to detect fluctuations up to 4V.

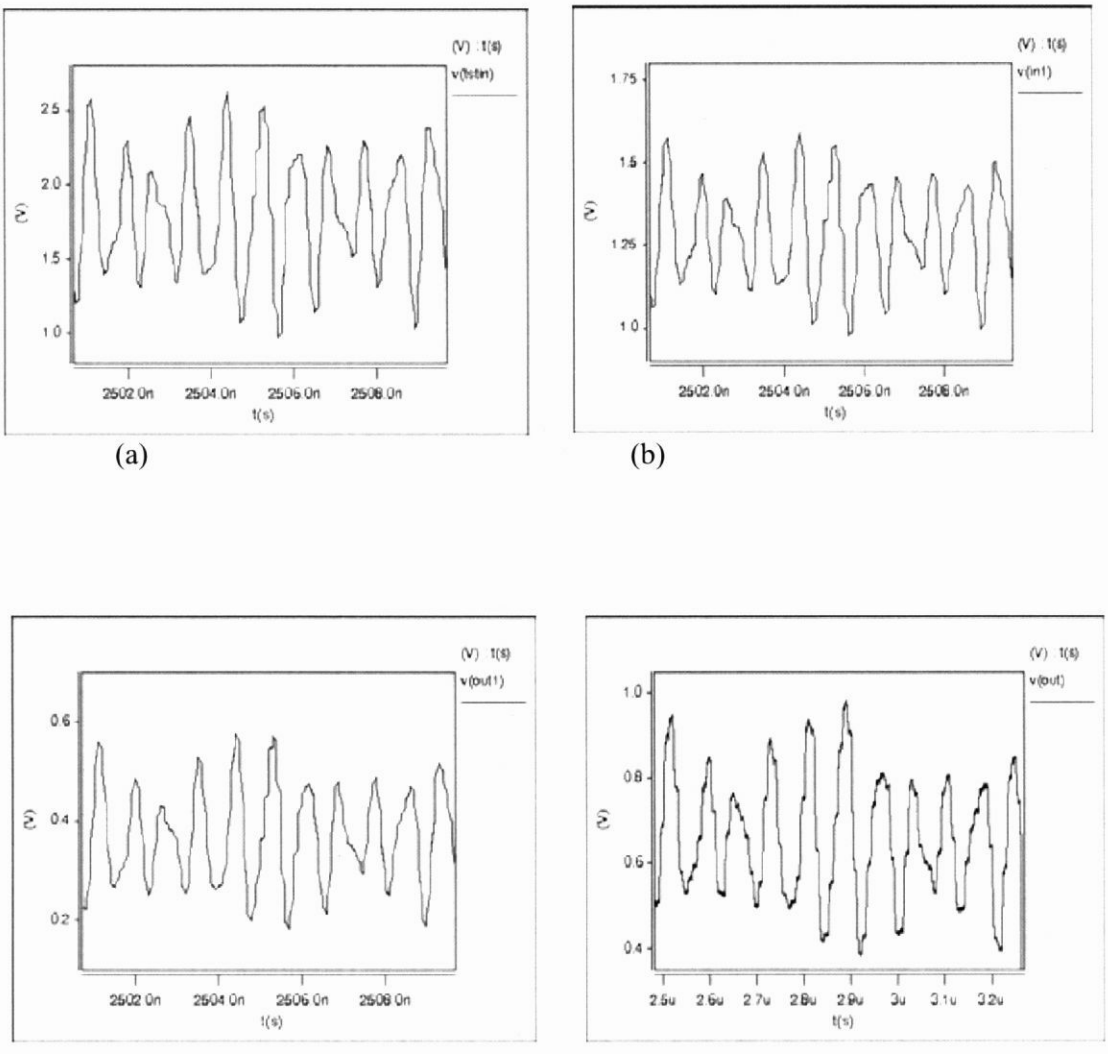
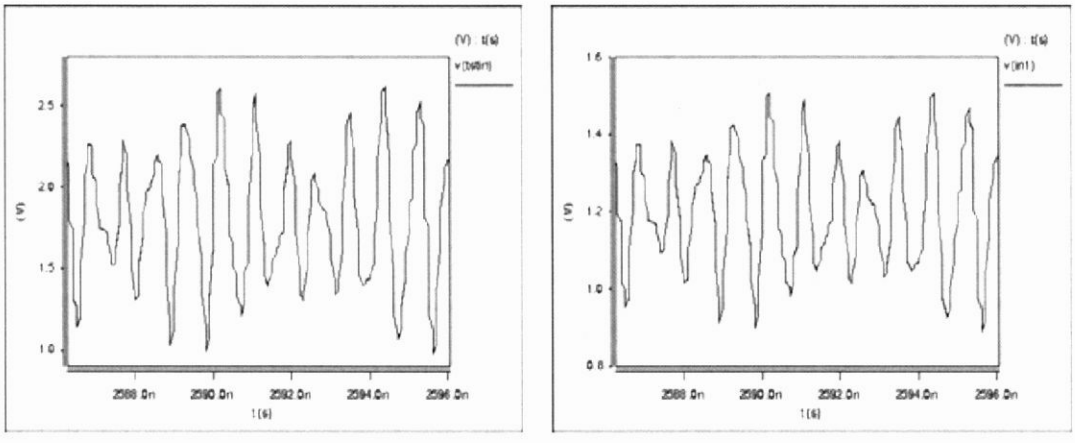
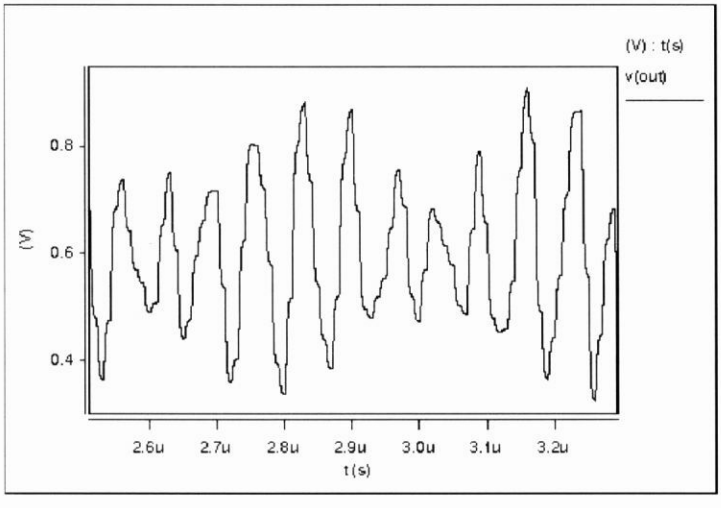


Figure 4-14 Simulation results of Detector I at tab 2. (a) Probing point signal (b) Output of the voltage divider (c) Buffer output (d) Detector output.



(a) (b)



(c)

Figure 4-15 Simulation results of Detector II at tab 2. (a) Probing point signal (b) Output of the voltage divider (c) Detector output.

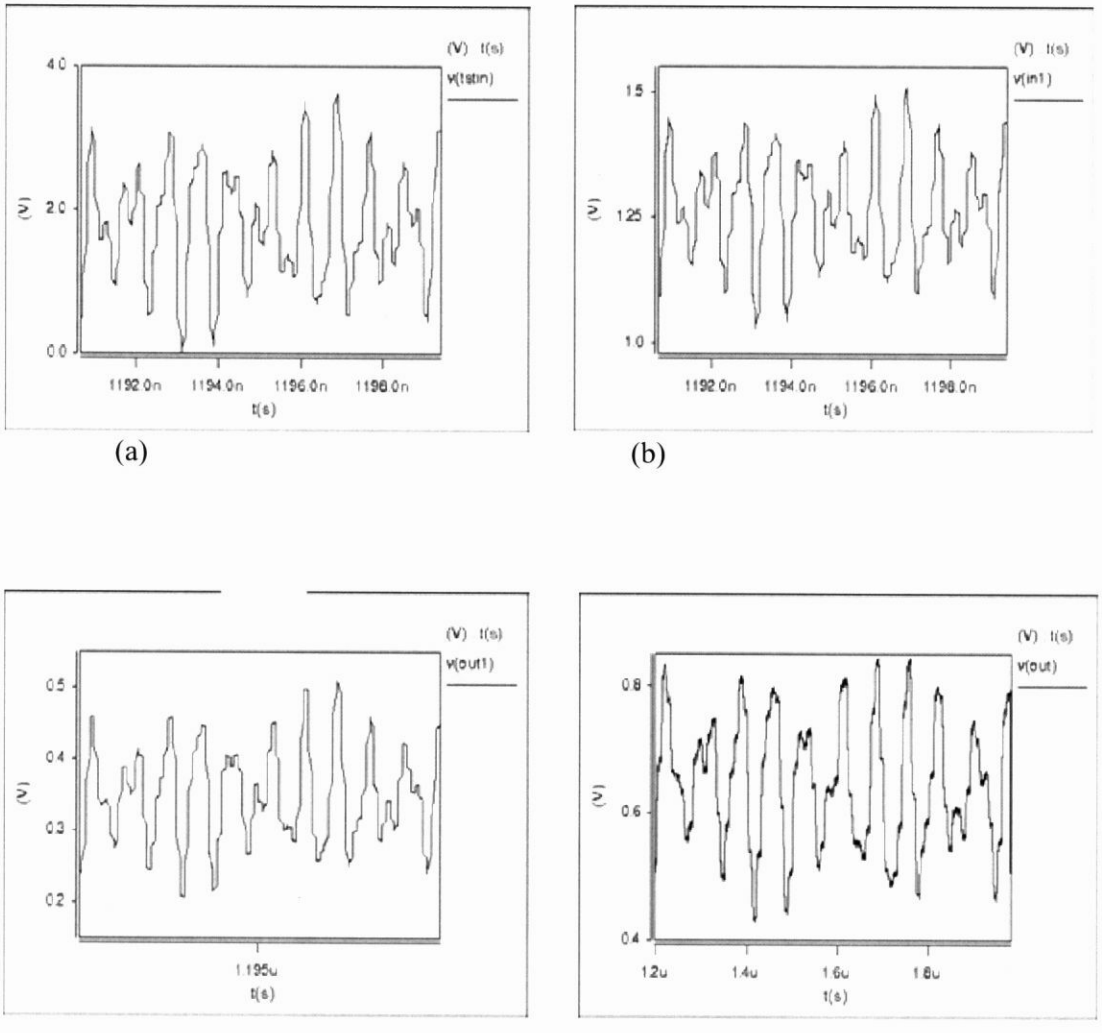
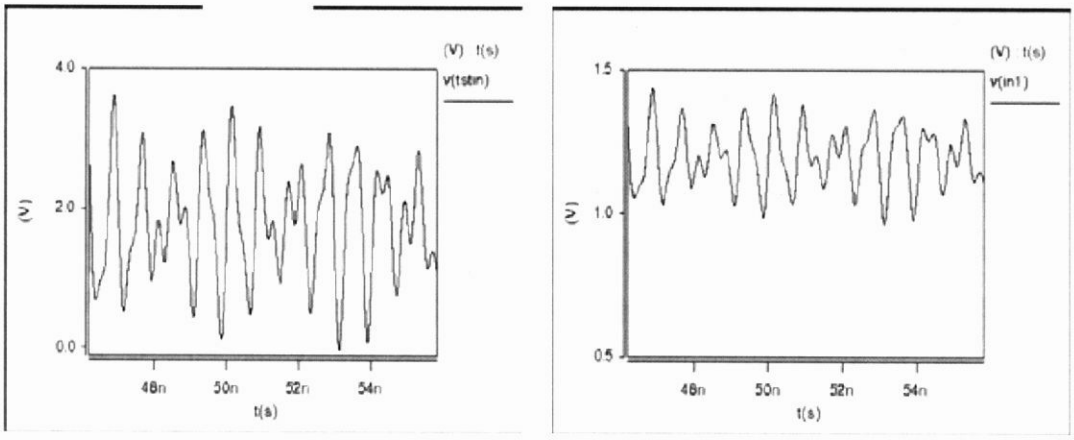
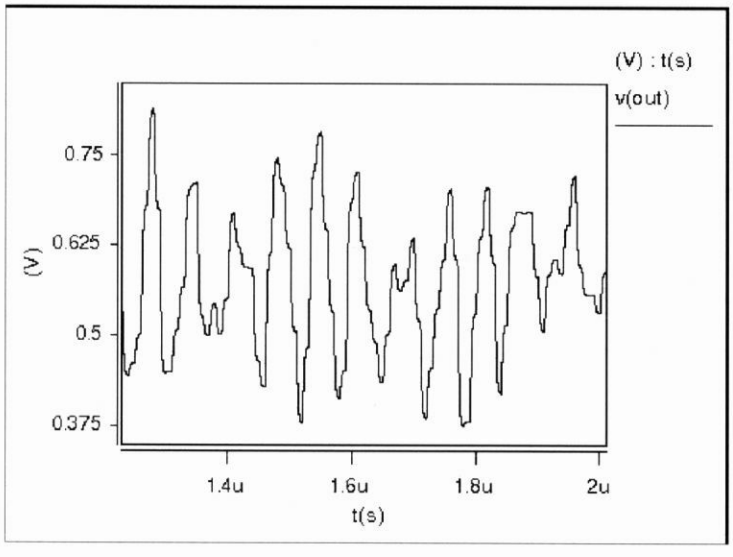


Figure 4-16 Simulation results of Detector I at tab 3. (a) Probing point signal (b) Output of the voltage divider (c) Buffer output (d) Detector output.



(a) (b)



(c)

Figure 4-17 Simulation results of Detector II at tab 32. (a) Probing point signal (b) Output of the voltage divider (c) Detector output.

Second, the extracted circuit of the detector I and II and the noise generation circuits are also simulated. During the simulation of the detector with the noise generation circuit, the detector and noise generation circuit are fed by clock signal having frequency 100MHz and fully activated. To test the accuracy of the detector, the noise generation circuit is disabled by setting the inputs of the four blocks to ground. Then, the supply voltage of noise generation circuit is measured. Figure 4-18 shows the output of input buffer (upper graph) and the detector's output (lower graph). The results show that the output contains small fluctuations (less than 30mV) due to the difference in parasitic capacitance of the wiring among the samplers.

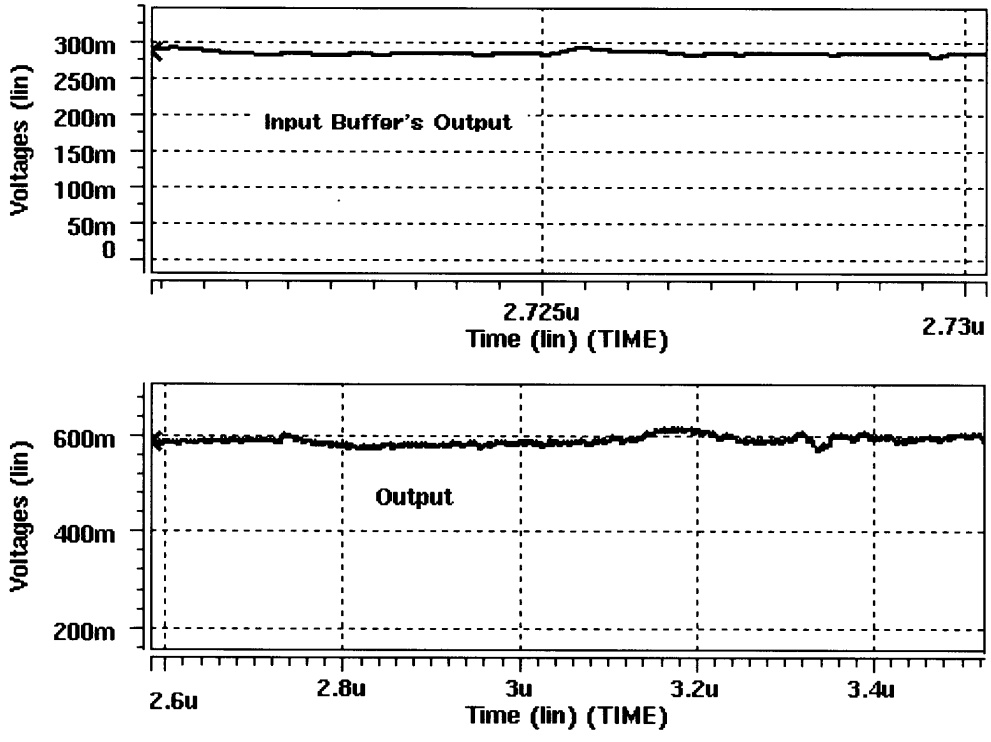


Figure 4-18 The simulation results of detector I at tab 2 when the probing point is quite. The input (upper graph) and output (lower graph).

The parasitic inductance of noise-generator's supply line is estimated to be 5nH. The detector with the noise generation circuit is simulated. Figure 4-19 shows the input and output of detector I when the noise generation circuit is fully activated, while figure 4-20 shows the input and output of detector II. The noise peaks are generated at the clock edges. The amplification/attenuation factor of the input/output ratio can be measured during the calibration and hence the original signal level can be recorded as it will be explained in the next subsection. The sampling speed in this design is adjusted to 10G sample/sec and is confirmed by simulation.

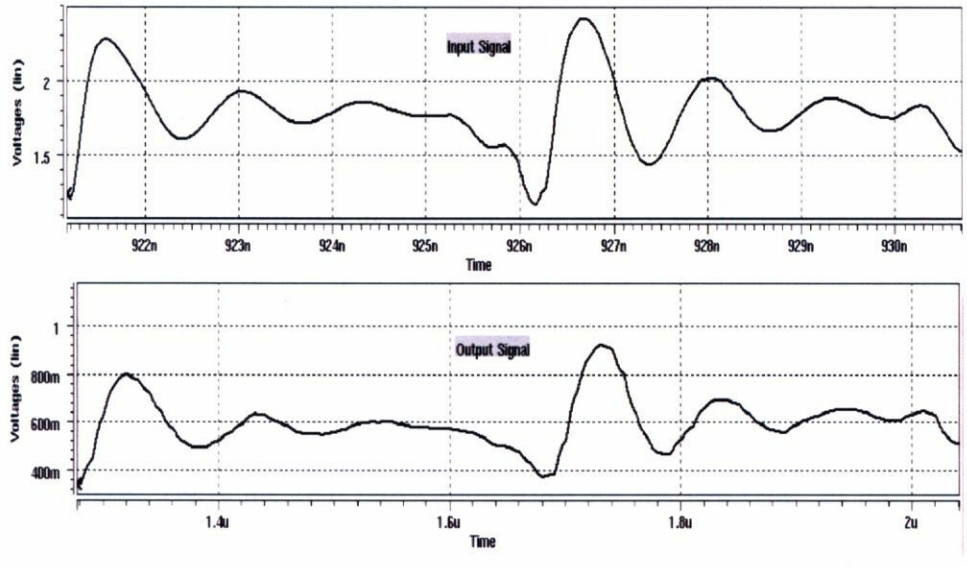


Figure 4-19 Power supply bounce of the noise-generation circuit. Probing node voltage (upper graph), Detector I output (lower graph).

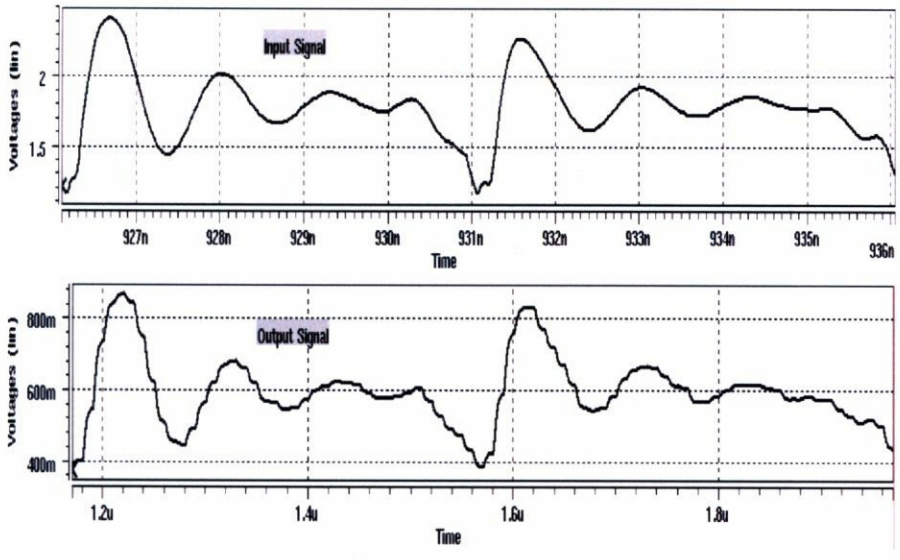


Figure 4-20 Power supply bounce of the noise-generation circuit. Probing node voltage (upper graph), Detector II output (lower graph).

4.4.2 Measurement Setup

One of the good features in this design is that, it needs neither sophisticated monitoring tools nor high-frequency measurement precautions off-chip. Although the detector is used to measure a high frequency signal, a conventional oscilloscope is enough to monitor the signal. Figure 4-21 show the measurement setup of the test chip. HP digital tester is used to generate the required clock and control signals. There are two fabrication trials for the test chip. In the first trial, the clock signal is common between the detector and noise-generation circuits, while in the second the clock of the detector is separately fed form the input signal of the noise-generation circuit. The captured time-window is 10nSec. It can be made wider/narrower by change the number of samplers. The clock frequency is chosen such that the bandwidth of the output channel is two orders of magnitude less than that of the input signal

In the following subsection, the measurement results of both trials are presented.

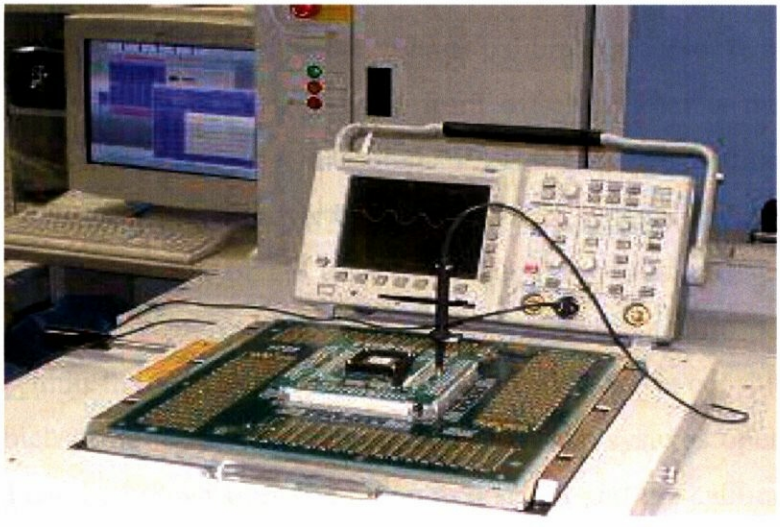


Figure 4-21 Test-chip measurement setup.

4.4.3 Measurement Results

Figure 4-22 shows the micrograph of the fabricated detector. The detector size is 640X270 μm. in fact the detector area, A, can be expressed by the following equation:

$$A = \alpha + n\beta$$

Where α is the fixed (basic) area, β is the area of one segment of figure 4-8 including the area of digital part needed for generation of the sampling and multiplexing controls and n is the number of samplers.

In our design, α and β are equal to 12460 and 1160μm^2 respectively. The detector consumes average current about 20mA at 2V operating voltage. The

fabricated chip is tested by HP93000 logic tester and the output is monitored by a conventional oscilloscope. The input-output transfer characteristic is measured by operating the detector as an on-chip sampling oscilloscope and applying a low frequency sine wave (6.5 MHz). The input is plotted versus the output as shown in figure 4-23, which is an example of the voltage calibration curve. Note that it is difficult to apply a high frequency signal from off-chip. That is the effect of parasites may result in inaccurate measurement. The noise generation circuit is fully activated by connecting all inverter chains to a clock signal having frequency 100MHz. The power supply of the noise generation circuit is measured by the detector. The detector captures time-windows triggered at specific points every time. Hence, within the capturing time-window, the detector is capable to report the events, which need not to periodically happen during systems operation. The original signal can be known from the monitored signal and the calibration graph shown in figure 4.23 in addition to the ratio T_m/T_s. To obtain the original signal, the time axis of the monitored signal is divided by the ration T_m/T_s and the value axis (vertical axis) is multiplied by the amplification/division ratio extracted form the calibration graph. In this work, the ratio T_m/T_s is measured by injecting a signal with known frequency. From the output signal, number of samplers and the output time-window, the ratio T_m/T_s can be measured. An example of the original detected noise signal is shown in figure 4-24. It is clear that the parasitic elements (inductance and resistance) are under-estimated during the simulation. To show the ability of the detector to capture the non-repeated events, the activation signal of noise-generation circuits is made different form capturing window to anther such that the generated noise signal is different each measurement cycle. Figure 4-25 shows an example of the captured signal. The signal is not calibrated in the vertical direction.. Figure 4-25 shows three successive capturing windows.

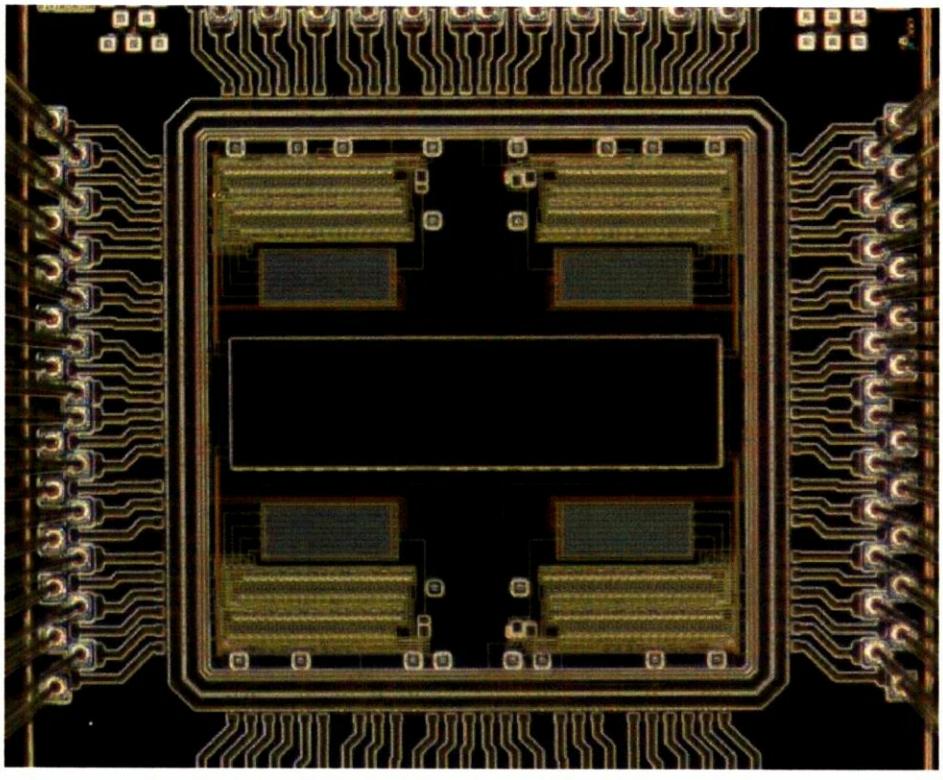


Figure 4.22 Micrograph of the test chip.

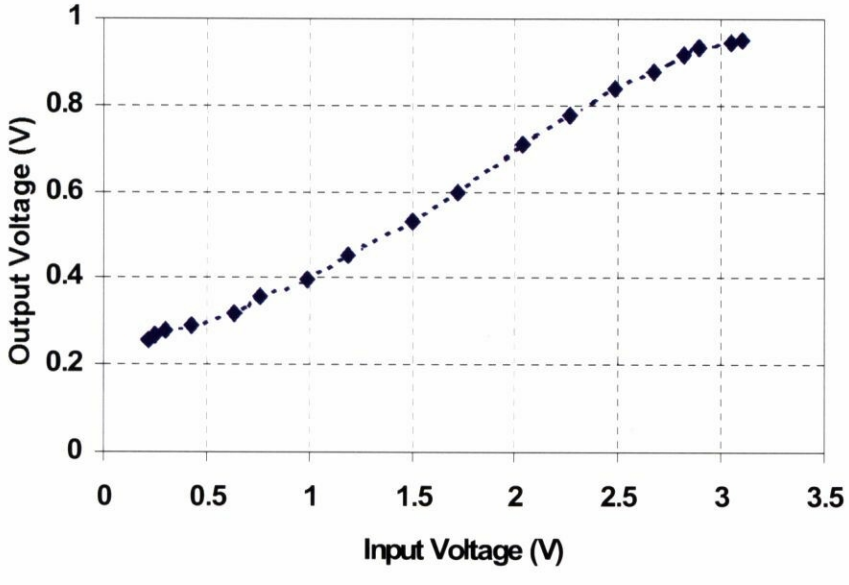


Figure 4.23 Transfer characteristics of detector I at tab 2 (2/5 division ratio).

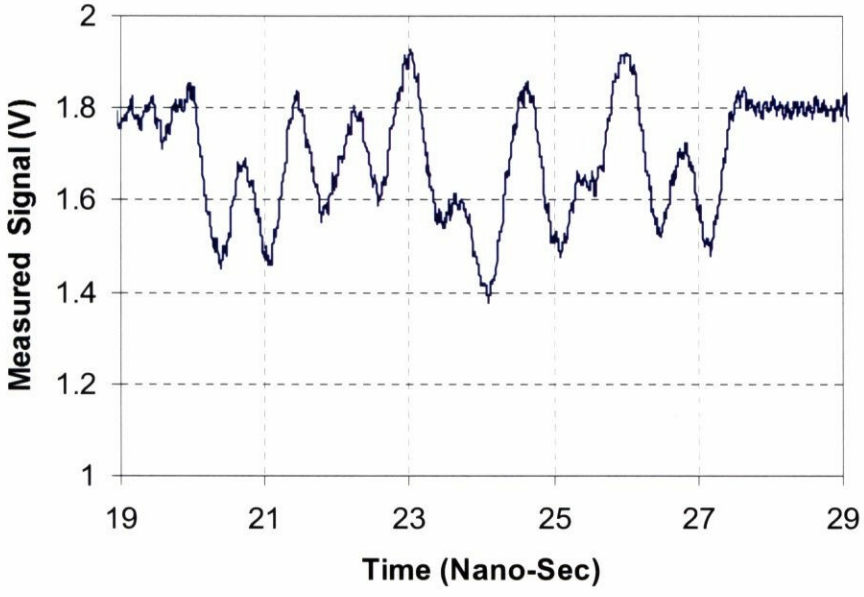


Figure 4.24 The measured power supply noise.

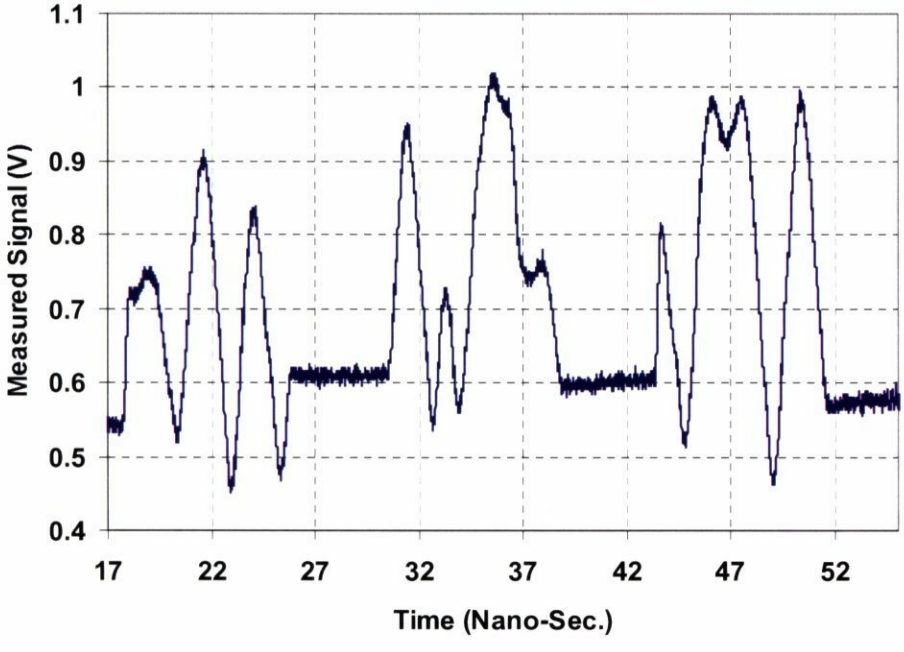


Figure 4.25 The measured power supply noise. (the vertical axis is not calibrated).

4.5 Accuracy Issues and Solutions

4.5.1 Fixed Pattern Noise

At zero input (noise circuit is quite), the output shows some fixed pattern noise (FPN) as shown in figure 4.26. The major reason for the fixed pattern noise is due to the fluctuations of the threshold voltage of PFETs in the S&H outputs and sampling and multiplexing switches. The effect of area variations of the sampling switches has been investigated by simulation and it is concluded that those variations have a negligible effects on the accuracy of the detector. Furthermore, the detector layout is done such that the switching events in the digital part do not affect the operation of the analog part. The clock, which controls the detector operation, has a possibility to share in generating such fixed pattern noise. However, to alleviate such effect, the power lines are made wide enough to ensure low parasitic resistance and inductance and hence the effects of the input clock and the control pulses generations on the detector accuracy are negligibly small. To check the periodicity of the noise pattern shown in figure 4.26, the autocorrelation of the signal has been calculated as shown in figure 4.27. The autocorrelation result shows that more than 80% of the noise pattern is periodic and can be removed as it is discussed later in this section and less than 20% is random, which is difficult to remove and is considered as the accuracy limit of the detector. In order to overcome the fixed pattern noise, there are two solutions.

1. Remove the PMOS buffers from the design. However in such case, the holding capacitor should big compared with multiplexing capacitor in order to make the multiplexed pulse independent of each other.
2. Modify the detector circuit according to figure 4.28. Using this modification, the FPN is removed by a way similar to the correlated double

sampling method [29] where the output is independent of V_{thp}. T_P is the active part of the measurement cycle where the sampled signals are being multiplexed. The switch S_{OUT} is controlled by a clock signal (CK) during the time T_P. CK should be synchronized with the MUX pulses M2, M4, M6,.etc. Since both MUX pulses and CK are generated from the input clock, it is easy to make such synchronization.

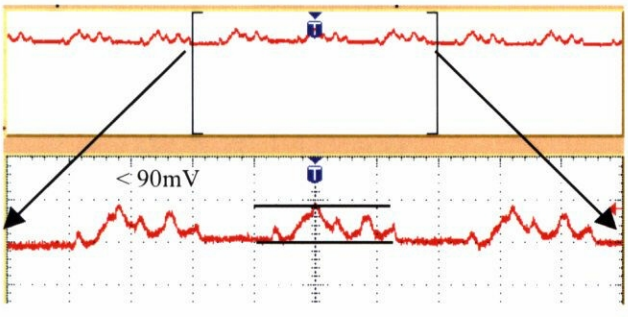


Figure 4.26 The measured output fixed pattern noise.

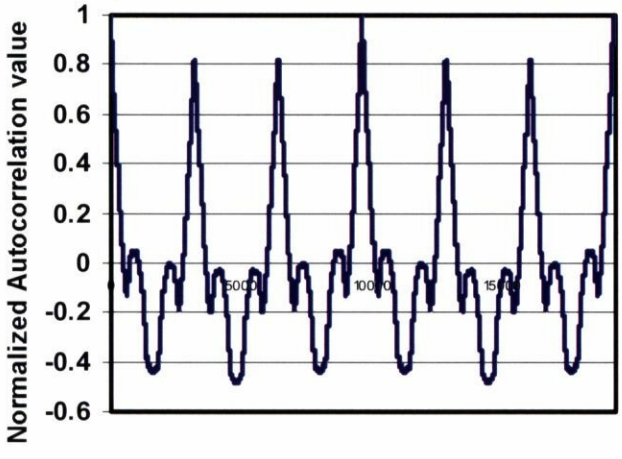


Figure 4.27 Autocorrelation of the noise pattern.

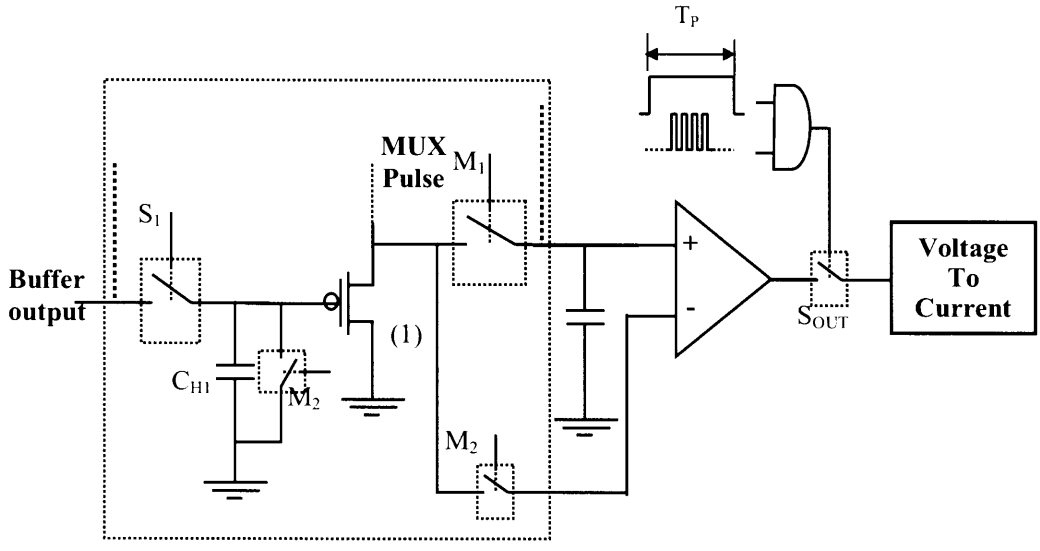


Figure 4.28 The proposed scheme for canceling the fixed pattern noise.

4.5.2 Retention Time

As it is mentioned earlier, the multiplexing time can be chosen freely by the user through controlling the frequency of the input clock. The limitation is the holding capacitor retention time- the time within which the capacitor can hold the charge. One of the limiting factors of retention time is the gate leakage. The holding capacitor is connected to the PMOS buffer as shown in figure 4.29. If the leakage through the gate insulator of the driving transistor is big, the retention time might be an issue. Since the gate insulator is scaled down with the global technology scaling, It is worth to investigate the effect of gate leakage on the retention time. The gate leakage has been studied in [30]. The data is extracted and used. The retention time is calculated according the following equation. Where t is the retention time, C_H and W are assumed to equal to 20ff and 1μ respectively. L_{min} is the minimum channel length and it is assumed according to the technology

node. ΔV is the error in the stored voltage and it is assumed to equal to 10mV and i is the leakage current through the gate insulator. The retention time versus the technology nodes is plotted in figure 4.30.

$$t = \frac{C_H \Delta V}{i}$$

$$i = L_{\min} \times W \times J$$

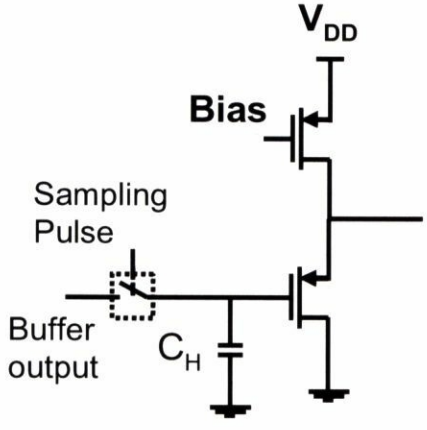


Figure 4.29 Connection of S&H to PMOS buffer.

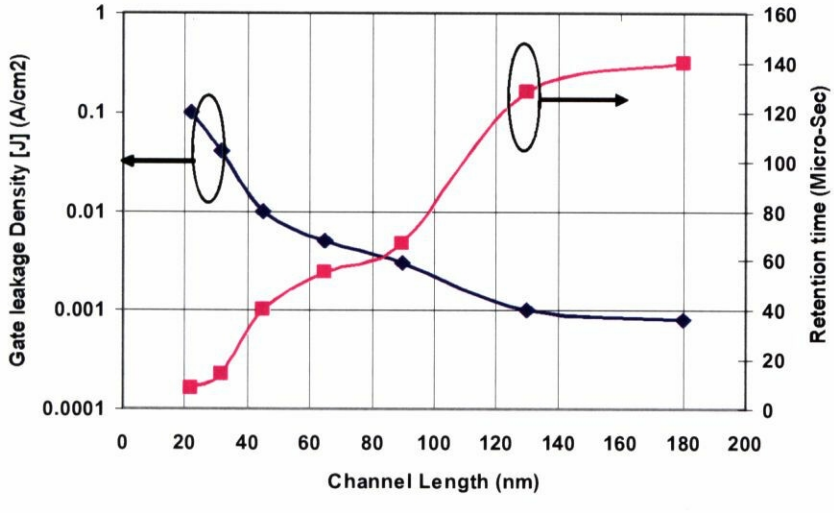


Figure 4.30 Leakage current and retention time versus technology nodes.

Figure 4.30 reveals that the detector will work correctly in even in the ultra scaled technology. The retention time in 20nm technology is about 6μSec. which means that the cycle can be extended to 6μSec. in other words, if the capturing time window is 10nSec and it is processed in 5μSec, the frequency of the captures signal is down 500 times.

4.6 High Speed Non-periodic Signal Detector

The previous version of the detector has been designed such that the sampling interval is 100pSec. The sampling pulse generator is designed by using delay line as shown in figure 4.10. The sampling pulses are separated in time by the delay of two successive inverters, which explains the reason behind the value of the sampling interval. In the high speed detector, the sampling pulses and the S&H circuits have been modified to duplicate the sampling rate.

4.6.1 Sampling Controls

The sampling pulse generator in the new design is modified such that the sampling interval is equal to the delay of one inverter. In this way, the sampling rate is two times as that of the previous version. The addition of NAND gates between the NOR gates generate a signal, which can be used to sample the probed signal once between each two samples of the previous design. The lifted area between each two NOR gated have been utilized to inset the added NAND gate and hence, there is no penalty coming form area overhead for this part. Figure 4.31 show the schematic diagram of the new sampling pulse generator. The successive sampling pulses are negative/positive and positive negative going pulses respectively as shown in 4.32. Since the successive pulses are of different timing format, the sampling and hold circuit should be changed to be suitable for the new pulses. The next subsection explains the new S&H circuit.

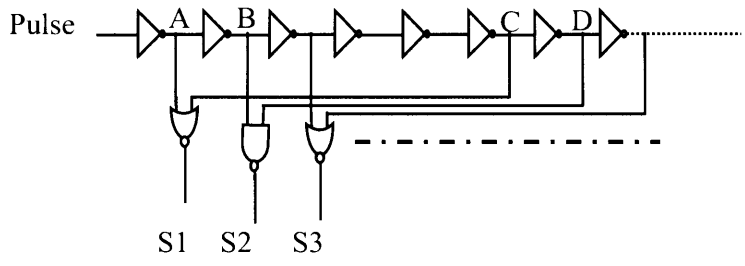


Figure 4.31 Sampling pulse generator of the high speed detector.

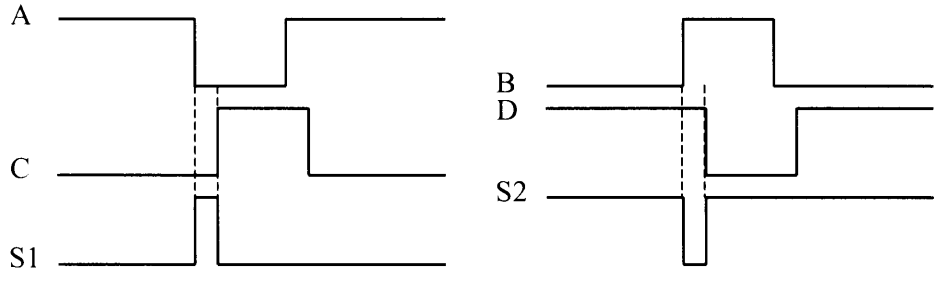


Figure 4.32 Timing diagram of generation of two successive sampling pulses.

4.6.2 Sample and Hold Circuit

The sample and hold circuit is modified from the previous version to meet the changes, which are introduced to the sampling pulse generator. Instead of using one NMOS transistor, a CMOS transmission gate has been used. Using the CMOS transmission gate gives the chance of sampling high and low levels signal more accurately than the case of using only NMOS. Moreover, it mitigates the problem of clock feed through. Figure 4.33 shows the schematic diagram of the modified sample and hold circuits for two successive sampling circuits. In fact, instead of using an inverter to obtain the complement of the sampling pulses, two NAND gates and inverter are connected as D flip flop to generate the two

complementary pulses (from Q and Q-bar). The NAND gates are sized to generate two-synchronized complementary sampling pulses.

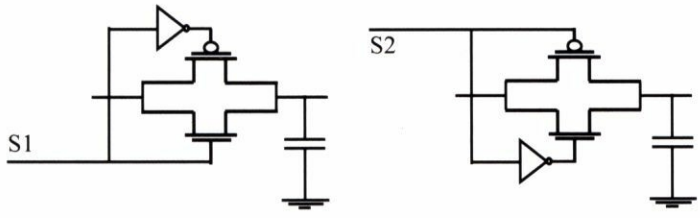


Figure 4.33 Schematic diagram of sampling switch of two successive sampling circuits.

4.6.3 Simulation Results

The high speed version of the detector has been design and simulated using Hitachi 0.18μm technology. A sample of timing diagram of the sampling pulse generator is shown in figure 4.34. the sampling interval is 50 pSec, which reveals that the maximum theoretical sensed frequency is 10GHz.

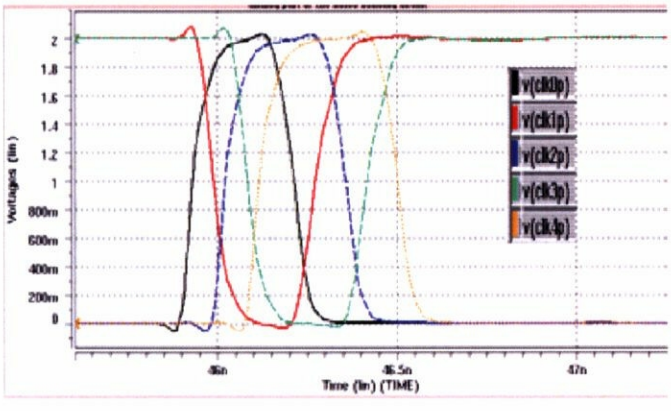


Figure 4.34 Sample of the of timing diagram of the sampling pulse generator.

The detector is designed to capture a 3-nano seconds time window of a noise signal. The simulation results come as shown in figure 4.35.

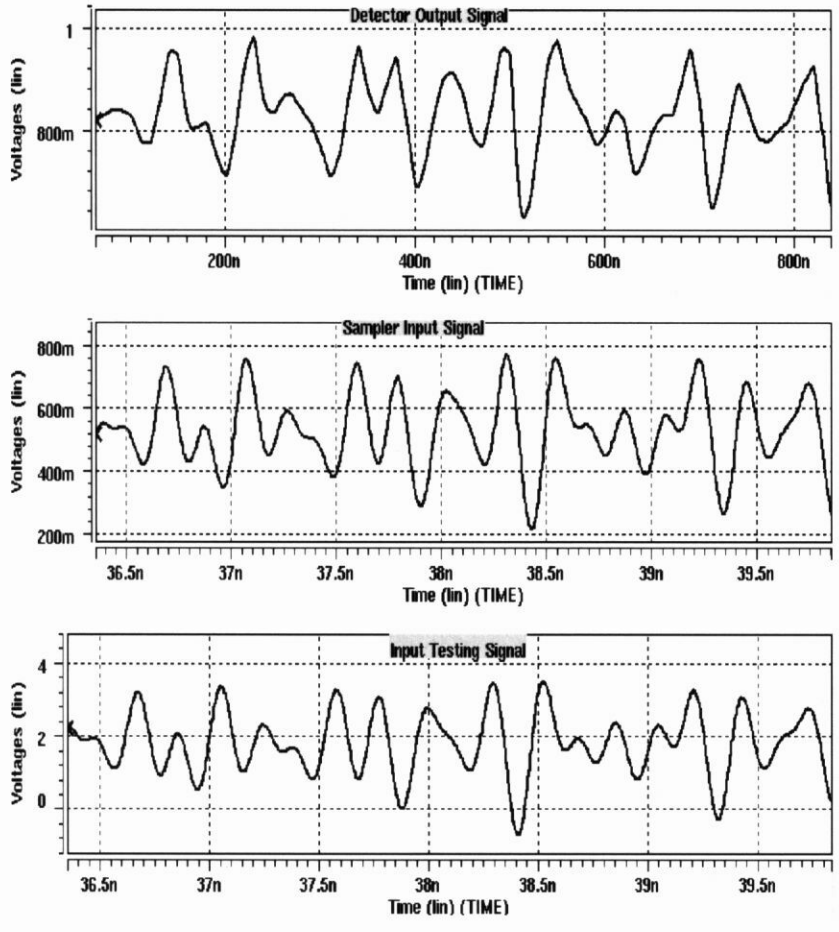


Figure 4.35 Simulation results of the high-speed detector. (lower graph) is the testing signal. (middle graph) is the buffer output. (upper graph) is the detector output.

4.7 Chapter Conclusion

In this chapter, first, an overview on the previous works regarding the on-chip noise measurement has been given. To avoid the problems attached with the previous designs, an on-chip noise detector has been designed and fabricated using

0.18μm technology. The detector can detect the single-event or the non-periodic signals within the measurement time window. It is equipped with programmable voltage divider to be able to detect high-swing signals having maximum theoretical frequency 5GHz. The bandwidth of the output signal can be controlled by the user to fit the monitoring tools off-chip and to avoid the effects of the on-chip parasitic elements and hence conventional equipments can be used to measure the signal off-chip. A test chip is fabricated and tested successfully. The detector's design has been modified to increase the sampling rate. Upon the simulation results, the modified version is capable to measure signals of frequency (theoretically) up to 10GHz.

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