Chapter 5

On-chip Minimum/Maximum Fluctuations Detection

5.1 Introduction

The continues technology scaling over the past few decades has enabled integrated circuits to speed up the computation rate by increasing clock frequencies and the number of computing elements. The device scaling has required decreasing the supply voltage to keep the device reliability; on the other hand, the overall power demand became larger, which made the design of power/ground net a challenging task [1-5] and led to an increase in the currents drawn from the power/ground networks. The trend of increasing power and clock frequency while reducing power supply voltage causes the power supply network to experience larger di/dt noise. Furthermore, the resistances of the interconnects have also increased due to the decrease in wire widths. As a result, the IR drop in the supply grid wires has become significant. In modern deep-submicron technologies, the supply voltage variation greatly affects the performance and reliability of both analog and digital circuits. In analog circuits, the deviation of the supply/ground from their nominal values can push the transistors out of saturation region and hence the circuits will no longer work correctly. In digital circuits, the supply/ground variations can increase the path delay and hence deteriorate the system throughput or even result in spurious pulses, which may be captured by the register elements in the primary output tending to function failure

[6-8]. The gate oxide reliability is another concern in deep submicron technologies. The gate oxide breakdown is generally understood to be the result of a gradual buildup of defects such as electron traps in the oxide, but the precise point at which breakdown occurs is statistically distributed so that only statistical averages can be predicted. The rate of defect generation in the oxide is proportional to the current density flowing through it, which in turn is function of the applied voltage, and therefore the reliability margin for gate-oxide breakdown has been drastically reduced as a consequence of device scaling [9]. There are extensive researches regarding the estimation of the switching noise in prior to chip fabrication in order to avoid or at least minimize its deleterious effects [10-13]. Nevertheless, performance is imprecisely defined due to the inability to close the design cycle with comprehensive post-fabrication validation data. In today's nano-technology, it is important for the designer to have the essential information to be aware about both the system performance and reliability. In this work we aim to provide the necessary power/ground fluctuation data, which will be helpful in identifying the performance and reliability limits of the current design. In addition, it can be used as feedback information for modifying the subsequent version of the design. The design is able to report the peak minimum and maximum voltage fluctuations in both supply and ground net at different spots in a design at different threshold levels. Moreover, the design is accompanied with the digital circuitry necessary to provide the timing information of noise pulses. In other words, the detector is able to report if the supply/ground voltage of a specific part in a design exceeds/lower than a predefined voltage level in addition to the moment of occurrence. By analyzing the data reported by our detector, the designer will be aware about the noise distribution on both power and ground net and hence will be a step closer to the accurate modeling of system performance and reliability.

5.2 Motivations

In recent VLSI/ULSI systems, the power/ground net is contaminated with switching noise as illustrated in figure 5.1-a, b. The noise is mainly due to sudden change in the current (di/dt) drawn form/discharged to the power supply/ground incorporated with parasitic inductance of the net wires. In addition, the voltage drop due to the wire resistance, which is referred to as IR drop. Since the systems performance is directly proportional to the actual value of power supply applied to the circuit. The worst case of the actual value of power supply will happen if the maximum undershoot (V_{DD_MIN}) in the supply net happened at the same of existence of the maximum overshoot (V_{GND_MAX}) of ground net. In other words, if τ_2 and τ_4 (shown in figure 5.1-a, b) have the same values. Also, the worst case conditions for the gate oxide reliability will happen if V_{DD_MAX} and V_{GND_MIN} are coincident.

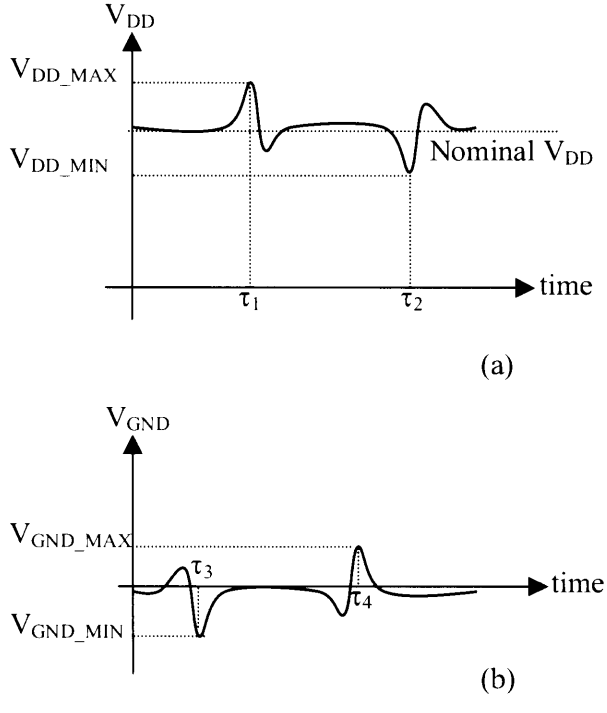


Figure 5.1. Illustration for (a) Power supply noise (b) Ground bounce.

There are two objectives of the design:

(i) The current target of the design is measure the parameters shown in figure 5.1-a, b, which are V_{DD_MAX}, V_{DD_MIN}, V_{GND_MAX} and V_{GND_MIN} as well as τ_1, τ_2, τ_3 and τ_4 within a design, the mentioned parameters are different form spot to another due to the difference in load and switching activity; So that the detector is replicated to form matrix probing heads as it will be explained later.

(ii) The next target of the design is to provide the data necessary to statistically model both the power supply and ground noise. This will be achieved by estimating the frequency of occurrence of the different noise pulses height and hence the designer will be able to construct the statistical distribution of noise pulses as illustrated by figure 5.2. This information will be helpful in more accurate modeling for the system reliability and/or performance.

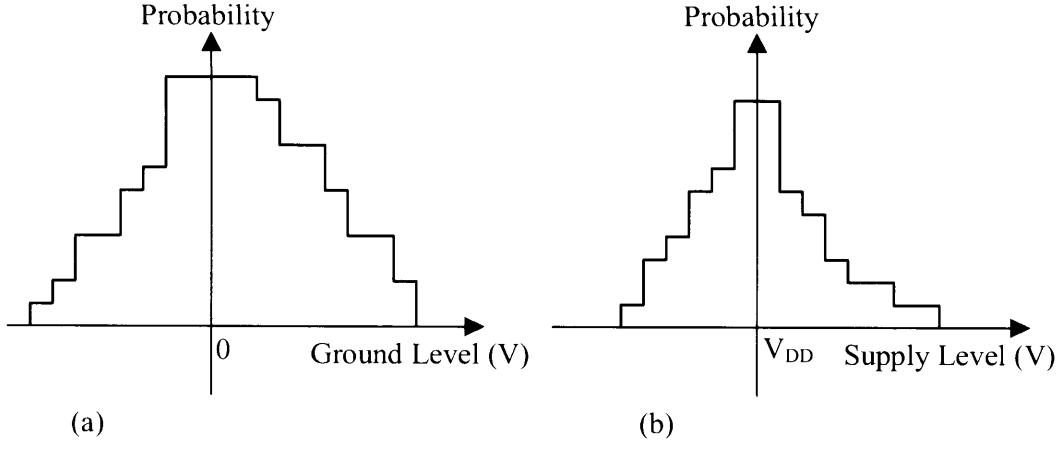


Figure 5.2. Illustration for the PDF of (a) ground bounce (b) power supply noise.

5.3 Limitations of the Conventional Peak Detector

The current objective of the design is to detect peak minimum and maximum of supply and ground net. The initial thinking to achieve this target is by using the

conventional diode-capacitor peak detector (PD) shown in figure 5.3. The accuracy and bandwidth of the detector are two important factors in the desired application. The noise pulses in power/ground net are usually narrow and hence the bandwidth of the detector should as wide as possible.

The accuracy of the conventional PD has been tested by simulation assuming 0.18μm technology at different values for the NMOS widths. The applied signal shape and the output are shown in figure 5.4. The error is plotted versus the pulse width in figure 5.5 at different values of the transistor width. The error is calculated according to equation 1.

$$Error = \frac{V_{out} - V_{out\_max}}{V_{out\_max}} \times 100 \qquad (6.1)$$

Where V_{out_max} is the correct output value.

The results reveal that the conventional PD is suitable for detecting pulse having width wider than 1μSec with error less than 10%, which means that the conventional detector is not suitable for sensing the peaks in power/ground net of an LSI circuit. That is the expected peaks (MIN/MAX) in the power line of LSI circuits would be (much) narrower than this value.

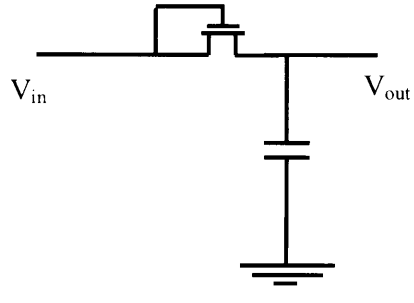


Figure 5.3 Schematic diagram of the conventional PD.

In the following subsections, a suitable peak minimum/maximum detector for power supply and ground bounce is presented.

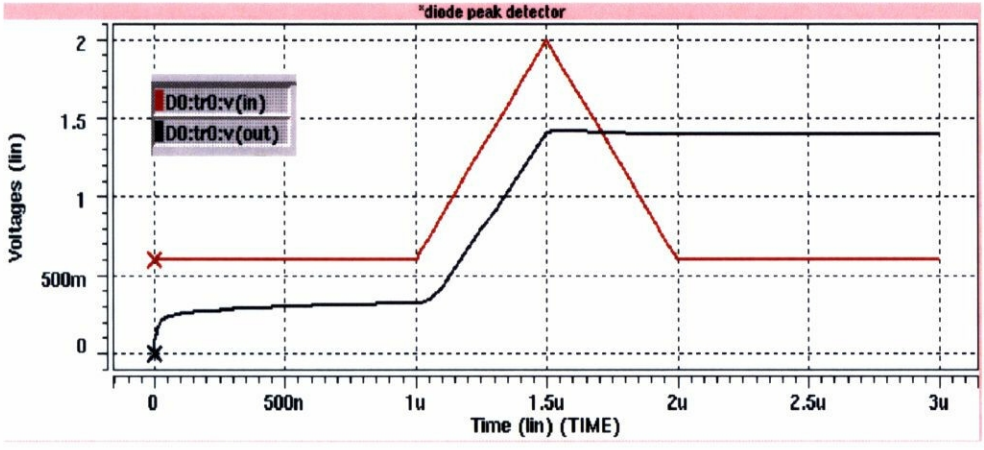


Figure 5.4 Input (V(in)) and output (V(out)) signals of the conventional PD.

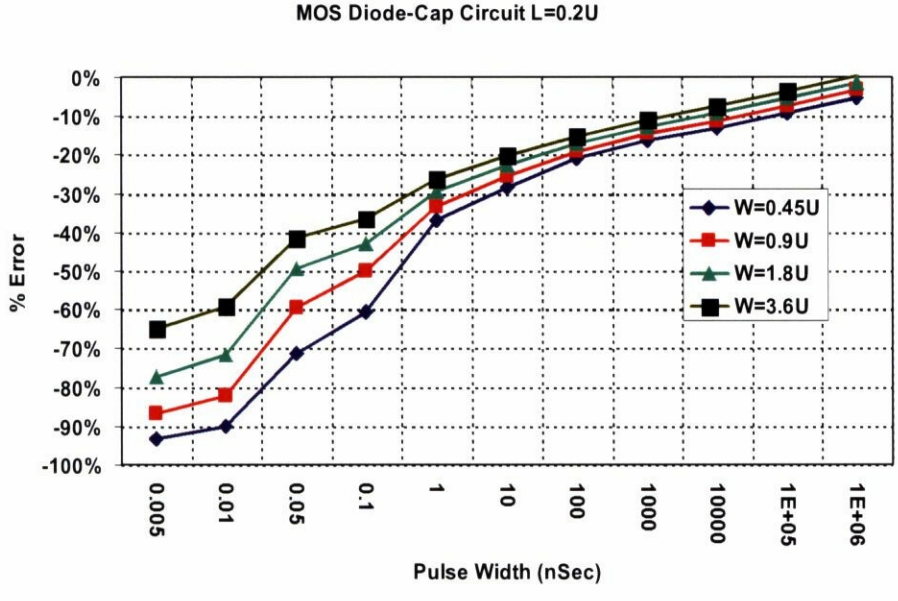


Figure 5.5 The accuracy of conventional PD at different MOS widths (W).

5.4 Architecture and Theory of Operation

The noise pulse on power/ground net is an analog high frequency signal. It is difficult to drive this signal, in its original form, off the chip accurately unless

using costly area overhead and expensive off-chip monitoring tools. An alternative way is to deliver digital information about the level and timing of the noise signal. To facilitate this process, a comparator is used to compare the noise level with a predefined reference voltage as shown in figure 5.6. The comparator output is processed to detect if, or not, the probed node voltage has exceed/lower than the reference voltage. The operation of this circuit can be explained by the aid of the illustrative timing diagram shown in figure 5.7. The detection process is started by setting the enable signal (E) of the head at the node under test. Reset signal, then, is applied to ensure that the latch history is cleared. To detect the peak maximum peak, the MIN/MAX is set low (logic zero). The reference voltage (V_{ref}) is set to specific level. If the supply/ground voltage (V_{meas}) exceeds V_{ref}, the comparator delivers a pulse, which is transmitted to the XOR gate output. The pulse causes the latch to be set.

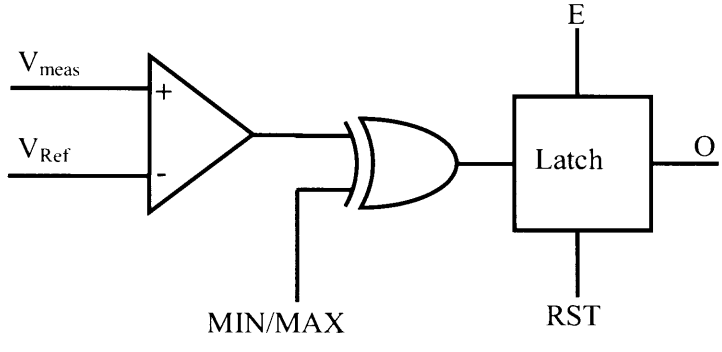


Figure 5.6 Schematic diagram of the MIN/MAX peaks detector.

The latch output is then delivered off-chip to report the existence of the peak overshoot. In the next section, I will explain the pulse delivery process. To detect the minimum peaks, a quite similar procedure is followed. The MIN/MAX signal is set high, the reference voltage is set to the minimum threshold level and the latch is reset. Under these conditions, the comparator output is normally high. If the voltage of node under test is lower than V_{ref}, a negative going pulse is

produced at the comparator output, which in turn, is translated into a positive going pulse at the XOR output and set the latch. The delivery of latch output will be done in same manner as in case of maximum peak detection. The role XOR is vital. Unless, using the XOR, two comparators would be needed for peak maximum and minimum respectively.

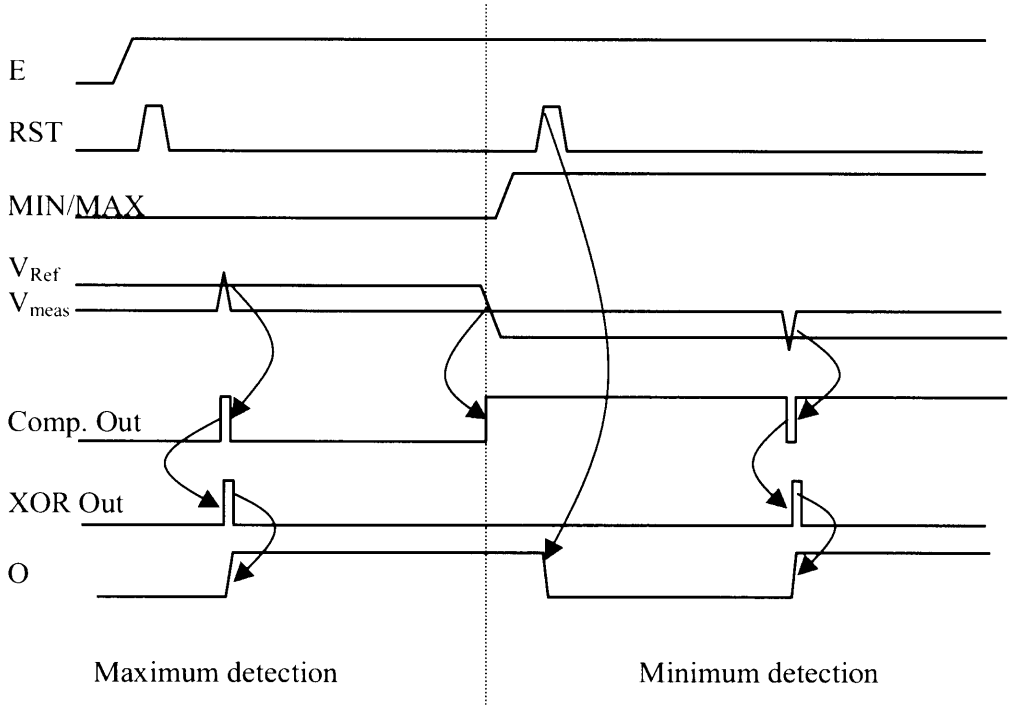


Figure 5.7 Illustrative timing diagram for MIN/MAX detection process.

The overall design is prepared to work in three related modes

1- DETECT.

2- DETECT and WHEN.

3- DETECT, WHEN and WHERE.

In the first mode (DETECT), the detector report the event (MAX/MIN) regardless the timing and spatial information of the event. The second mode, (DETECT and WHEN), is concerned with detecting the event level and the timing information of the event. Timing information means "to report when the event has happened with

respect to a reference moment. In the third mode, (DETECT, WHEN and WHERE), the detector delivers all information requested to know the event's level, timing as well as its position within the chip. The detection mode is selected by the user. The detector has been designed to be interfaced by a CPU as shown in figure 5.8 and hence the detection process is applicable for the very large integrated circuits. In the following subsections, the different parts of the design as well as the operation in the different modes are explained.

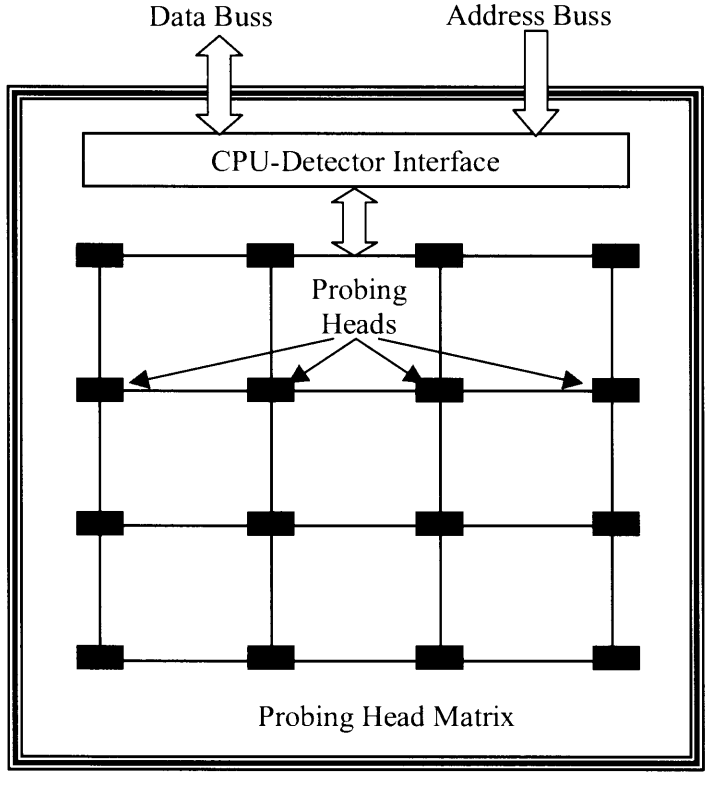


Figure 5.8 Block diagram of the overall design.

5.4.1 Probing Heads Matrix

The probing heads matrix consists of n×n probing heads. Each head consists of comparator, XOR and latch in addition to logic circuits necessary for head

enable and activation according to the detection mode. The outputs of the different heads are logically connected to each other through OR gate to produce one signal. The signal is referred to as OREDO. The schematic diagram of probing node matrix is shown in figure 5.9. The enable terminal (E) is controlled by the latch output and the OREDO signal according to the operating mode as it will be explained in the subsequent section.

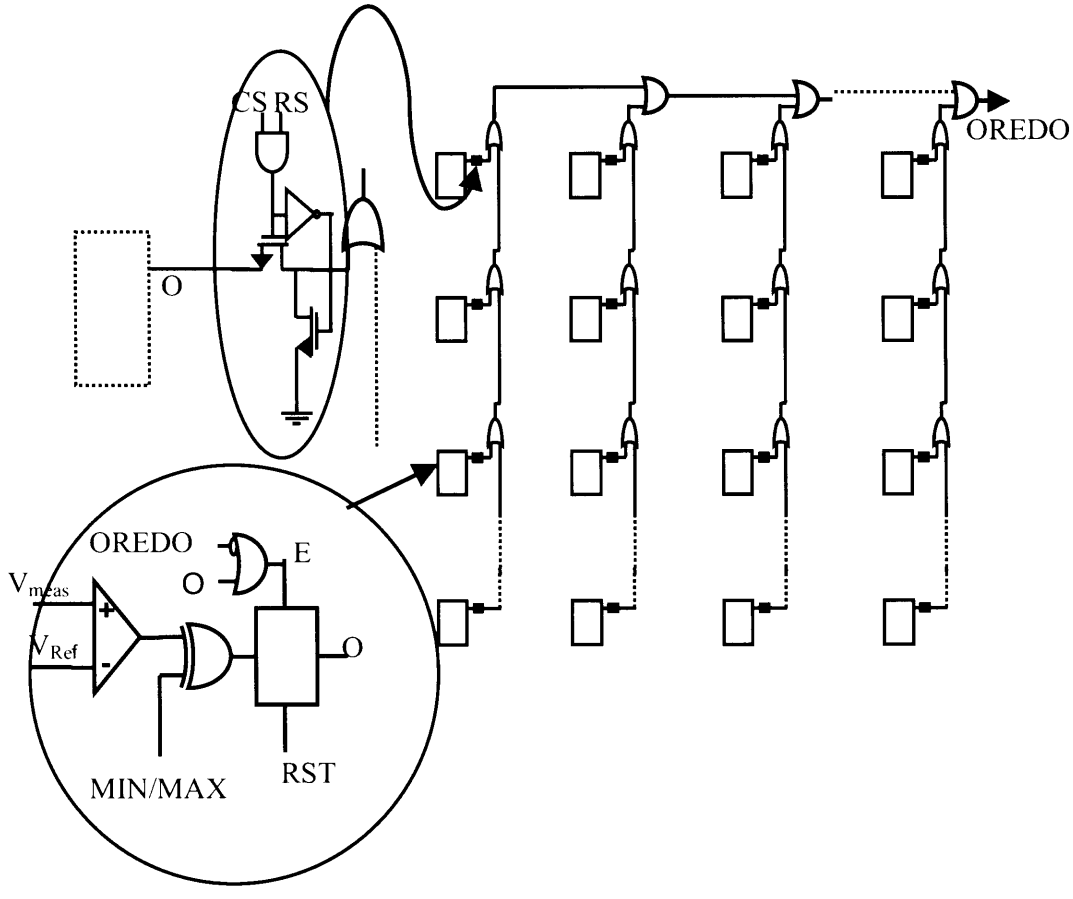
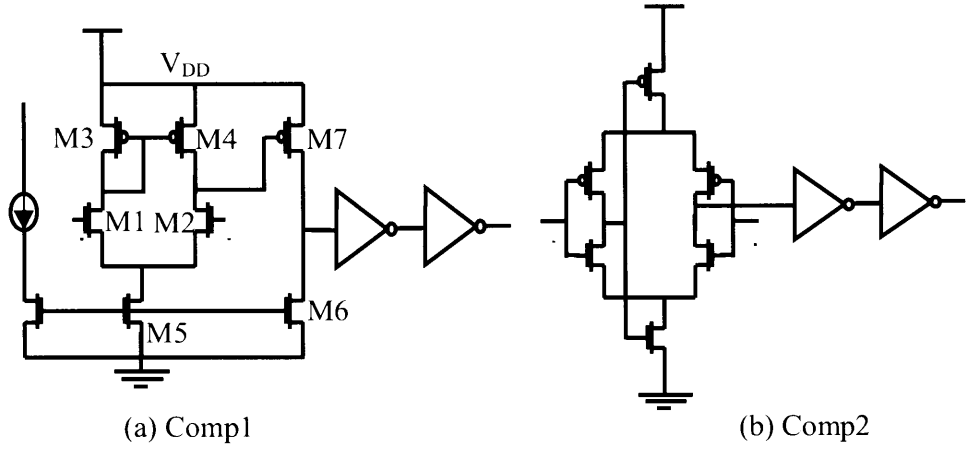


Figure 5.9 Schematic diagram of n×n probing heads matrix.

The comparator is an important building block in the design. That is, the comparator design will affect the detection accuracy. It is also important that the comparator costs small area and power overhead. Two comparator structures, having the schematic diagram shown in figure 5.10-a, b, have been simulated. The

detection accuracy versus the detected pulse-width is plotted as shown in figure 5.11. The results reveal that comparator (a) has slightly better performance than comparator (b). So that, comparator (a) has been chosen to build the probing head. In figure 5.11, the horizontal axis shows the detector accuracy, which is the difference between pulse level (V_{mea}) and the reference voltage. The vertical axis shows the minimum pulse width that can be detected. For an accuracy of 20mV, the minimum pulse width should be 600pSec. The common mode range of the comparator is 1.0V (0.6~1.6) assuming 0.18μm technology.



(a) Comp1 (b) Comp2

Figure 5.10 Schematic Diagram of the tested comparators.

Since the detector is intended to detect the peaks minimum/maximum in both power and ground net, level shifters and selection switchs are need to accomplish this operation. Two level-shifters, shown in figure 5.12, have been designed. The first is an NMOS buffer, shown in figure 5.12-a, which can be used effectively to shift the variation in the power line down to the working range of the comparator, while the second is a PMOS buffer, shown in figure 5.12-b, which can be used to move the variation of the ground line up to the common mode range of the comparator.

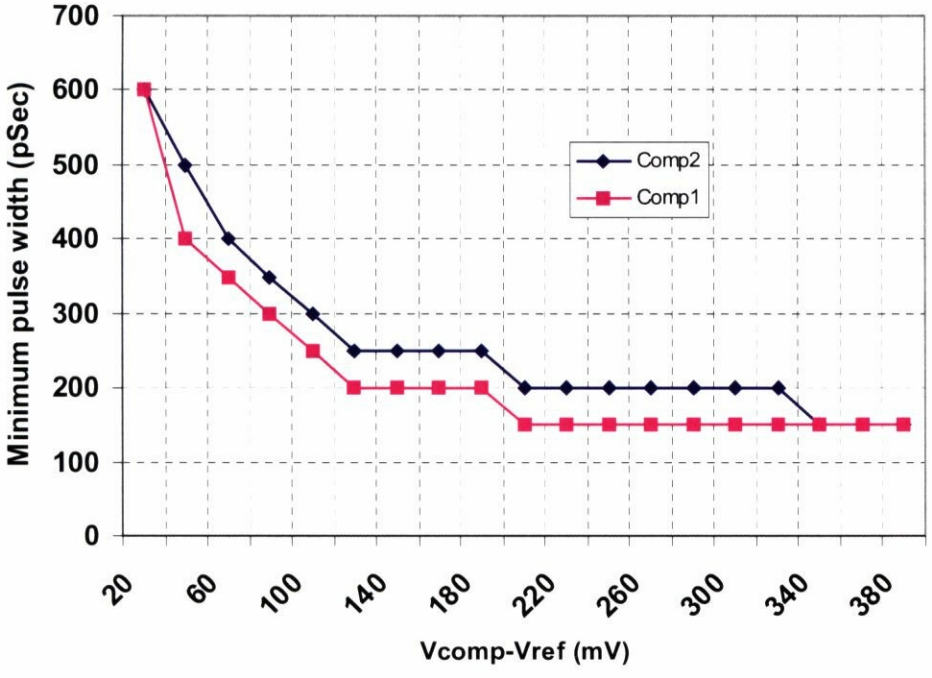


Figure 5.11 Accuracy versus pulse width of the tested comparators.

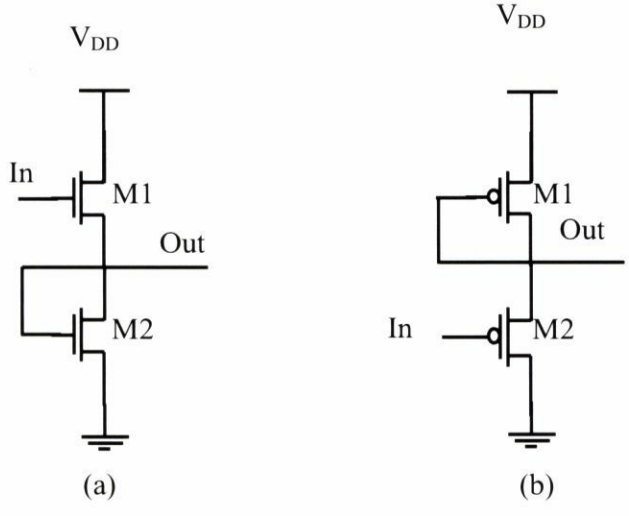
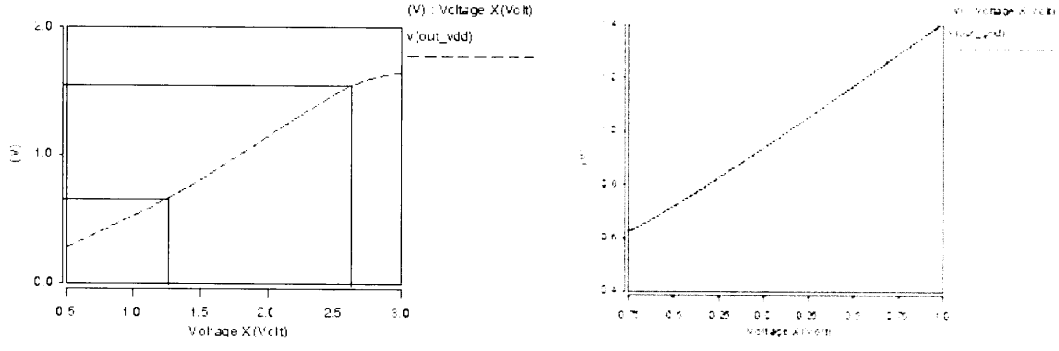


Figure 5.12 (a) Ground bounces level shifter (b) Power supply noise level-shifter.

The transfer characteristics of buffers are shown in figure 5.13-a, b. The transfer characteristics reveal that NMOS buffer can shift the variation in the power supply net ranged from 1.3 to 2.65V to be fit in the common mode range of the comparator assuming 1.8μm technology node. The PMOS buffer transfer curve shows that ground bounces ranged from -0.75 to 1V can be leveled up to the working range of the comparator. The frequency responses of both buffers are shown in figure 5.14-a, b. The band width of NMOS and PMOS buffer is around 10GHz. Figure 5.15-a and b show an example of the input and output signals to the NMOS buffer and PMOS buffer respectively.



(a) (b)

Figure 5.13 The transfer characteristics of (a) NMOS buffer (b) PMOS buffer.

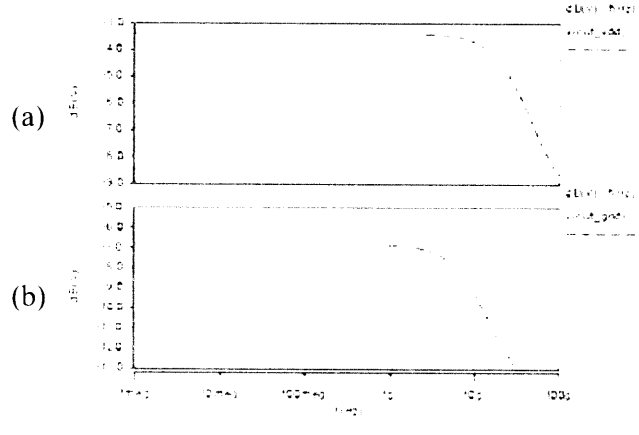
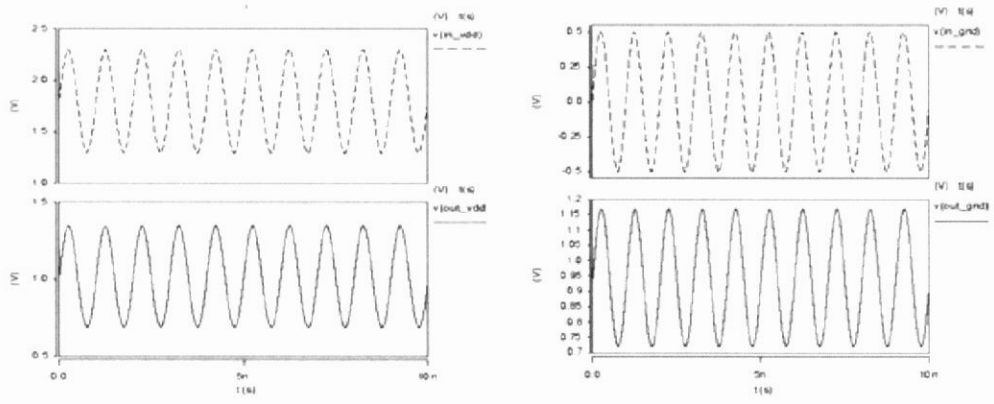


Figure 5.14 Frequency response of (a) NMOS buffer (b) PMOS buffer.



(a) (b)

Figure 5.15 Example of the input and output signals in (a) NMOS buffer (b) PMOS buffer.

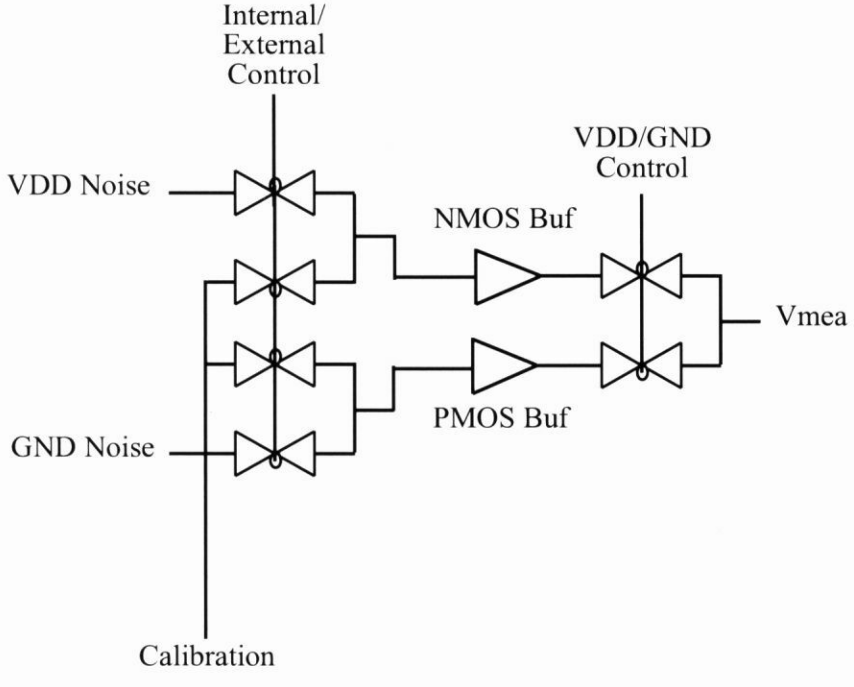


Figure 5.16 Schematic diagram of the calibration-VDD-GND noise selection and scaling circuit.

For the sake of calibration, an external signal is fed to the detector via a line called "Calibration" and the selection among power supply/ground signal or the calibration signal is done by two control signals and CMOS switches as indicated in figure 5.16 and according to the scheme shown in table 5.1.

INT/EXT	VDD/GND	Selection
0	0	Ground noise measurement
1	0	Ground measurement calibration
0	1	V_{DD} noise measurement
1	1	V_{DD} measurement calibration

Table 5.1 Selection schemes of VDD/Ground and calibration.

5.4.2 CPU Interface

The probing heads matrix is interfaced with the CPU through 16bits data buss and 4-bit lines of the address buss and a write signal (WRT). In addition to the address decoder, which includes the column and raw selectors, the interface contains a group of counters and registers to hold the necessary data and generate signals for the different detection modes. The counters and registers are as shown below:

(i) Input registers:

1. INT/EXT is a 1-bit register to hold a signal to control weather the detector will be calibrated by external signal or is used to measure the internal noise signals.
2. MIN/MAX is a 1-bit register to hold a signal to select the minimum or maximum level detection.
3. GND/V_{DD} is a 1-bit register to hold a signal to connect either the V_{DD} or the ground net to the detector.
4. RRESP is a flag register. Filling this register with logic one means that the CPU has responded to the read request reported by the head matrix after event detection.
5. CS is a 3-bit register to hold the necessary data to select one or more column(s).
6. RS is a 3-bit register to hold the necessary data to select one or more raw(s).

To write a data in a register, it is first enabled by decoding a dedicated address, then write the data through data buss (choose the in mode for the data buss). An example of connection of INT/EXT, MIN/MAX or GND/V_{DD} registers and the block diagram of column/raw address register and decoder are shown in figure 5.17, 18 respectively. The enable signal is produced at the address decoder as it will be shown later in section.

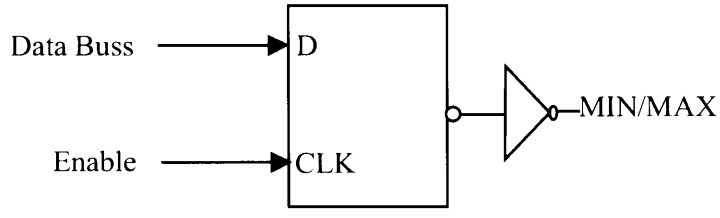


Figure 5.17 Block diagram of MIN/MAX register.

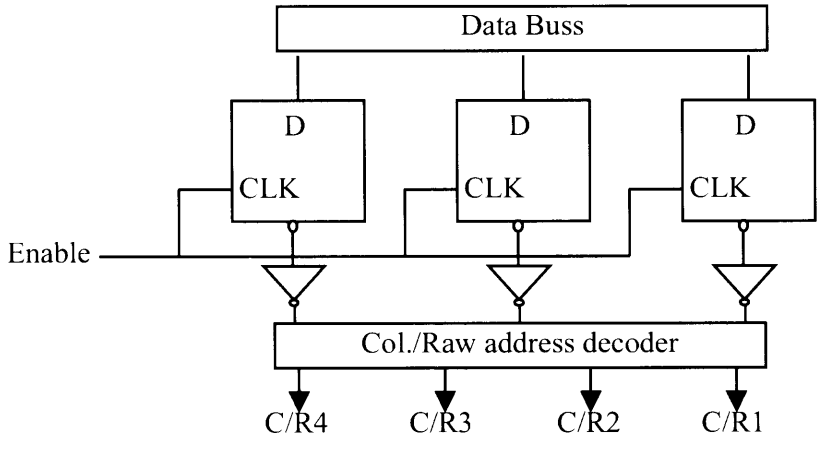


Figure 5.18 Block diagram Col./Raw address register and decoder.

The RRESP register connection is similar to that is shown figure 5.17 with additional reset terminal.

(ii) Output registers and counters are as follows:

1. RREQ is a three-state buffer to pass/isolate the read-request information to the CPU data buss. RREQ is logic one indicating that the CPU is requested to read the event reported by the probing head matrix.
2. OREDO is a three-state buffer to pass/isolate the OREDO signal to the CPU.
3. RCNT (Reference Counter) is a 16-bit counter used to hold an information about the starting (reference) instant of the detection process.
4. ECNT (Event Counter) is a 16-bit counter, which is used to hold information about the moment of event detection.

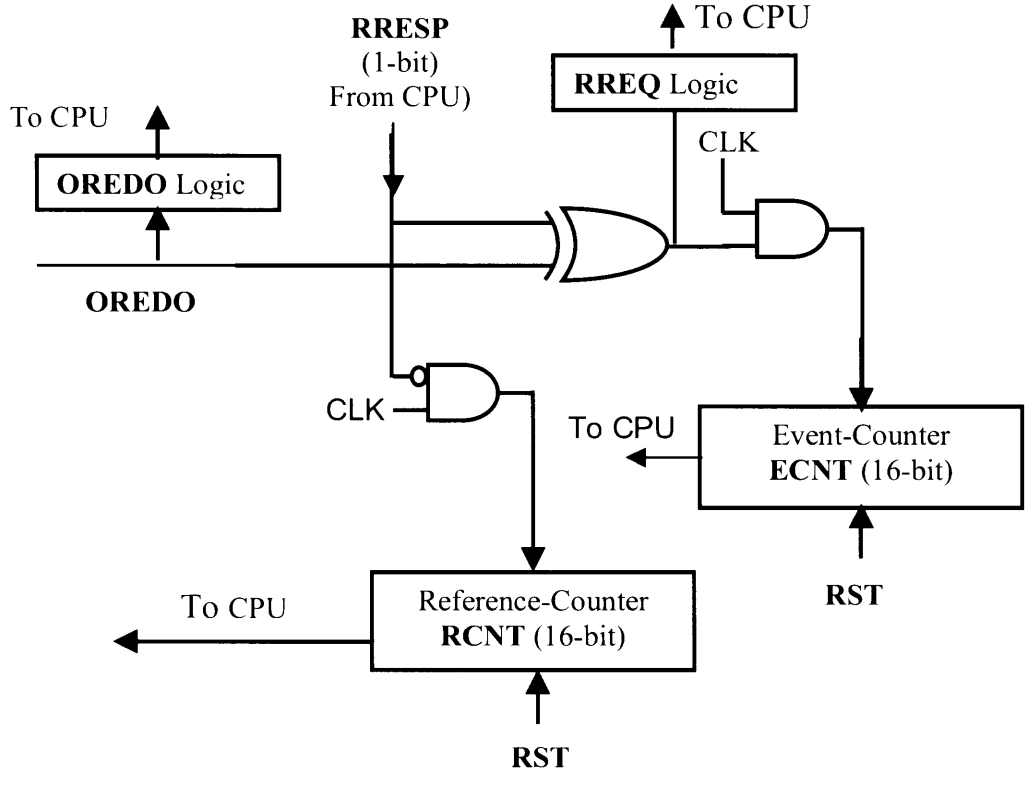


Figure 5.19 Schematic diagram of the counters connected to head matrix output.

The difference between the content of ECNT and that of RCNT expresses the timing information of the event (the moment at which the event happened with respect to reference instant), which can be evaluated by the CPU. Figure 5.19 shows the connections of some of the mentioned registers and counters with the head matrix.

The enable signals, produced by the address decoder, are generated according to the following table:

X0	X1	X2	X3	X4	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y8
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	1	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	1	0
1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	1	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	1	0	0	0	0	0	0

Table 5.2 Setting of the enable signals.

X0 is resulted form decoding the other 12 bits address. The enable signals, Y's, are defined in table 5.3.

MIN/MAX	Y0	RCNT	Y5
VDD/GND	Y1	ECNT	Y6
RRESP	Y2	RREQ	Y7
CS,RS	Y3	OREDO	Y8
RST	Y4	INT/EXT	Y9

Table 5.3 Definition of the enable signals.

The enable signals are multiplied by the WRT or its complement according the controlled function and then fed to the appropriate register/counter.

The column and raw address decoder are designed according to the truth table shown in table 5.4.

A	B	C	C/R0	C/R1	C/R2	C/R3
1	1	1	1	1	1	1
1	1	0	1	1	0	0
1	0	1	0	0	1	1
1	0	0	0	0	0	1
0	1	1	0	0	1	0
0	1	0	0	1	0	0
0	0	1	1	0	0	0
0	0	0	0	0	0	0

Table 4 Setting of the Col./row address decoder.

5.5 Detection Modes

There are three detection modes provided by the detector. The selection of any mode is done by the user through CPU programming. The procedures of the different detection modes are explained below.

5.5.1 DETECT

The first and fastest detection mode is called DETECT. In this mode, it is only required to observe the variation of the supply/ground level in either specific location within the design or globally through the design. In this mode, one of the following procedures is followed:

1- Select the location to be tested by choosing the corresponding head through the RS and CS.
2- Apply the required reference voltage.
3- Reset the head.
4- Check for the RREQ.

In case of global fluctuation observation is required, slightly different procedure is applied as followed:

1- Enable all the heads.
2- Apply the required reference voltage.
3- Reset all heads.
4- Check for the RREQ.

5.5.2 DETECT and WHEN

In the detection mode, DETECT and WHEN, CPU reads the contents of ECNT and RCNT to know when the event happened. The procedure will be as follows:

1- Enable all the heads.
2- Apply the required reference voltage.
3- Reset all heads.
4- Check for the RREQ.
5- Read the content of RCNT.
6- Read the content of ECNT.
7- Subtract the content of ECNT form that of RCNT.

5.5.3 DETECT, WHEN and WHER

In this mode, in addition to the second mode detection procedure, a binary search algorithm is used to determine the location of the event. The procedure will be as follows:

1- Enable all the heads.
2- Apply the required reference voltage.
3- Reset all heads.
4- Check for the RREQ.
5- Read the content of RCNT.
6- Read the content of ECNT.
7- Subtract the content of ECNT form that of RCNT.
8- Execute the binary search algorithm to find out the location of the event.

5.6 Test Chip

To practically test the operation of the proposed detector, a 4×4 heads matrix detector is implemented in a test chip using Rohm 0.18μm technology. Each head is attached with a noise generation circuit shown in figure 5.20. The noise generation circuit can generate negative and positive going pulses of different values on both V_{DD} and GND line. The level of the noise pulse is controlled by the pattern of both V_{DD} and GND noise controls. These controls are connected to all noise generation circuits in the test chip. The instant of the noise pulse is determined by a separate firing pulse, which is supplied to each noise generation circuit individually. The simulation result of the noise generated by the circuit is shown in figure 5.21. It is clear that the level of noise pulse changed by changing the pattern of the noise controls. The noise pulse is generated simultaneously with the firing pulse.

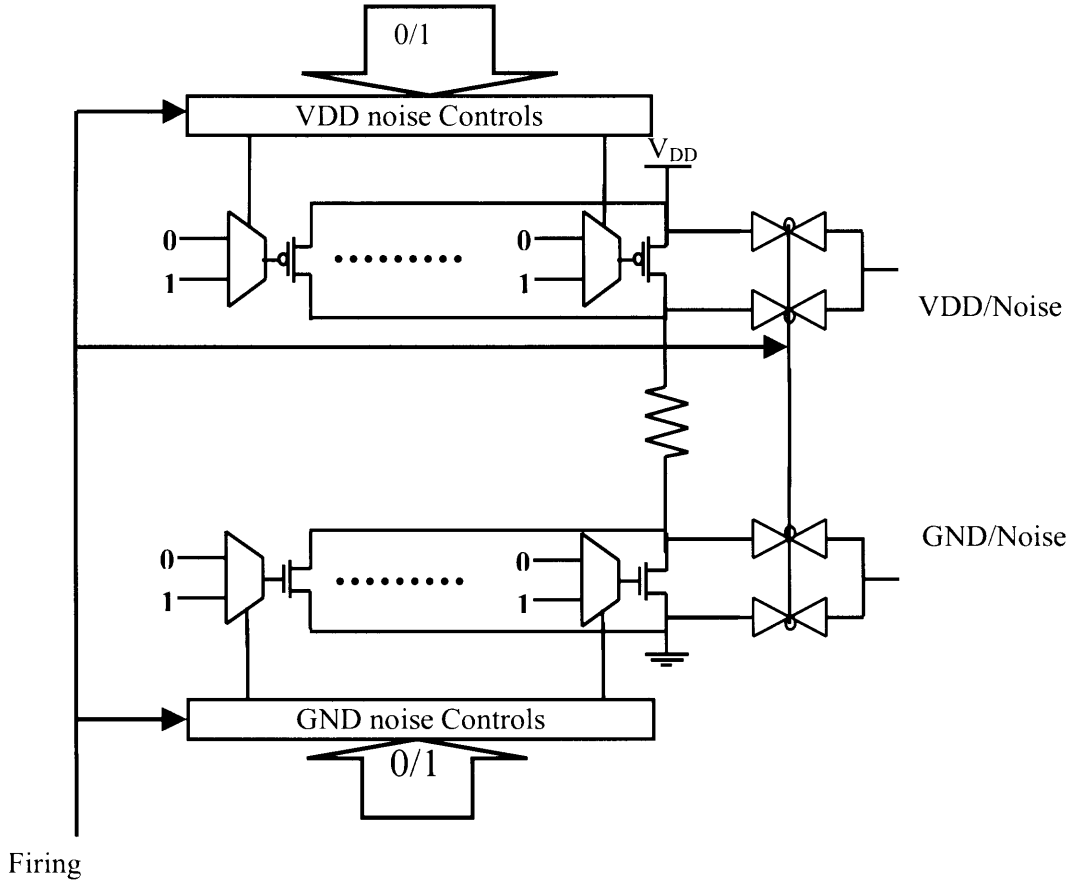
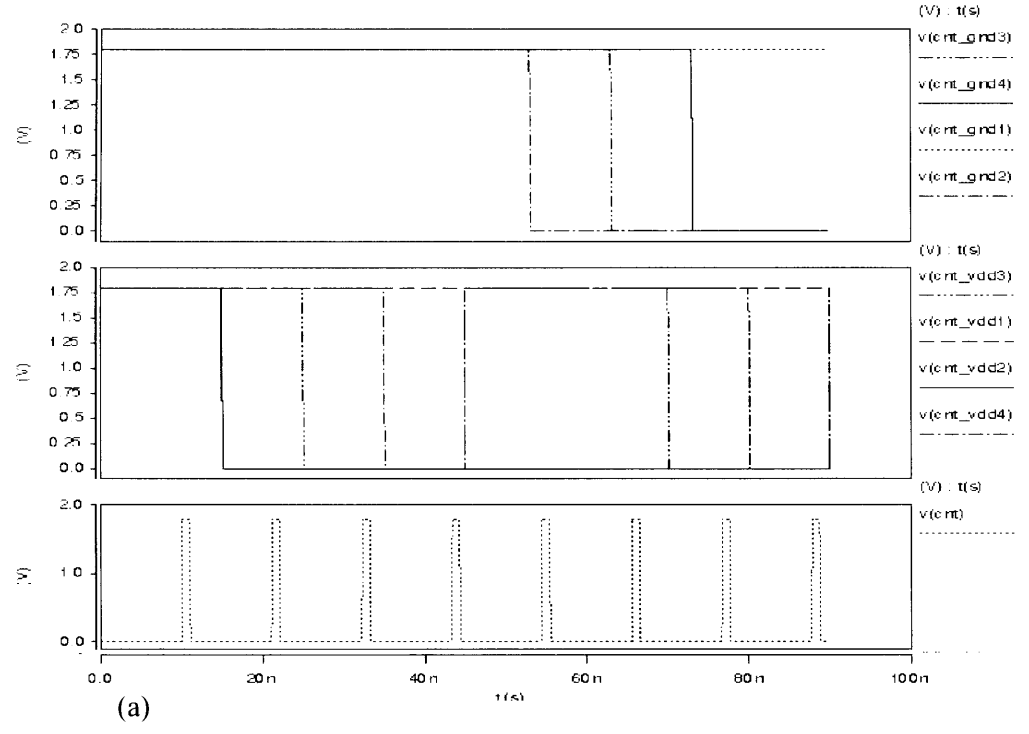


Figure 5.20 Schematic diagram of the noise generation circuit.

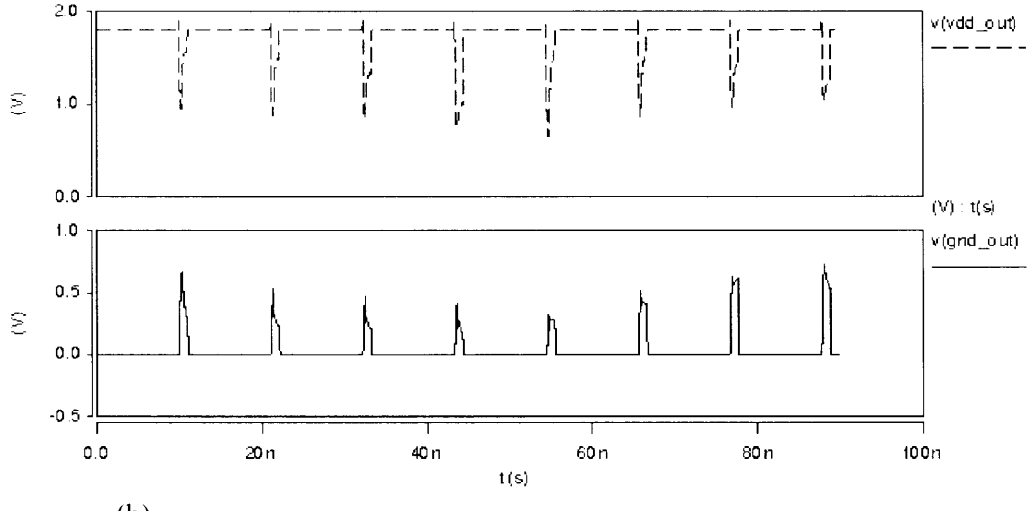
The layout of the test chip is shown in figure 5.22.

5.7 Simulation Results

The netlist of the probing head matrix is extracted from the layout. The extracted circuit is simulated using HSPICE. Samples of the simulation results for four heads are shown below in figure 5.23-a, b. The simulation is done for minimum and maximum pulse detection. The left half of results shows the peak maximum detection.



(a)



(b)

Figure 5.21 Simulation results of the noise generation circuit (a) input patterns of ground noise controls (upper graph), input patterns of VDD noise controls (middle graph), firing pulse (bottom graph). (b) power supply noise (upper graph), ground noise (lower graph).

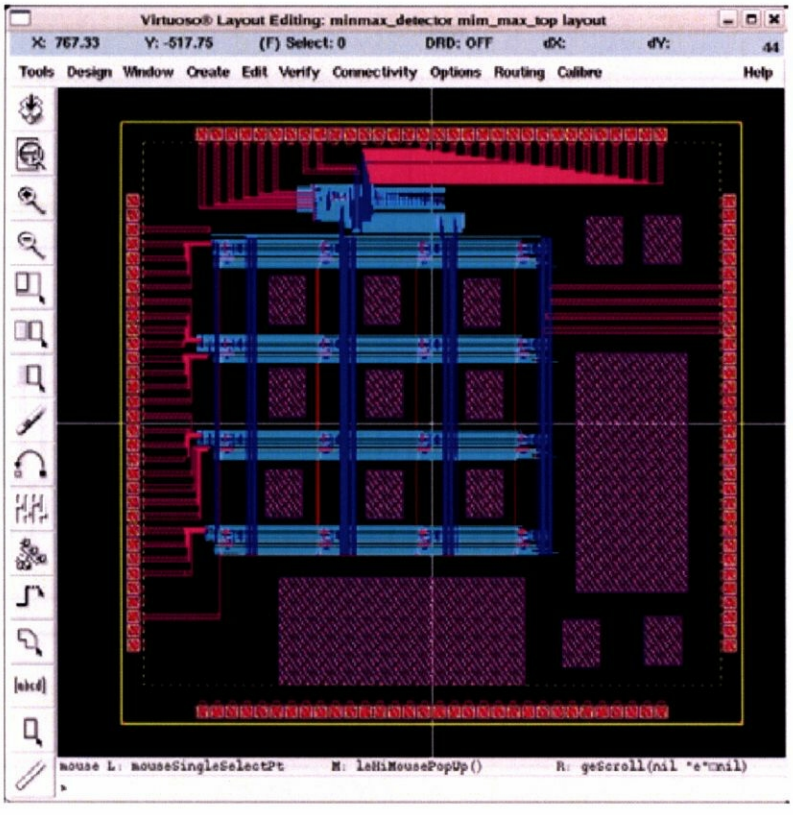
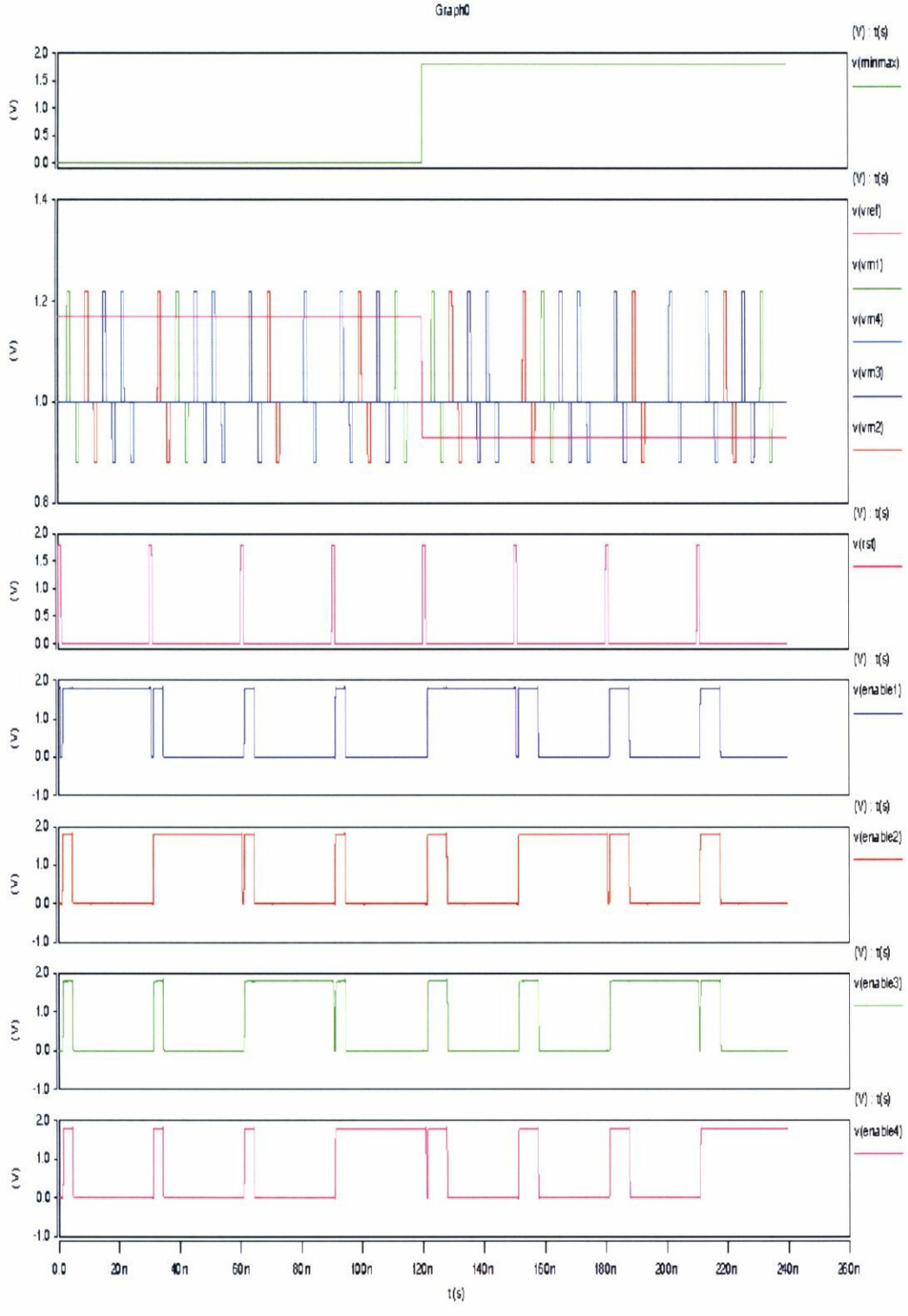
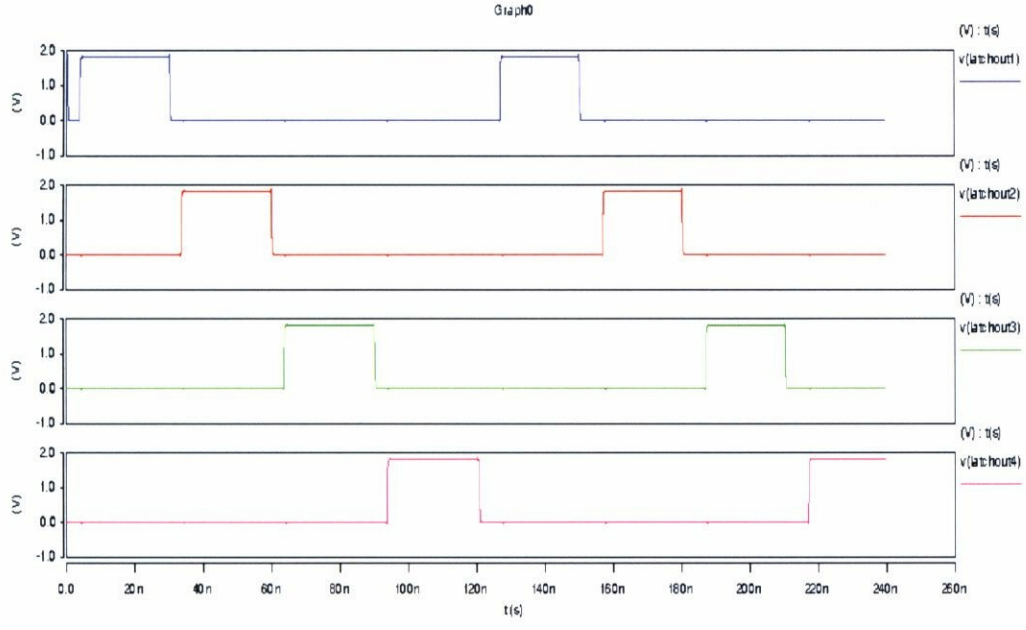


Figure 5.22 Layout of the test chip.

As shown in figure 5.23-a, the first top graph shows the min/max control signal. First it is set to zero, which means enable the maximum detection. The second top graph shows the spurious pulses in four probing nodes namely Vm1 to Vm4 in addition to the reference voltage Vref. The third top graph shows the reset signal (rst) applied to all probing nodes. As it can be seen, once the reset pulse applied, all the nodes are enabled and once a spurious pulse crosses the reference voltage (Vref), all nodes, but that is experienced the spurious pulse (hot node), are disabled and only the latch output of the hot node is set high and sustain on this setting until the next reset pulse.


Graph0
(V) : t(s)
v(minmax)
v(vref)
v(vm1)
v(vm4)
v(vm3)
v(vm2)
v(rst)
v(enable1)
v(enable2)
v(enable3)
v(enable4)
(V)
t(s)
0.0
20n
40n
60n
80n
100n
120n
140n
160n
180n
200n
220n
240n
260n

(a)



(b)

Figure 5.23 Simulation results of the test chip.

For example, after the first reset pulse, all the enable signals (v(anable1 ~ 4) the bottom four graphs of figure 5-23-a)) are set high until the first spurious pulse cross the reference voltage (Vm1 crosses Vref) then all enable signals go low but enable1 and the output of latch one (figure 5.23-b) is set high. This setting upholds until the subsequent reset. The scenario is repeated every reset as shown in figure 5.23-a, b.

5.8 Chapter Conclusion

In this chapter, a CPU-interfaced system to detect the minimum/maximum fluctuation in both V_{DD} and ground is designed. In addition to the magnitude information, the system has the ability to report the timing and spatial information of the spurious pulse. The system is designed using Rohm 0.18μm technology.

The fluctuation is detected by comparing the voltage of node-under-test with a reference voltage supplied form off-chip, and the fluctuation information is send off-chip in digital format. The detector is simple, therefore, it can be replicated within a design to detect the fluctuations on VDD/Ground nets at different spots, therefore safe operation can be guaranteed. The detector is interfaced by a CPU and hence it is suitable for future VLSI/ULSI circuits.

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Chapter 6

Conclusion

This study concerns with the noise immunity of static CMOS low power digital design by investigating the noise immunity of the current low power static CMOS design schemes and presenting a fast and accurate methodology to evaluate the noise sensitivity of the different nodes in a design during the design phase. In addition, for the modeling/characterization of noise in digital circuits, techniques to measure the non-periodic noise and sensing the peak minimum/maximum fluctuation on-chip have been presented. The study is presented in five chapters in addition to conclusion.

Chapter one gives a background about the power consumption and noise issues in current and future VLSI/ULSI digital design. It also includes the objectives of the study and thesis organization.

Chapter two presents the effect of noise on the performance of a selected group of low power as well as traditional digital design techniques. First, we present a model for the different noise sources in the digital circuits. Then we applied the model to a group of low power and traditional design testing circuits. The results clearly demonstrate that, from the noise immunity point of view, the dual threshold voltage technique is the best among the tested low power schemes having the same performance. In addition, in presence of strong noise, the low V_{DD} paths determine the speed of the dual supply circuits and the high V_{th} paths determine the speed of the dual V_{th} circuits, however the performance of the high V_{th} (dual V_{th} circuits) is better. In this chapter, we also present a methodology for

leakage power saving and at the same time, it has the same reliability of DVTCMOS. The methodology is referred to as DVTMTCMOS.

Chapter three presents a methodology to evaluate the noise-induced logic error probability in a given CMOS digital design in terms of supply voltage, threshold voltage, noise level and circuit configuration. At first, we modeled the noise immunity of the different logic gates in terms logic error probability including the effect of supply and threshold voltage, which is called electrical masking. Then, time masking has been modeled to reflect the variation of the spurious pulse width and generation time on the overall logic error probability. Moreover, the logic masking effect has been also considered. The electrical, timing and logic masking have been combined to form the overall logic error probability model. The model has been used to evaluate the logic error probability caused by the noise at the different nodes in two digital circuit examples, where, also the logic error probability is evaluated using HSPICE. The model results have been compared with the results obtained from HSPICE simulation. The comparison reveals that the model fit with the expected simulation results achieving speedup factor of more than 1000 over HSPICE. Moreover, the calculation time of the methodology is linearly proportional with the number of gates in a design, and hence, the method is suitable for investigating the big circuits. The model can be used to identify the weak parts against the noise in a given design during the design phase and hence it helps the designer in giving specific design considerations to strengthen the weak nodes.

Chapter four presents, at first, an overview on the previous works regarding the on-chip noise measurement. Then, to avoid the problems attached with the previous designs, an on-chip noise detector has been designed and fabricated using 0.18μm technology. The detector has the capability to detect the single-event or the non-periodic signals within the measurement time window. It is equipped with

a programmable voltage divider to be able to detect high-swing signals having maximum theoretical frequency of 5GHz. The bandwidth of the output signal can be controlled by the user to fit the monitoring tools capability off-chip and to avoid the effects of the on-chip parasitic elements, therefore conventional equipments can be used to measure the signal off-chip. Moreover, the detector is synthesizable and the designer can flexibly adjust its main parameters. A test chip is fabricated and tested successfully. The design has been modified to increase the sampling rate. Upon the simulation results, the modified version is capable to measure signals of frequency (theoretically) up to 10GHz. The detector can be used to characterize the on-chip noise and hence a realistic noise model is provided to the model mentioned in chapter three.

Chapter five presents a CPU-interfaced system to detect the minimum/maximum fluctuations in both V_{DD} and ground nets. In addition to the magnitude information, the system has the ability to report the timing and spatial information of the spurious pulse. The system is designed using Rohm 0.18μm technology. The fluctuation is detected by comparing the voltage of node-under-test with a reference voltage supplied form off-chip, and the fluctuation information is send off-chip in digital format. The detector is simple, therefore, it can be replicated within a design to detect the fluctuations on VDD/Ground net at different spots and hence, safe operation can be guaranteed. The detector is interfaced by a CPU and hence it is suitable for future VLSI/ULSI circuits.

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[1] M. Abbas, M. Ikeda and K. Asada," On-chip detector for single-event noise sensing with voltage scaling function" IEICE TRANS. ELECTRON., VOL. E89-C NO.3 March 2006.

[2] M. Abbas, M. Ikeda and K. Asada," Noise Immunity Investigation of Low power Design schemes" Accepted for publishing by IEICE TRANS. ELECTRON., VOL. E89-C. NO.8 August 2006, "in press".

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[3] M. Abbas, M. Ikeda and K. Asada, "Noise Effects on Performance of Low Power Design Schemes in Deep Submicron Regime" the 19th IEEE Int. Symp. On Defect and Fault Tolerance in VLSI, Cannes-France October-2004.

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