Chapter 6

Yield Optimization by Timing-Aware Cell Layout De-Compaction

6.1 Introduction

This chapter targets a timing-aware cell layout de-compaction method for yield enhancement. Recently, a lot of papers related to VLSI yield improvement have been published[14, 15, 16, 17, 18]. Most of them are proactive methodologies, which are not a post process. In [17], logic synthesis for manufacturability is proposed. This methodology introduces the manufacturability cost into logic synthesis and replaces the traditional area-driven technology mapping with a new manufacturability-driven one. It realizes larger reduction of the manufacturability cost when yield-optimized cells are available in the cell library. A new design flow proposed in [18] integrates manufacturability information into the timing-driven synthesis and place&route cost function. Yield-aware logic synthesis, place&route, and timing optimization are executed incrementally in this design flow. This flow uses a DFM extension library, which has variants of the basic logic functions with different manufacturability costs. They demonstrated the advantages of their methodology by applying it to several commercial ICs.

As stated above, a yield-enhanced standard-cell library is essential to these yield-aware VLSI design methodologies. Yield-enhanced standard-cell libraries were, however, designed mainly by hand and there is no fully automated standard cell yield optimization method proposed for this purpose. This chapter proposes an automatic yield-optimization technique for standard cells. Several papers have proposed the de-compaction method for yield-optimization[39, 40]. However, these methods consider only yield and area as costs, and the circuit performances are not considered. The careless modification of the original layout may degrade its performances severely and the created layout is not always acceptable for the

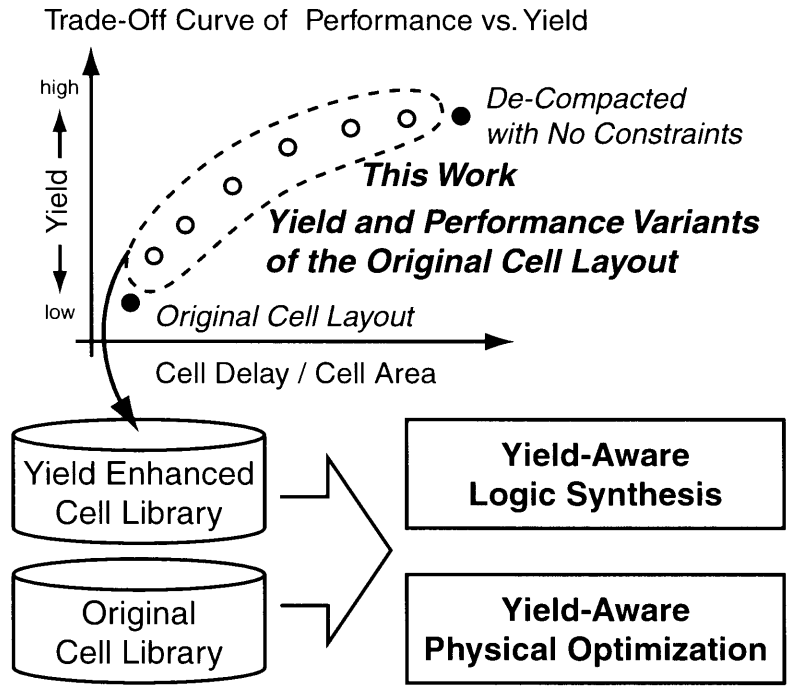


Figure 6.1 Overview of the proposed timing-aware cell layout yield enhancement framework.

target performances. Therefore, we propose a timing-aware cell layout de-compaction technique for yield optimization. The proposed method relaxes the width of a given cell layout under given timing constraints to optimize the yield. Since there is normally a high quality, hand-crafted original cell library, it is straightforward to optimize the yield by relaxing the width of the original layout with low computational effort, rather than creating it from scratch. Moreover, the layout after de-compaction preserves the integrity and the predictability of the original layout because it also preserves the relative geometry as the original layouts.

The proposed method optimizes the yield by minimizing the Critical Area (CA). Critical area is defined as the area in which the center of a spot defect must fall to cause a fault and its reduction plays an important role for yield enhancement. This de-compaction framework is also effective for OPC-relaxation. The OPC-relaxation results in terms of the fractured mask data size reduction is also shown in this chapter. Moreover, the proposed framework is applied to the redundant contact insertion adjacent to the single contacts. Recently, contact failure becomes one of the most dominant yield loss reasons and redundant contact insertion is highly recommended to improve the yield. To take the parametric yield into account, the proposed de-compaction framework is also extended to the gate layout pattern regularity enhancement to reduce the systematic variation of the gate critical dimensions.

The overview of the proposed method is illustrated in Figure 6.1. This method creates a yield-optimized cell layout under given various timing constraints and can pick up the yield variants of a cell layout from the cell delay versus yield trade off curve. These cells are prepared as a yield-enhanced cell library and used for the yield-aware logic synthesis and physical optimization. The proposed method performs a de-compaction of the original cell layout using Linear Programming (LP). We develop a new accurate linear delay model to formulate the timing constraints into LP. This model approximates the delay difference from the original delay induced by the differences of the parasitic capacitances after de-compaction.

Section 6.2 defines the problem solved in this chapter and explains the LP formulation of the design rule constraints. The formulation of the yield cost metrics, *i.e.*, critical area minimization, OPC relaxation, redundant contact insertion, and gate layout pattern regularity enhancement are explained in Section 6.3. Section 6.4 introduces the developed delay model, and the overall flow of the proposed method is described in Section 6.5. Then, the experimental results are shown in Section 6.6. Finally, Section 6.7 summarizes this chapter.

6.2 Problem Definition and Design Rule Constraints

The yield enhancement problem explained in this chapter is defined as follows:

- *Given*: Original cell layout
- *Minimize*: Yield cost function
- *Subject to*:
    1. Design rule constraints
    2. Timing constraints

Design rule constraints are formulated from a constraint graph constructed from a given layout, *i.e.*, a set of polygons, as shown in Figure 6.2. The target of the proposed de-compaction method is standard cells and their heights are usually fixed. Therefore, we explain the de-compaction of only horizontal direction. Each constraint exists between the vertical edges of polygons. Each vertex of the graph corresponds to each vertical edge of polygons and each edge of the graph has a weight value which corresponds to either the value of the minimum space or width. Once a constraint graph is constructed, it is straightforward to formulate the

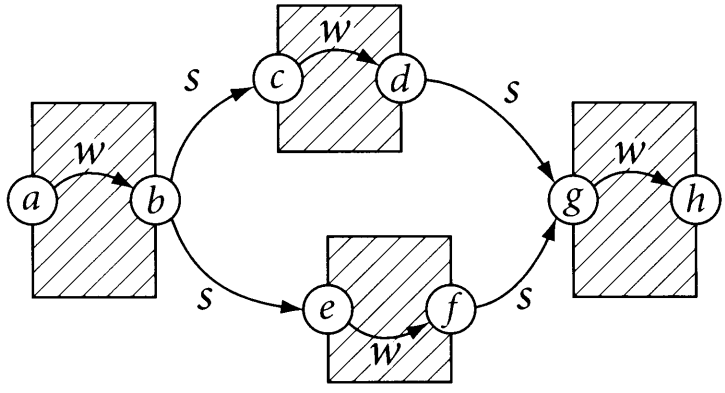


Figure 6.2 An example of a constraint graph constructed for polygons inside a given layout.

linear constraints. For example of Figure 6.2, a minimum-width constraint $b - a \geq w$, and a minimum-spacing constraint $g - d \geq s$, etc., are extracted.

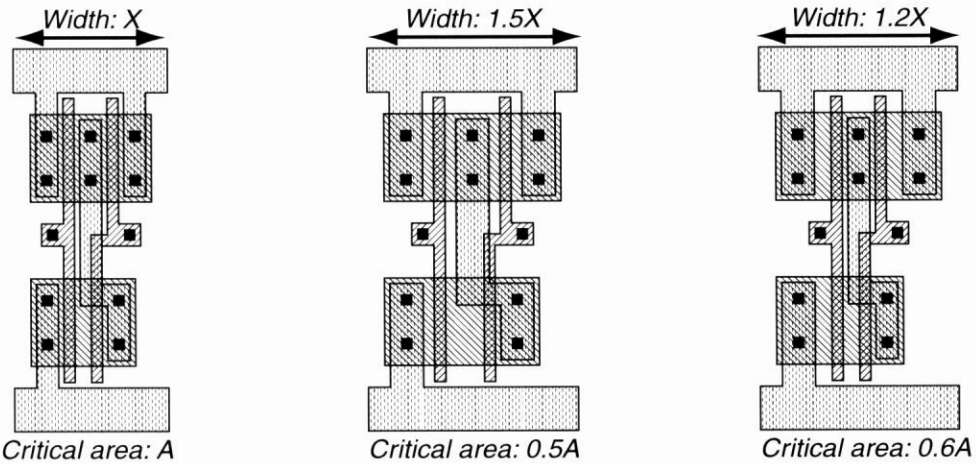
Formally speaking, a node V_i in a constraint graph represents a layout element E_i, usually an edge of a polygon or an instance of an object such as via. For example, let x_i represent the x coordinate of a layout element E_i, the minimum spacing constraint between two layout elements E_i and E_j is written as $x_j - x_i \geq d_{ij}$, where d_{ij} is the minimum distance required by a design rule. This constraint corresponds to a directed arc A_{ij}, from node V_i to V_j with weight d_{ij} in the constraint graph.

Of course, not only spacing and width design rules, but also other miscellaneous rules are formulated to create a layout without design rule violations after de-compaction. The LP formulation of the yield cost functions and the timing constraints will be explained in the following sections.

6.3 Yield Cost Metrics

6.3.1 Critical Area Minimization

In this section, we will explain how to minimize the total CA. Figure 6.3 shows the conceptual illustration of the cell layouts created by the conventional de-compaction method and the proposed timing-aware de-compaction method by minimizing the critical area. The conventional timing-unaware method increases the width and space in the original layout for CA minimization, whereas the timing-aware one does not increase the width and space of the nets which have an effect on the target delay during CA minimization to meet the given timing constraint. Therefore, the proposed method creates the yield and performance variants of



(a) The original layout.

(b) The conventional de-compaction.

(c) Timing-aware de-compaction.

Figure 6.3 The conceptual layouts of 2-input NAND created by the conventional and the timing-aware de-compaction methods.

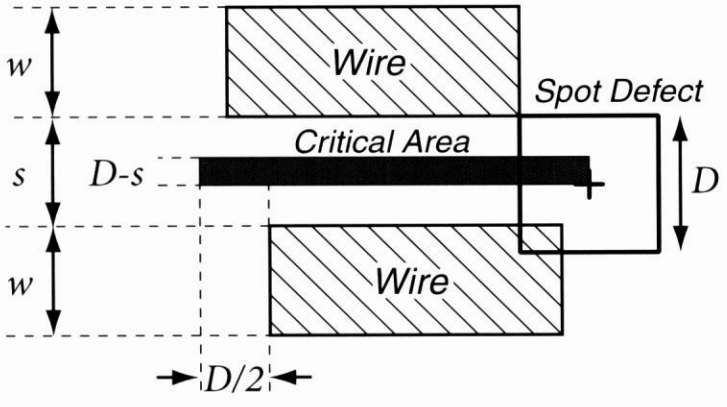
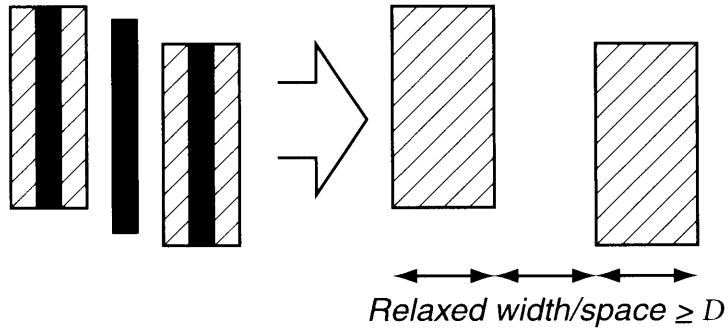
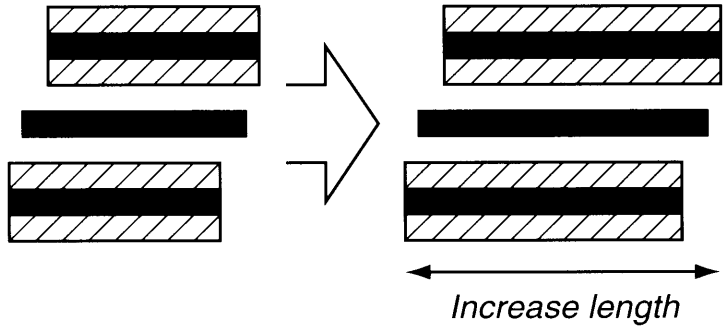


Figure 6.4 Schematic diagram of a short type critical area.

a cell layout depending on the given timing constraint. Figure 6.4 illustrates the schematic diagram of short type CA between two parallel wire segments whose width are w and spaced by s with the defect size D. We assume that the shape of the spot defect is square for simplicity of the CA calculation. If the center of the defect falls inside the CA, these two wires are connected and cause a fault. Open type CA is also defined for each single wire segment in the same manner. The total CA is calculated if the coordinates of all edges are known. In our formulation, all these coordinates are given as variables and the total CA should be minimized. Figure 6.5 shows variation of vertical and horizontal CA of both short and open type



(a) Vertical critical area.



(b) Horizontal critical area.

Figure 6.5 Variation of (a)vertical and (b)horizontal critical areas after horizontal de-compaction.

after horizontal de-compaction. The vertical CA are reduced by relaxing the width/space of polygons and finally become 0 when the width/space becomes the same value as the defect size D, whereas the horizontal CA are possibly increased since the length of horizontal wire segments are increased by horizontal de-compaction. The horizontal CA is easy to formulate as a linear function because it increases in proportion to the length. On the other hand, the calculation of the vertical CA is not so easy because it changes as shown in Figure 6.6. The critical area should be 0 if the width/space is larger than the defect size D. To realize this function, we use temporary variables r and l. These variables are defined as follows:

$$r \geq \frac{x_1 + x_2}{2}, \quad r \geq x_1 + \frac{D}{2} \tag{6.1}$$

$$l \leq \frac{x_1 + x_2}{2}, \quad l \leq x_2 - \frac{D}{2} \tag{6.2}$$

where x_1 and x_2 are the right and left edge of the polygons, respectively, as shown in Figure 6.7, and D is the defect size. Assume A is the vertical CA between these polygons, A can be written as $A \propto (r - l)$. To minimize the CA A, r should be minimized and l should be

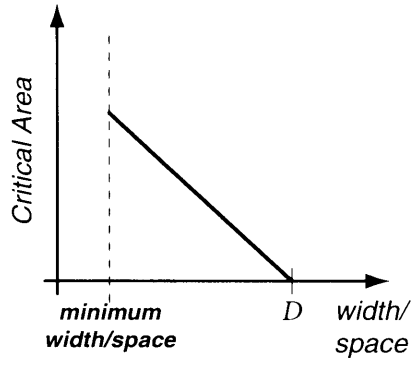


Figure 6.6 Change of the vertical critical area by the width or space.

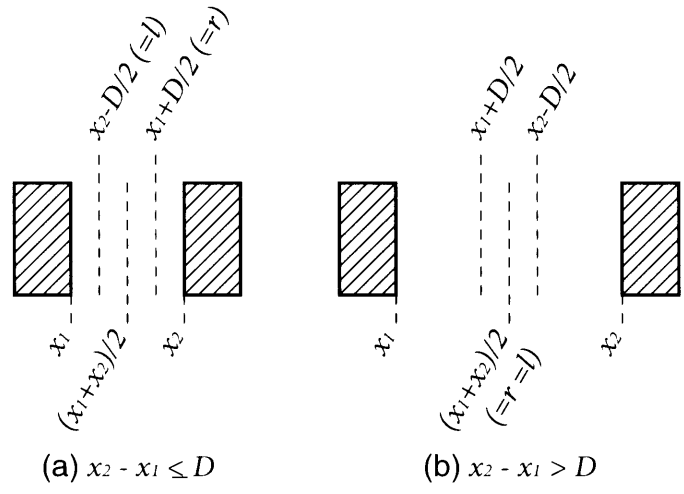


Figure 6.7 Calculation of the vertical critical area.

maximized. Under this condition, r and l are described as follows.

$$\begin{cases} r = x_1 + D/2, \quad l = x_2 - D/2 & (x_2 - x_1 \leq D) \\ r = l = (x_1 + x_2)/2 & (x_2 - x_1 > D) \end{cases} \tag{6.3}$$

Figure 6.7 also illustrates these conditions. We can formulate the cost function as a sum of CAs, each of which is formulated as Figure 6.6 using these variables.

6.3.2 OPC Relaxation

As the VLSI feature sizes are substantially smaller than the lithography wavelength, the resolution enhancement techniques (RETs) such as Optical Proximity Correction (OPC) and Phase Shift Masks become essential to draw the patterns correctly. Due to these RETs, the VLSI lithography processes become more and more complex and the cost of the masks is expected to increase steeply along with the mask data size as shown in Figure 6.8[41]. Among several RETs, OPC is one of the main contributors to the mask cost, which includes the mask data preparation and the mask writing process costs. Both of the costs increase almost in proportion to the data size of the mask writer format, which is converted by fracturing the GDSII layout data into rectangles and trapezoids. Therefore, the OPC alleviation by modifying the layout has a significant effect on the mask data size reduction. Recently, a lot of papers have been published in the area of the lithography-aware design

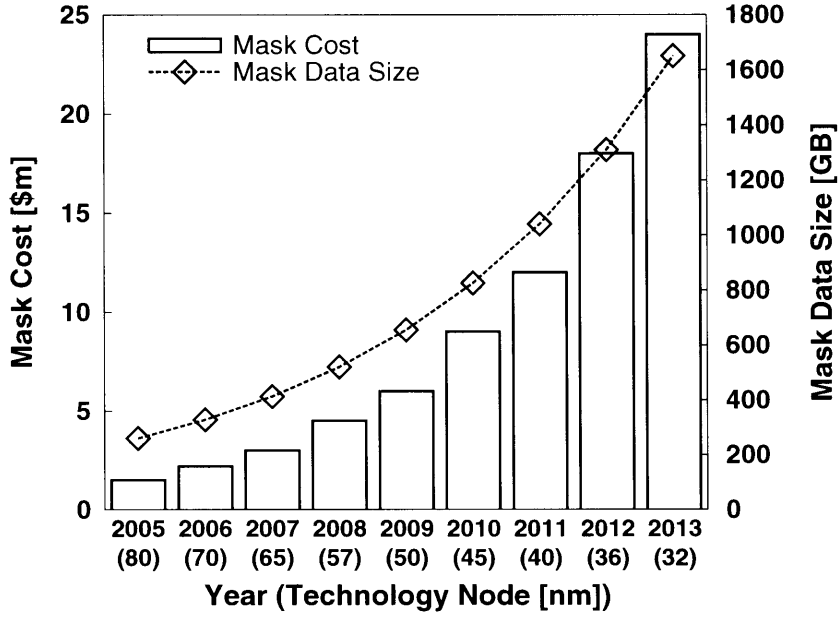


Figure 6.8 The expected mask cost and mask data size in the future technologies.

methodology[42, 43, 44, 45, 46, 16]. Among them, [42, 46] address the mask cost reduction problem considering the design intent. These OPC techniques are aware of the design informations, *e.g.*, timing slacks. Features in the layout which are not timing-critical might be expected to tolerate a larger degree of variation, and corrected by the less aggressive OPC. These papers showed significant reduction in OPC data volume with little or no increase in circuit delay. In this section, we will demonstrate the OPC relaxation in terms of the mask cost reduction using the proposed timing-aware cell layout de-compaction framework. The proposed de-compaction method expands the spacings between the polygons inside the layout and eases the optical proximity effects under given timing constraints under timing constraints. The layout after de-compaction can be printed correctly even by the modest OPC. Therefore, we can generate the OPC-friendly cell layouts and can reduce the OPC data size in terms of the fractured mask data size using the proposed method.

Figure 6.9 illustrates the conceptual example of OPC data volume reduction. By expanding the spacings between the polygons, the optical proximity effect between these polygons is reduced and the pattern modification by OPC is also reduced. The complex OPC results lead to complex mask patterning and large mask data volume. Therefore, the OPC relaxation through de-compaction is effective for OPC data volume reduction. This space expansion procedure is almost same as the wire spreading procedures to minimize the critical area between two wire segments explained in the previous section. Although the wire spreading

(a) (b)

Figure 6.9 The conceptual example of OPC data volume reduction by expanding the spacing between the polygons.

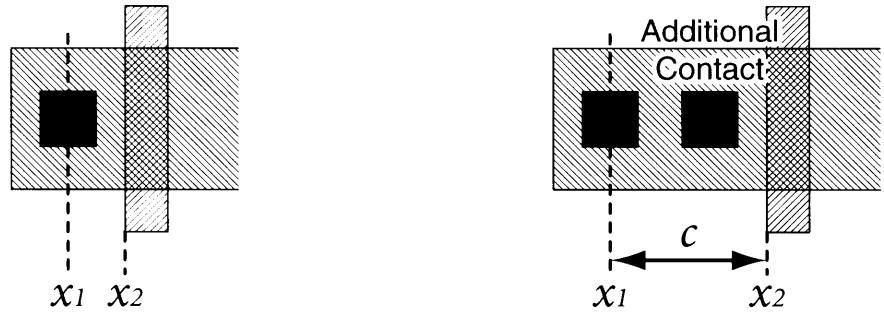
(a) (b)

Figure 6.10 The change of the OPC pattern from (a)hammer head style to (b)serif style.

procedure for critical area minimization also increases the wire width to avoid disconnection type failures, the wire width expansion is not effective for OPC data volume reduction. When the width of the wire increases wider than some threshold value, the OPCed pattern of this wire changes from so-called hammer-head style to serif style pattern as shown in Figure 6.10, and results in the data volume increase. Therefore, the proposed OPC-relaxation method executes only wire space expansion during de-compaction in the same manner as the previous section, whereas the width of the wire segments keep the same value as those of before the de-compaction.

6.3.3 Redundant Contact Insertion

In this section, we will explain how to maximize the number of the additional redundant contacts under timing and area constraints. In addition to the critical area based on the random defect related faults, there are a lot of other yield loss reasons in reality. Contact/Via open failure is one of the most important[47, 48, 49]. Due to various reasons such as cut misalignment in a manufacturing process, electro-migration and thermal stress, a contact may fail partially or completely. A well-known method to improve the contact yield is to



(a) No additional contact ($r_i = 1$). (b) An additional contact can be inserted ($r_i = 0$).

Figure 6.11 Formulation of the redundant contact insertion.

add a redundant contact adjacent to a single contact. Also for standard cells, the redundant contact insertion is commonly used to improve their yield[50]. In this section, we explain the formulation of the redundant contact insertion for standard cells under the timing-aware de-compaction framework.

The proposed method inserts redundant contacts adjacent to as many single contacts as possible under given timing and area constraints. Since two parallel contacts are assumed to be enough for yield enhancement, at most one redundant contact is inserted adjacent to each single contact. In our formulation, a Boolean variable is assigned to every single contact. Assume that the variable is written as r_i for a single contact i, this variable takes the value of 0 if a redundant contact is inserted adjacent to this single contact, otherwise 1. Therefore, to maximize the number of the redundant contacts, the cost function of the LP is formulated as follows.

$$Minimize : \sum_i r_i \tag{6.4}$$

We use Figure 6.11 to explain the constraint of the variable r_i. Figure 6.11 shows the simplified example of the contact insertion to the diffusion area. If the space between a contact and a gate becomes larger than the space for an additional contact, r_i takes the value of 0. This constraint is written as

$$\begin{cases} r_i = 1 & (x_2 - x_1 < c), \\ r_i = 0 & (x_2 - x_1 \geq c) \end{cases} \tag{6.5}$$

where c is the distance required for an additional contact. Under the condition of minimizing r_i, this constraint is expressed as follows.

$$x_2 - x_1 - c + c \times r_i \geq 0 \tag{6.6}$$

This constraint is formulated for every single contact inside the given layout. Using these constraints and the cost function, the proposed method inserts the redundant contact as many as possible under given timing constraints. Of course this optimization constraint can be used in linear combination with the critical area minimization which is explained in Section 6.3.1. Since the variables r_i are Boolean, while all the other variables are real numbers, the problem solved in the proposed method can be referred to as Mixed Integer Linear Programming (MILP).

6.3.4 Gate Layout Pattern Regularity Enhancement

Not only the functional yield considered in the previous sections, but also the parametric yield of the circuits become more and more important in the recent VLSI processes. As the VLSI technologies scale down to the subwavelength lithographic regime, the process parameter variations lead to severe variability of chip performances and both timing and power of integrated circuits are increasingly affected by process variations. Among many process variation sources, one of the most important parameter variations affecting circuit performance is the gate length variation of MOS transistors, since it directly affects both transistor switching speed and leakage power[51, 48, 52]. However, the gate Critical Dimension (CD) control in the future technologies is projected as one of the most difficult problems in International Technology Roadmap for Semiconductors(ITRS)[41] and indicated that the manufacturable solutions are not known after 2007 as shown in Figure 6.12.

Although the impacts from both systematic and random CD variations become greater and greater, it is reported that more than 50% of transistor gate length variations are due to systematic sources[52]. Empirical data show that the intra-die systematic CD variations resulting from the layout pattern non-uniformity are becoming comparable to, even dominant over lot to lot, wafer to wafer, and die to die variations[53]. Moreover, CD variation due to the depth of focus variation is known to show different behavior dependent on the pitches of CD patterns[15] and introduces the significant problems about the performance predictability. To reduce the systematic process variations, the regular layout has been shown to be effective[54]. Therefore, various regular design styles have been suggested[55, 56] and Restrictive Design Rules (RDR) [57, 14] have also been utilized to improve pattern printability and reduce variations. As for the standard cell layouts, the technology migration technique with on-pitch constraint has been proposed in [58]. Although the conventional technology migration techniques use linear shrink in conjunction with legalization technique to clean up

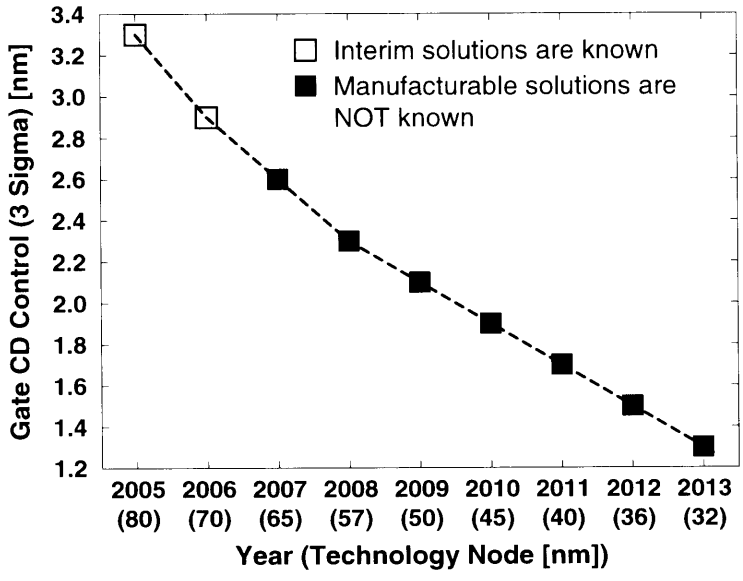


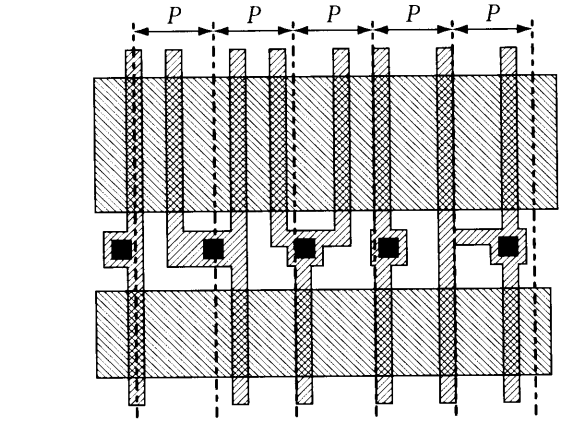
Figure 6.12 Required gate CD control in the future technologies.

the ground rule violations, this technique legalizes a given layout in order to meet on-pitch constraints with minimum layout perturbation.

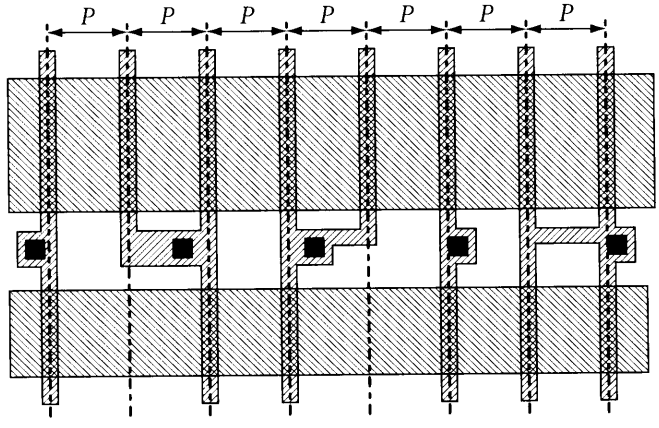
In this section, we propose a gate layout pattern regularity enhancement method to reduce the systematic variation of the gate CD. The proposed method performs a de-compaction of a cell layout considering the on-pitch constraints and enhances the pattern regularity under given timing constraints using LP. In contrast to [58] which minimizes the layout perturbation to meet the design rules and on-pitch constraints during technology migration, the proposed method minimizes the regularity cost under the design rules and timing constraints during de-compaction. Using the proposed timing-aware regularity enhancement method, we can explore the trade-off between performance and regularity cost, and can pick up the regularity variants from the trade-off curve.

To enhance the regularity, gate patterns in a cell layout have to meet three restrictions: fixed gate length, single orientation, and uniform pitch. We assume that the gate patterns in a given cell layout always have first two factors: fixed gate length and single orientation. Figure 6.13 shows the conceptual example of the regularity enhancement. As shown in this figure, the gate patterns in a layout are aligned in regular pitch during de-compaction under design rule and timing constraints.

The cost of the regularity is defined as shown in Figure 6.14. A piecewise linear cost function is used in the proposed method. When the gate layout pattern is placed in the



(a) The given original layout.



(b) The layout after regularity enhancement.

Figure 6.13 The conceptual example of gate layout pattern regularity enhancement for the regular pitch P by the proposed regularity enhancement method.

regular pitch, the cost is 0. As the distance between the gate and the regular pitch increases, the regularity cost increases linearly. This cost function is equivalent to the distance from the nearest regular pitch. The LP formulation of this cost function is explained in the following paragraph.

Let E_{gate} denote the set of layout elements of transistor gate, the regularity cost used in this paper is written as

$$\sum_{E_i^y \in E_{gate}} |x_i^y - k_i P|, \tag{6.7}$$

where x_i^y is an x coordinate of a gate element E_i^y, P is the regular pitch and k_i is an integer variable. This objective function is linearized by introducing two variables L_i and R_i for each

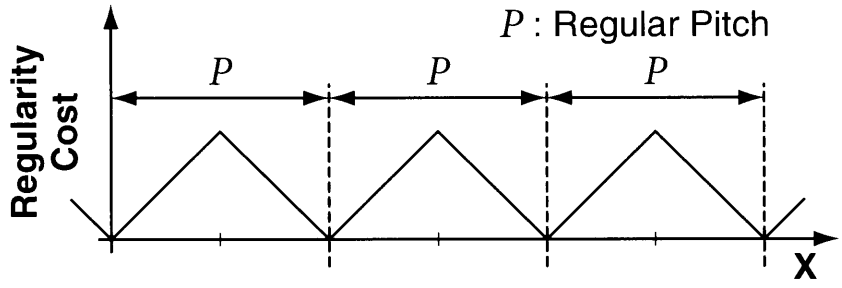


Figure 6.14 The regularity cost function used in the proposed regularity enhancement method.

element E_i^g. The linear formulation of this minimization constraint is written as follows.

$$Minimize \quad : \quad \sum_{E_i^g \in E_{gate}} (R_i - L_i) \tag{6.8}$$

$$Subject\ to \quad : \quad L_i \leq x_i^g, \quad L_i \leq k_i P \tag{6.9}$$

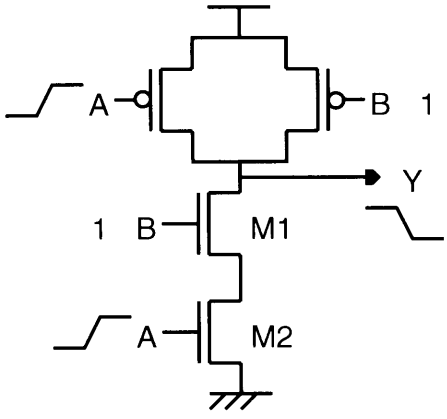
$$R_i \geq x_i^g, \quad R_i \geq k_i P \tag{6.10}$$

In this formulation, L_i is smaller than both x_i^g and $k_i P$, whereas L_i is maximized by the minimization constraint (6.8). Therefore, L_i is always equal to the smaller one of x_i^g or $k_i P$. On the other hand, R_i is larger than both x_i^g and $k_i P$, whereas R_i is minimized. Therefore, R_i is always equal to the larger one of them. Since k_i is an integer variable, the distance between a gate and the nearest regular pitch is calculated. By minimizing this cost function, we can optimize the regularity of the given cell layout. Since the proposed formulation includes the integer variables k_i whereas all the other variables are real numbers, this formulation is also referred to as Mixed Integer Linear Programming (MILP).

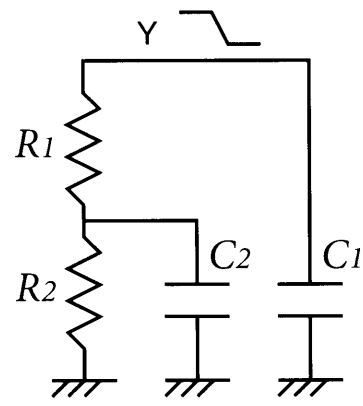
6.4 Delay Model

We need a linear delay model to formulate the timing constraint as LP. The well-known linear timing approximation is Elmore delay model. Figure 6.15 (a) illustrates a simple example of 2-input NAND. When the input signal A rises from logic level 0 to 1, then the output signal Y falls to logic level 0. In this situation, this transistor network is replaced by an RC network shown in Figure 6.15 (b) which consists of ON resistors R_1 and R_2 of the transistors M1 and M2, respectively, and parasitic capacitors C_1 and C_2. Using Elmore delay model, we can calculate the fall delay of the output signal Y as follows.

$$Delay_{A \to Y} = (R_1 + R_2) \times C_1 + R_2 \times C_2 \tag{6.11}$$



(a) Transistor network of 2-input NAND.



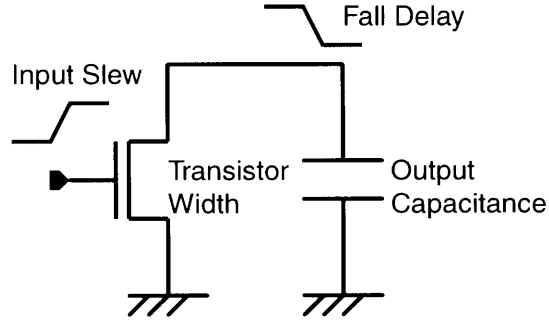
(b) RC network of 2-input NAND for fall delay of output signal Y.

Figure 6.15 An example of 2-input NAND and its RC network for calculating Elmore delay.

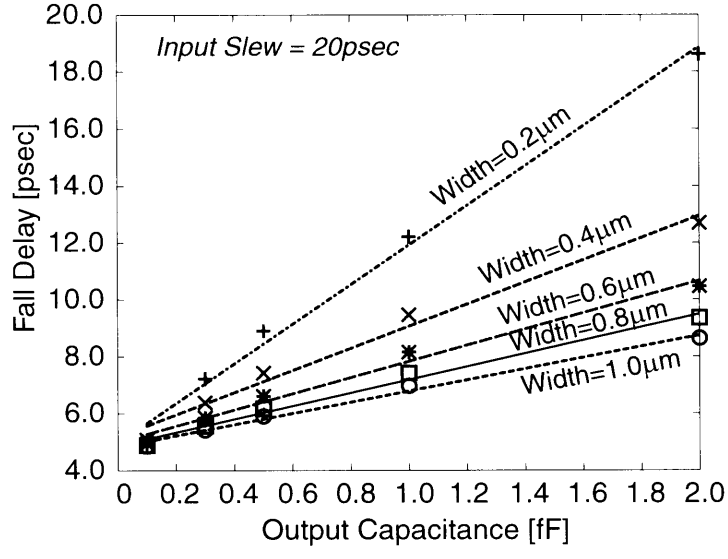
However, this model is not accurate enough to model the transistors of the recent deep sub-micron technologies. Therefore, we develop a new delay model which only calculates the delay difference induced by the difference of parasitic elements after de-compaction. Since the proposed method performs a de-compaction of a given original layout, we can extract the original parasitic elements and simulate the original delay values from this layout using a SPICE-like circuit simulator. Once the original delay value is simulated, a delay difference by the difference of the parasitic capacitances is approximated by a linear function. Figure 6.16 shows the graphs of fall delay of an N type transistor versus output capacitance. The schematic of the simulated circuit is shown in Figure 6.16 (a). Figure 6.16 (b) shows the delay variation by changing the width of the transistor and (c) shows the delay variation by changing the value of gate input slew. In both cases, the delay increases almost in proportion to the output capacitance, and the slope values are different from each other. In addition, the slew value of the output signal can also be approximated as a linear function to the output capacitance. The slope value of the slew is also dependent on the transistor width and the gate input slew. Figure 6.17 (a) shows the output slew variation by changing the width of the transistor and (b) shows the output slew variation by changing the value of gate input slew. Therefore, these slope values are calculated in advance and stored as a table of transistor width and input slew for P and N type transistors, respectively.

Using these slope values, the procedure of delay or slew increase calculation is written as follows.

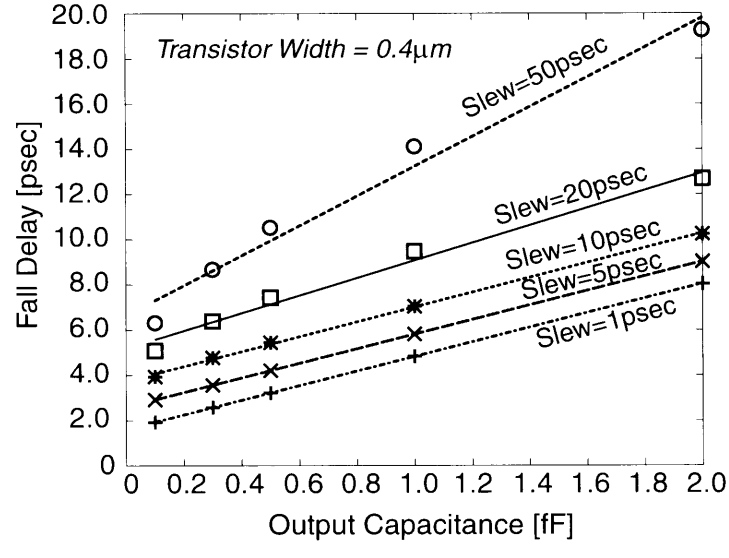
1. Convert a given transistor network into an RC network and formulate the Elmore delay



(a) Test circuit.

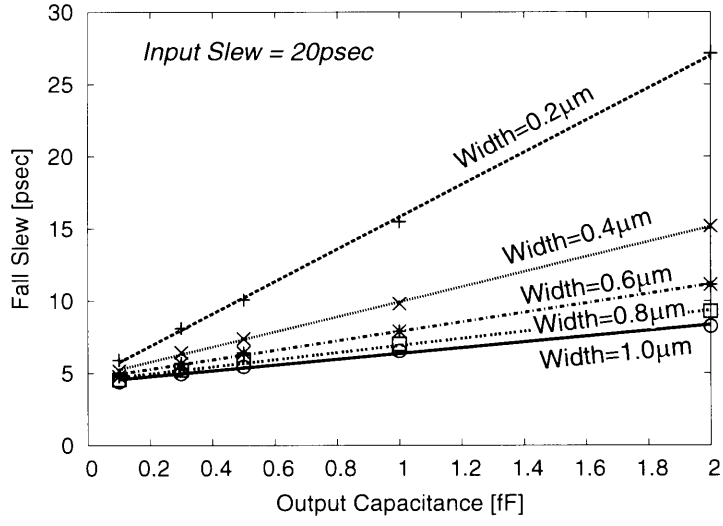


(b) Output delay variation by transistor width.

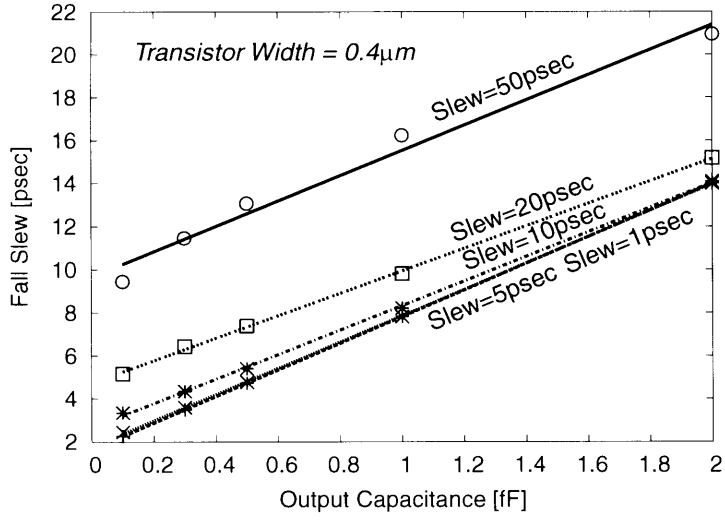


(c) Output delay variation by input slew.

Figure 6.16 Preliminary results of delay variation by changing the transistor width and the input slew.



(a) Output slew variation by transistor width.



(b) Output slew variation by input slew.

Figure 6.17 Preliminary results of output slew variation by changing the transistor width and the input slew.

function in the same manner as shown in Figure 6.15.

2. Replace the values of ON resistors by the slope values that are determined by the values of the width and the gate input slew of each transistor.

3. Replace the values of parasitic capacitors by the difference of each parasitic capacitor after de-compaction.

For example of Figure 6.15, the fall delay increase $\Delta Delay_{A \rightarrow Y}$ is described as a linear func-

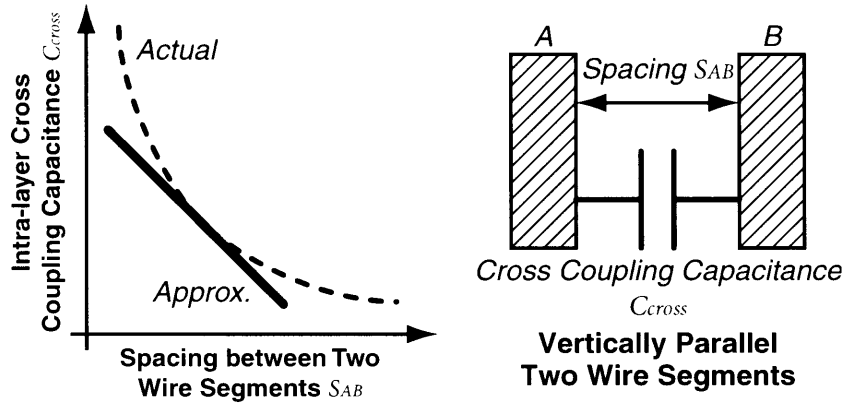


Figure 6.18 The linear approximation of the intra-layer cross coupling capacitance between two vertically parallel wire segments.

tion of parasitic capacitance differences as follows,

$$\Delta Delay_{A\to Y} = (k_1 + k_2) \times \Delta C_1 + k_2 \times \Delta C_2 \tag{6.12}$$

where k_1 and k_2 are the delay slope values of the transistors M1 and M2, respectively, and ΔC_1 and ΔC_2 are the differences of the parasitic capacitors C_1 and C_2 after de-compaction, respectively. Using this model, we can describe the timing constraints by a linear inequation as

$$Delay_{A\to Y}^{initial} + \Delta Delay_{A\to Y} \leq Delay_{A\to Y}^{target} \tag{6.13}$$

where $Delay_{A\to Y}^{initial}$ and $Delay_{A\to Y}^{target}$ are the original and the target cell delay, respectively. The increase of the output slew is also modeled in the same manner.

The difference of the parasitic capacitances also has to be linearly modeled by the coordinates of polygons in the original layout. The diffusion capacitance is calculated by a linear function of the area and the perimeter of the diffusion region. The parasitic capacitance of wires to ground or between overlapped layers is also calculated by a linear function of the area of the overlapped regions. For intra-layer cross coupling capacitances, it is easy to extract the capacitances between horizontally parallel wire segments because the de-compaction of the horizontal direction only increases the length of the parallel wires and this type of capacitance is mainly proportional to the length of the parallel wires. However, the coupling capacitances between vertically parallel wire segments are not so easy to calculate because the distance between these two wires are increased by the horizontal de-compaction and the capacitance value is not proportional but inversely proportional to the distance. Therefore, we approximate the value of this type of capacitance by linear function which is proportional to the

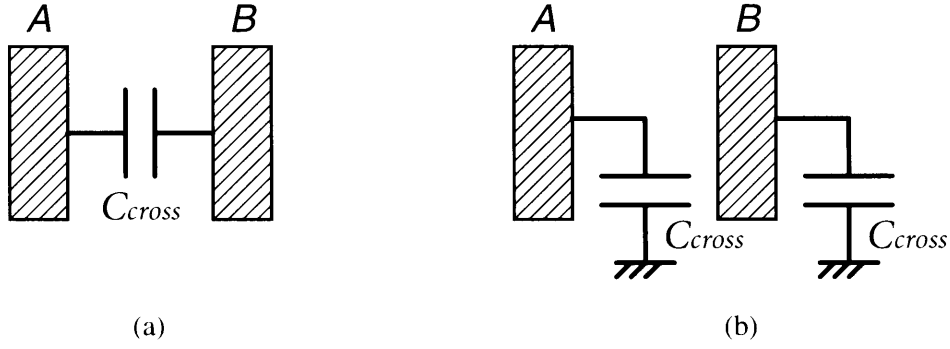


Figure 6.19 Approximation of the cross coupling capacitance between two signals A and B.

distance with negative slope value as shown in Figure 6.18. A capacitor between two signals is approximated by two capacitors from each signal to ground as shown in Figure 6.19. Both of them have the same capacitance as the original capacitor. Experimental results will show that these approximations are accurate enough to calculate the timing constraints under the proposed timing-aware de-compaction framework. At this stage, we can describe the timing constraints as linear functions of the coordinates of the polygons in the layout and can formulate them into the LP problem.

This model requires the slew of all the gate input signals in advance to determine the slope values of all the transistors. Therefore, this model describes the delay and slew value of single-stage transistor networks, since all the gate input waveforms are given for these cells. For multi-stage cells, on the other hand, the slew value of an inner node, which is an output of one stage and inputs to other stages, is not given in advance. Therefore, we have to approximate the change of the slew value of this inner node to apply the proposed model to multi-stage cells. The preliminary experiment, however, shows that the changes of the slew values of inner nodes caused by our de-compaction method are within several percents and these slew changes have little effects on the delay changes. For this reason, we use the slew values of the inner nodes of the original layout for the slew values of the inner nodes during de-compaction in the case of the multi-stage cells. These original slew values of the inner nodes are simulated and saved at the same time of the original delay simulation. Experimental results will show that even this simple approximation realizes accurate timing constraints for the multi-stage cells.

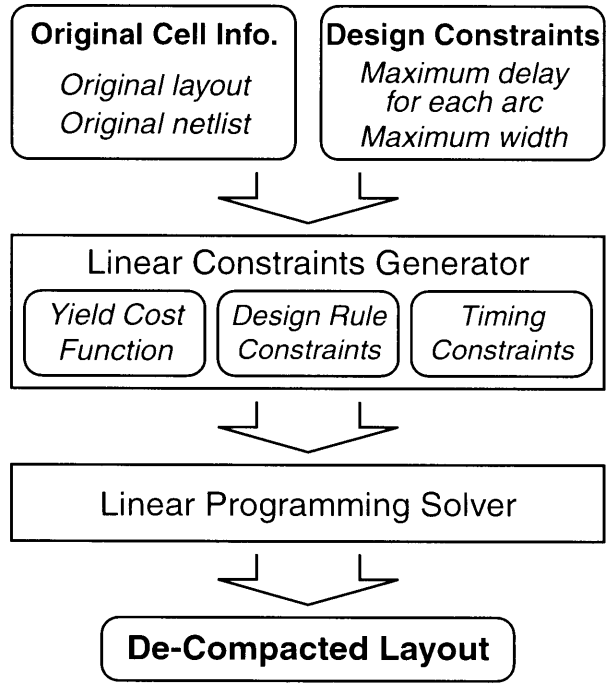


Figure 6.20 The overall flow diagram of the proposed timing-aware yield enhancement method.

6.5 Overall Flow

Figure 6.20 shows the overall flow diagram of the proposed method. The input to the proposed method is the original cell information and design constraints. The original cell information includes the original GDSII format cell layout for polygon information and the netlist of the cell in SPICE format for transistor connection information. Design constraints include the target cell delay for each timing arc and the maximum cell width. A timing arc is defined as a signal flow from an input to an output on a cell, *e.g.*, A rise $\rightarrow$ Y fall. These maximum delay and area values are given as plain text format in a specific syntax. Although the maximum width constraint was not explained in the previous sections, it can be formulated as a part of the design rule constraints. Using these informations, the linear constraints generator, which implements the proposed timing-aware cell layout de-compaction for yield optimization, formulates the constraints explained in the previous sections and generates an input LP file for the LP solver. The yield cost function is selected from CA minimization, OPC relaxation, redundant contact insertion, or gate layout pattern regularity enhancement. Of course, the linear combination of these cost functions can be used as the yield cost function. Then, the LP solver searches for the solution of the generated LP problem. Finally, a GDSII file of the cell layout after de-compaction is created from the solution of LP solver

Table 6.1 The topological characteristics of the benchmark circuits used for the experiment of the critical area minimization.

Circuit	*Explanation*	*#stage*	*#trans.*
NAND3_1	3-input NAND	1	6
NAND3_2	3-input NAND (buffered)	1	12
NAND4_3	4-input NAND (buffered)	1	36
NOR4_1	4-input NOR	1	8
NOR4_2	4-input NOR (buffered)	1	28
ON2222_3	A series-parallel circuit	1	56
ADDH_1	Half Adder	4	14
OR3_2	3-input OR (buffered)	2	23

which is equivalent to the coordinates of the polygons inside the layout. During final GDSII file generation, the width of the outside frame of the generated cell is enlarged to fit the multiple of the fixed pitch to be used as a standard cell layout.

6.6 Experimental Results

6.6.1 Critical Area Minimization

The proposed timing-aware de-compaction method for critical area minimization was implemented to show its effectiveness. In this experiment, we used ILOG *CPLEX 9.1*[27] for an LP solver and 8 cells from a standard-cell library of a 90nm technology were used as benchmarks. Among these 8 cells, 6 cells are single-stage and the others are multi-stage. Tables 6.1 and 6.2 summarize the characteristics of these cells. These tables show the circuit name, the explanation of each circuit, the number of the stages inside each circuit, the number of transistors, the original cell delay value, the original cell area, and the original critical area. $Delay_{orig}$ column shows the original delay of a timing arc. The delay values of these arcs were constrained in this experiment. To calculate the original cell delay, a netlist with parasitic capacitances is extracted using Mentor Graphics *Calibre xL*[59] and simulated using Synopsys *HSPICE*[60]. The tables of the delay slope value(Figure 6.16) for P and N type transistors are also calculated using *HSPICE* in advance. In this experiment, we did not connect an additional capacitor to the output net to clarify the effect of the intra-cell parasitic elements. The defect size used in this experiment is 1.5 times larger than the minimum

Table 6.2 The performance characteristics of the benchmark circuits used for the experiment of the critical area minimization.

Circuit	$Delay_{orig}$ *[psec]*	$Area_{orig}$ $[\mu m^2]$	CA_{orig} $[\mu m^2]$
NAND3_1	33.05	3.70	0.97
NAND3_2	34.56	6.53	1.97
NAND4_3	53.11	22.15	10.97
NOR4_1	73.65	4.76	1.30
NOR4_2	65.95	17.41	8.47
ON2222_3	64.83	28.75	9.92
ADDH_1	78.56	8.77	2.38
OR3_2	92.85	12.52	4.17

width/space of the first metal layer and the CAs are calculated only for the first metal layers. All the experiments were conducted on a Linux machine with Xeon 3.4GHz processor and 2GB of RAM.

Tables 6.3 and 6.4 summarize the results of the proposed timing-aware de-compaction method. These tables show the target and the actual delay value, the cell area, and the CA of the generated cell layouts. Delay error is calculated by $(t_{target} - t_{actual})/t_{target} \times 100$, where t_{target} and t_{actual} are the target and the actual delay, respectively. "No constraint" in the column of *Target* means that no timing constraints were set in this case. Because the vertical CA decreases but the horizontal CA possibly increases by horizontal de-compaction, there must be an optimal value of the total CA. The value of CA in the no constraint case is the minimum CA value for each cell. The runtime to create the de-compacted layout is about 0.1 second even for the largest example of ON2222_3 which consists of 56 transistors. The runtime for creating the tables of slope values and the first *HSPICE* simulation for each cell is excluded because they are conducted just once in advance. The delay values of the generated layouts are also simulated by *HSPICE* using a netlist extracted by *Calibre xL*. The errors of the target and actual delay values are less than 1% for most cases and the average absolute error is 0.49%. Figure 6.21 plots the target and the simulated delay values in the case of the single-stage cell NOR4_1 when the input signal to the P type transistor connected to VDD falls from logic level 1 to 0. The simulated delay values show good accordance with the target delay values. Figure 6.22 also plots the target and the simulated delay values in the case of the multi-stage cell ADDH_1. These results show that the developed delay model is accurate

Table 6.3 The delay accuracy of the proposed timing-aware critical area minimization method.

Circuit	*Target [psec]*	*Actual [psec]*	*error [%]*
NAND3_1	35	34.98	0.06
	37	36.77	0.63
	No constraint	37.92	—
NAND3_2	35	34.95	0.14
	36	35.76	0.67
	No constraint	36.54	—
NAND4_3	54	53.81	0.35
	55	54.72	0.51
	No constraint	55.83	—
NOR4_1	76	75.59	0.54
	80	79.62	0.48
	No constraint	81.33	—
NOR4_2	67	67.47	-0.70
	70	68.87	1.64
	No constraint	70.06	—
ON2222_3	66	65.63	0.56
	67	66.18	1.25
	No constraint	67.65	—
ADDH_1	79	79.08	-0.10
	80	80.03	-0.05
	No constraint	80.91	—
OR3_2	94	94.06	-0.06
	96	95.88	0.13
	No constraint	97.91	—
average	—	—	0.49

Table 6.4 Results of the critical area minimization by the proposed method.

Circuit	*Target [psec]*	*Area [μm^2]*	*increase [%]*	*CA [μm^2]*	*reduction [%]*
NAND3_1	35	5.70	54.05	0.47	51.55
	37	5.70	54.05	0.47	51.55
	No constraint	5.70	54.05	0.47	51.55
NAND3_2	35	8.11	24.20	1.56	20.81
	36	8.49	30.02	1.47	25.38
	No constraint	8.49	30.02	1.47	25.38
NAND4_3	54	23.87	7.77	10.29	6.20
	55	24.81	12.01	10.10	7.93
	No constraint	25.58	15.49	10.00	8.84
NOR4_1	76	5.71	19.96	0.92	29.23
	80	6.02	26.47	0.85	34.61
	No constraint	6.02	26.47	0.85	34.61
NOR4_2	67	19.33	11.03	7.59	10.39
	70	20.25	16.31	7.30	13.81
	No constraint	20.76	19.24	7.27	14.17
ON2222_3	66	31.20	8.52	9.11	8.17
	67	31.29	8.83	8.94	9.88
	No constraint	31.68	10.19	8.86	10.69
ADDH_1	79	10.94	24.74	1.87	21.43
	80	10.74	22.46	1.82	23.53
	No constraint	10.74	22.46	1.82	23.53
OR3_2	94	14.91	19.09	3.04	27.10
	96	15.62	24.76	2.94	29.50
	No constraint	15.78	26.04	2.93	29.74
average	—	—	25.50*	—	24.81*

* : An average of the no constraint cases

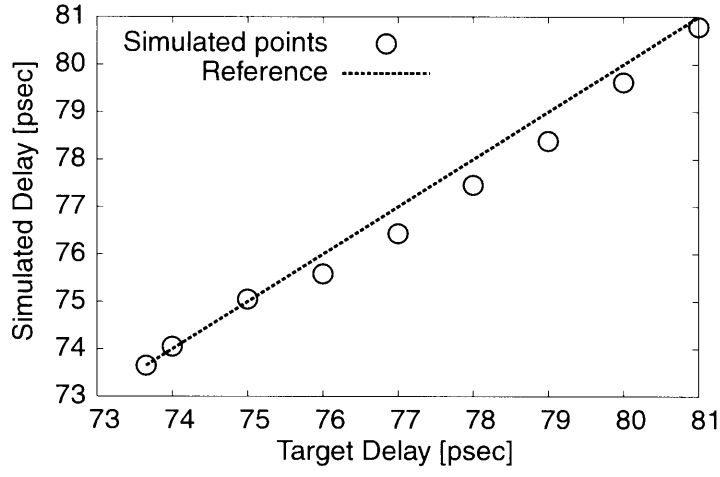


Figure 6.21 Accuracy of the proposed delay model in the case of the single-stage cell NOR4_1.

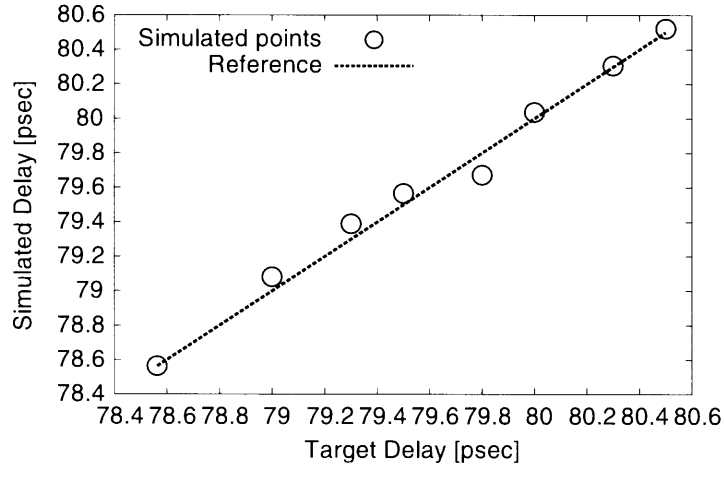
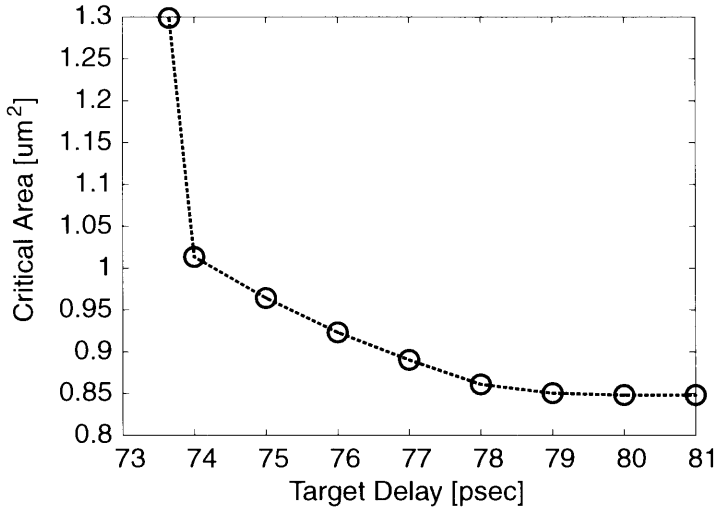


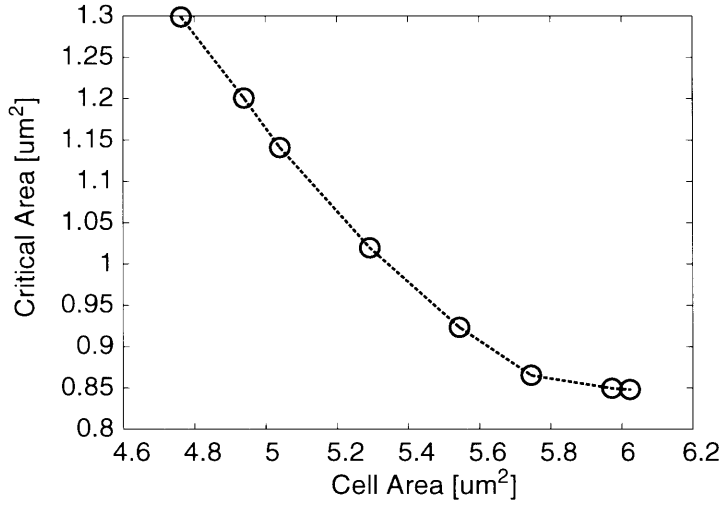
Figure 6.22 Accuracy of the proposed delay model in the case of the multi-stage cell ADDH_1.

enough for the proposed de-compaction method and can be applied to both single and multi-stage cells.

After de-compaction, the cell areas increase about 10 to 50% and the CAs decrease about 10 to 50% depending on the cells and the constraints. The average values of the cell area increase and the CA reduction without timing constraints are about 26% and 25%, respectively. As the timing constraint becomes tight, the cell area increase and CA reduction become small. In the cases of NAND3_1, NAND3_2, NOR4_1, and ADDH_1, the proposed method creates the cells with smaller delay than the no constraint case while their area and CA is equal to that of the no constraint case. As a special case, cell area of ADDH_1 with 79 psec delay constraint is larger than that of the 80 psec constraint. These results show the fact that the



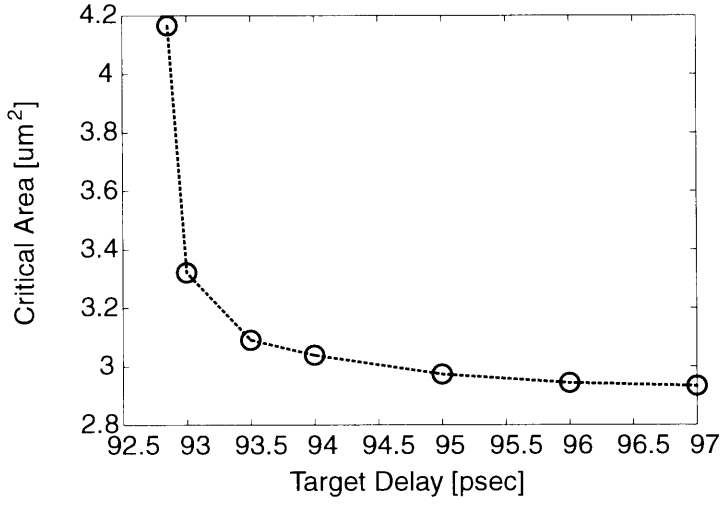
(a) Target delay versus critical area.



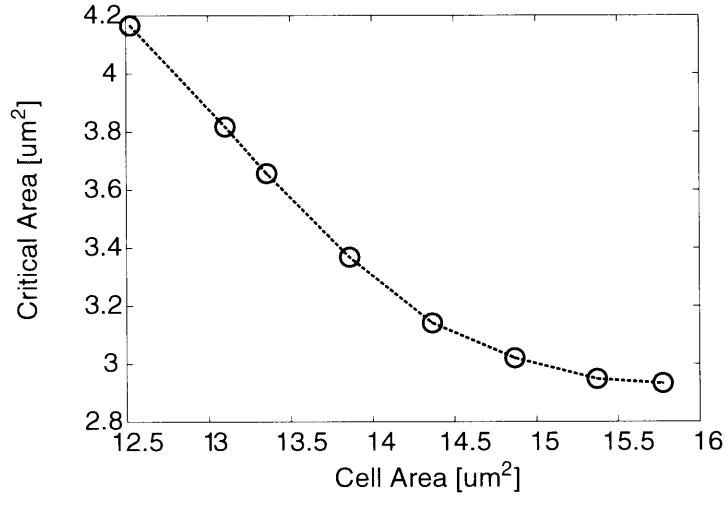
(b) Cell area versus critical area.

Figure 6.23 Trade-off curves of (a)target delay versus CA and (b)cell area versus CA in the case of the single-stage cell NOR4_1.

layout impacts on the timing are different by location, and the significance of the timing consideration during layout de-compaction. Figure 6.23 and Figure 6.24 show the trade-off curves of target delay versus CA and cell area versus CA in the cases of the single-stage cell NOR4_1 and the multi-stage cell OR3_2, respectively. As shown in these figures, the critical areas are minimized under given timing or area constraints for both cases. The conventional simple de-compaction method can not create these various yield-optimized cell layouts. On the other hand, the proposed method can pick up the yield and performance variants of a cell layout from these trade-off curves.



(a) Target delay versus critical area.



(b) Cell area versus critical area.

Figure 6.24 Trade-off curves of (a)target delay versus CA and (b)cell area versus CA in the case of the multi-stage cell OR3_2.

6.6.2 OPC Relaxation

This section shows the experimental results of the proposed timing-aware OPC relaxation method. In this experiment, we also used ILOG *CPLEX 9.1*[27] for an LP solver, and 20 cell layouts from a standard-cell library of a 90nm technology were used as benchmarks. The maximum wiring space allowed during de-compaction is defined as 1.5 times larger value than the minimum space of the first metal layer, whereas the width of the wire segments keep the same value as those of before the de-compaction as explained in Section 6.3.2. The OPC cost in terms of the fractured mask data size is calculated only for the first metal layer. All

the experiments were conducted on a Linux machine with Xeon 3.4GHz processor and 2GB of RAM. The runtime to perform a cell layout de-compaction was less than 0.1 seconds even for the largest example which consists of 32 transistors.

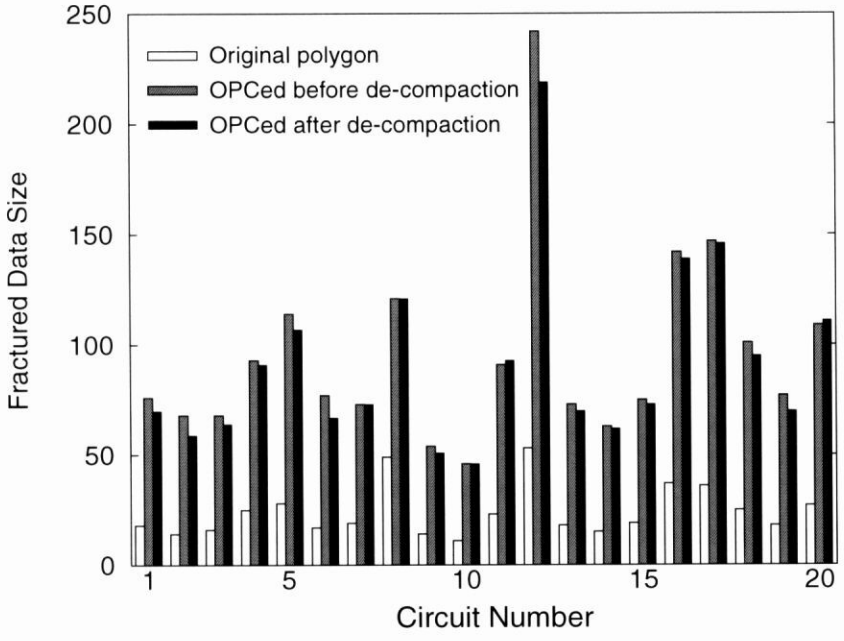
The fractured mask data size comparison between before and after de-compaction is shown in Figure 6.25. These two graphs show the fractured mask data size for 20 cell layouts in 90nm and 65nm technology, respectively. The 65nm cell layouts used in this experiment are prepared by shrinking the 90nm cell layouts. The OPC simulation and the fractured mask data size calculation is conducted using Mentor Graphics *Calibre*[61]. The lithographic condition used in this experiment is summarized as follows.

- Lithography Wavelength: 193nm
- Numerical Aperture: 0.8
- Mask Reduction Factor: 4

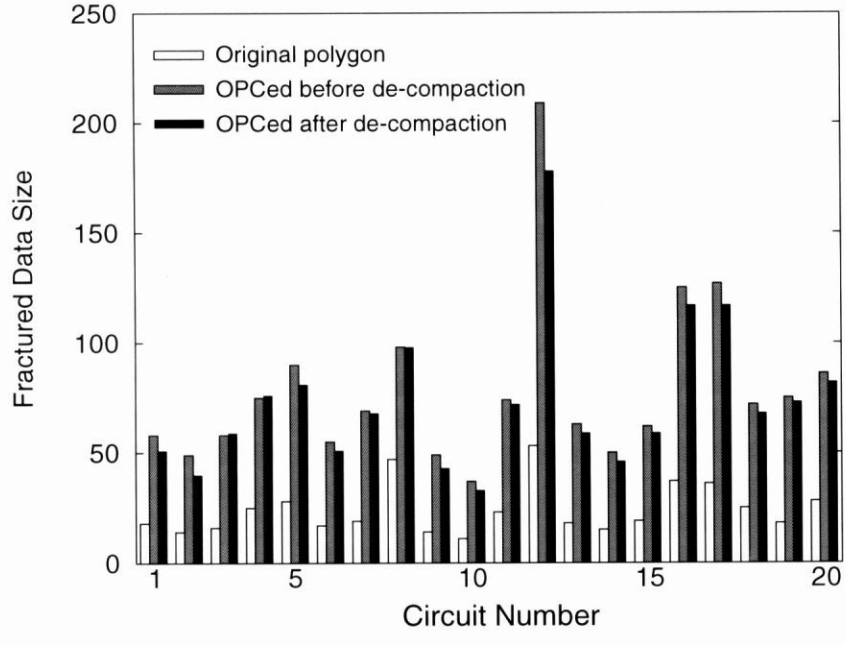
In this experiment, all cells are allowed 10% delay increase during de-compaction. However, 13 cells among 20 cells were enlarged to the maximum width through the de-compaction under this constraint. Therefore, the average delay increase of these 20 cells after de-compaction was about 6.73%. Under this condition, the average area overhead was 31.2%. As shown in these graphs, the fractured mask data size is reduced in the case of almost all cells for both 90nm and 65nm technologies. The data size was reduced 4.28% and 6.65% on an average in the case of 90nm and 65nm technology, respectively, and the maximum reduction ratios were 13.2% and 18.4%, respectively. The reduction of fractured mask data size directly translates to lower costs through shorter mask data preparation and mask writing time, and higher mask yield.

Figure 6.26 shows the expected maximum and average fractured mask data size reduction ratio depending on the technology nodes from 90nm to 65nm. The cells used in this experiment are also prepared by shrinking the 90nm cell layouts. All the simulations are conducted under the same lithographic conditions as explained before. As shown in this figure, the proposed de-compaction method for OPC mask data volume reduction is expected to be more effective in the small feature size technology.

Figure 6.27 illustrates an example of OPC results before and after de-compaction in the case of 65nm cell layout. From this figure, we can see that some pattern modifications by OPC is effectively removed by the de-compaction with small delay increase, particularly on the corner of wires.



(a) 90nm technology.



(b) 65nm technology.

Figure 6.25 The fractured mask data size of 20 cells in (a)90nm and (b)65nm technology in the case that 10% delay increase is allowed.

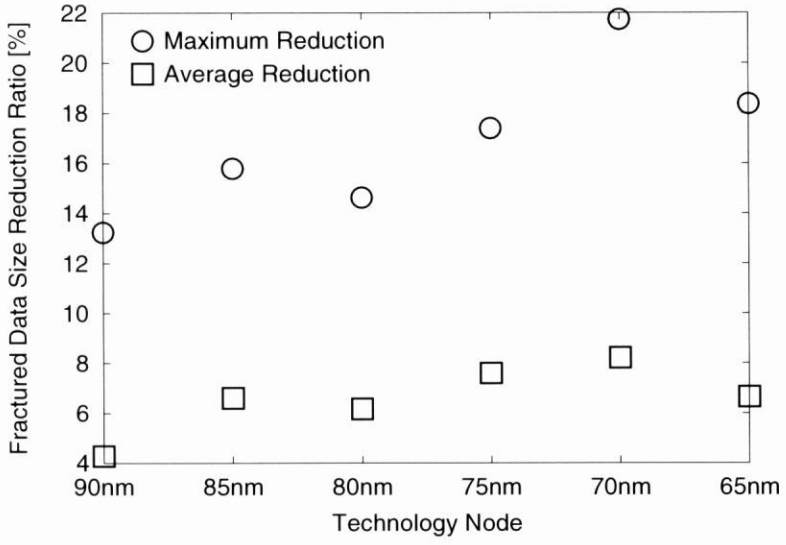
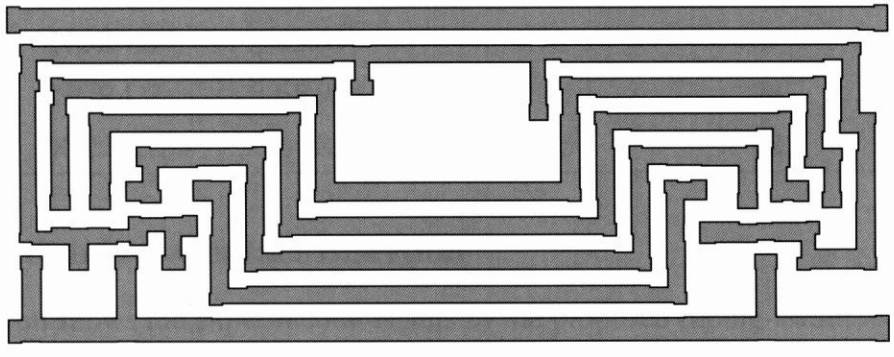
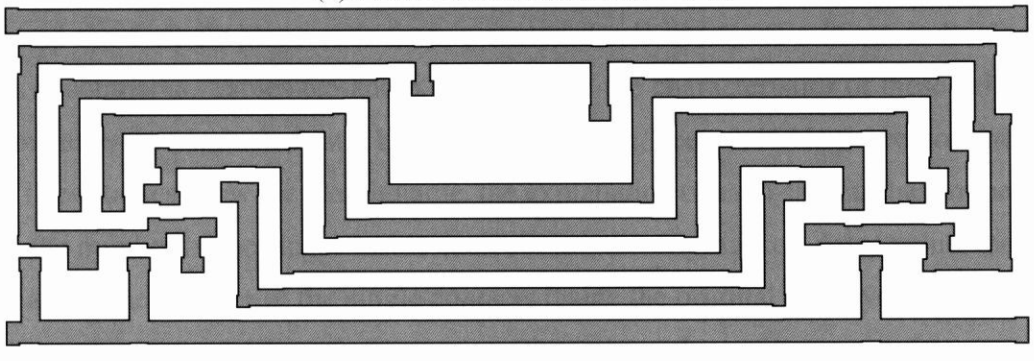


Figure 6.26 The reduction ratio of the fractured mask data size after de-compaction depending on the technology nodes.



(a) Fractured mask data size = 242.



(b) Fractured mask data size = 219, Delay increase = 3.4%, Area increase = 15.7%.

Figure 6.27 An example of OPC results in 65nm technology (a)before and (b)after de-compaction.

Table 6.5 The topological characteristics of the benchmark circuits used for the experiment of redundant contact insertion.

Circuit	*Explanation*	*#trans.*	*#stage*
NAND3_1	3-input NAND	6	1
NAND3_2	3-input NAND (buffered)	12	1
NAND4_3	4-input NAND (buffered)	36	1
NOR4_1	4-input NOR	8	1
NOR4_2	4-input NOR (buffered)	28	1
ON2222_3	A series-parallel circuit	56	1

Table 6.6 The performance characteristics of the benchmark circuits used for the experiment of redundant contact insertion.

Circuit	$Delay_{orig}$ *[psec]*	$Area_{orig}$ $[\mu m^2]$	*#Single Contact*
NAND3_1	33.05	3.70	7
NAND3_2	34.56	6.53	10
NAND4_3	53.11	22.15	20
NOR4_1	73.65	4.76	9
NOR4_2	65.95	17.41	28
ON2222_3	64.83	28.75	62

6.6.3 Redundant Contact Insertion

This section shows the experimental results of the proposed timing-aware redundant contact insertion method. In this experiment, we also used ILOG *CPLEX 9.1*[27] for an MILP solver and the 6 single-stage cells from a standard-cell library of a 90nm technology were used as benchmarks. Tables 6.5 and 6.6 summarize the characteristics of these cells. All the experiments were conducted on a Linux machine with Xeon 3.4GHz processor and 2GB of RAM. These tables show the circuit name, the explanation of each circuit, the number of transistors, the number of the stages inside each circuit, the original cell delay value, the original cell area, and the number of the single contacts inside the original cell layouts. $Delay_{orig}$ column shows the original delay of a timing arc. The delay values of these arcs were constrained in this experiment.

Tables 6.7 and 6.8 show the results of the proposed timing-aware redundant contact insertion method. These tables show the target and the actual delay value, the cell area, and the number of the additional contacts inside the generated cell layouts. Delay error is calculated

Table 6.7 The delay accuracy of the proposed timing-aware redundant contact insertion method.

Circuit	*Target [psec]*	*Actual [psec]*	*error [%]*
NAND3_1	36	36.18	-0.50
	39	39.65	-1.64
	No constraint	41.78	—
NAND3_2	36	35.47	1.49
	39	37.79	3.20
	No constraint	42.61	—
NAND4_3	55	54.75	0.46
	60	57.97	3.50
	No constraint	65.83	—
NOR4_1	78	78.31	-0.40
	86	85.59	0.48
	No constraint	93.88	—
NOR4_2	71	71.31	-0.43
	77	75.67	1.76
	No constraint	83.98	—
ON2222_3	71	69.18	2.63
	77	72.70	5.91
	No constraint	81.75	—
average	—	—	1.87

by $(t_{target} - t_{actual})/t_{target} \times 100$, where t_{target} and t_{actual} are the target and the actual delay, respectively. "No constraint" in the column of *Target* means that no timing constraints were set in this case. The runtime to insert the redundant contacts is about 2 second even for the largest example of ON2222_3 which consists of 56 transistors. The average absolute error of the target and actual delay value is less than 2%. Figure 6.28 plots the target and the simulated delay values in the case of NOR4_1 when the input signal to the P type transistor connected to VDD falls from logic level 1 to 0. The simulated delay values show good accordance with the target delay values. Figure 6.29 shows the trade-off curves of target delay and cell area versus number of the additional contacts in the case of NOR4_2. As the timing and area constraint become tight, the coverage of the redundant contact becomes small. These graphs show that the redundant contacts are correctly inserted under the given timing/area constraint.

Table 6.8 Results of the redundant contact insertion by the proposed method.

Circuit	*Target [psec]*	*Area [μm^2]*	*increase [%]*	*#Additional*	*Coverage [%]*
NAND3_1	36	5.12	38.38	3	42.9
	39	6.58	77.84	6	85.7
	No constraint	6.63	79.19	7	100
NAND3_2	36	8.34	27.72	4	40.0
	39	9.42	44.26	7	70.0
	No constraint	11.52	76.42	10	100
NAND4_3	55	24.27	9.57	5	25.0
	60	28.05	26.64	11	55.0
	No constraint	34.62	56.30	20	100
NOR4_1	78	6.33	32.98	4	44.4
	86	7.83	64.50	7	77.8
	No constraint	8.57	80.04	9	100
NOR4_2	71	23.38	34.29	13	46.4
	77	25.68	47.50	19	67.9
	No constraint	30.21	73.52	28	100
ON2222_3	71	35.66	24.03	24	38.7
	77	38.40	33.57	36	58.1
	No constraint	47.58	65.50	62	100
average	—	—	71.83*	—	—

* : An average of the no constraint cases

6.6.4 Gate Layout Pattern Regularity Enhancement

This section shows the experimental results of the proposed timing-aware gate layout pattern regularity enhancement method. In this experiment, we also used ILOG *CPLEX 9.1*[27] for an MILP solver, and 25 cell layouts from a standard-cell library of a 90nm technology were used as benchmarks. The regular pitch used in this experiment is defined as two times larger value than the minimum allowable spacing between gates without a contact between them. All the experiments were conducted on a Linux machine with Xeon 3.4GHz processor and 2GB of RAM.

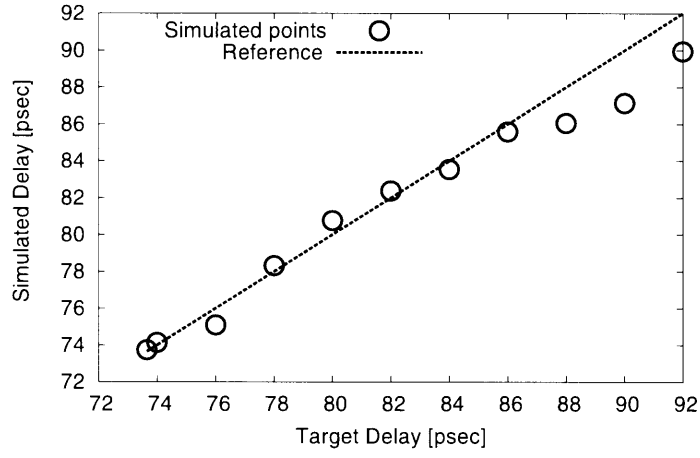
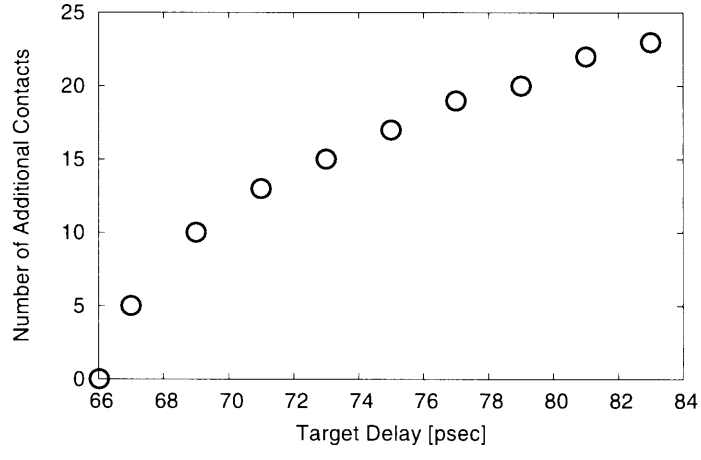
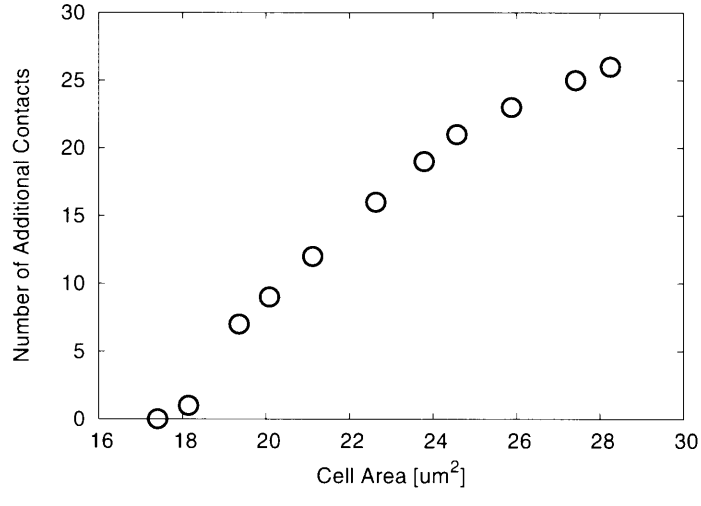


Figure 6.28 Accuracy of the proposed delay model in the case of NOR4_1.



(a) Target delay versus number of additional contacts



(b) Cell area versus number of additional contacts

Figure 6.29 Trade-off curves of target delay versus number of additional contacts in the case of NOR4_2.

Table 6.9 The delay accuracy, area increase, and runtime of the proposed regularity enhancement method with 10% allowable delay increase.

Cell Number	*Transistor Count*	*Delay Error [%]*	*Area Increase [%]*	*Runtime [sec]*
1	4	2.59(max.)	31.0	0.03
2	6	-0.01	26.5	0.03
3	6	0.73(max.)	23.4	0.03
4	6	1.41(max.)	31.3	0.03
5	7	0.45(max.)	22.6	0.04
6	8	0.92(max.)	25.1	0.05
7	8	-1.36	23.8	0.05
8	8	-3.26	44.3	0.02
9	8	-0.66	31.6	0.06
10	8	1.37(max.)	24.2	0.04
11	10	-3.00	38.4	0.05
12	10	2.27(max.)	31.3	0.08
13	10	0.24(max.)	25.6	0.07
14	12	0.02(max.)	31.9	0.05
15	12	-0.86	31.7	0.05
16	12	1.06(max.)	22.6	0.11
17	14	-1.53	46.8	0.08
18	16	-2.03	36.0	0.27
19	20	-0.71	48.3	0.30
20	20	-0.86	46.4	0.27
21	24	-2.81	48.3	0.64
22	28	0.59	36.5	14.62
23	32	-1.51	31.9	5.12
24	32	4.24(max.)	31.1	0.15
25	36	0.73	30.7	81.89
Average	—	1.42*	32.9	—

*: An average absolute error of non-maximum cases.

Table 6.10 The regularity cost reduction of the proposed regularity enhancement method with 10% allowable delay increase.

Cell Number	*Transistor Count*	*Regularity Cost before RE [A.U.]*	*Regularity Cost after RE [A.U.]*	*Reduction [%]*	*#Perfectly On-Pitch Gates*
1	4	650	100	84.6	3
2	6	810	140	82.7	4
3	6	850	250	70.6	3
4	6	810	100	87.7	5
5	7	830	100	88.0	6
6	8	980	400	59.1	4
7	8	1010	240	76.2	6
8	8	1010	0	100	8
9	8	1000	160	84.0	5
10	8	1050	440	58.1	4
11	10	1310	80	93.9	8
12	10	1340	280	79.1	8
13	10	1530	480	68.6	5
14	12	1520	480	68.4	7
15	12	1560	400	74.4	7
16	12	1320	480	63.6	8
17	14	1920	100	94.8	12
18	16	2160	440	79.6	9
19	20	2520	500	80.2	15
20	20	2510	300	88.0	16
21	24	3210	540	83.2	19
22	28	3580	960	73.2	23
23	32	3960	820	79.3	23
24	32	2020	0	100	32
25	36	4310	1230	71.5	23
Average	—	—	—	79.6	—

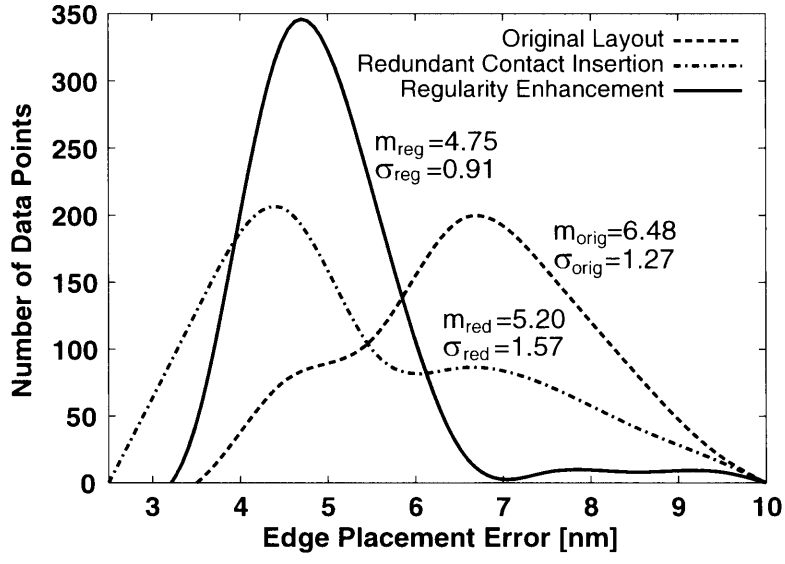


Figure 6.30 The gate CD EPE histogram of all the cells used in this experiment without OPC to highlight the effectiveness.

Tables 6.9 and 6.10 summarize the detailed experimental results of the proposed timing-aware regularity enhancement method when 10% delay increase is allowed during regularity enhancement (RE). These tables show the number of transistors, the delay error between the target and actual delay, the area increase, the runtime for each cell, the regularity cost before and after RE and its reduction ratio, and the number of gates placed perfectly on-pitch after RE. Delay error is calculated by $(t_{target} - t_{actual})/t_{target} \times 100$, where t_{target} and t_{actual} are the target and the actual delay, respectively. (max.) in the delay error column means that the maximum delay during regularity enhancement, which is equivalent to the delay of the regularity-enhanced cell with no timing constraint, is smaller than the target delay. Therefore, an average of absolute delay error is calculated without these cases. The average absolute error is about 1.4% and we can conclude that the delay increases are accurately constrained during regularity enhancement. The average regularity cost reduction of 79.6% is achieved by the proposed method. As a result, 73.7% gates in the regularity-enhanced layouts are placed perfectly on-pitch when 10% delay increase is allowed. Since the regular pitch used in this experiment is a little larger than the usual cases, this result is rather optimistic. However, this result clearly shows that the proposed method effectively enhances the regularity by de-compaction of the cell layout.

Figure 6.30 plots the gate CD Edge Placement Error (EPE) distribution before and after de-compaction for all of the cells used in this experiment with 10% allowable delay increase. This figure shows the EPE distributions of the original and the regularity-enhanced cell lay-

outs generated by the proposed regularity enhancement method. In addition, the EPE distribution of the cell layouts through timing-aware redundant contact insertion explained in the previous section is also plotted for comparison. Note that the redundant contact insertion is executed under the same timing constraints of the previous experiment without considering regularity constraint. Moreover, each generated cell has almost equal cell area to the corresponding regularity-enhanced cells. In this experiment, the print images used for calculating the EPE values are simulated using *Calibre*[37] through mask layout without OPC to highlight the effectiveness of the proposed method. The lithographic condition used in this experiment is summarized as follows.

- Lithography Wavelength: 193nm
- Numerical Aperture: 0.8
- Mask Reduction Factor: 4

As shown in this figure, the average value m of EPE decreases both through redundant contact insertion and regularity enhancement since the average pitch of the gate layouts increases. However, the standard deviation σ of EPE distribution is increased through redundant contact insertion due to the extra non-uniformity. On the other hand, the proposed regularity enhancement method effectively reduces the EPE distribution by introducing the gate layout pattern uniformity. The standard deviation σ of the EPE distribution is reduced by about 28% compared to that of the original layouts. This result shows that the proposed regularity enhancement method can reduce the systematic variation of the gate CD.

The timing accuracy of the proposed timing-aware regularity enhancement in the case of the largest example of 4-input NAND which has 36 transistors is shown in Figure 6.31. This figure plots the target and the simulated delay increase in the case that the input signal to the N type transistor connected to GND rises from logic level 0 to 1. The simulated delay values show good accordance with the target delay values. This result clearly shows the timing accuracy of the proposed timing-aware regularity enhancement method.

Figure 6.32 shows the trade-off curve of target delay versus regularity cost reduction ratio in the case of the same example. The proposed regularity enhancement method can pick up the regularity and performance variants of the original cell layout from this curve and these cells are prepared as a yield-enhanced library which is essential to realize yield-aware VLSI design flows.

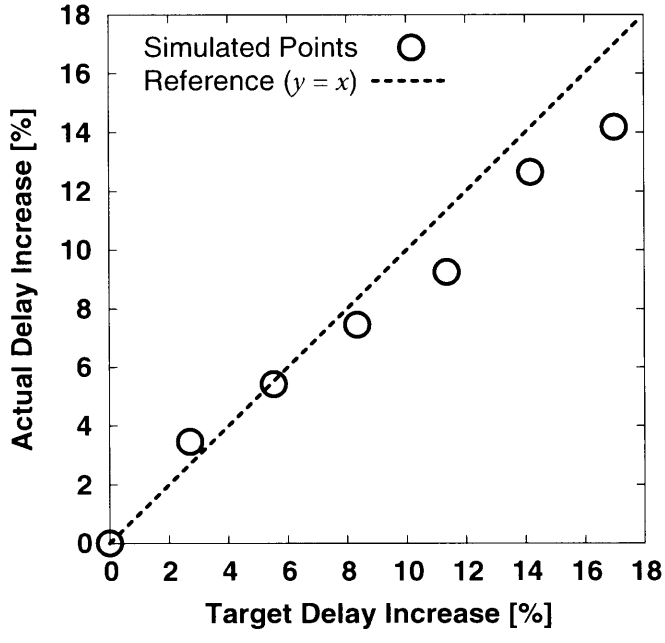


Figure 6.31 Accuracy of the cell delay constraint in the case of the largest example in Table 6.9.

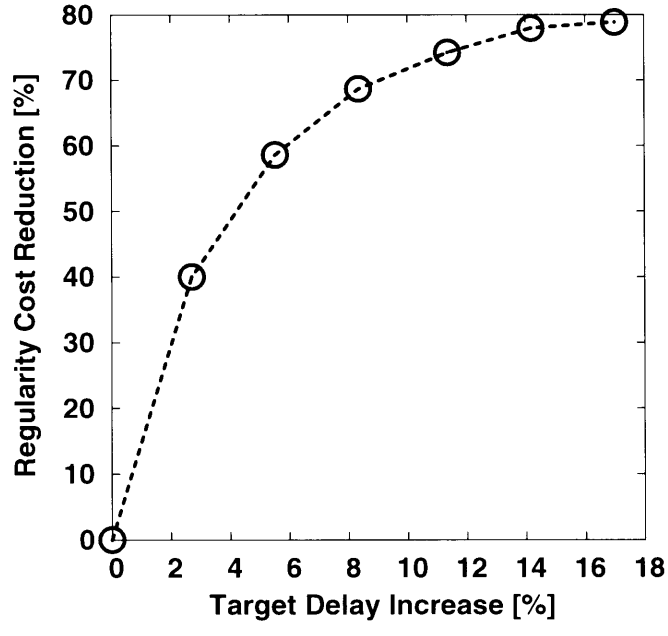


Figure 6.32 Trade-off curve between regularity enhancement and target cell delay in the case of the largest example in Table 6.9.

6.7 Summary

This chapter proposed a yield optimization method for standard cells by cell layout de-compaction under timing constraints. The proposed method performs a de-compaction of the original layout under given timing constraints using LP. We developed a new linear delay model which approximates the difference from the original cell delay and used this model to formulate the timing constraints as LP. Experimental results showed that the developed delay model is accurate enough to constrain the delay during de-compaction. The maximum CA reduction was about 25% on an average of 8 cells.

The proposed method was also shown to be effective for OPC mask data volume reduction. The proposed de-compaction method expands the spacings of the polygons inside the layout and eases the optical proximity effects under given timing constraints using LP. We use the fractured mask data size during mask creation to evaluate the OPC cost. Experimental results on a 90nm cell layouts showed that the proposed method reduces the fractured mask data size 4.28% on an average in the case that 10% delay increase is allowed. The effectiveness of the proposed method in the future technology was also demonstrated.

The redundant contact insertion was realized by the proposed timing-aware de-compaction framework. The proposed method inserts the redundant contacts as many as possible under given timing and area constraints using LP.

This chapter also showed the extension of the de-compaction method to a gate layout pattern regularity enhancement to reduce the systematic variation of the gate CD. With 10% allowable delay increase, 73.7% gates of 25 cells in a 90nm technology are placed perfectly on-pitch by the proposed method. Experiment on the EPE estimation showed that the standard deviation of the gate CD EPE distribution is reduced by about 28% compared to that of the original layouts and showed that the proposed regularity enhancement method is effective for reducing the systematic CD variation.

The proposed timing-aware yield enhancement method enables us to explore the trade-off between yield and performance. We can pick up the yield/performance variants from the trade-off curve and provide a yield-enhanced cell library. The proposed method is the essential technique to realize the yield-aware VLSI design methodologies.

Chapter 7

Conclusions

This thesis focused on the optimization methods for standard-cell layouts. We have proposed minimum-width transistor placement and intra-cell routing via Boolean satisfiability to optimize the area of the cell layouts, and also proposed a comprehensive cell layout synthesis method and a cell layout de-compaction method for yield optimization. The followings are conclusions through this thesis.

Chapter 2: We have proposed a minimum-width cell layout synthesis method for dual CMOS cells via Boolean Satisfiability. Cell layout synthesis problems *i.e.*, the transistor placement and the intra-cell routing problems are first transformed into SAT problems by our formulation. We have presented that the SAT formulation is more suitable for the transistor placement by comparing the runtime of the SAT and the 0-1 ILP formulations of it. We have also presented that the width of the placements generated by the proposed method are smaller than that of the conventional method by using our layout styles. Our method generates the cell layouts of 30 static dual CMOS logic circuits in 58% runtime with only 5% area increase compared with the commercial cell generation tool with cell layout compaction. These results showed that our cell layout styles defined for the SAT formulation is practical enough to generate the layout of dual CMOS cells quickly with a little area overhead.

Chapter 3: We have proposed a hierarchical layout synthesis method for large dual CMOS cells via Boolean Satisfiability. Experimental results showed that the proposed hierarchical transistor placement method generates the same width placement as the exact flat method proposed in Chapter 2 and drastically reduces the runtime. The comparison results of the cell layout synthesis for 30 benchmark circuits showed that the proposed method generates the same width layout as the flat method except one circuit. The comparison results with the commercial cell generation tool without cell layout compaction showed that the total cell width is increased about 4% by the proposed method due to the layout style restriction,

whereas the runtime is only about 3% of that of the commercial tool. From these results, we can conclude that the proposed method can be used as a quick layout generator in the area of transistor-level circuit optimization such as on-demand cell layout synthesis.

Chapter 4: We have proposed flat and hierarchical approaches for generating a minimum-width single-row transistor placement of CMOS cells in presence of non-dual P and N type transistors and generalized the single-row placement method to the multi-row placement method. Our approaches are the first exact minimum-width transistor placement method for non-dual CMOS cells. The experimental results showed that the flat single-row approach generates smaller width placement for 29 out of 103 dual cells than the transistor placement method for dual cells explained in Chapter 2 which theoretically generates the smallest width placement among the existing exact methods for dual cells. This result showed that the proposed method is not only applicable to CMOS cells with any types of structure, but also more effective even for dual CMOS cells compared with the transistor placement method only for dual cells. The hierarchical single-row approach which is based on circuit partitioning reduced the runtime drastically and generated 81% of 340 cells in an industrial standard-cell library of a 90nm technology within one hour for each cell, whereas the flat approach and the exact method only for dual cells generated 43% and 32%, respectively. The experimental results of the multi-row placement method showed that the proposed method generates more area-efficient placement than the conventional method only for dual cells by using the gate connection style which is more suitable for multi-row transistor placement than the conventional style and can solve the cells with up to 26 transistors in reasonable runtime.

Chapter 5: We have proposed an optimal cell layout synthesis technique to minimize the sensitivity to wiring faults. The sensitivity to wiring fault due to spot defects for intra-cell routings was modeled considering the spot defects size distribution and the end effect of critical areas, and used as a cost function. The impact of the sensitivity reduction on the yield improvement was also discussed in this chapter. Our cell layout synthesis technique generates the minimum width layouts of CMOS logic cells comprehensively, and selects the optimal layouts based on the cost functions. We applied our comprehensive layout synthesis method to 8 CMOS logic circuits which have up to 14 transistors and the results showed that the fault sensitivity is reduced about 15% on an average by selecting the minimum-sensitivity layouts rather than selecting the minimum-wire-length layouts. Our layout synthesis method is applicable for deriving the optimal cell layouts by some other cost metrics, such as power, delay, and signal integrity, if reasonable cost functions are given.

Chapter 6: We have proposed a timing-aware cell layout de-compaction method for yield optimization using Linear Programming (LP). The proposed method performs a de-compaction of the original layout in order to improve the yield by minimizing the Critical Area (CA) inside the cell. This yield improvement procedure is executed under given timing constraints. We developed a new linear delay model which approximates the difference from the original cell delay and used this model to formulate the timing constraints as LP. Experimental results showed that the developed delay model is accurate enough to constrain the delay during de-compaction. The CA is correctly minimized under the given timing constraint, and the maximum CA reduction was about 25% on an average of 8 cells. The proposed method was also shown to be effective for OPC mask data volume reduction. The proposed de-compaction method expands the spacings of the polygons inside the layout and relaxes the optical proximity effects under given timing constraints. Experimental results on a 90nm cell layouts showed that the proposed method reduces the fractured mask data size 4.28% on an average in the case that 10% delay increase is allowed. The redundant contact insertion was realized under the proposed timing-aware de-compaction framework. The proposed method inserts the redundant contacts as many as possible under given timing and area constraints using LP. This chapter also showed the extension of the de-compaction method to a gate layout pattern regularity enhancement to reduce the systematic variation of the gate critical dimension (CD). With 10% allowable delay increase, 73.7% gates of 25 cells in a 90nm technology are placed perfectly on-pitch by the proposed method. Experiment on the edge placement error (EPE) estimation showed that the standard deviation of the gate CD EPE distribution is reduced by about 28% compared with that of the original layouts and the proposed regularity enhancement method is effective for reducing the systematic CD variation. The proposed timing-aware yield enhancement method enables us to explore the trade-off between yield and performance. We can pick up the yield/performance variants from the trade-off curve and provide a yield-enhanced cell library. The proposed method is the essential technique to realize the yield-aware VLSI design methodologies.

Now we are sure that these results in this thesis such as the exact minimum-width cell layout synthesis techniques, the comprehensive cell layout synthesis method, and the cell layout de-compaction method for yield optimization will be used for standard-cell layout optimization in terms of area, delay, and yield, and contribute to the VLSI performance and reliability improvement.

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Journal Papers

1. T. Iizuka, M. Ikeda, and K. Asada, "High Speed Layout Synthesis for Minimum-Width CMOS Logic Cells via Boolean Satisfiability," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E87-A, no. 12, pp. 3293–3300, Dec. 2004.

2. T. Iizuka, M. Ikeda, and K. Asada, "Yield-Optimal Layout Synthesis of CMOS Logic Cells by Wiring Fault Minimization," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E88-A, no. 7, pp. 1957–1963, Jul. 2005.

3. T. Iizuka, M. Ikeda, and K. Asada, "Exact Minimum-Width Transistor Placement for Dual and Non-Dual CMOS Cells," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E88-A, no. 12, pp. 3485–3491, Dec. 2005.

4. T. Iizuka, M. Ikeda, and K. Asada, "Timing-Aware Cell Layout De-Compaction for Yield Optimization by Critical Area Minimization," *IEEE Transactions on Very Large Scale Integration Systems*. (*submitted*)

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1. T. Iizuka and K. Asada, "An Exact Algorithm for Practical Routing Problems," in *Proceedings of the Third IEEE Asia-Pacific Conference on ASICs*, pp. 343–346, Aug. 2002.

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5. T. Iizuka, M. Ikeda, and K. Asada, "Timing-Driven Cell Layout De-Compaction for Yield Optimization by Critical Area Minimization," in *Proceedings of IEEE/ACM Design, Automation and Test in Europe*, pp. 884–889, Mar. 2006.

6. T. Iizuka, M. Ikeda, and K. Asada, "Exact Minimum-Width Multi-Row Transistor Placement for Dual and Non-Dual CMOS Cells," in *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 5431–5434, May 2006.

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Domestic Conference Papers

1. T. Iizuka, M. Ikeda, and K. Asada, "An Exact Algorithm for Practical Routing Problems," in *Proceedings of IEICE Society Conference*, A-3-6, p. 61, Sep. 2002. (*in Japanese*)

2. T. Iizuka, M. Ikeda, and K. Asada, "Cell Layout Synthesis via Boolean Satisfiability," in *Proceedings of IPSJ DA Symposium*, pp. 139–144, Jul. 2003. (*in Japanese*)

3. T. Iizuka, M. Ikeda, and K. Asada, "Exact Wiring Fault Minimization via Comprehensive Layout Synthesis for CMOS Logic Cells," *IEICE Technical Report*, vol. 103, no. 476, pp. 157–161, Nov. 2003. (*in Japanese*)

4. T. Iizuka, M. Ikeda, and K. Asada, "Minimum-Width Transistor Placement Method via Boolean Constraints for Non-Complementary Transistors," in *Proceedings of IPSJ DA Symposium*, pp. 121–126, Jul. 2004. (*in Japanese*)

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Awards

1. *IEICE Young Researcher's Award*
   T. Iizuka, M. Ikeda, and K. Asada, "An Exact Algorithm for Practical Routing Problems," in *Proceedings of IEICE Society Conference*, A-3-6, p. 61, Sep. 2002. (*in Japanese*)

2. *Inose Science Award from Association for Promotion of Electrical, Electronic and Information Engineering*, Jul. 2003.

3. *Outstanding Paper Award from IPSJ SIGSLDM*
   T. Iizuka, M. Ikeda, and K. Asada, "Minimum-Width Transistor Placement Method via Boolean Constraints for Non-Complementary Transistors," in *Proceedings of IPSJ DA Symposium*, pp. 121–126, Jul. 2004. (*in Japanese*)

4. *Nikkei-BP LSI IP Design Award (Development Promotion)*
   T. Iizuka, M. Ikeda, and K. Asada, "Yield-Optimized CMOS Logic Cell Layout IP Synthesis System", May 2005. (*in Japanese*)

5. *IPSJ Yamashita SIG Research Award*
   T. Iizuka, M. Ikeda, and K. Asada, "Computational Cost Reduction for Minimum-Width Transistor Placement of Arbitrary Circuit Structures," in *Proceedings of IPSJ DA Symposium*, pp. 121–126, Aug. 2005. (*in Japanese*)

6. *Nikkei-BP LSI IP Design Award (IP Award)*
   T. Iizuka, M. Ikeda, and K. Asada, "Yield-Optimized Standard Cell Layout IP Synthesis System", May 2006. (*in Japanese*)

7. *Best Student Paper Award from IEEE International Conference on Electronics, Circuits and Systems*
   T. Iizuka, M. Ikeda, and K. Asada, "Timing-Driven Redundant Contact Insertion for Standard Cell Yield Enhancement," in *Proceedings of IEEE International Conference on Electronics, Circuits and Systems*, pp. 704–707, Dec. 2006.