Integrated Phased-Array Photonic Switches for Ultra-Large-Capacity Optical Packet Routing

超大容量光パケットルーティングのための集積化フェーズアレイ型光スイッチに関する研究

A dissertation submitted to the Graduate School of Engineering
The University of Tokyo
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

by

ソーアンジ　イブラーヒム　ムラット
Ibrahim Murat Soganci

under the supervision of
Professor Yoshiaki Nakano

June 2010

ACKNOWLEDGEMENT

This work could not have been done without the great support of many people. First and foremost, I would like to express my sincere appreciation to my advisor Professor Yoshiaki Nakano. My Ph.D. period has been fruitful thanks to his invaluable advices and the motivating, inspiring and friendly environment in the laboratory he is managing. I am very thankful for the responsibilities and freedom he has given me from the beginning of my studies.

I would also like to express my sincere gratitude to my co-advisor, Dr. Takuo Tanemura. All the work presented here has been carried out with his close supervision. I have learned so much from his technical advices that I feel fortunate that he has been my co-advisor. I am also very thankful to Professor Masakazu Sugiyama, from whom I have received many invaluable advices and learned a lot in our laboratory meetings.

I am also very grateful to Professor Hiroshi Toshiyoshi, Professor Shinji Yamashita, and Professor Zuyuan He for their invaluable comments, which helped me notice the weaknesses of my dissertation and improve it.

I would also like to express my sincere gratitude to Professor Harm Dorren, who was my advisor during my visits at Eindhoven University of Technology. His invaluable advices before, during and after my visits helped me improve my thesis and enhanced my knowledge especially on optical communication systems. He allowed me use the facilities at his institution freely with a great hospitality.

I am very thankful to many former and present members of Nakano/Sugiyama/Tanemura Laboratory, especially Koji Takeda, Salah Ibrahim, Akio Higo, Ling-Han Li, Koen Huybrechts, Masaru Zaitsu, Kentaroh Watanabe, Tomohiro Amemiya, Momoko Deura, Kazuhide Higuchi, Gengo Takahashi, Wen Yu, Shaojun Ma, Tomofumi Oyama, Yoshiyuki Kondo, Tatsuki Fujiwara, Masanori Kubota, Ryusuke Onitsuka, Myung-Joon Kwack, Xue-Liang Song, Foo Cheong Yit, Katsumasa

Horiguchi, Wang Yunpeng, Tomonari Shioda, Takuya Fujimura, Yuki Terada, Yuki Tomita, and Toshimasa Shimizu. Their friendly and inspiring support has made my life at the University of Tokyo enjoyable and fruitful. Please forgive me if I left anybody out by mistake. In addition to my colleagues, I am very thankful to the administrative assistants Ms. Ui, Ms. Tadokoro and Ms. Uchima for their daily support.

I am also very thankful to several people outside the University of Tokyo, especially Dr. Kevin Williams, Dr. Nicola Calabretta, Dr. Oded Raz, Wenrui Wang, Tjibbe de Vries, and Barry Smalbrugge at Eindhoven University of Technology. My optical packet switch experiments would not have been possible without their advices, ideas, and support.

I would like to give my sincere thanks to Ministry of Education, Culture, Sports, Science and Technology of Japan for my Ph.D. scholarship. This thesis would not exist without their financial support.

Last but not least, I am extremely thankful to my parents and my sisters. I have always known that they have been supporting me no matter how many thousands of kilometers there are in between.

ABSTRACT

The explosive growth of data capacity in communication networks has created new problems to be solved by the research community. The conventional optical-electrical-optical (OEO) networks are suffering from high power consumption. This problem is expected to be more serious in the future because the data capacity is estimated to continue increasing exponentially. Replacing the OEO configuration with transparent optical switching is promising to increase the energy efficiency by avoiding O/E and E/O conversion, (de)multiplexing and bit-by-bit processing. Optical packet switching (OPS) is particularly attractive because it offers the highest network utilization efficiency with bursty traffic.

OPS demands optical components with specifications beyond the state of the art, which makes it difficult to adapt this technology. The optical switch matrix has to reconfigure in time scales of a few nanoseconds or shorter. Moreover, the data capacity of the switching fabric in a core OPS node has to be scalable to ultra-high levels approaching or exceeding 1 Pb/s in the near future. The buffer also has to reach sufficient capacity in accordance with the throughput. Optical space switches can be building blocks of both switch matrices and tunable buffers. However, traditional integrated semiconductor switching technologies have difficulties in scaling to ultra-large capacities due to problems including signal quality degradation, footprint, and power consumption.

This dissertation focuses on a novel type of high-speed integrated photonic switch to extend the capacity limit of OPS. This device, referred as phased-array switch, has a number of unique properties. It can theoretically switch to hundreds of output ports in a single stage without cascading; it can switch multi-wavelength signals; and it is completely passive. After a detailed description of the principle of operation of this

switch and its design issues, experimental research on this device is presented. The first integrated 1×16 semiconductor photonic switch is among the switches introduced in this section. This device, which demonstrates wavelength dependence less than 0.7 dB in the entire C-band (1530-1565 nm), on-chip loss below 7 dB, average extinction ratio of 18.6 dB, and complete dynamic operation with a response time of 11 ns (limited by the controlling electronics), has improved the state of the art in integrated semiconductor photonic switching considerably. Another switch exhibits a polarization-dependent loss less than 2.2 dB mostly caused by the polarization dependence of the propagation loss. Moreover, an amplitude-controlled integrated phased-array switch is proposed and investigated theoretically for the first time. This device is capable of switching to an arbitrary combination of output ports simultaneously, i.e. multicasting.

Furthermore, experiments with an OPS node constructed from an all-optical label extractor, a phased-array switch, and an electronic switch controller are presented. There are several OPS demonstrations in the literature, but what makes these experiments special is the demonstration of modulation-format-agnostic routing compatible with wavelength-division multiplexing (WDM). In separate experiments, 160-Gb/s optical time-domain multiplexed (OTDM) on/off keying (OOK) and 120-Gb/s WDM differential phase-shift keying (DPSK) packets have been switched to 16 ports with power penalties below 0.7 dB. The OPS node has operated without manual control throughout the experiments. This OPS node can route packets with arbitrary modulation formats and bit rates as long as they fit in its ultra-broad bandwidth (1 dB bandwidth over 4.5 THz). Especially the modulation format independence is very important since spectrally efficient advanced modulation formats are likely to be used in the future.

An advanced photonic integrated circuit (PIC) consisting of hundreds of monolithic active and passive devices is also reported in this thesis. This fully integrated 1×100 switch consists of a two-stage phased-array switch cascaded with 100 semiconductor optical amplifier (SOA) gates, and fits in a footprint of 6 mm × 6.5 mm including the electrodes. The SOAs are employed in order to improve the extinction ratio. The active and passive devices have been integrated on a single substrate using the offset quantum well technique based on a layer of multiple quantum wells (MQW) above the core layer in active regions. As a result of the improved fabrication process

with two-step etching, the phase shifters in this PIC operate with a 2π current less than 1.5 mA. Despite the offset quantum well technique, which leads to a low confinement factor in the MQW layer, the SOA gates exhibit an extinction ratio over 40 dB with an injected current of 100 mA. The on-chip loss is less than 14.7 dB and the extinction ratio is larger than 50 dB among the outputs tested. A 10-Gb/s modulated signal has been transmitted through the switch with a power penalty less than 1 dB. PICs of this type are necessary for low-cost, compact and low-power optical switching; and this PIC is an example that demonstrates the potential of phased-array switching.

Finally, the estimated power consumption of ultra-large-capacity buffered optical packet switching fabrics is studied. Large-scale PICs comprising phased-array switches are assumed to be used for both routing and delay-line-based tunable buffering. The estimated energy per bit consumed by the buffer, switch matrix, switch controller and the semiconductor optical amplifiers to compensate for the optical loss in a hypothetical 1000×1000 router is less than 1.5 pJ/bit. The analysis is based on near-future device characteristics. A router of this scale has a maximum capacity of 1 Pb/s if the payload bit rate is 1 Tb/s per fiber. At this scale, phased-array switching is estimated to be 9.4 times as energy-efficient as broadcast-and-select switching, a common transparent switching scheme employed in OPS experiments.

To sum up, this thesis comprises experimental and theoretical research focusing on the application of phased-array switches in ultra-large-capacity OPS nodes. This study, which extends over the borders of device, circuit and subsystem level research, confirms that phased-array switches offer a serious potential for the future OPS networks if a number of technical challenges, mostly related to photonic integration, are overcome.

LIST OF RELATED PUBLICATIONS

Journal Papers

[1] I. M. Soganci, K. Takeda, T. Tanemura, M. Zaitsu, and Y. Nakano, “Design, fabrication and characterization of an InP photonic integrated circuit for 1×100 monolithic switching,” in preparation for submission to IEEE/OSA Journal of Lightwave Technology.

[2] I. M. Soganci, T. Tanemura, and Y. Nakano, “Power consumption in ultra-large-capacity buffered optical packet switch fabrics utilizing transparent photonic switches,” in preparation for submission to IEEE/OSA Journal of Lightwave Technology.

[3] (Invited) T. Tanemura, I. M. Soganci, T. Oyama, T. Ohyama, S. Mino, K. A. Williams, N. Calabretta, H. J. S. Dorren, and Y. Nakano, "Large-capacity high-resolution compact optical buffer based on InP phased-array switch and coiled fiber delay lines," submitted to IEEE/OSA Journal of Lightwave Technology.

[4] I. M. Soganci, N. Calabretta, T. Tanemura, W. Wang, O. Raz, K. Higuchi, K. A. Williams, T. J. de Vries, H. J. S. Dorren, and Y. Nakano, “160-Gb/s optical packet switching subsystem with a monolithic optical phased-array switch,” IEEE Photonics Technology Letters, vol. 22, no. 11, pp. 817-819, Jun. 2010.

[5] I. M. Soganci, T. Tanemura, K. A. Williams, N. Calabretta, T. de Vries, E. Smalbrugge, M. K. Smit, H. J. S Dorren, and Y. Nakano, “Monolithically integrated InP 1×16 optical switch with wavelength-insensitive operation,” IEEE Photonics Technology Letters, vol. 22, no. 3, pp. 143-145, Feb. 2010.

[6] I. M. Soganci, T. Tanemura, and Y. Nakano, “Integrated broadband 1×8 optical phased-array switch with low polarization sensitivity,” IEEE Photonics Journal, vol. 1, no. 2, pp. 80-87, Aug. 2009.

Refereed Conferences

[7] (Post-deadline paper) I. M. Soganci, T. Tanemura, K. Takeda, M. Zaitsu, M. Takenaka, and Y. Nakano, “Monolithic InP 100-port photonic switch,” in Proc. European Conference on Optical Communication (ECOC’10), Turin, Italy, 2010, Paper PD1.5.

[8] (Invited talk) Y. Nakano, T. Tanemura, and I. M. Soganci, “Monolithically integrated InP phased-array switch for optical packet switching and interconnection,” in Proc. Optical Fiber Communication Conference (OFC’10), San Diego, CA, 2010, Paper OMP4.

[9] (Invited talk) I. M. Soganci, T. Tanemura, and Y. Nakano, “Broadband monolithic photonic phased-array switches for high-throughput optical routing,” in Proc. IEICE General Conference, Sendai, Japan, Mar. 16-19, 2010, Paper C-4-7.

[10] (Post-deadline paper) T. Tanemura, I. M. Soganci, T. Oyama, T. Ohyama, S. Mino, K. A. Williams, N. Calabretta, H. J. S. Dorren, and Y. Nakano, “Optical buffer based on monolithic InP phased-array 1×16 switch with silica-PLC pitch converter and ultra-compact coiled fiber delay lines,” in Proc. Optical Fiber Communication Conference (OFC’10), San Diego, CA, 2010, Paper PDPA5.

[11] (Invited talk) T. Tanemura, I. M. Soganci, T. Oyama, and Y. Nakano, " Semiconductor photonic integrated switches and buffers for optical packet routing," 9th International Conference on Optical Internet (COIN’10), Jeju, Korea, July 11-14, 2010.

[12] (Invited talk) T. Tanemura, I. M. Soganci, and Y. Nakano, "Large-scale high-speed photonic switching circuit monolithically integrated on InP," 15th OptoElectronics and Communications Conference (OECC’10), Sapporo, Japan, July 5-9, 2010.

[13] T. Oyama, T. Tanemura, I. M. Soganci, T. Ohyama, S. Mino, and Y. Nakano, “Variable optical buffer using integrated 1×8 optical phased-array switch,” Conference on Photonics in Switching (PS’10), Monterey, CA, 2010, Paper PTuC5.

[14] N. Calabretta, I. M. Soganci, T. Tanemura, W. Wang, O. Raz, K. Higuchi, K. A. Williams, T. J. de Vries, Y. Nakano, and H. J. S. Dorren, “1×16 optical packet switch sub-system with a monolithically integrated InP optical switch,” in Proc. Optical Fiber Communication Conference (OFC’10), San Diego, CA, 2010, Paper OTuN6.

[15] I. M. Soganci, T. Tanemura, K. A. Williams, N. Calabretta, T. De Vries, E. Smalbrugge, M.

K. Smit, H. J. S. Dorren, and Y. Nakano, “High-speed 1×16 optical switch monolithically integrated on InP,” in Proc. European Conference on Optical Communication (ECOC’09), Vienna, Austria, 2009, Paper 1.2.1.

[16] I. M. Soganci, T. Tanemura, K. A. Williams, N. Calabretta, T. De Vries, E. Smalbrugge, M. K. Smit, H. J. S. Dorren, and Y. Nakano, “Integrated phased-array 1×16 photonic switch for WDM optical packet switching application,” in Proc. International Conference on Photonics in Switching (PS’10), Pisa, Italy, 2009, Paper WeI3-2.

[17] I. M. Soganci, T. Tanemura, and Y. Nakano, “Polarization-independent broadband 1×8 optical phased-array switch monolithically integrated on InP,” in Proc. Optical Fiber Communication Conference (OFC’09), San Diego, CA, 2009, Paper OWV1.

[18] I. M. Soganci, T. Tanemura and Y. Nakano, “High-speed 1×16 optical phased-array switch monolithically integrated on InP,” presented at The Japan Society of Applied Physics Autumn Meeting, Toyama, Japan, Sep. 8-11, 2009.

[19] N. Calabretta, I. M. Soganci, T. Tanemura, W. Wang, O. Raz, K. Higuchi, K. A. Williams, T. J. de Vries, Y. Nakano, and H. J. S. Dorren, “Optical packet switch sub-system with label processing and monolithically integrated InP optical switch,” in Proc. 2010 IEEE/LEOS Winter Topical Meetings, Majorca, Spain, 2010, Paper TuC3.4.

[20] T. Oyama, T. Tanemura, I. M. Soganci, T. Ohyama, S. Mino, and Y. Nakano, “Variable optical buffer using integrated 1×8 optical phased-array switch,” in Proc. IEICE General Conference, Sendai, Japan, Mar. 16-19, 2010, Paper B-12-15.

[21] (Invited talk) T. Tanemura, I. M. Soganci, K. Takeda, and Y. Nakano, "Research progress on phased-array semiconductor optical packet switches," IEICE Techn. Rep., vol. 108, no. 476, PN2008-87, pp. 19-22, Mar. 2009.

[22] I. M. Soganci, T. Tanemura, and Y. Nakano, “Integrated broadband 1×8 optical phased-array switch with low polarization sensitivity and nanoseconds reconfiguration time,” IEICE Tech. Rep., vol. 108, no. 417, PN2008-53, pp. 59-63, Jan. 2009.

[23] T. Tanemura, I. M. Soganci, K. Takeda, and Y. Nakano, “InP integrated optical phased-array 1×N switch for optical packet switching,” in Proc. IEICE Society Conference, Kawasaki, Japan, 2008, pp. C-53-54.

Workshops

[24] I. M. Soganci, T. Tanemura, and Y. Nakano, “Integrated broadband scalable 1×N optical phased-array switches for WDM optical packet networks,” presented at International Workshop on Advancement of Optical Signal Processing and Related Devices, Vienna, Austria, Sep. 25, 2009.

[25] I. M. Soganci, T. Tanemura, and Y. Nakano, “Design and fabrication of a compact InP/InGaAsP optical phased-array switch,” in Proc. International Nano-Optoelectronic Workshop, Tokyo, Japan, 2008, pp. 149-150.

CONTENTS

Acknowledgement……i
Abstract……iii
List of Related Publications……..…vii

CHAPTER 1 INTRODUCTION 1
1.1 Optical Switching Networks: Motivation and Basics 1
1.1.1 Exponentially Increasing Data Traffic 1
1.1.2 Scaling Optical-Electrical-Optical (OEO) Networks 1
1.1.3 All-Optical Networks 3
1.2 Integrated Photonics 10
1.2.1 Motivation and Challenges 10
1.2.2 Basics of Photonic Integrated Devices and Circuits 11
1.3 Integrated Photonic Switches 13
1.3.1 Important Characteristics of Optical Switches 13
1.3.2 Present State of Integrated Photonic Switches 17
1.4 Contribution and Organization of the Dissertation 18
1.4.1 Contribution of the Dissertation 18
1.4.2 Organization of the Dissertation 20
References of Chapter 1 21

CHAPTER 2 INTEGRATED PHASED-ARRAY PHOTONIC SWITCHING 27
2.1 Introduction 27
2.2 Basics and Brief Overview of Optical Phased Arrays 28
2.3 Integrated Phased-Array Photonic Switches 30
2.4 Analytical Explanation of Phased-Array Switching 31
2.5 Design Considerations of Phased-Array Switches 36
2.6 Comparison with Other Switch Technologies 40
2.7 Amplitude-Controlled Phased-Array Switches for Multicasting 44

2.8 Conclusion 47
References of Chapter 2 50

CHAPTER 3 INTEGRATED *1*×*N* PHASED-ARRAY PHOTONIC SWITCHES: DESIGN, FABRICATION AND CHARACTERIZATION 53
3.1 Introduction 53
3.2 Integrated 1×8 Photonic Switch with Low Polarization Sensitivity 54
3.2.1 Design of the Device 54
3.2.2 Fabrication of the Device 60
3.2.3 Characterization of the Device 63
3.2.4 Discussion 74
3.3 Wavelength-Insensitive Low-Loss Monolithic 1×16 Photonic Switch 75
3.3.1 Design and Fabrication of the Device 76
3.3.2 Characterization of the Device 77
3.3.3 Discussion 86
3.4 Conclusion 87
APPENDIX Measurement of Propagation Loss Using Fabry-Perot Resonance 89
References of Chapter 3 92

CHAPTER 4 HIGH-BIT-RATE OPTICAL PACKET SWITCHING EXPERIMENTS 95
4.1 Introduction 95
4.2 Labeling Scheme and Payload 96
4.3 OPS Node Subsystem 98
4.4 Experimental Setup and Results 101
4.5 Conclusion 105
References of Chapter 4 107

CHAPTER 5 PHOTONIC INTEGRATED CIRCUIT FOR 100-PORT MONOLITHIC SWITCHING 109
5.1 Introduction 109
5.2 Design of the PIC 110
5.2.1 Design of General Architecture 110
5.2.2 Active/Passive Integration 111
5.2.3 Design of Epitaxial Structure 113

5.2.4 Design of Phased-Array Switches 117
5.2.5 Design of PIC Layout 119
5.3 Fabrication of the PIC 124
5.4 Characterization of the PIC 126
5.5 Conclusion 133
References of Chapter 5 134

CHAPTER 6 POWER CONSUMPTION IN BUFFERED OPTICAL PACKET SWITCH FABRICS UTILIZING PHASED-ARRAY SWITCHES 137
6.1 Introduction 137
6.2 Architectures of Optical Switch and Buffer Analyzed 139
6.2.1 $N \times N$ Matrix Switch 139
6.2.2 Tunable Optical Buffer 141
6.2.3 Switch Controller 142
6.3 Calculation of Estimated Power Consumption 143
6.3.1 Power Consumption of a $1 \times N$ Switching Chip 143
6.3.2 Power Consumption of Complete $N \times N$ Optical Packet Switch with Buffers 151
6.4 Discussion and Conclusion 153
References of Chapter 6 155

CHAPTER 7 CONCLUSION 159

CHAPTER 1
INTRODUCTION

1.1 OPTICAL SWITCHING NETWORKS: MOTIVATION AND BASICS

1.1.1 Exponentially Increasing Data Traffic

The information age has made significant influence on the society in a very short time after the emergence of Internet in 1990s. Among many social, economic and technological effects of this sudden change is the explosion of data traffic. The annual internet traffic growth rate in North America was estimated to be approximately 100% in the early years [1]. Although this initial growth reduced after 2000, a steady annual expansion rate in the range of 50-60% has been reported until the end of 2008 [2]. As displayed in Fig. 1.1, the data traffic surpassed voice traffic in 2002; and the total traffic trend has been dominated by data since then. Similar trends have been observed in Japan and Europe. The global IP (Internet protocol) traffic, which is dominated by Internet, is expected to increase with an annual rate of 40% at least until 2013 [3].

1.1.2 Scaling Optical-Electrical-Optical (OEO) Networks

The increasing data traffic necessitates capacity upgrades because the systems that are already deployed are becoming full [1]. The OEO networks, which are being used at the moment, utilize optical fibers to transmit the data and electronic routers to reconfigure the connections. The most straightforward solution of this problem is scaling up the link

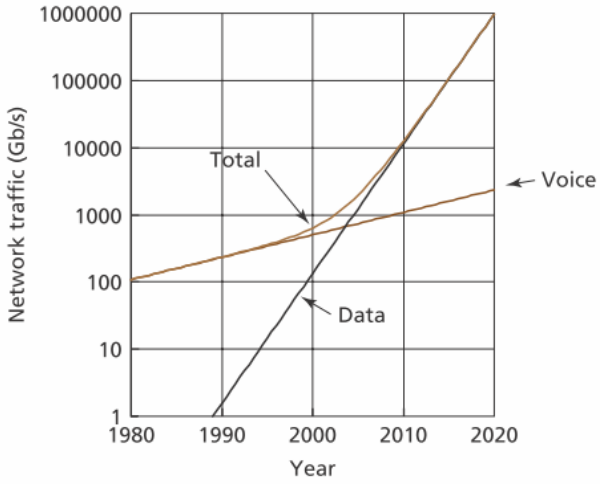


Fig. 1.1 North American network traffic including voice and data (after [2]).

capacity by increasing the bit rate per fiber and/or the number of fibers and scaling up the electronic circuits and optoelectronic components in the switching nodes, transmitters and receivers. This approach, which has been followed so far, is facing fundamental limitations set by especially the power consumption and size.

Optical technologies are not the limiting factor against capacity scaling. After the invention of erbium-doped fiber amplifier (EDFA) [4], which operates in the 1530-1565 nm band (C-band or erbium window), it became possible to transport wavelength-division multiplexed (WDM) ultra-broadband signals to long distances [5]. The recently reported 69.1 Tb/s transmission over 240 km is an example of the bandwidth potential of optical fibers [6]. The bit rates used in present communication networks are far from these experimental values, so the fiber capacity is still not fully utilized.

Electronic routers suffer from power consumption as the data capacity increases. The state-of-the-art electronic router, Cisco CRS-3, which has a maximum single-chassis capacity of 4.48 Tb/s, consumes approximately 12.3 kW of power [7]. A 100-Tb/s router with similar technologies is expected to consume 275 kW of power and occupy a large space of multiple racks. Power and size scale linearly with the throughput because of the bit-by-bit switching scheme in conventional electronic routers. As illustrated in the simple schematic diagram in Fig. 1.2, the data arriving at

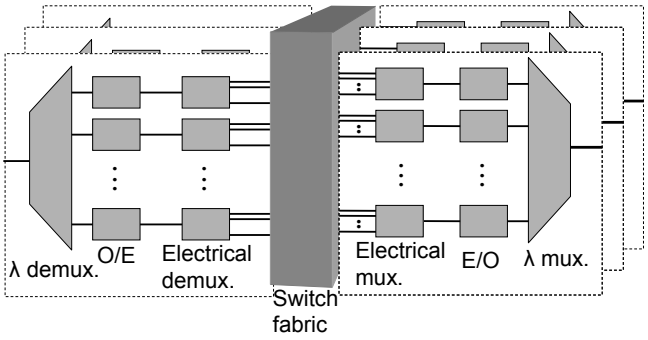


Fig. 1.2 A very simplified schematic diagram of basic functional blocks in an O/E/O router. Several functions are not shown for simplicity.

the node is wavelength demultiplexed, converted to electrical domain, demultiplexed to the bit rates that can be processed by the electronic circuits and switched by the electrical cross-connect. Electrical multiplexing, electrical/optical conversion and optical multiplexing are necessary before sending the data to the requested port. Especially OEO conversion and multiplexing/demultiplexing are power-hungry processes and they have to be implemented for all wavelength channels separately at every switching node. The power consumed for demultiplexing, multiplexing and clock recovery alone has been estimated to be 100 kW in a 40-Tb/s OEO node [8]. The other electronic processing operations also dissipate power linearly increasing with the bit rate, increasing up to unacceptable levels with high capacity. Another serious problem of electronic switching is the necessity of hardware replacement in case of bit rate or modulation format update. All these problems have led researchers to look for different technologies to route high-bit-rate signals.

1.1.3 All-Optical Networks[1]

The problems caused by the electronic routing bottleneck can be avoided by keeping the data in the optical domain until the final destination. A brief history of all-optical networks is given next.

[1] Throughout this thesis, the term "all-optical network" refers to networks without OEO conversion in the data plane. Therefore, these networks are not necessarily all-optical in the control plane.

1.1.3.1 First- and Second-Generation Optical Networks

Optical point-to-point links, which were first deployed in the early 1980s, can be regarded as the first-generation all-optical networks [9]. With the increasing size of communication networks, more complicated schemes became necessary. Wavelength-routing optical circuit switching networks, which have the granularity of a wavelength channel, have been the second-generation of all-optical networks [10]. These so-called optical transport networks (OTN) deployed optical add-drop multiplexers (OADM) and optical cross connects (OXC) [11]. OADMs are optical devices that configure the distribution of wavelength channels in WDM networks [12]. Due to the demand for reconfigurability, these devices were later modified to reconfigurable optical add-drop multiplexers (ROADM) [13], which included limited circuit switching to update the channel distribution according to the traffic conditions. OXCs are optical circuit switching devices used for restoration of the network, reconfiguration to adapt the changes and protection switching [14]. These coarse-granularity optical components added transparency and helped simplify the hardware in the data plane [11]. These networks are not strictly “all optical” because ROADMs and OXCs have limited capabilities, and have to be used together with electronic switching components.

1.1.3.2 Third-Generation Optical Networks

Circuit switching is not suitable for dynamic networks with bursty traffic because of the insufficient granularity, which reduces the network utilization efficiency dramatically [15]. As a solution, the third-generation all-optical networks technologies, namely optical burst switching (OBS) and optical packet switching (OPS), have been proposed. OPS technology is based on the switching of individual data packets in the optical domain. Unlike circuit switching, paths are not fixed, but they are formed between nodes according to the conditions of the networks as shown in Fig. 1.3. OBS has different implementations, but in general it is between OCS and OPS in terms of granularity, network efficiency and technological difficulty. The schematic architecture in Fig. 1.3 is valid for OBS, too.

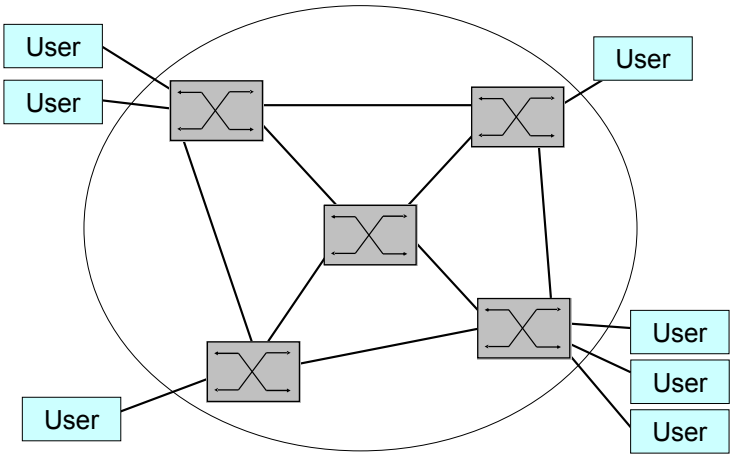


Fig. 1.3 Third-generation optical network architecture.

OBS has been implemented as fast circuit switching with special signaling such as tell-and-go (TAG), or packet switching with large aggregated packets of different sizes and formats [11]. The bursts are assembled at the edge routers (ingress). Later, an idle channel is found on the path to send the bursts. Different one- or two-way signaling protocols are used to reserve the channel for the burst. Depending on whether an OCS-like or an OPS-like scheme is adapted, built-in buffers may or may not be used at OBS nodes. The basic advantages of OBS over OPS are the possibility of avoiding optical buffering and the less stringent constraints on the switching speed. Although it varies depending on the application, switching speeds in the range of microseconds are typically sufficient for OBS. In spite of these advantages, it is not clear whether OBS is going to be commercially successful because of the relatively low network utilization efficiency, which has to be compensated for by constructing networks with excessive capacities [16].

OPS is the ultimate goal of researchers because of its good match with the contemporary bursty Internet traffic. Owing to its low latency, OPS is considered as promising not only for optical communications but also for high-performance computing systems [17]. However, it is the most demanding scheme in terms of the optical technologies used. A typical OPS node consists of three main parts, namely the input interface, switch fabric and the output interface as illustrated in Fig. 1.4 [18]. Input interface is the section separating the header from the payload and organizing the

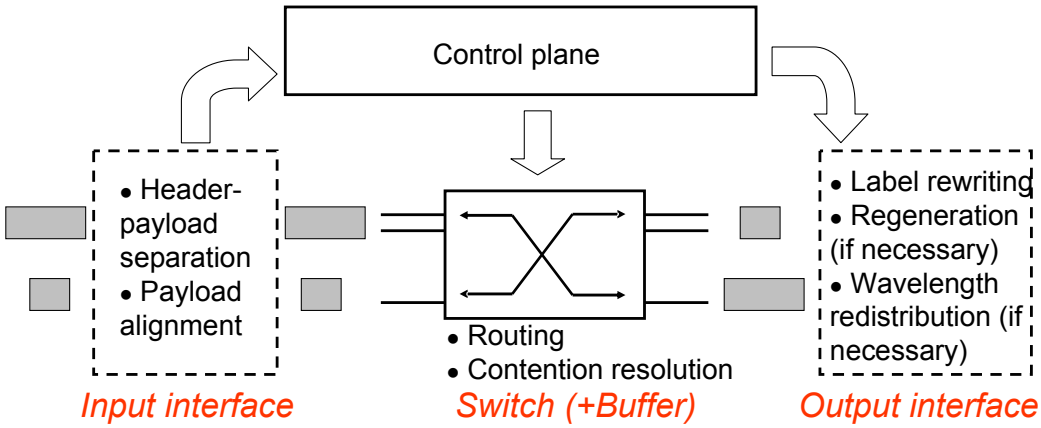


Fig. 1.4 Schematic of a generic OPS core node.

timing of incoming packets according to the latency of the controller, and the necessity of synchronization. The label separated at the input interface supplies the controller with the necessary information for routing of the packet properly. Payloads continue propagating in the data plane into the switch fabric. The duty of the switch fabric is to form the desired input/output connection while avoiding packet collision through contention resolution. The switch fabric is controlled by the switch controller in the control plane. After being routed, packets move to the output interface, which rewrites the headers for proper routing in the next port and does wavelength conversion if necessary. Moreover, regeneration is done at this stage if the signal quality is not sufficient.

The control plane of OPS routers can be either electronic or optical, but the data plane has to be all-optical to make use of the advantages of OPS. The most critical optical functions in the data plane are contention resolution and switching. As displayed in Fig. 1.5, switch fabrics are usually equipped with buffers to store contending packets. These buffers should have sufficient capacities to avoid packet loss. Unlike electronics, photonic memories are very immature, so delay lines are the only practical solution for optical buffering. In addition to contention resolution problem, high-speed switching with a sufficient capacity is a remaining challenge. The switch has to have a reconfiguration time in the range of a few nanoseconds or sub-nanosecond for OPS routing. Furthermore, it should be capable of reaching very high data capacity levels

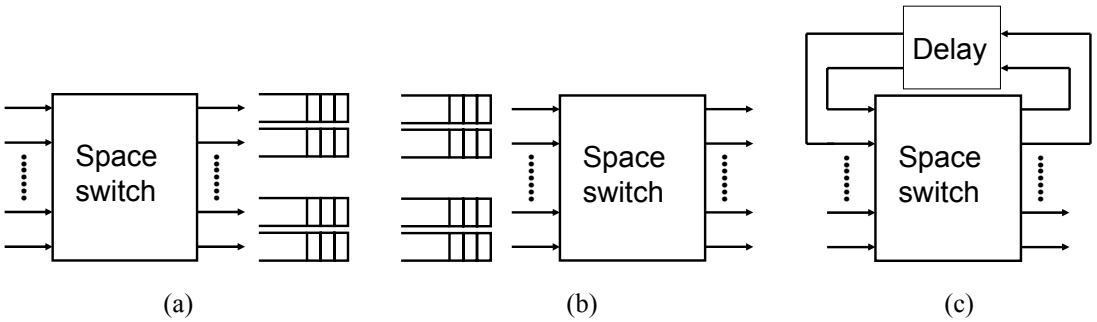


Fig. 1.5 (a) Output buffered, (b) input buffered, and (c) shared buffered optical packet switches.

with significant power, size and cost advantages compared to electronic switches.

1.1.3.3 Present State of Optical Packet Switching and Remaining Issues

Despite the technical difficulties, successful proof-of-concept demonstrations of different OPS functions have been reported by several research groups. The purpose of this section is not to give a review of these works, but is to understand the state of the art and the remaining issues to be solved. This is necessary to clarify the contribution of this dissertation.

High data rate capacity is a requirement to be satisfied for OPS to be considered as an option. The highest bit rate per port reported so far is 640 Gb/s (64 × 10 Gb/s) [19]. All-optical label processing, switching and buffering of differential phase-shift keying (DPSK) packets were achieved in this work. This is an important demonstration to show the potential of strictly transparent switches compatible with high-bit-rate WDM packets with advanced modulation formats. However, this is a simplified 2×2 switching experiment with a buffer depth of only two packets. The authors mention the difficulty of scaling the port count because of the high insertion loss of PLZT switches when cascaded, and add that scalable switches with low insertion loss, high extinction ratio and response time on the order of nanoseconds are demanded [19].

The OSMOSIS (Optical Shared Memory Supercomputer Interconnect System) project is a good example to show the technological problems to be solved for OPS to be commercializable. A 64×128 optical switch was built from discrete broadcast-and-select semiconductor optical amplifier (SOA) gate switches utilizing

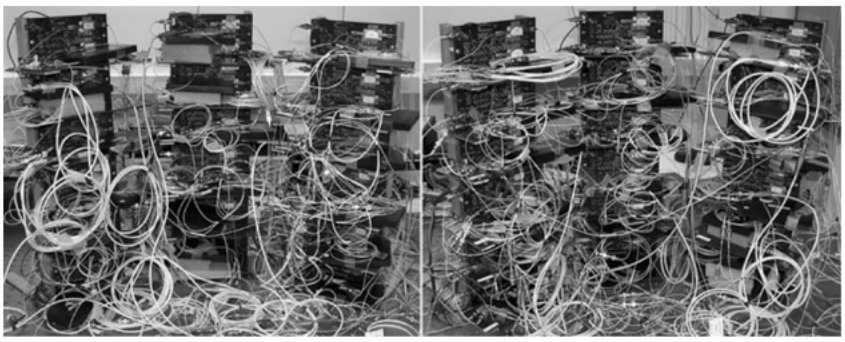


Fig. 1.6 Photographs of a 12-port OPS network without large-scale photonic integration (after [22]).

eight-channel WDM [20,21]. Strict design specifications including low latency, which is especially important for high-performance computers, were achieved in this project. However, cost advantage was not met compared to electronic switching because of the discrete optical components in the fabric. This project both experimentally verifies the technical possibility of OPS and reveals the necessity of photonic integration. It is clear that large-scale switches cannot be fabricated cost effectively out of discrete devices, so photonic integration is a more practical solution for OPS. As displayed in Fig. 1.6, even small-scale OPS networks become physically complicated if large-scale integration is not used [22].

To reach the throughput levels approaching 1 Pb/s, which is expected to be in use in the next ten years, either extremely large number of switching ports or high bit rates achieved by techniques such as WDM, optical time-division multiplexing (OTDM) or advanced modulation formats are necessary. For example, under the assumption that a single fiber has a bit rate of 1 Tb/s, switches comprising 1,000 input and output ports are required to reach a throughput of 1 Pb/s. The same throughput level can be achieved with 25,000 ports in case low-bit-rate (40 Gb/s) switching is preferred. Even the largest-scale integrated optical switches employed in OPS experiments in the literature have numbers of ports far less than thousands [23-25], so high-bit-rate OPS is crucial to reach ultra-high throughput. As explained in Section 1.2.3, common optical switch technologies used in OPS experiments lack scalability either in terms of port count or bit rate. Therefore, a novel type of transparent switch with broad bandwidth and port count scalability is highly desirable for OPS.

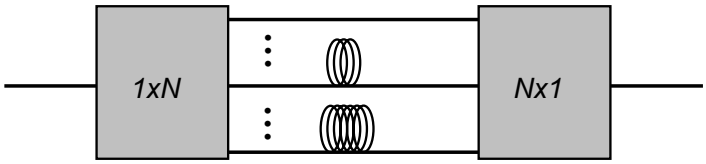


Fig. 1.7 Tunable optical buffer utilizing fiber delay lines and optical switches.

The other critical building block of an OPS router is the buffer. Electronic router buffers conventionally have very large capacities on the order of 250 ms × bit rate per port [26]. This is equivalent to a buffer of 250 Gbits for a line rate of 1 Tb/s. There are not any practical solutions of implementing optical buffering with this size. Research-level photonic memory elements are inferior to their electronic counterparts in terms of almost all aspects, including footprint, energy consumption, and cascadability [27,28]. On the other hand, tunable delay lines with these capacities have to be thousands of kilometers in length, which is obviously impractical. However, recently it has been claimed that buffer sizes used in electronic routers are too large and if the burstiness of the core network is mitigated, buffer sizes of only 10-20 packets per port are sufficient for contention resolution in a router with 80% load [29,30]. Tunable buffers with a depth of 10-20 packets can be constructed from delay lines and 1×N optical switches as in Fig. 1.7. For tunable buffering application, the delay lines are desired to be compact and low-loss, whereas the switches are desired to have high extinction ratio and low insertion loss.

The feasibility of OPS has been under discussion in the research community because of the problems explained above and other problems out of the scope of this dissertation, such as difficulty of fault management in transparent networks [31]. Novel integrated high-speed optical switches with scalable port counts, low loss, strict transparency, and wavelength and polarization independence are critical devices that can bring OPS one step closer to reality. The cost-effective implementation of these devices can be possible through photonic integration, which is explained in the next section.

1.2 INTEGRATED PHOTONICS

1.2.1 Motivation and Challenges

Analogous to electronic integration, photonic integration is the technology of packing multiple photonic devices on a single platform. The idea of photonic integration was first proposed in 1969 [32]. Since then, researchers have worked on generation, amplification, modulation, switching, transportation and detection of light in an integrated fashion. The main application of integrated photonics has been optical communications so far. The first and second-generation optical networks, explained in the previous section, have employed transmitters, receivers and networking devices such as ROADMs and OXCs, which consist of several optical components especially in high-capacity networks. As a result, optical communication has been suitable for photonic integration.

The major advantages of integrated photonics compared to discrete optical components are reduced packaging cost, reduced fiber coupling loss, reduced power consumption, small size, stability, and reproducibility. In spite of these advantages and the quite long history of the idea, the level of progress in photonic integration has been

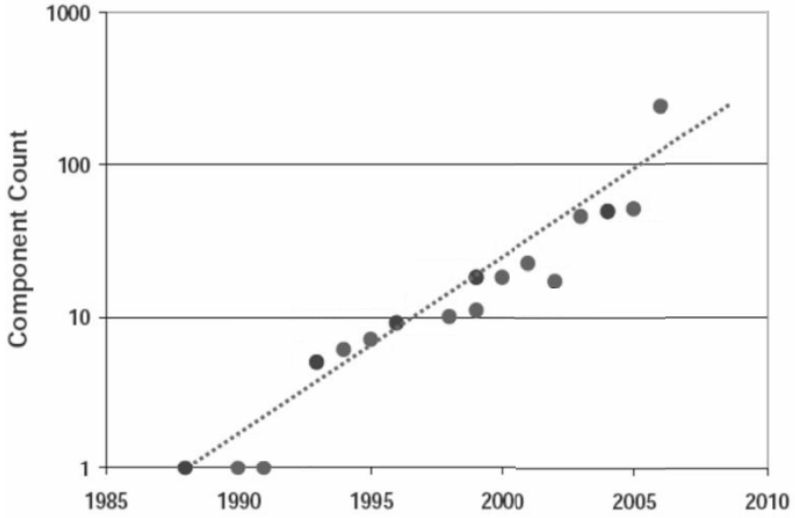


Fig. 1.8 Progress of component count in photonic integrated circuits (after [34], edited for clarity).

much slower than electronic integration, which has been following the well-known Moore's Law [33]. Even the state-of-the-art photonic integrated circuits (PIC) are limited to a few hundred devices on a chip (Fig. 1.8) [34].

There are three major obstacles against the scaling of PICs. First of all, different optical functions have considerably different optimal device structures, so it is challenging to integrate them without trading off device performance. The second problem is the size of photonic devices. Because of the diffraction limit, light in conventional guided-wave devices cannot be squeezed into dimensions smaller than one fourth of the wavelength. Considering that the communication band around 1550 nm is mostly used due to low fiber loss in that band, the fundamental limit to the size of photonic devices is much larger than the state-of-the-art electronic devices. Although plasmonic waveguides have been investigated to go beyond the diffraction limit [35], the high propagation loss is a challenging problem [36]. The third obstacle is the weak demand of large-scale PICs by optical communication industry. The data traffic in communication networks was very small until the advent of Internet in late nineties. Therefore, the market size was not sufficient to justify the expensive investment on this technology. Nevertheless, the explosion of communication data capacity after the advent of Internet has changed this situation. The stagnation of photonic integration before late nineties and the rapid improvement since then is clearly visible if we compare the largest-scale PICs until 1996 with the present PICs [37,38].

1.2.2 Basics of Photonic Integrated Devices and Circuits

Devices on PICs are usually arranged in a planar manner and are connected to each other via optical waveguides. PICs are sometimes referred as planar lightwave circuits (PLC). PICs have been fabricated with a variety of material systems, including silica on silicon [39,40], lithium niobate [41,42], silicon on insulator (SOI) [43,44], and III-V compound semiconductors [45,46]. Among them, compound semiconductors, especially InP is the material of choice for the largest-scale PICs because they have the richest variety of monolithic optical functionalities with a relatively large degree of freedom compared to the other materials. SOI has recently gained popularity because of

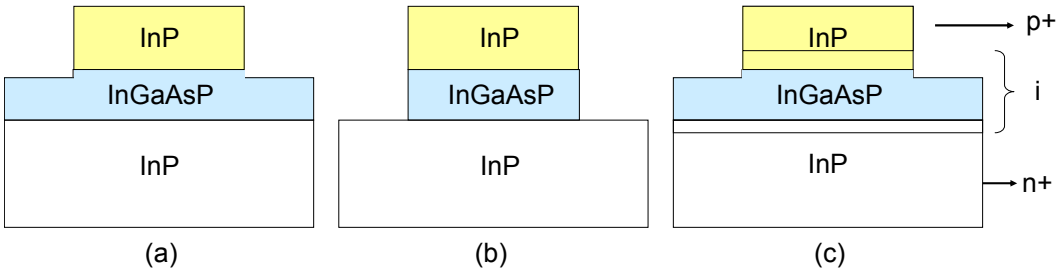


Fig. 1.9 Schematic cross-sections of (a) InP/InGaAsP shallowly-etched passive ridge waveguide (b) deeply-etched waveguide, and (c) pin optoelectronic waveguide.

the possible compatibility of the material system with CMOS and the tight vertical confinement leading to very compact devices. However, the biggest disadvantage of SOI is the lack of active devices because of the indirect bandgap of silicon. In addition to monolithic approaches, hybrid integration has been investigated to make use of the advantages of different materials. III-V bonded on SOI is an attractive hybrid integration solution to implement active functions such as lasing and detecting on silicon [47,48].

Independent from the material system, devices in PICs have a waveguide structure with a high-refractive-index core surrounded by lower-index claddings to guide light beams. Introductory information on integrated optics and waveguide theory are available in textbooks [49,50]. In guided-wave semiconductor devices, horizontal confinement is usually realized by etching and vertical confinement is realized by stacking layers with different refractive indices. In compound semiconductors, this is implemented by epitaxially growing lattice-matched alloys that have different composition parameters. The refractive index and bandgap of these alloys depend on the material composition, which gives the designers some degree of freedom. For example, the bandgap of the quaternary alloy, $In_{1-x}Ga_xAs_yP_{1-y}$, can be tuned between 1.35 eV (photon wavelength of 920 nm) and 0.75 eV (1650 nm) by changing x and y while still maintaining it lattice-matched to InP [51]. Furthermore, the refractive index of $In_{1-x}Ga_xAs_yP_{1-y}$ is higher than that of InP [52]. Therefore, a structure with a quaternary layer between InP layers is a natural waveguide with a tunable core bandgap. Passive waveguides, modulators, amplifiers, lasers and detectors can all be fabricated with the same template epitaxial design shown in Fig. 1.9. Optoelectronic devices with a pin

junction can be fabricated by doping InP as shown in Fig. 1.9-c. This simple bulk heterostructure is usually modified to include multiple quantum wells (MQW) or quantum dots (QD) for quantum-confined devices [53].

Although InP/InGaAsP heterostructure is very suitable for individual photonic devices, monolithic integration of these devices is not an easy task. The most significant reason is the mismatch of core layer bandgap between active and passive devices. For example, while laser diodes, photodetectors and SOAs comprise core layers with bandgap energies smaller than the photon energy, the optimal bandgap energies of electroabsorption modulators (EAM), phase modulators and passive waveguides are larger than the photon energy and different from each other. While quantum structures improve the performance of active devices, bulk core layer is better for passive devices because of the lower propagation loss. The monolithic integration of these devices is possible only with special active-passive integration methods such as butt-joint regrowth, selective-area growth, offset quantum well, dual quantum well, asymmetric twin waveguide and quantum well intermixing [54]. These active-passive integration methods usually increase the cost and complexity, thus reduce the yield of photonic chips. Therefore, both improvement of photonic integration technologies and modification of photonic device design for better integrability are demanded.

1.3 INTEGRATED PHOTONIC SWITCHES

1.3.1 Important Characteristics of Optical Switches

A brief review of basic characteristics of optical switches is essential to evaluate the present state and requirements of integrated photonic switching. Characteristics of optical switches can be classified into two major groups as the characteristics related to general configuration and the characteristics related to device performance.

1.3.1.1 Characteristics Related to General Configuration

These are fundamental characteristics depending on the switching scheme, so they

usually cannot be improved with design and optimization. The most important ones are explained briefly.

Switching domain (space, time and wavelength domain switching):
Space switching is the most common type and is based on forming a physical light path to a point in space. Space switching is a necessary functionality for OPS even if other kinds of switches are available. Time switching requires an optical memory function to control the temporal position of the optical signal. Buffering for OPS can be considered as time domain switching. Wavelength switching is equivalent to wavelength conversion. In optical communications, wavelength switching is used in order to rearrange the distribution of wavelength channels among multiple signals.

Degree of blocking (strictly nonblocking, wide-sense nonblocking, rearrangeably nonblocking and blocking switches):
Strictly nonblocking switches can route signals at different inputs to different ports simultaneously without blocking any established light paths. On the contrary, blocking switches cannot form new light paths if they are already switching a signal. Rearrangeably and wide-sense nonblocking switches can be operated as nonblocking switches under certain circumstances. Strictly nonblocking switches are desirable because they can route variable-size asynchronous packets [55], and have more relaxed buffering requirements compared to blocking switches. Synchronization increases the latency and power consumption, and reduces the network utilization efficiency [56].

Degree of transparency (strictly transparent, amplitude transparent, and digital transparent switches) [57,58]:
A strictly transparent switch preserves both amplitude and phase information, and can route signals with arbitrary modulation formats and bit rates. Amplitude transparent switches are transparent to intensity-modulated digital or analog signals, whereas digital transparent switches are transparent to only digital intensity modulation. The advantages of strict transparency have been emphasized recently because of the increasing employment of advanced modulation formats, which encode data in both intensity and phase of the light wave [59].

Switch control technology (all-optical, electro-optical, thermo-optical, mechanical):
Most switches proposed for OPS routing are electro-optical devices because of the maturity of electronic processing technology and the superiority of their reconfiguration speed compared to thermal and mechanical switches. All-optical switches usually utilize nonlinearities to control the switch in the optical domain and can achieve ultra-high speed approaching levels of Tb/s [60,61]. The most serious obstacles of all-optical switches are the weak nonlinearities in semiconductors used for photonic integration and the primitive status of optical signal processing. Both thermo-optical and mechanical switches have typical reconfiguration times in the range of ms, so they are not compatible with OPS.

Scalability:
Scalability is the technical possibility of enhancing the size of an optical switch in terms of the number of ports. Large-capacity routers have to deploy switches with a vast number of ports, so scalability is among the important factors determining the compatibility of switches with OPS. Scalability is not a single parameter, but it is a complicated qualitative measure influenced by several parameters including insertion loss, extinction ratio, footprint, power consumption, and cost.

Multicast capability:
Multicast switches are capable of switching a signal to multiple nodes, whereas singlecast switches can form a connection between a single input and a single output. Multicast switching is desirable for applications including video conferencing, high-definition television, interactive distance learning, and distributed games [62].

Physical size:
The physical size of an integrated switch affects its scalability for multiple reasons. In PICs, the propagation loss increases with the device size. In addition, especially compound semiconductor wafers are limited in size, which limits the number of on-chip components depending on the device size.

1.3.1.2 Characteristics Related to Device Performance

Switching speed:

Switching speed is defined by the time it takes for the switch to reconfigure from one state to another. Reconfiguration time is a useless transition period, so it should be covered by the guard time in OPS. With the average packet size in the range of a few kilobytes and future bit rates possibly close to or higher than 1 Tb/s, the packet sizes are expected to be shorter than a few nanoseconds, which means that the reconfiguration time of packet switches should be in the in the range of a few ns or hundreds of ps.

Extinction ratio:

It is the ratio of the optical power at a port when the signal is routed to that port, to the power when no connection is intended with that port. The extinction ratio of optical switches is more important than that of modulators because in large-scale OPS networks, the packets are routed through several nodes [63,64]. Crosstalk introduces penalty at each switching stage [65], so a low extinction ratio can limit the number of switching hops.

Insertion loss:

Insertion loss is the power loss caused by switching. Minimization of the insertion loss is a difficult task especially for switches with large port counts. The maximum number of switching hops and power consumption are strongly dependent on the insertion loss.

Polarization dependent loss (PDL):

PDL is the measure of dependence of loss on the polarization state of light. Very low PDL is requested for two reasons. First, the polarization cannot be maintained in regular single-mode fibers. Polarization-dependent devices have to be armed with polarization controlling components, which are difficult to integrate with other devices [66]. Second, recently polarization division multiplexing (PDM) has been employed in high-bit-rate optical communications to double the spectral efficiency [67-69]. Transparency cannot be achieved by polarization-dependent devices in PDM networks.

Excess noise:

Regeneration in the optical domain is immature and limited. Therefore, optical switches with very low excess noise are preferred. The major sources of loss are amplified spontaneous emission in gain media [70], nonlinear crosstalk between channels [71], and crosstalk between signals routed to different ports.

Uniformity among ports:

Power difference among ports can lead to large power imbalance between signals depending on their paths, and has a possibility of deteriorating the signal quality.

1.3.2 Present State of Integrated Photonic Switches

Owing to the long history of research, there are several types of optical switches in the literature. However, until the devices in this thesis were reported, even the largest-scale semiconductor integrated optical switches had ten or less output ports. Recent research on integrated semiconductor photonic switches for OPS has focused on broadcast-and-select SOA gate array switches and wavelength routing switches. Broadcast-and-select switches divide the signal to N arms using a passive coupler and amplify the signal in the selected arm using an SOA. Recently, integrated 1×8 and 16×16 InP switches were reported with this scheme [72-73]. These works are very promising because of the level of photonic integration, but broadcast-and-select switches are expected to suffer from accumulation of amplified spontaneous emission (ASE) noise if the number of ports increases. Dynamic range and interchannel crosstalk due to SOA nonlinearities are other serious problems [74]. Another excellent demonstration of monolithic photonic switching is a wavelength routing 8×8 switch consisting of eight wavelength converters and an arrayed waveguide grating (AWG) [45]. Wavelength routing switches cannot operate with WDM signals. Moreover, most wavelength converters including the ones in [45] are not strictly transparent, which means that they are not compatible with phase modulated signals. This is a serious problem if we consider that advanced modulation formats such as differential quadrature phase-shift keying (DQPSK) are likely to be used because of their high spectral efficiency. Because of these technical difficulties and other problems mostly

related to power consumption, broadcast-and-select and wavelength routing switches do not offer obvious advantages over electronic switches [75]. Another option is the integration of many 1×2 or 2×2 switches, such as directional-coupler switches, digital optical switches, etc, to obtain large-scale switches [76-77]. However, the signals have to pass through several switching elements, each imposing unavoidable reduction in signal quality. The footprint of these devices also becomes a problem in case of large port counts. Therefore, a different integrated switching technology with wavelength insensitivity, strict transparency, and port count scalability should be developed for feasible high-throughput OPS. Experimental research on integrated phased-array photonic switches to fulfill these requirements and their applications in OPS are the topics of this dissertation.

1.4 CONTRIBUTION AND ORGANIZATION OF THE DISSERTATION

1.4.1 Contribution of the Dissertation

This dissertation focuses on integrated photonic devices and their applications in ultra-high-capacity OPS networks. The research efforts reported here cover a number of experimental achievements for the first time in the literature.

Monolithically integrated InP/InGaAsP phased-array photonic switches with record-breaking output port counts are fabricated. The first 16-port fully integrated semiconductor photonic switch in the literature, presented in Chapter 3, has demonstrated promising device characteristics such as flat response extending over the C-band, low polarization dependence, insertion loss relatively insensitive to the port count, and complete dynamic switching in time scales of nanoseconds. These characteristics set the state of the art in semiconductor photonic switching in various aspects.

Novel amplitude-controlled phased-array switches are also proposed for the first time for multicast switching. Amplitude-controlled phased-array scheme has a

significantly large degree of freedom in terms of the engineering of output mode distribution. It has been theoretically demonstrated that switching can be achieved to an arbitrary combination of arbitrary outputs simultaneously.

Furthermore, this work includes the design, fabrication and characterization of an advanced InP photonic integrated circuit (PIC) for 100-port monolithic photonic switching for the first time. In terms of photonic integration technology, this circuit is among the largest scale PICs reported so far. In terms of optical communication, such a 100-port monolithic switch with ultra broad spectral response offers an unparalleled potential of data capacity. With the help of the SOAs monolithically integrated with phased-array switches, this PIC has demonstrated very high extinction ratio and relatively low on-chip loss. The experimentally verified integrability, port count scalability, wavelength insensitivity and high dynamic speed of the switches presented in this dissertation form a good combination for ultra-large-capacity transparent OPS.

The potential for large-capacity OPS was experimentally verified by switching high-bit-rate packets with different modulation formats through a simplified OPS node comprising an integrated phased-array switch, a switch controller and a label processor. Owing to the strict transparency and broad bandwidth of the OPS node in the data plane, both 160-Gb/s on-off keying (OOK) and 120-Gb/s WDM differential phase-shift keying (DPSK) packets were switched with very low penalties. As explained in Section 1.1.3.3, both WDM switching and compatibility with phase modulation are very desirable characteristics of OPS routers.

Our analysis of power consumption in buffered large-capacity $N\times N$ optical packet switch fabrics has revealed that the total energy per bit consumed by the switch controller, switch matrix, and tunable optical buffer deploying phased-array switches is less than 1.5 pJ/bit in a 1000×1000 switching configuration. According to this analysis, based on large-scale PICs such as the one experimentally investigated in this thesis, phased-array switching is almost ten times more energy efficient than broadcast-and-select switching if the number of input and output ports is on the order of 1000. These results are important since they offer the possibility of Pb/s-scale OPS (utilizing the broad bandwidth of phased-array switching along with the large number of ports) with high energy efficiencies.

1.4.2 Organization of the Dissertation

Chapter 2 describes optical phased-array switching. A detailed analytical explanation and design considerations are presented. Moreover, a novel amplitude-controlled phased-array switch is introduced with an explanation of multicast switching using this device. In Chapter 3, the design and fabrication of $1 \times N$ integrated phased-array photonic switches is explained along with the results of experimental device characterization. Chapter 4 is on the OPS experiments carried out with a simplified OPS router that comprises a phased-array switch, a switch controller and an all-optical label processor. Chapter 5 introduces the design, fabrication and characterization of an advanced photonic integrated circuit for 100-port monolithic switching. Chapter 6 presents the power consumption analysis of large-capacity buffered OPS matrix switches utilizing strictly transparent photonic switches for switching and tunable buffering. This chapter serves the purpose of assessing the feasibility of optical packet switching with the technologies presented in this thesis. Finally, Chapter 7 concludes the dissertation and discusses the technological challenges that have to be addressed for cost-effective implementation of optical packet switching based on phased-array switches.

REFERENCES OF CHAPTER 1

[1] A. M. Odlyzko, “Internet traffic growth: sources and implications,” in Proc. SPIE-Optical Transmission Systems and Equipment WDM Networking II, 2003, vol. 5247, pp. 1-15.

[2] R. W. Tkach, “Scaling optical communications for the next decade and beyond,” Bell Labs Technical Journal, vol. 14, no. 4, pp. 3-10, 2010.

[3] “Hyperconnectivity and the approaching zettabyte era,” white paper, http://www.cisco.com/en/US/solutions/collateral/ns341/ns525/ns537/ns705/ns827/VNIHyperconnectivity WP.pdf.

[4] E. Desurvire, C. R. Giles, and J. L. Zyskind, “Erbium-doped fiber amplifier,” U.S. Patent 5 027 079, June 25, 1991.

[5] A. A. M. Saleh, “Optical WDM technology for networking and switching applications,” in Proc. Conference on Optical Fiber Communication, 1992, Paper ThC1.

[6] A. Sano, et al., “69.1-Tb/s (432x170Gb/s) C- and extended L-band transmission over 240 km using PDM-16-QAM modulation and digital coherent detection,” in Proc. Conference on Optical Fiber Communication, San Diego, CA, 2010, Paper PDPB7.

[7] Cisco CRS-3, http://ciscosystems.com/en/US/products/ps5763, Apr. 2010..

[8] H. J. S. Dorren, N. Calabretta, and O. Raz, “Scaling all-optical packet routers: how much buffering is required?,” Journal of Optical Networking, vol. 7, no. 11, pp. 936-946, Nov. 2008.

[9] G. R. Hill, “Wavelength domain optical network techniques,” Proceedings of the IEEE, vol. 77, no. 1, pp. 121-132, Jan. 1990.

[10] M. Maier, Optical Switching Networks. New York, NY: Cambridge University Press, 2008, pp. 9-12.

[11] S. J. B. Yoo, “Optical packet and burst switching technologies for the future photonic internet,” Journal of Lightwave Technology, vol. 24, no. 12, pp. 4468-4492, Dec. 2006.

[12] Y. Tachikawa, Y. Inoue, M. Kawachi, H. Takahashi, and K. Inoue, “Arrayed-waveguide grating add-drop multiplexer with loop-back optical paths,” Electronics Letters, vol. 29, no. 24, pp. 2133-2134, Nov. 1993.

[13] C. G. M. Freeburg, T. Uitterdijk, Y. S. Oei, M. K. Smit, F. H. Groen, E. G. Metaal, P. Demeester, and H. J. Frankena, “First InP-based reconfigurable integrated add-drop multiplexer,” IEEE Photonics Technology Letters, vol. 9, no. 2, pp. 188-190, Feb. 1997.

[14] S. Johansson, M. Lindblom, P. Granestrand, B. Lagerstrom, and L. Thylen, “Optical cross-connect system in broad-band networks: system concepts and demonstrators description,” Journal of Lightwave Technology, vol. 11, no. 5-6, pp. 688-694, May/June 1993.

[15] K. Vlachos, et al., “Photonics in switching: enabling technologies and subsystem design,” Journal of Optical Networking, vol. 8, no. 5, pp. 404-428, May 2009.

[16] R. Parthiban, R. S. Tucker, C. Leckie, A. Zalesky, and A. V. Tran, “Does optical burst switching have a role in the network?,” in Proc. Conference on Optical Fiber Communication, Anaheim, CA, 2005, Paper OWC2.

[17] H. Onaka, et al., “WDM optical packet interconnection using multi-gate SOA switch architecture for peta-flops ultra-high performance computing systems,” in Proc. European Conference on Optical Communication, 2006, pp. 1-2.

[18] M. Maier, Optical Switching Networks. New York, NY: Cambridge University Press, 2008, pp. 138-143.

[19] H. Furukawa, N. Wada, and T. Miyazaki, “640 Gb/s (64-wavelength × 10 Gb/s) data-rate wide-colored NRZ-DPSK optical packet switching and buffering demonstration,” Journal of Lightwave Technology, vol. 28, no. 4, pp. 336-343, Feb. 2010.

[20] R. P. Luijten and R. Grzybowski, “The OSMOSIS optical packet switch for supercomputers,” in Proc. Optical Fiber Communication Conference, 2009, Paper OTuF3.

[21] R. Hemenway, R. Grzybowski, C. Minkenberg, and R. Luijten, “Optical-packet-switched interconnect for supercomputer applications,” Journal of Optical Networking, vol. 3, no. 12, pp. 900-913, Dec. 2004.

[22] A. Shacham, B. A. Small, O. L. Ladouceur, and K. Bergman, “A fully implemented 12 × 12 data vortex optical packet switching interconnection network,” Journal of Lightwave Technology, vol. 23, no. 10, pp. 3066-3075, Oct. 2005.

[23] N. Calabretta, O. Raz, W. Wang, T. Ditewig, F. Gomez Agis, S. Zhang, H. de Waardt, E. Tangdiongga, and H. J. S. Dorren, “Scalable optical packet switch for optical packets with multiple modulation formats and data rates,” in Proc. European Conference on Optical Communication, 2009, Paper 4.6.3.

[24] M. Scaffardi, E. Lazzeri, H. Furukawa, N. Wada, T. Miyazaki, L. Poti, and A. Bogoni, “160 Gb/s/port 2×2 OPS node test-bed performing 50 Gchip/s all-optical active label processing with contention detection,” Journal of Lightwave Technology, vol. 28, no. 6, pp. 922-930, Mar. 2010.

[25] J. P. Mack, K. N. Nguyen, M. M. Dummer, E. F. Burmeister, H. N. Poulsen, B. Stamenic, G. Kurczveil, J. E. Bowers, L. A. Coldren, and D. J. Blumenthal, “40 Gb/s buffered 2x2 optical packet switching using photonic integrated circuits,” in Proc. Conference on Lasers and Electro-Optics, 2009, Paper CMJJ6.

[26] G. Appenzeller, I. Keslassy, and N. McKeown, “Sizing router buffers,” in Proc. SIGCOMM, 2004, pp. 281-292.

[27] K. Takeda, M. Takenaka, T. Tanemura, and Y. Nakano, “All-optical flip-flop based on Mach-Zehnder interferometer bistable laser diode,” in Proc. European Conference on Optical Communication, Vienna, Austria, 2009, Paper 1.2.5.

[28] M. T. Hill, et al., “A fast low-power optical memory based on coupled micro-ring lasers,” Nature, vol. 432, pp. 206-209, Nov. 2004.

[29] G. Appenzeller, I. Keslassy, and N. McKeown, “Sizing router buffers,” in Proc. SIGCOMM, 2004, pp. 281-292.

[30] N. Beheshti, Y. Ganjali, R. Rajaduray, D. Blumenthal, and N. McKeown, “Buffer sizing in all-optical packet switches,” in Proc. Optical Fiber Communication Conference, 2006, Paper OThF8.

[31] S. Sygletos, I. Tomkos, and J. Leuthold, “Technological challenges on the road toward transparent networking,” Journal of Optical Networking, vol. 7, no. 4, pp. 321-350, Apr. 2008.

[32] S. E. Miller, “Integrated optics: an introduction,” Bell Systems Technological Journal, vol. 48, pp. 2059-2069, Sep. 1969.

[33] G. E. Moore, “Cramming more components onto integrated circuits,” Electronics, vol. 38, no. 8, pp. 114–117, Apr. 19, 1965.

[34] D. J. Blumenthal and M. Usami, “Optical signal processing: the roadmap towards high-speed optical packet/burst switching,” Short course, presented at European Conference on Optical Communication, Vienna, Austria, 2009.

[35] E. Ozbay, “Plasmonics: merging photonics and electronics at nanoscale dimensions,” Science, vol. 311, pp. 189-193, Jan. 2006.

[36] W. L. Barnes, A. Dereux, and T. W. Ebbesen, “Surface plasmon subwavelength optics,” Nature, vol. 424, pp. 824-830, Aug. 2003.

[37] C. A. M. Steenbergen, C. van Dam, A. Looijen, C. G. P. Herben, M. de Kok, M. K. Smit, J. W. Pedersen, I. Moerman, R. G. F. Baets, and B. H. Verbeek, “Compact low loss 8 x 10 GHz polarisation independent WDM receiver,” in Proc. European Conference on Optical Communication, 1996, vol. 1, pp. 129-133, Paper MoC.4.1.

[38] M. Ziari, et al, “Large scale integration of photonic integration circuits on Indium Phosphide and high-index contrast Si platforms,” in Proc. European Conference on Optical Communication, 2009, Paper 1.7.2.

[39] T. Miya, “Silica-based planar lightwave circuits: passive and thermally active devices,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 6, no. 1, pp. 38-45, Jan./Feb. 2000.

[40] C. R. Doerr and K. Okamoto, “Advances in silica planar lightwave circuits,” Journal of Lightwave Technology, vol. 24, no. 12, pp. 4763-4789, Dec. 2006.

[41] P.S. Cho, G. Harston, A. Greenblatt, A. Kaplan, Y. Achiam, R. M. Bertenburg, A. Brennemann, B. Adoram, P. Goldgeiger, and A. Hershkovits, “Integrated optical coherent balanced receiver,” in Proc. Optical Fiber Communication Conference, 2006, Paper CThB2.

[42] H. Okayama and M. Kawahara, “Prototype 32 × 32 optical switch matrix,” Electronics Letters, vol. 30, no. 14, pp. 1128-1129, Jul. 1994.

[43] C. R. Doerr, et al., “Monolithic polarization and phase diversity coherent receiver in silicon,” Journal of Lightwave Technology, vol. 28, no. 4, pp. 520-525, Feb. 2010.

[44] N. S. Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, “Optical 4x4 hitless silicon router for optical networks-on-chip (NoC),” Optics Express, vol. 16, no. 20, pp. 15915-15922, Sep. 2008.

[45] S. C. Nicholes, M. L. Masanovic, B. Jevremovic, E. Lively, L. A. Coldren, and D. J. Blumenthal, “An 8 x 8 InP monolithic tunable optical router (MOTOR) packet forwarding chip,” Journal of Lightwave Technology, vol. 28, no. 4, pp. 641-650, Feb. 2010.

[46] S. Nagarajan et al., “Single-chip 40-channel InP transmitter photonic integrated circuit capable of aggregate data rate of 1.6 Tbit/s,” Electronics Letters, vol. 42, no. 13, pp. 771-773, Jun. 2006.
[47] L. Liu, R. Kumar, K. Huybrechts, T. Spuesens, G. Roelkens, E. J. Geluk. T. de Vries, P. Regreny, D. van Thourhout, R. Baets, and Geert Morthier, “An ultra-small, low-power, all-optical flip-flop memory on a silicon chip,” Nature Photonics, vol. 4, pp. 182-187, Mar. 2010.
[48] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, “Electrically pumped hybrid AlGaInAs-silicon evanescent laser,” Optics Express, vol. 14, pp. 9203-9210, Sep. 2006.
[49] B. A. Saleh and M. C. Teich. Fundamentals of Photonics. New York, NY: Wiley, 1991, pp. 238-271.
[50] R. G. Hunsperger. Integrated Optics: Theory and Technology. New York, NY: Springer, 2009.
[51] R. E. Nahory, M. A. Pollack, W. D. Johnston, and R. L. Barns, “Band gap versus composition and demonstration of Vegard’s law for $In_{1-x}Ga_xAs_yP_{1-y}$ lattice matched to InP,” Applied Physics Letters, vol. 33, no. 7, pp. 659-661, Oct. 1978.
[52] S. Adachi. Physical Properties of III-V Semiconductor Compounds. New York, NY: Wiley, 1992, pp. 165-168.
[53] L. Coldren and S. Corzine. Diode Lasers and Photonic Integrated Circuits. New York, NY: Wiley, 1995.
[54] E. J. Skogen, J. W. Raring, G. B. Morrison, C. S. Wang, V. Lal, M. L. Masanovic and L. A. Coldren, “Monolithically integrated active components: a quantum-well intermixing approach,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 11, no.2, pp. 343-355, Mar./Apr. 2005.
[55] Z. Haas, “The staggering switch: an electronically controlled optical packet switch,” J. Lightwave Technol., vol. 11, no. 5/6, pp. 925-936, May/Jun. 1993.
[56] B.-Y. Choi, S. Moon, Z.-L. Zhang, K. Papagiannaki, C. Diot, “Analysis of point-to-point packet delay in an operational network,” in Proc. IEEE Infocom, 2004, vol. 23, no. 1, pp. 1798-1808.
[57] R. Tkach, E. Goldstein, J. Nagel and J. Strand, “Fundamental limits of optical transparency,” in Proc. Optical Fiber Communication Conf., 1998, pp. 161–162.
[58] A. A. M. Saleh, “Transparent optical networks for the next-generation information infrastructure,” in Proc. Optical Fiber Communication Conference, 1995, vol. 8, pp. 241-243.
[59] G. Bosco, A. Carena, V. Curri, R. Gaudino, P. Poggiolini, “Modulation formats suitable for ultrahigh spectral efficient WDM systems,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 10, no. 2, pp. 321-328, Mar./Apr. 2004.
[60] H. Nakamura, et al., “Ultra-fast photonic crystal/quantum dot all-optical switch for future photonic networks,” Optics Express, vol. 12, no. 26, pp. 6606-6614, Dec. 2004.
[61] O. Wada, “Femtosecond all-optical devices for ultrafast communication and signal processing,” New Journal of Physics, vol. 6, p. 183, 2004.
[62] N. K. Singhal and B. Mukherjee, “Protecting multicast sessions in WDM optical mesh networks,” Journal of Lightwave Technology, vol. 21, no. 4, pp. 884-892, Apr. 2003.
[63] O. L. Ladouceur, B. A. Small, and K. Bergman, “Physical layer scalability of WDM optical packet

interconnection networks," Journal of Lightwave Technology, vol. 24, no. 1, pp. 262-270, Jan. 2006.
[64] W. J. Dally and B. Towles, Principles and Practices of Interconnection Networks. San Francisco, CA: Morgan Kaufmann, 2004.
[65] L. A. Buckman, L. P. Chen, and K. Y. Lau, "Crosstalk penalty in all-optical distributed switching networks," IEEE Photonics Technology Letters, vol. 9, no. 2, pp. 250-252, Feb. 1997.
[66] L. M. Augustin, J. J. G. M. V. Tol, E. J. Geluk, and M. K. Smit, "Short polarization converter optimized for active-passive integration in InGaAsP/InP," IEEE Photonics Technology Letters, vol. 19, no. 20, pp. 1673-1673, Oct. 2007.
[67] M. Kato, et al., "Transmitter PIC for 10-channel x 40Gb/s per channel polarization -multiplexed RZ-DQPSK modulation," in Proc. Optical Fiber Communication Conference., 2009, Paper OThN2.
[68] A. Sano, H. Masuda, T. Kobayashi, M. Fujiwara, K. Horikoshi, E, Yoshida, Y. Miyamoto, M. Matsui, M. Mizoguchi, H. Yamazaki, Y. Sakamaki, and H. Ishii, "69.1-Tb/s (432 x 171 Gb/s) C- and extended L-band transmission over 240 km using PDM-16-QAM modulation and digital coherent detection," in Proc. Optical Fiber Communication Conference., 2010, Paper PDPB7.
[69] H. Furukawa, N. Wada, N. Takezawa, K. Nashimoto, and T. Miyazaki, "640 (2×32λ×10) Gb/s polarization-multiplexed, wide-colored optical packet switching achieved by polarization-independent high-speed PLZT switch," in Proc. Optical Fiber Communication Conference, 2008, Paper OTuL7.
[70] M. J. Connelly. Semiconductor Optical Amplifiers. Dordrecht, The Netherlands: Kluwer, 2002, pp. 12-15.
[71] M. G. Oberg and N. A. Olsson, "Crosstalk between intensity-modulated wavelength-division multiplexed signals in a semiconductor laser amplifier," IEEE Journal of Quantum Electronics, vol. QE-24, no. 1, pp. 52-59, Jan. 1998.
[72] Y. Kai, K. Sone, S. Yoshida, Y. Aoki, G. Nakagawa, and S. Kinoshita, "A compact and lossless 8x8 SOA gate switch subsystem for WDM optical packet interconnections," presented at European Conference on Optical Communication, Brussels, Belgium, 2008, Paper We.2.D.4.
[73] H. Wang, A. Wonfor, K. A. Williams, R. V. Penty, and I. H. White, "Demonstration of a lossless monolithic 16x16 QW SOA switch," in Proc. European Conference on Optical Communication (Postdeadline papers), 2009, pp. 1-2.
[74] M. G. Oberg and N. A. Olsson, "Crosstalk between intensity-modulated wavelength-division multiplexed signals in a semiconductor laser amplifier," IEEE Journal of Quantum Electronics, vol. QE-24, no. 1, pp. 52-59, Jan. 1988.
[75] R. S. Tucker, "The role of optics and electronics in high-capacity routers," Journal of Lightwave Technology, vol. 24, no. 12, pp. 4655-4673, Dec. 2006.
[76] K. Hamamoto, S. Sugou, K. Komatsu, and M. Kitamura, "Extremely low loss 4 × 4 GaAs/AlGaAs optical switch matrix," Electronics Letters, vol. 29, no. 17, pp. 1580-1581, Aug. 1993.
[77] R. Krahenbuhl, R. Kyburz, W. Vogt, M. Bachmann, T. Brenner, E. Gini, and H. Melchior, "Low-loss polarization-insensitive InP-InGaAsP optical space switches for fiber optical communication," IEEE

Photonics Technology Letters, vol. 8, no. 5, pp. 632-634, May 1996.

CHAPTER 2
INTEGRATED PHASED-ARRAY PHOTONIC SWITCHING

2.1 INTRODUCTION

The overview of optical switching technologies in the previous chapter has revealed that strictly transparent, wavelength-insensitive, integrated optical switches with scalable data capacity are of crucial importance for optical packet switching (OPS). The purpose of this chapter is to present a comprehensive introduction of integrated $1 \times N$ phased-array photonic switch, which has a potential to satisfy these requirements. A detailed explanation of the principle of operation, comparison with other switches and the key points of device design are given to make it easier to grasp the following chapters and to make it possible for the readers to design similar devices if necessary. In addition to phased-array photonic switches, this chapter introduces a novel type of amplitude-controlled phased-array switch capable of switching to an arbitrary number of ports simultaneously.

Section 2.2 presents a brief introduction of phased array scheme and an overview of optical phased-array devices in the literature. Section 2.3 presents the integrated phased-array photonic switches investigated in this study. The analytical derivation of phased-array switching is available in Section 2.4. In Section 2.5, design rules to achieve good switching characteristics are described based on the analysis in the previous section. Section 2.6 compares phased-array switches with other types of switches especially in terms of large-capacity packet switching potential. Section 2.7 introduces amplitude-controlled phased-array switches and discusses their potential for

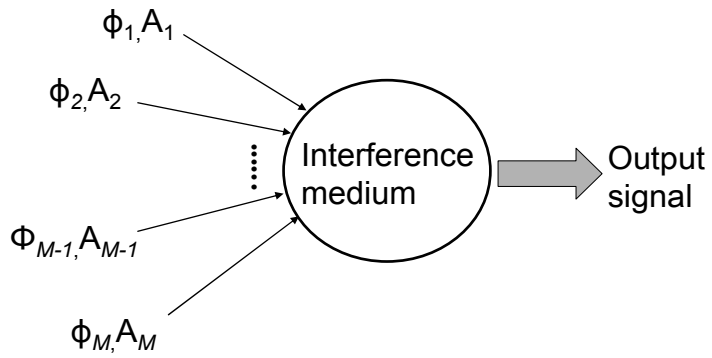


Fig. 2.1 General principle of operation of a phased-array device (ϕ: phase, A: amplitude).

multicasting. Finally, Section 2.8 summarizes the chapter.

2.2 BASICS AND BRIEF OVERVIEW OF OPTICAL PHASED ARRAYS

Phased arrays are components or systems that control the spatial distribution of electromagnetic waves through phase conditions of an array of signals. Phased-array antenna arrays, optical beam deflectors, optical multiplexers/demultiplexers and optical switches are major applications of phased arrays. Independent of the implementation and application, all phased arrays operate by interference of multiple coherent signals that have an engineered phase distribution as illustrated in Fig. 1. Phased arrays were invented by Karl Ferdinand Braun in 1905 to improve the directivity of radio waves [1]. Consequently, the first application of phased arrays was antenna arrays until the adoption of phased array principle in optical technologies in 1970s [2-4]. These initial devices used guided-wave phase shifters and free-space optics for optical beam steering [5]. The basic condition of steering a single beam at the output plane of a phased-array device is a linear slope of phase in the arrayed signals.

Arrayed waveguide grating (AWG) multiplexer/demultiplexer, developed in 1991 [6,7], has been the most widespread optical phased-array device so far. Unlike the earlier beam steering devices, AWGs are completely integrated. Both distribution of the input signal into arrayed arms and the interference of phased signals are implemented

with star couplers. A linear phase slope is maintained by a gradually changing length of arrayed waveguides. Since the effective phase difference depends on the wavelength, signals at different wavelengths are separated at the output. These devices are used for both multiplexing and demultiplexing of wavelength channels in wavelength-division multiplexed (WDM) optical communication networks [8,9]. AWG technology has reached a level of maturity and devices with hundreds of channels are fabricated and deployed in networks [10].

The third application of optical phased arrays is optical switching, which is the main focus of this chapter. There are only a limited number of optical phased-array switches in the literature. The first phased-array device referred as an optical switch utilized AlGaAs/GaAs guided-wave phase shifters and slab waveguides for integrated beam steering to nine output ports [11]. In spite of the relatively large size of the device and low coupling efficiency to the output waveguides, this device is important as a pioneering $1 \times N$ optical space switch. Next, a design similar to an AWG was developed by using SiON-SiO_2 waveguides with thermooptical phase shifters for up to 1×8 switching capability [12]. This device suffers from large footprint and slow dynamic operation limited by the response time of the thermooptic effect. Recently, a 1×4 switch was also demonstrated incorporating directional couplers instead of a single interferometric medium. Nevertheless, this device configuration is not scalable because of the number of waveguide crossings and the length of the coupling section [13]. A high-speed switching module combining an AlGaAs phase shifter array with free-space lenses was also demonstrated based on the phased array scheme [14]. Although free space optics has the advantage of coupling a large number of waveguide modes simultaneously, switching matrices consisting of free-space components do not offer merits in terms of size, cost, and reliability as discussed in Chapter 1. Switches uniting a phased array with the imaging property of multimode waveguides were also developed [15]. However, relatively low tolerance to fabrication conditions and footprint are problems of multimode-interferometer devices.

From this brief review of optical phased-array switches, one can understand that although the multi-port switching potential of phased-array devices has been noticed by several researchers, none of these demonstrations incorporates the speed, footprint, and

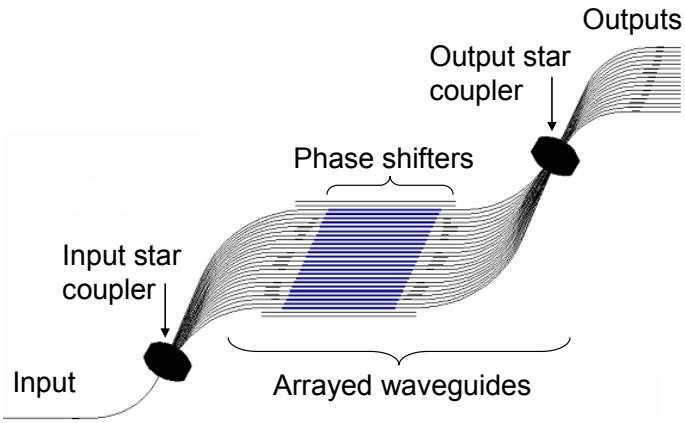


Fig. 2.2 Planar layout of a $1 \times N$ phased-array photonic switch.

integrability necessary for ultra-large-capacity optical packet switching. High-speed integrated phased-array photonic switches, introduced in the next section, have been proposed and demonstrated to solve this problem [16].

2.3 INTEGRATED PHASED-ARRAY PHOTONIC SWITCHES

The phased-array photonic switch investigated here is an entirely monolithically integrated semiconductor photonic device consisting of two star couplers, an array of phase shifters and output waveguides as shown in Fig. 2.2. Star couplers are passive optical devices that couple multiple optical waveguide modes at one plane with the modes at the other plane [17]. In the phased-array switch, the input star coupler distributes the optical mode in the input waveguide among the arrayed waveguides by means of diffraction. All the waveguides in the array region between the star couplers are exactly equal in length, which is the reason of the antisymmetrical design. If the condition of equal arrayed waveguides is not satisfied, the device becomes highly wavelength dependent and operates like a tunable AWG. Each phase shifter at the center of the arrayed waveguides is used to manipulate the phase condition of individual waveguide mode separately. These phase-controlled signals diffract in the second star

coupler, whose output plane embodies the output waveguides. The optical mode pattern at the output plane depends on the phase conditions of array modes through interference. The basic single-port switching condition is satisfied by forming a linear phase slope in the array, analogous to beam steering in antenna arrays and optical phased arrays. In addition to single-port switching, arbitrary distribution of optical modes at the output plane are achievable by controlling the phase and amplitude conditions of arrayed signals with a modification of the device design in Fig. 2.2. This phenomenon is explained in Section 2.7.

This device design incorporates the large-port-count switching capability of optical phased arrays with integrability, small footprint, wavelength insensitivity, and high-speed response. A quantitative analysis of basic device characteristics has to be carried out to test the validity of this argument and compare the phased-array switch with other device technologies. The next section gives an analytical explanation of phased-array switching to form a basis for a quantitative evaluation and design guidelines.

2.4 ANALYTICAL EXPLANATION OF PHASED-ARRAY SWITCHING

An intuitive analysis of guided-wave optical phased-array devices can be carried out by using Fourier optics. Similar Fourier optics analyses have been done for AWGs previously [18]. The definition of expressions in the formulation is available in Table 2.1. An enlarged image of the output star coupler is presented in Fig. 2.3 to show the parameters referred as array pitch, output pitch and star coupler length. The waveguides on the star couplers are arranged on a circle centered at the center of the opposite waveguide plane. Therefore, the distance from the center of arrayed waveguides to any point on the intersection of output waveguides with the star coupler is equal to L. The indices from 0 to 3 refer to the input of input star coupler, output of input star coupler, input of output star coupler, and output of the output star coupler respectively.

The derivation begins with the mode field at the input waveguide. The field

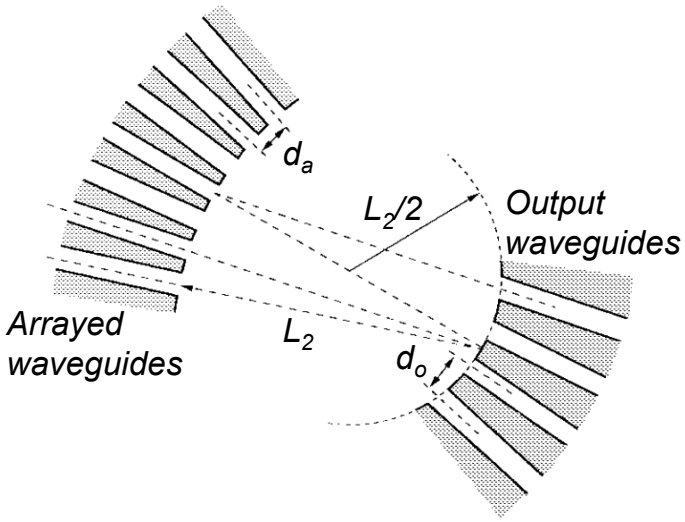


Fig. 2.3 Output star coupler (modified from [9]).

distribution at the output of the input star coupler is dependent on the field at the input via diffraction. As long as the inequality

$$L \gg \frac{\pi w^2}{4\lambda} \tag{2.1}$$

is valid, Fraunhofer diffraction approximation can be used in the star couplers. This relation is typically valid in both star couplers. Therefore,

TABLE 2.1

SYMBOLS IN PHASED-ARRAY SWITCHING ANALYSIS

Symbol	Explanation
f_0, f_1, f_2, f_3	Field (optical)
x_0, x_1, x_2, x_3	transverse distance
L_1, L_2	Length of input and output star couplers
n_{eff}	Effective refractive index in star couplers
λ	Wavelength
w_0, w_1, w_2, w_3	Mode width
d_a	Array pitch
d_o	Output pitch
M	Number of arrayed waveguides

$$f(x_1) = \frac{1}{\sqrt{\alpha_\upsilon}} \mathcal{F}\{f(x_0)\}\Big|_{u=\frac{x_1}{\alpha_\upsilon}}, \tag{2.2}$$

where

$$\alpha_\upsilon = \frac{\lambda L_1}{n_{eff}}. \tag{2.3}$$

The wavelength dependence of α_υ can be ignored inside the communications band, so this parameter is referred as α_1 and α_2 for the input and output star couplers respectively. The field at the output of the first star coupler has a broadening proportional to the length of the star coupler according to (2.2) and (2.3). Although waveguide modes are well-known to be sinusoidal inside the core and exponentially decaying in the cladding, an analytic solution can be derived more easily if we assume that it has a Gaussian distribution. The normalized field at the input waveguide is

$$f_0(x_0) = \sqrt[4]{\frac{2}{\pi w_0^{\,2}}} \cdot exp\left[-\left(\frac{x_0}{w_0}\right)^2\right]. \tag{2.4}$$

Therefore, the field at the output of the first star coupler is

$$f_1'(x_1) = \sqrt[4]{\frac{2\pi w_0^{\,2}}{\alpha_1^{\,2}}} \cdot exp\left[-\left(\frac{\pi w_0 x_1}{\alpha_1}\right)^2\right] \tag{2.5}$$

As a natural result of diffraction theory, the width of the mode at the output of first star coupler is inversely proportional to the width of the input waveguide. This wide Gaussian function is the envelope which defines the distribution of optical coupling to the arrayed waveguides. The exact expression of coupling an optical field with a waveguide is the overlap integral between the modes as in

$$\eta = \int_{-\infty}^{\infty} f_w(x_1) f_1'(x_1)\, dx, \tag{2.6}$$

where f_w is the waveguide mode function. Since f_1' function is very slowly changing compared to f_w, it can be assumed as a constant equal to its value in the middle of the waveguide.

$$\eta = f_1^{'}(x_w)\int_{-\infty}^{\infty} f_w(x_1)\,dx\,, \tag{2.7}$$

where x_w is the position of the waveguide. The field distribution at the input of the array plane consisting of waveguides with identical modes is then equal to

$$f_1(x_1) = C\sum_{i=-(M-1)/2}^{(M-1)/2} f_1^{'}(d_a\cdot i)\cdot f_w(x_1 - d_a\cdot i)\,. \tag{2.8}$$

The constant terms are referred as C independent of their values from this point on. (2.8) is equivalent to the convolution of the waveguide mode with M delta functions multiplied by $f_1^{'}$. Using (2.4) and (2.5), this equation takes the form,

$$f_1(x_1) = \left\{\begin{array}{l} C\cdot exp\left[-\left(\dfrac{\pi w_0 x_1}{\alpha_1}\right)^2\right]\cdot \\ rect\left(\dfrac{x_1}{(M-1)\cdot d_a}\right)\cdot\sum_{i=-\infty}^{\infty}\delta(x_1 - d_a\cdot i)\end{array}\right\} * exp\left[-(x_1/w_1)^2\right]. \tag{2.9}$$

In (2.9), the first expression on the left side of the convolution sign is the Gaussian envelope; the rectangle function is due to the finite size of the arrayed waveguides; and the comb function has a period equal to the array pitch to account for the arrayed waveguides. The term on the right side of the convolution sign is the waveguide mode in the array plane input. If the phase shifters are left unbiased, and array pitch and waveguide width are equal at the input and output of the array plane, this expression is exactly the same at the input of the second star coupler because all the arrayed waveguides are equal in length. For single-output switching, a linearly changing phase component is inserted into the brackets as

$$f_2(x_2) = \left\{\begin{array}{l} C\cdot exp\left[-\left(\dfrac{\pi w_0 x_1}{\alpha_1}\right)^2\right]\cdot exp\left(\dfrac{jx_2\Delta\varphi}{d_a}\right)\cdot \\ rect\left(\dfrac{x_1}{(M-1)\cdot d_a}\right)\cdot\sum_{i=-\infty}^{\infty}\delta(x_1 - d_a\cdot i)\end{array}\right\} * exp\left[-(x_1/w_2)^2\right]. \tag{2.10}$$

The array pitch at the input and output of the Fourier plane is assumed to be equal, which is usually a valid assumption. $\Delta\phi$ is the phase difference between adjacent

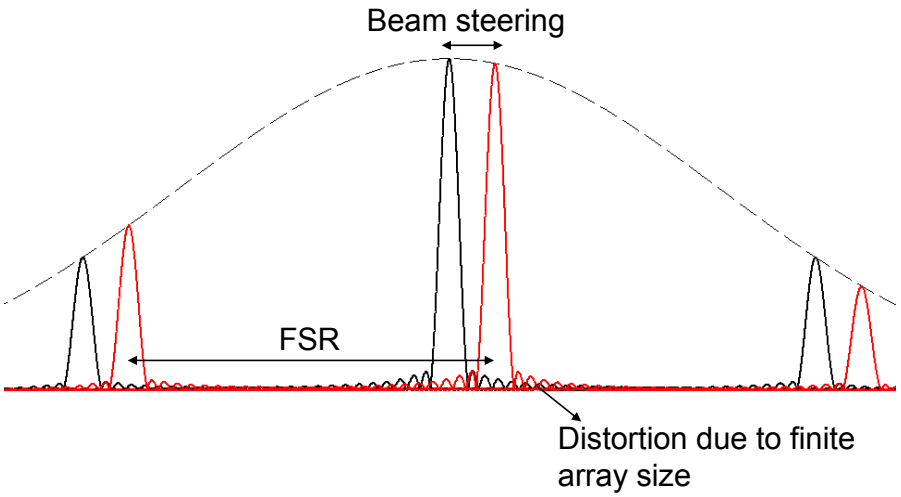


Fig. 2.4 Field distribution at the output of the second star coupler. The red and black curves correspond to two different values of phase slope.

waveguides in the array. The field at the output plane is calculated by applying Fraunhofer diffraction approximation once more to include the effects of the output star coupler. The resultant field distribution at the output plane is expressed by the equation

$$f_3(x_3) = C\left\{\begin{array}{l}\left[exp\left(\frac{-x_3^{\,2}}{w_0^{\,2}}\cdot\frac{\alpha_1^{\,2}}{\alpha_2^{\,2}}\right)\right] * \left[sinc\left(\frac{x_3(M-1)\cdot d_a}{\alpha_2}\right)\right] * \\ \delta\left(\frac{x_3}{\alpha_2}-\frac{\Delta\phi}{2\pi.d_a}\right) * \left[\sum_{i=-\infty}^{\infty}\delta\left(\frac{x_3}{\alpha_2}-\frac{i}{d_a}\right)\right]\end{array}\right\} \cdot exp\left(\frac{-\pi^2 x_3^{\,2} w_2^{\,2}}{\alpha_2^{\,2}}\right). \qquad (2.11)$$

The first function inside the brackets is the Fourier transform of the broad envelope function in the Fourier plane. One can see that the width of this function can be engineered through α_1 and α_2, which depend on the star coupler and waveguide dimensions as presented by (2.3). The sinc function is the Fourier transform of the rectangle function and as expected, it causes an undesired distortion in the signal. The delta function is responsible for the switching since convolution with a delta function causes a shift. The linear relationship between the phase slope and the position of beam at the output is apparent. The delta train corresponds to the infinite number of diffraction modes. In principle, coupling to only the fundamental mode is desired since the higher order diffraction modes contribute to coupling loss. The distance between these modes, α_2 / d_a , is referred as the free spectral range (FSR) and is an important

design parameter. The exponential on the right side is the Fourier transform of the arrayed waveguide mode, and determines the distribution of optical power among the fundamental and higher order modes at the output. As an example, Fig. 2.4 plots the function in (2.11) for two different values of phase difference between adjacent arrayed waveguides. This analytical derivation is the basis of design considerations explained in the next section.

2.5 DESIGN CONSIDERATIONS OF PHASED-ARRAY SWITCHES

Among the several basic characteristics of optical switches explained in Section 1.3.1, the ones that can be controlled through the layout design are the extinction ratio, insertion loss, output power uniformity and footprint. The design parameters which are the most effective on the switch characteristics are the width of waveguides at the intersections with the star couplers, the length of star couplers, the number of arrayed waveguides, array pitch and the output pitch.

The effective length of star couplers is inversely proportional to the width of the optical mode in the waveguide according to diffraction theory, which states that narrower beams are diffracted in a shorter distance than wide ones. The mode size depends on the waveguide width and the refractive index contrast between the core and

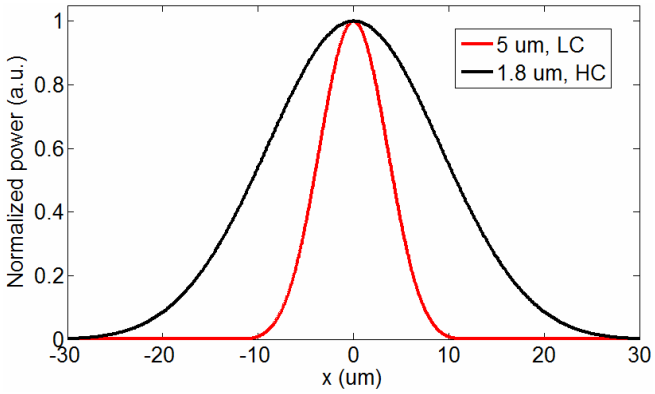


Fig. 2.5 Diffracted optical power at the output of a star coupler with a 1.8-µm-wide high-confinement (HC) and a 5-µm-wide low-confinement (LC) input waveguide.

the cladding. High-index-contrast waveguides are capable of confining the optical modes into tighter dimensions, so they can operate with shorter star couplers, which reduces the footprint. Fig. 2.5 compares the optical power distribution at the output of a star coupler for a tightly confined and a loosely confined input waveguide. The loosely confined waveguide leads to a narrower diffracted function because of the shorter effective length of the star coupler. Furthermore, the crosstalk between adjacent output waveguides is lower with high-index-contrast waveguides if the output pitch is the same in both cases. Therefore, narrow waveguides with confinement as high as possible should be preferred at the inputs and outputs of the star couplers.

The designer would intuitively choose the output pitch as large as possible to suppress the crosstalk. Nevertheless, there is an upper limit defined by the FSR. If the waveguides in the output plane cover a total width larger than the FSR, multiple waveguides receive light beams from different diffraction modes. To avoid this, the maximum value of the output pitch should be

$$d_o\left(max\right)=\frac{FSR}{N}. \tag{2.12}$$

Therefore, a good design with low crosstalk aims at achieving a large FSR.

The array pitch affects the extinction ratio and the insertion loss by two different mechanisms. First, FSR is inversely proportional to the array pitch with the relation

$$FSR=\frac{\alpha_2}{d_a}. \tag{2.13}$$

As explained in the previous paragraph, large FSR values lead to lower crosstalk, i.e. higher extinction ratio. Thus, one thinks that keeping the array pitch as small as possible is one way of achieving high extinction ratio. However, for a fixed number of arrayed waveguides, smaller array pitch increases the distortion due to truncation, which reduces the extinction ratio. Using a large number of arrayed waveguides with a small pitch solves this problem, but it comes with the cost of increased power consumption due to the large number of phase shifters and increased complexity of operation. The optimal value of the array pitch has to be calculated according to the number of arrayed waveguides. An extinction ratio over 30 dB is theoretically achievable if the number of arrayed waveguides is approximately equal to 1.5 times the number of outputs.

The other design parameter is the length of the star couplers. The input and output star couplers do not necessarily have to be equal in length. The width of the output waveguides has to be designed according to the star coupler dimensions based on the relation,

$$w_o = w_i \cdot \frac{\alpha_2}{\alpha_1}, \tag{2.14}$$

where w_i and w_o are the input and output mode sizes respectively. Note that the broadening caused by distortion (convolution with sinc function in (2.11)) also has to be considered in addition to (2.14). Since the smallest footprint is obtained with input and output waveguide modes as narrow as possible, usually w_i and w_o are designed to be

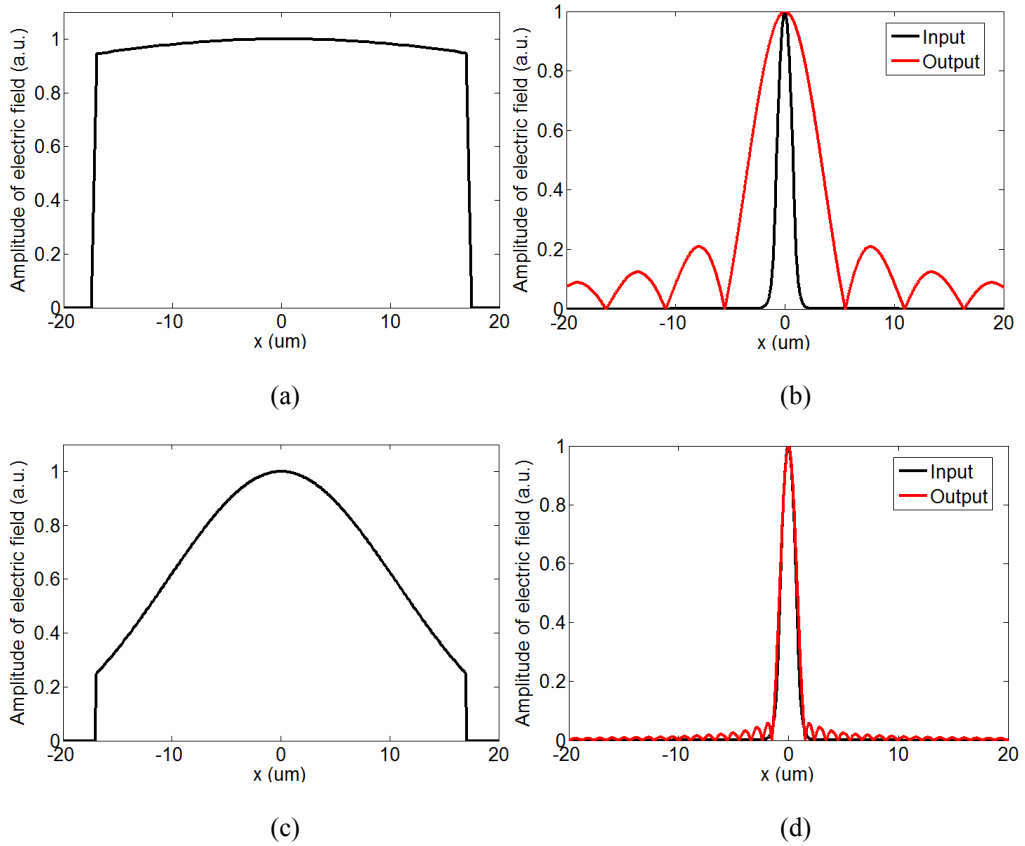
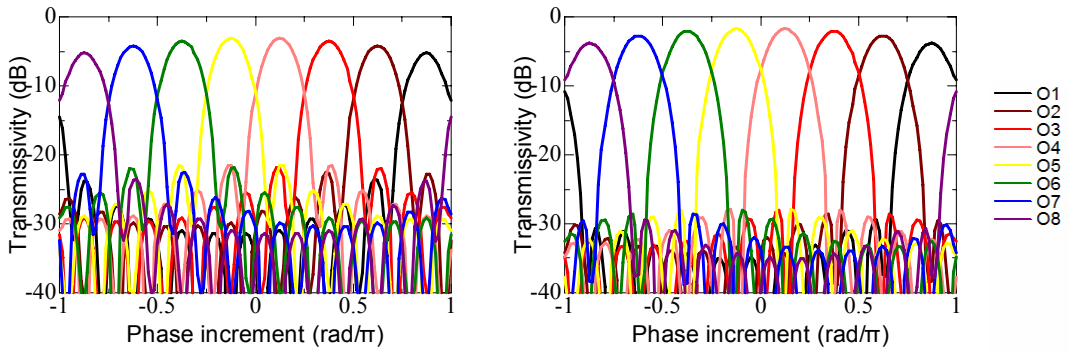


Fig. 2.6 Output mode distributions of the first star coupler (a) in a switch with very long star couplers and (c) in a switch with 5 times shorter star couplers; the comparison of input and output (fundamental) modes of the switch (b) with very long star couplers and (d) with 5 times shorter star couplers. The mode broadening and large side lobes in (b) are caused by the truncation and results in a large crosstalk.

equal to each other, which means that the input and output star couplers are equal in length. Similar to the case for array pitch selection, there is a dilemma while chosing the length of star couplers. The star couplers have to be long enough for a large FSR, but short enough to mitigate the distortion of the optical mode. The output mode is broadened and distorted because of the truncation at the output of the first star coupler. This phenomenon is displayed in Fig. 2.6 with a comparison between a highly distorted mode (a, b) and a less distorted mode (c, d). Because of the shorter star couplers, the mode at the output of the first star coupler is much narrower in (c), which suppresses the effect of truncation. As a result, the output mode shape has a much better matching with the input mode in (d) than in (b). Moreover, the loss in the first star coupler is higher in case of Fig. 2.6-a because a larger portion of the mode is outside the array. The effect of star coupler length on switching performance is shown in Fig. 2.7. The transmittance of optical power to the outputs of two 1×8 switches is shown with respect to the phase increment. As explained before, most of the light is deflected to one output at certain phase increment values. The switch in (b), which has an approximately optimal star coupler length, has considerably better extinction ratio and insertion loss values than the switch in (a), whose star couplers are too long.



(a) (b)

Fig. 2.7 Comparison of 1×8 switching with two different designs. (a) Too long star couplers (150 μm in this example) lead to high insertion loss and high crosstalk because of large modal distortion. (b) The switch with a star coupler length of 105 μm exhibits a better insertion loss and extinction ratio. Both switches incorporate 12 arrayed waveguides. O1 – O8: Output 1 – Output 8.

There is also a trade-off between the uniformity among output ports and insertion loss. The insertion loss in central ports can be mitigated by designing the full-width-at half-maximum (FWHM) of the output envelope small, so that higher-order modes receive very small power. However, this leads to a large power nonuniformity causing high insertion loss in the outputs at the edges. Again, an optimal value has to be found.

To sum up, the star coupler length, array and output pitches, and the number of arrayed waveguides are not independent parameters and their values have to be optimized depending on the design priorities. In other words, optimal values of these parameters vary depending on whether the insertion loss, extinction ratio, footprint, uniformity or power consumption are preferred to be optimized. The readers are encouraged to grasp the theory explained above instead of following a recipe. Two case studies, one leading to a moderate compromise of all device characteristics and the other aimed at a small footprint and low power consumption, are described in Chapter 3 and Chapter 5.

2.6 COMPARISON WITH OTHER SWITCH TECHNOLOGIES

In this section, phased-array switches are compared to other transparent and WDM-compatible optical switch types. Amplitude transparent or opaque switches and single-wavelength devices are not covered in this comparison. Switch types with slow dynamic response are also not included in the comparison because they do not offer any solutions for OPS.

High-speed strictly transparent optical switches besides phased-array switches can be classified as broadcast-and-select semiconductor optical amplifier (SOA) gate array switches and small-scale (1×2 or 2×2) switches. There are several different types of small-scale switches including Mach-Zehnder interferometer (MZI) switches [19], directional coupler switches [20], digital optical switches [21], transverse index compensation switches [22], and total internal reflection switches [23]. However, it is meaningful to evaluate them together because a large number of these switches have to

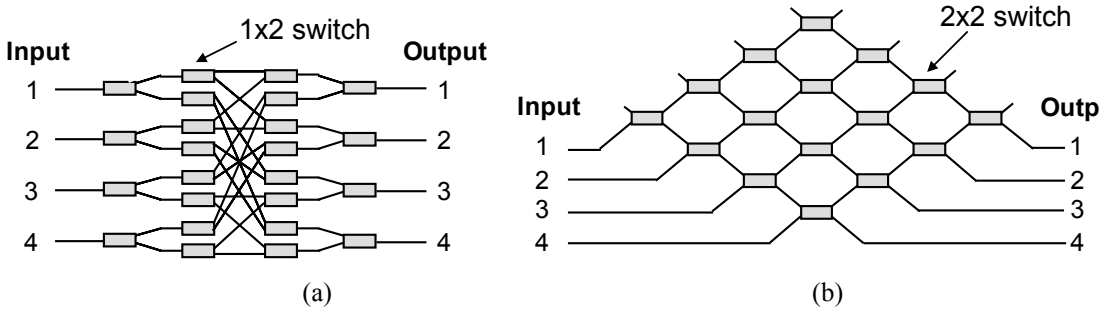
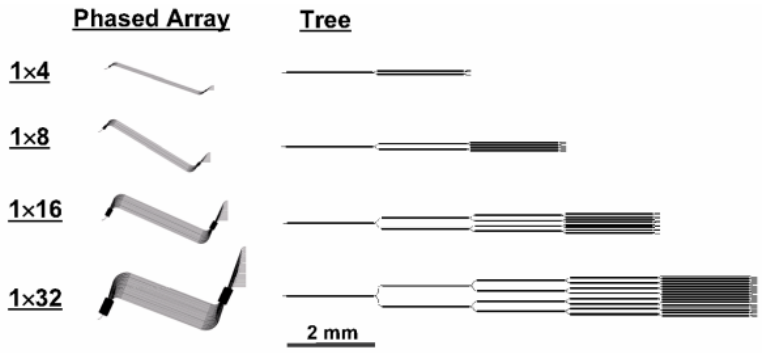


Fig. 2.8 (a) A *4×4* Spanke switch consisting of multiple *1×4* tree switches and (b) a *4×4* crossbar switch.

be cascaded to construct switch matrices with large number of ports, which is usually the limiting factor irrespective of the switching technology. On the contrary, broadcast-and-select switches can have a relatively large number of ports in a single stage as an alternative to phased-array switches.

The first comparison is with small-scale switches on the footprint and signal quality. Among various architectures of multi-switch fabrics, Spanke and crossbar are more suitable for asynchronous packets because they are strict-sense and wide-sense nonblocking respectively [24,25]. An $N\times N$ Spanke switch consists of $1\times N$ switches, which can be constructed by 1×2 switches in the tree architecture as shown schematically in Fig. 2.8-a. The tree architecture has superior scalability than the crossbar architecture, displayed in Fig. 2.8-b, because the number of switches on the light path increases logarithmically with the output port count in contrast with the linear increase in the crossbar switch. Therefore, phased-array switches are compared with $1\times N$ tree switches here.

The number of switching stages on the light path is important in terms of not only footprint, but also the signal quality because there is unavoidable optical loss, crosstalk and additional noise in every stage. Moreover, the propagation loss in addition to the switch loss is also proportional to the number of stages. In a $1\times N$ tree, this parameter is equal to log_2N, whereas the number of switching stages in a phased-array switch is equal to 1 independent of N. The 1×2 switches listed above are typically millimeters long on the InP platform. Fig. 2.9 displays a comparison of phased-array switches with a switch based on the tree architecture. In this comparison, the physical size of the 1×2



(a) (b)

Fig. 2.9 Comparison of phased-array and tree switches with an assumption of 2-mm-long phase shifters (after [26]).

switches is underestimated [26]. These switches are assumed to have a length equal to a phase shifter, which is longer in reality. Even under these conditions, the advantage of phased array architecture in terms of optical path length and footprint are apparent. Note that this comparison is done under the assumption of conventional InP ridge waveguides. The advantage of phased-array switching increases further if higher-index-contrast waveguides with smaller bending radii are employed [27]. In summary, phased-array switches that have tens of output ports are expected to have less reduction of signal quality due to switching elements, lower optical propagation loss, shorter optical path length, and smaller footprint than tree switches that have equal number of output ports.

The other potential candidate for OPS is the broadcast-and-select SOA gate array switch shown in Fig. 2.10. The switching mechanism is based on splitting the input signal into multiple arms, each equipped with an SOA. The SOAs located on the light path of a connection are forward biased to obtain optical gain. Since an unbiased SOA is

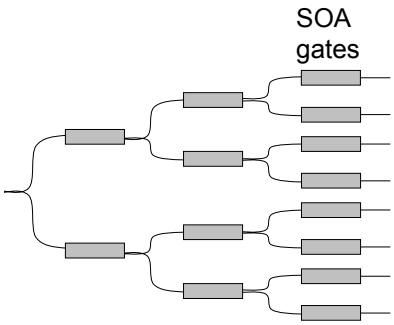
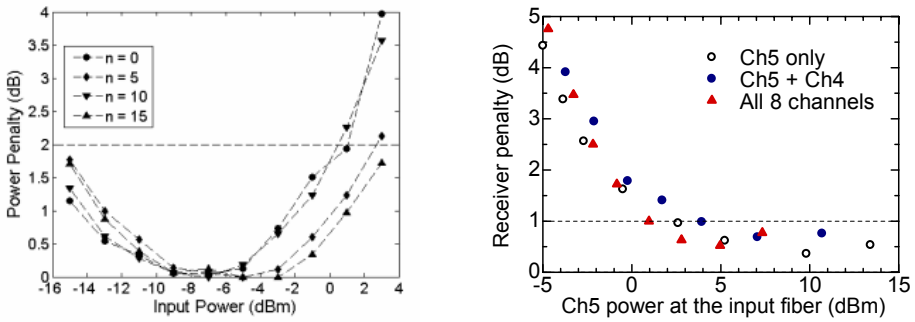


Fig. 2.10 Three-stage distributed broadcast-and-select SOA gate array switch.

absorptive, the optical power in the other arms is dissipated. Broadcast-and-select switches can comprise multiple stages of SOA gates following small-scale splitters as in Fig. 2.10 (distributed architecture), or a single-stage of SOA gates following a $1\times N$ splitter (lumped architecture). The preference depends on the number of outputs, but distributed switches have a better scalability than lumped switches due to less accumulation of amplified spontaneous emission (ASE) noise [28]. The advantages of broadcast-and-select switch are the high extinction ratio, small footprint compared to the switches based on tree architecture, and low complexity of control. Broadcast-and-select switches have been employed in OPS demonstrations because of these advantages [29,30]. Although these switches can be lossless owing to the SOAs on the light path, the loss in the passive section puts an upper limit on the scalability because regeneration is necessary after a certain number of amplification steps. The losses in the phased-array switch and the passive section of the broadcast-and-select switch have to be estimated to compare their scalability. Theoretically, the $1\times N$ passive coupling loss is equal to $(3dB)\times(\log_2 N)$. For example, the passive components of an ideal 1×64 broadcast-and-select switch have a loss of 18 dB, whereas the experimental loss is higher due to coupling and propagation loss along with nonidealities. According to the calculations described in Section 2.4, the theoretical loss of phased-array switches increases very slowly with the number of outputs as long as the number of phase shifters is 1.6 times the number of outputs. A quantitative comparison of optical loss in phased-array and broadcast-and-select switches is added in Chapter 6. As that analysis shows, phased-array switches have an advantage of lower optical loss than broadcast-and-select switches, which leads to a dramatically lower power consumption and reduced effects of ASE.

Gain saturation of SOAs is another problem that broadcast-and-select switches suffer from. If multi-channel WDM signals are amplified with an SOA in the saturated regime, nonlinear crosstalk occurs between different wavelength channels [31]. This phenomenon is observed with SOAs, but not erbium-doped fiber amplifiers (EDFA) because the gain dynamics of SOAs are fast enough to follow the bit pattern. This causes an additional power penalty in case of high input power as shown in Fig. 2.11-a [32]. High-saturation-power or gain-clamped SOAs are proposed as a solution, but they



(a) (b)

Fig. 2.11 (a) Single-channel power penalty vs. input power in a small-scale broadcast-and-select switch (after [32]), and (b) 8-channel power penalty vs. input power in a phased-array switch (after [34]).

come at the cost of power consumption and do not solve the problem completely [33]. In case of phased-array switches, this problem can be avoided completely by using EDFAs instead of SOAs to compensate for the losses. In that case, no residual power penalty caused by gain saturation is observed as displayed in Fig. 2.11-b [34]. Even if SOAs are employed to compensate for the losses of phased-array switches, the effect of gain saturation is theoretically less severe than broadcast-and-select switches because of the lower gain necessary for equal number of ports.

2.7 AMPLITUDE-CONTROLLED PHASED-ARRAY SWITCHES FOR MULTICASTING

The phased-array switches explained so far are capable of forming one connection at a time. In other words, they cannot switch to multiple ports simultaneously. Switching to multiple channels, which is referred as multicasting, is desirable in communication networks for applications including video-conferencing, high-definition video distribution, interactive distance learning, and distributed games [35-37]. Phased-array switches can attain the functionality of multicasting with a modification of design. If we add amplitude controllers to the phase controllers in the array plane of phased-array switches, the optical mode distribution at the output plane can be engineered with a high

degree of freedom as explained below.

The mode profile at the output plane of single-port switching phased-array switches is given by (2.11). Multicasting is equivalent to modifying this equation into the following form.

$$f_3(x_3) = C\left\{\begin{array}{l}\left[exp\left(\frac{-x_3^{\,2}}{w_0^{\,2}}\cdot\frac{\alpha_1^{\,2}}{\alpha_2^{\,2}}\right)\right] * \left[sinc\left(\frac{x_3(M-1)\cdot d_a}{\alpha_2}\right)\right] * \\ \left[\delta\left(\frac{x_3}{\alpha_2}-\frac{\Delta\phi_1}{2\pi.d_a}\right)+\delta\left(\frac{x_3}{\alpha_2}-\frac{\Delta\phi_2}{2\pi.d_a}\right)+\ldots+\delta\left(\frac{x_3}{\alpha_2}-\frac{\Delta\phi_M}{2\pi.d_a}\right)\right] * \\ \left[\sum_{i=-\infty}^{\infty}\delta\left(\frac{x_3}{\alpha_2}-\frac{i}{d_a}\right)\right]\end{array}\right\}\cdot exp\left(\frac{-\pi^2 x_3^{\,2} w_2^{\,2}}{\alpha_2^{\,2}}\right),$$

(2.15)

where the light is deflected to M different points simultaneously. The single delta function in (2.11) is replaced by a sum of M delta functions. The amplitude and phase of the optical field distribution in the array plane is found by deriving the inverse Fourier transform of (2.15).

$$f_{\,2}(x_2) = C\left\{\begin{array}{l}exp\left[-\left(\frac{\pi w_0 x_1}{\alpha_1}\right)^2\right]\cdot \\ \left[exp\left(\frac{jx_2\Delta\varphi_1}{d_a}\right)+exp\left(\frac{jx_2\Delta\varphi_2}{d_a}\right)+\ldots+exp\left(\frac{jx_2\Delta\varphi_M}{d_a}\right)\right]\cdot \\ rect\left(\frac{x_1}{(M-1)\cdot d_a}\right)\cdot\sum_{i=-\infty}^{\infty}\delta(x_1 - d_a\cdot i)\end{array}\right\} * exp\left[-(x_1/w_2)^2\right],$$

(2.16)

which is identical to (2.10) except the sum of complex exponentials instead of a single complex exponential in the middle term in brackets. The single complex exponential in (2.10) represents the linear phase distribution in the array plane, so it is the perturbation due to phase shifters. Replacing that term with a sum of complex exponentials is equivalent to perturbing not only phase, but also amplitude distribution in Fourier plane. This can be implemented by attaching amplitude controlling devices, i.e. SOAs or variable optical attenuators (VOA) in the array plane as visualized in Fig. 2.12. This

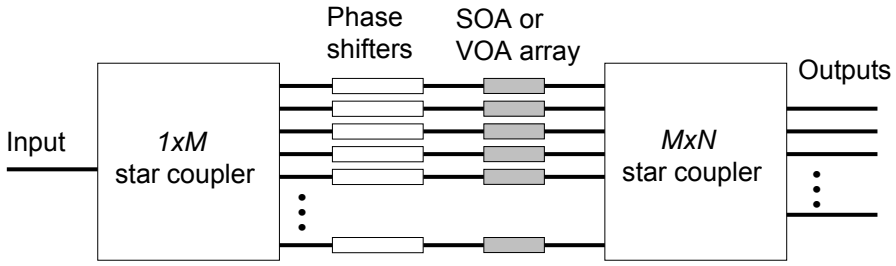


Fig. 2.12 Schematic diagram of the amplitude-controlled phased-array switch.

device can be referred as an amplitude-controlled phased-array switch. Next, the amplitude and phase distribution in the array plane is derived.

According to (2.16), the amplitude and phase distribution in Fourier plane is derived by calculating the sum of complex exponentials with arbitrary phase values.

$$f\left(x_2\right) = exp\left(\frac{jx_2\Delta\varphi_1}{d_a}\right) + exp\left(\frac{jx_2\Delta\varphi_2}{d_a}\right) + \ldots + exp\left(\frac{jx_2\Delta\varphi_M}{d_a}\right). \tag{2.17}$$

(2.17) is the master equation that can be applied for switching to an arbitrary number of ports simultaneously. Let us investigate the case of switching to two ports as an example. In this case, (2.17) becomes

$$f\left(x_2\right) = cos\left(\frac{x_2\Delta\varphi_1}{d_a}\right) + cos\left(\frac{x_2\Delta\varphi_2}{d_a}\right) + j\left[sin\left(\frac{x_2\Delta\varphi_1}{d_a}\right) + sin\left(\frac{x_2\Delta\varphi_2}{d_a}\right)\right]. \tag{2.18}$$

The amplitude (squared) and phase of this function are expressed as

$$\left|f\left(x_2\right)\right|^2 = \left[cos\left(\frac{x_2\Delta\varphi_1}{d_a}\right) + cos\left(\frac{x_2\Delta\varphi_2}{d_a}\right)\right]^2 + \left[sin\left(\frac{x_2\Delta\varphi_1}{d_a}\right) + sin\left(\frac{x_2\Delta\varphi_2}{d_a}\right)\right]^2, \tag{2.19}$$

$$\angle f\left(x_2\right) = tan^{-1}\left[\frac{sin\left(\frac{x_2\Delta\varphi_1}{d_a}\right) + sin\left(\frac{x_2\Delta\varphi_2}{d_a}\right)}{cos\left(\frac{x_2\Delta\varphi_1}{d_a}\right) + cos\left(\frac{x_2\Delta\varphi_2}{d_a}\right)}\right], \tag{2.20}$$

After a straightforward trigonometric derivation, these equations are simplified to

$$\left|f\left(x_2\right)\right|^2 = 2\left[1 + cos\left(\frac{x_2\left(\Delta\varphi_1 - \Delta\varphi_2\right)}{d_a}\right)\right], \text{ and} \tag{2.21}$$

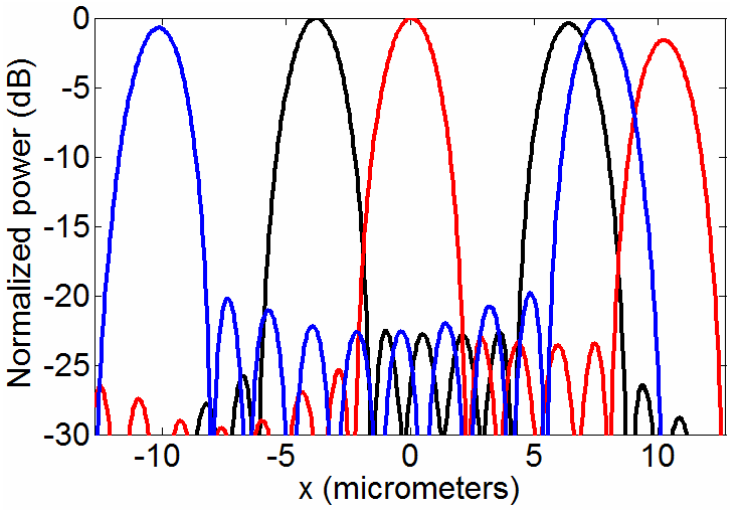


Fig. 2.13 Normalized power distribution at the output plane under different amplitude and phase conditions of two-port switching. The phase increment values of the exponentials in (2.17) are as follows. Black: 0.5π, -0.3π; red: 0.8π, 0; blue: 0.6π, -0.8π.

$$\angle f\left(x_2\right)=\frac{x_2\left(\Delta\varphi_1+\Delta\varphi_2\right)}{2d_a}. \tag{2.22}$$

According to (2.22), two-port switching is implemented by a linear phase shift similar to the single-port switching condition. However, the power distribution has to be arranged sinusiodally. Fig. 2.13 demonstrates two-port switching examples with different position pairs at the output. This graph verifies that multiple switching points can be freely selected through the conditions of the phase shifters and SOAs. These calculations were carried out under the assumption of a switch with 14 arrayed waveguides. Simultaneous switching to four different points is shown in Fig. 2.14 to prove that the number of simultaneous switching ports can be increased arbitrarily without crosstalk penalty.

2.8 CONCLUSION

According to the overview of optical phased arrays in Section 2.2, AWG is the most commercially successful optical phased-array device. Although the first phased-array switch was demonstrated approximately at the same time as the AWG, this technology has not been investigated thoroughly so far. As a consequence, completely integrated phased-array switches satisfying the stringent requirements of OPS were not available

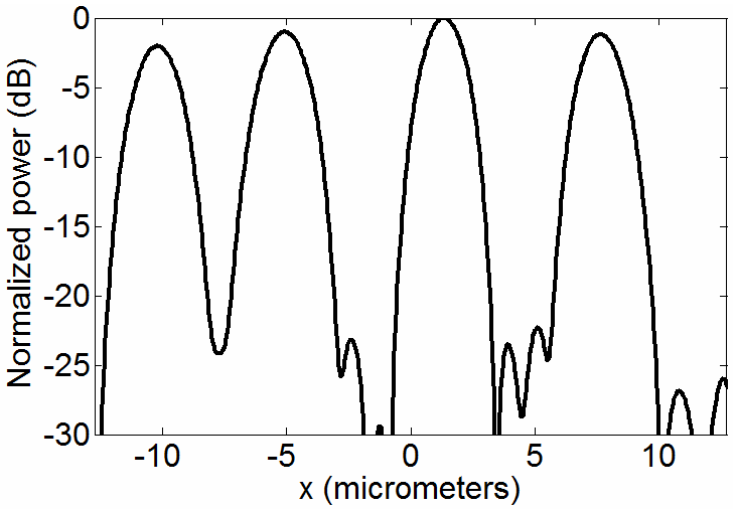


Fig. 2.14 Normalized power distribution at the output plane under the condition of four-port switching. The phase increment values of the exponentials in (2.17) are: -0.8π, -0.4π, 0.1π, and 0.6π.

until the integrated InP switches studied in this thesis.

The principle of operation of phased-array switches has been explained analytically. This analytical derivation has been used to introduce the design considerations. The design of phased-array switches does not have a straightforward recipe since there is a trade-off among basic characteristics including the insertion loss, extinction ratio, power consumption, and uniformity of power. The relation between the design parameters and these characteristics has been described.

Next, a comparison has been done with other promising strictly transparent multi-wavelength optical switching technologies. Phased-array switches theoretically offer shorter optical path length, smaller footprint, and lower loss than tree architectures consisting of 1×2 switches. Moreover, phased-array switches suffer less from the ASE noise and gain saturation of SOAs compared to broadcast-and-select SOA gate array switches. As a result, they offer a higher potential of scalability and cascadability without regeneration.

Finally, amplitude-controlled phased-array switches have been introduced as devices capable of engineering the distribution of optical signal at the output plane with a higher degree of freedom compared to phased-array switches. These switches can theoretically switch to arbitrary combinations of output ports simultaneously. This

functionality, referred as multicasting, is very desirable in optical switching. Theoretically, amplitude-controlled phased-array switches can achieve multicasting with extinction ratio comparable to that of singlecasting.

REFERENCES OF CHAPTER 2

[1] W. H. Wee and J. B. Pendry, “Super phase array,” New Journal of Physics, vol. 12, p. 033047, Mar. 2010.

[2] F. G. Kear, “Maintaining the directivity of antenna arrays,” Proc.Institute of Radio Engineers, vol. 22, no. 7, pp. 847-869, Jul. 1934.

[3] R. A. Meyer, “Optical beam steering using a multichannel lithium tantalate crystal,” Applied Optics, vol. 11, no. 3, pp. 613-616, Mar. 1972.

[4] H. Sasaki and R. M. De La Rue, “Electro-optic multichannel waveguide deflector,” Electronics Letters, vol. 13, no. 10, pp. 295-296.

[5] D. R. Wight, J. M. Heaton, B. T. Hughes, J. C. H. Birbeck, K. P. Hilton, and D. J. Taylor, “Novel phased array optical scanning device implemented using GaAs/AlGaAs technology,” Applied Physics Letters, vol. 59, no. 8, pp. 899-902, Aug. 1991.

[6] M. K. Smit, “New focusing and dispersive planar component based on an optical phased array,” Electronics Letters, vol. 24, no. 7, pp. 385-386, Mar. 1988.

[7] C. Dragone, C. A. Edwards, and R. C. Kistler, “Integrated optics N × N multiplexer on silicon,” IEEE Photonics Technology Letters, vol. 3, no. 10, pp. 896-899, Oct. 1991.

[8] Y. Tachikawa, Y. Inoue, M. Kawachi, H. Takahashi, and K. Inoue, “Arrayed-waveguide grating add-drop multiplexer with loop-back optical paths,” Electronics Letters, vol. 29, no. 24, pp. 2133-2134, Nov. 1993.

[9] M. K. Smit and C. van Dam, “PHASAR-based WDM devices: principles, design and applications,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 2, no. 2, pp. 236-250, Jun. 1996.

[10] Y. Hibino, “Recent advances in high-density and large-scale AWG multi/demultiplexers with higher index-contrast silica-based PLCs,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 8, no. 6, pp. 1090-1101, Nov./Dec. 2002.

[11] J. M. Heaton, D. R. Wight, J. T. Parker, B. T. Hughes, J. C. H. Birbeck, and K. P. Hilton, “A phased array optical scanning (PHAROS) device used as a 1-to-9 way switch,” IEEE Journal of Quantum Electronics, vol. 28, no. 3, pp. 678-685, Mar. 1992.

[12] E. Fluck, F. Horst, B. J. Offrein, R. Germann, H. W. M. Salemink, and G.-L Bona, “Compact versatile thermooptical space switch based on beam steering by a waveguide array,” IEEE Photonics Technology Letters, vol. 11, no. 11, pp. 1399-1401, Nov. 1999.

[13] K. Suzuki, T. Yamada, M. Ishii, T. Shibata, and S. Mino, “High-speed optical 1×4 switch based on generalized Mach-Zehnder interferometer with hybrid configuration of silica-based PLC and lithium niobate phase-shifter array,” IEEE Photonics Technology Letters, vol. 19, no. 9, pp. 674-676, May 2007.

[14] E. Shekel, A. Feingold, Z. Fradkin, A. Geron, J. Levy, G. Matmon, D. Majer, A. Rafaely, M. Rudman, G. Tidhar, J. Vecht, and S. Ruschin, “64×64 fast optical switching module,” in Proc. Optical Fiber Communication Conference, 2002, Paper TuF3.

[15] R. M. Jenkins, J. M. Heaton, D. R. Wight, J. T. Parker, J. C. H. Birbeck, G. W. Smith, and K. P. Hilton, "Novel 1×N and N×N integrated optical switches using self-imaging multimode GaAs/AlGaAs waveguides," Applied Physics Letters, vol. 64, no. 6, pp. 684-686, Feb. 1994.

[16] T. Tanemura, M. Takenaka, A. Al Amin, K. Takeda, T. Shioda, M. Sugiyama, and Y. Nakano, "InP-InGaAsP integrated 1×5 optical switch using arrayed phase shifters," IEEE Photonics Technology Letters, vol. 20, no. 12, pp. 1063-1065, Jun. 2008.

[17] C. Dragone, C. H. Henry, I. P. Kaminow, and R. C. Kistler, "Efficient multichannel integrated optics star coupler on silicon," IEEE Photonics Technology Letters, vol. 1, no. 8, pp. 241-243, Aug. 1989.

[18] M. Munoz, D. Pastor, and J. Capmany, "Modeling and design of arrayed waveguide gratings," Journal of Lightwave Technology, vol. 20, no. 4, pp. 661-674, Apr. 2002.

[19] N. Agrawal, C. M. Weinert, H.-J. Ehrke, G. G. Mekonnen, D. Franke, C. Bornholdt, and R. Langenhorst, "Fast 2×2 Mach-Zehnder optical space switches using InGaAsP-InP multiquantum-well structures," IEEE Photonics Technology Letters, vol. 7, no. 6, pp. 644-645, Jun. 1995.

[20] T. Aizawa, Y. Nagasawa, K. G. Ravikumar, and T. Watanabe, "Polarization-independent switching operation in directional coupler using tensile-strained multi-quantum well," IEEE Photonics Technology Letters, vol. 7, no. 1, pp. 47-49, Jan. 1995.

[21] H. Yanagawa, K. Ueki, and Y. Kamata, "Polarization- and wavelength-insensitive guided-wave optical switch with semiconductor Y-junction," Journal of Lightwave Technology, vol. 8, no. 8, pp. 1192-1197, Aug. 1990.

[22] B. Acklin, M. Schienle, B. Weiss, L. Stoll, and G. Muller, "Novel optical switches based on carrier injection in three and five waveguide couplers: TIC and SIC," Electronics Letters, vol. 30, no. 3, pp. 217-218, Feb. 1994.

[23] H. Inoue, T. Kirihara, Y. Sasaki, and K. Ishida, "Carrier-injection type optical S^3 switch with traveling-wave amplifier," IEEE Photonics Technology Letters, vol. 2, no. 3, pp. 214-215, Mar. 1990.

[24] R. A. Spanke, "Architectures for guided-wave optical space switching systems," IEEE Communications Magazine, vol. 25, no. 5, pp. 42-48, May 1987.

[25] G. I. Papadimitriou, C. Papazoglou, and A. S. Pomportsis, "Optical switching: switch fabrics, techniques, and architectures," Journal of Lightwave Technology, vol. 21, no. 2, pp. 384-405, Feb. 2003.

[26] T. Takenaka and Y. Nakano, "Design and scalability analysis of optical phased-array 1×N switch on planar lightwave circuit," IEICE Electronics Express, vol. 5, no. 16, pp. 603-609, Aug. 2008.

[27] M. Takenaka, M. Yokoyama, M. Sugiyama, Y. Nakano, and S. Takagi, "InGaAsP photonic wire based ultrsmall arrayed waveguide grating multiplexer on Si wafer," Applied Physics Express, vol. 2, 122201, Nov. 2009.

[28] R. F. Kalman, L. G. Kazovsky, and J. W. Goodman, "Space division switches based on semiconductor optical amplifiers," IEEE Photon. Technol. Lett., vol. 4, no. 9, pp. 1048-1051, Sep. 1992.

[29] Y. Kai, K. Sone, S. Yoshida, Y. Aoki, G. Nakagawa, and S. Kinoshita, "A compact and lossless 8×8 SOA gate switch subsystem for WDM optical packet interconnections," in Proc. European Conference on

Optical Communication, 2008, Paper We.2.D.4.
[30] R. Hemenway, R. Grzybowski, C. Minkenberg, and R. Luijten, “Optical-packet-switched interconnect for supercomputer applications,” Journal of Optical Networking, vol. 3, no. 12, pp. 900-913, Dec. 2004.
[31] M. G. Oberg and N. A. Olsson, “Crosstalk between intensity-modulated wavelength-division multiplexed signals in a semiconductor laser amplifier,” IEEE Journal of Quantum Electronics, vol. QE-24, no. 1, pp. 52-59, Jan. 1988.
[32] J. P. Mack, H. N. Poulsen, and D. J. Blumenthal, “40 Gb/s autonomous optical packet synchronizer,” in Proc. Optical Fiber Communication Conference, 2008, OTuD3.
[33] D. Wolfson, S. L. Danielsen, C. Joergensen, B. Mikkelsen, and K. A. Stubkjaer, “Detailed theoretical investigation of the input power dynamic range for gain-clamped semiconductor optical amplifier gates at 10 Gb/s,” IEEE Photonics Technology Letters, vol. 10, no. 9, pp. 1241-1243, Sep. 1998.
[34] T. Tanemura, K. Takeda, and Y. Nakano, “Wavelength-multiplexed optical packet switching using InP phased-array switch,” Optics Express, vol. 17, no. 11, pp. 9454-9459, May 2009.
[35] Y. Wang, C. Yu, T. Luo, L. Yan, Z. Pan, and A. E. Willner, “Tunable all-optical wavelength conversion and wavelength multicasting using orthogonally polarized fiber FWM,” Journal of Lightwave Technology, vol. 23, no. 10, pp. 3331-3338.
[36] K. Lau, S. H. Wang, L. Xu, C. Lu, H. Y. Tam, and P. K. A. Wai, “All-optical multicast switch employing Raman-assisted FWM in dispersion-shifted fiber,” IEEE Photonics Technology Letters, vol. 20, no. 10, pp. 1730-1732, Oct. 2008.
[37] N. K. Singhal and B. Mukherjee, “Protecting multicast sessions in WDM optical mesh networks,” Journal of Lightwave Technology, vol. 21, no. 4, pp. 884-892, Apr. 2003.

CHAPTER 3
INTEGRATED *1×N* PHASED-ARRAY PHOTONIC SWITCHES: DESIGN, FABRICATION AND CHARACTERIZATION

3.1 INTRODUCTION

The theoretical characteristics of phased-array switches explained in Chapter 2 are very promising, but they are not conclusive without experimental verification because it is well known that optoelectronic devices deviate from ideal conditions. Two sets of monolithically integrated switches are designed, fabricated, and tested for this purpose. The first device is a 1×8 switch with low polarization sensitivity and the second device is a low-loss 1×16 switch. Polarization sensitivity is an important property of optical switches for two reasons. The polarization state of light is not preserved in ordinary single-mode fibers, so polarization-sensitive optical devices require precise polarization control, which increases the cost and complexity. Moreover, polarization-sensitive optical devices are not transparent to polarization-division multiplexed (PDM) signals, which have recently been employed to double the spectral efficiency [1]. The 1×8 switch presented in this chapter is experimentally investigated in terms of the extinction ratio, insertion loss, wavelength sensitivity, and dynamic response in addition to polarization sensitivity. Later in the same chapter, a 1×16 optical switch is investigated in order to understand the relationship between basic device properties and the number of ports, and solve the problems observed in the 1×8 switch, especially the insertion loss. Both switches are designed for very broad spectral operation band for compatibility

with high-bit-rate data. This chapter presents examples of phased-array switch design, describes the fabrication of passive InP integrated photonic devices, explains their characterization techniques, presents the device characteristics and discusses the results.

Section 3.2 describes the efforts to implement a polarization-insensitive wide-bandwidth integrated 1×8 phased-array switch. This includes the epitaxial structure and layout design considerations, fabrication procedures, calibration and basic characterization of the switch. Discussion on the problems of this device and possible solutions are added at the end of this section. Section 3.3 focuses on a switch with double on-chip switching capability and significantly improved performance. Construction of a switch controller for dynamic control and the experiments on the complete dynamic operation of the switch are also presented here. Finally, Section 3.4 concludes the chapter.

3.2 INTEGRATED 1×8 PHOTONIC SWITCH WITH LOW POLARIZATION SENSITIVITY

3.2.1 Design of the Device

The targeted design specifications were an extinction ratio over 30 dB, an insertion loss below 3 dB, and a polarization dependent loss as low as possible. Low wavelength sensitivity was aimed in order to cover the C-band of optical communications (wavelength range of 1530-1565 nm). The device footprint was not the priority, so the design was implemented according to relatively low-loss shallowly etched ridge waveguides instead of deeply etched waveguides, which would lead to a smaller footprint.

3.2.1.1 Design of the Epitaxial Structure

The design of the epitaxial layers is the first step of photonic integrated circuit design because the layout design depends strongly on the epitaxial structure. An InP/InGaAsP p-i-n double heterojunction with a bulk intrinsic layer was selected as the epitaxial design of the entire device. The p-i-n double heterojunction maintains photon

confinement in the core layer, which is accompanied by carrier confinement under forward bias and electric field under reverse bias. The p- and n-doped layers are InP, whereas the undoped layer in the center is InGaAsP, which has a lower bandgap energy than InP [2]. If carriers are injected through the junction, the potential barrier caused by the bandgap difference confines the electrons and holes in the InGaAsP region. The core layer of a phase modulator can comprise a bulk structure or quantum confined structures such as quantum wells and quantum dots. Quantum-confined phase modulators typically have higher efficiencies than bulk devices because of the engineered density of states [3,4]. As a result, especially multiple-quantum well (MQW) stacks are frequently used in modulators. However, polarization insensitivity is much more difficult to achieve with MQW phase modulators than bulk ones because of the separation of the heavy and light holes in MQW and the selection rule [5]. Although polarization dependence of MQW devices can be mitigated by tensile strain [6], covering a broad spectral band is not easy. A bulk layer of InGaAsP was preferred in these experiments because the efficiency of phase shifters is not the priority.

The bandgap of the intrinsic InGaAsP layer has to be selected as a trade-off between the efficiency of phase shifters and the optical propagation loss. The optical loss of InGaAsP extends to energies below the bandgap energy, which is called Urbach tail or Urbach absorption [7]. This absorption reduces exponentially as the difference between bandgap and photon energies increases. On the other hand, the wavelength dependence of phase modulation efficiency is larger if the photon energy is close to the bandgap energy [8]. For a photon wavelength of 1.55 μm, the optical absorption in InGaAsP that has an emission wavelength of 1.3μm (Q1.3) is 0.02 dB/cm. Carrier-induced phase modulation of 1.55-μm-wavelength photons is still effective under these conditions. Therefore, Q1.3 was selected as the core layer. Undoped InP (u-InP) layers were inserted between the core and the doped layers to reduce the free carrier absorption. The thicknesses of layers were designed according to the calculations of optical mode distribution using the transfer matrix method (TMM) [9]. The core layer thickness was designed as 500 nm because it supports a single vertical mode and a high optical confinement of 77%. The p-doping level of InP was set as 5×10^{17} cm^{-3}. At this doping level, p-InP has a high absorption coefficient of 10 cm^{-1} [10]. The thickness of

TABLE 3.1

EPITAXIAL DESIGN OF THE INTEGRATED PHASED-ARRAY SWITCH

DEFINITION	Thickness (nm)	Doping (cm^{-3})
p-InGaAs	200	1×10^{19}
p-InP	750	5×10^{17}
u-InP	300	N/A
u-Q1.3 InGaAsP	500	N/A
u-InP	50	N/A
n-InP	250	5×10^{17}
n-InP	substrate	2×10^{18}

the u-InP layer above the core has to be sufficient to maintain a low propagation loss. According to our TMM calculations, the overlap of optical power with the p-InP layer is limited to 1.1% with a 300-nm-thick u-InP in between. The thickness of p-InP was designed to be 750 nm to reduce the overlap with the highly absorbing InGaAs contact layer to 1.5×10^{-4}. Highly p-doped InGaAs, which has a smaller bandgap energy than InP, was employed as the contact layer to obtain an Ohmic p-contact. Since the optical absorption in n-InP is significantly lower than the absorption in p-InP, the u-InP layer thickness below the core was designed as only 50 nm. To mitigate the absorption in highly n-doped substrate further, a 250-nm-thick n-InP layer with a doping rate of 5×10^{17} cm^{-3} was located above the substrate. The final epitaxial design is listed in Table 3.1.

3.2.1.2 Design of the Planar Layout

The layout of the switch was designed by using the effective index method, which simplifies the two-dimensional waveguide problems by solving the modes in the one-dimensional vertical waveguide and using effective indices of the vertical waveguides in the one-dimensional lateral waveguide [11]. The etching depth of ridge waveguides has to be known to estimate the effective index at the cladding. For this device, a single-step shallow etching until the top 50 nm of the core layer was decided to be used. This etching depth was chosen deliberately as a compromise between two

TABLE 3.2

EFFECTIVE INDEX AT THE CORE AND CLADDING OF WAVEGUIDES

	Core	Cladding
TE	3.299	3.246
TM	3.291	3.214

extreme cases of shallow etching with low loss and single mode and deep etching with small radii of curvature. The effective indices of TE- and TM-polarized light calculated under this condition are written in Table 3.2.

The number of phase shifters in the 1×8 switch was set to 14 to achieve a good extinction ratio. The waveguides were designed to be 2.5 μm wide in the bends and the intersections with the star couplers, 4 μm at the phase shifters, and 5 μm at the input and outputs of the device. These relatively wide multimode waveguides were preferred to reduce the propagation loss caused by sidewall roughness. Wide waveguides at the input and outputs reduce the fiber coupling loss owing to the better overlap with the fiber mode. The effects of multimode waveguides on the switching performance are discussed in Section 3.2.4. The design of the phased-array switch began with independent selection of some parameters because this is a problem of multiple variables and multiple solutions. In this particular case, the array pitch was used as the initial condition. The algorithm is as follows. First, the array pitch both at the input and output of the array was set as 3 μm. Next, the output pitch value was swept in the 3-4 μm range while the corresponding output star coupler length was calculated from the FSR. The input star coupler length was set as equal to the output star coupler length, in which case the undistorted output mode size is exactly equal to the input mode size. Using these parameters, the optical loss and crosstalk in the output plane were calculated. There is an optimal output pitch value to minimize the crosstalk. If the output pitch is too large, the star couplers have to be long, which increases the mode distortion due to truncation in the first star coupler. Therefore, both loss and crosstalk increase. In the other extreme, where the output pitch is too small, the crosstalk is large because of the large mode overlap between the adjacent ports. The optimal value of the output pitch was calculated as 3.2 μm in this case. The lengths of both star couplers

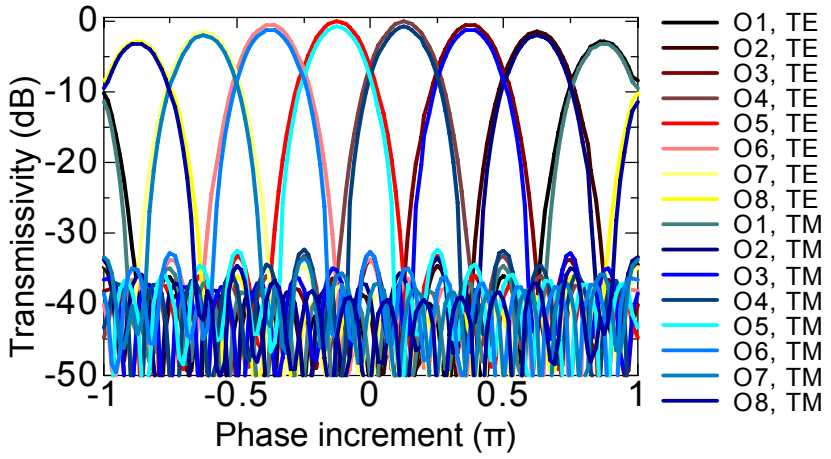


Fig. 3.1 Analytically calculated performance of the designed switch.

were 163 μm long. The calculated switching performance under these conditions is plotted in Fig. 3.1. The extinction ratio is higher than 30 dB and the optical loss is lower than 3 dB in the outermost outputs, which have the worst characteristics. Moreover, the theoretical polarization dependence of the optical loss is less than 0.35 dB.

The phase modulation mechanism used in this device was carrier-induced refractive index change in the Q1.3 material. The physical mechanisms of refractive index change through carrier injection are the bandfilling, free-carrier plasma, and the bandgap shrinkage effects. The refractive index change is dependent on the modulation of absorption coefficient through Kramers-Kronig relations. Bandfilling and free-carrier plasma effects, which are dominant over bandgap shrinkage, lead to a decrease of the refractive index if the density of carriers in the intrinsic region increases [8]. In addition to these mechanisms, the thermo-optical effect exists if the temperature increases due to current flow. The thermo-optic effect is undesired because its dynamic response is much slower than that of the electrooptical effects. The only way of reducing temperature change is optimizing the design and processing conditions to reduce the current and contact resistance. The width and length of phase shifters are important design parameters along with the epitaxial design, which has been explained. Theoretically, narrow phase shifters operate with a lower current than wide ones because of the smaller area as long as the confinement of optical mode does not drop significantly.

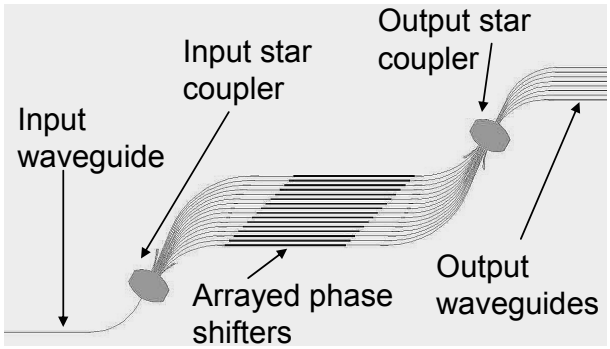


Fig. 3.2 Planar layout of the designed 1×8 switch.

Nevertheless, it was experimentally observed that 4-μm-wide phase shifters are more efficient than narrower ones because of the damage caused by the dry etching process and the higher contact resistance. Therefore, the phase shifter width was decided to be 4 μm. The length of the phase shifters was designed to be 800 μm after our previous experiments, where we measured $I_{2\pi}$ (the current required for a phase shift of 2π) to be approximately equal to 20 mA.

The other layout parameters not directly related to switching performance were designed in order to achieve low optical loss and a compact size. The minimal radius of curvature in the waveguide bends was calculated to be 360 μm by using two-dimensional beam propagation method (BPM) with the effective index approximation. Geometrical optimization of radii and angles of bends was carried out to make the antisymmetrical switch design as small as possible. The input and output waveguides were linearly tapered to a width of 5 μm for higher modal match with the optical fiber. The length of the tapers was 50 μm, which is more than enough for a low-loss transition of optical modes. The waveguides were facet normal at the input and the output. The pitch of the phase shifters and the output waveguides was designed as 30 μm. Under forward-biased operation, the electrical crosstalk between phase shifters is negligible even with such short distances. The final layout design of the switch is displayed in Fig. 3.2. The dimensions of the designed 1×8 switch are 3.3 mm × 1.8 mm. The size is strongly dependent on the degree of confinement in the waveguides because high-index-contrast waveguides are compatible with short star couplers and small bending radii. Therefore, if minimizing the footprint had been the major design goal, the

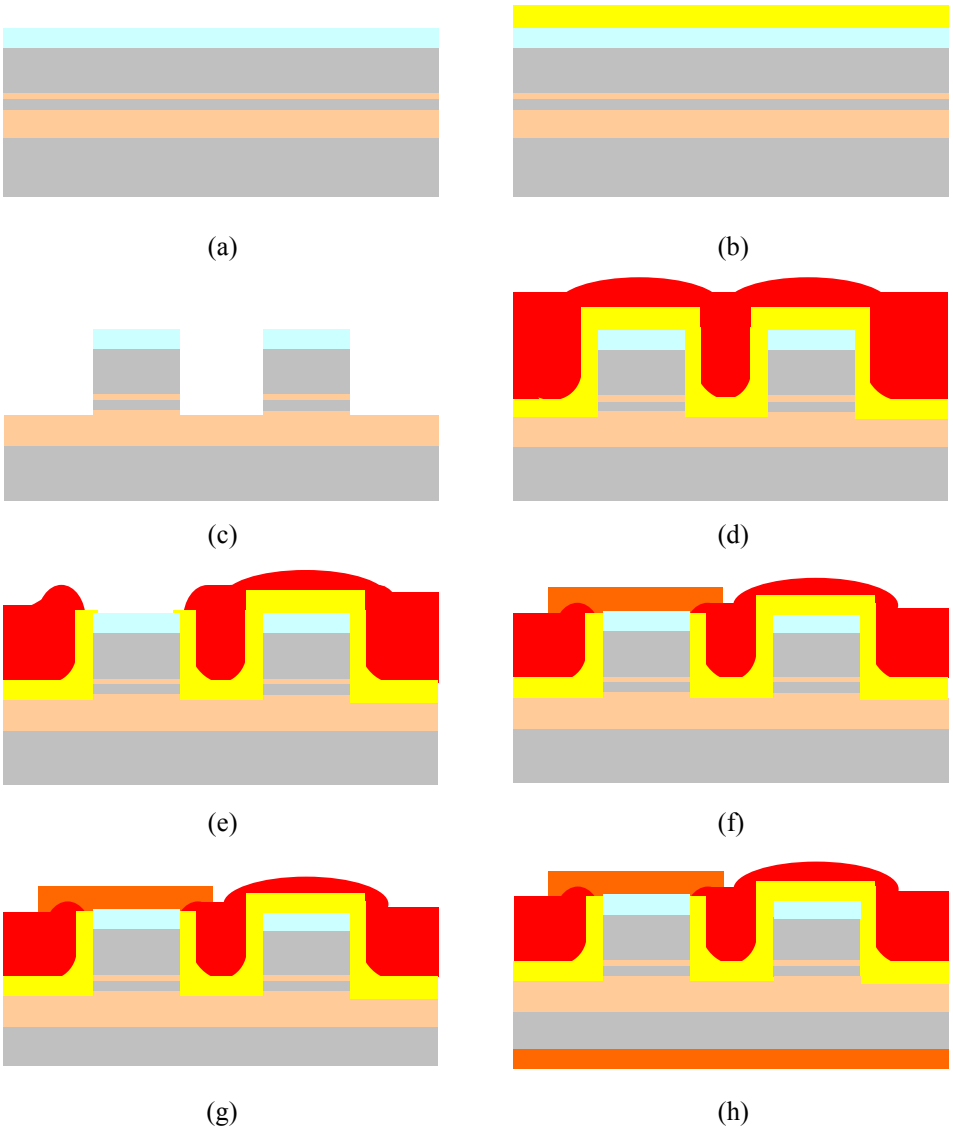


Fig. 3.3 Fabrication process of the phased-array switch. (a) Cleaved sample, (b) SiO_2 hard mask sputtering, (c) Waveguides formation by etching, (d) SiO_2 passivation layer sputtering and polyimide coating, (e) Contact opening, (f) p-metallization, (g) Substrate polishing, (h) n-metallization.

devices would have been considerably smaller with deeply etched waveguides.

3.2.2 Fabrication of the Device

The first step of the device fabrication is metal-organic vapor-phase epitaxial (MOVPE)

growth. The growth of the wafer used for the fabrication of this device was not carried out in our laboratory. Instead, it was purchased from a commercial supplier. Since the entire device has an identical stack design, a single growth cycle was followed. Next, the fabrication process after growth is explained with the help of the schematics in Fig. 3.3. Note that a simple fabrication process was followed for this device and it was modified for the other devices according to the measurement results.

Contact lithography was used throughout the process. After SiO_2 hard mask sputtering and patterning, all waveguides and star couplers were formed by dry etching down to approximately 50 nm below the top of the core layer (Fig. 3.3-c). The dry etching process is chlorine (Cl_2) based inductively-coupled-plasma reactive-ion etching (ICP-RIE) at a temperature of 220ºC. Argon (Ar) was also introduced into the etching chamber to increase the directionality of the sidewalls. After dry etching, the SiO_2 hard mask was removed by chemical etching in buffered hydrofluoric acid (BHF). Next, a 300-nm-thick layer of SiO_2 was sputtered for passivation. Passivation is necessary to reduce the leakage current and optical propagation loss caused by waveguide sidewall roughness. This was followed by the spin-coating of a thick polyimide layer for both electrical isolation and planarization (Fig. 3.3-d). This step is necessary to prevent the electrical wires from being disconnected due to the height difference between the core and cladding of the waveguides, which is close to 1.5 μm in this device. The polyimide was used as a negative photoresist during the contact opening lithography. The polyimide in the contact opening regions was removed partially by developing after contact opening patterning. Next, the sample was annealed in a temperature-controlled chamber at 180ºC for 30 min, 300ºC for 30 min, and 400ºC for 1 hour respectively. The annealing is necessary for the hardening of the polyimide. Next, the remaining polyimide in the contact opening regions was removed by anisotropic etching in O_2/Ar plasma in an ICP-RIE chamber. Note that the etching rate is approximately equal inside and outside the contact opening, so attention has to be paid to form sufficient height difference between inside and outside of the contact opening window before the etching. The polyimide was etched until no polyimide was left on the top of the phase shifters. Next, the SiO_2 in these regions was etched with the help of CHF_3, Ar, and O_2 in an ICP-RIE chamber. (Fig. 3.3-e).

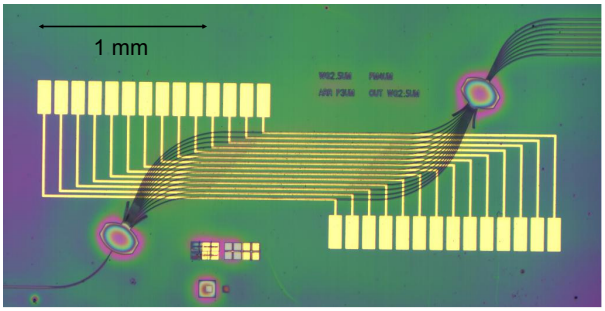


Fig. 3.4 Micrograph of the fabricated switch.

After contact opening, a short H_2SO_4:H_2O_2:H_2O (1:1:10) treatment was done to obtain a clean interface at the top of the contact layer. Later, 50-nm-thick titanium (Ti) and 400-nm-thick gold (Au) were deposited and patterned by lift-off for p-metallization (Fig. 3.3-f). The reason of depositing Ti under the Au layer is to improve the adhesion of the metal layers and to prevent the diffusion of Au into the contact layer. Next, the substrate of the sample was polished to a thickness of 260 nm for better thermal conductivity and easier cleaving (Fig. 3.3-g). Au was sputtered on the back side of the sample as an n-contact electrode (Fig.3.3-h). The sample was annealed with a rapid thermal process to form Ohmic contacts between the highly doped semiconductor and the metal. After the annealing, the sample was cleaved into chips consisting of individual switches. The micrograph of a cleaved 1×8 switch is shown in Fig. 3.4. The aberrations at the intersections between the star couplers and waveguides were caused by the resolution of our contact lithography process and etching conditions.

The processed chips were mounted on aluminum nitride (AlN) chip carriers (submounts) by using a conductive epoxy. The reason of using AlN is its high thermal conductivity, which affects the device temperature. The electrode pads were wire-bonded to the chip carrier electrodes to access p-contacts. The n-contact was used as the common ground. The chip carrier was mounted on a copper plate with a thermally conductive epoxy for heat removal. To control the phase shifters independently, the electrodes on the chip carrier were wire-bonded to a printed circuit board (PCB), which was electrically connected to a multi-channel current source.

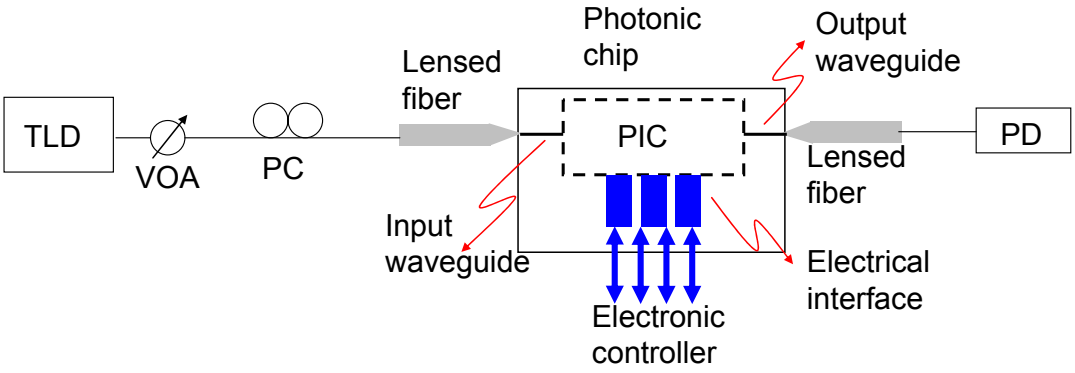


Fig. 3.5 Basic optical measurement setup. TLD: tunable laser diode, VOA: variable optical attenuator, PC: polarization controller, PIC: photonic integrated circuit, PD: photodetector.

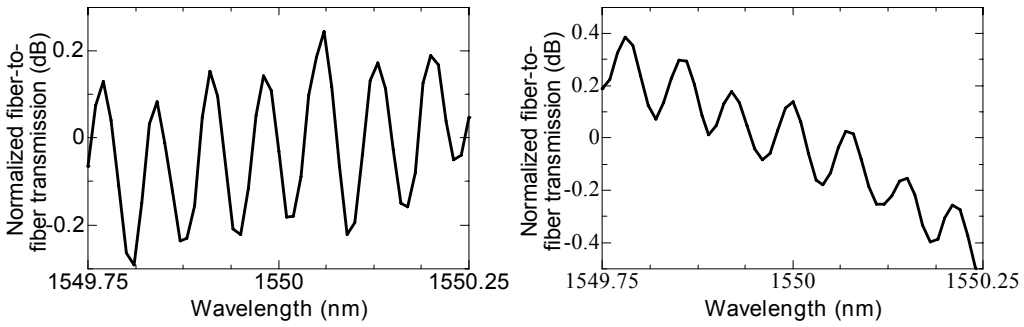
3.2.3 Characterization of the Device

3.2.3.1 Basic Characterization of Waveguides and Phase Shifters

The first step of the characterization is the measurement of the current-voltage (I-V) curve to check the electrical properties of the pin double heterojunction. An unexpected I-V curve (e.g. high current below the threshold voltage) is the sign of malfunctioning phase shifters. An average phase shifter exhibited a differential resistance of 50 Ω and a threshold voltage of 0.8 V. This threshold voltage is close to the theoretical value.

Next, optical and optoelectronic measurements were done with the experimental setup shown in Fig. 3.5 schematically. This is the general setup used for basic optical experiments such as propagation loss, static and dynamic optical switching measurements. A tunable laser emitting around the wavelength of 1550 nm was used as the light source. A variable optical attenuator (VOA) was used to control the optical power at the input. The polarization state of light at the input of the chip was controlled by using a polarization controller. The light was transmitted between these components via single mode fibers (SMF). The light was coupled to and from the chip by end-coupling to the cleaved waveguide facets. To obtain a lower coupling loss, a special fiber with a lens attached at the tip (lensed fiber) was employed. The fibers were maintained a focal distance away from the facets.

The propagation loss in the straight test waveguides was measured by using the



(a) (b)

Fig. 3.6 Fiber-to-fiber transmission spectrum of optical power normalized to the average value at 1550 nm for (a) TE-, and (b) TM-polarized light.

Fabry-Perot oscillation in the fiber-to-fiber transmission spectrum. In a photonic chip with facet-normal input and output waveguides, light is partially reflected back at the input and output facets, which causes an interference among the incident and reflected waves. As a result, an oscillation is observed in the transmission spectrum. The amplitude of this oscillation in dB scale, i.e. the peak-to-valley ratio, depends on the on-chip loss and facet reflectivity with the following relation.

$$L(dB) = -10\log\left(\frac{1}{r_1 r_2}\frac{\sqrt{H}-1}{\sqrt{H}+1}\right), \tag{3.1}$$

where L is the on-chip loss in dB, r_1 and r_2 are the field reflection coefficients at the input and output, and H is the peak-to-valley power ratio. The derivation of this equation is available in the Appendix. The waveguide propagation loss was measured with the straight test waveguides located on the same chip as the switch. The normalized fiber-to-fiber optical power transmission spectra for TE and TM polarization states of light are available in Fig. 3.6. The coupling loss to the waveguides is in the 5-6 dB range. The estimated waveguide propagation loss is 22-23 dB/cm for TE and 27-28 dB/cm for TM polarization according to (3.1) assuming that $r_1 r_2 = 0.30$. These propagation losses are extremely high because of two major reasons. The InGaAs contact layer, which has a very high absorption coefficient at 1550 nm, was not removed from the top of passive waveguides for simplification of the fabrication process. The absorption coefficient in p-doped InGaAs is 8000 cm^{-1} [12]. The power overlap of the

fundamental mode on InGaAs layer, which was calculated as 1.5×10^{-4} using TMM, leads to a loss over 5 dB/cm. The other reason is the very high sidewall roughness in the waveguides. Although the substrate temperature was intended to be 220 ºC during chlorine etching, we noticed poor heat transfer to the sample after the fabrication of this device. It is known that $InCl_3$, which is the output of a chemical reaction between indium and chlorine, increases the surface roughness at temperatures below 150 ºC [13]. These problems were solved during the fabrication of other devices as explained later.

The next measurement was the phase-current relationship of the phase shifters. The test phase shifters on the chip were used for this purpose. Similar to the measurement of waveguide propagation loss, efficiency of a single phase shifter can be measured by observing the Fabry-Perot oscillation in the optical transmission spectrum. The peak wavelengths shift linearly proportional to the phase shift, and they reach the peak wavelengths of the adjacent modes after a phase shift equal to π, which

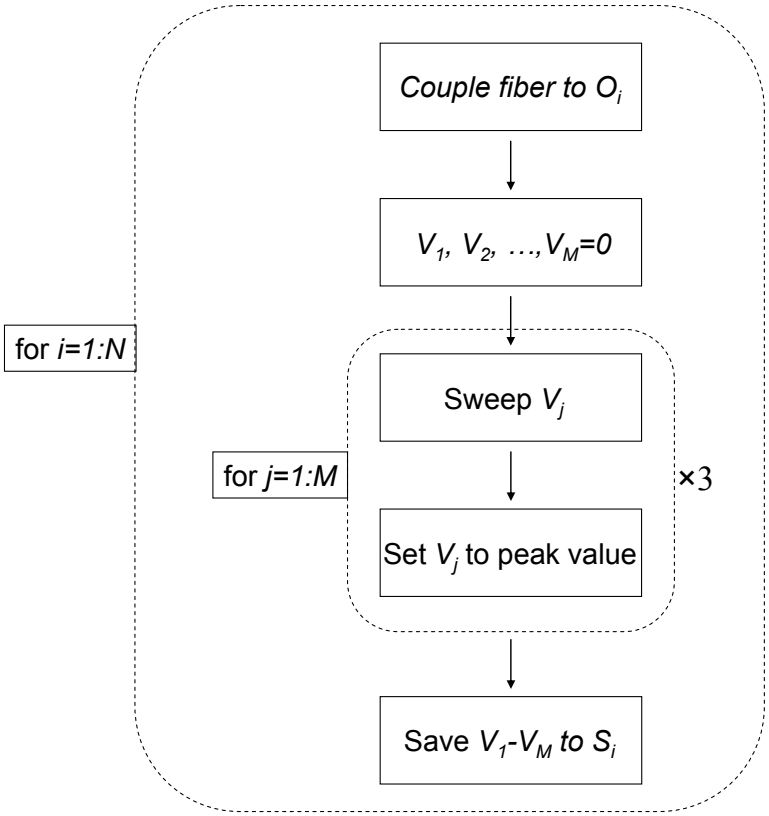


Fig. 3.7 Algorithm for finding the operating conditions of a $1 \times N$ phased-array switch. M is the number of phase shifters, O_i is the ith output, and S_j is the jth state.

corresponds to a phase shift of 2π in round-trip propagation. The current required for a phase shift of π, referred as I_{π}, was measured as approximately 14 mA. Since phase values have to be up to 2π, higher current injection is necessary to operate the switch.

3.2.3.2 Finding the Operating Conditions of the Switch

A $1 \times N$ phased-array optical switch that can route to a single output port at a time has N different states of operation. Each state of operation forms a connection between the input and the corresponding output port. The state of switching is determined by the bias conditions of the phase shifters. Each switching state has a unique set of analog bias voltages across the phase shifters. Considering that there are $AOR \times N$ phase shifters, where AOR is the array-to-output ratio, a table of $(AOR \times N) \times N$ analog voltages has to be filled to operate a $1 \times N$ switch. The voltages (or the corresponding currents) in this lookup table were derived experimentally before the characterization of the switch.

Theoretically, the bias voltages can be calculated after measuring the phase-voltage curves of the phase shifters. A mapping between the phase and the voltage is sufficient to find the conditions in all states in an ideal phased-array switch. Nevertheless, this method cannot be used because of the phase errors in the array, which gives the arrayed waveguides an unpredictable distribution of initial phase under no bias. Phase error is a well-known phenomenon in arrayed waveguide gratings (AWG) and is caused by the aberrations in the waveguide width and the star coupler-waveguide intersections [14,15]. Because of the phase error, an iterative algorithm was used in order to find the optimal bias voltages corresponding to the switching states.

A multi-channel current source was used to control the bias conditions of the phase shifters. The bias conditions of each state were derived with the following algorithm, which is displayed schematically in Fig. 3.7. Initially, all the bias voltages were set to zero and the fiber was coupled to the output port whose state was to be found. Later, the bias voltages of all phase shifters were swept in a range that covers a phase of 2π one-by-one. Theoretically, the output power depends on the phase of an arrayed waveguide sinusoidally. Fig. 3.8 shows the power measured at an output of the switch versus the current injected to one of the phase shifters. In this example, peaks

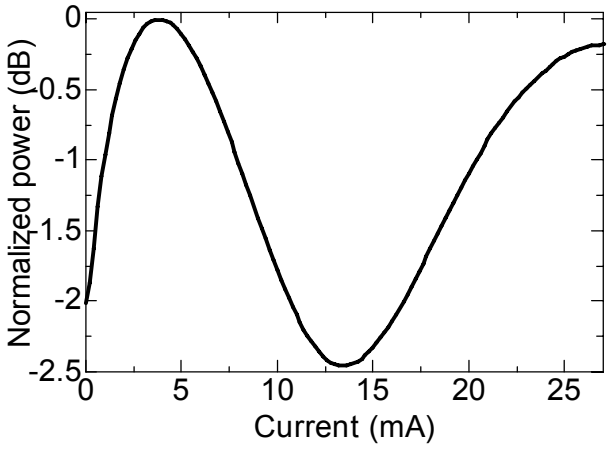


Fig. 3.8 Normalized optical power measured at an output of the switch vs. the current injected to one of the phase shifters.

exist at both 4 mA and 27 mA, which means that the phase changes by 2π in this interval. After sweeping the voltage across a phase shifter, its bias voltage is set to the smallest value corresponding to a peak of the optical power to keep the energy consumption and device temperature as low as possible. After setting the bias values of all phase shifters to peak positions, this iteration is repeated twice to form a better matching of phases. The optimization procedure is explained graphically with the help of phasors in Fig. 3.9. In this example, the imaginary switch consists of four arrayed waveguides. The phasors F_1-F_4 represent the amplitude and phase of optical field in the arrayed waveguides. The phase in each waveguide is assumed to be random initially (Fig. 3.9-a). Sweeping the voltage across the first phase shifter is equivalent to rotating F_1 around the origin with a small change of its amplitude, which is ignored in this demonstration. The peak optical power is observed when the phase of F_1 is exactly equal to the phase of F_2+F_3+F_4. After the phase of F_1 is set to its new value, F_2 is rotated around the origin and its phase is set to the phase of F_1+F_3+F_4. As shown in Fig. 3.9-e, when all voltages are swept, the phases on the arrayed waveguides are much closer to each other compared to the initial condition. As a result, the field calculated as their sum has a much larger amplitude than the initial value. If this procedure is repeated twice, phase matching is achieved to a degree that the amplitude of the sum of phasors is larger than 90% of the highest possible amplitude (perfect phase matching condition).

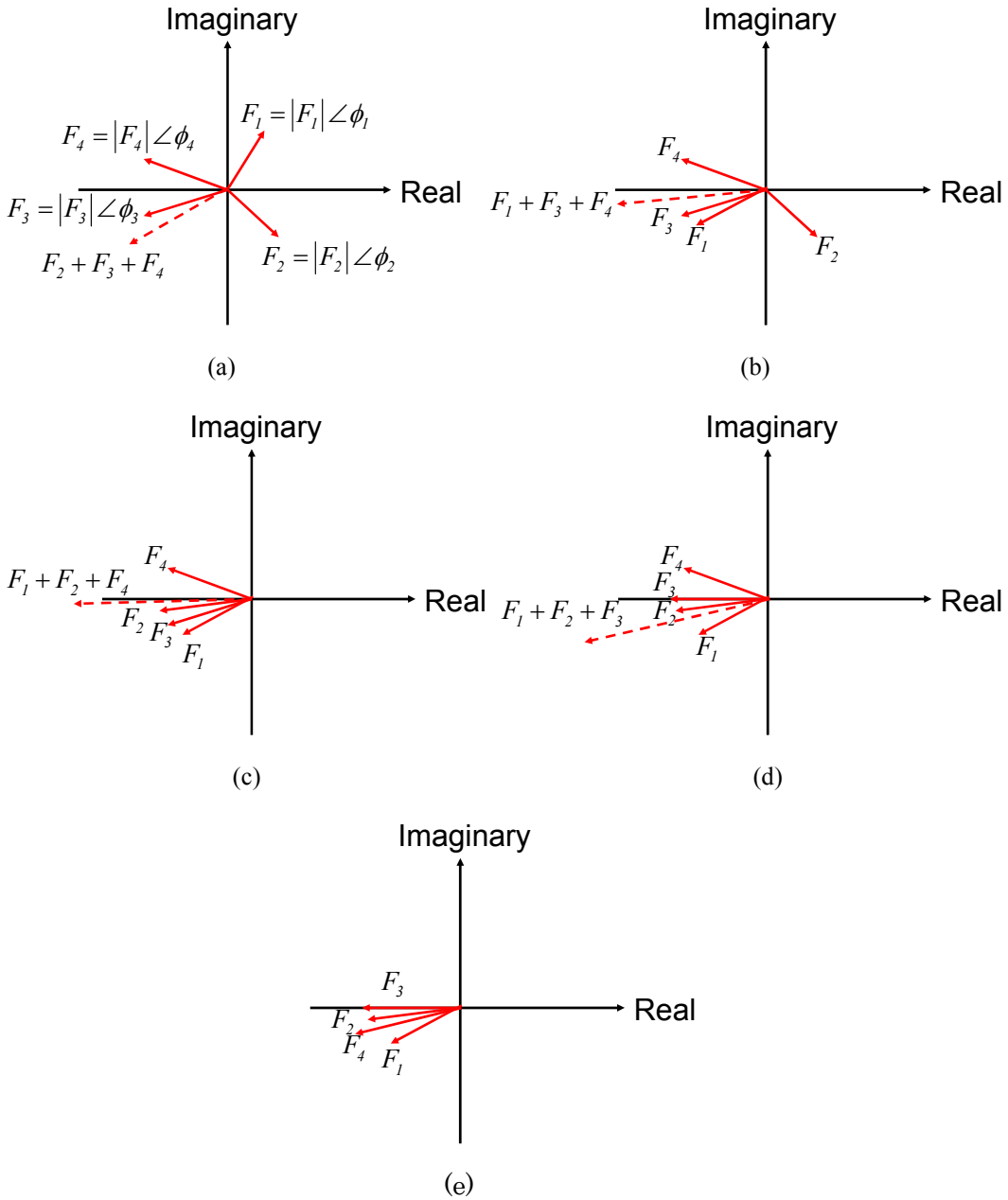


Fig. 3.9 Phasor representation of the procedure to find the switching conditions in a hypothetical switch with four phase shifters. (a) Initial condition with a random distribution of phase among the arrayed waveguides, (b) after setting V_1 to the peak value, (c) after setting V_2 to the peak value, (d) after setting V_3 to the peak value, and (d) after setting V_4 to the peak value. F_1 - F_4 represent the amplitude and phase of the waveguide mode fields. The amplitude values of the phasors and their sums are not to scale.

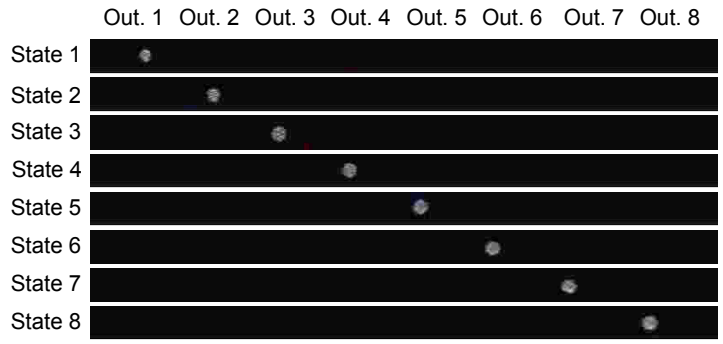


Fig. 3.10 Near-field images at the output plane of the switch in eight different states. Out. 1 – Out. 8: Output 1 – Output 8.

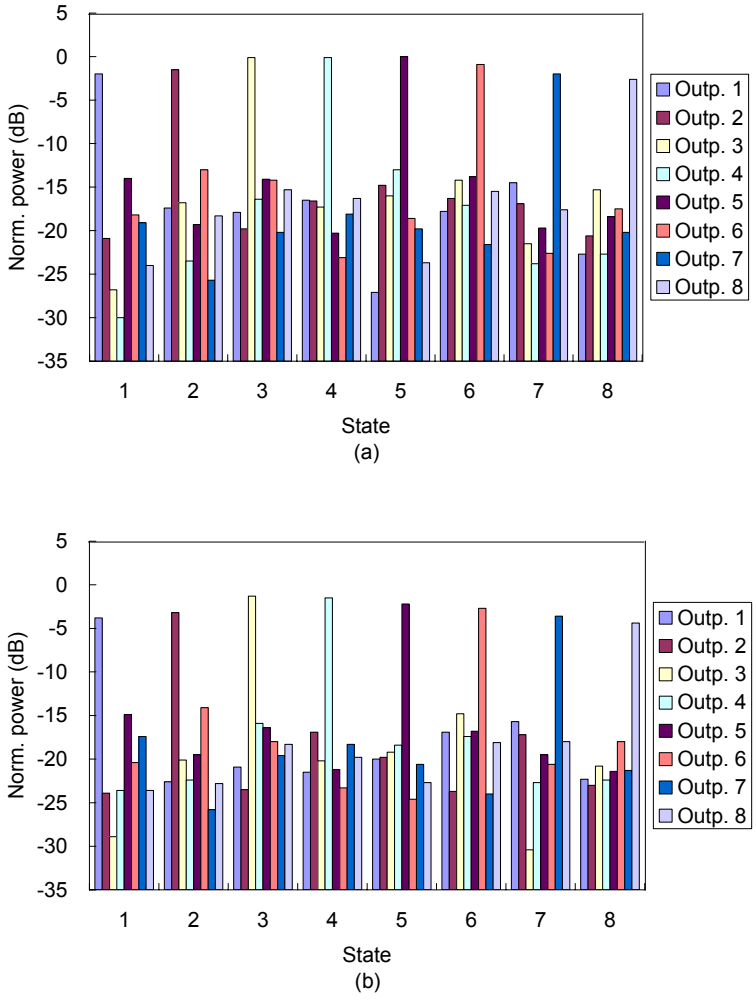


Fig. 3.11 Normalized optical transmittance of (a) TE- and (b) TM-polarized light to the output ports of the 1×8 switch in eight switching states.

Note that this constructive interference occurs in a single output at a time because the phase distribution in the other outputs is different as a consequence of different path lengths in the output star coupler. Eight switching states of the 1×8 switch were found with this procedure. Throughout the process, the polarization state and the wavelength of light were maintained as TE and 1550 nm respectively. The sample was mounted on a thermo-electric cooler with a fixed temperature of 20ºC.

3.2.3.3 Static and Dynamic Characterization of the Switch

After the switching conditions were found, the device was characterized under static condition, i.e. while the switching state was constant in time. First, operation of the device was observed qualitatively by monitoring the near-field images at the output plane using a microscope objective lens and an infrared camera, which recorded the images in Fig. 3.10. As a consequence of switching, the beam is observed in different positions of the output plane depending on the state. In order to evaluate the switching performance quantitatively, the optical power coupled to a lensed fiber from the output ports was measured one by one. Fig. 3.11 compares the transmittance to the outputs in all the switching states with TE- and TM-polarized input light. For a clear view of crosstalk levels, the power was normalized to the highest output power (State 5, Out. 5, TE), where the fiber-to-fiber loss was measured as 29.9 dB. The crosstalk suppression ratio is 17.7 dB on average, and 11.5 dB and 10.9 dB in the worst cases for TE- and TM-polarized input respectively. The on/off extinction ratio is above 12.1 dB (TE) and 11.4 dB (). The polarization-dependent loss (PDL) is in the range of 1.2-2.2 dB at the wavelength of 1550 nm. Note that the switching conditions were optimized for TE polarization in the beginning and were kept unchanged without further optimization for TM polarization. The value of PDL is consistent with the polarization dependence of the propagation loss, which was measured as approximately 5 dB/cm. Therefore, the inherent PDL of the switch is estimated to be a small portion of the measured value. Among the total fiber-to-fiber loss of 29.9 dB for the best case (State 5, Out. 5, TE), the on-chip loss is estimated to be approximately 18 dB. The major contribution to this loss is the high propagation loss in the waveguides.

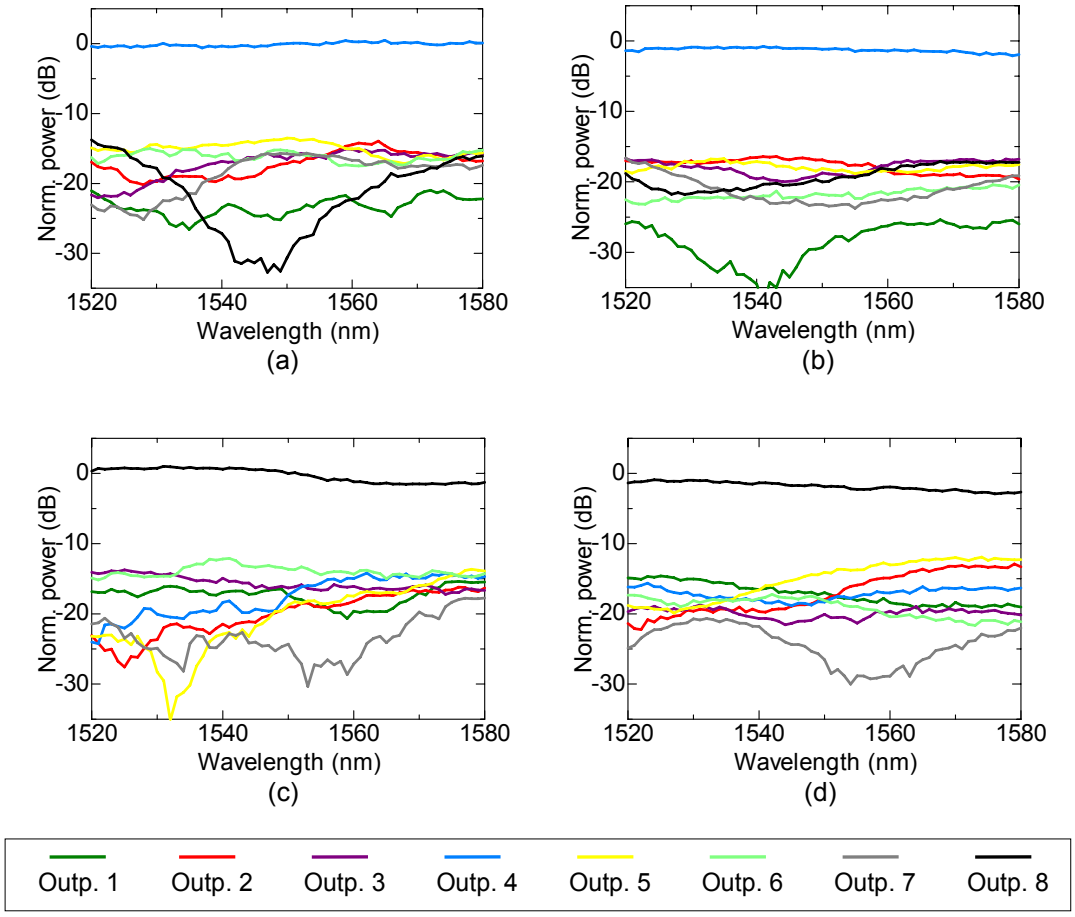


Fig. 3.12 Normalized optical power at the outputs of the switch as a function of the wavelength in State 4 (TE in (a) and TM in (b)) and State 8 (TE in (c) and TM in (d)). Normalization was done with respect to the power of 1550-nm-wavelength, TE-polarized light in each state.

Next, the wavelength dependence of the switch was measured by sweeping the wavelength of the CW light between 1520 nm and 1580 nm. In Fig. 3.12, the optical power at the output ports is plotted as a function of wavelength in switching states of State 4 and State 8 and both polarization states of TE and TM. Similar results were obtained in the other states, where the maximum wavelength-dependent loss of 2.5 dB. In this spectral range, the highest value of crosstalk was -9.6 dB, which was observed in State 8. This low wavelength dependence owes to the optimally designed arrayed waveguides with equal path length as well as the low wavelength sensitivity of the phase shifters.

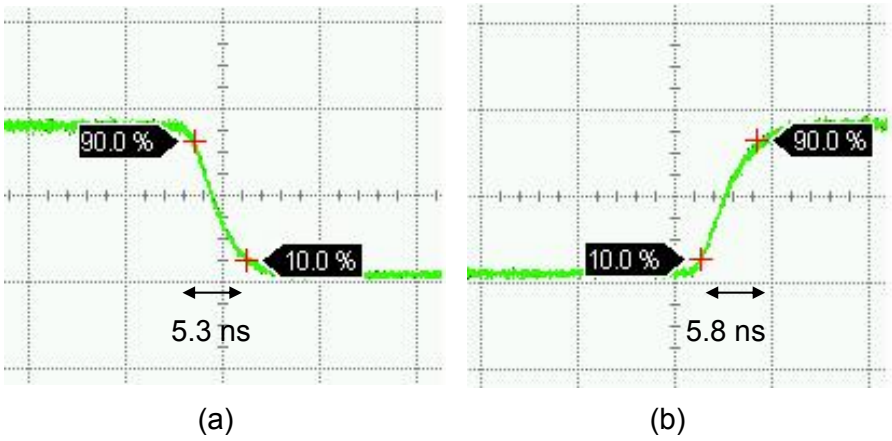


Fig. 3.13 (a) Falling and (b) rising edges of the optical power at Output 4 in time domain with a square-wave electrical signal applied at one of the phase shifters.

In addition to the static characteristics, the dynamic switching response was measured. For simplicity, one of the phase shifters was driven by a square-wave voltage between 0 V and 1.5 V from an arbitrary waveform generator with a 10%-90% transition time of 1.4 ns. All the other electrodes were grounded. Fig. 3.13 shows the rising and falling edges of the optical waveform at Output 4 monitored using a high-speed digital sampling oscilloscope with an electrical bandwidth of 65 GHz. The optical extinction ratio in this measurement is 5.4 dB because only one phase shifter was dynamically driven instead of a complete dynamic switching experiment. The rising edge, which corresponds to the depletion of carriers in this experiment, has a 10%-to-90% transition time of 5.8 ns; and the fall time, which corresponds to carrier injection, is 5.3 ns. The reconfiguration speed is limited by the carrier lifetime in the InGaAsP guide layer and the electrical parasitics

Finally, the bit error rate (BER) characteristics of the switch were tested. BER measurement is a widely used technique to assess the signal quality in optical communication links. A modulated signal is transmitted through the link and detected, after which the ratio of erroneous bits is measured. This figure of merit is referred as BER and depends on several factors including the signal-to-noise ratio (SNR) and the modulation format. The measurement setup is shown schematically in Fig. 3.14. The signal routed by the switch is intentionally attenuated to certain levels of power and

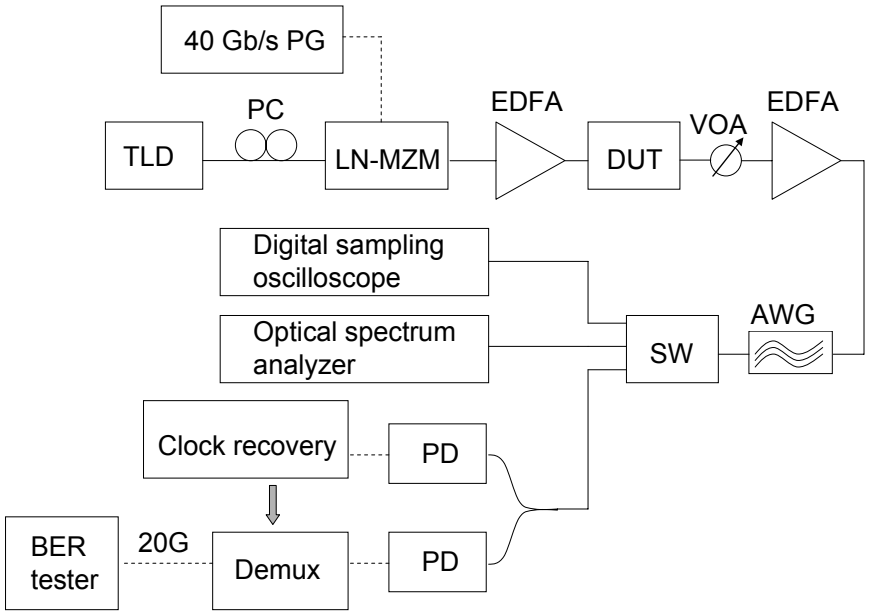
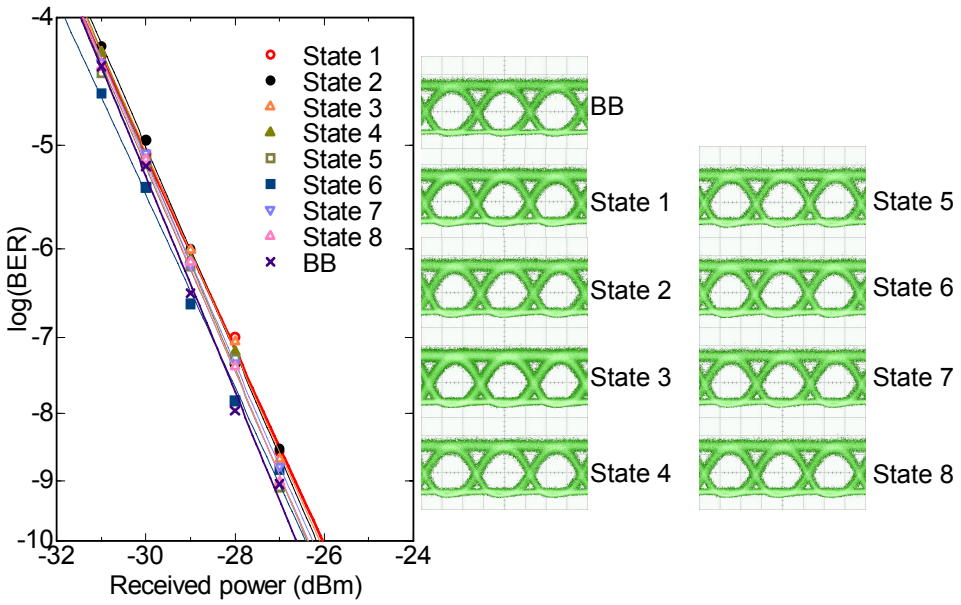


Fig. 3.14 Schematic diagram of the BER measurement setup. TLD: tunable laser diode, PC: polarization converter, LN-MZM: lithium niobate Mach-Zehnder modulator, PG: pattern generator, EDFA: erbium-doped fiber amplifier, DUT: device under test, VOA: variable optical attenuator, AWG: arrayed waveguide grating, SW: opto-mechanical switch, PD: photodetector, Demux: demultiplexer, 20G: 20 Gb/s.

amplified before detection by an avalanche photodetector in the preamplified receiver configuration. Low average power leads to a high BER because of the reduced SNR. The impairments caused by a device in the link are quantified by comparing the BER trends with and without the device under test (DUT). The condition without the DUT is realized by bypassing it and is referred as back-to-back condition. If the DUT introduces distortion to the signal, higher average power becomes necessary for a target BER compared to the back-to-back condition. This power difference is equivalent to the reduction of effective power and is referred as power penalty, which is a widely-used figure of merit.

The BER of the signal routed to different output ports of the switch was measured with a 40-Gb/s non-return-to-zero (NRZ) on/off keying (OOK) modulated pseudo-random binary sequence (PRBS). Figure 3.15 displays the measured BER versus received optical power and the corresponding eye diagrams observed by a digital sampling oscilloscope. The power penalty at the BER of 10^{-9} is lower than 0.6 dB in all



(a) (b)

Fig. 3.15 (a) BER vs. average received power after transmission through different ports of the switch compared to the back-to-back (BB) condition, and (b) eye diagrams observed on a digital sampling oscilloscope screen under the corresponding conditions.

switching states. This value is almost within the measurement error limit, so the switch does not introduce significant distortion to the signal. Note that the waveguides are facet-normal at the input and output of the chip and these facets were not subjected to anti-reflection coating. The reflections usually cause some power penalty due to the Fabry-Perot oscillations, which lead to power fluctuations. The eye diagrams, which present a qualitative evaluation of the detected signal, are clear and do not have any visible distortions compared to the back-to-back condition.

3.2.4 Discussion

The most serious problem of this switch is the high propagation loss. The waveguide propagation loss can be reduced by removing the InGaAs contact layer in the passive sections and by improving the etching process to reduce sidewall roughness. This high propagation loss is not only the major reason of high insertion loss, but also does it

contribute to a large portion of the PDL. The high crosstalk in the experiment compared with the calculation is attributed to the higher-order waveguide modes and the aberrations of waveguide width and star coupler-waveguide intersections. Since the design parameters were optimized for the fundamental waveguide modes, switching conditions are not met with the higher-order modes, which have different refractive indices. The 2.5-μm-wide waveguides in this device are multimode and the higher order modes can be excited both in the straight waveguide-bend intersections and in the star couplers. The deviation of waveguide width from the designed value also affects the extinction ratio significantly as shown in Fig. 3.16. The extinction ratio reduces considerably if the waveguides are wider than designed. For a constant value of output pitch, the distance between adjacent waveguides becomes smaller if the waveguides get wider. This leads to a higher modal overlap with the optical beam deflected to adjacent ports. According to the scanning electron microscope (SEM) images, the measured waveguide width was approximately 500 nm larger than the designed value. Therefore, a better control of the width of preferably single-mode waveguides is expected to improve the extinction ratio.

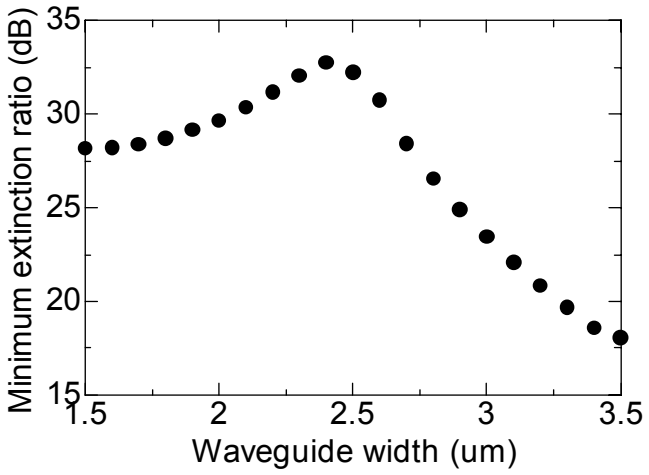


Fig. 3.16 Minimum extinction ratio versus the width of waveguides at the intersections with star couplers. Higher-order modes are ignored.

3.3 WAVELENGTH-INSENSITIVE LOW-LOSS MONOLITHIC 1×16 PHOTONIC SWITCH

The device introduced in the previous chapter has demonstrated interesting characteristics, including low polarization dependence and broad spectral range. However, it suffers from a major problem of high propagation loss. The fiber-to-fiber loss of approximately 30 dB is too high for high-speed optical packet switching experiments. Moreover, the claim of scaling phased-array switches without trading off basic device characteristics had to be tested experimentally in order to propose ultra-high-capacity packet routing by employing these devices. An integrated 1×16 switch was designed and fabricated with these motivations. Both design and fabrication of this device were revised based on the previous experimental results.

3.3.1 Design and Fabrication of the Device

The phase shifters in the previous device suffered from low efficiency, which could be improved by reducing the bandgap energy of the quaternary layer. However, the same wafer as the previous device was used for practical reasons. Therefore, the modifications in the design were limited to the planar layout of the photonic circuit. Width of the waveguides in the bends and at the openings of the star couplers was reduced to 2 μm to mitigate the effect of higher order modes. The minimum bending radius was modified to 500 μm to increase the modal overlap with straight waveguides and suppress the radiation loss at the bends. An AOR of 1.5, which corresponds to an array size of 24, was chosen as a compromise between high extinction ratio and low power and small size. The length of star couplers was set as 240 μm. The array and output pitches were 2.5 μm and 2.8 μm respectively. With these design parameters, the theoretical value of the insertion loss is less than 3.5 dB and the extinction ratio is above 31 dB.

The waveguide etching process was modified to reduce the propagation loss. Instead of the chlorine etching, methane (CH_4)-based reactive ion etching was preferred. This is a room-temperature process with a repeatable sidewall angle and a more

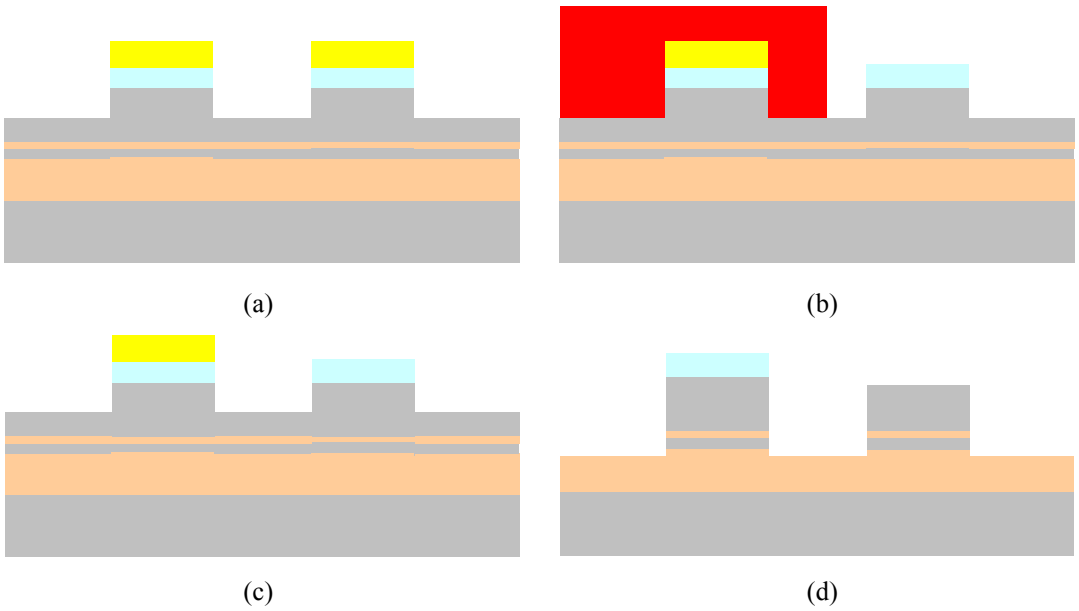
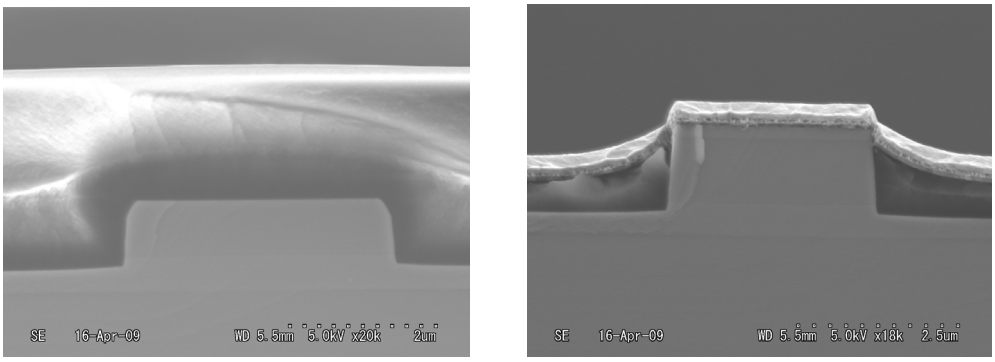


Fig. 3.17 Two-step etching process. (a) First-step etching, (b) selective etching of hard mask on passive waveguides, (c) photoresist removal, (d) second-step etching.

controllable etching depth. A cyclical process, which consists of multiple subsequent steps of CH_4/H_2 etching and oxygen cleaning, was used in order to prevent the effects of polymer deposition during etching [16]. The sidewalls of waveguides were measured to be tilted by 7º. The p-doped InGaAs contact layer was removed in the passive waveguides by using a two-step etching process separated by a lithography and wet chemical etching of the SiN_x hard mask. These steps are shown in Fig. 3.17 schematically. In addition to these modifications, two minor modifications in the process were using only polyimide without SiO_2 for passivation and leaving a baked photoresist layer on the polyimide for easier contact opening and planarization. SEM images of waveguide and phase shifter cross-sections are shown in Fig. 3.18. The top view of the device in an optical microscope and the SEM image of the same device after wire bonding are also presented in Fig. 3.19. The aberrations in star coupler openings and waveguide dimensions have been mostly mitigated in this device.

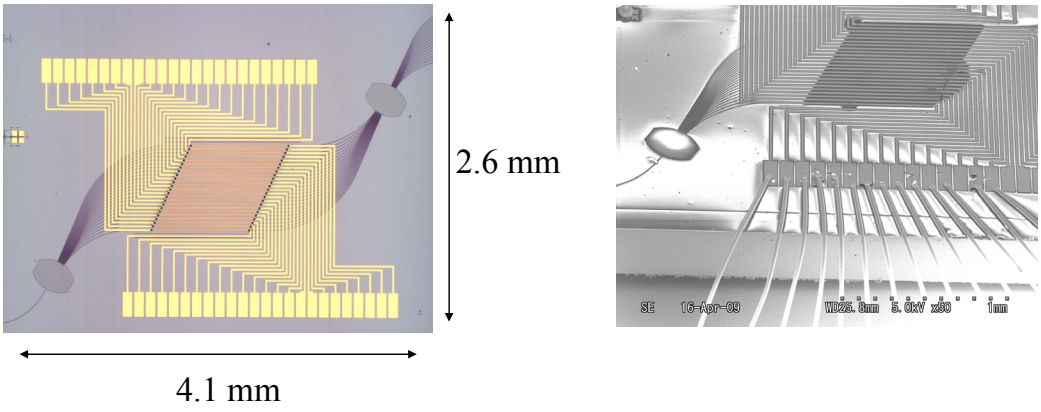
3.3.2 Characterization of the Device

The propagation loss in passive waveguides was measured as lower than 2 dB/cm based



(a) (b)

Fig. 3.18 SEM cross-sectional images of (a) a passive waveguide protected by polyimide (dark layer) and a thick layer of photoresist (above polyimide), (b) a phase shifter with a p-contact.



(a) (b)

Fig. 3.19 (a) Optical microscope image of the switch, and (b) SEM image of the same device after wire bonding. The total device size is 4.1 mm × 2.6 mm including the input/output bends and lateral tapers, which are not completely shown in the figure. The waveguides are facet-normal at the input and the outputs.

on the approximately 5 dB amplitude of Fabry-Perot oscillations in the fiber-to-fiber transmittance (Fig. 3.20). Therefore, the propagation loss problem was successfully solved. However, low efficiency of phase shifters was encountered as a problem. As shown in Fig. 3.21, a phase shift of only 0.5π is obtained by current injection, which has a peak at approximately 20 mA and reduces with a rollover at larger values of current. The reason of this rollover is the thermo-optic effect, which becomes dominant over

carrier-induced phase modulation with large current due to heating. Since thermo-optic effect cannot be used for packet switching because of its slow dynamic response, the usable part of this graph is the region on the left of the peak, which corresponds to a maximum phase shift of only 0.5π. This phase shift is not sufficient to operate the switch. Experiments with both TE and TM polarization states and substrate temperatures of 10ºC and 20ºC gave similar results as expected.

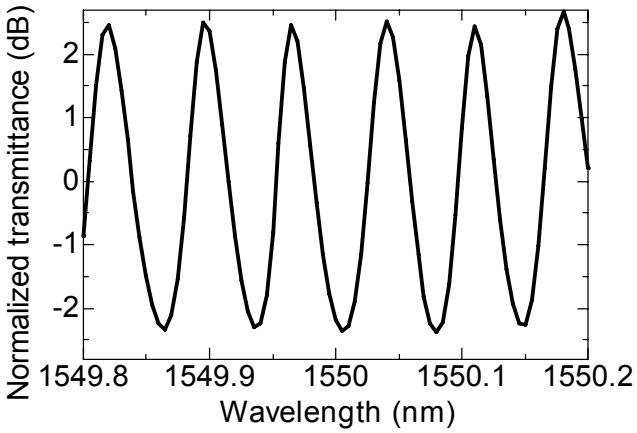


Fig. 3.20 Fabry-Perot oscillations of the fiber-to-fiber optical transmittance.

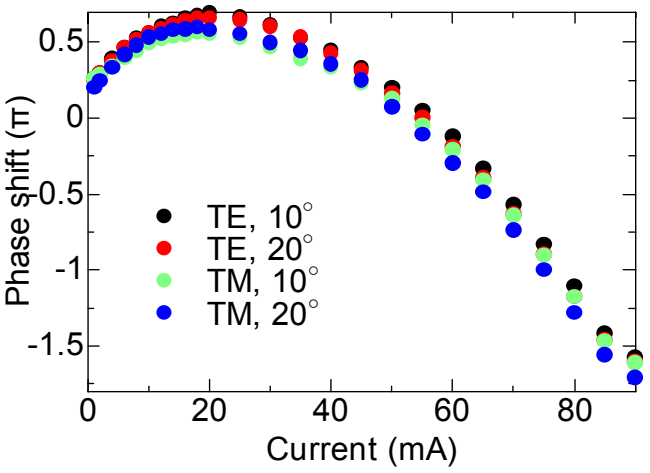


Fig. 3.21 Phase shift in a 800-μm-long phase shifter versus current injection.

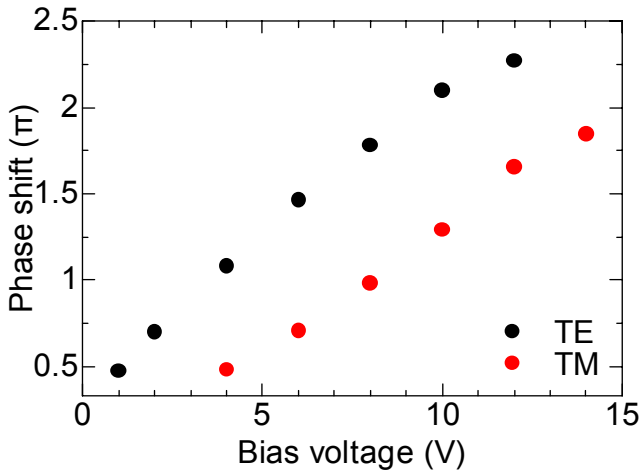


Fig. 3.22 Phase shift in a 800-μm-long phase shifter versus the reverse bias voltage.

This low efficiency is attributed to the plasma damage caused by the CH_4-H_2 etching process. It is known that CH_4-H_2 RIE etching process imparts damage to InP and InGaAsP surfaces [17,18]. Crystallographic damage in the regions close to the surface and passivation of acceptors in the p-doped materials are two major defects caused by this etching process. The latter effect is compensated for by thermal annealing, which is a routine process step, so the formation of recombination centers due to crystallographic defect is supposed to be the major cause of efficiency reduction.

As a solution to the efficiency problem, the phase shifters were decided to be operated in the reverse bias regime. The electric field around the intrinsic region induces phase modulation by linear and quadratic electrooptic effects in bulk InGaAsP [19]. The efficiency of phase modulation under reverse bias was measured as plotted in Fig. 3.22. A relatively high bias of 12 V is necessary to obtain a phase shift of 2π because the phase shifters are shorter than conventional electrooptical phase shifters. There is a significant efficiency difference between TE and TM polarization states since the linear electrooptic effect (Pockels) is inactive for TM-polarized light, whereas it is active for TE-polarized light in waveguides oriented in $[0\bar{1}1]$ direction [20]. The nonlinear dependence of phase shift on voltage in TM polarization state is attributed to the lack of linear electrooptic effect.

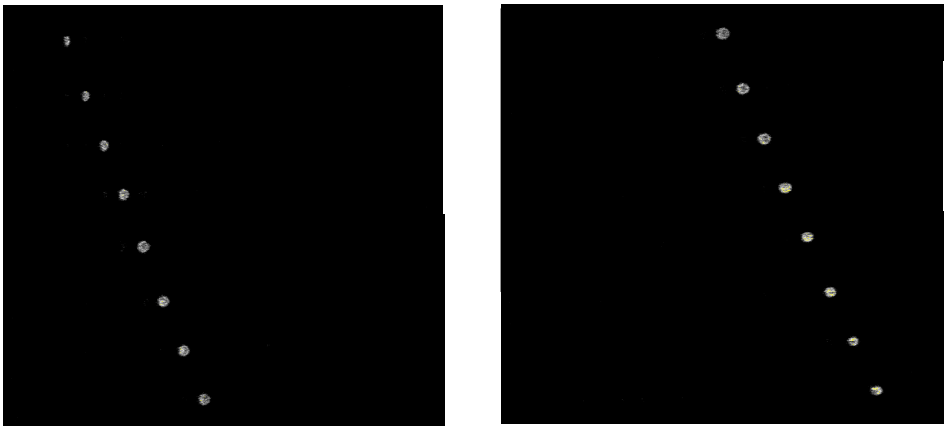


Fig. 3.23 Near-field images at the output plane of the 1×16 switch. Left column: State 1 – State 8 from top to bottom. Right column: State 9 – State 16 from top to bottom.

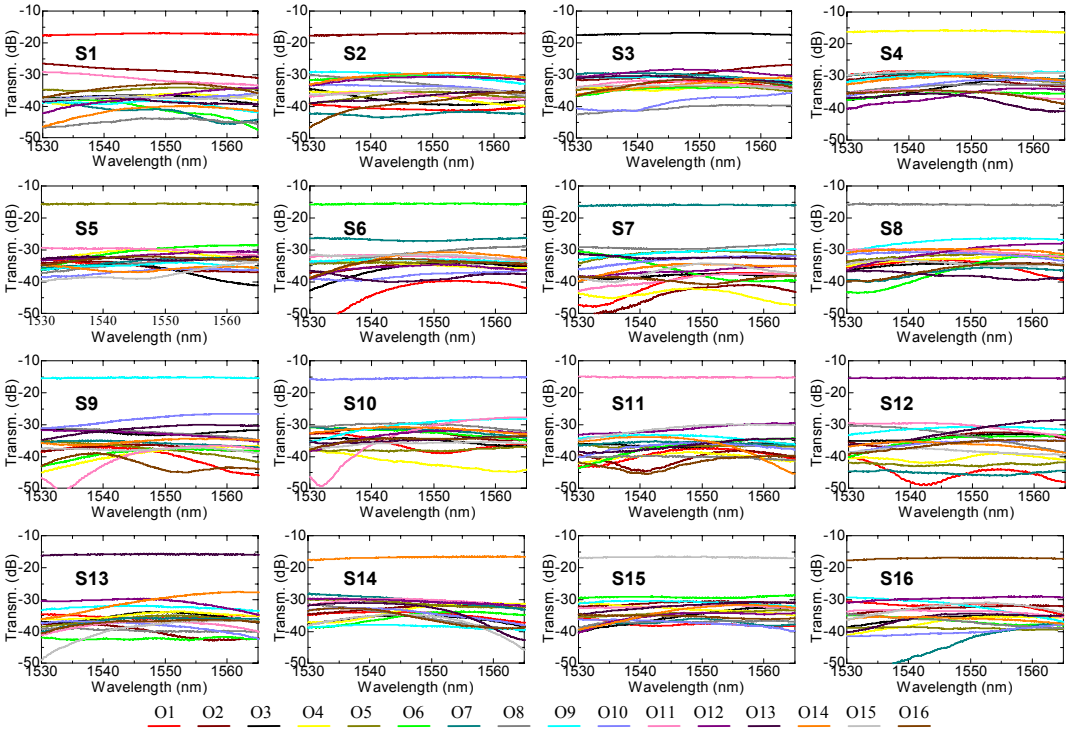


Fig. 3.24 Wavelength dependence of fiber-to-fiber transmittance measured at Outputs 1-16 (O1-O16) in States 1-16 (S1-S16). The transmittance spectra were averaged over bands of 100 pm for clarity.

Static switching was demonstrated using a combination of the electrooptic and carrier-induced phase modulation mechanisms with TE-polarized signal. The voltages applied to the phase shifters were between -10V and +1.5V. The substrate temperature

was maintained at 20ºC with the help of a thermo-electric cooler throughout the measurements. The near-field images in Fig. 3.23 display the beam deflection to all the 16 ports at the output successfully. A complete quantitative characterization of insertion loss and extinction ratio was carried out in the *C*-band (1530-1565 nm). Fig. 3.24 presents the wavelength dependence of fiber-to-fiber transmittance at the output ports. In all the states, the wavelength dependence of the transmitted power is below 0.8 dB in the entire *C*-band. At the wavelength of 1550 nm, the static extinction ratio has an average value of 18.6 dB. The minimum extinction ratio is observed at Output 9 (S9/S8) and is equal to 11.3 dB. The fiber-to-fiber loss is between 15.1 dB (S11) and 17.0 dB (S1), out of which approximately 10 dB is estimated to be due to the fiber coupling. The on-chip loss was cross-checked from the Fabry-Perot oscillation in the transmitted power spectrum caused by the lack of anti-reflection coating on the facets. Fig. 3.25 shows the fiber-to-fiber transmittance spectrum at an output as an example. The peak-to-valley ratio of these oscillations is above 1.5 dB, from which the on-chip loss is calculated to be less than 7 dB in all of the switching states. The on-chip loss reduced by 11 dB compared to the previous switch as a result of the modified fabrication process. The maximum power nonuniformity among output ports is 1.9 dB.

As the final static characterization, the power penalty was measured with a 40-Gb/s-NRZ binary sequence. The experiment setup is identical to the setup used for the characterization of the 1×8 switch. The BER graphs at Outputs 1, 9, and 16 are

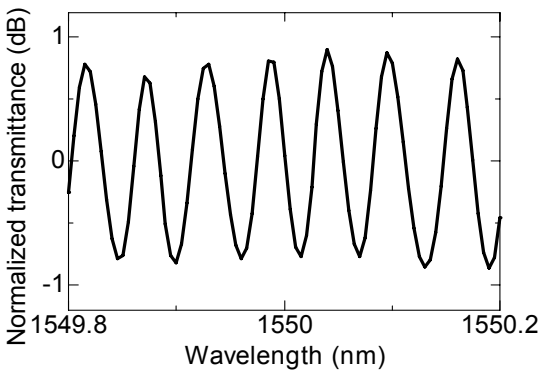


Fig. 3.25 Normalized transmittance spectrum to Output 9 in State 9. The oscillations are caused by reflections at the input and output facets and the low on-chip loss.

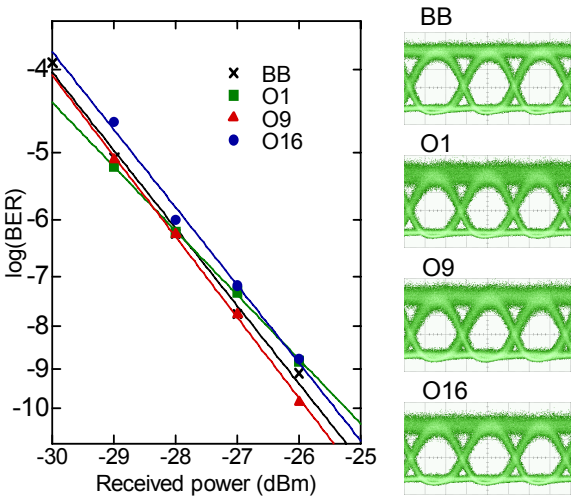


Fig. 3.26 BER versus received power at the "on" outputs in States 1, 9, and 16 compared to the back-to-back configuration. The eye diagrams are available on the right hand side.

available in Fig. 3.26. Outputs 1 and 16 were chosen because they demonstrate the highest insertion loss as expected theoretically. Among all the measured ports, the power penalty is less than 0.4 dB at a BER of 10^{-9}. The eye diagrams have clear openings, which is consistent with the low power penalty. The effect of Fabry-Perot oscillations on the eye diagrams is visible although it is small. This can be avoided by anti-reflection coating and tilted waveguides at the input and output facets.

Complete dynamic operation of an integrated InP phased-array switch was demonstrated for the first time with this device. The dynamic operation of this switch necessitates a switch driver circuit with at least 24 dynamically reconfigurable analog voltage outputs. The driver was implemented with a field-programmable gate array (FPGA). The switch controller is described schematically in Fig. 3.27. The basic operating mechanism of the switch controller is as follows. The voltage settings of the 16 states are saved in a look-up table in digital domain. For this particular switch, the dimensions of the look-up table are 16×24. The look-up table is filled initially after finding the switching conditions and it does not have to be updated if the environmental conditions are stable. At the input of the switch controller, there are a number of comparators that read the digital signals representing the state number. For example, a 4-bit signal of "1010" corresponds to State 10. After identifying the designated port with

the comparators, the digital bit sequence corresponding to that state is read from the look-up table. This bit sequence is converted to an analog voltage with the help of a digital-to-analog converter (DAC). In this particular case, the output of DAC is amplified to the desired bias voltage value. All these operations are implemented dynamically after each arrival of address bits. A photograph of the switch and the switch controller during dynamic measurement is available in Fig. 3.28. Three FPGAs are programmed, each responsible for eight phase shifters. Miniature coaxial cables were used in order to transport the AC voltages to the printed circuit board (PCB), which was connected to the phase shifters via bond wires.

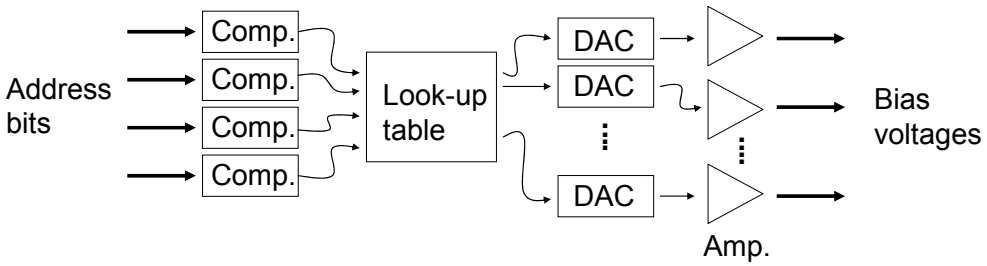


Fig. 3.27 Schematic diagram of the switch controller. Comp: comparator.

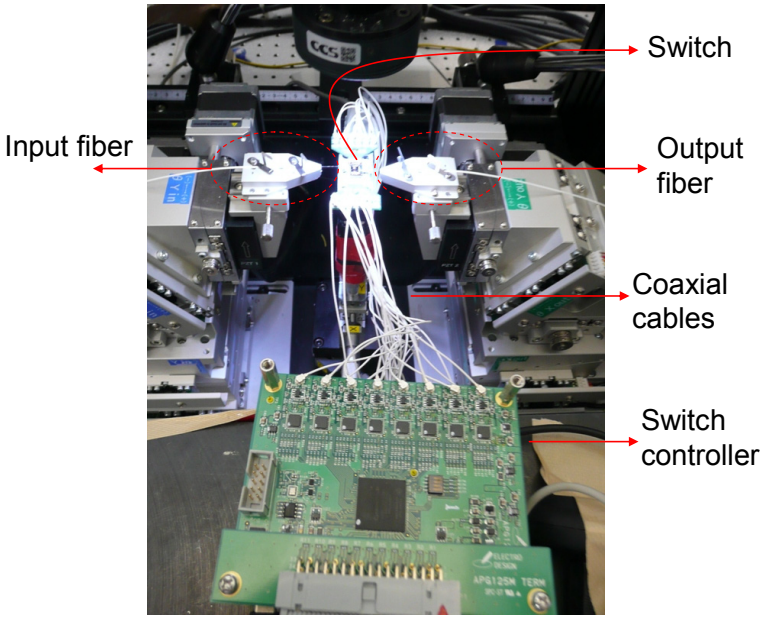


Fig. 3.28 Photograph of the switch and the switch controller during dynamic operation.

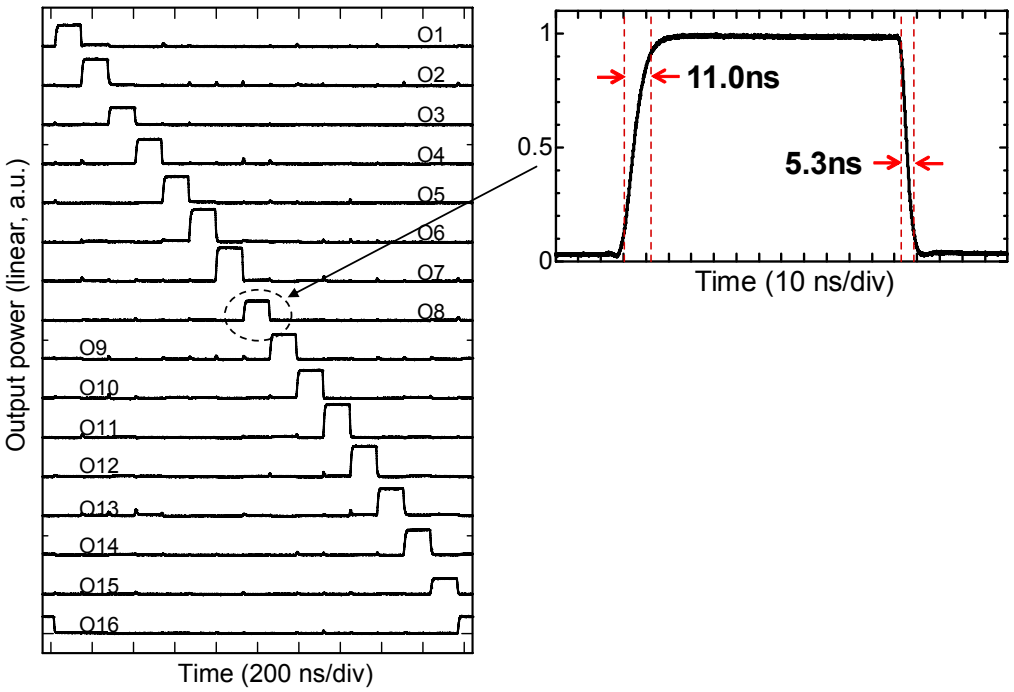


Fig. 3.29 Temporal waveforms of output power as the switching state changes from 1 up to 16 sequentially. A zoomed view of State 7-8-9 transition at Output 8 is available on the right hand side.

The operating conditions were derived by using the iterative algorithm explained in Section 3.2.3.2. The bias voltages were saved in the look-up table with a resolution of 2 mV. Next, the dynamic performance of the device was tested with a scenario in which continuous-wave (CW) light was switched to all the output ports dynamically. Fig. 3.29 displays the power measured at the outputs in temporal domain while the switching state changes from 1 up to 16 sequentially with a clock period of 130 ns. Dynamic switching to all the ports was succeeded. Although a sequential case is presented here, similar performance was observed with arbitrary orders of switching states. The minimum dynamic extinction ratio was equal to 10.9 dB among all outputs. Under some circumstances, the transient values of bias voltages lead to a temporary increase of output power at some outputs, which causes an undesired crosstalk. However, this phenomenon has limited impact in a typical OPS application with sufficient guard times.

In the inset of Fig. 3.29, a zoomed image of the waveform at Output 8 is shown

during the transition between States 7, 8, and 9. The rise time (10% - 90%) is approximately 11 ns, whereas the fall time (90% - 10%) is 5.3 ns. The difference between the fall and rise times can be explained by the nonlinear relationship between the output power and the bias voltage. On the leading edge (i.e. during the increase of optical power), the output power stays considerably lower than its final value until all bias voltages are approximately equal to their final values. The output power does not increase significantly until the end of electrical transition. On the trailing edge, the power drops at the beginning of the electrical transition because the phase conditions are distorted. Therefore, the transient time of the bias voltages is at least on the order of 6 ns. This is a cumulative effect of both the slow response of DACs and FPGAs and the electrical parasitics. The bond wires to the electrodes on the chip are a few mm long, which causes a relatively high inductance. In addition to the electrical transients, the other mechanism that limits the dynamic response speed is the carrier lifetime. Since carrier-induced phase modulation mechanisms were employed along with electrooptic effects, the lifetime of free carriers in the core layer became a limiting factor. Free carrier lifetime depends on several factors including the carrier density, temperature, crystal quality and surface conditions. For carrier densities comparable to the values in the devices investigated here ($\sim 10^{17}$ cm^{-3} under the condition of carrier injection), the typical free carrier lifetime in InGaAsP is a few ns [21]. Therefore, carrier-induced phase modulation is typically not compatible with response times shorter than 1 ns.

3.3.3 Discussion

The on-chip loss of this switch, which is less than 7 dB, is close to its theoretical value as a consequence of the improved waveguide formation conditions. Nevertheless, the extinction ratio is considerably lower than the theoretical value. Since aberrations in waveguides and star couplers have mostly been eliminated and the waveguides do not support more than two lateral modes, the relatively low extinction ratio should be originating from one or more additional reasons. Electrical and thermal crosstalk between phase shifters is considered as the major reason of low extinction ratio in this device. During the fabrication of this device, no precautions were taken to prevent

electrical crosstalk because the phase shifters were designed for operation in the upper-right quadrant of the I-V diagram. In that case, a resistance of 1 kΩ or even lower does not cause significant crosstalk because of the both low effective device resistance and low voltage under forward bias. However, with reverse bias up to 10 V across the phase shifters, it was experimentally observed that changing the bias condition of one phase shifter influenced the voltage across other phase shifters. Therefore, the phase conditions of arrayed waveguides were not independent from each other. The electrical resistance between phase shifters can be reduced by trenches or ion implantation.

The dynamic response time of the switch affects the guard time in packet switching. The ratio of guard time over packet time cannot be very large since the utilization efficiency is inversely proportional to this ratio. Therefore, the reconfiguration time of the switch influences the packet size indirectly. The reconfiguration time of this device, which is 11 ns, is short enough for typical bit rates and packet lengths. An average IP packet consists of a payload of 10 kilobits [22]. For a bit rate of 40 Gb/s, the length of an average packet is 250 ns, which is more than 20 times longer than the reconfiguration time of this switch. However, guard times even shorter than 1 ps can be demanded to achieve much larger capacities in the future. In that case, electrooptic phase modulation should be preferred to carrier injection and attention should be paid to reduce the effects of electrical parasitics. The switch controller should consist of faster electronic components. There are not any fundamental limitations to reducing the reconfiguration time to sub-ns levels even with the currently available technology.

3.4 CONCLUSION

The design, fabrication and characterization of two phased-array switches were explained in this chapter. The first device, which is the first integrated InP phased-array switch fabricated by dry etching, demonstrated promising properties including low polarization sensitivity and wavelength sensitivity. This device had a serious problem of high optical propagation loss mostly due to the fabrication process. The design and fabrication of the 1×16 switch was modified according to the feedback from these

experiments. This 1×16 switch improved the state of the art in integrated photonic switching in multiple aspects. First of all, it is the first monolithic semiconductor photonic switch with 16 outputs. Second, it reveals an almost perfectly flat spectral response in an ultra wide band exceeding 4.5 THz. The 3-dB bandwidth, which was not measured because of the lack of equipment, is expected to be considerably wider. Another important point is the insertion loss below 7 dB. This on-chip loss is lower than the passive splitter loss in a broadcast-and-select switch, which is theoretically more than 12 dB. Therefore, this device has verified the claimed advantage of phased-array switches over broadcast-and-select switches for the first time. The reduction of optical switch insertion loss is very important for communication system design both to reduce the power dissipated by the amplifiers and to increase the cascadability of the switch through lower amplified spontaneous emission accumulation. Owing to the transparency of the switch, 40-Gb/s NRZ signal has been transmitted with a low penalty, and there are not any fundamental reasons for not increasing the bit rate and changing the modulation format. In addition to these static properties, the complete dynamic operation of the switch was also achieved. Even with low-cost slow electronics, non-optimized electrical wiring and phase shifters partially operating on carrier injection, reconfiguration to all ports was demonstrated in a time scale of approximately 11 nanoseconds. Moreover, degradation of switching performance was not observed compared to the static conditions. These experimental results offer a great potential to deploy phased-array switches for ultra-high-capacity optical packet switching, which is investigated experimentally in the next chapter.

APPENDIX
MEASUREMENT OF PROPAGATION LOSS USING FABRY-PEROT RESONANCE

The intensity of electric field at the output is given by the equation,

$$|E_{out}| = |E_{in}| t_1 \gamma t_2 \left[1 + r_1 r_2 \gamma^2 \, exp(2j\beta L) + \left(r_1 r_2 \gamma^2 \, exp(2j\beta L) \right)^2 + \ldots \right], \quad (3.A.1)$$

where E_{out} is the output field, E_{in} is the input field, t_1 and t_2 are the field transmission coefficients, and r_1 and r_2 are the field reflection coefficients as shown in Fig. 3.A.1. γ is the on-chip field transmissivity in a single propagation, L is the length of the chip, and β is the effective wave number in the waveguide. (3.A.1) is equivalent to

$$\frac{|E_{out}|}{|E_{in}|} = t_1 \gamma t_2 \frac{1}{1 - r_1 r_2 \gamma^2 \, exp(j2\beta L)}. \quad (3.A.2)$$

The minimum and maximum values of $\frac{|E_{out}|}{|E_{in}|}$ correspond to $exp(j2\beta L) = -1$ and $exp(j2\beta L) = 1$, respectively.

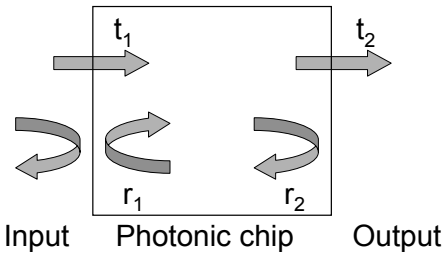


Fig. 3.A.1 Reflection and transmission coefficients in a photonic chip.

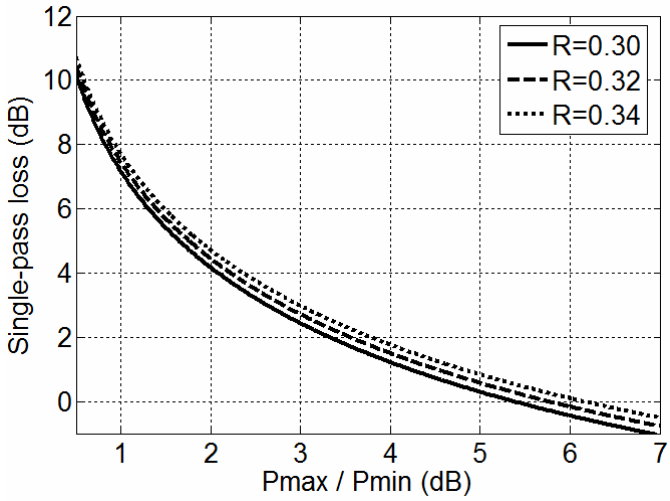


Fig. 3.A.2 Single-pass waveguide propagation loss versus the peak-to-valley ratio of optical power measured at the output. The trend is plotted for three different values of power reflection coefficient, R. The reflection coefficient is assumed to be equal at both facets.

$$\left.\frac{|E_{out}|}{|E_{in}|}\right|_{min} = \frac{t_1 \gamma t_2}{1 + r_1 r_2 \gamma^2} \tag{3.A.3-a}$$

$$\left.\frac{|E_{out}|}{|E_{in}|}\right|_{max} = \frac{t_1 \gamma t_2}{1 - r_1 r_2 \gamma^2}. \tag{3.A.3-b}$$

Therefore, the ratio of the maximum field amplitude to the minimum field amplitude is

$$\frac{|E_{out}|_{max}}{|E_{out}|_{min}} = \frac{1 + r_1 r_2 \gamma^2}{1 - r_1 r_2 \gamma^2} \tag{3.A.4}$$

If we refer to the peak-to-valley ratio of the power as H, then

$$\frac{|E_{out}|_{max}}{|E_{out}|_{min}} = \sqrt{H}\ . \tag{3.A.5}$$

The power transmissivity, Γ is equal to the square of the field transmissivity, γ. If these are substituted into (3.A.4),

$$\sqrt{H} = \frac{1 + r_1 r_2 \Gamma}{1 - r_1 r_2 \Gamma}. \tag{3.A.6}$$

Therefore,

$$\Gamma(dB) = -10 \log\left(\frac{1}{r_1 r_2}\frac{\sqrt{H} - 1}{\sqrt{H} + 1}\right) \tag{3.A.7}$$

is the optical power loss caused by a single propagation from one facet to another. The propagation loss in the waveguide is derived from 3.A.7 and the length of the chip.

$$\alpha\left(\frac{dB}{cm}\right) = -\frac{10}{L} log\left(\frac{1}{r_1 r_2}\frac{\sqrt{H}-1}{\sqrt{H}+1}\right) \tag{3.A.8}$$

In typical InP/InGaAsP waveguides, $r_1 r_2$ is on the order of 0.30-0.35. Fig. 3.A.2 plots the single-pass propagation loss in a photonic chip as a function of the peak-to-valley ratio of optical power and the reflection coefficient.

REFERENCES OF CHAPTER 3

[1] A. Sano, et al., "69.1-Tb/s (432 x 171-Gb/s) C- and extended L-band transmission over 240 km using PDM-16-QAM modulation and digital coherent detection," in Proc. Optical Fiber Communication Conference, 2010, Paper PDPB7.

[2] W. R. Frensley, "Heterostructure and quantum well physics," in Heterostructures and Quantum Devices, P. S. Zory, Jr., Ed. San Diego: Academic Press, 1994, pp. 1-24.

[3] J.-F. Vinchant, J. A. Cavailles, M. Erman, P. Jarry, and M. Renaud, "InP/GaInAsP guided-wave phase modulators based on carried-induced effects: theory and experiment," Journal of Lightwave Technology, vol. 10, no. 1, pp. 63-70, Jan. 1992.

[4] L. Zhang, J. Sinsky, D. Van Thourhout, N. Sauer, L. Stulz, A. Adamiecki, and S. Chandrasekhar, "Low-voltage high-speed traveling wave InGaAsP-InP phase modulator," IEEE Photonics Technology Letters, vol. 16, no. 8, pp. 1831-1833, Aug. 2004.

[5] M. A. Newkirk, B. I. Miller, U. Koren, M. G. Young, M. Chien, R. M. Jopson, and C. A. Burrus, "1.5 μm multiquantum-well semiconductor optical amplifier with tensile and compressively strained wells for polarization-independent gain," IEEE Photonics Technology Letters, vol. 4, no. 4, pp. 406-408, Apr. 1993.

[6] Y. Chen, J. E. Zucker, N. J. Sauer, and T. Y. Chang, "Polarization-independent strained InGaAs/InGaAlAs quantum-well phase modulators," IEEE Photonics Technology Letters, vol. 4, no. 10, pp. 1120-1123, Oct. 1992.

[7] S. John, C. Soukoulis, M. H. Cohen, and E. N. Economou, "Theory of electron band tails and the Urbach optical-absorption edge," Physical Review Letters, vol. 57, no. 14, pp. 1777-1780, Oct. 1986.

[8] B. R. Bennett, R. A. Soref, and J. A. Del Alamo, "Carrier-induced change in refractive index of InP, GaAs, and InGaAsP," IEEE Journal of Quantum Electronics, vol. 26, no. 1, pp. 113-122, Jan. 1990.

[9] J. Chilwell and I. Hodgkinson, "Thin-films field-transfer matrix theory of planar multilayer waveguides and reflection from prism-loaded waveguides," Journal of Optical Society of America A, vol. 1, no. 7, pp. 742-753, Jul. 1984.

[10] H. C. Casey and P. L. Carter, "Variation of intervalance band absorption with hole concentration in p-type InP," Applied Physics Letters, vol. 44, no. 1, pp. 82-83, Jan. 1984.

[11] A. Ghatak and V. Lakshminarayanan, "Propagation characteristics of planar waveguides," in Optical Waveguides: From Theory to Applied Technologies. M. L. Calvo and V. Lakshminarayanan, Ed. Boca Raton: CRC Press, 2007, pp. 25-26.

[12] N. Shimizu, K. Mori, T. Ishibashi, and Y. Yamabayashi, "Quantum efficiency of InP/InGaAs uni-traveling-carrier photodiodes at 1.55-1.7 μm measured using supercontinuum generation in optical fiber," Japanese Journal of Applied Physics, vol. 38, pp. 2573-2576, Apr. 1999.

[13] B. Docter, E. J. Geluk, M. J. H. Sander-Jochem, F. Karouta, and M. K. Smit, "Deep etching of DBR gratings in InP using Cl_2 based ICP processes," in Proc. Symposium IEEE/LEOS Benelux Chapter, 2006,

pp. 97-100.

[14] W. Jiang, N. K. Fontaine, F. M. Soares, J. H. Baek, K. Okamoto, S. J. B. Yoo, F. Olsson, and S. Lourdudoss, “Dynamic phase-error compensation for high-resolution InP arrayed-waveguide grating using electro-optic effect,” in Proc. IEEE Lasers and Electro-Optics Society Annual Meeting, 2008, Paper MF2.

[15] P. Munoz, D. Pastor, J. Capmany, and S. Sales, “Analytical and numerical analysis of phase and amplitude errors in the performance of arrayed waveguide gratings,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 8, no. 6, pp. 1130-1141, Nov./Dec. 2002.

[16] J. E. Schramm, D. I. Babic, E. L. Hu, J. E. Bowers, and J. L. Merz, “Anisotropy control in the reactive ion etching of InP using oxygen in methane/hydrogen/argon,” in Proc. IEEE International Conference on Indium Phosphide and Related Materials, 1994, Paper WE4.

[17] T. R. Hayes, U. K. Chakrabarti, F. A. Baiocchi, A. B. Emerson, H. S. Luftman, and W. C. Dautremont-Smith, “Damage to InP and InGaAsP surfaces resulting from CH_4-H_2 reactive ion etching,” Journal of Applied Physics, vol. 68, no. 2, pp. 785-792, Jul. 1990.

[18] H. C. Neitzert, R. Fang, M. Kunst, and N. Layadi, “CH_4-H_2 reactive ion etching induced damage of InP,” Journal of Vacuum Science and Technology B, vol. 18, no. 6, pp. 2803-2807, Nov./Dec. 2000.

[19] R. G. Walker, “High-speed III-V semiconductor intensity modulators,” IEEE Journal of Quantum Electronics, vol. 27, no. 3, pp. 654-667, Mar. 1991.

[20] J.-F. Vinchant, J. A. Cavailles, M. Erman, P. Jarry, and M. Renaud, “InP/GaInAsP guided-wave phase modulators based on carrier-induced effects: theory and experiment,” Journal of Lightwave Technology, vol. 10, no. 1, pp. 63-70, Jan. 1992.

[21] A. Sugimura, “Band-to-band Auger recombination effect on InGaAsP laser threshold,” IEEE Journal of Quantum Electronics, vol. QE-17, no. 5, pp. 627-635, May 1981.

[22] R. S. Tucker, “The role of optics and electronics in high-capacity routers,” Journal of Lightwave Technology, vol. 24, no. 12, pp. 4655-4673, Dec. 2006.

CHAPTER 4
HIGH-BIT-RATE OPTICAL PACKET SWITCHING EXPERIMENTS

4.1 INTRODUCTION

OPS is the major potential application of phased-array switches. OPS is a demanding technology, which is the reason that research on optical switches is still active after several years of research. Although the basic static and dynamic performance of phased-array switches presented in Chapter 3 is promising, it does not guarantee compatibility with OPS. The effect of crosstalk and loss on the bit-error rate (BER), limits of packet size and guard time, the influence of payload bit rate and modulation format on performance, and compatibility with labeling schemes are technical points to be investigated before these devices become a serious candidate for packet switching.

In order to answer these questions, a simplified OPS node was constructed from a phased-array switch, a switch controller and an all-optical label extractor. Especially to verify the compatibility with different modulation formats, two types of packets carrying 160-Gb/s optical time-domain multiplexed (OTDM) on-off keying (OOK) and 120-Gb/s wavelength-division multiplexed (WDM) differential phase-shift keying (DPSK) payloads were routed. Optical in-band parallel labels were attached to the packets to encode the address information. The experiments were carried out in both 1×8 and 1×16 configurations to observe the influence of port count on the performance of the OPS node.

Section 4.2 introduces the packets employed in the experiments. Section 4.3 gives information on the OPS node and Section 4.4 presents the OPS experiments along with

their results. The conclusion of this chapter is in Section 4.5.

4.2 LABELING SCHEME AND PAYLOAD

An optical packet consists of two functional pieces, namely the payload and the label (header). Payload is the data carried by the packet, and the label consists of the necessary information to transport the data to the destination successfully. The size of the payload depends on the application. The majority of Internet Protocol (IP) packets used in conventional E/O/E networks are inside a range spanning from 40 bytes up to 1500 bytes, whereas more than half of the traffic is carried in packets of 1500 bytes or larger [1,2]. The label, which consists of approximately 40 bits [3], is typically considerably smaller than the payload. Therefore, the label can be transmitted at a bit rate much lower than that of the payload, and label processing in the electronic domain is much less power hungry than data processing. As a natural consequence, a scheme based on label processing in the electronic domain and transparent data switching in the optical domain has emerged. In this way, the maturity of electronic signal processing and the data capacity of transparent optical switching are utilized simultaneously.

There are several different ways of attaching labels to optical packets. They can be classified into two types as serial and parallel labels. Serial labels are serial to the payload in the time domain. The extraction of this type of labels requires strict control of timing, which is difficult for especially asynchronous and variable-length packets. Relatively complicated envelope detection circuits are necessary to extract these labels [4]. On the other hand, parallel labels share the same time interval with the payload. The label is located on a separate wavelength, frequency, modulation format or code to maintain the label and payload as separate from each other. Wavelength multiplexed labeling uses exactly the same method as WDM, and labels are separated from the payload with the help of optical filters [5]. In some applications, labels are distinguished from the payload in frequency domain inside the same wavelength channel. Subcarrier multiplexing is an example of this scheme [6,7]. These labels can also be separated with the help of optical filters. Another technique is based on modulating the label and payload with orthogonal modulation formats [8-10]. In real systems, it is difficult to

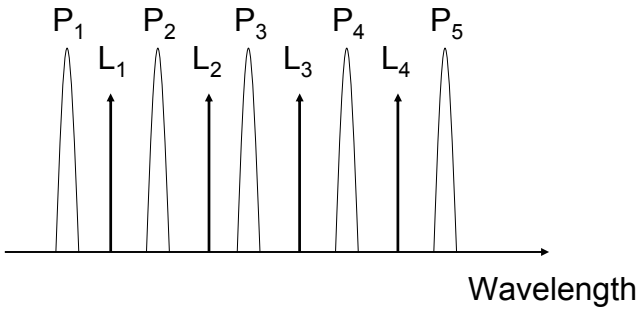


Fig. 4.1 Schematic spectral distribution of WDM payload (P_i) and in-band parallel labels (L_i).

prevent coupling between the payload and label because of nonidealities. Optical codes, which are used in optical code-division multiple-access (O-CDMA) networks, are also utilized to encode and decode optical labels [11].

Wavelength-multiplexed labels were employed in the OPS experiments reported in this chapter. These are parallel in-band labels, which have two differences from conventional wavelength-multiplexed labels. In one packet duration, only one bit is represented in a wavelength channel; and the labels are located inside the payload spectrum. The single-bit-per-channel approach has the advantage of removing serial-to-parallel conversion from the label extractor. In addition to that, in-band labeling offers efficient utilization of the spectrum [12]. Although parallel labeling seems to be inefficient due to the number of separate channels required, the number of bits is limited in label swapping applications, where the labels carry local information [13]. To denote a maximum number of N output ports in a node, $log_2(N)$ parallel labels are employed. For example, ten label bits are sufficient to represent 1024 different addresses. Moreover, if the labels are located between WDM payload channels as in Fig. 4.1, multiple label channels do not impose significant impairments. As demonstrated in the experimental section, even if the labels are completely inside the spectrum of a wideband payload, the penalty can be maintained small with proper label extraction.

Two types of payload were routed in the OPS experiments. In-band parallel labels were attached to 160-Gb/s return-to-zero (RZ) OOK and 120-Gb/s WDM DPSK payloads in separate experiments. The 160-Gb/s payload was obtained by time-multiplexing sixteen 10-Gb/s data streams, which were generated by modulating 10-GHz pulse trains from a mode-locked fiber laser (MLFL). The optical pulses have a

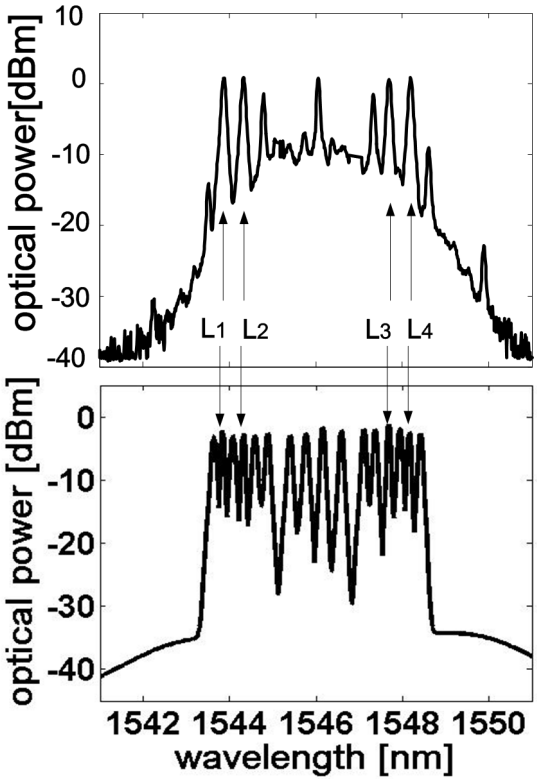


Fig. 4.2 Spectra of 160-Gb/s OTDM-OOK (upper) and 120-Gb/s WDM-DPSK (lower) packets with 4 in-band parallel labels. .

full-width at half-maximum (FWHM) of 1.5 ps and a 20-dB spectral width of 5 nm around the peak wavelength of 1546 nm. The second type of packet consists of 12 DPSK-modulated 10-Gb/s non-return-to-zero (NRZ) channels with wavelengths between 1543.7 nm and 1548.5 nm (50 GHz spacing). Four in-band parallel labels are located at wavelengths of 1543.9, 1544.3, 1547.7, and 1548.2. The labels are completely inside the 20-dB bandwidth of the OOK payload and between the WDM channels of the DPSK payload. The spectra of two types of packets are displayed in Fig. 4.2.

4.3 OPS NODE SUBSYSTEM

The OPS node consists of three building blocks, namely the label extractor, optical switch and the switch controller. A schematic diagram of the OPS node is available in Fig. 4.3. The label extractor separates the labels from the payload by filtering and sends

them to the switch controller after optical-to-electrical (O/E) conversion. According to the address information encoded in the labels, the switch controller reconfigures the state of the optical switch. During label processing, the payload propagates in a fiber delay line to adjust the timing of switch reconfiguration and arrival of the payload at the input of the switch. The payload propagates through the switch without any processing and exits the output determined by the switch controller according to the label. Note that the label rewriting function is excluded in this work for simplicity.

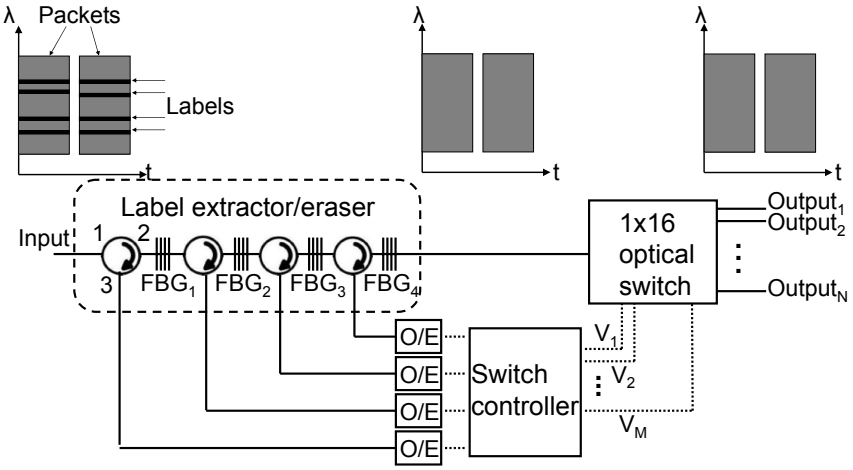
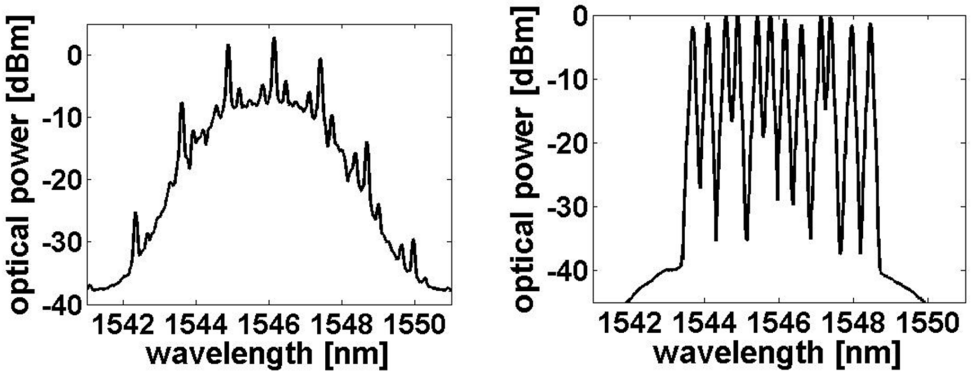


Fig. 4.3 Schematic diagram of the OPS node subsystem. FBG: fiber Bragg grating.



(a) (b)

Fig. 4.4 Spectra of (a) 160-Gb/s OTDM-OOK and (b) 120-Gb/s WDM-DPSK packets after label extraction.

Label extraction/erasure is achieved using a cascade of fiber Bragg gratings (FBGs), whose reflection peaks match the wavelengths of respective label bits. This label extractor is completely passive, which is an advantage of parallel labeling. Even under the condition of complete spectral coverage of labels by the payload, the penalty caused by spectral filtering is suppressed to below 0.6 dB owing to the narrow bandwidth of FBGs, which is approximately 6 GHz [14]. The packet spectra after label extraction are shown in Fig. 4.4.

Integrated phased-array switches described in Chapter 3 were employed as the optical switch. The switch controller used in the dynamic switching experiments in Chapter 3 was also used in this subsystem without a significant modification. The readers are referred to the relevant chapter for detailed information on these components.

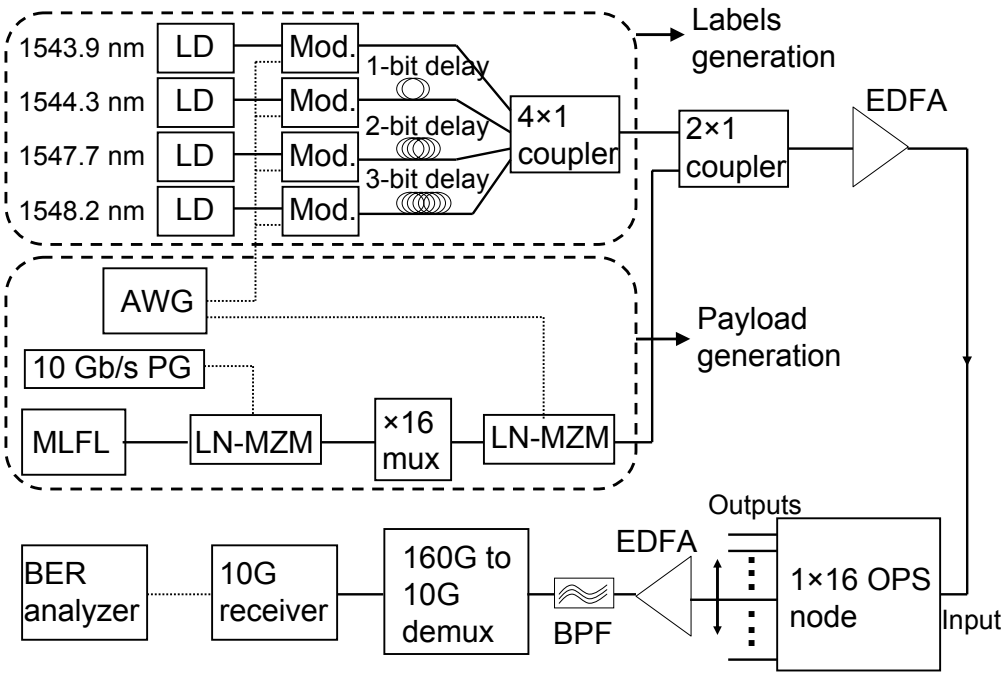
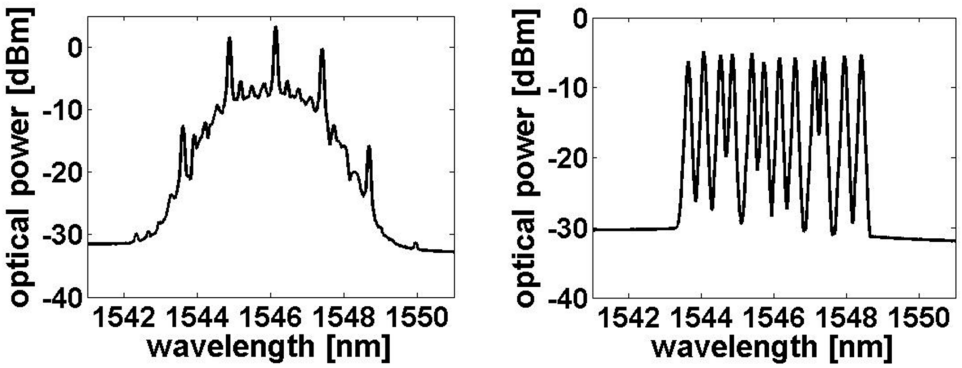


Fig. 4.5 Experimental setup of 160-Gb/s 1×16 OPS subsystem. Optical and electrical connections are represented by solid and dashed lines, respectively. (AWG: arbitrary waveform generator; PG: pattern generator; LN-MZM: LiNbO3 Mach-Zehnder modulator; mux: multiplexer; EDFA: Erbium-doped fiber amplifier; BPF: optical band-pass filter; demux: demultiplexer).

4.4 EXPERIMENTAL SETUP AND RESULTS

The experimental setup used with the OTDM-OOK packets is shown in Fig. 4.5 schematically. The setup for the DPSK packets is identical to this except payload generation section. The payloads described in Section 4.2 were modulated with a 1792-bit-long user-defined pattern based on 2^7-1 pseudo-random binary sequence (PRBS). Both payloads were modulated at a bit rate of 10 Gb/s before time-domain and wavelength-domain multiplexing. The OOK packet was modulated with a lithium niobate ($LiNbO_3$) Mach-Zehnder amplitude modulator, whereas a commercial DPSK modulator was used for the other type of packets. After multiplexing, the binary streams were gated by another $LiNbO_3$ Mach-Zehnder modulator to form the packets. 147.2-ns-long packets were separated by 32-ns-long guard times. The modulator used for gating was controlled by an arbitrary waveform generator (AWG). The parallel labels were generated by modulating the output of wavelength-tunable continuous-wave (CW) laser diodes. All label bits were modulated with the same bit pattern and shifted with respect to each other by using optical fiber delay lines. The parallel labels were first coupled to each other and then coupled to the payloads with passive optical couplers. The coupling loss was compensated for by an erbium-doped fiber amplifier (EDFA). These packets were routed by the 1×16 OPS node, amplified by an EDFA again, and filtered to eliminate out-of-band amplified spontaneous emission (ASE). Finally, the payload was demultiplexed to the bit rate of 10 Gb/s before reception and BER analysis. The OTDM payload was demultiplexed by using two cascaded electroabsorption modulators, whereas the WDM-DPSK payload was demultiplexed with a tunable optical filter. Demodulation of the DPSK signal was implemented by using a one-bit-delay Mach-Zehnder interferometer.

The optical power of each extracted label was approximately -20 dBm and the average power at the input of the switch was 7 dBm. The polarization state was maintained as TE at the switch input. Throughout the experiments, the substrate temperature of the switch was maintained at 18ºC for stability. The spectra of packets at the output of the OPS node are given in Fig. 4.6. The switch does not influence the spectrum because of its flat response and the absence of nonlinear distortion. An

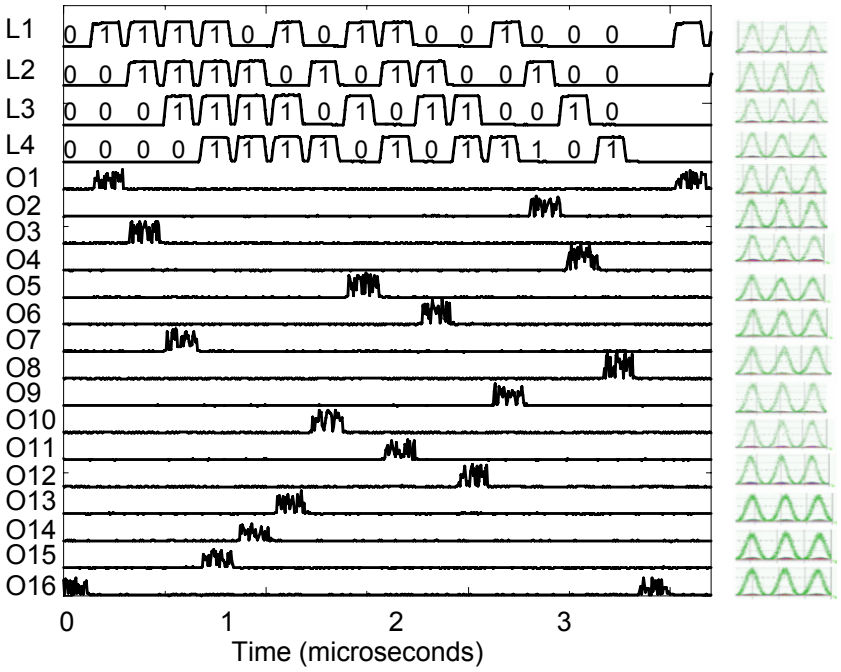


(a) (b)

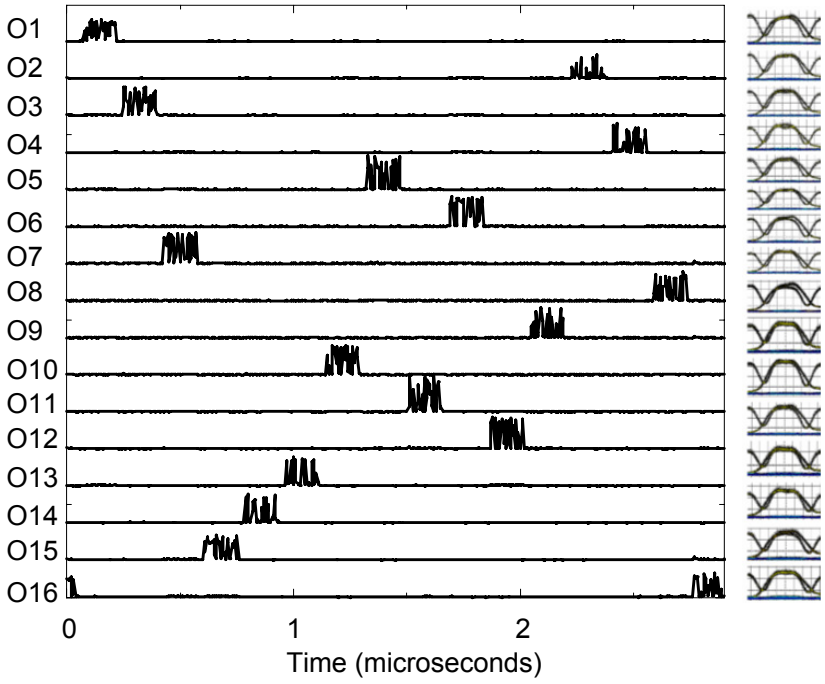
Fig. 4.6 Spectra of (a) 160-Gb/s OTDM-OOK and (b) 120-Gb/s WDM-DPSK packets after switching.

increase is observed in the noise floor level because of the EDFA noise. The bandwidth of the 160-Gb/s signal became slightly narrower because of the optical filters used after EDFAs.

The labels were organized in time domain so that a packet was routed to each output port in an interval of N packets, where N is the number of outputs. The waveforms at the outputs were monitored without any manipulation in the experiment setup. Fig. 4.7-a presents the time-domain waveforms and eye diagrams of dynamically switched 160-Gb/s OTDM-OOK packets at the outputs (O1-O16) of the 1×16 OPS node. The input waveforms of labels (L_1-L_4) are also plotted in the same figure. These waveforms indicate that the packets were switched autonomously to the destination address represented by "$L_4L_3L_2L_1$." Note that labels from "0001" to "1111" directly represent the port number of the switch, whereas Port 16 is encoded by "0000". The minimum dynamic extinction ratio is between 11.0 dB and 13.3 dB among the 16 output ports. The data traces of WDM-DPSK packets are also available in Fig. 4.7-b. The spikes observed at the transitions during the dynamic characterization of the switch (Section 3.3.2) are not visible in these graphs because the transient regions are covered by the guard time. The eye diagrams of routed packets after demultiplexing are also displayed in the same figure. The eye diagrams of DPSK packets belong to the channel at a wavelength of 1544.1 nm, which is the most sensitive to distortion by label extraction because it is spectrally located between two labels.

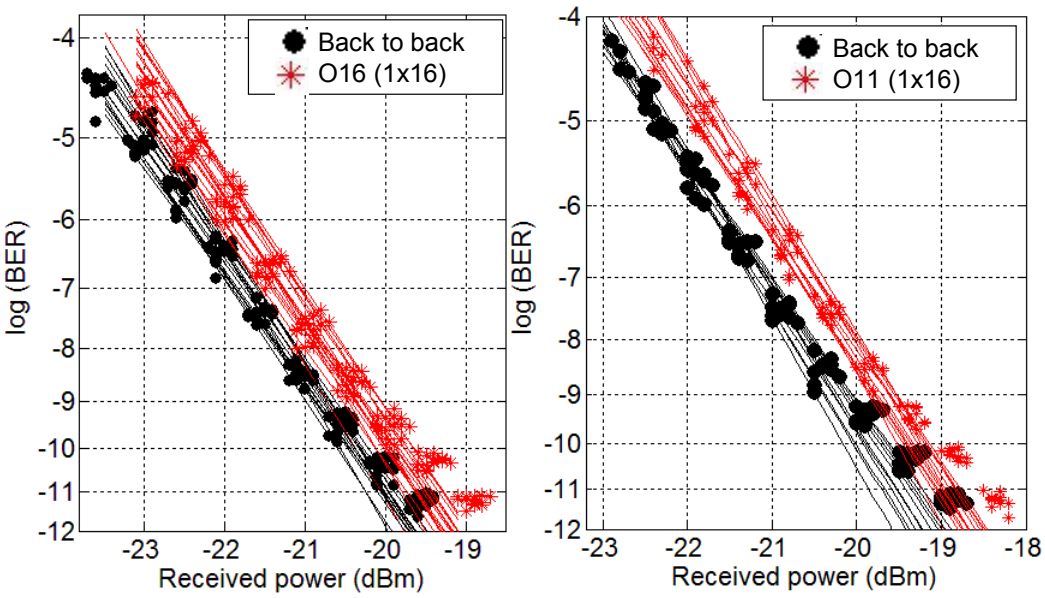


(a)



(b)

Fig. 4.7 Output waveforms with (a) 160-Gb/s OTDM-OOK, and (b) 120-Gb/s WDM-DPSK packets. The eye diagrams on the right side belong to output ports with indices increasing from top to bottom. L_1-L_4: Label 1 – Label 4.



(a) (b)

Fig. 4.8 BER vs. received power for (a) OTDM-OOK, and (b) WDM-DPSK packets compared with the BER vs. received power in back-to-back condition.

Next, the BER of routed channels was measured. The BER measurement could not be carried out with the configuration shown in Fig. 4.7 because such a switching pattern would cause a very low duty ratio and was not compatible with the electronic bandwidth limitation of the receiver circuit. Therefore, a condition of two-state switching, where the packets were switched alternatingly between two output ports, was tested. Packets were routed between the ports with the lowest extinction ratios in order to measure the maximum power penalty. Fig. 4.8 shows the BER characteristics of the demultiplexed packets measured under the dynamic switching condition. To allow fair comparison with the back-to-back case, the received power of the switched packets was derived by adding 3 dB to the measured average power. At the ports with the lowest extinction ratio, error-free packet switching was achieved with a power penalty of 0.7 dB for the OTDM-OOK packets and 0.6 dB for the WDM-DPSK packets at the BER of 10^{-11}.

Finally, in order to investigate the effect of the port count on the packet switching characteristics, a 1×8 node subsystem was also configured and the same measurements

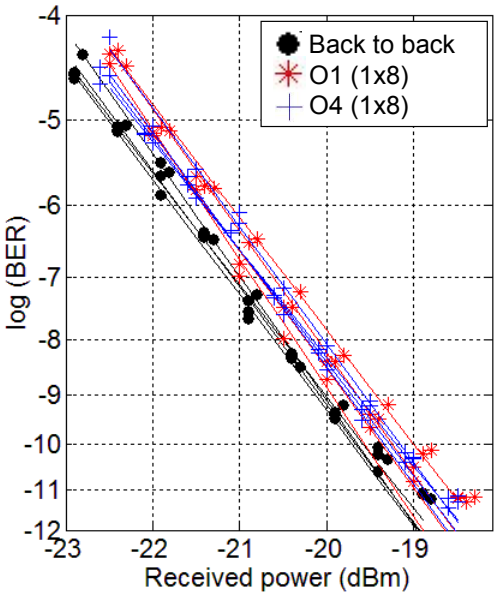


Fig. 4.9 BER vs. received power in a 1×8 OPS node.

were carried out with 160-Gb/s OTDM-OOK packets. A 1×8 switch with 12 electrodes fabricated on the same InP wafer as the 1×16 switch was employed for switching. Three label wavelengths at 1544.3, 1547.7, and 1548.2 nm were used to encode the address. Similar results were obtained, such as the maximum on-chip loss of approximately 7 dB, dynamic extinction ratio of 10.3-12.3 dB, and a power penalty of 0.5 dB. The measured BERs for the 1×8 subsystem are plotted in Fig. 4.9.

4.5 CONCLUSION

The OPS node subsystem described in this chapter proved its capability of label processing and packet routing in all the experiments. 160-Gb/s OTDM RZ-OOK and 120-Gb/s WDM NRZ-DPSK data packets were successfully routed by label extraction and switch reconfiguration without any manual control. The performance of the subsystem was evaluated in both 1×8 and 1×16 configurations. All these experiments with different bit rates, modulation formats, and numbers of physical connections were completed with successful low-power-penalty switching. We consider these results as significant for optical communications research because a number of difficult tasks have

been realized simultaneously. The number of switching ports was increased up to 16 without any degradation of performance, in spite of the fact that most OPS demonstrations in the literature are small scale. Both phase- and amplitude-modulated packets with large data capacities were switched with very similar power penalties, which requires strict transparency in a wide spectral band. Label extraction was succeeded by completely passive components without any necessity of synchronization. The bit rates, port counts, and guard time in these experiments are far from physical limits considering the 1-dB bandwidth of phased-array switches exceeding 4 THz, theoretical analyses stating that the switch can be scaled up to at least tens of ports without trading off basic characteristics, and the possibility of reducing the reconfiguration time to sub-nanosecond levels.

REFERENCES OF CHAPTER 4

[1] B.-Y. Choi, S. Moon, Z.-L. Zhang, K. Papagiannaki, C. Diot, “Analysis of point-to-point packet delay in an operational network,” in Proc. IEEE INFOCOM, 2004, vol. 23, no. 1, pp. 1798-1808.

[2] S. Yao, B. Mukherjee, S. J. B. Yoo, and S. Dixit, “A unified study of contention-resolution schemes in optical packet-switched networks,” J. Lightwave Technol., vol. 21, no. 3, pp. 672-683, Mar. 2003.

[3] S. J. B. Yoo, “Optical packet and burst switching technologies for the future photonic internet,” Journal of Lightwave Technology, vol. 24, no. 12, pp. 4468-4492, Dec. 2006.

[4] Z. Hu, R. Doshi, H.-F. Chou, H. N. Poulsen, D. Wolfson, J. E. Bowers, and D. J. Blumenthal, “Optical label swapping using payload envelope detection circuits,” IEEE Photonics Technology Letters, vol. 17, no. 7, pp. 1537–1539, Jul. 2005.

[5] A. Okada, “All-optical packet routing in AWG-based wavelength routing networks using an out-of-band optical label,” in Proc. Optical Fiber Communication Conference, 2002, vol. 1, pp. 213–215.

[6] C. L. Lu, M. Sabido, P. Poggiolini, R. T. Hofmeister, and L. G. Kazovsky, “Cord-A WDMA optical network—Subcarrier-based signaling and control scheme,” IEEE Photonics Technology Letters, vol. 7, no. 5, pp. 555–557, May 1995.

[7] E. Park and A. E. Willner, “Self-routing of wavelength packets using an all-optical wavelength shifter and QPSK subcarrier routing control headers,” IEEE Photonics Technology Letters, vol. 8, no. 7, pp. 938–940, Jul. 1996.

[8] V. Olmos, I. T. Monroy, F. M. Huijskens, and A. M. J. Koonen, “In-band time-to-live signaling system for combined DPSK/SCM scheme in OLS,” IEEE Photonics Technology Letters, vol. 16, no. 10, pp. 2386–2388, Oct. 2004.

[9] J. J. V. Olmos, I. T. Monroy, Y. Liu, M. G. Larrode, J. Turkiewicz, H. J. S. Dorren, and A. M. J. Koonen, “Asynchronous, self-controlled, all-optical label and payload separator using nonlinear polarization rotation in a semiconductor optical amplifier,” Optics Express, vol. 12, no. 18, pp. 4214–4219, Sep. 2004.

[10] C. W. Chow, C. S. Wong, and H. K. Tsang, “Optical packet labeling based on simultaneous polarization shift keying and amplitude shift keying,” Optics Letters, vol. 29, no. 16, pp. 1861–1863, Aug. 2004.

[11] N. Wada, H. Harai, and F. Kubota, “Optical packet switching network based on ultra-fast optical code label processing,” IEICE Trans. Electron., vol. E87C, no. 17, pp. 1090–1096, Jul. 2004.

[12] N. Calabretta, H.-D. Jung, E. Tangdiongga, and H. Dorren, “All-optical packet switching and label rewriting for data packets beyond 160 Gb/s,” IEEE Photonics Journal, vol. 2, no. 2, pp. 113-129, Apr. 2010.

[13] D. J. Blumenthal, “Optical packet switching,” in Proc. Lasers and Electro-Optics Society Annual Meeting, 2004, vol. 2, pp. 910–912.

[14] N. Calabretta, Wenrui Wang, T. Ditewig, O. Raz, F. Gomez Agis, S. Zhang, H. de Waardt, H.J.S.

Dorren, “Scalable optical packet switches for multiple data formats and data-rates packets,” IEEE Photonics Technology Letters, vol. 22, no. 7, pp. 483-485, Mar. 2010.

CHAPTER 5
PHOTONIC INTEGRATED CIRCUIT FOR 100-PORT MONOLITHIC SWITCHING

5.1 INTRODUCTION

The switches introduced in Chapter 3 are important for proof of concept and detailed characterization, but switches of that scale do not have sufficient capacity potential for the future packet switching routers. If router capacities on the order of 100 Tb/s or higher are targeted, at least 100 fiber connections are needed at the input and output even with 1 Tb/s WDM packets. The implementation of advanced photonic integrated circuits (PIC) capable of such large-scale switching is very important for the future of OPS because this technology is very unlikely to replace electronic switching unless large-scale photonic integration of functional elements in the router is achieved. The present state of integrated photonic switches is far from this goal, so considerable effort has to be put on both device and photonic integration research. Besides the phased-array switches presented in Chapter 3, switches with the highest level of integration reach up to 16 ports at most [1,2].

This chapter focuses on the experimental work on an advanced photonic integrated circuit for switching to up to 100 output ports monolithically. A two-stage cascade of 1×10 switches has been preferred for energy efficiency and easier control of the device. Semiconductor optical amplifiers (SOA) have been attached at the output ports in order to improve the extinction ratio and compensate for the optical loss. The motivations of this project are closing the gap between state of the art in photonic switching and requirements, and contributing to the know-how on photonic integration with a chip

comprising hundreds of components. Section 5.2 describes the design of the PIC, which is different from the design of devices in Chapter 3. Section 5.3 explains the fabrication process, which has been modified to implement the advanced functionalities of the PIC. The characterization results are presented in Section 5.4 before the conclusion in Section 5.5.

5.2 DESIGN OF THE PIC

5.2.1 Design of General Architecture

A cascaded scheme has been employed in order to reach the large port count with smaller number of phase shifters to control at a time. Similar to switches based on tree architecture that consist of 1×2 switches, the two-stage cascade comprises ten 1×10 switches attached at the outputs of a 1×10 switch. Therefore, there are eleven 1×10 switches, ten of which are in the second stage, whereas a single switch is in the first stage. The advantage of this approach is explained as follows. In a single-stage $1\times N$ switch, there are $AOR \cdot N$ phase shifters, where AOR refers to the array-to-output ratio. If this $1\times N$ switch is constructed as a two-stage cascade with equal size in the first and second stages, only $2\,AOR \cdot \sqrt{N}$ phase shifters have to be operated at a time since it is sufficient to operate only one switch in the first and second stages separately. In this specific case, the number of phase shifters that consume power reduces to one fifth by preferring two stages to a single stage.

Another modification in the general design is integrating SOAs at the output waveguides. The schematic diagram describing the PIC is available in Fig. 5.1. SOAs

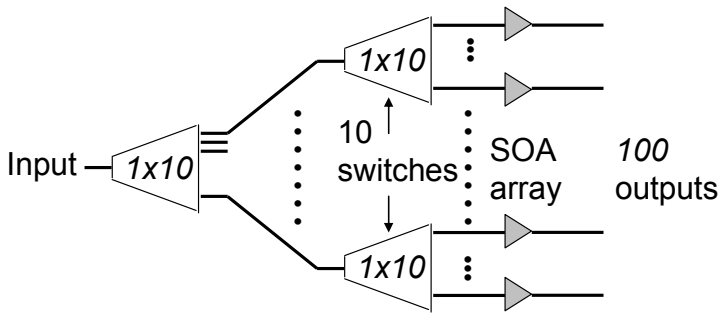


Fig. 5.1 Schematic diagram of the two-stage monolithically integrated 1×100 switch with integrated SOAs.

are absorptive devices when they are not biased because of their low bandgap energies. They supply gain under the condition of population inversion maintained by current injection. Among the 100 SOAs in the PIC, current is injected to only one device at a time. The extinction ratio increases because of the gain in the output with a forward-biased SOA and the absorption in the other outputs.

5.2.2 Active/Passive Integration

This PIC comprises passive and active photonic devices, which have different epitaxial designs. SOAs require bandgap energies smaller than or equal to photon energy in the core, whereas the difference between the bandgap energy and the photon energy has to be sufficient to maintain low propagation loss in passive waveguides. Special integration methods have to be employed to fabricate this kind of PICs. Selective area growth [3], butt-joint regrowth [4], offset quantum well [5], dual quantum well [6], and quantum well intermixing [7] are among the most common active-passive integration techniques. A very brief review of active/passive integration schemes is given next. For better understanding, Fig. 5.2 presents the schematic cross sections of material stacks with different active/passive integration schemes [8].

Selective area growth is based on patterning a dielectric mask (usually SiO_2 or Si_3O_4) on the substrate before the growth. Both material composition and growth rate of compound semiconductors depend on the size and proximity of the mask. As a

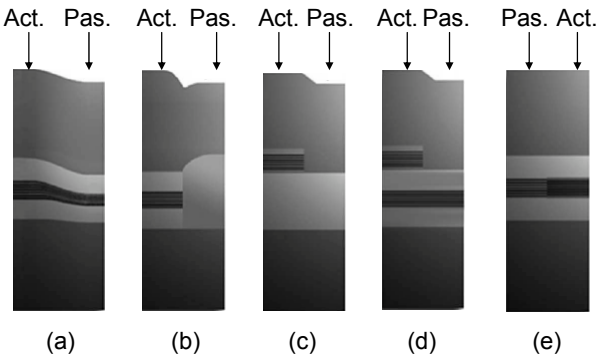


Fig. 5.2 Schematic cross sections of active and passive photonic devices fabricated by using (a) selective area growth, (b) butt-joint regrowth, (c) offset quantum well, (d) dual quantum well, (e) quantum well intermixing (after [8]).

consequence, the bandgap energy of quantum wells can be engineered via mask design. The advantage of this method is single growth, which both reduces the cost and increases the yield. However, all devices on the chip consist of the same epitaxial structure, which limits the flexibility. Moreover, active/passive transition is not very sharp.

In butt-joint regrowth scheme, some regions of the wafer are etched after growth. The epitaxial structure of etched regions is completed after the following growth(s). This etching and growing cycle can be repeated several times. The merit of this technique is the ability to grow optimized structures for different components. The disadvantages are the difficulty of achieving high-quality interfaces between active and passive regions and the inefficiency of multiple-growth process.

In offset quantum well scheme, a multiple quantum well (MQW) layer is grown above the bulk core layer initially. In passive regions, the MQW and cladding layers are etched and a bulk cladding layer is grown. The active devices operate through the overlap of the waveguide mode with the MQW layer. Simplicity is the biggest advantage of this scheme. However, its flexibility is even less than that of selective-area growth. Moreover, the active devices are relatively inefficient because they rely on the small overlap with the offset MQW layer. Dual quantum well is a special version of offset quantum well with an MQW layer in the center of the core layer in addition to the offset MQW. With dual quantum well scheme, in addition to the problems observed with offset quantum well technique, passive waveguides have a high propagation loss because of the MQW inside the core layer.

In quantum well intermixing, the wafer is grown with the longest band-edge wavelength in the PIC. Later, the regions where shorter wavelengths are required are exposed to a special treatment to blur the boundaries of wells and barriers by inter-diffusion of elements. This can be done by irradiation of high power laser, thermal annealing or ion bombardment. This method is simple to implement and more flexible than the double quantum well and offset quantum well methods. However, the reduction of quantum well quality is a drawback for some applications. Another disadvantage is being limited to a single epitaxial design similar to selective area growth.

Offset quantum well method has been preferred as the active/passive integration

scheme to fabricate the switch. Offset quantum well method is suitable for this particular PIC for multiple reasons. In addition to the aforementioned simplicity of process, low overlap of waveguide modes with the offset quantum wells, which is usually undesired with active devices, is an advantage in this configuration because low modal overlap leads to high output saturation power [9]. Offset quantum well technique is compatible with designs in which high SOA gain is not necessary. The bulk guiding layer is preferred to MQW to achieve low propagation loss in passive waveguides. Fig. 5.3 shows a more detailed schematic cross section of active and passive devices fabricated with offset quantum well technique. The implementation of offset quantum well technique is explained in the section that summarizes device fabrication.

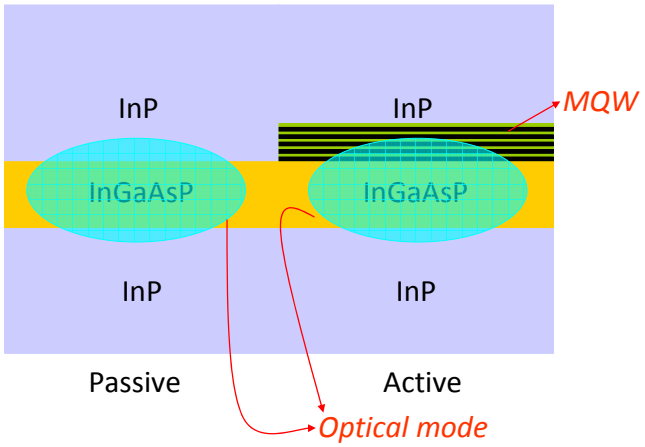


Fig. 5.3 Schematic cross sections of active and passive InP/InGaAsP photonic devices fabricated with offset quantum well method.

5.2.3 Design of Epitaxial Structure

The three major parameters strongly affected by epitaxial design are the propagation loss in passive waveguides, efficiency of phase shifters, and extinction ratio of SOAs. It is impossible to optimize all of these parameters simultaneously since there are a number of trade-offs as explained next. The most important design parameters are the bandgap energy and thickness of the quaternary layer and the dimensions and quantity of quantum wells.

Since the previously fabricated devices, which comprised a Q1.3 layer in the core,

suffered from low phase shifter efficiency, the bandgap energy of the quaternary layer was modified. As a natural result of Kramers-Kronig relations, the efficiency of carrier injection-based refractive index change increases as the bandgap energy gets closer to photon energy [10]. Nevertheless, the absorption also increases as the energy difference reduces. The absorption tail below bandgap energy is modeled exponentially as follows [11].

$$\alpha = \alpha_0 \, exp\left(\frac{E - E_0}{\gamma} \right), \tag{5.1}$$

where α_0 is the absorption coefficient at the absorption edge and γ is a constant defining the rate of absortion reduction with energy difference. For InGaAsP, α_0 and γ are on the order of 3000 cm-1 and 10 meV respectively. The absorption coefficient as a function of wavelength was calculated according to the relation in (5.1). Finally, Q1.37 was decided to be employed as the guiding layer since the estimated absorption coefficient of 0.53 dB/cm is tolerable.

The thickness of Q1.37 layer was optimized next. In this case, the mode overlap with MQW was also accounted for in addition to the efficiency of phase shifters and the absorption coefficient. The modulation of effective refractive index of a waveguide mode depends on the modulation of guiding layer refractive index, Δn_{guide}, and the confinement factor, Γ.

$$\Delta n_{eff} = \Gamma \cdot \Delta n_{guide} . \tag{5.2}$$

Around the free carrier concentration levels in the guiding layer, which is approximately 10^{17} cm^{-3}, the dependence of refractive index modulation on carrier concentration can be assumed to be linear, i.e.

$$\Delta n_{guide} \propto N , \tag{5.3}$$

where N is the free carrier concentration. The steady-state free carrier concentration under carrier injection is given by

$$N = \frac{I\tau}{twL} , \tag{5.4}$$

where I is the injected current, τ is the free carrier lifetime, t is the thickness of Q1.37 layer, w is the width of the waveguide and L is the length of the phase shifter. The free

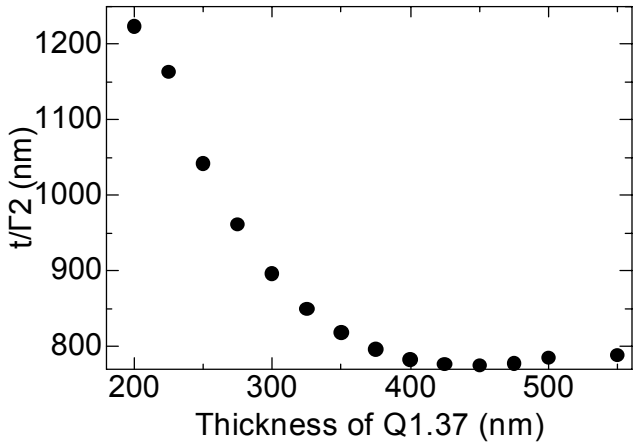


Fig. 5.4 t/Γ^2 versus thickness of the quaternary layer.

carrier lifetime depends on the carrier concentration. Auger recombination can be ignored with the carrier concentration level aforementioned. Assuming that spontaneous emission is the only recombination mechanism, free carrier lifetime is inversely proportional to the carrier density.

$$\tau \propto \frac{I}{N}. \tag{5.5}$$

Therefore,

$$N^2 \propto \frac{I}{twL}. \tag{5.6}$$

From (5.2), (5.3) and (5.6), the relation between refractive index modulation and current is derived as

$$\Delta n_{eff} \propto \Gamma \left(\frac{I}{twL} \right)^{1/2}. \tag{3.1}$$

In order to maximize the efficiency of phase modulation, the ratio, t/Γ^2 has to be minimized. The thickness, t, is a design parameter and Γ increases as t increases. This ratio was calculated as a function of the thickness of the quaternary layer by using the transfer matrix method and plotted in Fig. 5.4. As expected, the efficiency is very low if the guiding layer is very thin, which leads to a low confinement factor. On the other

hand, a guiding layer that is too thick requires high current injection because of the large volume to be filled. Therefore, there is an optimal point with high enough confinement ratio and small enough volume. This optimal point is observed at a thickness of 425 nm in this particular case. However, it is apparent from Fig. 5.4 that in a broad range of thicknesses in the 350-550 nm range, the efficiency is close to the peak value. The guiding layer should not be thicker than 550 nm since it supports higher order modes.

The propagation loss in passive waveguides also depends on the thickness of the quaternary layer because the overlap of the optical mode with the cladding layer reduces as the guiding layer becomes thicker. Fig. 5.5 plots the sum of the loss in the p-InP cladding layer and the Q1.37 guiding layer under the assumption that there is a 250-nm-thick undoped InP between these two layers. The absorption coefficient in p-InP is assumed to be 10 cm^{-1} [12]. The absorption reduces as the quaternary layer thickness increases because of the lower overlap with the p-InP layer.

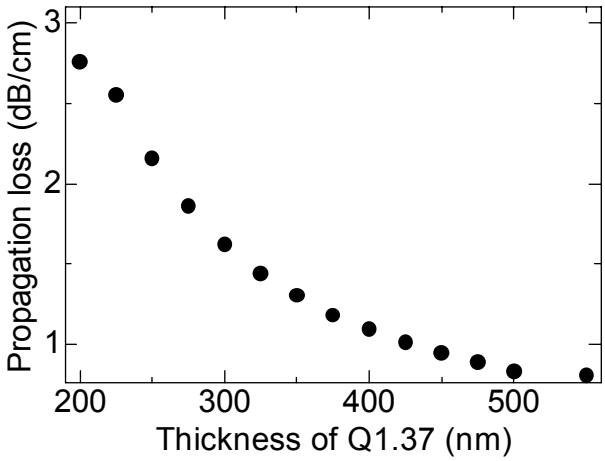


Fig. 5.5 Propagation loss due to absorption in p-InP cladding and Q1.37 guiding layers as a function of the thickness of the guiding layer.

If the efficiency of phase shifters and propagation loss were the only important parameters, it would be logical to choose a thickness in 400-500 nm range. However, the extinction ratio of SOAs is another parameter depending on the thickness of the quaternary layer. The quantum wells were designed to obtain an emission edge at a wavelength of 1.55 μm. The InGaAs/InGaAsP (Q1.25) wells and barriers were designed

to be 8-nm wide, which was experimentally confirmed to lead to an emission edge at the desired wavelength. The wells were designed to have a compressive strain of 0.4% in order to optimize the gain in TE state of polarization. Fig. 5.6 shows the overlap of fundamental waveguide mode with MQW as a function of the thickness of the guiding layer. The calculation was done for cases of 7 and 6 quantum wells. It is not beneficial to increase the number of quantum wells further because the penalty of larger volume to be filled is dominant over the increase of mode overlap. After an overall evaluation of Fig. 5.4-Fig. 5.6, the thickness of the guiding layer was decided to be 350 nm and the MQW was decided to consist of 7 quantum wells and 8 barriers width a width of 8 nm each. Under these conditions, the estimated absorption loss in passive waveguides is 1.3 dB/cm and the overlap of optical mode with the MQW is 7.5%. The final design of the epitaxial stack before regrowth is indicated in Table 5.1. The 12-nm-thick undoped InP above the guiding layer serves as the etch stop layer during the etching of MQW in the passive regions. The 200-nm-thick InP at the top protects the MQW layer in the active regions during the processing before the regrowth.

5.2.4 Design of Phased-Array Switches

The phased-array switches in the second stage of the cascade were modified because of the existence of the SOAs at the output. The extinction ratio of these switches does not have to be very high since the SOAs improve this parameter. According to analytical calculations, a high array-to-output ration (AOR) is mostly necessary to increase the extinction ratio. The insertion loss does not increase abruptly even if the AOR is less than 1.5. Therefore, the number of phase shifters was reduced in order to reduce the footprint, power consumption and complexity of operation. The number of phase shifters in the second-stage switches was set to 12. This corresponds to an AOR of 1.2, which is significantly lower than the usual value of 1.5 or higher. The major mechanism that increases the loss in switches with small AOR is the truncation of the diffracted light at the input of the arrayed waveguides. Because of the small number of arrayed waveguides, a significant portion of the diffracted light does not couple to the waveguide modes. This phenomenon also increases the effects of mode distortion at the

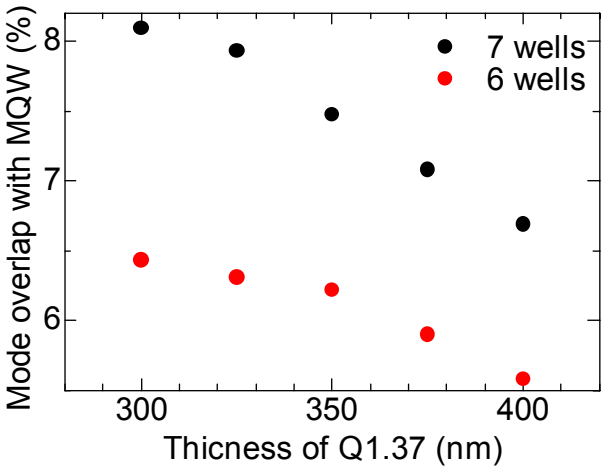


Fig. 5.6 Overlap of the fundamental waveguide mode with the MQW consisting of 7 or 6 wells.

TABLE 5.1

EPITAXIAL DESIGN OF THE PIC BEFORE REGROWTH

DEFINITION	Thickness (nm)	Doping (cm^{-3})
u-InP	200	N/A
u-Q1.25	20	N/A
MQW (7 wells, 6 barriers, 0.4% compressive wells)	7×8+6×8	N/A
u-Q1.25	20	N/A
u-InP	12	N/A
n-Q1.37	350	N/A
n-InP	200	5×10^{17}
n-InP	substrate	$>1\times10^{18}$

output plane, which both contributes to loss and crosstalk. The solution of this problem is shortening the star couplers. However, the second star coupler cannot be shortened freely due to the free spectral range (FSR) limitation. Therefore, the first star coupler was shortened without modifying the length of the second one. Normally, this causes a widening of optical mode proportional to L_2/L_1 at the output plane. Nevertheless, up to a certain value of L_2/L_1, mode widening has less severe impacts on the loss and crosstalk

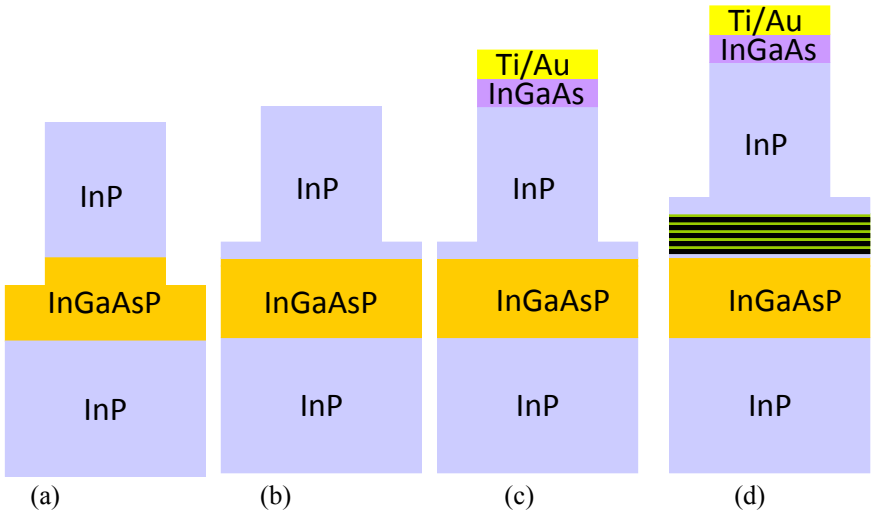
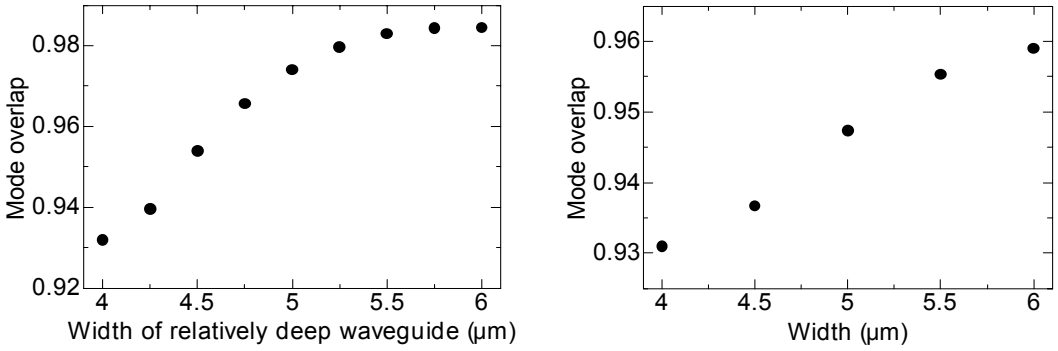


Fig. 5.7 Four different types of waveguides in the PIC. (a) Relatively deeply etched passive waveguide, (b) shallowly etched passive waveguide, (c) phase shifter, (d) SOA.

than distortion. After a comparative evaluation, the following design parameters were found to be optimum. The lengths of the first and second star coupler were 100 and 135 μm respectively. All waveguides at the intersections of star couplers were 2-μm wide. The array pitch was 2.5 μm and the output pitch was 2.55 μm. The worst theoretical values of optical loss and extinction ratio were 4.3 dB and 22.0 dB respectively. The switch in the first stage of the cascade consisted of 15 arrayed waveguides. Its first and second star couplers were 110 and 135 μm respectively. The array and output pitch values were identical to the values of the second stage switches. The estimated worst loss and extinction ratio were 3.7 dB and 31.2 dB respectively. Therefore, the penalty of reducing AOR from 1.5 to 1.2 is 0.6 dB in terms of the loss and more than 9 dB in terms of the extinction ratio. This deteriorated extinction ratio was planned to be compensated for by using the SOAs.

5.2.5 Design of PIC Layout

The single-step etching process applied during the fabrication of the switches explained in Chapter 3 was not preferred in this PIC. A scheme based on shallow and deep waveguides for certain functions was preferred in order to minimize the propagation



(a) (b)

Fig. 5.8 (a) Mode overlap between a 4-μm-wide shallow waveguide (etched until 200 nm above the Q1.37 layer) and a deeper waveguide (50 nm of Q1.37 layer is etched) which have different widths, (b) mode overlap between shallow and deep waveguides having equal widths at the intersection.

loss and the footprint simultaneously. Long straight waveguides were designed as shallowly etched waveguides with loose optical confinement, which have lower propagation loss than deeply etched waveguides. On the other hand, comparatively deeply etched waveguides were employed at the bends to reduce the radius of curvature. The phase shifters and SOAs were designed as shallowly etched waveguides in order to mitigate the degradation of electrical characteristics caused by the dry etching process. Schematic profiles of four different types of waveguides in the PIC, namely shallowly etched waveguides, relatively deeply etched waveguides, phase shifters and SOAs, are shown in Fig. 5.7. The waveguide in Fig. 5.7-a is not really a deeply etched waveguide because the guiding layer is mostly or completely etched in deeply etched waveguides. The reason of stopping the etching at the top of the guiding layer is to prevent higher order modes in 2-μm-wide waveguides and suppress the propagation loss caused by sidewall roughness. These waveguides are referred as “deeply etched” in this dissertation for simplicity. The photonic circuit layout was designed based on these waveguide types. A commercial software based on the three dimensional beam propagation method (BPM) was used for the following simulations.

The number of modes supported by the waveguides was calculated as a function of the etching depth. 2-μm-wide waveguides support two modes if the etching is shallower than the top 100 nm of the quaternary layer. Although it would be better to support only the fundamental mode, two-mode waveguides are also acceptable because

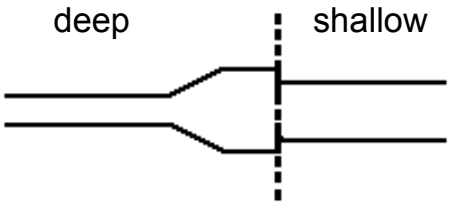


Fig. 5.9 Low-loss interface between a deep and a shallow waveguide.

the coupling ratio to the first-order mode is very low as a consequence of the mode shape. The roughness-based propagation loss increases dramatically as the waveguide width reduces [13], so a two-mode waveguide was preferred to a single-mode lossy waveguide. 5-μm-wide waveguides support only the fundamental mode if etching is stopped 200 nm above the quaternary layer. However, very shallow etching is not good in terms of isolation of devices from each other. Especially the p-doped InP cladding layer, which is 250 nm above the quaternary layer, is quite conductive. Considering that uncertainties of etching depth can be on the order of 50-100 nm on the sample, the final etching depth was set as 150 nm above the quaternary layer.

The optical modes in shallow and deep waveguides have different sizes as a natural result of the different degrees of confinement. The intersections between these two types of waveguides have to be carefully designed to prevent high coupling losses. The highest mode overlap is achieved if the deeply etched waveguide is wider than the shallow waveguide as plotted in Fig. 5.8-a. In principle, such a transition can be implemented with the help of a taper as in Fig. 5.9. However, aligning the deep-shallow waveguide interface exactly at that point is not practical with contact lithography. Therefore, the widths of deep and shallow waveguides have to be equal at the intersection. This case was also simulated and plotted in Fig. 5.8-b. The coupling loss reduces as the shallow and deep waveguides become wider. The width of waveguides at the intersection was set as 5 μm.

The radiation loss of bends was also simulated for different radii of curvature. According to the simulations, the radius of curvature can be reduced to as small as 150 μm, which has a radiation loss less than 0.1 dB. However, the minimum radius of curvature was set as 200 μm as a margin for uncertainty of etching depth. At the intersections, straight waveguides and bends were offset from each other in transverse

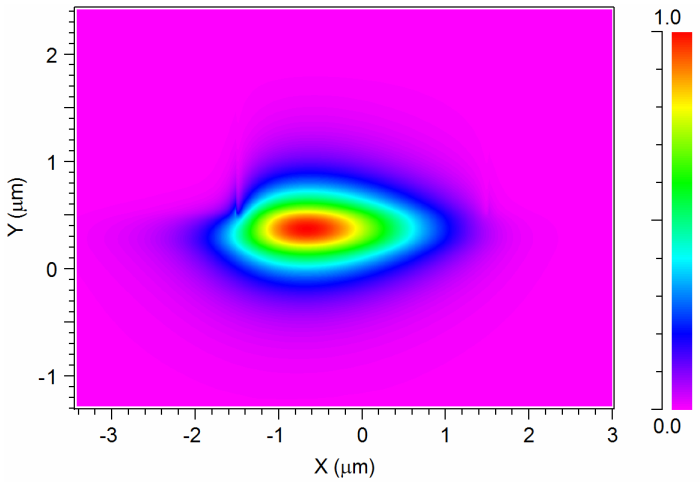


Fig. 5.10 Electric field amplitude of the fundamental mode in a 3-μm-wide bend with a radius of 200 μm (x axis is horizontal and y axis is vertical).

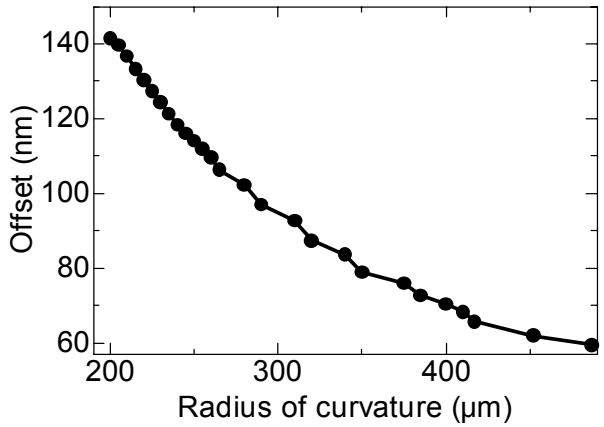


Fig. 5.11 Fundamental mode offset in a 2-μm-wide waveguide (top 75 nm of Q1.37 layer is etched) as a function of the radius of curvature.

direction in order to maximize coupling to the fundamental mode. The optical modes in bends are distorted in shape and shifted towards the outer region of the bend. The mode profile of a bend calculated by using 3D-BPM is shown in Fig. 5.10 as an example of this phenomenon. The amount of shift and distortion depend on the etching depth and the radius of curvature. In general, smaller radius of curvature leads to larger shift and distortion. Shallowly etched waveguides suffer from this more severely than deeply etched waveguides. Since the fundamental mode of symmetrical straight waveguides is

centered at the geometrical center of the waveguide, the straight waveguide and the bend have to be offset. The offset of waveguides deployed in the PIC was calculated for radii of curvature in the 200-500 nm range. The result is displayed in Fig. 5.11.

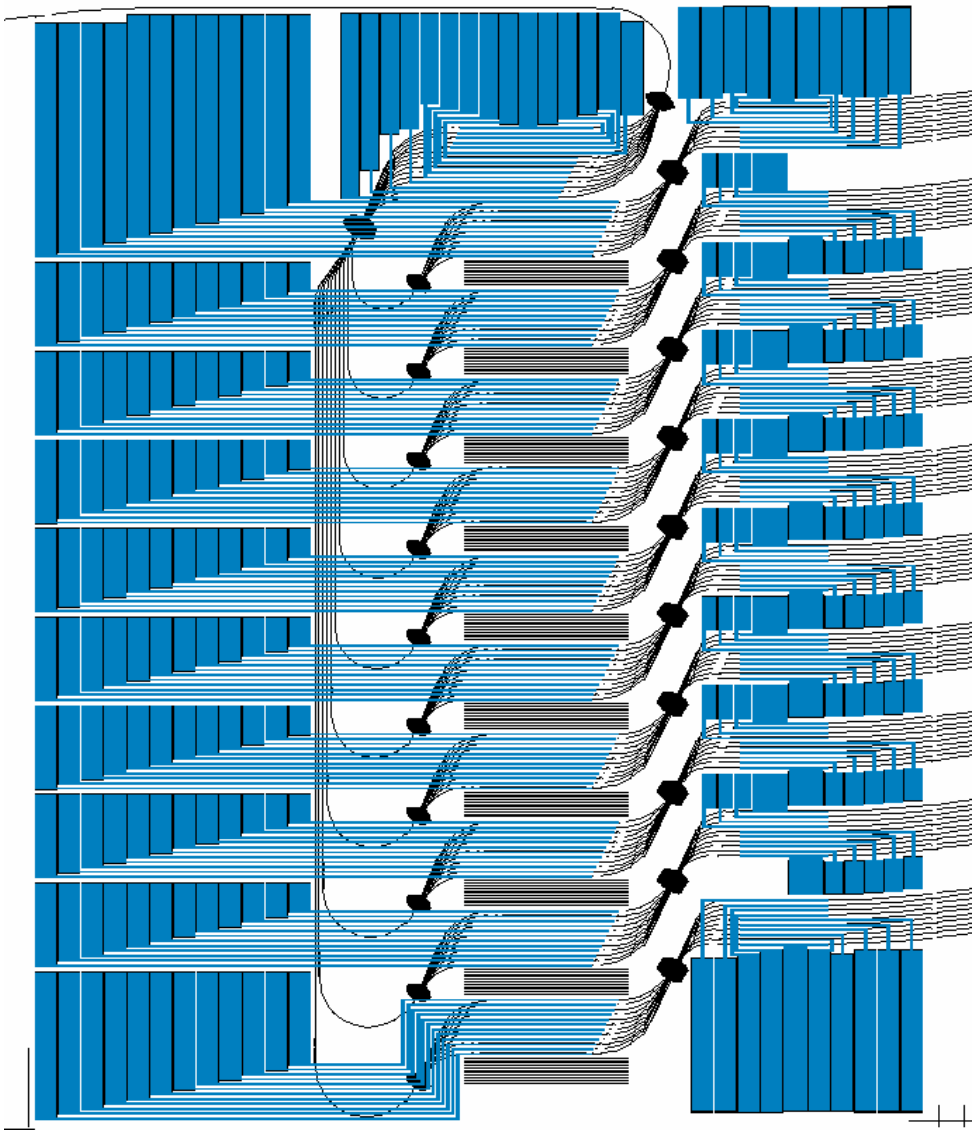


Fig. 5.12 Waveguide and electrode layouts of the 1×100 switching PIC (black: waveguide, blue: electrodes).

Facet-normal waveguides were not preferred at the input and outputs of the PIC because the reflected light couples back to the waveguide perfectly in this configuration.

In addition to the wavelength-dependent fiber-to-fiber loss caused by Fabry-Perot resonance, there is a probability of lasing due to SOA gain, which is not desired in this PIC. A simple way of eliminating the negative effects of reflection is tilted incidence on the facets. The waveguides were tilted by 7º both at the input and output facets. With this angle of incidence, the reflected light does not couple to waveguide modes. Similarly, the interface between active and passive regions was tilted by 7º.

The switches were located on the chip in a configuration to minimize the footprint and average optical path length. The layouts of photolithography masks for waveguide and electrode patterning are available in Fig. 5.12. Although very large electrodes are not good in terms of capacitance, the electrode pads were designed as large as possible in this PIC in order to increase the yield of wire bonding. The output waveguides were located with a pitch of 30 μm, which is the pitch of our spot size converter planar lightwave circuit used for simultaneous multi-port coupling [14]. Dummy waveguides were inserted between the array sections of phased-array switches in order to improve the uniformity of contact opening process. The final dimensions of the PIC are 6 mm × 6.5 mm, a significant portion of which is occupied by the electrodes.

5.3 FABRICATION OF THE PIC

The fabrication process explained in Chapter 3 had to be modified for this PIC. The two major differences are the additional steps for the offset quantum well active/passive integration and the two-step waveguide etching. The fabrication process of the PIC until waveguides formation is displayed in Fig. 5.13. The first step is the active/passive lithography that defines the regions with and without MQW layers. After the lithography, the cladding and MQW in the passive regions were removed using chemical etching techniques (Fig. 5.13-b). First, InP cladding layer was selectively etched by using an H_3PO_4 : HCl (3:1) solution. In this process, HCl was the material doing the etching and H_3PO_4 was used to make the process more controllable by increasing the viscosity. Next, the MQW was etched by using H_2SO_4 : H_2O_2 : H_2O (1:1:5) solution at a temperature of 5ºC. Previous experiments in our laboratory revealed that if the regrowth is done after this step, there is a discontinuity between the

active and passive epitaxial stacks because of the undercut that occurs during wet chemical etching. This phenomenon is shown schematically in Fig. 5.14. Another chemical treatment was added in order to prevent this problem. After removing the photoresist completely, the sample was treated in H_2O : HBW : HBr solution for 4 minutes. This solution etches both InP and InGaAsP isotropically, so makes the sidewall of the active region smoother. Later, InP was etched everywhere on the sample by using H_3PO_4 : HCl solution. This was followed by a treatment in H_2SO_4 to clean the surface and a treatment in buffered hydrofluoric acid (BHF) to remove the oxides on the surface. The sample was rinsed in deionized water between treatments. These pre-regrowth processes are very important since they directly influence the quality of regrowth.

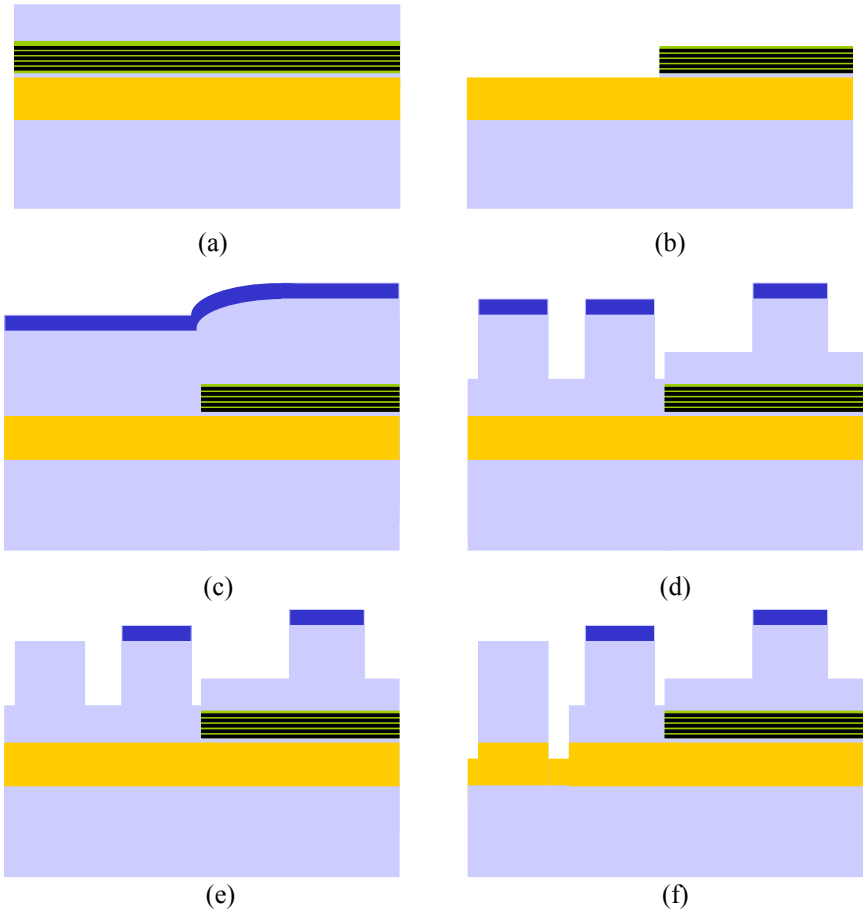


Fig. 5.13 Fabrication process of the PIC until the end of waveguide etching. (a) unprocessed wafer, (b) after cladding layer and MQW are etched in the passive regions, (c) after regrowth, (d) after the first-step waveguide etching, (e) after removing InGaAs contact layer in passive waveguides, (f) after the second-step waveguide etching.

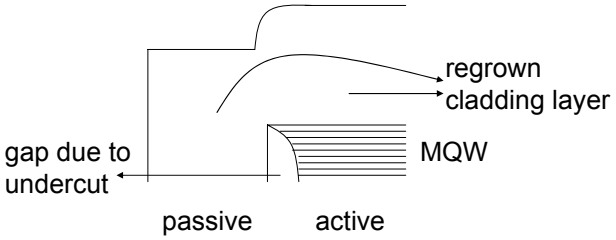


Fig. 5.14 Discontinuity of growth at the active/passive interface caused by undercut.

Next, InP and InGaAs were regrown on the sample by using metal-organic vapor phase epitaxy (MOVPE) (Fig. 5.13-c). The details of MOVPE growth are out of the scope of this dissertation. The readers are referred to [15] for detailed information on the regrowth process. Above the 250-nm-thick undoped InP spacer, the InP cladding and InGaAs contact layers were p-doped by concentrations of 5×10^{17} cm^{-3} and 1×10^{19} cm^{-3} respectively. Following the regrowth, SiO_2 was sputtered as a hard mask for waveguide etching. After the waveguide lithography, the first-step etching was done until the final etching depth of shallow waveguides (Fig. 5.13.-d). Methane-based reactive ion etching (RIE) was used for waveguides formation. Following the first etching, SiO_2 hard mask was removed completely with the help of BHF. The contact opening regions were defined by lithography, after which the InGaAs contact layer was removed from the passive waveguides by chemical etching with H_2SO_4 : H_2O_2 : H_2O solution (Fig. 5.13-e). This was followed by sputtering SiO_2 again and lithography for the definition of deep and shallow regions. After dry etching SiO_2 in deep regions, the second-step waveguide etching was done until the final depth of deeply etched waveguides (Fig. 5.13-f). The rest of the process was identical to the process described in Section 3.2.2.

5.4 CHARACTERIZATION OF THE PIC

The fabricated PICs were cleaved into individual circuits before the post-processing steps explained in Chapter 3. The micrograph of a PIC after fabrication is available in Fig. 5.15. The color difference outside the waveguides is caused by the difference of polyimide thickness on different regions of the chip. For example, the output facet has a much thinner polyimide layer to increase the yield of cleaving process. The phase

shifters and SOAs are also clearly visible from the color difference of polyimide. The input waveguide is on the top left corner of the chip.

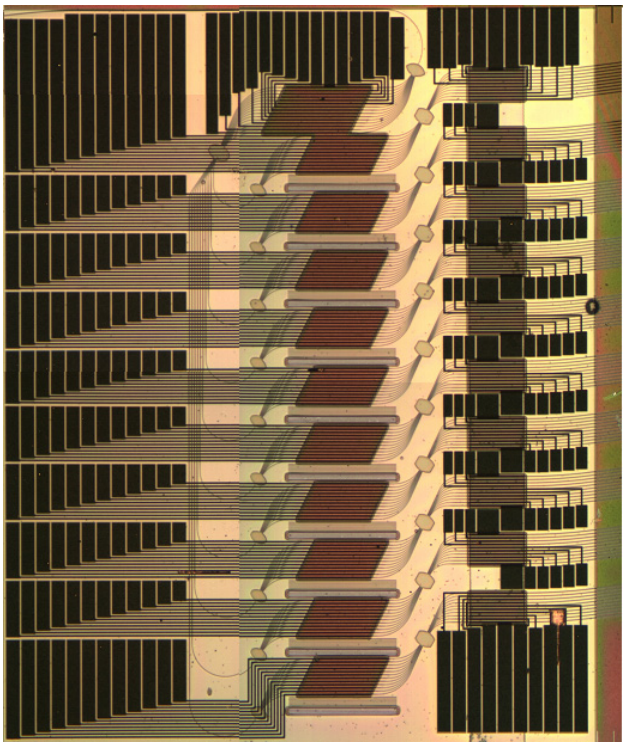


Fig. 5.15 Optical microscope image of the fabricated PIC.

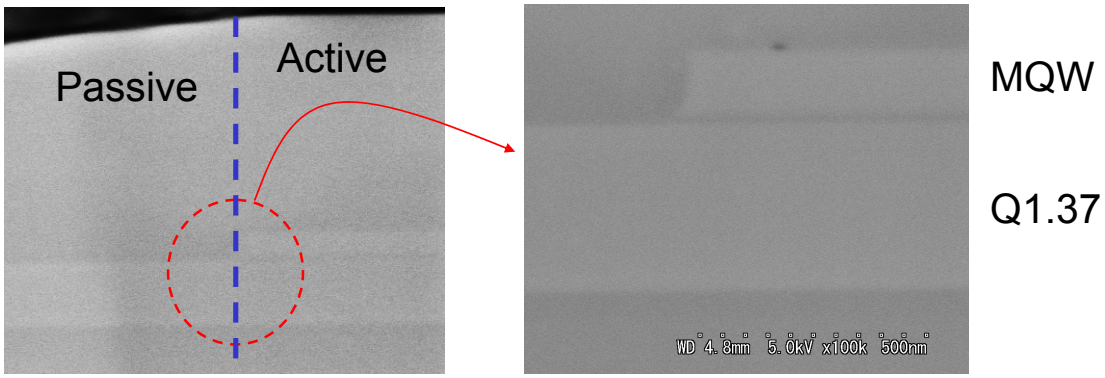
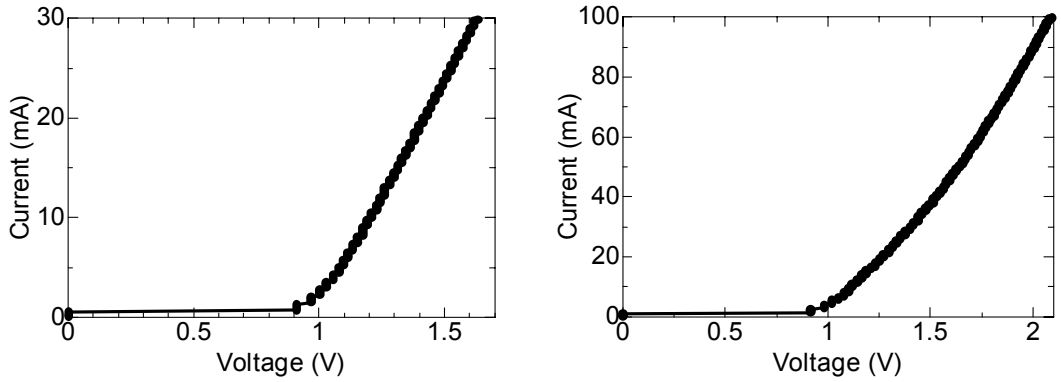


Fig. 5.16 SEM images of active-passive interface.



(a) (b)

Fig. 5.17 I-V curves of (a) a phase shifter and (b) an SOA.

The qualities of active/passive interface and regrowth were checked with a scanning electron microscope (SEM). As shown in Fig. 5.16, the offset quantum well technique was successfully implemented without visible defects or discontinuities at the interface. A good active-passive interface without any defects is necessary for low coupling loss.

Next, the electrical characteristics of the phase shifters and SOAs were measured. Pin diode behavior with a differential resistance on the order of 10-20 Ω was observed for both phase shifters and SOAs as shown in Fig. 5.17. The I-V curve of the SOA was characterized in a wider range of current because this device typically operates with a larger current than the phase shifter. Similar properties were observed with all devices in different locations of the PIC randomly selected for testing, which implies that the entire PIC was fabricated without malfunctioning devices detected. The optoelectronic properties of these devices were investigated later. The amplified spontaneous emission (ASE) of a number of SOAs was measured through a fiber coupled to the output waveguides. Fig. 5.18 plots a typical ASE vs. current curve observed with the SOAs in the PIC. The absorption and gain behavior of the SOAs was also characterized by measuring the transmittance of laser emission at a wavelength of 1550 nm through the chip. As shown in Fig. 5.19, the extinction ratio is over 40 dB between the current values of 0 mA and 100 mA. The sublinear trend of gain vs. current graph is in agreement with the previous reports on MQW-SOAs in the literature [16,17]. This is

caused by the gain saturation due to the step-like density of states in MQW and the increasing Auger recombination due to carrier density.

The efficiency of phase shifters was characterized by injecting 1550-nm laser emission to the input of the switch and measuring the optical power at one of the

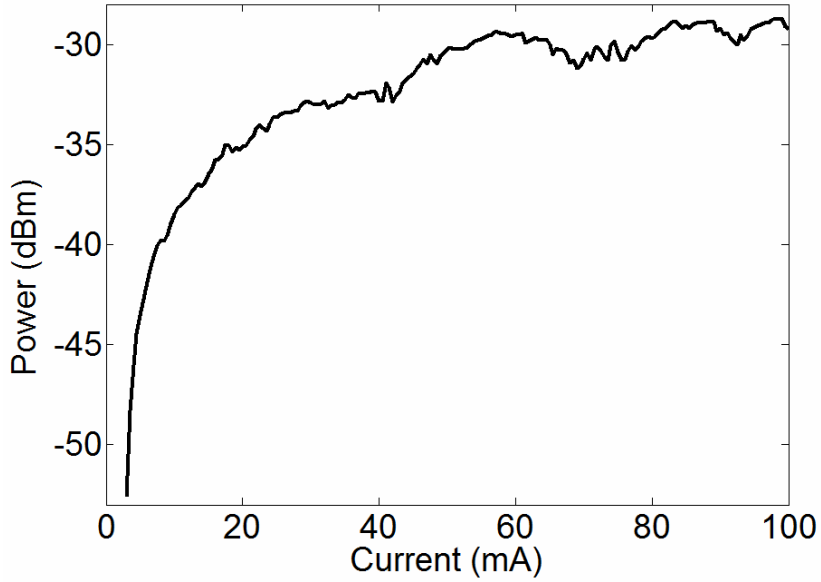


Fig. 5.18 ASE of an SOA versus current.

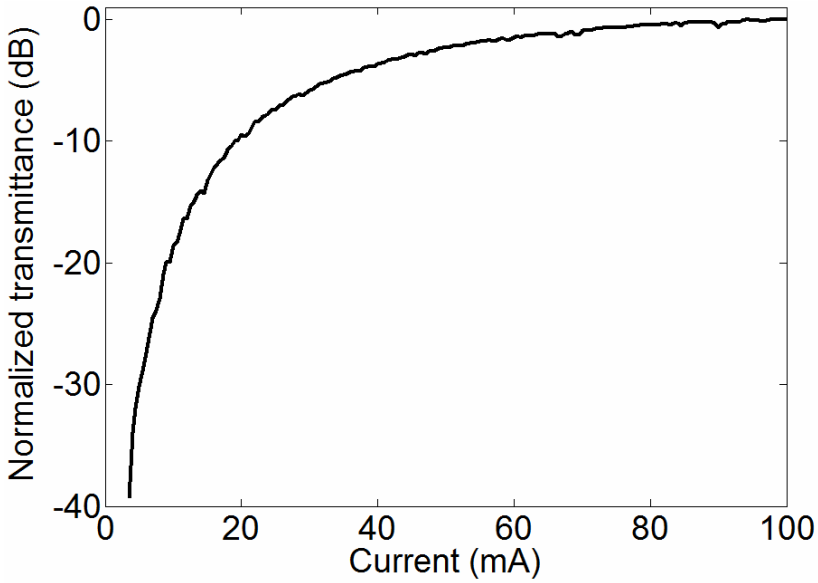


Fig. 5.19 Normalized transmittance of an SOA versus current.

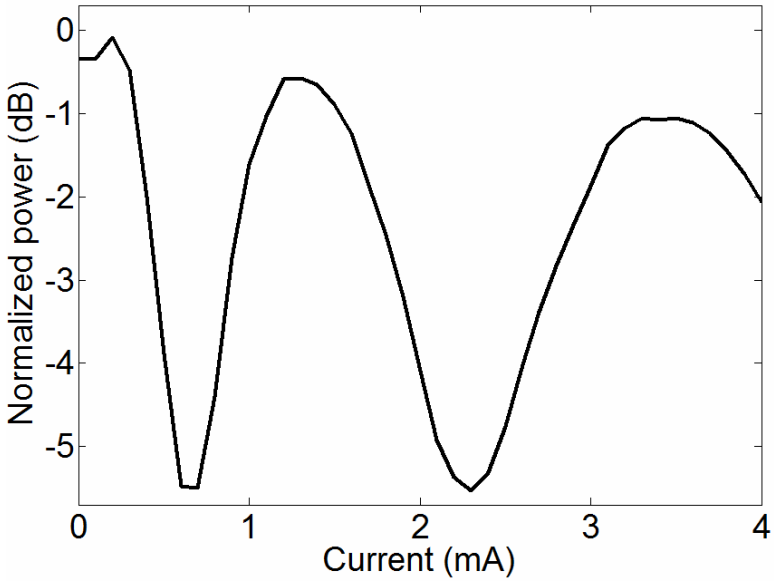


Fig. 5.20 Normalized power at a switch output versus the current injected to a phase shifter.

outputs while changing the phase shifter current. $I_{2\pi}$, which is the current necessary to change the phase by 2π, is less than 1.5 mA according to Fig. 5.20. This corresponds to a dramatic enhancement of phase modulation efficiency compared to the devices presented in Chapter 3. The major reason of this improvement is the shallow etching of phase shifters, which has reduced the damage on electrical characteristics caused by reactive ion etching. The improved efficiency of phase shifters reduces the overall power consumption and heat generation tremendously.

Demonstration of switching was done after the separate characterization of individual devices explained above. The operating conditions of the phase shifters were derived using the algorithm explained in Section 3.2.3.2. The current through the SOA at the corresponding output was maintained at 70 mA while finding the operating conditions of each state. The output light was filtered using an arrayed waveguide grating (AWG) to mitigate the influence of ASE on the measurement. Among the 100 possible switching states, 30 have been tested as a proof of operation of the device. States 1-10 and 71-90 were selected for characterization because these states have higher theoretical loss than the states that route to the central outputs. The fiber-to-fiber loss in these states is between 21.0 dB and 25.7 dB under the condition of an SOA current of 100mA. This corresponds to an on-chip loss in the range of 10.0 dB – 14.7

dB. Fig. 5.21 plots the on-chip loss in States 71-80 as an example. As expected, the outputs at the edges of 1×10 switches receive less power than the ones at the center. The power nonuniformity can be mitigated through SOA gain conditions. The contribution of the 1×100 phased-array switch loss on the fiber-to-fiber loss was measured indirectly with the help of the ASE of the SOAs. A current of 100 mA was injected to one of the SOAs and the switches were configured to the state that forms a light path to the output containing that SOA. The power was measured at the input and output waveguides in equal conditions. In principle, the active-passive coupling loss and fiber-waveguide coupling loss are equal in left and right sides of the SOA, which means that the difference between the ASE power at the input and the output should be equal to the on-chip loss in the passive part of the 1×100 switch. The loss at a wavelength of 1550 nm should be lower than the difference because the relatively broadband and unpolarized ASE should experience a higher loss compared to a polarization-controlled laser oscillation. Therefore, this estimation puts an upper limit on the actual loss in devices. The estimated gain of the SOAs was measured to be less than 6 dB with an injection current of 100 mA. This value includes the active-passive coupling loss, which has not been measured.

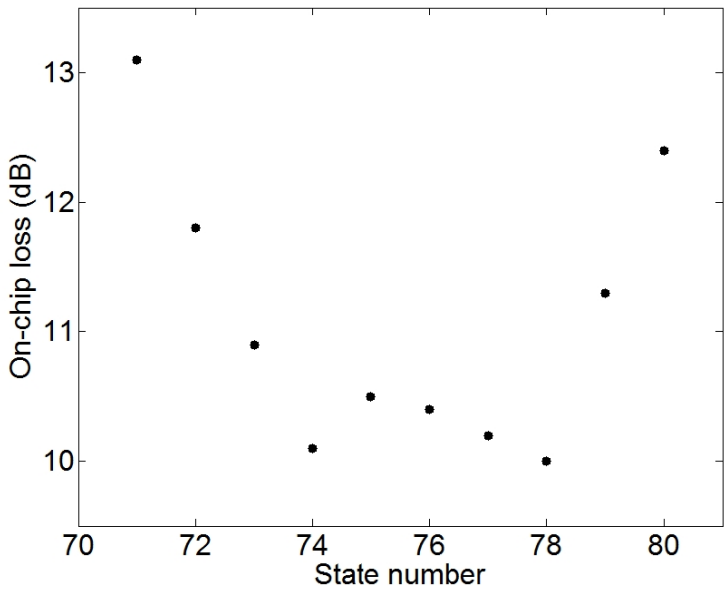


Fig. 5.21 On-chip loss in States 71 – 80. The total fiber-waveguide coupling loss is assumed to be 11 dB.

The exact value of the extinction ratio is difficult to measure because of the very low optical power in the "off" state, which is below the sensitivity limit of the photodetector (-70 dBm). The total extinction ratio is the sum of the extinction ratio of the phased-array switch and the SOA. The extinction ratio of the SOA, which is the difference of transmittance between zero bias and a current of 100 mA, is more than 40 dB as plotted in Fig. 5.19. The total extinction ratio was measured to be more than 50 dB in all states that were tested. The actual value, which could not be measured as explained above, is expected to be higher. This extinction ratio is sufficiently high for typical optical switching applications.

The spectral response of the switch was measured by injecting light within a range of wavelengths into the device. Since a filter could not be employed in this experiment, the effect of ASE noise on the measurement was suppressed by injecting the light from the output (measured CW power of 0.6 dBm) and monitoring the power at the input. Fig. 5.22 shows the transmittance spectrum in State 76 with an SOA current of 100 mA as an example. The 3-dB band extends from 1533 nm to beyond 1570 nm, which is the longest wavelength measured due to the limitations of the tunable laser.

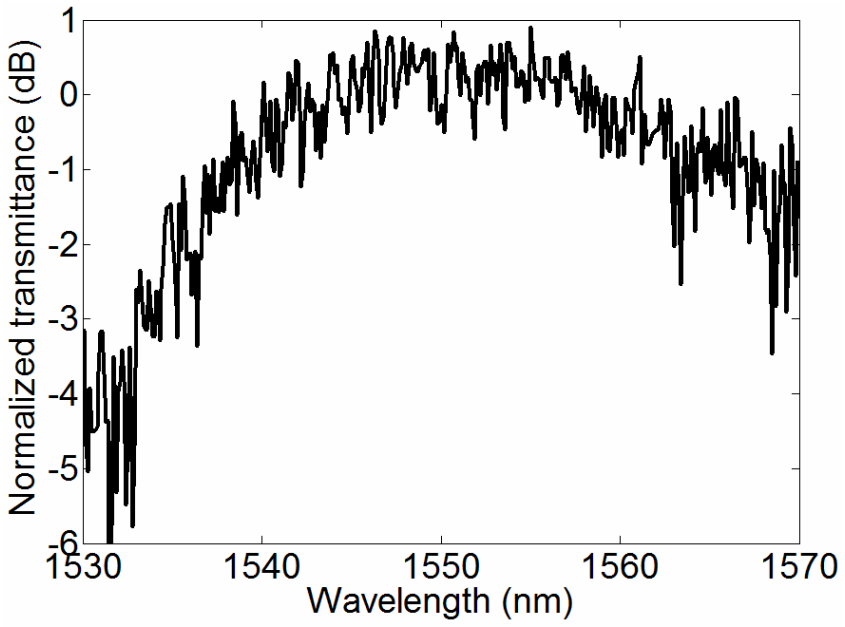


Fig. 5.22 Spectral response of State 76 with an SOA current of 100 mA

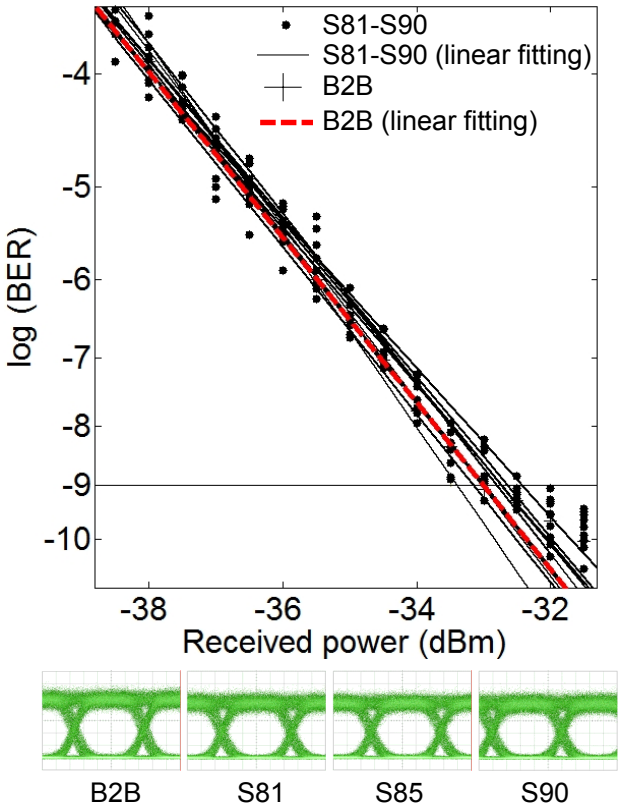


Fig. 5.23 BER as a function of received power and some eye diagrams recorded with a received power of -25 dBm. Both data points and linear fitting curves are available for BER. B2B: back to back,.

Finally, the performance of the switch was tested with a 2^{31}-1-bit-long pseudorandom binary sequence at a bit rate of 10 Gb/s using a preamplified receiver. As shown in Fig. 5.23, the power penalty is below 1 dB at a bit error rate (BER) of 10^{-9} in all the states measured (State 81 – 90). The fluctuations of BER data points and the negative power penalty at some channels are due to the fluctuations of fiber-waveguide coupling loss mostly caused by experimental conditions. The low-penalty operation is attributed to the transparency of the phased-array switch and the low-gain SOAs operated in the linear regime.

5.5 CONCLUSION

A PIC consisting of 135 phase shifters, 100 SOAs, 22 star couplers and numerous

waveguides was successfully fabricated by using the offset quantum well technique. This PIC has a potential of switching to up to 100 ports, which has not been achieved with any other monolithic semiconductor photonic switches before. The total size of the PIC is limited to 6.5 mm × 6 mm owing to the footprint advantage of phased-array switches with large number of ports.

The PIC was fabricated successfully using the offset quantum well technique and two-step etching. The phase shifters in this PIC demonstrate a significantly higher efficiency ($I_{2\pi}$ < 1.5 mA) compared to the phase shifters in the previous switches ($I_{2\pi}$ > 20 mA) presented in Chapter 3, owing to the shallow etching and smaller bandgap of the quaternary layer. The SOAs have an extinction ratio of more than 40 dB with a current of 100 mA. The static operation of the switch has also been demonstrated with a number of ports at the edges of the switch. The on-chip loss is less than 14.7 dB in spite of the limited number of phase shifters controlled in the second-stage switch due to problems with wire bonding. A very large extinction ratio above 50 dB has been achieved with this switch as a result of the serial cascade of phased-array switches with SOAs. A 10-Gb/s modulated signal has been transmitted through the chip with a power penalty below 1 dB.

This PIC is significant for two major reasons. First of all, it is among the largest-scale photonic integrated circuits. Large-scale photonic integration has been able to find very few applications so far. A PIC of this scale is important as a potential novel application. Second, integrated photonic switches of this scale or even larger are necessary for ultra-large-throughput optical packet switching as discussed in the next chapter. This PIC is believed to move optical packet switching one step closer to reality.

REFERENCES OF CHAPTER 5

[1] S. C. Nicholes, M. L. Masanovic, B. Jevremovic, E. Lively, L. A. Coldren, and D. J. Blumenthal, "An 8 x 8 InP monolithic tunable optical router (MOTOR) packet forwarding chip," Journal of Lightwave Technology, vol. 28, no. 4, pp. 641-650, Feb. 2010.

[2] H. Wang, A. Wonfor, K. A. Williams, R. V. Penty, and I. H. White, "Demonstration of a lossless monolithic 16x16 QW SOA switch," in Proc. European Conference on Optical Communication (Postdeadline papers), 2009, pp. 1-2.

[3] T. Shioda, T. Doi, A. Al Amin, X.-L. Song, M. Sugiyama, Y. Shimogaki, and Y. Nakano, "Simulation and design of the emission wavelength of multiple quantum well structures fabricated by selective area metalorganic chemical vapor deposition," Thin Solid Films, vol. 98, pp. 174-178, 2006.

[4] J. Binsma, P. Thijs, T. VanDongen, E. Jansen, A. Staring, G. VanDenHoven, and L. Tiemeijer, "Characterization of butt-joint InGaAsP waveguides and their application to 1310 nm DBR-type MQW gain-clamped semiconductor optical amplifiers," IEICE Transactions on Electronics, vol. E80-C, no. 5, pp. 675-681, May 1997.

[5] B. Mason, G. Fish, S. DenBaars, and L. Coldren, "Widely tunable sampled grating DBR lasers with integrated electroabsorption modulator," IEEE Photonics Technology Letters, vol. 11, no. 6, pp. 638-640, Jun. 1999.

[6] J. W. Raring, M. N. Sysak, A. T. Pedretti, M. Dummer, E. J. Skogen, J. S. Barton, S. P. DenBaars, and L. A. Coldren, "Advanced integration schemes for high-functionality/high-performance photonic integrated circuits," Proceeding of SPIE, vol. 6126, pp. 61260H1-61260H20, 2006.

[7] S. McDougall, O. Kowalski, C. Hamilton, F. Camacho, B. Qiu, M. Ke, R. De La Rue, A. Bryce, and J. Marsh, "Monolithic integration via a universal damage enhanced quantum-well intermixing technique," IEEE Journal of Selected Topics in Quantum Electronics, vol. 4, no. 4, pp. 636-646, Ju./Aug. 1998.

[8] J. W. Raring and L. A. Coldren, "40-Gb/s widely tunable transceivers," IEEE Journal of Selected Topics in Quantum Electronics, vol. 13, no. 1, pp. 3-14, Jan./Feb. 2007.

[9] K. Morito, S. Tanaka, S. Tomabechi, and A. Kuramata, "A broad-band MQW semiconductor optical amplifier with high saturation output power and low noise figure," IEEE Photonics Technology Letters, vol. 17, no. 5, pp. 974-976, May 2005.

[10] B. R. Bennett, R. A. Soref, and J. A. Del Alamo, "Carrier-induced change in refractive index of InP, GaAs, and InGaAsP," IEEE Journal of Quantum Electronics, vol. 26, no. 1, pp. 113-122, Jan. 1990.

[11] J.-P. Weber, "Optimization of the carrier-induced effective index change in InGaAsP waveguides – application to tunable Bragg filters," IEEE Journal of Quantum Electronics, vol. 30, no. 8, pp. 1801-1816, Aug. 1994.

[12] H. C. Casey and P. L. Carter, "Variation of intervalance band absorption with hole concentration in p-type InP," Applied Physics Letters, vol. 44, no. 1, pp. 82-83, Jan. 1984.

[13] A. Al Amin, "Research on Monolithic Integration of WDM Subsystem on InP," Ph.D. thesis, The

University of Tokyo, Japan, 2004.
[14] T. Tanemura, I. M. Soganci, T. Oyama, T. Ohyama, S. Mino, K. A. Williams, N. Calabretta, H. J. S. Dorren, and Y. Nakano, “Optical buffer based on monolithic InP phased-array 1×16 switch with silica-PLC pitch converter and ultra-compact coiled fiber delay lines,” in Proc. Optical Fiber Communication Conference (OFC’10), San Diego, CA, 2010, Paper PDPA5.
[15] S. A. Ibrahim, “A study on all-optical switching device using active multimode interferometers,” Ph.D. thesis, The University of Tokyo, Japan, 2009.
[16] J. Z. Wilcox, G. L. Peterson, S. Ou, J. J. Yang, M. Jansen, and D. Schechter, “Gain- and threshold-current dependence for multiple-quantum-well lasers,” Journal of Applied Physics, vol. 64, no. 11, pp. 6564-6567, Dec. 1988.
[17] P. Harsma, “Integration of semiconductor optical amplifiers in wavelength division multiplexing photonic integrated circuits,” Ph.D. thesis, Eindhoven University of Technology, The Netherlands, 2000.

CHAPTER 6
POWER CONSUMPTION IN BUFFERED OPTICAL PACKET SWITCH FABRICS UTILIZING PHASED-ARRAY SWITCHES

6.1 INTRODUCTION

Chapter 4 has focused on experimental research on OPS applications of phased-array switches. The scale of these experiments has been limited as a natural consequence of its being academic experiments for proof of concept. Studies on the feasibility of OPS routers with ultra-large capacities are of crucial importance because they can directly influence the amount of intellectual and capital investment on OPS technologies. Especially the power consumption is an important indicator since power reduction at high bit rates has been the major motivation of OPS as mentioned in several articles [1-5]. Nevertheless, the reports available on this problem have dramatically different conclusions. For example, [6,7] lead to the conclusion that OPS does not offer a significant advantage to electronic routing, whereas some articles claim that optical switching technologies are much more power efficient [8,9]. However, even in the papers claiming the energy efficiency of OPS, the difficulty of implementing large optical buffers is mentioned. These limited number of papers give the message that OPS might be more energy efficient than electronic switching depending on the technology, but the advantage of OPS is not very obvious and there are serious technical difficulties against scaling the switch and buffer capacities.

The state-of-the-art single-chassis electronic router has a maximum capacity of

4.48 Tb/s [10]. The power consumption rate of this router is 2.75 nJ/bit, which corresponds to a power consumption of 275 kW at a throughput of 100 Tb/s. Considering that multi-chassis routers are already in use and estimating an annual IP capacity enhancement of 40% [11], routers with throughput approaching 1 Pb/s are expected in the next ten years. OPS should offer significantly higher power efficiency than electronic switching and should be able to scale up to the aforementioned capacities with low cost in order to replace this established technology. WDM-OPS can help us reach large capacity levels by reducing the number of ports, latency, cost and size of the router [12-16]. This necessitates compatibility with multi-wavelength and high-bit-rate packets. Moreover, there is a probability of utilizing spectrally efficient advanced modulation formats in future communication systems. The optical buffer and the switch have to be both strictly transparent and wavelength insensitive to route WDM packets with advanced modulation formats.

As explained in detail in Chapter 1, presently available switch technologies have difficulties in satisfying all the stringent constraints of multi-wavelength compatibility, loss, size and signal quality with large numbers of ports. Researchers are still searching for a switch with low power consumption, low excess noise and low crosstalk. Optical buffering is even more difficult than switching because of the immaturity of digital photonics. Different techniques of delay lines have been proposed for buffering, but none of these techniques offers capacity, size, power and cost necessary for OPS. Slow-light [17-20] and waveguide delay lines suffer from high loss, which leads to high power consumption [6]. Fiber delay lines (FDL) offer the lowest power consumption, but they are bulky. Independent of the delay line technology, tunability of buffering duration is demanded, so delay lines have to be equipped with optical switches [21].

In this chapter, the power consumption in large-scale OPS routers that utilize phased-array switches is investigated in a semi-theoretical approach. A switch matrix and an optical buffer, both strictly transparent and compatible with high-bit-rate packets (such as WDM, OTDM, etc.), are assumed to be constructed from phased-array switches. The analysis is carried out for up to 1000 input and output fiber connections in order to investigate the feasibility of ultra-high throughput in the range of hundreds of Tb/s or a few Pb/s. Ultra-compact high-index-contrast FDLs are proposed to be used

together with these switches to achieve low power, small size and high capacity at the same time. The power consumption of a router with an exactly identical architecture, which comprises broadcast-and-select SOA gate array switches, is also calculated for comparison. Section 6.2 introduces the switch and buffer architectures studied. The calculation method and results are available in Section 6.3. A discussion and conclusion section ends the chapter.

6.2 ARCHITECTURES OF OPTICAL SWITCH AND BUFFER ANALYZED

6.2.1 *N*×*N* Matrix Switch

Asynchronous (non-slotted) operation is a desired characteristic of OPS networks because synchronization increases the power, latency, complexity, and the cost. Nonblocking switches are necessary for asynchronous operation. Spanke architecture is a strictly nonblocking $N \times N$ switching architecture that can be built from $1 \times N$ switches as shown in Fig. 6.1 [22]. An $N \times N$ Spanke matrix comprises $2N$ $1 \times N$ switches in total. With the switch technologies analyzed in this paper, an entire $N \times N$ switch with hundreds of connections cannot fit on a single compound semiconductor wafer. Even if the entire circuit can be crammed on a single substrate with an ultra-compact design, the waveguide crossings cause crosstalk and loss along with design complexity. Thus, the input and output stages are assumed to be built on different chips and connected to each

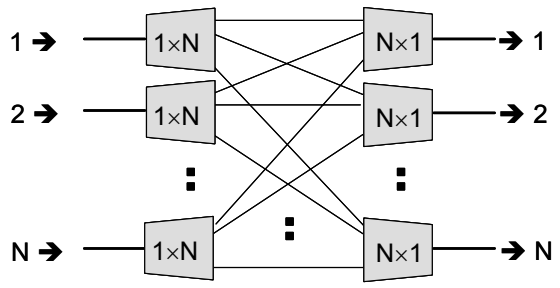


Fig. 6.1. Strictly nonblocking $N \times N$ switch with Spanke architecture.

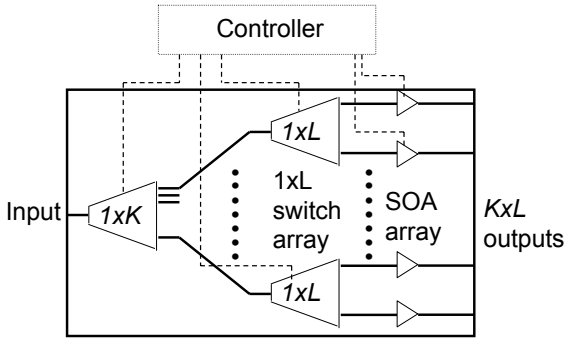


Fig. 6.2 A two-stage monolithic *1×(K×L)* optical switch with an SOA array to compensate for coupling and on-chip losses.

other via fibers as a realistic solution.

Although phased-array *1×N* switches have a good scalability potential for tens of outputs, further considerations on device design are necessary for hundreds or thousands of ports. For example, a phased-array 1×1000 switch should comprise 1600 phase shifters in a single device under the assumption of an array-to-output ratio (AOR) equal to 1.6. Both power consumed by the phase shifters and the length of star couplers increase to unacceptable levels in a device of this scale. Instead of that, two-stage cascaded switching leads to both power saving and improved extinction ratio. In cascade architecture, a *1×(K×L)* switch is obtained by connecting the outputs of a *1×K* switch to *K 1×L* switches as displayed in Fig. 6.2. In the schematic diagram, there is an array of SOAs at the output of the switch to compensate for the losses. The SOAs are preferred to be located at the output to improve the extinction ratio, which affects the maximum number of switching hops in the network [23]. Note that this architecture is identical to the architecture of the PIC presented in Chapter 5.

The total number of phase shifters in a cascaded *1×(K×L)* device is $AOR \cdot K(1+L)$. However, only $AOR(K+L)$ of these phase shifters have to be operated at a time since all the switches in the second stage except one can be left unbiased. Consequently, the power consumption of phase shifters in a 2-stage cascaded switch is much less than that in a single-stage switch, which is proportional to $AOR(K \cdot L)$. In a configuration of a few hundreds or thousands of output ports, increasing the number of cascaded stages further does not have any merits because the size and loss advantage of

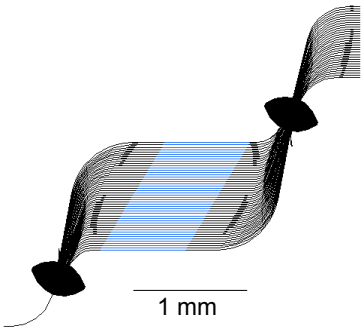


Fig. 6.3 Layout design of a *1*×*32* InP phased-array switch comprising high-mesa waveguides (black) and 750-μm-long phase shifters (blue).

phased-array scheme is the most pronounced for tens of output ports. With the two-stage architecture, a 1×1024 switch can be obtained from thirty three 1×32 switches, whose layout design based on high-mesa InP/InGaAsP waveguides is shown in Fig. 6.3.

Similar to phased-array switches, broadcast-and-select switches also have to be cascaded for switching to hundreds of ports. It is well known that distributed broadcast-and-select switches consisting of low-gain SOA gates located between small-scale splitters have better scalability than switches with smaller number of high-gain SOAs and large-scale splitters [24]. A three-stage design has been preferred as a compromise among several parameters including power dissipation, noise accumulation, the number of SOAs, and footprint (Fig. 2.10). This configuration allows reaching 1000 outputs with 111 passive 1×10 splitters and 1110 SOAs. Each packet propagates through 3 SOAs and 3 splitters in a three-stage *1*×*N* broadcast-and-select switch independent of *N*.

6.2.2 Tunable Optical Buffer

A tunable buffer can be constructed from a number of FDLs with different lengths and two *1*×*N* switches as shown in Fig. 6.4. The duty of the switches is to select the fiber that will offer the time delay necessary to avoid contention resolution. Ideally, one of these switches can be replaced by a passive coupler. However, this modification reduces the extinction ratio and increases the effect of crosstalk between packets. Tunable delay lines are assumed to comprise two switches in the present study. Both phased-array and

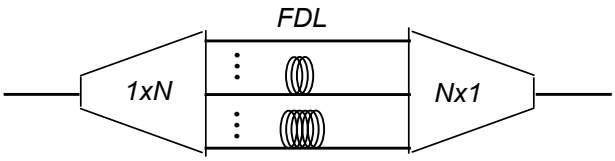


Fig. 6.4 A tunable optical buffer consisting of space switches and fiber delay lines.

broadcast-and select switches are compatible with this configuration.

The capacity of the buffer is critical to determine the length of FDLs and the port count of the switches. The buffer size in electronic packet routers is conventionally equivalent to a delay of 250 ms [25]. The propagation distance for a delay of this length is approximately 50,000 km, which is impractical. However, a recent article states that the buffer size can be reduced significantly without increasing the packet loss rate [25]. Simulation results revealed that if transmission control protocol (TCP) packets are spread in time to reduce the burstiness of the traffic, only 10-20 packets per port are sufficient for contention resolution in a router with 80% load [26]. Since none of the currently available optical buffering technologies is capable of extremely large-capacity buffering as in electronic routing, modification of the packet traffic for small buffer sizes is a reasonable approach and is adopted in this analysis.

A tunable buffer with a maximum depth of 20 packets and a resolution of single packet can be realized with two 1×21 switches and 21 delay lines that have a step size of one packet duration. The packet size depends on the protocol and the application. An average IPv4 packet consists of a payload of 10 kbits. Although transparent space switches are in principle compatible with variable-length packets, for simplicity and an intuitive comparison between different bit rates, a fixed packet size of 10 kbits is assumed in this study. For a bit rate of 1 Tb/s, this corresponds to a packet length of 10 ns and a delay length of 200 ns in the longest delay line. In this case, the length step between delay lines is 2 m and the longest delay line is only 40 meters.

6.2.3 Switch Controller

Because of the necessity of supplying several analog voltages to the phase shifters, phased-array switches are expected to require more complicated controller circuits than

broadcast-and-select switches. The power dissipated by the controller of broadcast-and-select switches is neglected, so we focus on the controller of phased-array switches in this section. The duty of the switch controller is to supply the set of bias voltages at the phase shifters to maintain the light path to the requested output port. In a $1 \times N$ switch, there are N sets of bias voltages corresponding to N switching states. Each switching state is identified by $AOR \times N$ analog voltages, so a look-up table of $AOR \times N^2$ bias voltages has to be stored in the memory of the switch controller. Since this table is stored in digital domain, one digital-to-analog converter (DAC) is necessary for each phase shifter. The switch controller is not the only component in the control plane because a label processor is also necessary to extract the labels, inform the switch controller and rewrite labels if necessary. The design of the label processor depends significantly on the labeling scheme, which is out of the scope of this paper.

6.3 CALCULATION OF ESTIMATED POWER CONSUMPTION

Since monolithic $1 \times N$ switches are the building blocks of both the buffer and the switch, calculating the power consumption of a $1 \times N$ switching chip simplifies the problem.

6.3.1 Power Consumption of a $1 \times N$ Switching Chip

The general power consumption equation of an optoelectronic component is given by

$$P_{consumed} = P_{in} - P_{out} + P_{sup\,plied}, \tag{6.1}$$

where $P_{sup\,plied}$ is the total power consumed to operate the component, and P_{in} and P_{out} are the input and output power respectively. It is assumed that the optical losses, including the on-chip, coupling and fiber losses are compensated for completely by on-chip SOAs. Therefore, supplied power is the only power consumption mechanism. The supplied power includes both bias power of photonic devices and devices for heat control.

Electro-optical phase shifters operating under reverse bias do not necessarily have to be cooled if low-resistance Ohmic contacts and good isolation of the pin junction are achieved. Even SOAs that can operate without coolers up to 70ºC are already commercially available [27]. A slow temperature control mechanism is still necessary to keep the operating conditions stable, but such a slow tuning can be implemented with relatively low power, which is neglected in this analysis.

The power consumption of a phased-array-based 1×N chip consists of three components.

i) Phase shifters,

ii) SOAs,

iii) Switch controller.

On the other hand, SOA power dissipation is assumed to be the only energy consuming mechanism in broadcast-and-select switches. Broadcast-and-select switch power is calculated in the section focusing on the power dissipation of SOAs.

6.3.1.1 Power Consumption of Phase Shifters

The power per phase shifter depends on the phase modulation mechanism. Since phase shifters operated by reverse-biasing a pin junction are both faster and more energy-efficient than carrier-injection type devices, they are likely to be preferred. The power consumption of a reverse-biased phase shifter is given by

$$P_{ps} = V_b I_l + \sum_{t=1}^{NT} \alpha_t C_d \left(\Delta V\right)_t \left(V_f\right)_t f, \tag{6.2}$$

where the first term is the static power consumption and the second term is the dynamic one. V_b is the bias voltage, I_l is the leakage current, NT is the number of dynamic transition pairs, α_t is the activity factor of the corresponding transition (i.e. the number of transitions per clock cycle), C_d is device capacitance, ΔV is the bias voltage change in a transition, V_f is the bias voltage after the corresponding transition, and f is the packet frequency.

In an ideal phase shifter, the static power consumption is negligible compared to the dynamic value. The phase shifters in the phased-array switch can have multiple bias

voltage values between *0 V* and $V_{2\pi}$. The capacitive charging energy of each transition depends on the initial and final bias values, the maximum of which is equal to $C_d V_{2\pi}^{\ 2}$. The number of transition pairs and the corresponding transition energies depends on the position of the phase shifters in the array. The complicated dynamic power expression in (6.2) can be simplified to a conventional dynamic power equation as

$$P_{dyn}(av) = \alpha_{eff} C_d V_{2\pi}^{\ 2} f, \tag{6.3}$$

where α_{eff} is the effective activity factor calculated as the accumulated contribution of all possible transitions. Throughout the calculations, α_{eff} is assumed to be equal to 0.17 with an overestimation.

$V_{2\pi}$ is 2.5 V in a state-of-the-art 750-μm long InP/InGaAsP phase shifter [28]. This phase shifter has an estimated device capacitance of 0.5 pF. Substituting these values in (3) leads to an average dynamic power consumption of

$$P_{dyn}(av) = f \cdot (0.53\,pJ) \tag{6.4}$$

In other words, the energy per packet, *EPP* is equal to 0.53 pJ. This value has to be multiplied by the number of biased phase shifters to calculate the total power dissipation. In a $1 \times \sqrt{N} \times \sqrt{N}$ two-stage switch, which has a functionality of $1 \times N$, the number of phase shifters that have to be biased at a time is

$$N_{ps} = 2AOR\sqrt{N} \tag{6.5}$$

Therefore, the energy per packet of phase shifters is

$$EPP_{PS} = AOR\sqrt{N} \cdot (1.06\,pJ) \tag{6.6}$$

Assuming that each packet carries 10 kbits on average, the energy per bit is

$$EPB_{PS} = AOR\sqrt{N} \cdot (0.106\,fJ) \tag{6.7}$$

independent of the bit rate.

6.3.1.2 Power Consumption of SOAs

The gain and noise characteristics of SOAs depend on the device design and signal power, so basing the analysis on a single SOA design does not lead to a fair comparison. For example, a 4-Tb/s payload carries 100 times higher power than a 40-Gb/s payload,

so it necessitates an SOA with a 20-dB higher saturation output power. Since custom SOA design is out of the scope of this paper, an assumption based on constant electrical-to-optical conversion efficiency is preferred with the following equation.

$$P_e = \frac{P_{out} - P_{in}}{\eta}, \tag{6.8}$$

where P_e is the electrical power dissipated, P_{out} and P_{in} are the output and input optical powers respectively, and η is the electrical-to-optical conversion efficiency. For a constant gain, the power consumption is linearly dependent on the input optical power, so different architectures and bit rates can be compared based on the lowest signal power to reach a certain signal-to-noise ratio (SNR) at the output. The output power of an SOA is defined by the well-known equation

$$P_{out} = P_{in}G + N_{in}G + n_{sp}\left(G-1\right)h\upsilon_c\Delta\upsilon_o, \tag{6.9}$$

where P_{in} is the input signal power, N_{in} is the input noise power, G is the gain of SOA, n_{sp} is the spontaneous emission factor, h is Planck's constant, v_c is the carrier frequency, and Δv_o is the optical bandwidth. The rightmost term is the ASE. If multiple SOAs are cascaded to compensate for the losses in between, so that the optical power is maintained as constant, the output power becomes

$$P_{out} = P_{in} + N_{in} + h\upsilon_c\Delta\upsilon_o\sum_{i=1}^{M}\left(n_{sp}\right)_i\left(G_i - 1\right), \tag{6.10}$$

where M is the total number of SOAs and i corresponds to the index of SOAs. If we assume that all SOAs are identical and operated with equal gain, and the input noise power is negligible, the expression simplifies to

$$P_{out} = P_{in} + Mh\upsilon_c\Delta\upsilon_o n_{sp}\left(G-1\right). \tag{6.11}$$

The electrical SNR of this signal after square-law detection is given by [29] as

$$SNR = \frac{P_{in}^{\ 2}}{4P_{in}Mh\upsilon_c\Delta\upsilon_e n_{sp}\left(G-1\right) + 2p\left[Mh\upsilon_c n_{sp}\left(G-1\right)\right]^2\Delta\upsilon_e\Delta\upsilon_o}. \tag{6.12}$$

The first term in the denominator is the signal-spontaneous emission beat noise and the second term is the spontaneous-spontaneous beat noise, which is typically negligible if a narrow optical filter is located before the detector. p is a coefficient, which is equal to 1 if a polarizer is used before detection and is equal to 2 if a polarizer is not used. This

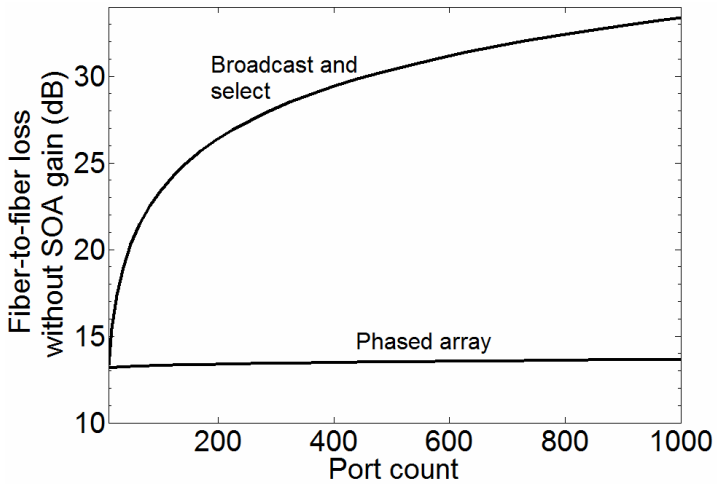


Fig. 6.5 Fiber-to-fiber optical loss (without SOA gain) of integrated two-stage $1 \times N$ optical phased-array switches and broadcast-and-select switches vs. output port count.

parameter is assumed to be 2 in our calculation. (6.12) is used in order to calculate the input power to achieve a threshold SNR. The electrical bandwidth is assumed to be equal to the bit rate. M is equal to 1 for $1 \times N$ phased-array switches and 3 for broadcast-and-select switches. The gain is equal to the fiber-to-fiber loss of the switching chip. The conversion efficiency of SOAs is assumed to be 0.1, which is a reasonable assumption based on the articles in the literature. The spontaneous emission factor is assumed to be 1.5 in case of phased-array switches and 3 in case of broadcast-and-select switches. The reason of this difference is the fact that SOAs in broadcast-and-select switches should have high extinction ratio, which requires high optical loss under zero bias. The SNR at the output is set as 30 dB to leave a margin for further cascading. Next, the insertion loss of phased-array switching chips is calculated to derive the gain of SOAs.

The theoretical loss of phased-array switches with tens of outputs is below 5 dB as long as AOR is 1.6. The optical path length is calculated based on 2-μm-wide deeply etched InP/InGaAsP waveguides. The optical propagation loss is 1 dB/cm, which is an achievable figure of merit with InP photonic integrated circuits. A fiber-to-chip coupling loss as low as 1.2 dB has recently been reported for tapered optical fibers and InP photonic integrated circuits [30]. Therefore, the total fiber coupling loss is assumed to be 2.4 dB. An additional loss of 0.5 is also assumed to account for nonidealities. Adding all terms, the fiber-to-fiber loss without SOA gain in a two-stage cascaded $1 \times N$

phased-array switch is plotted in Fig. 6.5. The estimated fiber-to-fiber loss without SOA gain in broadcast-and-select switches is also calculated similarly. The on-chip loss is assumed to be the sum of the theoretical loss of an ideal splitter and an additional loss of 0.5 dB to account for the waveguide propagation loss and active-passive coupling loss. To be consistent with the phased-array case, an additional loss of 0.5 dB is included due to nonidealities in multi-port fiber coupling. The loss in passive components of broadcast-and-select switches is also plotted in Fig. 6.5. Especially if the number of outputs is large, phased-array scheme has significantly lower loss than the broadcast-and-select scheme. If single-stage phased-array switches are preferred instead of cascades, then the fiber-to-fiber loss is less than 9 dB for output counts below 90. The switches employed in the tunable buffer are of this type because of their relatively small number of ports.

The total single-chip SOA gain is equal to the optical loss plotted in Fig. 6.5. This value is substituted into (6.12) to derive the signal power. Next, the estimated power consumption is calculated according to (6.8). In Fig. 6.6, the energy per bit of SOAs is plotted as a function of the port count of monolithic $1 \times N$ phased-array and broadcast-and-select switches. The SOA power dissipation in phased-array switches is considerably lower than broadcast-and-select switches because of the lower optical loss. Note that the energy per bit does not change with WDM because the optical power is proportional to the number of WDM channels.

6.3.1.3 Power Consumption of the Switch Controller

In the switch controller, the building blocks that can dissipate power are the memory, digital-to-analog converters (DAC), and electrical amplifiers if necessary. The power consumption of the circuit that reads the incoming bits is neglected. The size of the memory depends on the resolution of the bias voltage. $V_{2\pi}$ of 2.5 V and a resolution of 10 mV lead to eight bits for each phase shifter. Even for 1,000 ports, 12.8 kbits are sufficient to store the entire bias information. Such small-scale memories can be implemented by static random access memories (SRAM). According to the International Technology Roadmap for Semiconductors (ITRS), the read/write energy of an SRAM

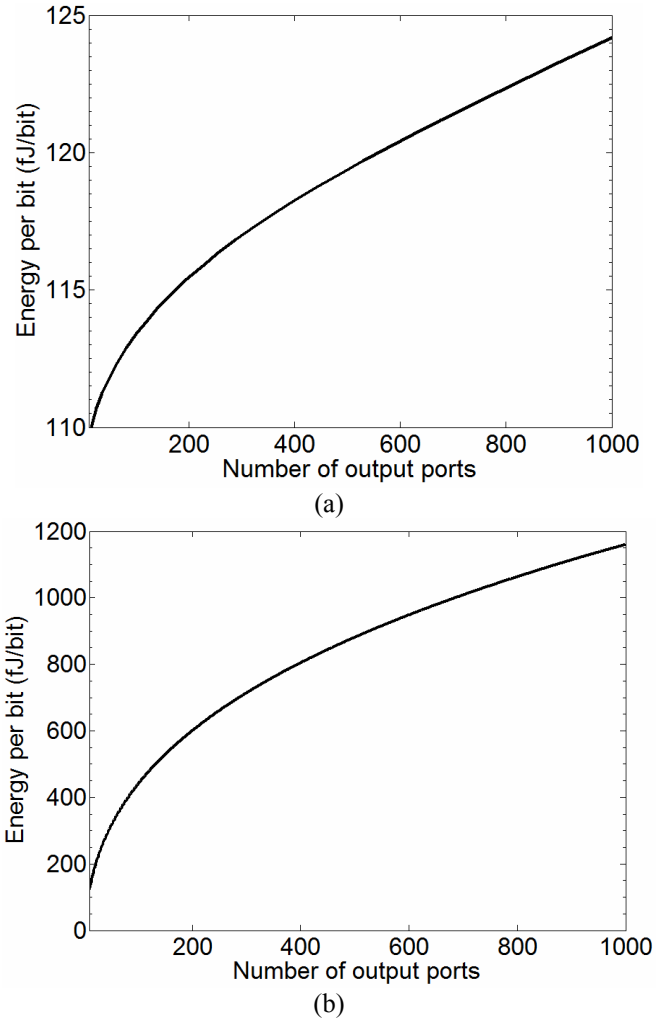


Fig. 6.6 Estimated energy consumption of SOAs in (a) two-stage cascaded $1\times N$ phased-array switches and (b) three-stage $1\times N$ broadcast-and-select switches.

was 7×10^{-16} J/bit in 2007 and it is expected to reduce to 2×10^{-17} J/bit in 2022 [31]. This corresponds to an annual energy efficiency improvement of 21%, so the value in 2015 can be approximately estimated as 1×10^{-16} J/bit. Therefore, the memory energy for a single phase shifter is 0.8 fJ/packet. The static power dissipation of an SRAM cell has been simulated as approximately 40 nW, leading to only 320 nW per phase shifter [32]. Therefore, the static power is neglected.

The share of DAC in total power consumption is much larger than that of the memory. A 12-bit DAC operating at 2.9 Gsps and supporting an output of 2.5 V_{pp} has been reported to dissipate a power of 188 mW [33]. The static power consumption is negligible at these clock frequencies, so this power is approximately proportional to the

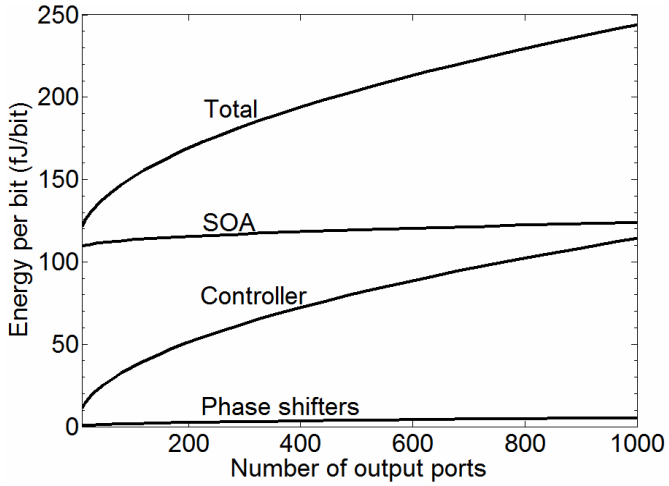


Fig. 6.7 Energy per bit of a monolithic cascade $1\times N$ phased-array switch with SOAs that compensate for the losses.

sampling rate. Under an assumption of 20% annual improvement of energy efficiency, an 8-bit DAC is estimated to consume 11.3 mW/Gsps in 2015. The sampling rate is inversely proportional to the packet length, so it is proportional to the bit rate in case of packets with equal size. Amplifiers are unnecessary with a DAC having these specifications because 2.5 V is sufficient to obtain a phase shift of 2π. Summing up all components, the energy per packet in the switch controller is

$$EPP_{ctrl} = \left(2AOR\sqrt{N}\right)\cdot\left(11.3\,pJ\right), \tag{6.13}$$

The left side of multiplication sign corresponds to the number of phase shifters operated and the expression on the right is the energy per packet to control a single phase shifter, which almost completely consists of the dynamic DAC power. From (6.13),

$$EPB_{ctrl} = AOR\sqrt{N}\cdot\left(2.26\,fJ\right) \tag{6.14}$$

is the energy consumed by the switch controller for a single payload bit.

6.3.1.4 Total Power Consumption in a Two-Stage $1\times N$ Phased-Array Switch with SOAs

The derivations above are combined together to derive the total power consumption. The energy efficiency of a monolithic $1\times N$ phased-array switch is plotted in Fig. 6.7 based on (6.7), (6.14), and Fig. 6.6-a. The energy per bit is independent of the bit rate

because all non-negligible power consumption terms are proportional to the bit rate under the assumption of packets with a certain number of bits. The power dissipated by the SOAs is dominant for small number of ports. Owing to the small dependence of the insertion loss on the number of ports, SOA power increases slowly with the port count compared to the switch controller power, which is proportional to the number of phase shifters. The dynamic power consumption of the phase shifters is negligible compared to the other factors. For a comparison between phased-array and broadcast-and-select switches, Fig. 6.7 can be directly compared to Fig. 6.6-b because broadcast-and-select switches are assumed to consume power only for the SOA gain. Under this assumption, a 1×1000 phased-array switch is five times as energy efficient as a broadcast-and-select switch with an equal number of ports.

6.3.2 Power Consumption of Complete *N*×*N* Optical Packet Switch with Buffers

In this section, the switch matrix and buffer architectures introduced in Section 6.2 are evaluated in terms of energy efficiency. The $N \times N$ switch consists of $2N$ identical $1 \times N$ switches already studied in Section 6.3.1. In an $N \times N$ switch, each packet is transmitted through two $1 \times N$ switches, so the power consumption of phase shifters and the switch controller in an $N \times N$ matrix switch is twice as much as the consumption in a $1 \times N$ switch. However, the relation is not linear for the SOAs if we maintain the condition of a certain SNR at the output. If M chips are cascaded, the signal power has to be approximately multiplied by M according to (6.12). The power consumed by the SOAs is proportional to M^2 because there are M times as many SOAs as a single chip on the light path. In this particular case, two $1 \times N$ switches are cascaded with two 1×21 switches for buffering. SOA power consumption is re-calculated under the condition of 30 dB SNR at the output of the OPS node.

The length of the longest optical fiber in the tunable buffer is inversely proportional to the bit rate. In case of a single wavelength channel with a bit rate of 40 Gb/s and a maximum buffer depth of 20 packets, the longest fiber should maintain a delay of 5 μs, which is equivalent to 1 km in space domain. Owing to the very low

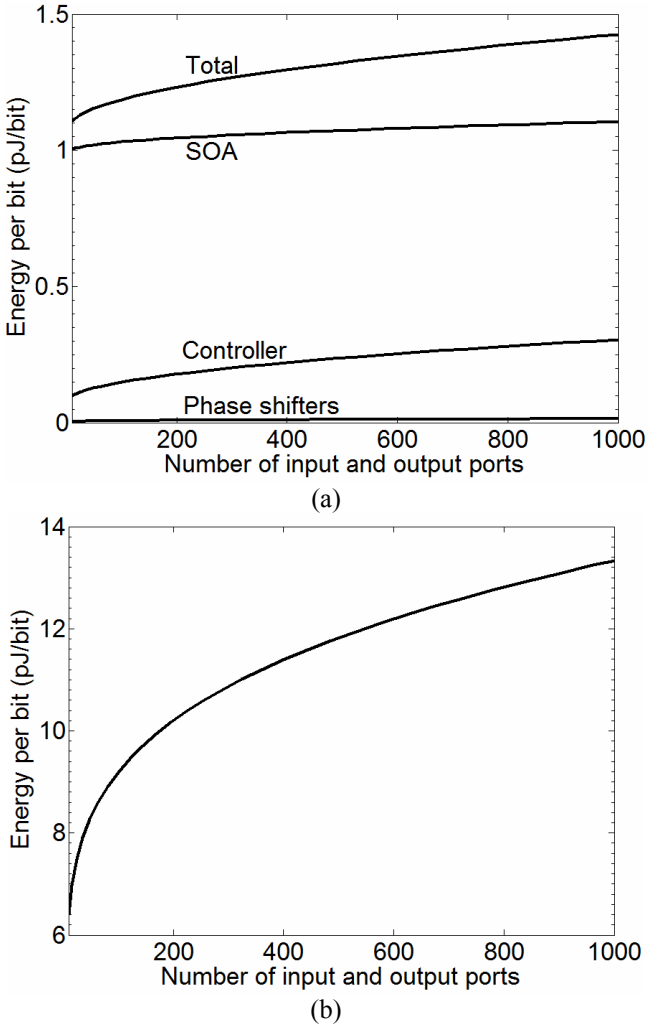


Fig. 6.8 Energy per bit of an $N \times N$ optical packet switch with buffers. The optical switches in the buffer and the matrix are (a) phased-array switches, and (b) broadcast-and-select switches.

propagation loss of the compact high refractive index fibers, fiber propagation loss is small compared to the 8.2 dB fiber-to-fiber loss of an integrated single-stage 1×21 switch. If phased-array switches are employed, the energy per bit in the buffer is in the 550-600 fJ/bit range as long as N is below 1000. This value is in the 2.1-3.6 pJ/bit range if broadcast-and-select switches are preferred. The dependence on the port count arises from the dependence of signal power on the number of ports, which influences the SOA power in the buffer.

All in all, the total energy dissipated by the $N \times N$ switch and the buffer to route a single bit of data is displayed in Fig. 6.8. For input and output port counts up to 1000, the energy per bit is less than 1.5 pJ/bit with phased-array switches and less than 13.8

pJ/bit if broadcast-and-select switches are utilized. This dramatic difference is caused by the high loss in the passive parts of the broadcast-and-select switches.

6.4 DISCUSSION AND CONCLUSION

We have studied the energy efficiency of optical packet switching routers incorporating integrated phased-array and broadcast-and-select photonic switches for both switching and tunable buffering. These two types of switches are promising because of their strict transparency and compatibility with WDM packets with arbitrary bit rates. Spanke architecture has been chosen to construct a nonblocking $N \times N$ switch with hundreds of connections necessary for high-throughput routers. In addition to the switch matrix, relatively large-capacity transparent tunable optical buffers are proposed based on $1 \times N$ transparent space switches and high-index-contrast fiber delay lines that combine compact size with low propagation loss.

The results of the analysis reveal that a 1000×1000 strictly transparent OPS router is expected to consume less than 1.5 pJ/bit if integrated phased-array switches are employed for routing and tunable buffering. On the other hand, OPS routers with the same architecture based on broadcast-and-select SOA gate array switches are close to ten times more power hungry than the former. Phased-array switching is a more power efficient solution owing to the low optical loss that has to be compensated for. The numbers derived in this analysis are not theoretical limits since the power consumption in SOAs, which is the dominant power consumption mechanism, can be reduced by assuming a more distributed approach with a larger number of lower-gain SOAs. The maximum data capacity of these hypothetical routers depends on the bit rate per fiber, which can increase freely as long as the payload is inside the operating spectrum of the switch. For example, considering that the 1-dB bandwidth of a phased-array switch is experimentally larger than 4.5 THz, payloads with bit rates above 1 Tb/s can be routed even without advanced modulation formats and polarization division multiplexing. A router with 1000 fibers at the inputs and outputs, each carrying 1 Tb/s has a maximum throughput of 1 Pb/s. According to the calculations in this paper, a buffered switch fabric of this scale has an estimated power consumption of only 1.47 kW. Since the

energy per bit increases as the number of ports increases, the power consumption of a given throughput reduces if the bit rate per fiber scales up. For example, a 1 Pb/s switch fabric with 250 input/output fibers, each carrying 4 Tb/s, consumes 1.25 kW, which is slightly lower than the value above. The effect of WDM switching on the power consumption is not very large according to these calculations. However, WDM switching offers other advantages, including latency, cost, size, and shorter delay line buffers.

Although these results are promising, the implementation of an optical router of this type requires the solution of several technological problems. Low-loss fiber coupling to hundreds or thousands of waveguides on a single chip is a challenging task not even tried so far. Temperature control power has been ignored in this analysis. The temperature dynamics have to be considered carefully to mitigate the thermal crosstalk in phased-array switches. Another important problem remaining is the uncertainty of the size of buffers required. This analysis is based on recent theoretical studies that claim that buffer sizes of only 10-20 packets are sufficient under certain circumstances. These claims have not been experimentally tested yet. Further studies on small-buffer routers are awaited to support the validity of this analysis.

REFERENCES OF CHAPTER 6

[1] S. J. B. Yoo, “Optical packet and burst switching technologies for the future photonic internet,” Journal of Lightwave Technology, vol. 24, no. 12, pp. 4468-4491, Dec. 2006.

[2] H. J. S. Dorren, N. Calabretta, and O. Raz, “Scaling all-optical packet routers: how much buffering is required?,” Journal of Optical Networking, vol. 7, no. 11, pp. 936-946, Nov. 2008.

[3] D. J. Blumenthal, “Optical packet switching,” in Proc. IEEE Lasers and Electro-Optics Society Annual Meeting, vol. 2, pp. 910-912, Nov. 2004.

[4] L. Stampoulidis, et al., “Enabling Tb/s photonic routing: development of advanced hybrid integrated photonic devices to realize high-speed, all-optical packet switching,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 14, no. 3, pp. 849-860, May/Jun. 2008.

[5] R. Beheshti, Y. Ganjali, R. Rajaduray, D. Blumenthal, and N. McKeown, “Buffer sizing in all-optical packet switches,” in Proc. Optical Fiber Communication Conference, Anaheim, CA, 2006, Paper OThF8.

[6] R. S. Tucker, “The role of optics and electronics in high-capacity routers,” Journal of Lightwave Technology, vol. 24, no. 12, pp. 4655-4673, Dec. 2006.

[7] R. S. Tucker, “Optical packet switching: a reality check,” Optical Switching and Networking, vol. 5, pp. 2-9, Mar. 2008.

[8] S. Aleksic, “Analysis of power consumption in future high-capacity network nodes,” Journal of Optical Communications and Networking, vol. 1, no. 3, pp. 245-258, Aug. 2009.

[9] V. Eramo and M. Listanti, “Power consumption in bufferless optical packet switches in SOA technology,” Journal of Optical Communications and Networking, vol. 1, no. 3, pp. B15-B29, Aug. 2009.

[10] Cisco CRS-3, http://ciscosystems.com/en/US/products/ps5763, Apr. 2010.

[11] Cisco Corporation, “Hyperconnectivity and the approaching zettabyte era,” white paper, Jun. 2009.

[12] H. Onaka, S. Kinoshita, and Y. Aoki, “WDM optical packet interconnection for petascale ultra-high-performance computing systems,” in Proc. Conference on Photonics in Switching, 2007, pp. 57-58.

[13] H. Furukawa, N. Wada, N. Takezawa, K. Nashimoto, and T. Miyazaki: “640 (2x32λx10) Gbit/s polarization- multiplexed, wide-colored optical packet switching achieved by polarization-independent high-speed PLZT switch,” in Proc. Optical Fiber Communication Conference, 2008, paper OTuL7.

[14] A. Schaham, B. A. Small, O. L. Ladouceur, and K. Bergman: “A fully implemented 12x12 data vortex optical packet switching interconnection network,” Journal of Lightwave Technology, vol. 23, no. 10, pp. 3066-3075, Oct. 2005.

[15] K. A. Williams, G. F. Roberts, T. Lin, R. V. Penty, I. H. White, M. Glick, and D. McAuley, “Integrated optical 2×2 switch for wavelength multiplexed interconnects,” IEEE Journal of Selected Topics in Quantum Electronics, vol. 11, no. 1, pp. 78-85, Jan./Feb. 2005.

[16] T. Tanemura, K. Takeda, and Y. Nakano, “Wavelength-multiplexed optical packet switching using InP phased-array switch,” Optics Express, vol. 17, no. 11, pp. 9454-9459, May 2009.

[17] L. V. Haul, S. E. Harris, Z. Dutton, and C. H. Behroozi, “Light speed reduction to 17 meters per second in an ultracold atomic gas,” Nature, vol. 397, no. 6720, pp. 594–598, Feb. 1999.
[18] Y. A. Vlasov, M. O’Boyle, H. F. Hamann, and S. McNab, “Active control of slow light on a chip with photonic crystal waveguides,” Nature, vol. 438, no. 7065, pp. 65–69, 2005.
[19] C. J. Chang-Hasnain, P. C. Ku, J. Kim, and S. L. Chuang, “Variable optical buffer using slow light in semiconductor nanostructures,” Proceedings of the IEEE, vol. 91, no. 11, pp. 1884–1897, Nov. 2003.
[20] J. B. Khurgin, “Optical buffers based on slow light in electromagnetically induced transparent media and coupled resonator structures: Comparative analysis,” Journal of Optical Society of America B, vol. 22, no. 5, pp. 1062–1074, May 2005.
[21] H. Furukawa, H. Harai, N. Wada, T. Miyazaki, N. Takezawa, and K. Nashimoto, “A 31-FDL buffer based on trees of 1x8 PLZT optical switches,” in Proc. 32nd European Conference and Exhibition on Optical Communication (ECOC 2006), Cannes, France, 2006, Paper Tu4.6.5.
[22] R. A. Spanke, “Architectures for guided-wave optical space switching systems,” IEEE Communications Magazine, vol. 25, no. 5, pp. 42-48, May 1987.
[23] L. A. Buckman, L. P. Chen, and K. Y. Lau, “Crosstalk penalty in all-optical distributed switching networks,” IEEE Photonics Technology Letters, vol. 9, no. 2, pp. 250-252, Feb. 1997.
[24] R. F. Kalman, L. G. Kazovsky, and J. W. Goodman, “Space division switches based on semiconductor optical amplifiers,” IEEE Photonics Technology Letters, vol. 4, no. 9, pp. 1048-1051, Sep. 1992.
[25] G. Appenzeller, I. Keslassy, and N. McKeown, “Sizing router buffers,” in Proc. SIGCOMM, 2004, pp. 281-292.
[26] N. Beheshti, Y. Ganjali, R. Rajaduray, D. Blumenthal, and N. McKeown, “Buffer sizing in all-optical packet switches,” in Proc. Optical Fiber Communication Conference, 2006, Paper OThF8.
[27] CIP Technologies, http://www.ciphotonics.com.
[28] L. Zhang, J. Sinsky, D. Van Thourhout, N. Sauer, L. Stulz, A. Adamiecki, and S. Chandrasekhar, “Low-voltage high-speed traveling wave InGaAsP-InP phase modulator,” IEEE Photonics Technology Letters, vol. 16, no. 8, pp. 1831-1833, Aug. 2004.
[29] M. J. Connelly. Semiconductor Optical Amplifiers. New York, NY: Kluwer, 2004, pp. 103-107.
[30] C. R. Doerr, L. Zhang, L. Buhl, V. I. Kopp, D. Neugroschl, and G. Weiner, “Tapered Dual-Core Fiber for Efficient and Robust Coupling to InP Photonic Integrated Circuits”, in Proc. Conference on Optical Fiber Communication, 2009, San Diego, CA, Paper OThN5.
[31] International Technology Roadmap for Semiconductors, http://www.itrs.net/Links/2007ITRS/Home2007.htm.
[32] G. Razavipour, A. A. Kusha, and M. Pedram, “Design and analysis of two low-power SRAM cell structures,” IEEE Transactions on VLSI Systems, vol. 17, no. 10, pp. 1551-1555, Oct. 2009.
[33] C. H. Lin, F. M. L. van der Goes, J. R. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, “A 12-bit 2.9 Gs/s DAC with IM3 < -60 dBc beyond 1GHz in 65 nm CMOS,” IEEE Journal of

Solid-State Circuits, vol. 44, no. 12, pp. 3285-3293, Dec. 2009.

CHAPTER 7
CONCLUSION

This thesis has focused on integrated phased-array photonic switches and their applications for optical packet switching. The questions that were initially intended to be answered were whether phased-array switches can exhibit good device characteristics, whether they have the scalability in terms of bit rate and number of physical connections, and whether these devices can satisfy the stringent requirements of optical packet switching. This thesis is based on the experiments in device, circuit and subsystem level supported by theoretical studies aimed to answer these questions. A brief summary of results and their interpretation are as follows.

The integrated phased-array switches designed and fabricated for an experimental evaluation of device characteristics demonstrated promising properties. First, an InP/InGaAsP 1×8 phased-array switch was designed and fabricated as a proof of concept for polarization- and wavelength-insensitive single-stage switching to 8 ports. The results of the experiments were in reasonable agreement with the calculations, exhibiting a wavelength dependent loss of 2.5 dB across an ultra-broad operational bandwidth of approximately 7.5 THz, and a polarization dependence below 2.2 dB mostly caused by the high polarization-dependent propagation loss in the waveguides. Based on the feedback obtained during the characterization of this device, a 1×16 phased-array switch was designed and fabricated in order to achieve in a low-loss switch that could be deployed in optical packet switching experiments and confirm the scalability of phased-array switching scheme by demonstrating the first monolithic semiconductor photonic switch capable of routing to 16 output ports. This device verified the expectations very well with an on-chip loss below 7 dB to all ports, an average extinction ratio of 18.8 dB, and complete dynamic operation with a reconfiguration time on the order of a few nanoseconds. The dynamic characteristics

were comparable to the static ones. Higher-order modes, aberrations of waveguides and star couplers, and electrical crosstalk between phase shifters are estimated to be the mechanisms that reduce the extinction ratio. The readers are advised to focus on these problems if a higher extinction ratio is desired.

In addition to experimental research on phased-array switches, a novel type of amplitude-controlled phased-array switch was proposed for multicast switching. The amplitude control in the array plane along with phase control increases the degree of freedom dramatically. This device can switch a single signal to arbitrary combinations of multiple output ports in principle. The amplitude control also makes it possible to regulate the output power of the device. The basic principle of operation of amplitude-controlled phased-array switches has also been explained in this thesis for the first time. This device can find applications related to multicast switching in communication networks.

The optical packet switching performance of phased-array switches was also tested completely for the first time in this thesis. A simplified optical packet switching node comprising a multi-port phased-array switch, a switch controller and an all-optical label processor for parallel labels was built. Packets with different bit rates (160-Gb/s OTDM and 120-Gb/s WDM) and modulation formats (OOK and DPSK) were routed through the node with very low power penalties. These experiments have confirmed that this switch is insensitive to the modulation format and bit rate of payloads. This is a natural consequence of the strict transparency and flat spectral response of the switch in a broad wavelength band. These results are very encouraging because not only are modulation-format agnostic optical packet switching experiments very rare in the literature, but also does this switching scheme support relatively large number of ports. Spectrally efficient payloads that carry data of several Tb/s can be routed by this switch in principle. This leads to a data capacity on the order of tens of Tb/s if the 1×16 switch is deployed as the building block of a matrix switch.

Furthermore, an advanced photonic integrated circuit (PIC) comprising hundreds of monolithic active and passive devices was reported in this thesis. This PIC has a potential for monolithic switching to 100 outputs, which makes it by far the largest-scale semiconductor integrated photonic switch in the literature. The preliminary measurements on the PIC have led to promising results, including an extinction ratio

over 50 dB, an on-chip loss below 15 dB, and efficient phase shifters ($I_{2\pi}$ < 1.5 mA) and SOAs (extinction ratio > 40 dB with a current of 100 mA) despite the non-ideal offset quantum well technique. A power penalty less than 1 dB was also measured with a 10-Gb/s modulated signal. PICs of this type are necessary for low-cost, compact and low-power implementation of ultra-high-capacity optical packet switching. If the port count of this chip and bit rate potential of transparent ultra-broadband operation are combined, an unparalleled data rate capacity can be achieved.

Finally, the power consumption of optical packet switching fabrics utilizing phased-array switches has been analyzed. This is a semi-empirical, semi-theoretical analysis based on state-of-the-art photonics and electronics technologies. Large-scale PICs similar to the one mentioned in the previous paragraph were assumed to be used for both routing and transparent tunable buffering. The energy consumed by a hypothetical 1000×1000 router, including the power consumed by the switches, switch controller and the SOAs to compensate for the losses, was calculated to be less than 1.5 pJ/bit. Note that this number is not the physical limit, but is based on present and near future device characteristics. Routers based on phased-array switches were found to be significantly more power efficient (e.g. close to 10 times more efficient in case of 1000×1000 switching) than those based on broadcast-and-select switches, the most commonly used transparent switch employed in optical packet switching experiments. The energy efficiency gap between phased-array optical packet switching and optical/electrical/optical switching is even larger although a precise comparison cannot be done.

These results and interpretations form a self-consistent analysis of the feasibility of optical packet networks using phased-array switches. The final single-statement conclusion is as follows. Energy-efficient optical packet routers with Pb/s-scale throughput are realistic owing to the port-count scalability of integrated phased-array switches, the potential for large-scale photonic integration, and the compatibility of these switches with high-bit-rate packets based on advanced modulation formats. This conclusion is very promising, but there are several technical challenges that have to be overcome by researchers before reaching this goal. These technical challenges are listed next.

- implementing phased-array switches with response time in the picoseconds

range in order to switch high-bit-rate packets with very short guard times;

- suppressing the electrical crosstalk between large number of phase shifters in large-scale switches;
- improving the optical extinction ratio by a more controlled fabrication process with single-mode waveguides and mitigating the effects of thermal crosstalk;
- simultaneous coupling of waveguide modes to hundreds or even thousands of fibers from large-scale photonic integrated circuits.

Most of the points in the list above are generally related to the level of large-scale photonic integration technology, which is still in its infancy. The advancement of photonic integration technology is strongly dependent on the market size of its applications since research and development on these technologies require large amounts of investment. Optical packet switching based on phased-array switches may be one of these applications to validate the investment on photonic integration.